ULTRA LOW POWER CMOS RECTIFIER DESIGN FOR RADIO FREQUENCY ENERGY HARVESTING SYSTEMS USING SELF-BODY-BIASING TECHNIQUES

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FACULTY OF ENGINEERING
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THESIS SUBMITTED IN FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

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ORIGINAL LITERARY WORK DECLARATION

Name of Candidate: AMIN KHALILI MOGHADDAM

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Field of Study: ELECTRONICS

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ABSTRACT

The internet of things (IoT) technology has recently gone through a significant evolution and the obsession in this field is due to its ability to simultaneously connect and remotely control any physical objects. The IoT usually incorporates radio frequency identification (RFID) systems and other schemes which enable automated object identification in numerous applications such as environmental monitoring, object tracking, contact-less identification, and implantable medical device (IMD). Such systems commonly use wireless power transfer techniques for the purpose of operation. An integrated radio frequency energy harvesting (RFEH), which adopts a viable and efficient technique, is responsible for capturing sufficient power for the above-mentioned applications. The performance of the RFEH system relies on the performance of the integrated rectifier in order to operate with high efficiency. In this work, a symmetric differential-drive cross-coupled bridge (DDCCB) rectifier structure is proposed for far-field RFEH systems with the capability of capturing radio frequency (RF) signals and converting into a positive and a negative direct current (DC) voltage at the output. Four self-body-biasing techniques are proposed without requiring any additional or auxiliary circuits using local nodes in the structure. Only one of the proposed techniques illustrates a significant improvement in simulations which is referred to as lower dc feeding (LDCF) technique in this work. The proposed self-body-biasing technique has been implemented in a double-rail three-stage configuration with identical design parameters with the conventional self-body-biasing technique which is referred to as source-to-body (SB) biasing technique in this work. The SB and the LDCF rectifiers were fabricated in a standard 130 nm CMOS process and compared at the operation frequency of 500 MHz, 953 MHz and 2 GHz along with a corresponding load of 2 kΩ, 10 kΩ and 50 kΩ. The LDCF technique allows the p-type transistors to operate

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with a dynamic threshold voltage (V_{th}) which improves the power conversion efficiency (PCE) when the rectifier is operating at a smaller received power. A 9.5% of maximum improvement is achieved at the peak PCE when the rectifier is operating at 953 MHz, and driving a 10 kΩ load. A maximum PCE of 73.9% is measured at 2 GHz when the rectifier is driving a 2 kΩ load. The LDCF technique also offers a self-limiting capability for its output voltage, by reducing the PCE at larger received power. A limiting voltage level of 3.5 V is measured irrespective to the operating frequency and load. This capability aids the protection of the subsequent circuits in a wireless sensor from being overpowered.

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ABSTRAK

Teknologi Internet of Things (IoT) baru-baru ini melalui evolusi ketara dan obsesi dalam bidang ini adalah disebabkan oleh keupayaannya untuk menyambung secara serentak dan mengawal dengan sebarang objek fizikal dari jauh . IoT biasanya menggabungkan sistem Pengenalan Frekuensi Radio (RFID) dan skim lain yang membolehkan pengenalan objek automatik dalam pelbagai aplikasi seperti pemantauan alam sekitar, pengesanan objek, pengenalan tanpa sentuh, dan peranti perubatan boleh diimplan (IMD). Sistem seperti ini biasanya menggunakan teknik pemindahan kuasa tanpa wayar untuk tujuan operasi. Penuaian tenaga frekuensi radio bersepadu (RFEH), yang mengamalkan teknik yang berdaya maju dan cekap adalah, bertanggungjawab dalam mengumpul kuasa yang mencukupi untuk aplikasi tersebut di atas. Prestasi sistem RFEH bergantung kepada prestasi penerus bersepadu untuk beroperasi dengan kecekapan yang tinggi. Dalam kajian ini, satu struktur penerus simetri jambatan pemacu-pengkamiran silang-pasang (DDCCB) adalah dicadangkan untuk sistem RFEH jauh-jarak dengan keupayaan mengumpul isyarat Frekuensi Radio (RF) dan menukar kepada arus terus (DC) positif dan negatif voltan pada keluaran. Empat teknik pincangan badan-diri dicadangkan tanpa memerlukan sebarang litar tambahan sebaliknya menggunakan nod tempatan dalam struktur. Hanya salah satu teknik yang dicadangkan menunjukkan peningkatan yang ketara dalam simulasi dan ia dinamakan sebagai teknik penyuapan dc rendah (LDCF) dalam penyelidikan ini. Teknik pincangan badan-diri yang dicadangkan itu telah dilaksanakan dalam konfigurasi dua landasan tiga peringkat dengan parameter reka bentuk yang serupa dengan teknik pincangan badan-diri konvensional yang disebut sebagai teknik pincangan sumber-ke-badan (SB) dalam penyelidikan ini. Penerus-penerus SB dan LDCF telah dihasilkan dalam proses CMOS 130nm yang standard dan dibandingkan pada frekuensi operasi 500 MHz, 953

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MHz dan 2 GHz beban sepadan 2 kΩ, 10 kΩ dan 50 kΩ. Teknik LDCF membolehkan jenis-p transistor untuk beroperasi dengan voltan ambang (V_{th}) yang dinamik dimana ia boleh meningkatkan kecekapan penukaran kuasa (PCE) apabila penerus beroperasi dengan kuasa yang diterima yang lebih kecil. Peningkatan maksimum setinggi 9.5% dapat dicapai pada PCE puncak apabila penerus beroperasi pada 953 MHz, dan memacu beban 10 kΩ. PCE maksimum setinggi 73.9% diukur pada 2 GHz apabila penerus memacu beban 2 kΩ. Teknik LDCF juga menawarkan keupayaan pengehadan-diri untuk voltan keluaran, dengan mengurangkan PCE pada kuasa penyambutan yang lebih besar. Tahap voltan pengehadan setinggi 3.5 V diukur tanpa mengira frekuensi operasi dan beban. Keupayaan ini membantu dalam melindung litar berikutnya di penderia tanpa wayar daripada kelebihan kuasa.

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LIST OF SYMBOLS AND ABBREVIATIONS

AC	:	alternating current.
BJT	:	bipolar junction transistor.
CMOS	:	complementary metal-oxide-semiconductor.
DB	:	drain-to-body.
DC	:	direct current.
DDCCB	:	differential-drive cross-coupled bridge.
DNW	:	deep n-well.
DUT	:	device under test.
DVTS	:	dynamic voltage-threshold scaling.
EH	:	energy harvesting.
EIRP	:	effective isotropic radiated power.
ESD	:	electrostatic discharge.
FCC	:	federal communications commission.
FFNC	:	far-field non-coupling.
FR4	:	flame retardant 4.
GPS	:	global positioning system.
HBT	:	hetero-junction bipolar transistor.
HEMT	:	high-electron mobility transistor.
Hybrid-DCF	:	hybrid DC feeding.
IC	:	integrated circuit.
IHDCF	:	identical higher DC feeding.
IMD	:	implantable medical device.
IoT	:	internet of things.
JFET	:	junction field effect transistor.
LDCF	:	lower dc feeding.
LDO	:	low drop out.
MESFET	:	metal-semiconductor field effect transistor.
MIM	:	metal-insulator-metal.
MMID	:	millimeter identification.
MOSFET	:	metal-oxide-semiconductor transistor.
NFNRC	:	near-field non-resonant coupling.
NFRC	:	near-field resonant coupling.
PCB	:	printed circuit board.
PCE	:	power conversion efficiency.
PDK	:	process design kit.
PNA	:	power network analyzer.
PSA	:	power signal analyzer.
PSG	:	power signal generator.

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RF	:	radio frequency.
RFEH	:	radio frequency energy harvesting.
RFID	:	radio frequency identification.
SB	:	source-to-body.
SDCF	:	symmetric DC feeding.
SoC	:	system on chip.
UHF	:	ultra high frequency.
V_{th}	:	threshold voltage.
VNA	:	vector network analyzer.
WiFi	:	wireless fidelity.
WPT	:	wireless power transfer.

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CHAPTER 1: INTRODUCTION

1.1 Introduction to energy harvesting

The dramatic increase in the world population and its implications on energy cost encourage the world to employ other alternatives such as green energy sources. Energy harvesting (EH) as a long term solution, which preserves the natural resources and improves the global economy, can be considered as a suitable source (Vullers, van Schaijk, Doms, Hoof, & Mertens, 2009).

The main aim of adopting EH systems is to allow electronic devices in the wearable and identification systems to be battery-free and self-powered using scavenging ambient or environmental energy, where integrating a battery is not an optimal solution. The application of EH systems stretches from structural health monitoring to identification and tracking systems such as RFID or millimeter identification (MMID) (Niell Elvin, 2013). For instance, self-powered sensors, which are mostly used in embedded and microsystems, are able to function constantly for a long period of time without requiring to be connected to any power-lines or even a battery, which obviates the need of battery replacement routine. To be concise, EH technology has considerably enhanced the low-power sensor applications, and it is still under development. As EH systems are evolving, power consumption in integrated circuits (ICs) requires to be relatively reduced in order to allow designers and engineers to obtain more functionality with the applications of EH technology.

The variation of free energy from the environment that EH systems usually capture, can be simply categorized into 4 major groups. First, energy from the light, which can be extracted from sunlight along with indoor and outdoor lighting. This type of energy is usually converted into electricity energy by photoelectric cells such as solar cells.

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Vibrations and movements of any object can also be converted into electricity energy by piezoelectric materials, which the source of energy is mechanical as the second group. Heat or thermal energy is also converted into electricity in the form of electric current via specific semiconductors and metals with a large Seeback coefficient. A material with a large Seeback coefficient is able to transform a temperature difference into an electric energy to some extent. The last group of the energy source is electromagnetic and RF waves energy. With the fast growing pace of technology especially in the field of telecommunications, RF radiation has recently become more ubiquitous. However, the intended receivers consume only small amount of RF energy and the rest is wasted in the environment (Squires, 2015).

The most important performance measuring parameter of an EH system is the efficiency, which can be defined as the ratio of the DC power at the output and the available power at the input. Among all the energy source groups, which are freely available in our environment, light energy is the most pervasive source but light energy harvester systems present considerably low efficiency [around 10% (Jingbi You & Yang, 2013)]. In addition, light energy harvesting systems are only able to operate during day time, and in the absence of the sun light the harvesters will not be able to provide any energy. Thermo-electric energy harvesting systems, which use heat energy, also requires a persistent temperature difference to be able to reach to its maximum efficiency, which is relatively low. For instance, the system is only able to operate with a 20% efficiency (Knight, Davidson, & Behrens, 2008) for a temperature difference of 100 C°. Furthermore, harvesting energy through piezoelectric relies on a continuous vibration frequency without interruption to achieve a relatively acceptable conversion efficiency (Drayson, 2015). On the other hand, RF energy harvesting systems are able to operate with a comparatively high conversion efficiency (Hsieh, Chou, & Chiang, 2015).

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Performance of the RFEH system relies on the level of RF power density. Power density at the input of the RFEH system varies from 0.01 μW/cm^2 to 300 μW/cm^2, and in some cases the density even reaches 1000μW/cm^2, depending on the application of the system. Unlike the other energy sources, RF signals are deliberately generated and regulated. The fast growth in the field of telecommunications and radio technologies is causing the radio spectrum to become significantly populated by television, radio, cellular, global positioning system (GPS), wireless fidelity (WiFi), satellite and radar signals. For each communication system, a frequency band is dedicated with associated standard and regulations about their implementations and allowable transmitting RF power (Drayson, 2015).

Power consumption is another parameter that determines the application of an RFEH system. Fig.1.1 depicts the power consumption of typical applications that adopt EH technology. The power consumption for the applications that apply RFEH system is usually between 100 nW and 1 mW.

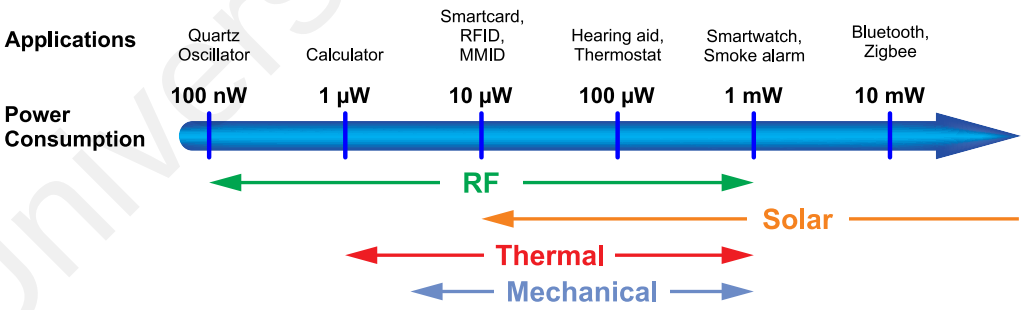

Figure 1.1: Power consumption of the applications adopting EH system.

1.2 Motivation

The mobile network industry is developing and growing rapidly due to the extreme demands for smart-phones, tablets, mobile broadband access and social network applications. Mobile operators occupy a wide range of frequency bands spanning from 450 MHz to

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3.5 GHz. Moreover, the number of devices equipped with WiFi is growing where the operating frequency range is between 2.4 and 5.9 GHz. Consequently, RF power density will increase year on year and rapidly expanding the number of devices powered by free ambient RF energy. RFEH systems are also the most promising solutions for the IoT technology where RFEH systems are considered as a commonly applicable power source for anticipated 26 billion devices with $300 billion industry investment by 2020 (Drayson, 2015). That is to say, energy harvesting from this band of frequency is highly important, and more efforts are required to enhance this technology.

1.3 Problem statement

The efficiency and the DC output voltage are the important factors that determine the performance of an RFEH system. The efficiency and DC output voltage of an RFEH system are strongly dependent on the capability of the antenna in capturing the RF power, the matching network accuracy at the selected frequency range, and the number of switching devices. The efficiency of the switching devices, which form a complete RF-to-DC converter, also extremely affect the overall efficiency of the system. The RF-to-DC converter is also generally referred to as a rectifier. A typical block diagram of an RFEH system for a wireless sensor node is depicted in Fig. 1.2. The voltage limiter prevents the connected application from being overpowered and a low drop out (LDO) regulator provides a stable DC voltage for the application.

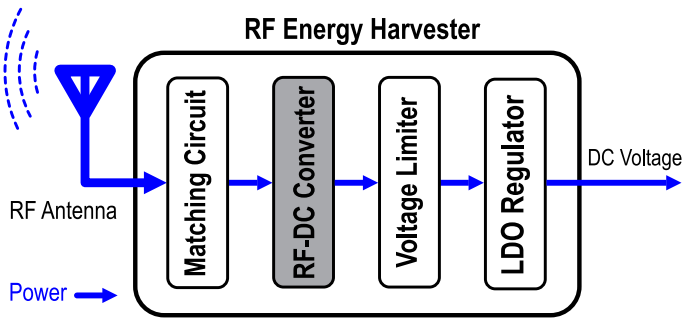

Figure 1.2: Block diagram of a typical RFEH system.

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In an RFEH system, threshold voltage or voltage drop of the switching devices (metal-oxide-semiconductor transistor (MOSFET) transistors or diodes) in the rectifier significantly affects the performance of the system. A rectifier with a lower threshold MOSFET or a lower voltage drop diode is able to operate with lower input power levels and provides a larger DC output voltages (J. Dickson, 1980; Papotto, Carrara, & Palmisano, 2011).

Among different structures and configurations for the rectifier, the (differential-drive cross-coupled bridge) DDCCB structure has outperformed the other rectifier configurations in terms of efficiency. It should be noted that a DDCCB rectifier requires to be driven by a differential RF signal. Since the body-source voltage affects the threshold voltage, the transistors are able to operate with a dynamic threshold voltage by changing the body-source voltage.

Adopting a symmetric RF power harvester with the ability of generating a positive and a negative DC voltage at the output, increases the rectification efficiency, alleviates the non-linearity of input resistance, and allows the system to be more efficient at the antenna. Furthermore, a rectifier with the symmetric supplying ability prepares a condition for the succeeding analog circuits to be more flexible and efficient (Ashry, Sharaf, & Ibrahim, 2009). However, a symmetric rectifier configuration using DDCCB structure has not been introduced yet even though the DDCCB structure offers a high conversion efficiency.

1.4 Research aim and objectives

The aim of this thesis is to design a highly efficient DDCCB rectifier for RF energy harvesting system with the ability of generating a symmetric DC voltage and self-body-biasing capability. The objectives of this research include:

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1. To identify the critical performance parameters for rectifier design based on DDCCB structure.

2. To design a novel and high efficiency DDCCB-based rectifier with following features:

    a) Generating a symmetric DC voltage at the output.

    b) Operating with a scalable V_{th} for the integrated p-type MOSFET transistors.

    c) Adopting a self-body-biasing technique.

    d) Output self-limiting capability in terms of DC voltage.

3. To verify the proposed rectifier configuration through fabrication and measurement of the performance parameters.

1.5 Research Scope

The scope of this thesis is the DDCCB-based rectifier design at an operating frequency range between 500 MHz and 2 GHz while driving a variable load between 2 kΩ and 50 kΩ in a standard complementary metal-oxide-semiconductor (CMOS) fabrication process.

1.6 Thesis organization

This thesis is organized as follows: an exhaustive literature review with basic concepts and a general block diagram of RFEH is presented in Chapter 2 along with theory of scattering parameters. In Chapter 3 four symmetric DDCCB rectifiers are proposed with self-body-biasing capability. The methods and techniques that have been utilized to verify the proposed rectifier structures are presented in Chapter 4. The simulation and measurement results, and the performance of the proposed rectifier structures are discussed in terms of performance parameters and the selected proposed rectifier structure is compared to other state-of-arts in Chapter 4 as well. Finally this thesis is concluded in Chapter 5 with a

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suggestion for future work.

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CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

In this chapter, a review of RFEH system is presented following with a short history of the rectifier evolution and the reported state-of-the-art configurations. It also compares the rectifier configurations in terms of performance and identifies the important performance and design parameters. The operation mechanism of the DDCCB rectifier for RFEH systems will be explained in detail. Finally, theory of scattering parameters for the characterization of the DDCCB rectifier will be presented.

2.2 MOSFET transistors

The development of the solid-state transistor is one of the most influential invention in the 20th century. The implementation of almost all modern day electronic devices relies on this device. Most of the circuits in RFEH systems are not exempted from this reliance including the rectifier.

The transistors in RF and microwave electronic devices or applications are usually classified into following groups: junction transistors such as bipolar junction transistor (BJT) and hetero-junction bipolar transistor (HBT), and field-effect transistors such as junction field effect transistor (JFET), metal-semiconductor field effect transistor (MESFET), high-electron mobility transistor (HEMT), and MOSFET. An appropriate type of technology for implementation of transistors can be selected by the characteristics of the application (Maas, 1998). The electronic devices that adopt MOSFET transistors offer an enhanced performance than of that JFETs but relatively lower than MESFETs. The operation mechanism of both MOSFET and JFET transistors are comparable but MOSFET offers better precision in terms of the gate size in the fabrication process. Moreover, the gate of MOSFET transistors can be shorter compared to the JFET transistors. Although

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the performance of MOSFET is relatively mediocre to some extent than MESFET, it is considerably more cost efficient for the electronic devices operating at up to 10 GHz. An integrated circuit using MOSFETs, both n-type and p-type, can be implemented using a standard CMOS fabrication process.

CMOS technology has been growing rapidly with no realistic bottleneck and has already become a leading technology since it allows large and complex circuits to be miniaturized, and defines system on chip (SoC). The seeds of CMOS technology were planted in the early 1930s by (Edgar, 1930) with introducing the field-effect device concept. However, it took more than 30 years to implement and make the concept become practical. The development of the CMOS technology, which uses the concept of field-effect device, started in the 1960s with enhancement of silicon dioxide. Since then, the CMOS technology has been under rapid development (Foty, 2004).

In n-type MOSFET transistors, the gate is required to be a good conductor, which in modern technologies poly-silicon material is selected to build the gate of MOSFET transistors. Silicon dioxide, or in short "oxide", is used as a dielectric layer and sandwiched between the gate and the substrate. The performance of the transistor is significantly under influence of the dielectric layer. The source and the drain are made of $n+$, which are referred to as diffusion regions. It should be noted that the drain and the source regions build PN junctions with the p-type substrate. To avoid substrate leakage the diodes built by the PN junctions are usually required to be in reverse-biased. However, the parasitic capacitance of depletion region associated to the two diodes must be taken into consideration. Fig.2.1(a) depicts general dimensions of today's MOSFET transistors. L is the length and W is the width of transistor (Razavi, 2008).

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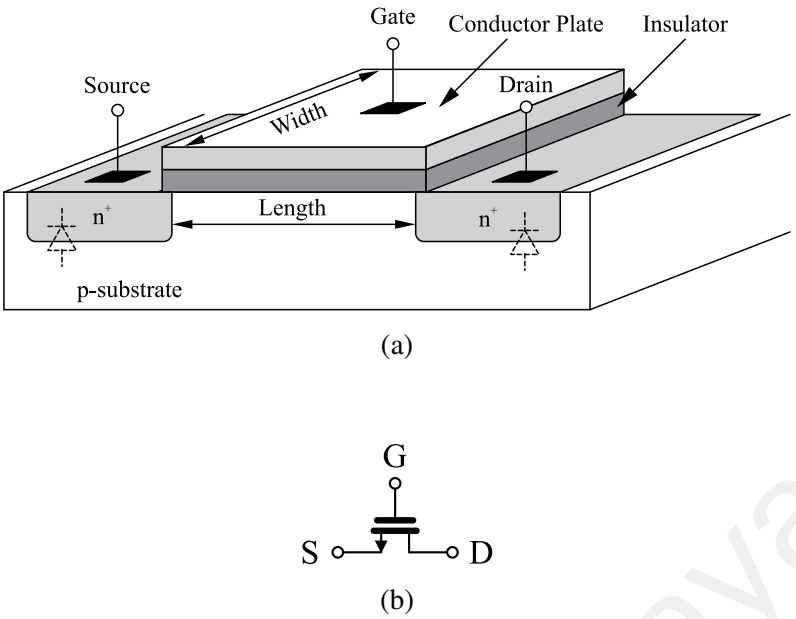

Figure 2.1: n-type MOSFET a) Physical cross section view. b) Symbolic representation.

2.2.1 Operating regions/modes of an n-type MOSFET transistor

An n-type MOSFET transistor operates in three regions of operation. When gate-source voltage is smaller than threshold voltage (V_{th}), which is the minimum voltage that a MOSFET transistor requires to build a channel between its source and drain ($V_{gs} < V_{th}$), the transistor is in "cutoff" mode, and theoretically no conduction exists between the drain and the source. However, in reality, a weak conduction exists between the drain and the source, which is referred to as weak inversion and the transistor is in sub-threshold mode.

When V_{gs} is larger than V_{th} and the drain-source (V_{ds}) voltage is larger than $V_{gs} - V_{th}$, which is referred to as overdrive voltage, a channel between the drain and the source is established and the transistor operates like a resistor controlled by V_{gs}. This mode of operation is called triode or linear mode. In triode mode of operation, the drain current can be obtained by

$$I_D = \frac{1}{2}.\mu_n.C_{ox}.\left(2(V_{gs} - V_{th}).V_{ds} - V_{ds}^2\right) \tag{2.1}$$

where C_{ox} denotes the gate capacitance per unit and μ_n is the mobility of electron for n-type.

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When $V_{gs} > V_{th}$ and $V_{ds} > V_{gs} - V_{th}$, the transistor operates in the saturation (or active) mode in which the channel between drain and source has been created but due to the large electric field between the drain and the source, the drain current is less under control of the gate-source voltage and can be expressed as:

$$I_D = \frac{1}{2}.\mu_n.C_{ox}.\frac{W}{L}.\left(V_{gs} - V_{th}\right)^2 \tag{2.2}$$

For more advanced technologies and higher operating frequencies, the effect of channel-length modulation should be taken into account. Hence, equation (2.2) should be modified as

$$I_D = \frac{1}{2}.\mu_n.C_{ox}.\frac{W}{L}.\left(V_{gs} - V_{th}\right)^2.\left(1 + \lambda V_{ds}\right) \tag{2.3}$$

where λ is the channel-length modulation coefficient factor. In a standard CMOS technology and for operating frequency below 10 GHz, it is assumed that λ=0.

2.2.2 Sub-threshold leakage current

When the gate-source voltage is below V_{th}, the drain current is supposed to be zero. However, a small current exists and can flow between the source and the drain, and the current can be expressed by (Burasa, Constantin, & Wu, 2014)

$$I_D = I_0.\frac{W}{L}.\left(e^{V_{gs}/n.V_T}\right).\left(1 - e^{-V_{ds}/n.V_T}\right).\left(1 + \lambda V_{ds}\right) \tag{2.4}$$

where V_T is the thermal voltage and n is the sub-threshold region swing parameter and I_0 is a process dependent, which is experimentally achievable.

Since the supply voltage of MOSFET transistors are continuously scaled down with the advancement in the fabrication technologies, the effect of sub-threshold conduction is also becoming more imperative since the amount of sub-threshold conduction is de-

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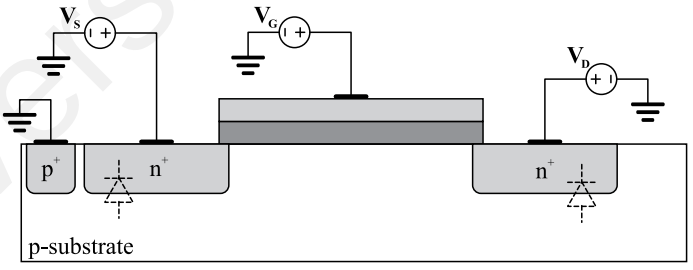
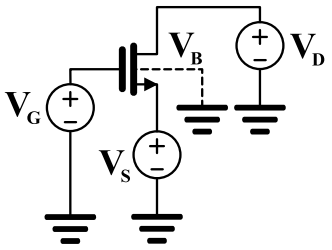
termined by the V_{th}, which is between supply voltage and ground. Hence, sub-threshold conduction is required to be minimized in order to both reduce the dynamic power consumption and maintain electric fields of the integrated circuits as low as possible to preserve device reliability (Soudris, Piguet, & Goutis, 2002).

2.2.3 Body effect

It is often assumed that the source and the substrate, also called the "bulk" or the "body", are tied to ground for n-type MOSFETs, and to the highest available voltage for p-type MOSFETs. The structure of a p-type MOSFET will be explained in Section 2.2.5. However, the source-to-body configuration can be changed where a dynamic V_{th} is required. If the source is supplied with a positive voltage while the substrate is still tied to the ground, the configuration in Fig.2.2, the diode (PN junction) between the source and the substrate remains in reverse-biased and the transistor operates properly since the leakage current is effectively suppressed. The dotted line amended to the symbol of the transistor represents the body terminal in the n-type MOSFET transistor and V_{sb} denotes the voltage difference



(a)



(b)

Figure 2.2: n-type MOSFET including the body terminal a) Physical cross section view. b) Symbolic representation.

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between the source and the body. As V_{sb} departs from zero, the V_{th} of the transistor changes. To be more precise, as the source potential increases with respect to the body potential, V_{th} of the transistor increases, which is referred to as "body effect". The body effect of a n-type MOSFET can be formulated as (Razavi, 2008)

$$V_{thN} = V_{th0N} + \gamma \left(\sqrt{|2\Phi_F + V_{sb}|} - \sqrt{|2\Phi_F|} \right) \tag{2.5}$$

where V_{th0N} is the threshold voltage of the transistor while the source-body potential is zero, γ is the body effect coefficient, $2\Phi_F$ is the surface potential coefficient, and γ and $2\Phi_F$ are fabrication-dependent parameters.

2.2.4 MOSFET device capacitances

The capacitances of the MOSFET device is usually considered as parasitic factors in most analog circuits. These parasitic capacitances associated with the MOSFET device should also be taken into consideration especially when the circuit is required to operate at high frequency. Since an RFEH system is sometimes required to operate at high frequencies, the effect of the parasitic capacitances should be taken into account. Between each pair of the MOSFET terminals, a capacitance exists, which the value of the capacitance might depend on the biasing conditions of the transistor. It should be noted that the source-to-

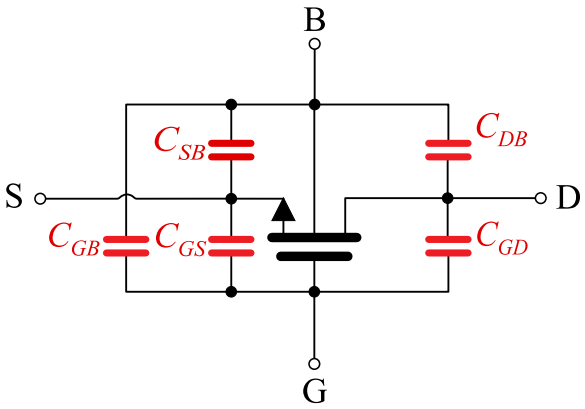

Figure 2.3: MOSFET capacitances.

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drain capacitance is negligible. Fig.2.3 illustrates the parasitic capacitances of an n-type MOSFET transistor (Razavi, 2008).

2.2.5 p-type MOSFET transistor

In most CMOS technologies, the p-type and the n-type MOSFET transistor exhibit comparable DC and alternating current (AC) properties; however, some differences in the properties exist. The transconductance parameter of a p-type MOSFET is relatively smaller by the factor between $1/2$ and $1/3$ compared with a n-type MOSFET. In addition in a standard CMOS technology with p-type substrate and n-type well, the body terminal of the p-type MOSFET is electrically isolated since the transistor is made in an implanted n-well as depicted in Fig.2.4. In modern analog circuits, a good use of this capability can be made to mitigate the body effect in electronic devices. Another difference is that for low values of the body bias, the p-type MOSFET exhibits a smaller incremental body

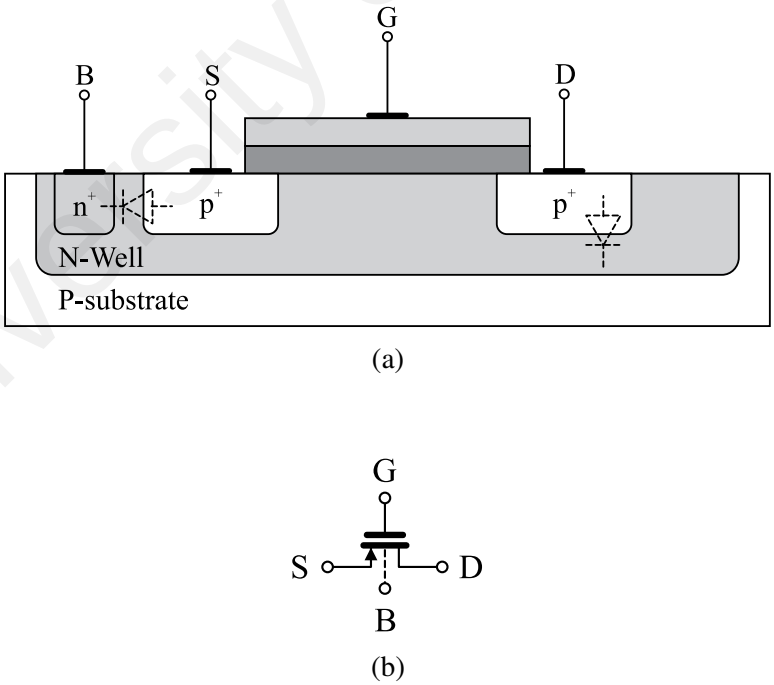

Figure 2.4: p-type MOSFET a) physical cross section view. b) symbolic representation.

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effect and for larger values of the body bias, the incremental body effect is larger. If the n-type is chosen for the substrate, this capability comes with n-type MOSFET. In standard CMOS technologies either n-type or p-type well is chosen for the substrate. Hence, only one type of MOSFET is able to offer this isolation capability depending on the selected substrate type (Gray, 2009).

To be able to electrically isolate the body terminal of n-type MOSFET in a standard CMOS technology with p-type substrate, deep n-well (DNW) fabrication process is commonly used. Fig.2.5 illustrates the structure of a n-type MOSFET structure with p-type substrate process. It should be noted that in the DNW structure, body no longer represents the substrate, and it is completely isolated from the substrate, which alleviate the substrate power loss.

2.3 RFEH system description

An RFEH system is capable of capturing and converting received RF signals into electricity in the form of DC voltage, which is a promising solution to wireless devices that face constrains in the power or energy such as RFID and wireless sensor networks. These constrains in power limit the devices' lifetime, which considerably confines the performance of the wireless devices. Conversely, an RFEH system offers a sustainable power supply from radio frequency sources. Hence, the RFEH is capable of providing a reliable power for wireless devices by capturing and harvesting RF signals for the purpose of

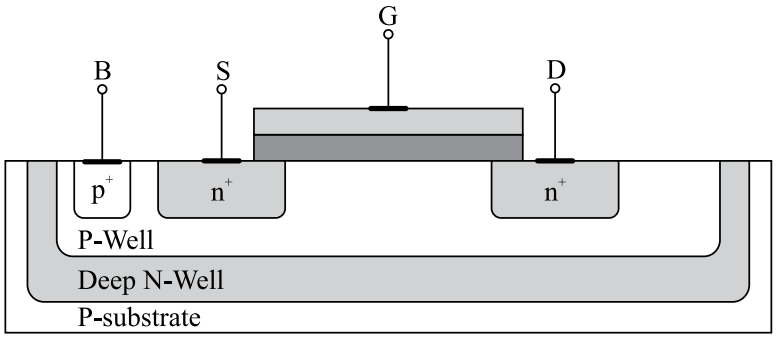

Figure 2.5: n-type MOSFET transistor structure with DNW implementation

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communication and information processing. As a result, RFEH systems have become prominent in various applications (Lu, Wang, Niyato, Kim, & Han, 2015) .

In RFEH systems, the source of energy can be categorized into two groups. First, ambient RF sources such as TV broadcasting, WiFi, Bluetooth, and cellular network with frequency range of 0.2-2.4 GHz. Ambient RF sources are not preferred to be used for wireless power transfer due to the low power density (Mishra et al., 2015). However, few technical studies reported in harvesting limited energy from ambient RF sources for specific applications (Piñuela, Mitcheson, & Lucyszyn, 2013).

On the other hand, dedicated RF sources, which employ directional transmission technique, exhibit comparatively higher power density. Dedicated RF sources are mainly used to supply wireless sensor nodes since they are fully controllable. The frequency range of dedicated RF sources varies from a few kHz up to 60 GHz. Despite many advantages for dedicated RF sources, they suffer from several drawbacks including losses caused by energy shadowing and fading. The power density at the node is also limited due to allowable radiation power regulated by federal communications commission (FCC) (*FCC codes of regulation.*, n.d.) to protect human body from hazardous radiations. Consequently, the efficiency of the system considerably decreases (Mishra et al., 2015).

RFEH systems utilize wireless power transfer (WPT) techniques, which can be categorized into three groups as far-field non-coupling (FFNC), near-field non-resonant coupling (NFNRC), and near-field resonant coupling (NFRC) (Garnica, Chinga, & Lin, 2013). The FFNC includes an antenna and rectifier to capture and convert incident RF signals into a DC voltage. The communication distance is relatively longer compared to other techniques but it suffers from low power conversion efficiency. The Faraday's induction law is used for transferring power in NFNRC technique. The NFNRC technique offers comparatively higher power transfer efficiency at a very short communication

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distance. However, the efficiency deteriorates rapidly when the distance exceeds the effective communication range. Although the NFRC technique exhibits higher efficiency, the communication distance is still short comparing the FFNC technique.

Unlike active wireless microsystems, which include an integrated power source such as a battery for their operation, in a passive wireless microsystem, the power for operation can be captured from a dedicated RF source emitting RF waves. Passive wireless microsystems normally adopt FFNC and NFRC WPT techniques based on the aspects of the wireless links with the RF source, and the boundary that separate them is defined as

$$\text{Boundary} = \frac{\lambda}{2\pi} \tag{2.6}$$

where λ is the wavelength of the signal. NFRC is more suitable for operating frequencies up to a few tens of MHz since the resonant frequency of the planar coupling coil is relatively low. The most popular application of the NFRC technique is in biomedical implantable devices due to the high level of RF wave absorption by living tissues at high frequencies. The near-field coupling technique also offers a large voltage at the coupling coils of the microsystem, and the interference from nearby devices are significantly weak since the distance between the source and the microsystem is considerably short.

On the other hand, the FFNC technique is commonly used at ultra high frequency (UHF), microwave, and even millimeter frequencies such as ISM 900 MHz (Hameed & Moez, 2015), 2.4 GHz bands (Olgun, Chen, & Volakis, 2010), and 60 GHz respectively (Burasa et al., 2014). the key features of the FFNC technique include a high data transferring rate, a small antenna dimension, and a long communication distance. The focus of this research is the FFNC technique for RFEH systems.

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The maximum effective isotropic radiated power (EIRP) of RF sources are usually regulated to prevent hazardous RF radiation to the human body, which limits the power density leading in reducing the communication distance between the microsystem or sensor and the RF source in the FFNC technique. For instance, the maximum EIRP is 4 W in North America at UHF bands, which bounds the communication distance to a few meters (Vita & Iannaccone, 2005a). Under such a limited power density, the total efficiency of the energy harvester, which is a critical measuring parameter, determines the maximum communication distance. The efficiency of the RFEH is under influence of a number of factors including the efficiency of the antenna, the accuracy of the matching network circuit between the antenna and the RFEH, and the power conversion efficiency (PCE) of the rectifier that converts received RF signals to a DC voltage from which the rest of the circuitry in the system is powered.

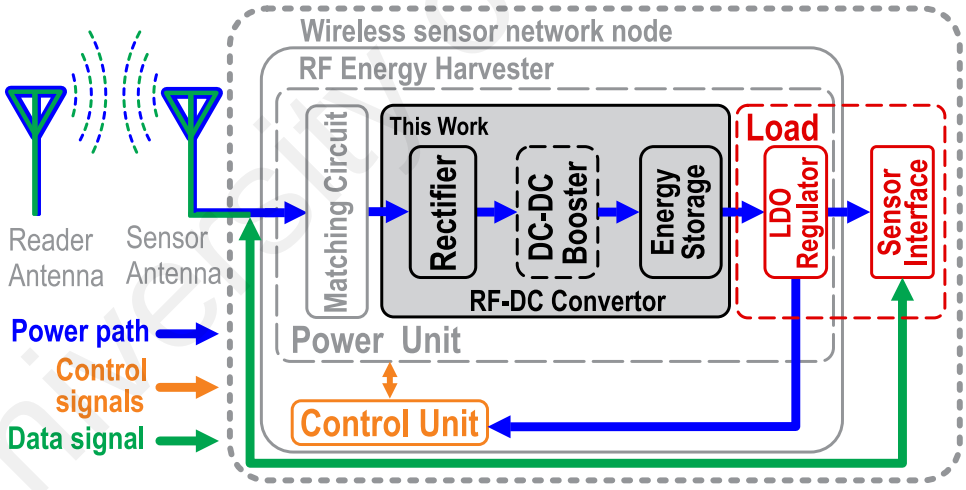

Figure 2.6: Block diagram of a typical RFEH system.

A typical block diagram of a FFNC-RFEH system is depicted in Fig.2.6, which is more complete than Fig.1.2. It consists of two main parts, which are the power and the control unit. The power is generated in the power unit. The power path is depicted in Fig.2.6 with blue arrow lines. The power unit is also responsible to deliver the extracted power to both the load and the control unit. The control signals, depicted in Fig.2.6 with

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an orange arrow line, are generated by the control unit to tune the power unit parameters in order to maximize or regulate the output power. The data signal is depicted with a green arrow line in Fig.2.6, carries the data information sent by either a central hub/reader or the microsystem.

The microsystem antenna is usually designed with radiation resistance of 50 Ω at a specific frequency. In addition, the input impedance of the rectifier typically includes a reactance component due to the parasitic capacitance of the integrated switching devices (MOSFET transistors). Hence, matching network is required to transform the input impedance of the rectifier to 50 Ω by using inductors.

In Fig.2.7, a matching network is integrated between the antenna and the rectifier where V_a represents the voltage source, R_a is the radiation resistance, and R_L denotes the equivalent rectifier resistance. It should be noted that the input impedance of the rectifier is here assumed to be purely resistive to simplify the analysis. However, this assumption is achievable if a shunt inductor is employed to neutralize the reactive part of the rectifier impedance (Vita & Iannaccone, 2005a).

$$P_L = \frac{V_L^2}{R_L} = \frac{A_v^2 V_a^2}{R_L} \tag{2.7}$$

where

$$A_v = \frac{1}{2}\sqrt{\frac{R_L}{R_a}} \tag{2.8}$$

With an accurate matching network, maximum power will be transferred to the rectifier with minimum signal reflection. Moreover, the matching network provides a condition to maximize the voltage at the input of the rectifier. Considering a loss-less matching network, the power delivered to the matching network and the rectifier will be

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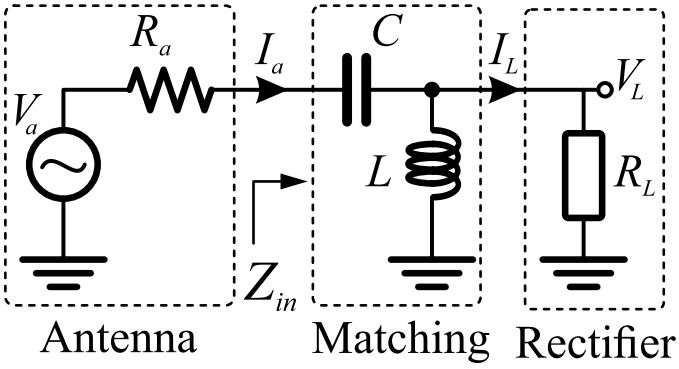

Figure 2.7: Matching circuit to maximize the power delivery to the rectifier

equal and the large voltage provided by the matching network reduces the power loss at the rectifier. Therefore, the overall conversion efficiency of the RFEH will be maximized.

2.3.1 Rectifier PCE

The RF signals emanating from a central hub or reader are collected and converted into signal voltages by an RF antenna. The extracted signal voltages can be modeled as an equivalent voltage source (V_S) and a source resistance (R_S). An impedance matching network is usually required to maximize the available power for the rectifier. Hence, the available power can be calculated as

$$P_{available} = \frac{V_S^2}{8R_S} \tag{2.9}$$

when a proper matching network is considered (Hsieh et al., 2015). In RFEH systems, the received power at the antenna is usually weak due to the limited allowable power levels regulated by the FCC and the degrading propagation loss (Mandal & Sarpeshkar, 2007; Le, Mayaram, & Fiez, 2008). The available power significantly drops with the increase in the distance between the source and the RFEH system based on the Friis transmission equation, given by

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$$P_{tag} = \text{EIRP}_{\text{reader}} \cdot G_{tag} \cdot \eta_{\text{rectifier}} \cdot \left(\frac{\lambda}{4\pi d}\right)^2 \tag{2.10}$$

In Eq.2.10 $\text{EIRP}_{\text{reader}}$ is the effective isotropic radiation power of a reader, G_{tag} is the gain of RFEH antenna, $\eta_{\text{rectifier}}$ is the PCE of the rectifier and d is the communication distance. Furthermore, the received power faces even more attenuation with multi-path fading (Hsieh et al., 2015). As a result, the overall efficiency of the RFEH is strongly under influence of the PCE of the rectifier, which also determines the communication range. The PCE of a rectifier is defined as the ratio of power at the output of the rectifier, which is in the form of DC voltage, to the power at the input of the rectifier, which is in the form of AC voltage.

$$\eta_{rectifier} = \frac{P_{out}}{P_{in}} \tag{2.11}$$

The switching devices in the rectifier are not loss-less since they consume power in order to convert the captured power into a DC voltage. As a result, the PCE of the rectifier is always less than 100%.

Depending on the structure of the RFEH, the rectifier also boosts the converted voltage level if it is employed as a multi-stage voltage multiplier. Otherwise, the extracted voltage is enhanced by a separate DC-DC booster. For protection purposes, the generated voltage at the output is sometimes limited by a voltage limiter (Ouda, Arsalan, Marnat, Shamim, & Salama, 2013). Finally the converted power charges the energy storage (usually a capacitor), which acts as a buffer in the system. The application and the structure of the load system determines whether the load can be directly supplied by the energy storage (Pellerano, Alvarado, & Palaskas, 2010) or requires an additional voltage regulator to reduce the output ripple. Therefore, the performance of the rectifier plays a great role in the overall performance of the RFEH system. An exhaustive description, structures, and

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a brief historical development of the rectifier for RFEH is presented in the subsequent section (Section 2.4).

2.4 Rectifier for RFEH systems

As mentioned, in NFRC technique, which is typically used in biomedical implantable devices and smart cards, the power is transferred inductively, which allows to deliver a large voltage level to the microsystem. Hence, RF-to-DC conversion is achievable by a normal diode bridge, and the DC voltage at the output of the diode bridge is sufficient for the passive wireless microsystem even with its associated power loss across the diodes. Fig. 2.8 depicts a typical diode bridge rectifier. To improve the RF-to-DC conversion efficiency, Schottky diodes are commonly used since the power loss across these types of diodes are considerably lower due to their small voltage drop in the forward bias (Wang, Liu, Sivaprakasam, & Kendir, 2005; Atluri & Ghovanloo, 2006). However, additional steps are required in the fabrication process in order to implement Schottky diodes in the standard CMOS process, which results in an increase in the fabrication cost. On the other hand, MOSFET transistors can be used in the diode-connected configuration to design a rectifier. A diode-connected MOSFET transistor is achievable by connecting the gate and the drain together. Using the diode-connected MOSFET configuration allows the

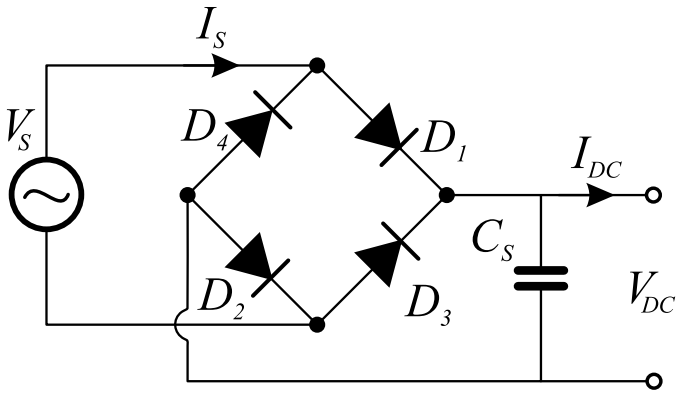

Figure 2.8: Diode bridge rectifier configuration used in NFRC power transferring technique

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rectifier to be implemented in standard CMOS technologies, which maintains the cost of fabrication to be more affordable and efficient. It should be noted that the power still losses across each MOSFET due to the threshold voltage of the transistors but since the power density at the antenna is relatively large in the NFRC power transferring technique, the loss associated to the transistors' threshold voltage does not considerably affect the performance of the rectifier, and the loss can be neglected.

In the FFNC power transferring technique, which is commonly used in passive RFID tags and wireless microsensors, the power is captured directly in the form of radio-frequency waves without any inductive links. Therefore, the received power at the microsystem antenna is usually small, which approximates a few hundred mV and the diode bridge rectifier configuration is not efficient since the voltage drops of the transistors are no longer negligible compared to the amplitude of the received RF signal at the antenna. To achieve more efficient RF-to-DC conversion and also higher DC voltage at the output, a voltage-multiplier, which has been developed based on a voltage-doubler, is commonly used in the FFNC technique to accomplish the RF-to-DC conversion.

Fig.2.9 depicts the schematic of a common voltage-doubler. The peak of the received voltage is detected by D_2 and C_2, and subsequently the voltage is clamped by D_1 and C_1. Assuming the voltage drop across the diodes are zero and the amplitude of the received signal is V_m, the voltage at the voltage-doubler output is equal to $2 \times V_m$. In the negative half-cycle of the RF signal, D_1 is in forward bias operation and turns "on", and the current charges C_1 to V_m. In the following and the positive half-cycle of the RF signal, D_1 turns "off" as it is reverse biased, and the stored charge in C_1 starts to add on to the input voltage ($V_a = V_{in} + V_m$). Therefore, D_2 turns "on" and C_2 also charges up to $2V_m$. A normal voltage-doubler almost always generates insufficient DC voltage since the level of voltage is always limited to $2V_m$.

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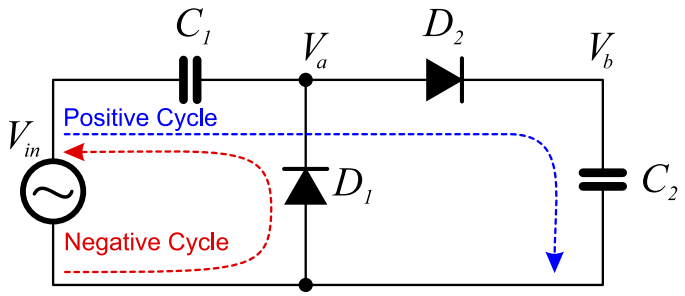

Figure 2.9: Structure of a typical voltage-doubler consists of two diodes and two capacitors.

A multi-stage voltage-doubler is commonly used as a voltage multiplier in order to achieve a DC voltage larger than $2V_m$ (Cockcroft, Gilbert, & Walton, 1935). Fig. 2.10 illustrates the configuration of a multi-stage voltage multiplier based on the voltage-doubler structure in which coupling capacitors (C_c) and stray capacitors (C_{st}) are employed. The maximum efficiency occurs when C_c is considerably larger than C_{st} (J. F. Dickson, 1976). The structure requires a pair of clocking signal as Φ and $\bar{\Phi}$ for operation. The clocking signal only drives the first coupling capacitors. The efficiency extremely decreases when C_c and C_{st} become comparable, which is a significant drawback in monolithic integration.

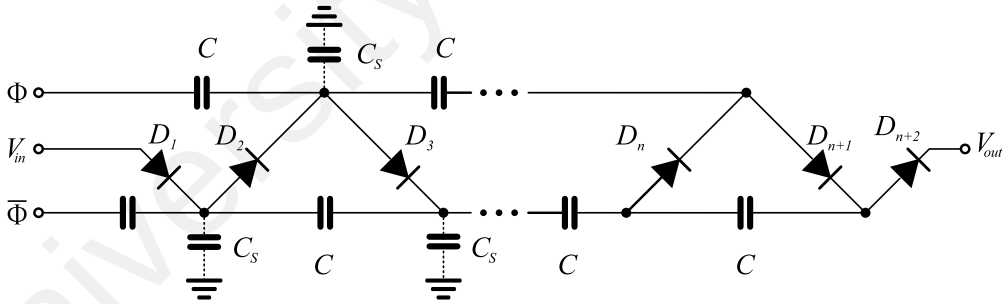

Figure 2.10: Structure of a conventional multi-stage voltage-doubler adopted as a voltage multiplier.

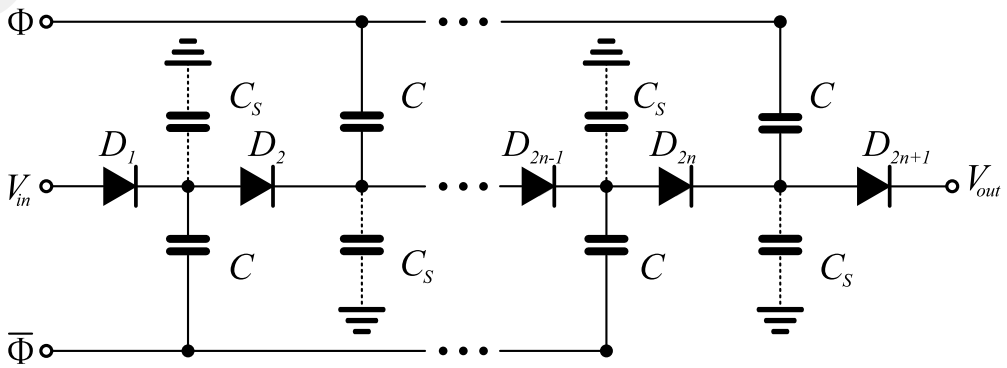

Figure 2.11: Rectifier structure proposed by Dickson, which is known as a charge-pump.

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J. F. Dickson, 1976 introduced a modified structure of the voltage multiplier by driving all the coupling nodes with a differential clocking signal as depicted in Fig.2.11. The structure in Fig.2.11 became popular and is known as Dickson charge-pump thereafter. In the Dickson charge-pump structure, both coupling and stray capacitors are directly driven by the clocking signals, which eliminate the drawback of the normal voltage multiplier since all the capacitors are connected in parallel. However, the shunt capacitor, which is placed at the output of the charge-pump is required to be large enough to withstand the maximum DC voltage (V_{DC}) generated at the output. The output voltage of a N-stage Dickson charge-pump can be calculated by (Karthaus & Fischer, 2003)

$$V_{DC} = N.(V_m - V_{th}) \tag{2.12}$$

where N denotes the number of stages.

Reducing V_{th} of diodes increases the generated DC voltage at the output. Therefore, Schottky diodes are normally used to design a Dickson-based voltage multiplier since their threshold voltage is considerably small with large saturation current, and the diodes also offer a low junction capacitance and small series resistance (Karthaus & Fischer, 2003). However, as mentioned, using Schottky diodes requires additional fabrication process steps and additional masks, which sometimes this capability is not available in a standard CMOS process. Even if this capability is available, it might induce an increase in the fabrication cost.

The Dickson charge-pump can be implemented in a standard CMOS process by replacing diodes with MOSFET transistors in the diode-connected configuration. Fig.2.12 shows the Dickson-based charge pump using n-type MOSFET transistors. A similar charge-pump can be designed using p-type MOSFET transistors. The compatibility with

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the standard CMOS fabrication process is the main advantage of this configuration but it suffers from the power dissipation since the threshold voltage of the transistors is not relatively small. Hence, the efficiency of the charge-pump using MOSFET transistors is noticeably lower especially when the received power at the input is small.

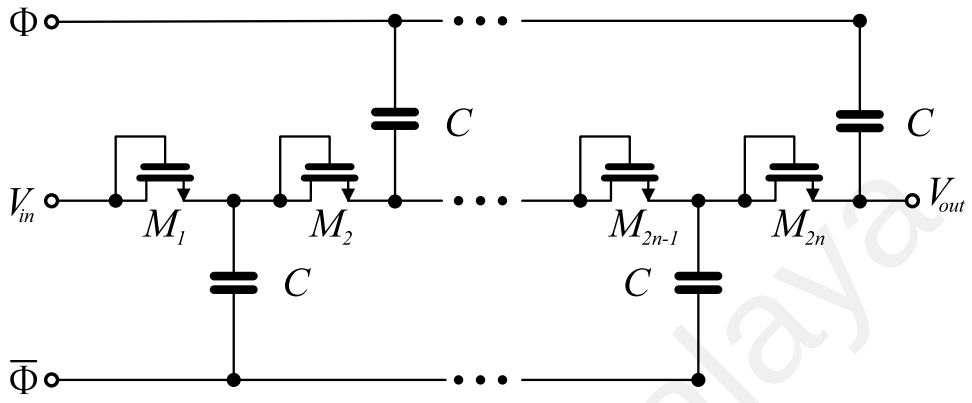

Figure 2.12: Dickson charge-pump structure using n-type MOSFET transistors.

The voltage drop across the MOSFET transistors can be minimized by adding an extra MOSFET transistor parallel with each diode-connected MOSFET transistors (Wu & Chang, 1998) in the Dickson charge-pump structure as depicted in Fig.2.13. The added MOSFET transistors operate in triode region and reduce the voltage drop across each MOSFET transistor. The operation mechanism of this configuration is as follows: when Φ is 0, M_{1A} turns "on" since voltage at point 1 is initially zero and the input voltage charges C_1. It should be noted that the maximum voltage V_1 is only $V_m - V_{th}$ without transistor M_{1B}. M_{1B} operates in triode region since M_{2A} is in "off" state.

It is important to note that clocking signals (Φ, $\bar{\Phi}$) are required to be non-overlapping in order to provide the suitable operation conditions for the Dickson-based voltage mul-

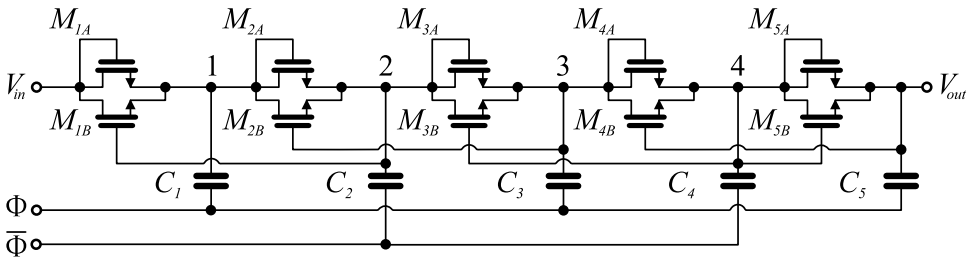

Figure 2.13: Circuit configuration of static Dickson charge-pump.

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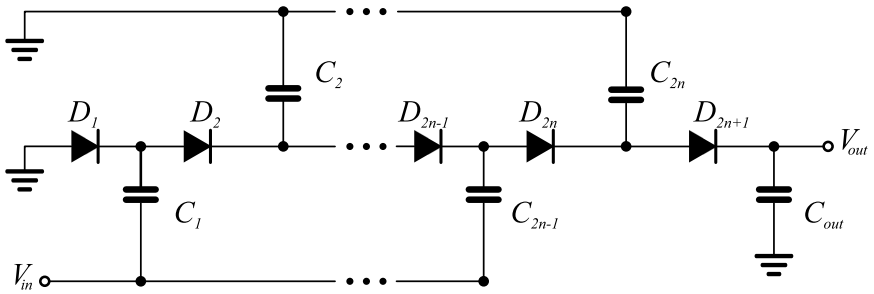

Figure 2.14: Modified Dickson charge-pump structure using diodes.

tipliers. However, in most cases only one RF signal is available for RFEH systems. Therefore, the Dickson charge-pump cannot be directly used. The Dickson-based charge-pump can be modified by grounding $\bar{\Phi}$ and V_{in} while connecting the RF incoming signal to Φ terminal as depicted in Fig.2.14, which is comparable with the voltage-doubler structure. The effect of stray capacitance is significantly suppressed in rectifier since the RF signal is connected to every other node of the diode chain. It is clear that a fully differential RF signal, which can be coupled to $C_{1,3,5}$ and $C_{2,4,6}$ will further improve the performance.

The modified Dickson charge-pump can also be implemented by n-type or p-type MOSFET transistors in diode-connected configurations. Fig.2.15 shows the modified Dickson charge-pump using n-type MOSFETs while in Fig.2.16 p-type MOSFET transistors are used to construct the charge-pump. Although the modified structure does not need non-overlapping clock signals, the efficiency of the charge-pump is comparatively lower than its Schottky-diode counterpart due to the voltage drop across the drain and the source of the transistors. n-type MOSFET transistors with near zero threshold voltage have been implemented (Facen & Boni, 2007; Shameli, Safarian, Rofougaran, Rofougaran, & Flaviis, 2007) to mitigate the power loss due to the threshold voltage. However, the transistors with near zero threshold voltage are not supported in standard CMOS technologies. In addition, the transistors also deteriorate the performance of the charge-pump due to their large channel resistance.

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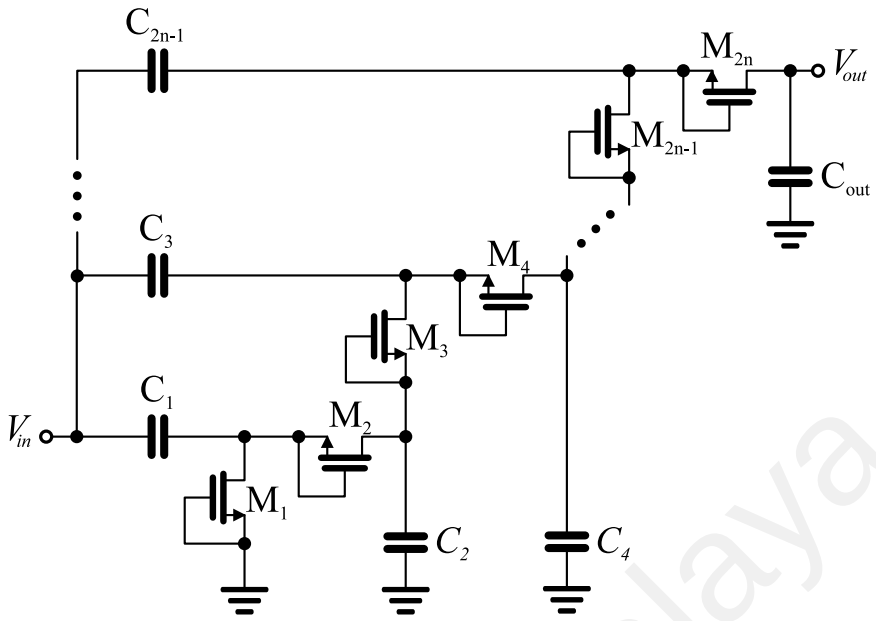

Figure 2.15: Structure of modified Dickson charge-pump using n-type MOSFET transistors.

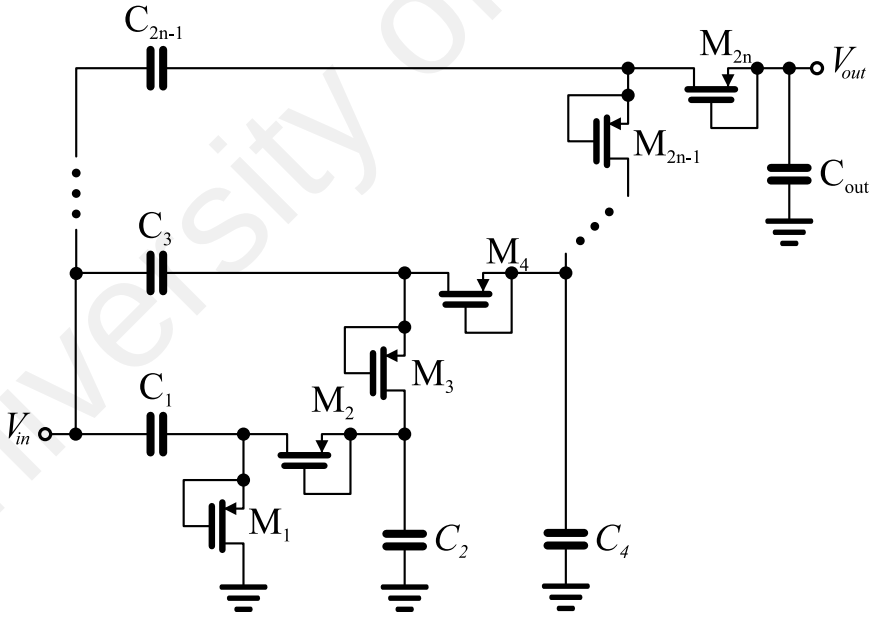

Figure 2.16: Structure of modified Dickson charge-pump using p-type MOSFET transistors.

Mandal & Sarpeshkar, 2007 introduced a low power voltage multiplier with high efficiency to solve the problem of the charge-pump in terms of efficiency as depicted in Fig.2.17 using a couple of n-type MOSFET and a couple of p-type MOSFET transistors.

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The structure has been modified thereafter by (Kotani, Sasaki, & Ito, 2009) and named as a DDCCB rectifier. The DDCCB rectifier structure is able to considerably decrease both the threshold voltage and leakage current of the MOSFET transistors. Therefore, a larger DC voltage can be generated at the output of the DDCCB rectifier compared with Dickson-based rectifiers. In Section 2.5 the mechanism of the DDCCB rectifier will be explained in detail.

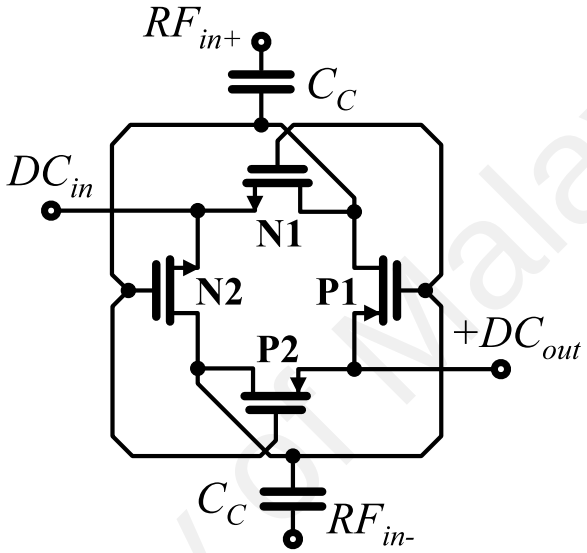

Figure 2.17: Circuit configuration of DDCCB rectifier using p-type and n-type MOSFET transistors.

Umeda et al., 2006 proposed another scheme to alleviate the threshold voltage of the MOSFET transistors, which is shown in Fig2.18, and referred to as V_{th}-cancellation technique to improve the efficiency of the voltage multipliers. The gate voltage of M_1 (V_{G1}) can be expressed as

$$V_{G1} = V_m + V_b \tag{2.13}$$

where V_b is the biasing voltage of the transistors' gate, which is externally provided. The output voltage can be expressed as

$$V_{out} = 2(V_{GSmax} - V_{th}) = 2(V_m + V_b - V_{th}) \tag{2.14}$$

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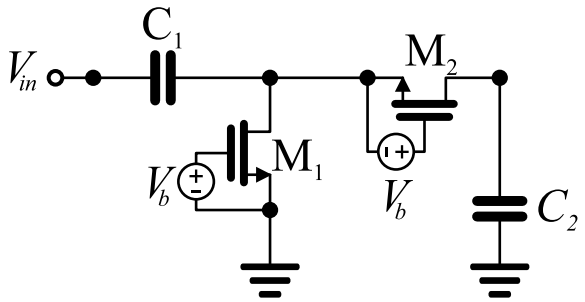

Figure 2.18: Circuit configuration of voltage multiplier using V_{th}-cancellation technique with external source (V_b).

Assuming $V_b = V_{th}$, the output voltage is consequently equal to $2V_m$. Therefore, the power loss caused by the threshold voltage is seemingly suppressed. It should be noted that the circuit configuration of the voltage multiplier proposed by (Umeda et al., 2006) requires an external voltage source, which is not available where an RFEH system is adopted. An internal threshold voltage cancellation technique was proposed by (Nakamoto et al., 2007) as depicted in Fig.2.19 to eliminate the need for an external voltage source. Two voltage dividers are added so that R_1 and M_{1a}, along with R_2 and M_{2a} provide and store the biasing voltage in C_{1a} and C_{2a} for the gate of M_1 and M_2 respectively. To minimize the static power consumption of M_{1a} and M_{2a}, the values of R_1 and R_2 should be large to provide a condition for the compensation technique to be effective.

Among all the state-of-the-art architectures that have been proposed and introduced,

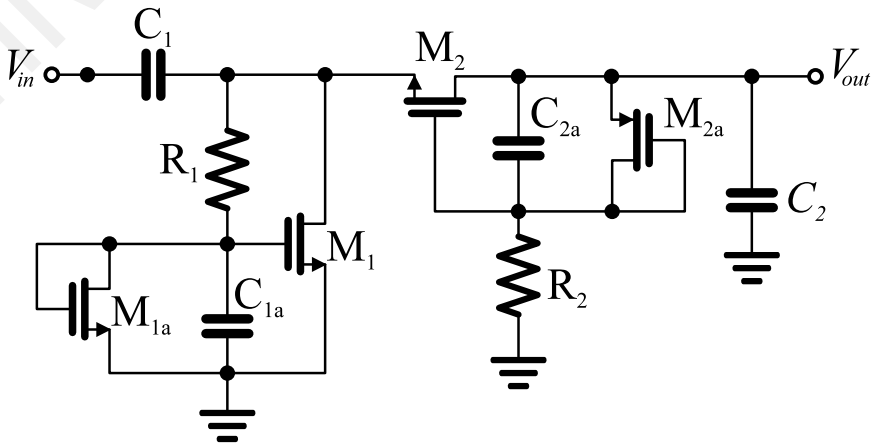

Figure 2.19: Circuit configuration of voltage multiplier using internal V_{th}-cancellation technique.

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DDCCB structures have demonstrated considerable high efficiency performance, which have made this circuit configuration very popular as a RF-to-DC converter in RFEH systems. Fig. 2.20 illustrates the maximum PCE achieved by the recent state-of-the-art that have been reported with a summary as given in Table 2.1.

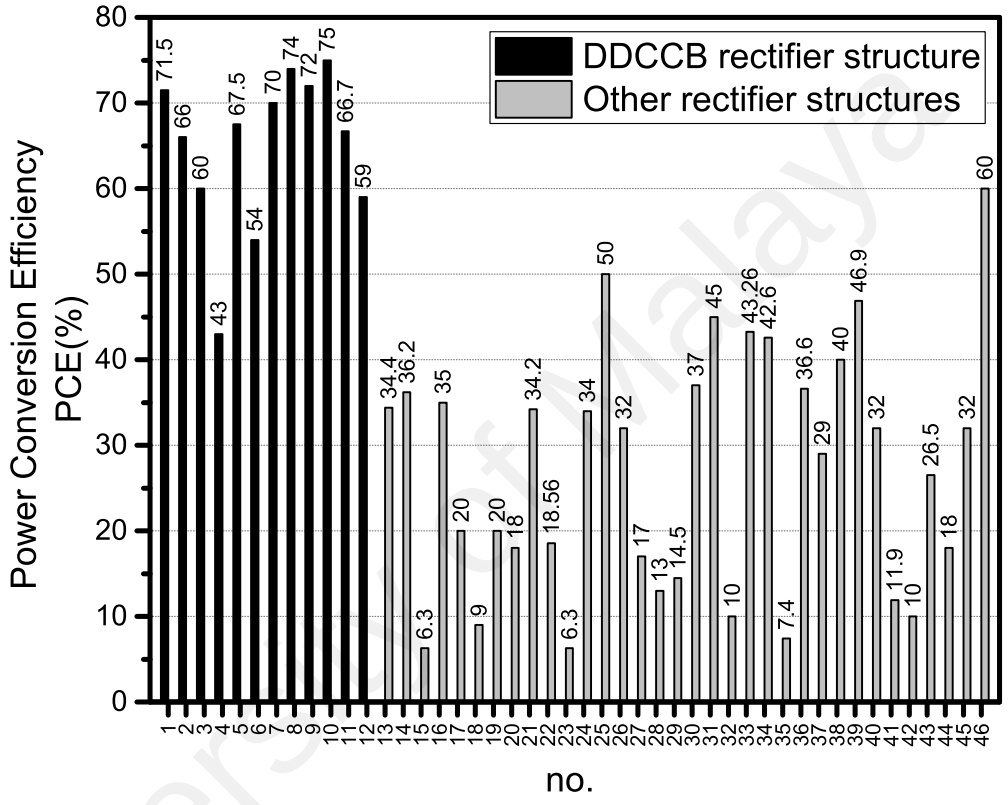

Figure 2.20: A comparison among the state-of-the-art based on their maximum PCE performance parameter cross referenced on Table 2.1.

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Table 2.1: List of state-of-the-art based on their reported maximum PCE and topology

no.	Work	Structure	PCE(%)
1	(Theilmann, Presti, Kelly, & Asbeck, 2010)	DDCCB	71.5
2	(Sasaki, Kotani, & Ito, 2008)	DDCCB	66
3	(Bakhtiar, Jalali, & Mirabbasi, 2010)	DDCCB	60
4	(Wei et al., 2011)	DDCCB	43
5	(Kotani et al., 2009)	DDCCB	67.5
6	(Kamalinejad, Keikhosravy, Mirabbasi, & Leung, 2013b)	DDCCB	54
7	(Kapucu, Panadés, & Dehollain, 2013)	DDCCB	70
8	(Kamalinejad, Mirabbasi, & Leung, 2011)	DDCCB	74
9	(Ouda et al., 2013)	DDCCB	72
10	(Hsieh et al., 2015)	DDCCB	75
11	(Kamalinejad, Keikhosravy, Mirabbasi, & Leung, 2013a)	DDCCB	66.7
12	(Chang, Chouhan, & Halonen, 2016)	DDCCB	59
13	(Lee, Lee, & Kang, 2008)	Others	34.4
14	(Lee & Lee, 2009)	Others	36.2
15	(Barnett, Liu, & Lazar, 2009)	Others	6.3
16	(Vaz, Solar, Rebollo, Gutierrez, & Berenguer, 2010)	Others	35
17	(Essel, Brenk, Heidrich, & Weigel, 2009)	Others	20
18	(Curty, Joehl, Krummenacher, Dehollain, & Declercq, 2005)	Others	9
19	(Vita & Iannaccone, 2005b)	Others	20
20	(Karthaus & Fischer, 2003)	Others	18
21	(Shen et al., 2013)	Others	34.2
22	(Y. Yao, Shi, & Dai, 2005)	Others	18.56
23	(Bergeret, Gaubert, Pannier, & Gaultier, 2007)	Others	6.3
24	(Fahsyar & Soin, 2010)	Others	34
25	(Yi, Ki, & Tsui, 2007)	Others	50
26	(Ashry et al., 2009)	Others	32
27	(Ebrahimian, El-Sankary, & El-Masry, 2010)	Others	17
28	(Y. Yao, Wu, Shi, & Dai, 2009)	others	13
29	(Kocer & Flynn, 2006)	Others	14.5
30	(Curty, Joehl, Dehollain, & Declercq, 2005)	Others	37
31	(Scorcioni et al., 2012)	Others	45
32	(Martins & de Sousa, 2013)	Others	10
33	(C. Y. Yao & Hsia, 2014)	Others	43.26
34	(Du et al., 2013)	Others	42.6
35	(Papotto et al., 2011)	Others	7.4
36	(Nakamoto et al., 2007)	Others	36.6
37	(Kotani & Ito, 2007)	Others	29
38	(Jingtian et al., 2009)	Others	40
39	(Dong-Sheng et al., 2010)	Others	46.9
40	(Cui, Akita, & Kitagawa, 2010)	Others	32
41	(Mansano, Bagga, & Serdijn, 2013)	Others	11.9
42	(Asl & Zarifi, 2014)	Others	10
43	(Lui, Murphy, & Toumazou, 2012)	Others	26.5
44	(Khansalee, Zhao, Leelarasmee, & Nuanyai, 2014)	Others	18
45	(Hameed & Moez, 2015)	Others	32
46	(Le et al., 2008)	Others	60

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2.5 Operating mechanism DDCCB rectifier

A unit stage structure of a DDCCB CMOS rectifier is depicted in Fig.2.21a. The DDCCB rectifier was more common and well-known as a rectifier for low-frequency operation (Facen & Boni, 2007). However, the DDCCB rectifier is also able to operate at higher frequency such as UHF (Kotani et al., 2009) and even at millimeter wave (Burasa et al., 2014).

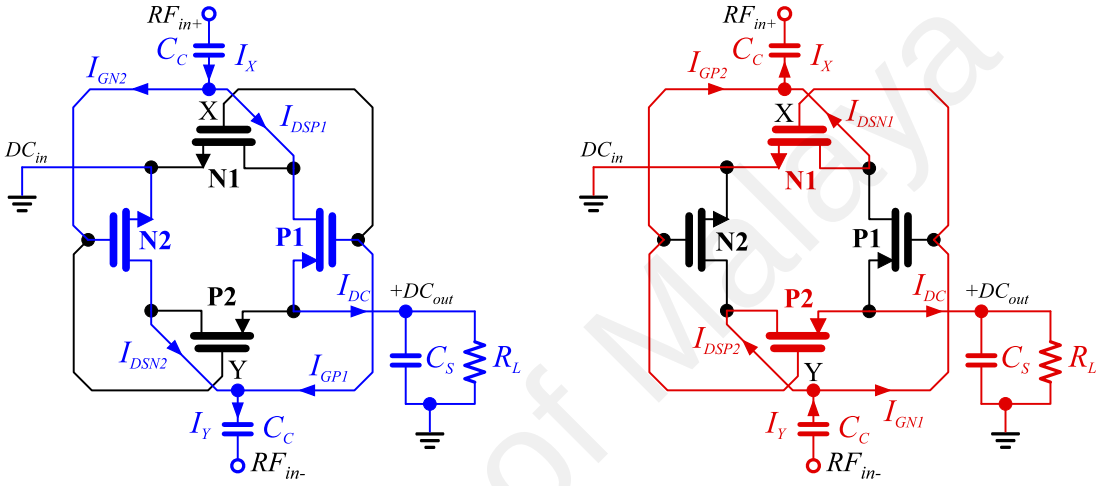

Figure 2.21: Operating mechanism of DDCCB rectifier in a)positive b)negative RF cycle.

To comprehend the operation of the DDCCB rectifier, it only requires to follow through a single RF cycle considering C_Cs are short circuited at the UHF frequency band. A DC voltage is generated by rectification operation at the internal RF nodes of X and Y, statically biases the gate of transistors and provides the V_{th}. In a positive RF-cycle, which the current path is depicted in Fig.2.21(a), when the voltage level between the nodes of antenna (RF_{in+} and RF_{in-}) rises, P_1 and N_2 turn on and current flows through the output to supply the load R_L while the other two transistors, P_2 and N_1, do not only remain in "off" state but also the gate of the transistors will be positively and negatively biased respectively; resulting in effectively suppression in their reverse leakage current.

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The current at node X and Y can be obtained by

$$I_X = I_{GN2} + I_{DSP1} \tag{2.15}$$

$$I_Y = I_{GP1} + I_{DSN2} \tag{2.16}$$

Continuing the RF signal, the input voltage drops until it becomes lower than V_{th}, which causes the P_1 and N_2 return back to "off" state. In the negative cycle of incoming RF signal, when the voltage between two nodes of the antenna reaches V_{th} again, P_2 and N_1 switch "on" and rectify the RF signal. In addition, the gate of transistors in "off" state (P_1 and N_2) are positively and negatively biased respectively; in the negative RF-cycle since the DDCCB rectifier is driven by a differential signal. The current path in the negative RF-cycle is depicted in Fig.2.21(b). The current at node X and Y in negative RF-cycle can be obtained by

$$I_X = I_{GP2} + I_{DSN1} \tag{2.17}$$

$$I_Y = I_{GN1} + I_{DSP2} \tag{2.18}$$

Consequently, I_X and I_Y in a full RF-cycle can be expressed as

$$I_X = I_{GN2} + I_{DSP1} + I_{GP2} + I_{DSN1} \tag{2.19}$$

$$I_Y = I_{GP1} + I_{DSN2} + I_{GN1} + I_{DSP2} \tag{2.20}$$

Note that the structure will never operate and the DC output will remain in 0 V if the input voltage does not become greater than the V_{th} of MOSFET transistors.

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2.6 Parasitic capacitance of DDCCB rectifier

The input impedance of a DDCCB rectifier is affected by the input reactance, which is predominated by the parasitic capacitance of the integrated transistors. Hence, the C_{in} plays an important role in the performance of the DDCCB rectifier. Since in each RF cycle one n-type MOSFET and one p-type MOSFET transistor are "on", and the two other transistors are "off", C_{in} in both RF cycles can be approximated as (Burasa et al., 2014)

$$\begin{cases} C_{in(\mathrm{POS})} = C_{gs\mathrm{P}_1(\mathrm{on})} + C_{gs\mathrm{N}_2(\mathrm{on})} + C_{gs\mathrm{P}_2(\mathrm{off})} + C_{gs\mathrm{N}_1(\mathrm{off})} \\ C_{in(\mathrm{NEG})} = C_{gs\mathrm{P}_2(\mathrm{on})} + C_{gs\mathrm{N}_1(\mathrm{on})} + C_{gs\mathrm{P}_1(\mathrm{off})} + C_{gs\mathrm{N}_2(\mathrm{off})} \end{cases} \tag{2.21}$$

with

$$\begin{cases} C_{gs(\mathrm{on})} = \dfrac{2}{3} \cdot \dfrac{\varepsilon_{ox}}{t_{ox}} \cdot W \cdot L \\ C_{gs(\mathrm{off})} = \dfrac{\varepsilon_{ox}}{t_{ox}} \cdot W \cdot L_{diff} \end{cases} \tag{2.22}$$

where ε_{ox}, t_{ox}, and L_{diff} are the oxide dielectric constant, oxide thickness, and channel length diffusion, respectively. The gate-to-source capacitance (C_{gs}) of the transistors usually increases when the operation frequency is raised and causes the input parasitic capacitance (C_{in}) to become larger. Consequently, the transistors operate in weak inversion region due to the reduction in the differential voltage and an increase in input impedance. Therefore, the PCE degrades. (Burasa et al., 2014).

In the FFNC power transferring technique, the DC output voltage is normally insufficient if a single-stage rectifier is adopted. A far-field RFEH system is expected to generate from three to five times V_{th} DC voltage to be considered as a V_{DD} supply for the CMOS digital base-band circuits. To achieve a larger DC output voltage level, a multi-stage rectifier structure is commonly adopted. Fig.2.22 depicts circuit configuration of a three-stage DDCCB rectifier.

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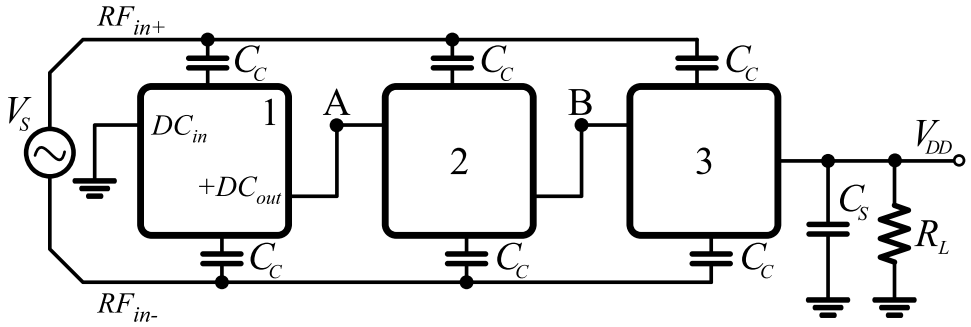

Figure 2.22: Circuit configuration of a three stage DDCCB rectifier.

In a multi-stage DDCCB rectifier, cells are stacked in series through the extracted DC path and connected in parallel via coupling capacitors (C_C) to the input terminals, which feed the rectifier with RF signals (it is usually emulated by a sinusoidal voltage source). The number of stage is usually determined by the required DC output voltage and dependent on the harvester application. Fig.2.22 depicts a three-stage DDCCB rectifier driving a load (R_L). The capacitors C_Cs are responsible for transferring the electric charge from the RF signal nodes. C_Cs are considered short at the operating frequency. C_Cs could be very small but they are expected to be larger than parasitic capacitance at the connected node. Smoothing capacitor (C_S) is usually connected in parallel with the load to mitigate the ripple at the output (Kotani et al., 2009).

2.7 Scattering parameter characterization theory

A DDCCB rectifier is considered as a differential device or network since it is driven with a differential RF signal. Unlike a single-ended device [see Fig.2.23(a)], a differential device, as depicted in Fig.2.23(b) requires some specific measurement methods (Bockelman & Eisenstadt, 1997). Instead of standard S-parameters, mixed-mode S-parameters are normally served by differential/common-mode excitations to achieve a direct and more empirical characterization of differential devices.

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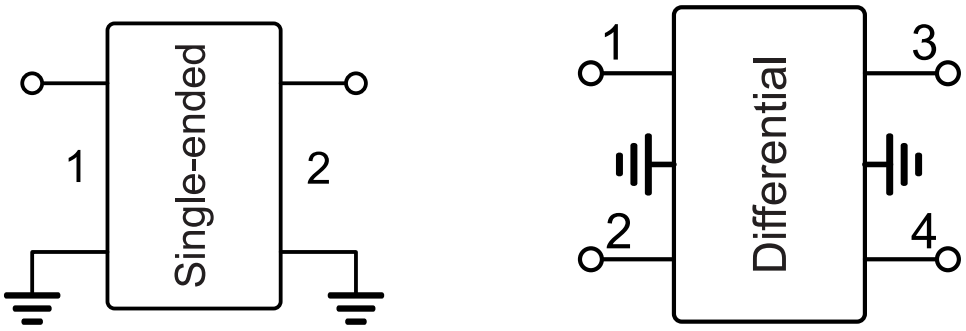

(a) (b)

Figure 2.23: a) Single-ended network, b) Differential network.

2.7.1 Mixed-mode S-parameter theory

Scattering parameters analysis is a useful method to characterize two-port RF devices. Although differential devices comprise of four ports, they can be regarded as two-port devices driven by common/differential-mode input/output signals. Hence, a special analysis is required to translate the standard S-parameter in order to characterize the differential devices. This type of analysis is referred to as mixed-mode S-parameters (Bockelman & Eisenstadt, 1997). The standard S-parameter matrix of a four-port network is defined as

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \tag{2.23}$$

The vector notation of the equation (2.23) can be written as $\bar{b} = [S]\bar{a}$, where $[S]$ represents the four-port S-parameters matrix, or sometimes it is called standard S-parameters matrix, and $\bar{b}$ and $\bar{a}$ denotes the reflected and input power wave vectors at the device respectively. The equation (2.23) can also be expanded as

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$$
\begin{aligned}
b_1 &= S_{11}a_1 + S_{12}a_2 + S_{13}a_3 + S_{14}a_4 \\
b_2 &= S_{21}a_1 + S_{22}a_2 + S_{23}a_3 + S_{24}a_4 \\
b_3 &= S_{31}a_1 + S_{32}a_2 + S_{33}a_3 + S_{34}a_4 \\
b_4 &= S_{41}a_1 + S_{42}a_2 + S_{43}a_3 + S_{44}a_4
\end{aligned}
\tag{2.24}
$$

Each individual S-parameter elements in the equation (2.23) and (2.24) can be calculated or measured by assuming the following conditions

$$
S_{xy} = \frac{b_x}{a_y} \Bigg|_{a_{i,i\neq y}=0} \tag{2.25}
$$

where x and y denote the selected pair of ports. For instance, for S_{11}

$$
S_{11} = \frac{b_1}{a_1} \Bigg|_{a_2,a_3,a_4=0} \tag{2.26}
$$

Similar relationships can be expressed for mixed-mode power waves to develop the mixed mode S-parameters as

$$
\begin{bmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{bmatrix} = \begin{bmatrix} S_{dd11} & S_{dd12} & S_{dc11} & S_{dc12} \\ S_{dd21} & S_{dd22} & S_{dc21} & S_{dc22} \\ S_{cd11} & S_{cd12} & S_{cc11} & S_{cc12} \\ S_{cd21} & S_{cd22} & S_{cc21} & S_{cc22} \end{bmatrix} \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} \tag{2.27}
$$

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The expanded of equation (2.27) can also be expressed as

$$\begin{aligned} b_{d1} &= S_{dd11}a_{d1} + S_{dd12}a_{d2} + S_{dc11}a_{c1} + S_{dc12}a_{c2} \\ b_{d2} &= S_{dd21}a_{d1} + S_{dd22}a_{d2} + S_{dc21}a_{c1} + S_{dc22}a_{c2} \\ b_{c1} &= S_{cd11}a_{d1} + S_{cd12}a_{d2} + S_{cc11}a_{c1} + S_{cc12}a_{c2} \\ b_{c2} &= S_{cd21}a_{d1} + S_{cd22}a_{d2} + S_{cc21}a_{c1} + S_{cc22}a_{c2} \end{aligned} \tag{2.28}$$

The naming notation of subscripts are as

$$S_{m_o m_i p_o p_i} = S_{(output-mode)(input-mode)(output-port)(input-port)} \tag{2.29}$$

where the modes of stimulus can be either common (c) or differential (d). When two identical signals in terms of magnitude and phase travel along a pair of conductors, it is expressed as a common mode while differential mode corresponds to the condition that the two identical signals travel along the pair of conductors with opposite phase with respect to the reference ground. Unlike in a single-ended device, in an ideal differential network, the ground is not the path that return signal currents. A constant mid-potential level between the differential input signals exists that corresponds to the reference ground terminal.

It should be noted that any arbitrary signal traveling along a pair of conductors can be represented as a combination of both purely common and differential-mode signals. Fig.2.24 illustrates the difference between the single-ended and mixed-mode S-parameters and their required excitations in order to obtain the first column of the corresponding S-parameter matrices in a differential network. Fig.2.24(a) depicts the standard S-parameters in which an applied incident power wave is represented by a_1, and b_1-b_4 are the four output power waves reflected by the ports, which all are defined with respect to a common ground.

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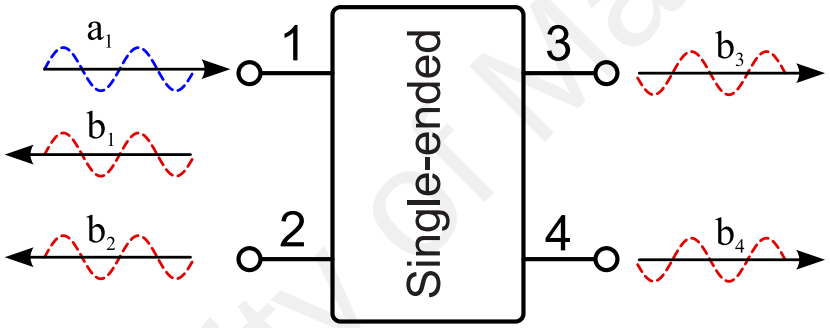
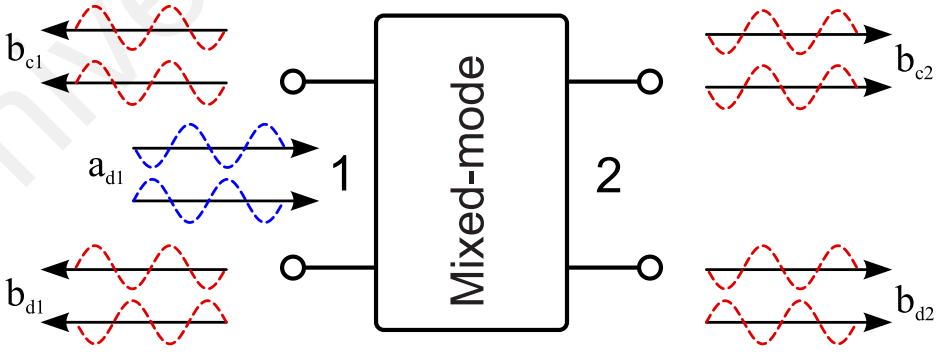
On the other hand, in Fig.2.24(b), an equivalent two-port network represents the mixed-mode parameters since a four-port network can be represented as a pair of input and a pair of output ports. Therefore, the mixed-mode input port can be defined as a signal sum or difference of signals between the single-ended port 1 and 2 depending on the excitation mode (common or differential). In a similar way, the mixed-mode output mode can be defined between the singled-ended port 3 and 4. In Fig.2.24(b), an example is depicted when a_{d1} as a differential incident power wave is applied at the mixed-mode port 1, which causes the network to reflect four power waves at both port 1 and 2 (b_{d1}, b_{c1}, b_{d2} and b_{c2}).



(a)



(b)

Figure 2.24: An example of a) Single-ended and b) Mixed-mode excitations of a four port circuit.

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The 16 terms of the mixed-mode S-parameter matrix in equation (2.27) can be divided into four 2×2 sub-matrices as

$$\begin{bmatrix} \begin{bmatrix} S_{dd11} & S_{dd12} \\ S_{dd21} & S_{dd22} \end{bmatrix} & \begin{bmatrix} S_{dc11} & S_{dc12} \\ S_{dc21} & S_{dc22} \end{bmatrix} \\ \begin{bmatrix} S_{cd11} & S_{cd12} \\ S_{cd21} & S_{cd22} \end{bmatrix} & \begin{bmatrix} S_{cc11} & S_{cc12} \\ S_{cc21} & S_{cc22} \end{bmatrix} \end{bmatrix} = \begin{bmatrix} S_{dd} & S_{dc} \\ S_{cd} & S_{cc} \end{bmatrix} \tag{2.30}$$

In equation (2.30), each common/differential-mode for input/output excitations is well presented by a 2×2 sub-matrix where S_{dd} is differential-mode S-parameters, S_{dc} is common-mode to differential-mode, S_{cd} is differential-mode to common-mode, and S_{cc} is common-mode S-parameters.

2.7.2 Mixed-mode S-parameters of a three port network

Mixed-mode S-parameters can also be used to characterize three-port devices such as baluns and power spliters. The standard and mixed-mode S-parameter matrices can be expressed as

$$S_{th}^{std} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \tag{2.31}$$

$$S_{th}^{mm} = \begin{bmatrix} S_{ss11} & S_{sd12} & S_{sc12} \\ S_{ds21} & S_{dd22} & S_{dc22} \\ S_{cs21} & S_{cd22} & S_{cc22} \end{bmatrix} \tag{2.32}$$

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2.7.3 Standard/mixed-mode S-Parameter transformation

The standard S-parameters can be simply transformed into mixed-mode S- parameters. That is to say, a differential circuit can be measured using a standard four-port S-parameter and transform it to the relevant mixed-mode s-parameter.

$$\begin{bmatrix} S_{dd} & S_{dc} \\ S_{cd} & S_{cc} \end{bmatrix} \Longleftarrow \text{Transformation} \Longrightarrow \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \tag{2.33}$$

A comprehensive study and details of transformation are presented by (Bockelman & Eisenstadt, 1995). The transformation of standard S-parameters of a four-port device can be obtained by

$$S^{mm} = M \cdot S^{std} \cdot M^{-1} \tag{2.34}$$

where

$$M = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \tag{2.35}$$

By applying equation (2.34) into equation (2.30) all mixed-mode parameters can be translated into the algebraic form as given by

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$$
\begin{aligned}
S_{dd} &= \begin{bmatrix} S_{dd11} & S_{dd12} \\ S_{dd21} & S_{dd22} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} \left(S_{11}-S_{12}-S_{21}+S_{22}\right) & \left(S_{13}-S_{14}-S_{23}+S_{24}\right) \\ \left(S_{31}-S_{32}-S_{41}+S_{42}\right) & \left(S_{33}-S_{34}-S_{43}+S_{44}\right) \end{bmatrix} \\
S_{dc} &= \begin{bmatrix} S_{dc11} & S_{dc12} \\ S_{dc21} & S_{dc22} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} \left(S_{11}+S_{12}-S_{21}-S_{22}\right) & \left(S_{13}+S_{14}-S_{23}-S_{24}\right) \\ \left(S_{31}+S_{32}-S_{41}-S_{42}\right) & \left(S_{33}+S_{34}-S_{43}-S_{44}\right) \end{bmatrix} \\
S_{cd} &= \begin{bmatrix} S_{cd11} & S_{cd12} \\ S_{cd21} & S_{cd22} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} \left(S_{11}-S_{12}+S_{21}-S_{22}\right) & \left(S_{13}-S_{14}+S_{23}-S_{24}\right) \\ \left(S_{31}-S_{32}+S_{41}-S_{42}\right) & \left(S_{33}-S_{34}+S_{43}-S_{44}\right) \end{bmatrix} \\
S_{cc} &= \begin{bmatrix} S_{cc11} & S_{cc12} \\ S_{cc21} & S_{cc22} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} \left(S_{11}+S_{12}+S_{21}+S_{22}\right) & \left(S_{13}+S_{14}+S_{23}+S_{24}\right) \\ \left(S_{31}+S_{32}+S_{41}+S_{42}\right) & \left(S_{33}+S_{34}+S_{43}+S_{44}\right) \end{bmatrix}
\end{aligned}
\tag{2.36}
$$

In the equation (2.36), a sum of four standard S-parameter term results each of the mixed-mode s-parameter terms. In a similar way, the standard S-parameters of a three port network can be transformed to the mixed-mode S-parameters

$$
S_{th}^{mm} = M_{th} \cdot S_{th}^{std} \cdot M_{th}^{-1} \tag{2.37}
$$

where

$$
M_{th} = \frac{1}{\sqrt{2}}\begin{bmatrix} \sqrt{2} & 0 & 0 \\ 0 & 1 & -1 \\ 0 & 1 & 1 \end{bmatrix} \tag{2.38}
$$

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Hence, by applying (2.38) into (2.37), the algebraic form of mixed-mode S-parameters of a three port network can be expressed as

$$S_{th}^{mm} = \begin{bmatrix} S_{ss11} & S_{sd12} & S_{sc12} \\ S_{ds21} & S_{dd22} & S_{dc22} \\ S_{cs21} & S_{cd22} & S_{cc22} \end{bmatrix} = \begin{bmatrix} 2S_{11} & \sqrt{2}\left(S_{12} - S_{13}\right) & \sqrt{2}\left(S_{12} + S_{13}\right) \\ \sqrt{2}\left(S_{21} - S_{31}\right) & \left(S_{22} - S_{23} - S_{32} + S_{33}\right) & \left(S_{22} + S_{23} - S_{32} - S_{33}\right) \\ \sqrt{2}\left(S_{21} + S_{31}\right) & \left(S_{22} - S_{23} + S_{32} - S_{33}\right) & \left(S_{22} + S_{23} + S_{32} + S_{33}\right) \end{bmatrix} \tag{2.39}$$

2.7.4 Extracting standard S-parameter by a two-port VNA

The mixed-mode S-parameters of a four-port electronic device are usually measured using a four-port vector network analyzer (VNA) or power network analyzer (PNA) equipment with a differential measurement feature. Depending on the equipment utilized for measurement, sometimes the only feature available for the measurement equipment is the standard S-parameters measurement. In this case, the standard S-parameters can be transformed to mixed-mode S-parameters as it has been explained in Section 2.7.3.

For the purpose of testing and characterization of a device with four ports, a four port measuring equipment is usually used to measure the standard S-parameters, which is subject to availability of such equipment. The standard S-parameters are also achievable using a single-ended two-port VNA or PNA. In this technique, selected two ports are connected to the measuring equipment respectively, and the other ports are coupled and terminated by a 50 Ω terminator. For instance, to achieve the standard S-parameters of a four-port device, 6 possible combinations of four individual ports are measured as port1&2, port1&3, port1&4, port2&3, port2&4, port3&4. Fig.2.25 illustrates all the two

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ports combination to obtain the standard S-parameters (Fan, Lu, Wai, & Lok, 2003).

2.8 Summary

In this chapter, a concise information about CMOS technology has been presented along with basic operation principles, and the parasitic effects of MOSFETs. Moreover, some of the most common rectifier structures and their benefits and shortcomings have been explained. The DDCCB rectifier structure has been studied in more detail due to its higher PCE. Finally, theoretical information about scattering parameters for characterizing the rectifier has been discussed. In the next chapter, a novel DDCCB-based rectifier structure will be introduced with the capability of symmetric DC voltage at the output. In addition, new self-body-biasing techniques will be presented to improve the performance of the rectifier.

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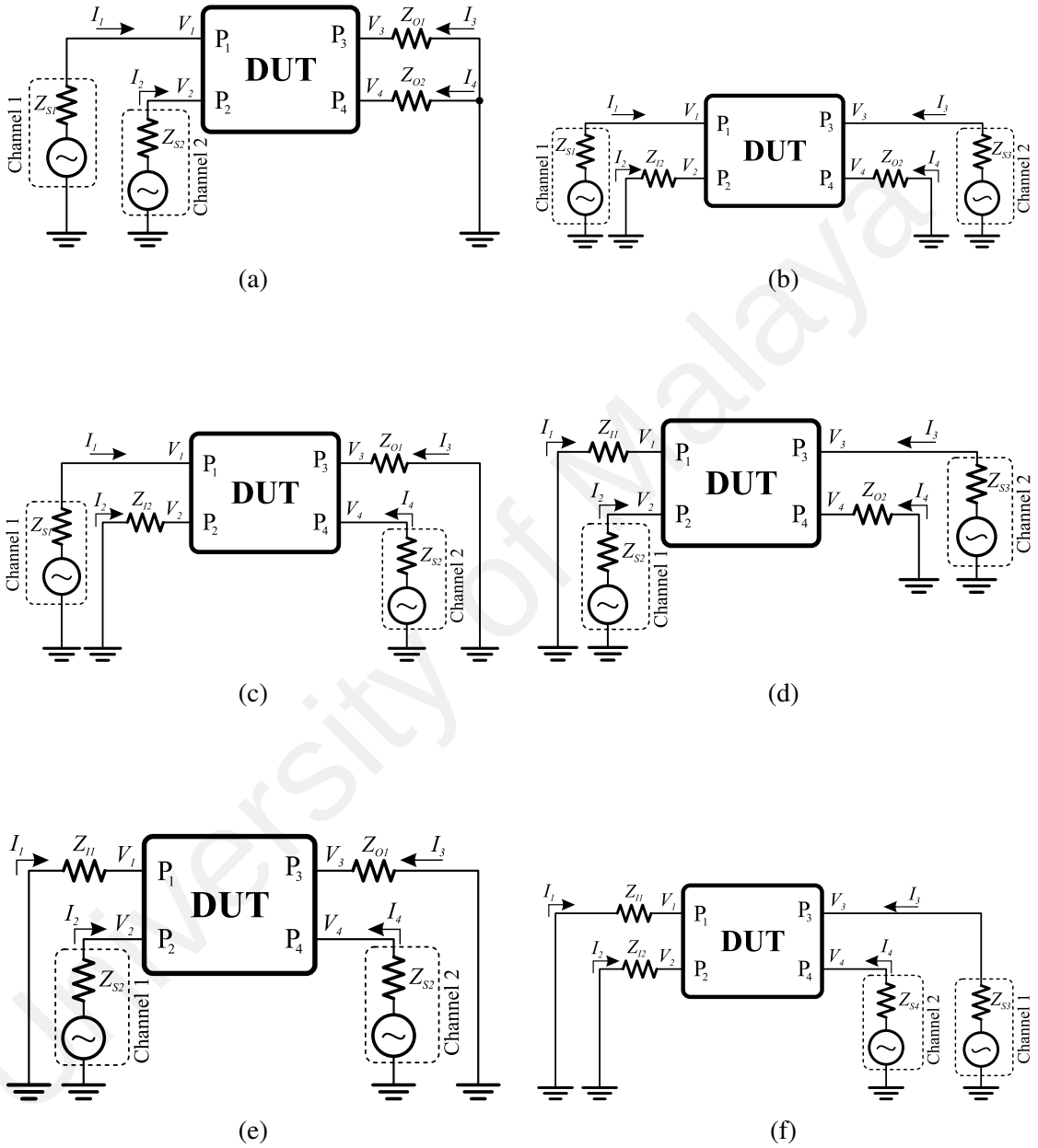

Figure 2.25: Standard S-parameters measurement technique with two port VNA. a) Port 1 and 2. b) Port 1 and 3. c) Port 1 and 4. d) Port 2 and 3. e) Port 2 and 4. f) Port 3 and 4.

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CHAPTER 3: METHODOLOGY

3.1 Introduction

As discussed in Chapter 2, integrating a rectifier with a symmetric DC output capability in the RFEH system increases the rectification efficiency, non-linearity of input resistance, and allows the interface to be more efficient to the antenna. A rectifier with the symmetric DC output capability also provide a condition for the succeeding analog circuits to be more flexible and efficient (Ashry et al., 2009). In addition, the body of MOSFET transistors in the DDCCB rectifier can be regulated to reduce the threshold voltage in order to mitigate the power loss in the rectifier structure. However, threshold voltage reduction usually causes the leakage current of the transistors to increase in the reverse bias. Biasing the body of the transistors can also be used to control the efficiency of the rectifier and limit the DC output voltage to protect the subsequent circuitry in a wireless sensor node when the communication distance is too short and the energy harvester captures surplus power. In this chapter, the design methodology of four novel DDCCB rectifier structures are proposed with symmetric DC output capability to drive the load system using self-body biasing techniques. Among all proposed structure, only one structure exhibits significantly improved performance in terms of DC voltage at the output and PCE, and the rectifier operates with an adaptive efficiency based on the received power at the input.

3.2 Proposed a symmetric DDCCB rectifier structure

To design a rectifier with a symmetric DC output capability, an alternative rectifier cell is required to extract and convert the incoming RF signals into a negative DC voltage. A simple observation through the operation mechanism of DDCCB rectifier reveals that a negative DC voltage could be generated by swapping the n-type and p-type MOSFET transistors in the rectifier structure where the n-type transistors are employed to conduct

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the positive RF cycle and the p-type transistors are employed to conduct in the negative RF cycle. As a result, the current flows from the output to the ground and generates a negative DC voltage. Fig.3.1 illustrates the schematic circuit configuration such a rectifier cell, which is also known as a reverse rectifier.

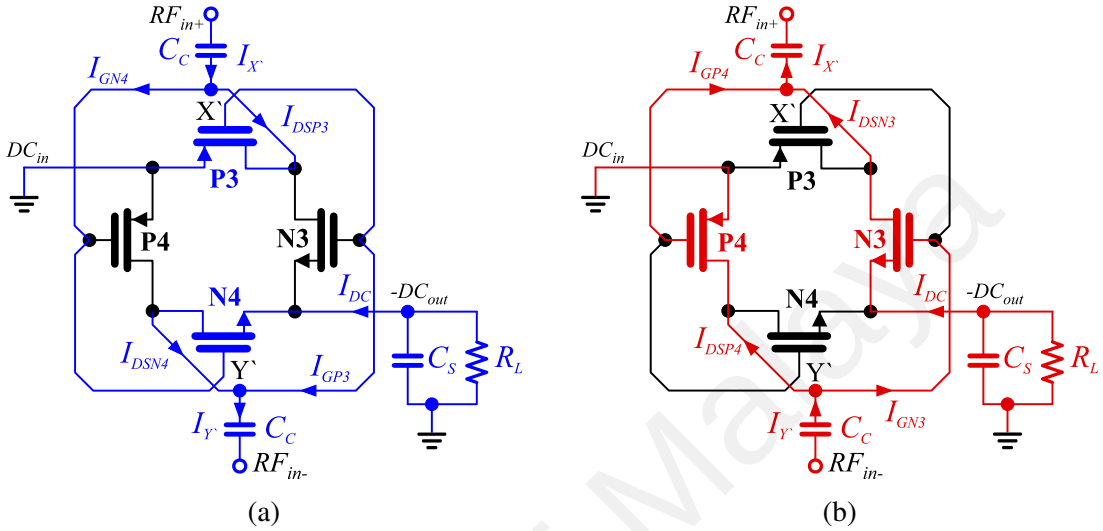

Figure 3.1: Operating mechanism of a reverse DDCCB rectifier in a) positive b) negative RF cycle.

To comprehend the operation of the reverse DDCCB rectifier it only requires to follow through a single RF cycle considering C_Cs are short at UHF frequency band. In contrast with the conventional DDCCB rectifier, a negative DC voltage is generated by rectification operation at the internal RF nodes of X$'$ and Y$'$, which statically biases the gate of transistors and provides the V_{th}. In a positive RF-cycle in which the current path is depicted in Fig.3.1(a), when the voltage level between the nodes of antenna (RF_{in+} and RF_{in-}) rises, P_3 and N_4 turn "on" and the current is drawn from the load R_L to the output while other two transistors (P_4 and N_3) do not only remain in "off" state, but also the gate of P_4 and N_3 are positively and negatively biased respectively; resulting in effectively suppressing their reverse leakage current. The current at node X$'$ and Y$'$ can be obtained by

$$I_{X'} = I_{GN4} + I_{DSP3} \tag{3.1}$$

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$$I_{Y'} = I_{GP3} + I_{DSN4} \tag{3.2}$$

Following the RF signal to the negative cycle, the input voltage drops until it becomes lower than V_{th}, which causes the P_3 and N_4 revert back to "off" state. In the negative cycle of the RF signal, when the voltage between two nodes of antenna reaches -V_{th}, P_4 and N_3 switch to "on" state and rectify the RF-signal. In addition, the gate of P_3 and N_4 in "off" state, are positively and negatively biased respectively in the negative RF-cycle since the DDCCB rectifier is driven by a differential signal. The current path in the negative RF-cycle is depicted in Fig.3.1(b). The current at node X' and Y' in the negative RF-cycle can be obtained by

$$I_{X'} = I_{GP4} + I_{DSN3} \tag{3.3}$$

$$I_{Y'} = I_{GN3} + I_{DSP4} \tag{3.4}$$

Consequently, $I_{X'}$ and $I_{Y'}$ in a full RF-cycle can be expressed as

$$I_{X'} = I_{GN4} + I_{DSP3} + I_{GP4} + I_{DSN3} \tag{3.5}$$

$$I_{Y'} = I_{GP3} + I_{DSN4} + I_{GN3} + I_{DSP4} \tag{3.6}$$

The reverse DDCCB rectifier would not operate and the DC output would remain to be 0 V if the input voltage is not greater than the V_{th} of MOSFET transistors. Combining the normal or positive, which the operation mechanism is explained in Section 2.5, and the reverse rectifier cells in a parallel configuration constructs a DDCCB rectifier with a symmetric DC output capability. Fig.3.2 illustrates the structure of a symmetric DDCCB rectifier. The normal DDCCB rectifier is located at the top of the figure, and generates a positive DC voltage as V_{DD} while the reverse DDCCB rectifier is at the bottom, and generates a negative DC voltage at the output as V_{SS} to drive the load system R_L.

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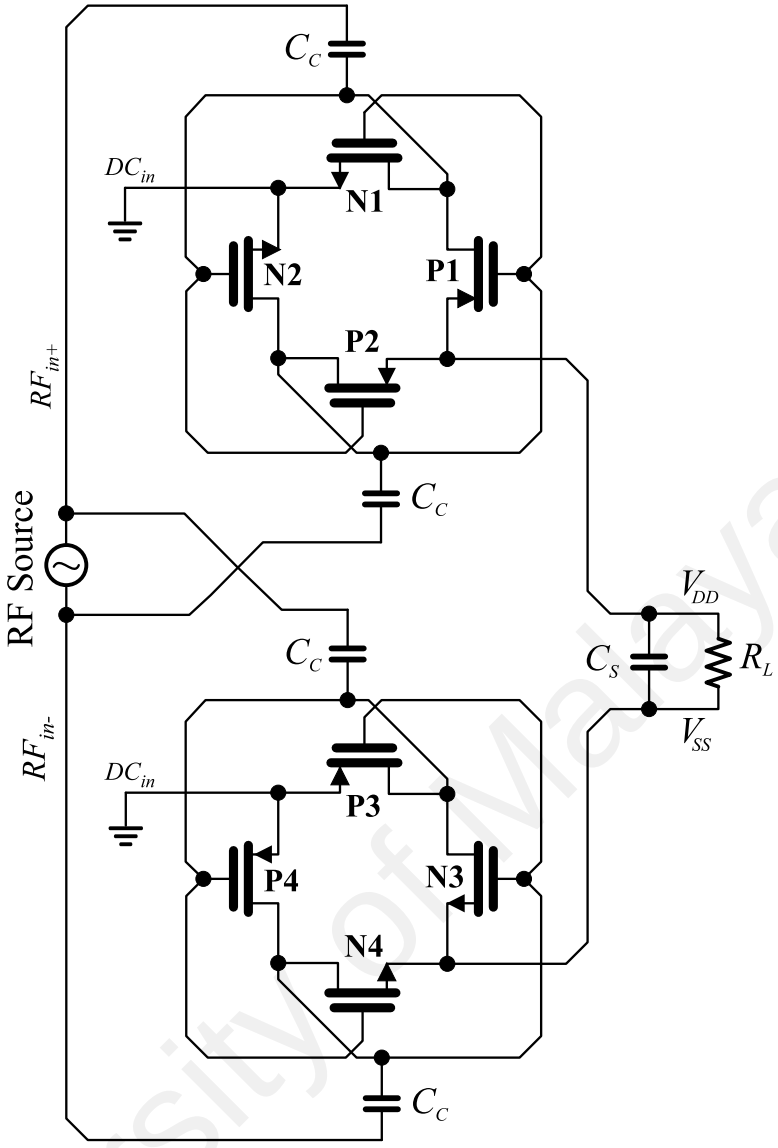

Figure 3.2: Combining the normal and the reverse DDCCB rectifier cells to construct a rectifier with a symmetric DC output capability.

3.3 Body-biasing for DDCCB rectifier

The body-source potential (V_{sb}) is directly related to the threshold voltage of a MOSFET transistor and often used to manipulate the threshold voltage through a method referred to as dynamic voltage-threshold scaling (DVTS) technique (Mehta & Amrutur, 2012). As mentioned, threshold voltage (V_{th}) of a n-type or p-type MOSFET transistor in the forward bias is expressed as (Razavi, 2008):

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$$V_{thN} = V_{th0N} + \gamma \left(\sqrt{|2\Phi_F + V_{sb}|} - \sqrt{|2\Phi_F|} \right) \tag{3.7}$$

$$V_{thP} = V_{th0P} - \gamma \left(\sqrt{|2\Phi_F - V_{sb}|} - \sqrt{|2\Phi_F|} \right) \tag{3.8}$$

where V_{th0N} and V_{th0P} are the threshold voltages when V_{sb} is zero. γ is the body effect coefficient and $2\Phi_F$ is the surface potential coefficient.

In reference to the classic theory, the leakage current in the reverse bias mode can also be determined as (Razavi, 2008):

$$I_{leakage} = I_0 . \left(\frac{W}{L}\right) . \left(e^{\frac{V_{gs} - V_{th}}{nV_T}} \right) . \left(1 - e^{\frac{-V_{ds}}{V_T}} \right) \tag{3.9}$$

where I_0 is a process-dependent parameter, V_T is the thermal voltage and W/L is the aspect ratio of the transistors. The channel-length modulation effect is negligible for the operation frequency lower than C-band and further strengthen by the fabrication in channel length of 130 nm. For higher frequency bands operation and sub-micron CMOS technology, the effect of channel-length modulation becomes more conspicuous and should be taken into account.

In reference to equations (3.7) and (3.8), V_{th} can be only be manipulated by V_{sb} since other parameters are strictly dependent upon the material properties of the CMOS process, which are not easily adjustable unless the design is implemented in a customized process, which causes an increase in the fabrication cost. In addition, a trade-off between the threshold voltage and the leakage current usually exists, which limits the degree of freedom for threshold voltage reduction [see Eq.(3.9)]. Thanks to the inherent feature of the DDCCB rectifier, the leakage current is considerably restrained, which has been thoroughly discussed in Section 2.5. Hence, it is feasible to reduce the threshold voltage

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to some extent by regulating V_{sb} without any major increase in the reverse leakage current especially for p-type MOSFET transistors since the N-wells are isolated, and allow the body to be freely biased. However, excessive threshold voltage reduction translates into PCE degradation, which will be explained in Section 5. It should be noted that n-type MOSFET transistors are required to be implemented in a triple-well, also known as deep N-well (DNW), structure in order to be able to independently bias the body of n-type MOSFET transistors. Fig. 3.3 depicts the simulation result of V_{th} as a function of V_{sb} for a p-type MOSFET transistor while the drain-to-source voltage (V_{ds}) is set to -3.0 V and the width of transistor is set to 20 μm with 130 nm of length. The V_{th} curve shows a gradual drop as V_{sb} increases till the PN junction between the source and the body turns "on" ($V_{sb} > 0.7$ V). When the PN junction turns "on", the current leaks even in the forward bias through the body. Further increase does not affect V_{th}. Therefore, the body biasing of rectifier's p-type MOSFET transistors can be regulated in order to decrease the V_{th}. Fig.

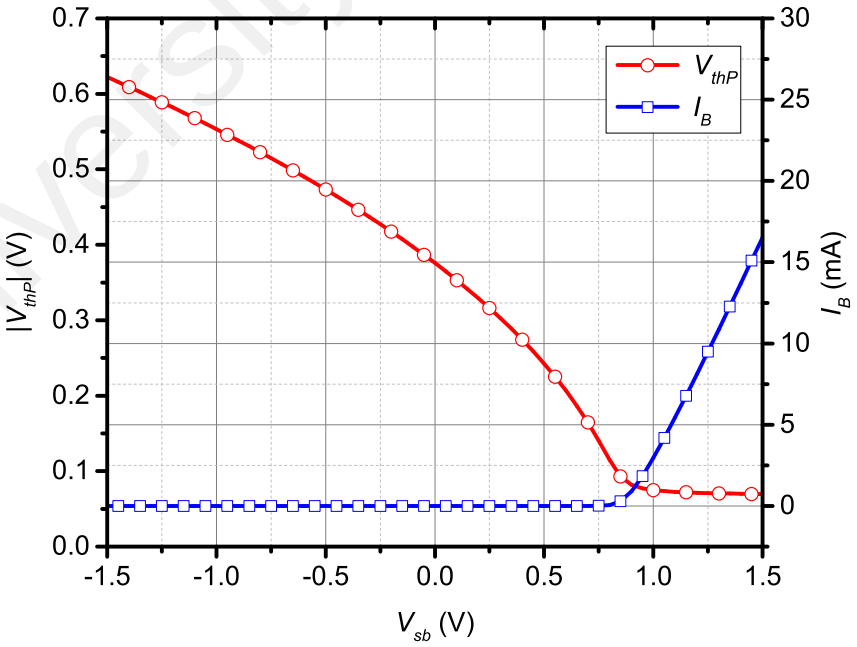

Figure 3.3: Simulated threshold voltage and body current variation as a function of V_{sb} for a p-type MOSFET transistor.

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3.4 depicts the simulation result of V_{th} as a function of V_{sb} for a n-type MOSFET transistor with an identical condition and parameter values as explained for the p-type transistor. The V_{th} of an n-type transistor shows a gradual drop as V_{sb} decreases till the PN junction between the source and the body turns "on" (V_{sb} > 0.6 V). It should be noted that the PN junction between the body and the source of an n-type transistor comparatively turns "on" with lower voltage than of the p-type transistor. When the PN junction turns "on", the current leaks even in the forward bias through the body in a n-type transistor. Further increase does not affect V_{th}. Therefore, the body biasing of rectifier's n-type MOSFET transistors can also be regulated in order to decrease the V_{th}.

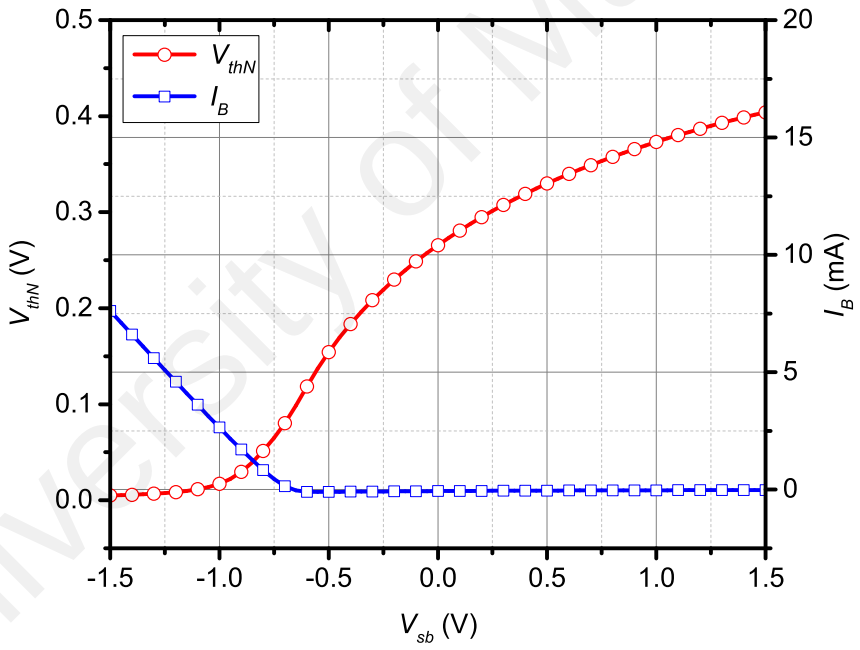

Figure 3.4: Simulated threshold voltage and body current variation as a function of V_{sb} for a n-type MOSFET transistor.

3.3.1 Multi-stage DDCCB rectifier structure

A single stage rectifier does not usually generate sufficient DC voltage at the output to sustain the subsequent blocks in a wireless sensor node. To achieve a larger output DC voltage, a multi-stage structure can be used. Otherwise, an additional DC-DC booster or

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voltage multiplier is required.

In a multi-stage DDCCB rectifier, the cells are stacked in series through the extracted DC path and connected in parallel via C_C to the input terminals, which feed the rectifier with RF signals (it is usually emulated by a sinusoidal voltage source). The number of stages is usually determined by the required output voltage, which is dependent on the harvester application. Fig.3.5 depicts a double-rail three-stage DDCCB rectifier driving a load (R_L). Smoothing capacitor (C_S) is usually connected in parallel with the load to mitigate the ripple at the output. It should be noted that in Fig.3.5 the above rail, which consists of three normal DDCCB rectifier cells converts the RF signal into a positive DC voltage as V_{DD} while the bottom rail converts the RF signal into a negative DC voltage as V_{SS}.

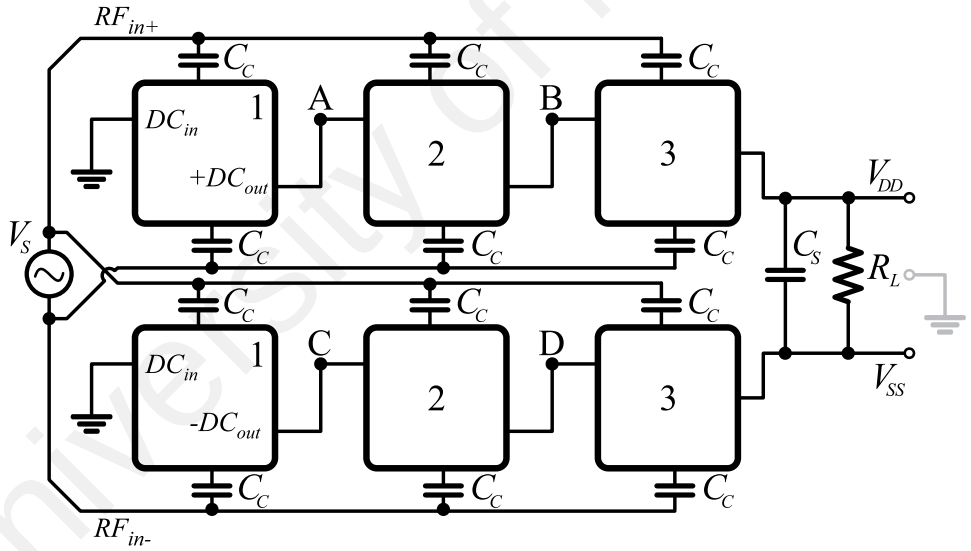

Figure 3.5: Proposed a symmetric multi-stage DDCCB rectifier configuration with double-rail three-stage configuration.

As mentioned, the voltage of transistors' body can be configured to moderately control V_{th}. The regulated V_{th} provides a condition for the rectifier to operate with a dynamic efficiency. As concluded in Section 3.3, for the p-type MOSFET transistors in the DDCCB rectifier, V_{sb} should be configured with a positive DC voltage to minimize the body effect especially for smaller received power. In other words, V_b is required to be

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biased by a lower DC voltage than V_s. In the DDCCB rectifier structure, this DC voltage can be provided from each cell output. Fig.3.6 depicts each cell output (A, B, C, D, V_{DD} and V_{SS} of Fig.3.5) versus input power to drive a 100 kΩ load at 953 MHz operating frequency when SB biasing technique is adopted. The generated DC voltage level in each cell varies by amount of input power as shown in Fig.3.6. Due to the symmetric capability of the rectifier, both negative and positive DC voltages are provided. Therefore, the body of p-type MOSFET transistors should be connected to DC_{in} in the positive rectifier rail while they should be connected to the DC_{out} for the negative rectifier rail in order to allow V_{sb} to be set by a positive value.

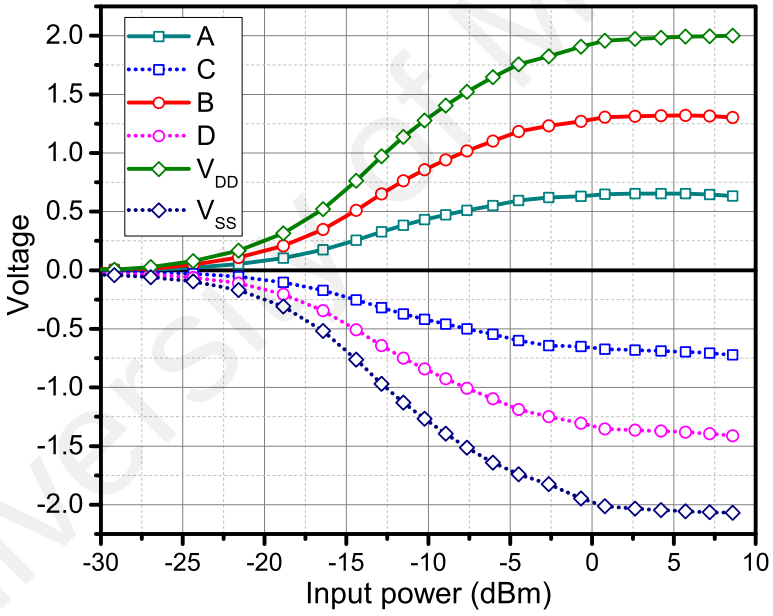

Figure 3.6: Generated DC voltage in each cell versus input power in the DDCCB rectifier using SB self-body-biasing technique at 953 MHz driving a 100 kΩ.

3.4 Proposed a symmetric self-body-biased DDCCB rectifier

As explained in Chapter 2, a DDCCB rectifier is composed of 4 transistors as 2 n-type and 2 p-type MOSFETs. Therefore, a proper self-body biasing technique is proposed to regulate the V_{sb} and alleviate the threshold voltage of the p-type MOSFET transistors in the

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symmetric multi-stage DDCCB rectifier. Therefore, the body of the p-type transistors is required to be connected to the input DC (DC_{in}) of each cell in the positive rectifier rail and to the output DC ($-DC_{out}$) of each cell in the negative rectifier rail as depicted in Fig.3.7. However, the body of n-type MOSFET transistors are tied to the source. Therefore, in this configuration, which is referred to as LDCF self-body biasing technique, the n-type transistors operate with non-scalable V_{th} since the V_{sb} is 0 while the p-type transistors operate with a scalable V_{th} since V_{sb} of the p-type transistors is no longer equal to zero. In Chapter 4, it will be discussed, adopting the LDCF technique is significantly effective in order to improve the performance of the DDCCB rectifier.

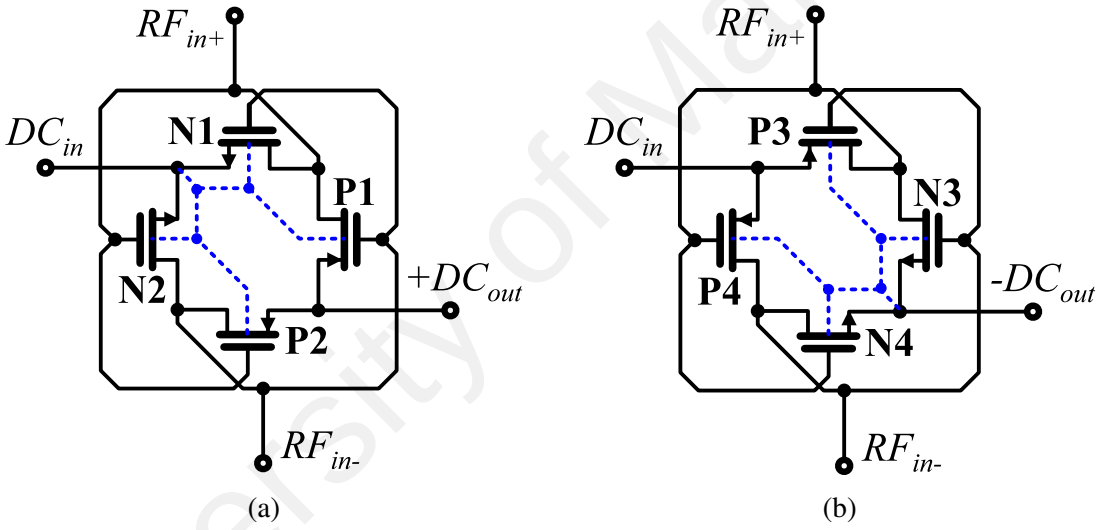

Figure 3.7: Circuit configuration of proposed LDCF body biasing technique for DDCCB rectifier. a) positive b) negative rectifier.

Constructing a multi-stage rectifier based on Fig.3.5 and adopting LDCF body biasing technique allows the p-type transistors' body to be fed by the self-generated DC voltage in the DDCCB rectifier. Fig.3.8(a) depicts the complete structure of the proposed rectifier with capability of generating symmetric DC voltage at the output while using a self-body-biasing technique as LDCF. The structure is adopted a double-rail three-stage configuration. The positive rail, which is highlighted with a gray dotted line above the structure is responsible to convert the RF power into positive DC voltage as V_{DD} while the

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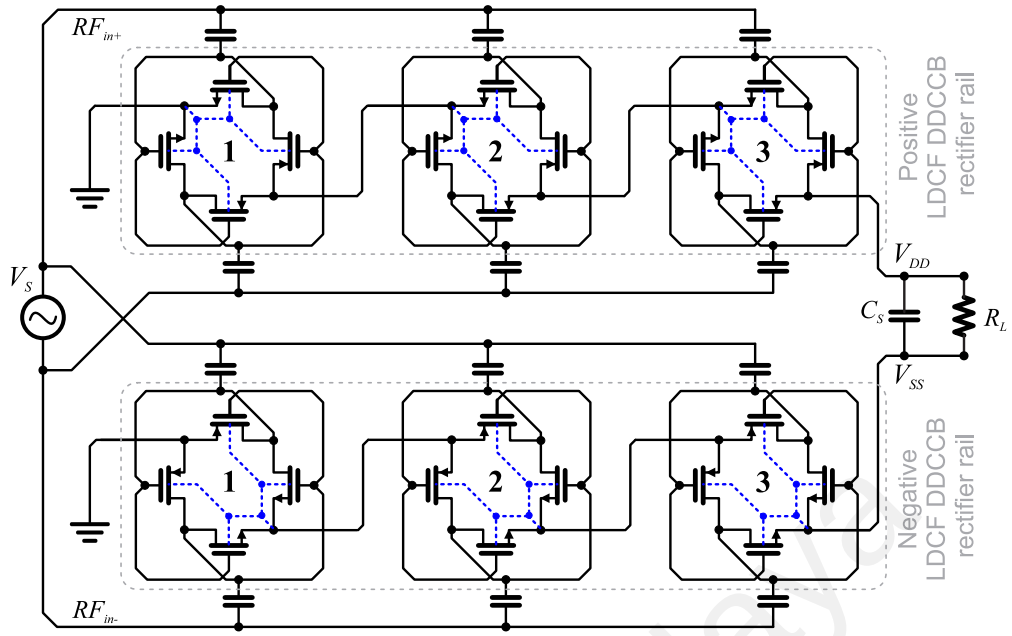
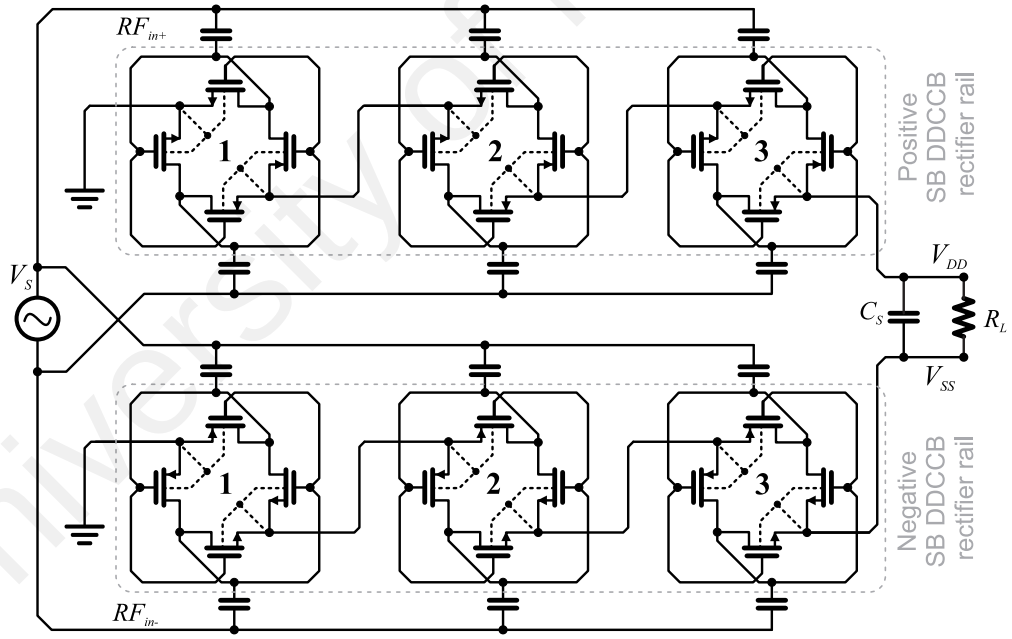


(a)



(b)

Figure 3.8: Circuit configuration of proposed symmetric DDCCB rectifiers using self-body-biasing techniques with capability of generating a positive and negative DC voltages. a) LDCF technique. b) SB technique.

negative rail at the bottom of the structure generates negative DC voltage as V_{SS}. The total DC voltage generated at the output drives the load system with a parallel C_S. A similar circuit configuration can be constructed for the conventional self-body-biasing in which

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the body of the transistors is tied to the source, which is here referred to as SB technique. Fig.3.8(b) illustrates a DDCCB rectifier adopting the SB self-body-biasing technique in a double-rail three-stage configuration.

3.4.1 Other proposed self-body-biasing techniques

In this Section, other alternative self-body-biasing techniques are proposed. The body of the transistors in the DDCCB rectifier can also be connected to the drain, which is referred to as drain-to-body (DB) technique as depicted in Fig.3.9. The DB technique requires DNW implementation since the body of the n-type transistors is not tied to the source, which needs to be isolated from the substrate.

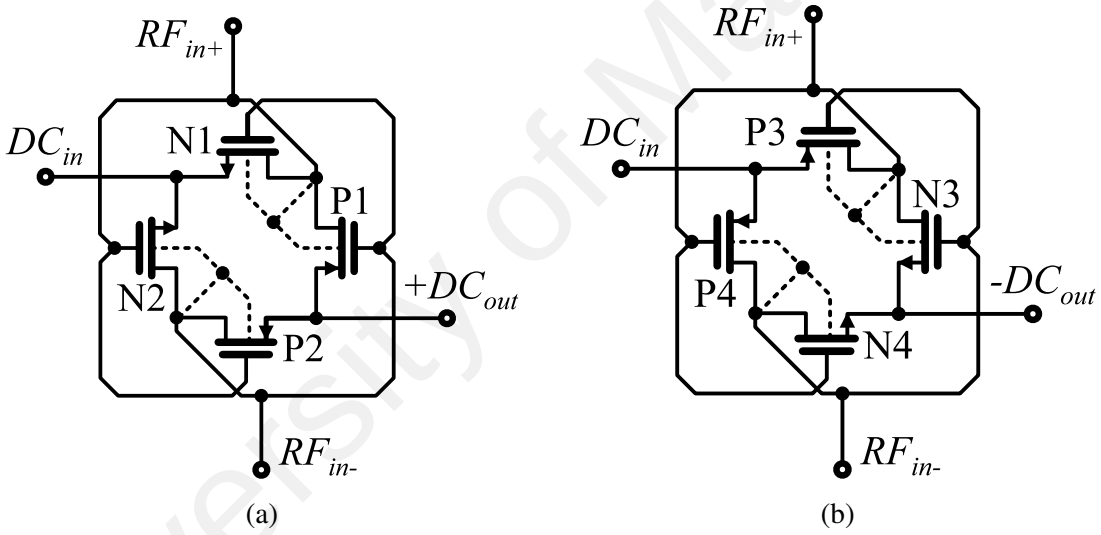

Figure 3.9: Circuit configuration of proposed DB body biasing technique for DDCCB rectifier. a) positive b) negative rectifier.

The DB self-body-biasing technique can be used to construct a multi-stage rectifier in which the body of all transistors are connected to the drain in the DDCCB rectifier structure. Fig.3.10 illustrates the complete circuit configuration of the DDCCB rectifier adopting DB technique in a double-rail three-stage configuration.

Other local nodes with DC voltage level in the adjacent or other stages in a multi-stage DDCCB rectifier can also be used to bias the body of the MOSFET transistors. For example, in identical higher DC feeding (IHDCF) technique, the body of all MOSFET

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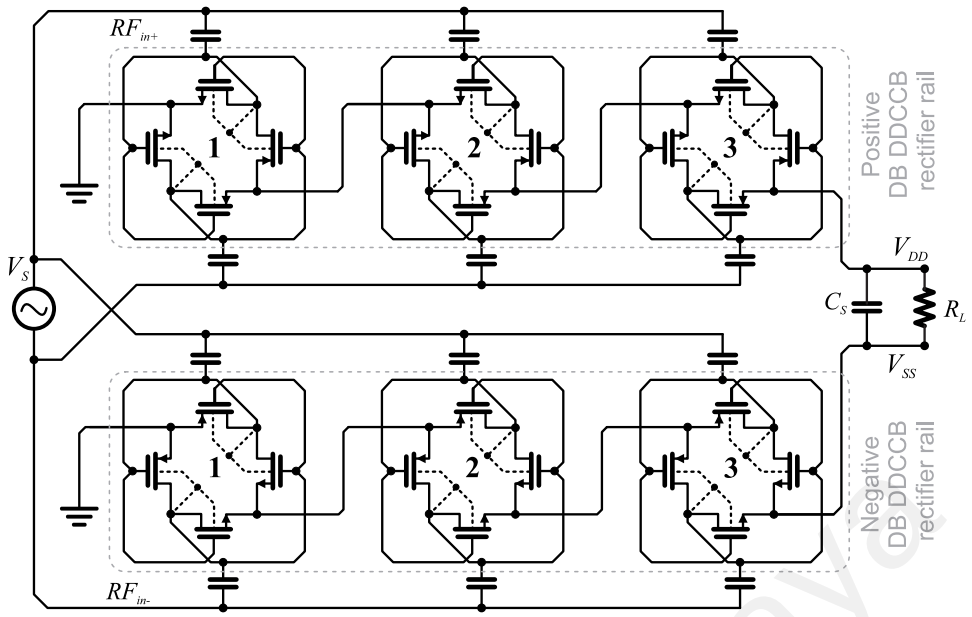

Figure 3.10: Circuit configuration of proposed symmetric DDCCB rectifiers using DB self-body- biasing technique with capability of generating positive and negative DC voltage.

transistors in each rectifier rail are connected to the higher generated DC voltage level in the multi-stage DDCCB rectifier. To be more precise, the body of n-type and p-type transistors in the positive rectifier rail are connected to the V_{DD}, which presents the higher DC voltage level in the rail in the structure. In the negative rectifier rail, the body of the transistors are connected to the ground, which presents the higher DC voltage level in the rail. Fig.3.11(a) shows the complete circuit configuration of the multi-stage DDCCB rectifier adopting the IHDCF self-body-biasing technique in a double-rail three-stage configuration.

In hybrid DC feeding (Hybrid-DCF) technique, the first stage in the positive and negative rectifier rail is similarly biased with a similar body biasing for the other two stages in each rectifier rail. In other words, in the first stage of the multi-stage Hybrid-DCF rectifier, the body of n-type and p-type transistors is connected to a lower DC voltage as DC_{in} with respect to the DC_{out} in the positive rectifier rail, and the DC_{in} of the first stage is connected to the common ground. In the first stage of negative rectifier rail, the body of the transistors is also connected to DC_{in}, which is also connected to the common

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ground, as a higher DC voltage with respect to the $-DC_{out}$. The body of the transistors in the other two stages are connected to the highest DC voltage, which is V_{DD} in the positive rectifier rail. In the negative rectifier rail, the body of the transistors in the other two stages are connected to the lowest DC voltage, which is V_{SS}. Fig.3.11(b) illustrates the complete circuit configuration of the multi-stage DDCCB rectifier adopting Hybrid-DCF self-body-biasing technique in a double-rail three-stage configuration.

3.5 Summary

In this chapter, a new symmetric DDCCB rectifier structure has been introduced in order to give the rectifier the ability of generating symmetric DC voltage at the output. Moreover, four self-body-biasing techniques have been introduced to improve the performance of the rectifier. In the next chapter, the LDCF and SB techniques will be implemented on two DDCCB-based rectifiers with identical design parameters to verify the technique. The measurements setups and procedures will be explained, and the performance of the LDCF rectifier will be discussed.

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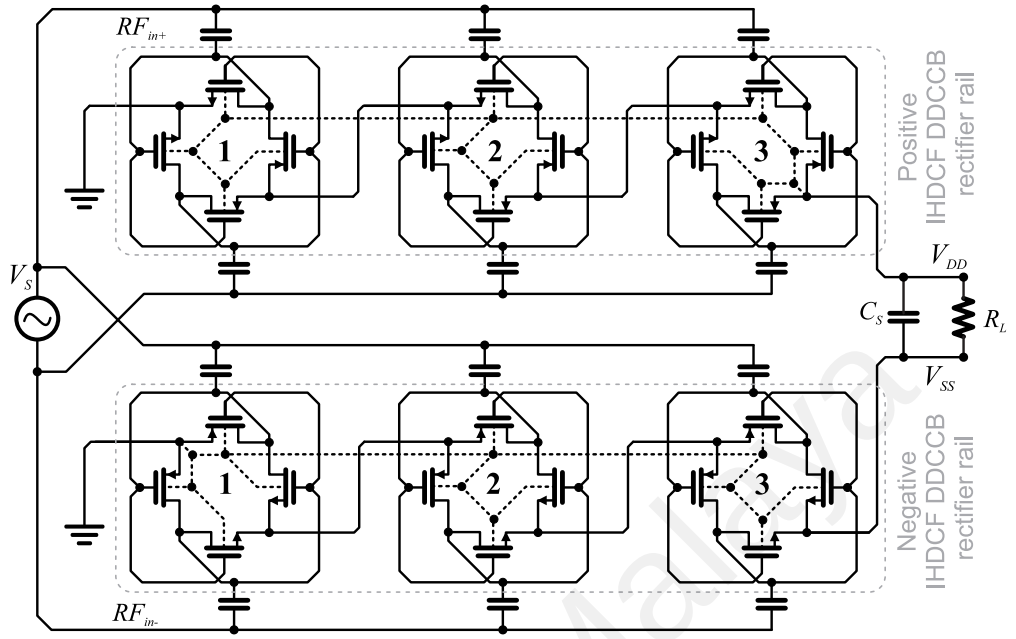
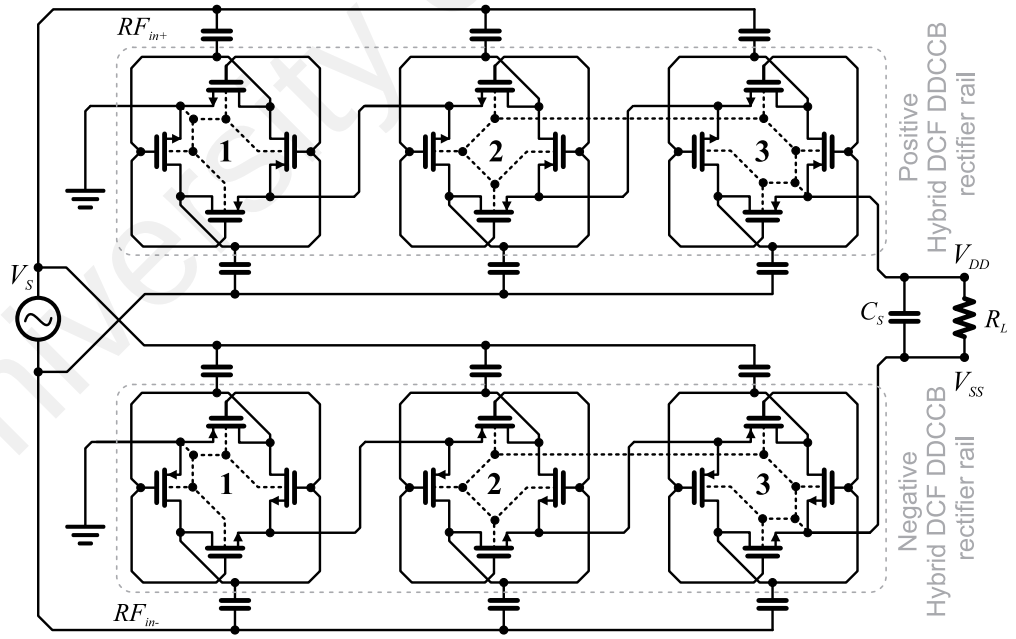


(a)



(b)

Figure 3.11: Circuit configuration of proposed symmetric DDCCB rectifiers using self-body biasing techniques with capability of generating positive and negative DC voltage. a) IHDCF technique. b) Hybrid-DCF technique.

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CHAPTER 4: RESULTS AND DISCUSSIONS

4.1 Introduction

The methods and techniques that have been used and adopted to verify the proposed structures in Chapter 3 is presented in this chapter. Both simulation and experimental setup will be explained as well. The proposed structures have been confirmed by multiple iteration in the simulation and one of them has been verified by experimental results through the measurement and characterization.

The performance of all the proposed rectifiers, which have been proposed in Chapter 3 are discussed and compared, based on the simulation results, in terms of PCE performance parameter in this chapter. The two designs with self-body-biasing techniques i.e. LDCF and SB were sent for fabrication. However, other proposed rectifiers do not considerably improve the performance of the DDCCB rectifier. Therefore, they are not fabricated to obtain experimental results.

The performance of LDCF and SB rectifiers are discussed and compared based on the measurement results in terms of DC output voltage and PCE. According to the measurement results, the LDCF rectifier outperforms the SB rectifier.

4.2 Simulation and Experiment

4.2.1 Chip design

In Chapter 3, four self-body-biasing techniques have been introduced for DDCCB-based rectifier structure. The self-body-biasing techniques have been named as LDCF, DB, IHDCF, and Hybrid-DCF. The techniques along with conventional SB technique have been implemented in separate rectifiers with identical design specifications to evaluate the performance of the proposed structures. Cadence Virtuoso as a circuit simulator has been used via SILTERRA process design kit (PDK) in a standard 130 nm CMOS technology

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Table 4.1: Components' value of the proposed rectifiers

Component	Value
C_C	600 fF
C_S	3.2 pF
Total Width n-type	25 μm
Total Width p-type	40 μm
Length n&p-type	130 nm

to simulate and confirm the design parameters. The rectifiers were designed with total transistor width of 25 μm and 40 μm with equal 5 fingers for n-type and p-type MOSFET transistors respectively. The length of 130 nm was chosen for both type of transistors. This aspect ratio between n-type and p-type transistors approximates the ON-resistances be almost identical. metal-insulator-metal (MIM) type of on-chip capacitor was selected as coupling and smoothing capacitors. 600 fF MIM C_Cs as coupling capacitors were deliberately implemented so that its effect on the conversion efficiency is not considerable. A 3.2 pF MIM C_S as smoothing capacitor was selected in order to mitigate the output ripple. The value of C_S was determined by simulation. It should be noted that smaller C_S causes more ripple at the output while larger value translates to slower operation in terms of setup time. Table 4.1 lists the components' value, which have been used to design all the four proposed rectifiers. The components' value were obtained after multiple iterations so that they do not considerably degrade the PCE. It should be noted that a preliminary simulation results indicate that the rectifier adopting the LDCF technique exhibits significant improvement and other techniques are not very successful candidate to improve the performance of the DDCCB rectifier in terms of PCE. Hence, other techniques have not been selected for the layout extraction process, and only LDCF and SB techniques have been proceeded to the layout extraction and fabrication process. Further discussion about the performance of the other techniques will be covered in Section 4.4 of this chapter.

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The layout of LDCF and SB rectifiers have been designed and extracted as illustrated in Fig. 4.1 based on the proposed structures in Fig.3.8(a) and Fig.3.8(b). Both LDCF and SB rectifiers have been located in a complete chip for the purpose of fabrication. Fig.4.2 depicts the layout of the complete chip.

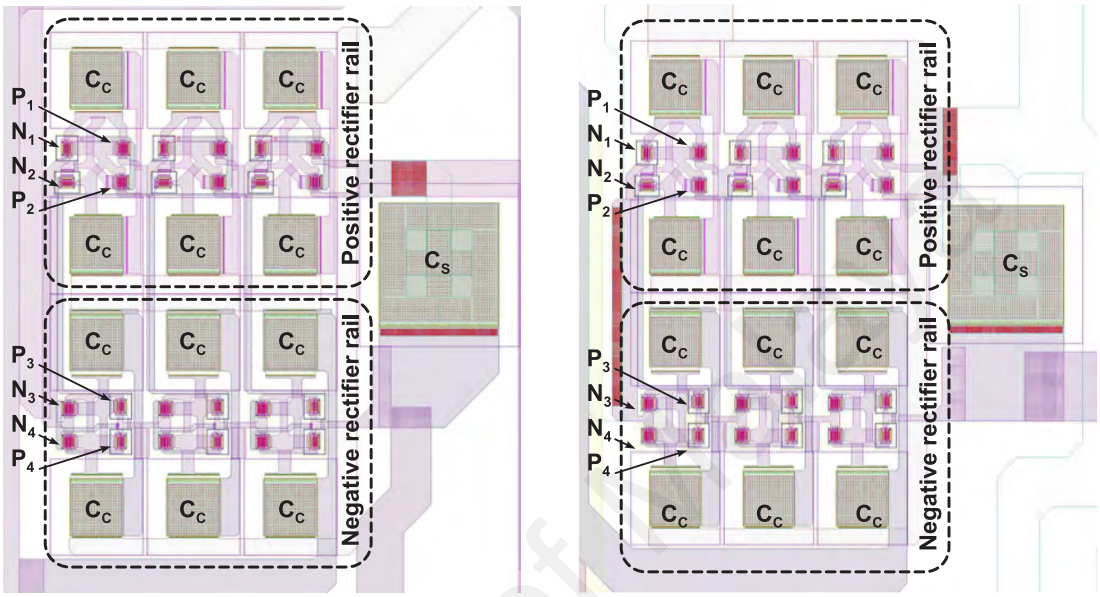

Figure 4.1: The proportional layout of the double-rail three-stage DDCCB rectifiers adopting a) LDCF b) SB self-body-biasing technique.

The complete layout has been fabricated in a standard 130 nm CMOS process and the die photograph of the chip is illustrated in Fig. 4.3 with a total chip area consumption of 0.954 mm^2 including the RF pads. An active area of 0.029 mm^2 was dedicated to each rectifier. The substrate loss is negligible due to the selected frequency and the length of the transistors. Hence, no de-embedding block is needed to be integrated to the chip. The RF pad in the design kit offers electrostatic discharge (ESD) protection capability, which requires the pads to be biased by a DC voltage. All the RF pads were biased with 3.0 V and ground except the RF pads, which are associated to V_{SS} (output of the negative rectifier rail) signals were biased with -3.0 and 3.0 V to keep the original signals, and prevent any power dissipation by the ESD circuits.

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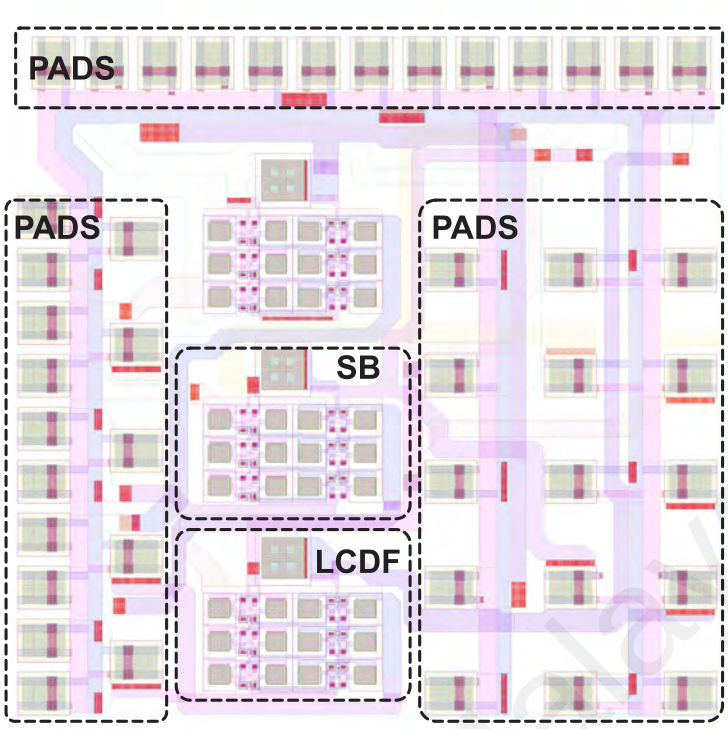

Figure 4.2: Complete layout of the chip including LDCF and SB rectifiers.

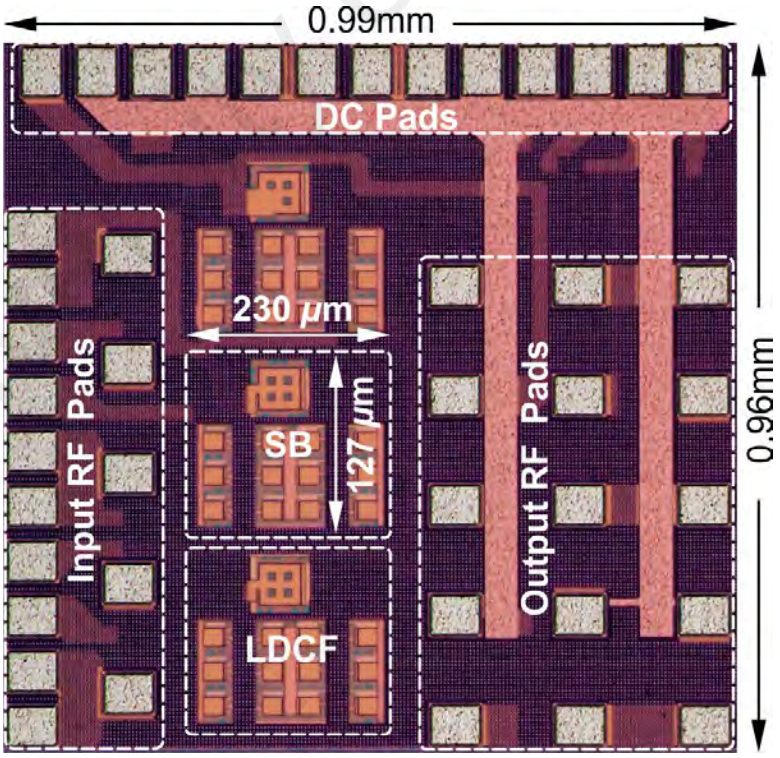

Figure 4.3: Photomicrograph of the fabricated rectifiers using the SB and LDCF body biasing techniques

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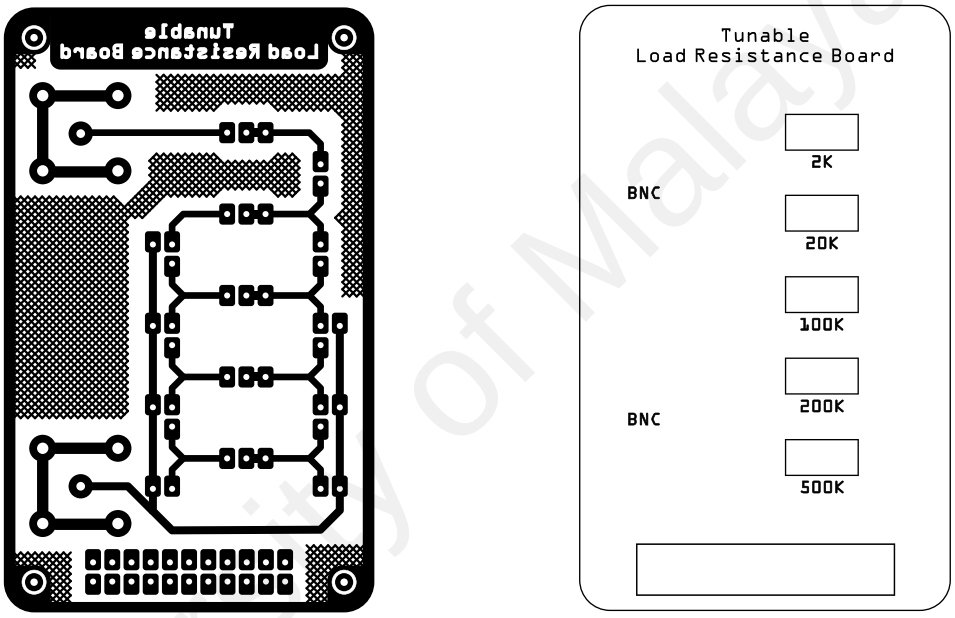
4.2.2 PCB design

A flame retardant 4 (FR4) printed circuit board (PCB) was implemented in order to realize a variable resistor to emulate the load system R_L and subsequently to evaluate the rectifiers under different load conditions. A computer-aid design software, CorelDRAW, is used to draw the PCB layout.Fig. 4.4 shows the design of the PCB. The PCB has also been fabricated, and Fig. 4.5 depicts the photo of the fabricated PCB. The PCB is capable of being tuned between 1 kΩ and 800 kΩ as a load for the rectifiers.



(a) (b)

Figure 4.4: Layout of the variable resistor. a) Bottom layer b) Label layer.

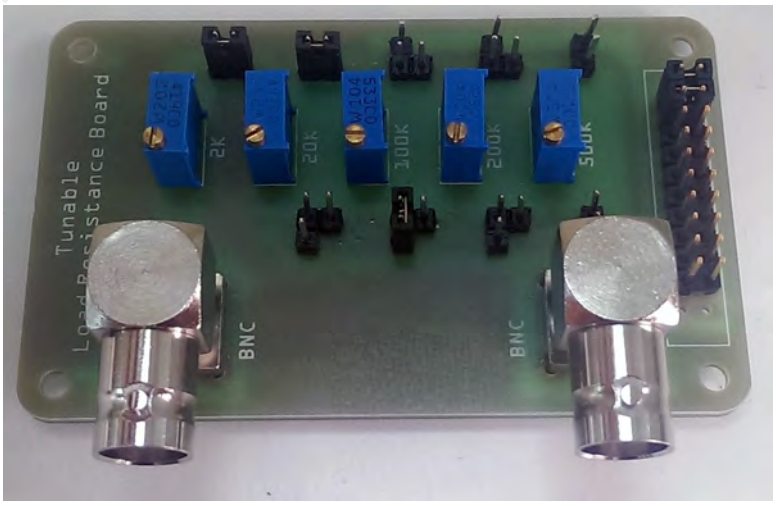


Figure 4.5: Photo of the fabricated variable resistor in an FR4 PCB .

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4.3 Measurement setups and procedures

An on-wafer probing technique was used to evaluate and measure the rectifiers' performance parameters. Two differential probes were dedicated for the input and output. An E8267D power signal generator (PSG) was used along with a broadband balun in order to generate a differential signal and eventually to drive the rectifiers. The total output DC voltage, which is equal to $V_{DC} = V_{DD} - V_{SS}$ was measured using a digital multimeter. Fig. 4.6 shows the configuration of the measurement setup. To carry out an accurate

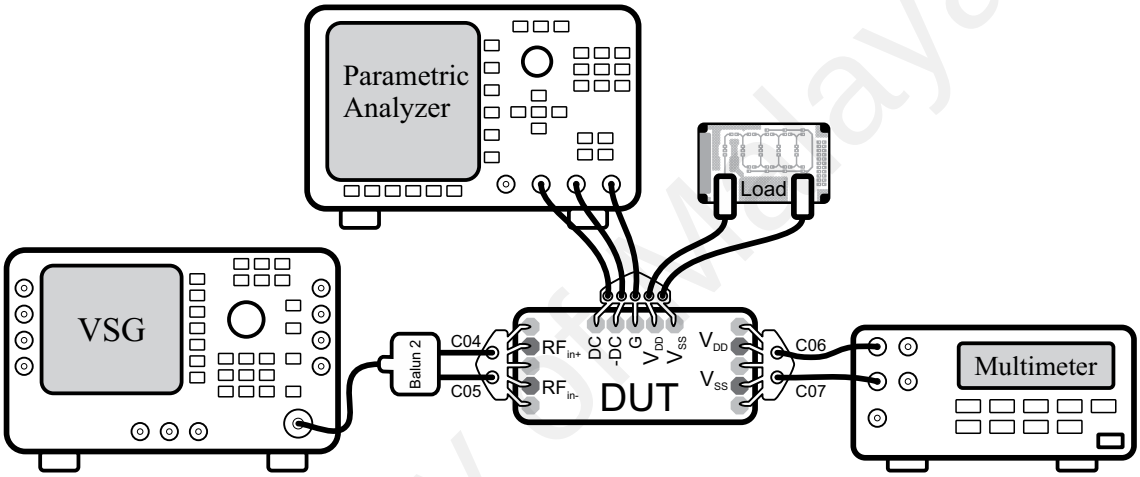

Figure 4.6: Measurement setup configuration for evaluating the performance of SB and LDCF rectifiers in terms of V_{DC}.

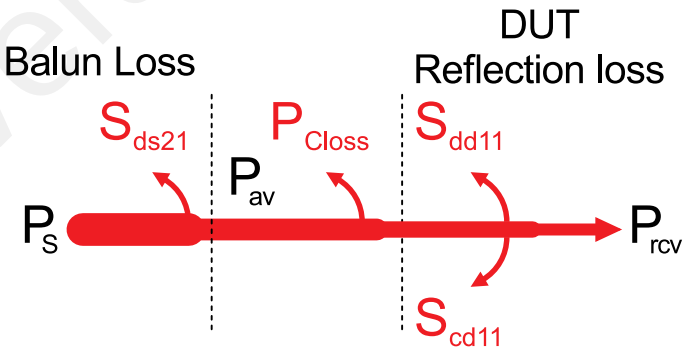

Figure 4.7: Power dissipation from source to DUT.

measurement procedure, the performance of both SB and LDCF rectifiers have been measured taking all the power losses up to the device under test (DUT). The power losses are depicted in Fig.4.7 where P_S is the power generated by PSG, S_{ds21} represents the insertion loss by the balun, P_{av} is the available power at the balun's output, P_{closs} denotes the power

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losses through the cables, while S_{dd11} and S_{cd11} are the rectifiers' reflection coefficients for differential-to-differential and differential-to-common modes respectively, and P_{rcv} is received power by the rectifiers. The rectifiers' PCE can be calculated as

$$PCE(\%) = \frac{P_{DC}}{P_{rcv}} \times 100 \tag{4.1}$$

where P_{DC} is the power delivered to the load system or the consumed power by the R_L. P_{rcv} were obtained by using the equation:

$$P_{rcv} = (P_{av} - P_{closs}).(1 - |\, S_{dd11} \,|^2 - |\, S_{cd11} \,|^2) \tag{4.2}$$

where

$$P_{av} = (P_S).(1 - |\, S_{ds21} \,|^2) \tag{4.3}$$

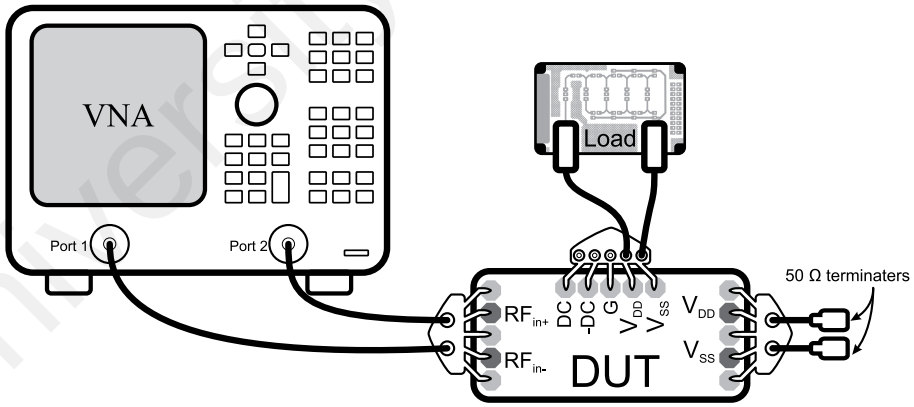

Figure 4.8: Measurement setup for extracting standard S-parameters of LDCF and SB rectifiers.

The reflection coefficients of the rectifiers have been extracted using E8364B PNA. The measurement setup for extracting the reflection coefficients is shown in Fig.4.8. Both SB and LDCF rectifiers are considered four-port networks. In addition, since the input of the rectifiers are differential, mixed-mode S-parameters are required to evaluate

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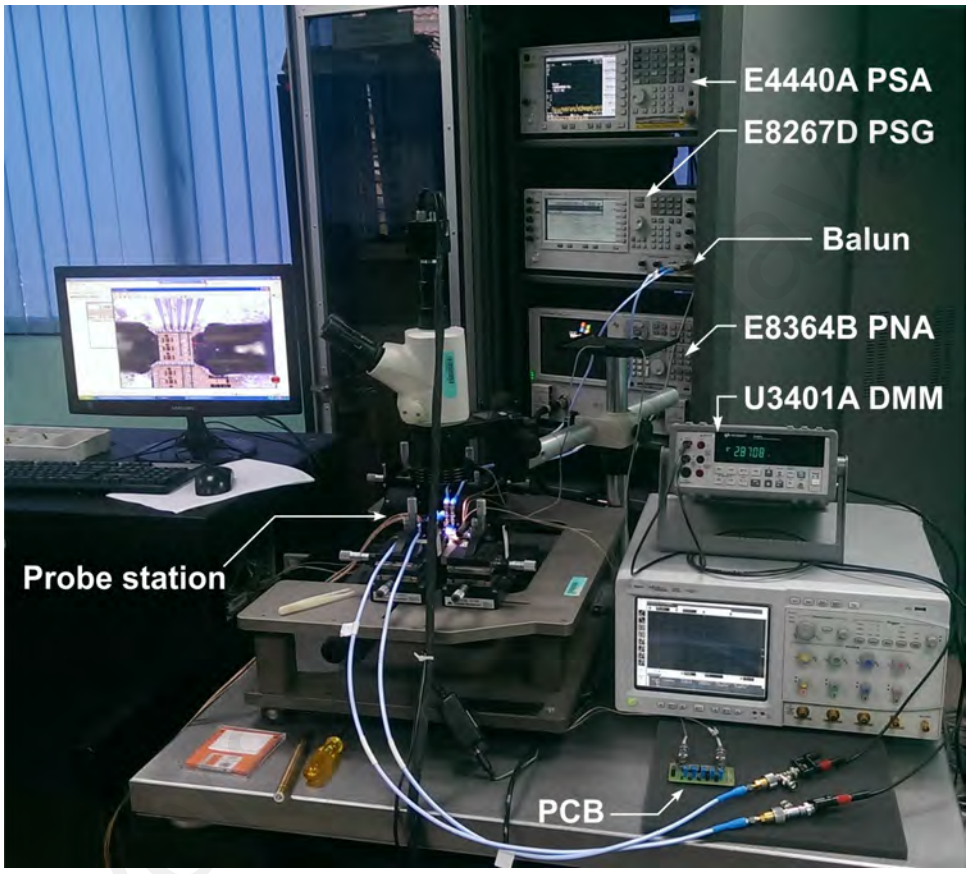
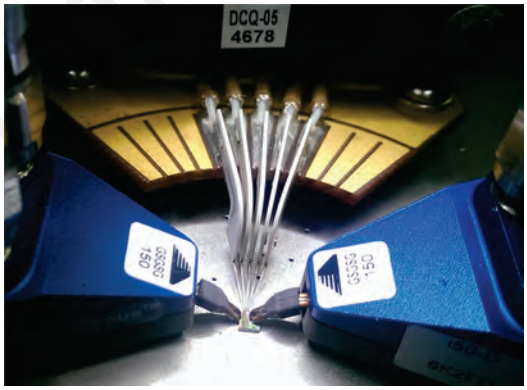
the rectifiers' performance. However, the available PNA did not come with mixed-mode measurement capability. Hence, standard S-parameters of the rectifiers have been extracted and transformed to the mixed-mode S-parameters as it was explained in Section 2.7.3. It should be noted that for extracting the reflection coefficients of the rectifiers, it requires a setup as depicted in Fig.2.25(a), which has been realized as in Fig.4.8. The balun was



(a)



(b)

(c)

Figure 4.9: Photograph of the probe station and equipment used for characterizing the SB and LDCF rectifiers. a) measurement setup. b)RF and DC Probes. c) wide-band balun.

also characterized via E8364B PNA. The loss of the cables were also considered and measured using E4440A power signal analyzer (PSA). The insertion loss of the balun were obtained using measurement of standard S-parameters, which can also be carried out by a two port PNA as explained in Section 2.7.4. Noted that a balun is a three port network but the same concept can be performed to extract the standard S-parameter of the balun. The mixed-mode S-parameters of the balun was extracted as explained in Section 2.7.3. DC power dissipation at the rectifier output (P_{DC}) can be obtained through the equation $P_{DC} = V_{DC}^2/R_L$. Fig. 4.9 shows a photo of complete instruments and facilities used to extract the performance of the rectifiers.

4.4 Simulation results

A preliminary simulation and comparison of all four proposed techniques including the SB technique, as the conventional body-biasing technique, for the DDCCB rectifier structure is depicted in Fig.4.10 in terms of PCE performance parameter under two different load conditions.

Under 20 kΩ load condition, the LDCF and SB techniques are significantly effective and improve the performance of the DDCCB rectifier in terms of PCE. However, other self-body-biasing techniques do not exhibit a significant improvement in the performance of the DDCCB rectifier. The PCE of the rectifiers increase as input power increases until it reaches to the maximum point and the PCE rapidly decreases. The rectifier with SB self-body-biasing technique comparatively operates with a higher maximum PCE. A peak PCE of 76% is achieved in the simulation for the SB rectifier under 20 kΩ load. The maximum PCE for the rectifier adopting LDCF technique is 75.3%. Although the maximum PCE of the SB rectifier is comparatively higher than the LDCF rectifier, the curve of the PCE is shifted to the right side of the input power for the LDCF rectifier, which indicates that the LDCF rectifier operates with better efficiency in the lower input

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power condition. Since the body of p-type transistors in the LDCF rectifier is biased with a lower voltage with respect to the source, the V_{th} of the transistors are reduced leading to PCE improvement in the lower input power. According to the simulation results improving the PCE of the DDCCB rectifier. Peak PCEs of 64.9%, 59.9%, and 32.1% are achieved in the simulation under 20 kΩ load for the rectifiers adopting DB, Hybrid-DCF, and IHDCF respectively. The performance of the LDCF and SB rectifiers are also significant under 100 kΩ, and both techniques improve the performance of the DDCCB rectifier in terms of PCE. The PCE curve is shifted to the lower input power since a larger load draw less current from the rectifiers. It should be noted that the LDCF rectifier performance is comparatively better since the PCE curve is relatively shifted to the right side of the input power compared to the SB and other self-body-biasing techniques. Under 100 kΩ load, peak PCEs of 73.5%, 73.1%, 53.6%, 47.3%, and 27.5% are achieved in the simulation for the SB, LDCF, Hybrid-DCF, DB, and IHDCF respectively.

The LDCF self-body-biasing technique has been selected for layout extraction and fabrication due to its significant improvement of the PCE in the DDCCB rectifier. As a conventional self-body-biasing technique, SB rectifier has also been selected for layout extraction and fabrication in order to present a performance comparison between the SB and LDCF techniques in the measurement.

Fig. 4.11 depicts the simulated transient response of the proposed RF-to-DC converter based-on DDCCB rectifier structure with a double-rail three stage configuration using the LDCF self-body biasing technique. The structure is driven by a differential RF signal (RF_{in+}, RF_{in-}) with a -2.49 dBm received power under 10 kΩ load. The proposed structure converts the RF signal into a positive and negative DC voltages (V_{DD}, V_{SS}). Fig. 4.11(a) depicts the waveform of the differential input RF signal and the transient response of the proposed LDCF rectifier as a symmetric DC output voltage for the first 20 ns. The

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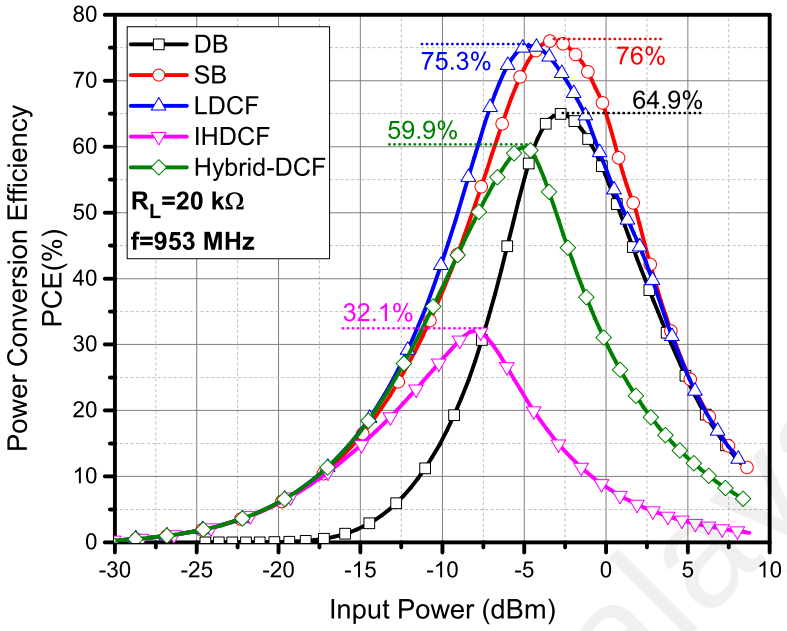
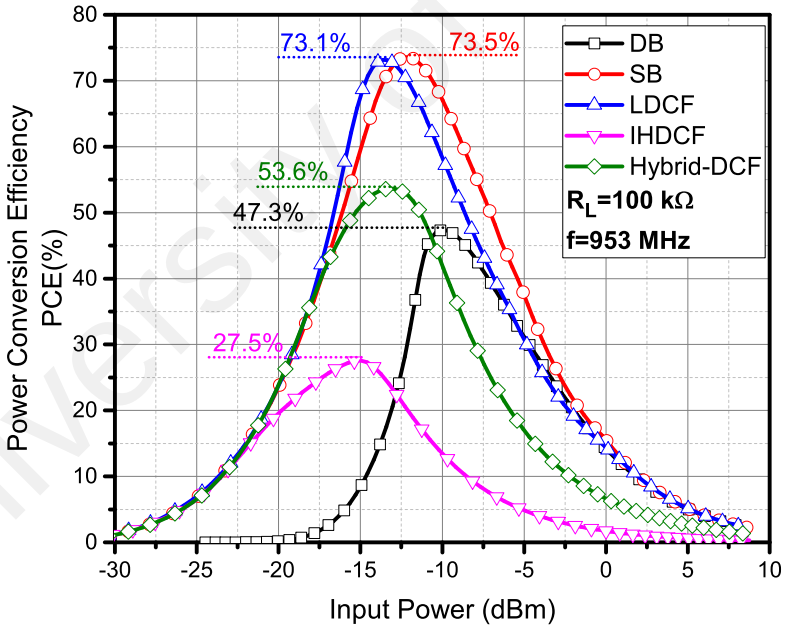


(a)



(b)

Figure 4.10: Simulated PCE of self-body-biasing techniques versus input power at 953 MHz under a) 20 kΩ b) 100 kΩ load.

converted RF power is gradually stored in the C_S and finally reaches to its steady-state after 100 ns, which depicted in Fig.4.11(b). The setup time to reach the steady state is strongly dependent upon the received power, the value of capacitors (C_C, C_S), and the load

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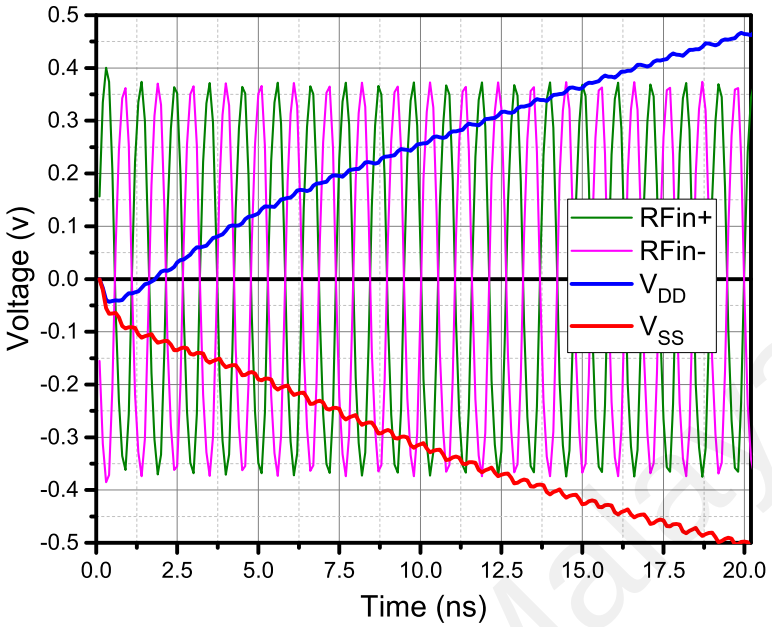
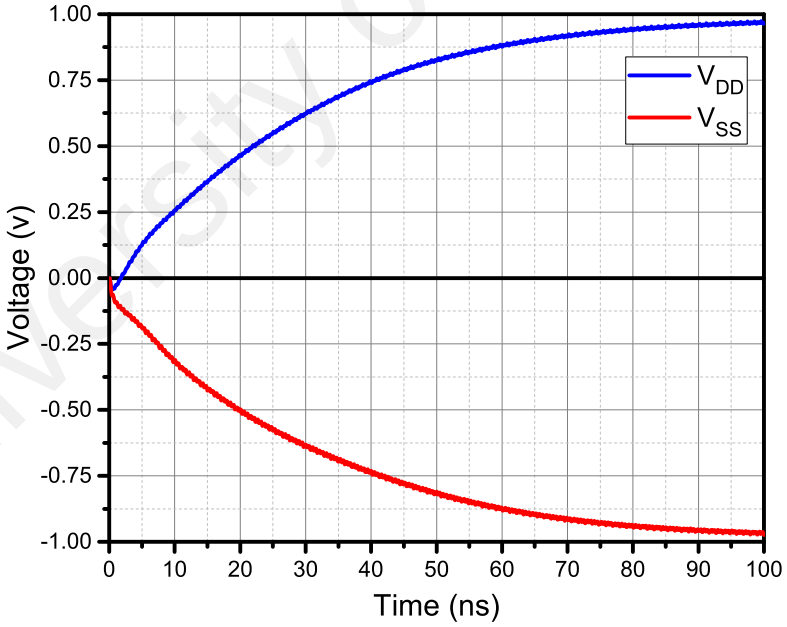
system (R_L).



(a)



(b)

Figure 4.11: Simulated results of proposed symmetric LDCF rectifier driven by -2.49 dBm power and under 10 kΩ load. a) up to 20 ns b) up to 100 ns.

In the positive rectifier rail, the body of the p-type transistors are biased by the DC output of (n-1) while they are biased by the output of (n+1) for the negative rectifier rail

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where n represents the cell number in Fig.3.5. Hence, the effective value of V_{sb} is always positive since $V_s > V_b$ for all cells. Here, V_{sbpxn} can be defined where x denotes the p-type number and n corresponds to the cell number. Therefore, in the positive and negative rectifier rails, the body of two p-type transistors in each cell are identically biased and it can be concluded that

$$\left\{\begin{array}{lll} V_{sbp11} = V_{sbp21} & \& & V_{sbp31} = V_{sbp41} \\ V_{sbp12} = V_{sbp22} & \& & V_{sbp32} = V_{sbp42} \\ V_{sbp13} = V_{sbp23} & \& & V_{sbp33} = V_{sbp43} \end{array}\right\} \tag{4.4}$$

Fig.4.12 depicts V_{sb} of all p-type transistors in a double-rail three-stage rectifier using the LDCF technique. The curves of V_{sb} are relatively equal over the range of input power between -35 dBm and 5 dBm. It can be concluded that all bodies are almost equally biased with the same potential and smaller than the source terminal of p-type transistors.

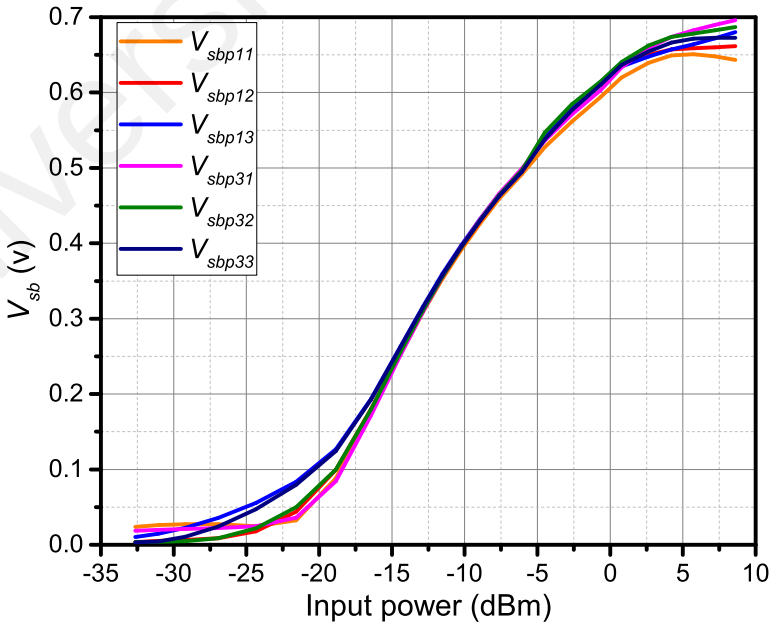

Figure 4.12: V_{sb} of p-type transistors in the LDCF DDCCB rectifier as a function of input power driving a 100 kΩ load.

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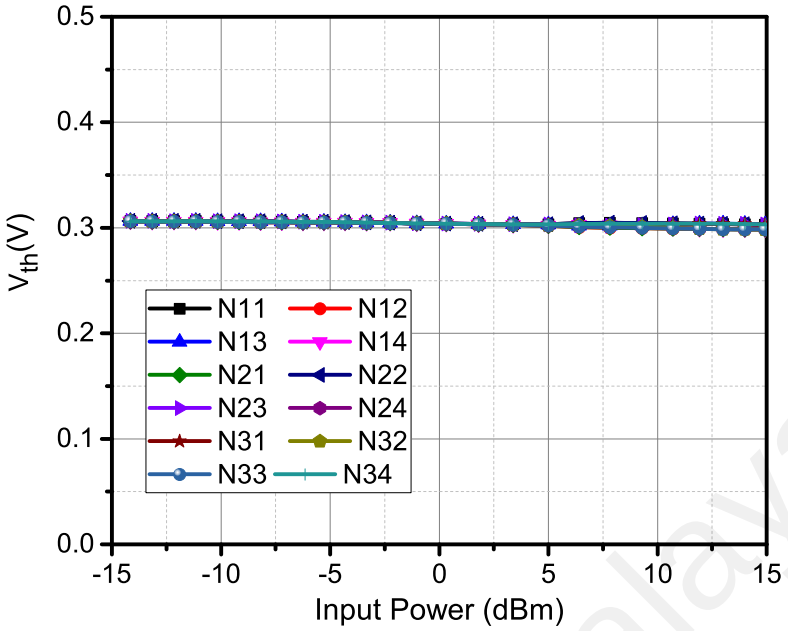

Figure 4.13: Threshold voltage of n-type transistors as a function of input power in the proposed symmetric LDCF rectifier under 100 kΩ load.

V_{sb} rises as input power increases leading to reduced V_{th}. It is interesting to note that the LDCF technique mitigates the threshold voltage when the input power is small while for higher input power the PN junction between the source and the body of p-type transistors turns "on" leading to current leakage through the body. Further discussion about the body leakage will be presented in the following sections in this chapter.

Fig.4.13 shows the variation of threshold voltage of n-type transistors in the LDCF rectifier. Since the source and the body of the n-type transistors are connected, V_{sb} is equal to zero and all n-type transistors in the structure operate with a static threshold voltage. Hence, no variation is observed in the threshold voltage of n-type transistors for the LDCF rectifier. On the other hand, since the body of p-type transistors are biased with a lower DC voltage with respect to the source, p-type transistors operate with a scalable threshold voltage depending on the received power. As input power increases V_{sb} increases causes the threshold voltage of the p-type transistors to decrease as depicted in Fig. 4.14.

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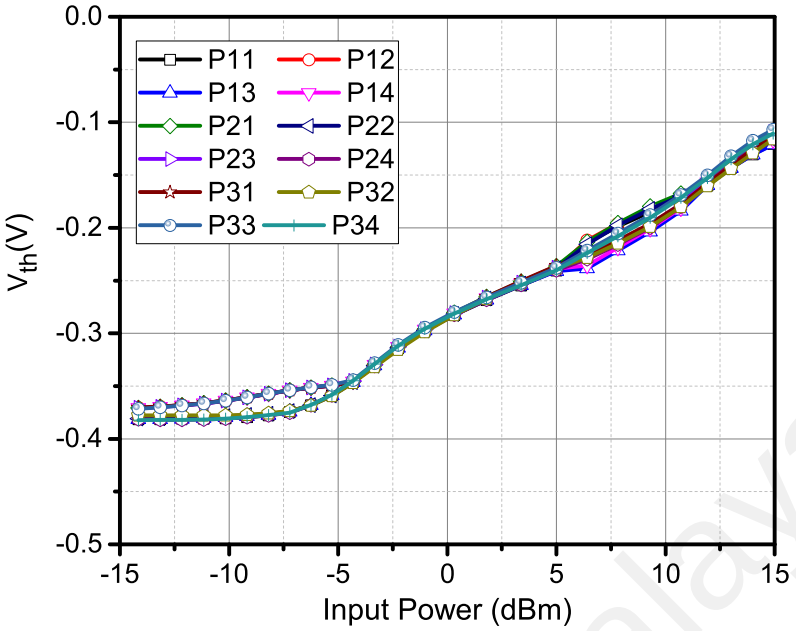

Figure 4.14: Threshold voltage of p-type transistors as a function of input power in the proposed symmetric LDCF rectifier under 100 kΩ load.

4.4.1 Parasitic capacitance

Since the scope of this work is confined for the operating frequencies between 953 MHz and 2 GHz, the size of transistors has been set through multiple iterations in the simulation so that C_{in} moderately affects the PCE at the operation frequency between 953 MHz and 2 GHz. Fig.4.15 depicts the simulation results of the input impedance ($|\ Z_{in}\ |$) for both LDCF and SB rectifier as a function of operating frequency while driving a 10 kΩ load at -6 dBm of input power. Input impedance of the rectifiers decreases with an increase of frequency till it reaches to the minimum point (between 1.5 and 1.75 GHz). The rectifiers encounter larger $|\ Z_{in}\ |$ with further increase in frequency due to the increase in input reactance. It is noteworthy that the $|\ Z_{in}\ |$ of the LDCF rectifier is relatively smaller than the SB rectifier.

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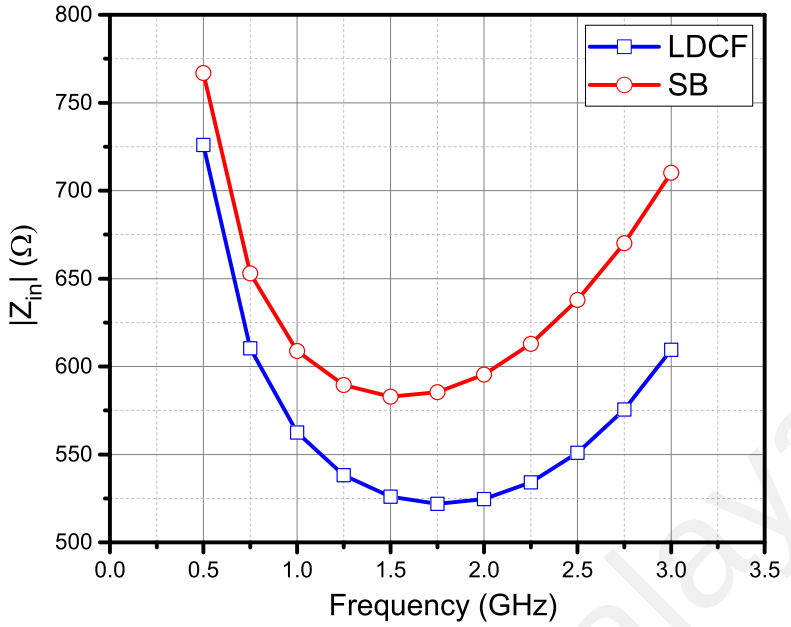

Figure 4.15: Simulated input impedance | Z_{in} | of the rectifiers as a function of frequency under a 10 kΩ load at -6 dBm.

4.5 Measurement results and discussions

To evaluate the performance of the SB and LDCF rectifiers, the PCE of rectifiers are required to be measured, which needs the measurement of the mixed-mode S-parameters of the rectifiers. Since a balun has been realized to drive the rectifiers with a differential RF signal, the balun as well needs to be characterized. The reflection coefficients' of the rectifiers at the selected frequencies have been obtained and listed in Table 4.2. The insertion loss of the balun is also listed for the selected frequencies in Table 4.3

Table 4.2: Transformed reflection coefficients of the SB and the LDCF rectifiers.

Frequency	SB		LCDF	
(MHz)	S_{dd11}	S_{cd11}	S_{dd11}	S_{cd11}
500	0.245-j0.759	0.247+j0.009	0.236-j0.768	0.221-j0.022
953	0.361+j0561	-0.188+0j231	0.375+j0.566	-0.146+j0.218
2000	-0.563+j0.151	-0.181-j0.354	-0.592+j0.171	-0.18-j0.291

The performance of the rectifiers using SB and LDCF self-body-biasing techniques are compared in the figures in Fig.4.16, Fig.4.18, and Fig.4.19 at different frequencies

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Table 4.3: Transformed insertion loss of balun

Frequency (MHz)	Balun S_{ds21}
500	0.327-j0.628
953	-0.368-j0.601
2000	-0.208+j0.653

under varied loads. At the frequency 953 MHz, which is one of the most prominent operating frequencies for passive RFID systems and other identification schemes, the LDCF outperforms the SB self-body-biasing technique in lower received power region in terms of the generated V_{DC}. Fig.4.16(a) shows the V_{DC} of each rectifier as a function of P_{rcv} under three different loads as 2 kΩ, 10 kΩ and 50 kΩ. Both rectifiers behave almost similar in response to the P_{rcv} variations. V_{DC} rises as the P_{rcv} increases at different slopes. Increasing the load resistance improves the V_{DC} since a larger load draws less charge from the C_S leading to the storage of more DC voltage. The rectifier adopting LDCF biasing technique shows a better performance in terms of V_{DC} compared to the rectifier with the conventional SB biasing technique.

The operation of the LDCF rectifier can be categorized into three regions. For instance, while the LDCF rectifier is driving a 50 kΩ load resistance, the rectifier operates with enhanced performance when the P_{rcv} is between -9 and -1 dBm [Enhanced region in Fig.4.16(a)]. In other words, in the enhanced region of operation, the LDCF rectifier generates a larger V_{DC} and the curve shifted to the lower P_{rcv} compared to the SB rectifier under the same load condition. As the P_{rcv} increases and enters to the region between -1 dBm and 5dBm [Intermediate region in Fig.4.16(a)], both rectifiers' V_{DC} are almost equal in terms of magnitude. Further increase in P_{rcv}, raises the V_{DC} for the SB rectifier while the V_{DC} of the LDCF rectifier becomes saturated after 5 dBm [Protected region in Fig.4.16(a)] and the V_{DC} does not exceed 3.5 V.

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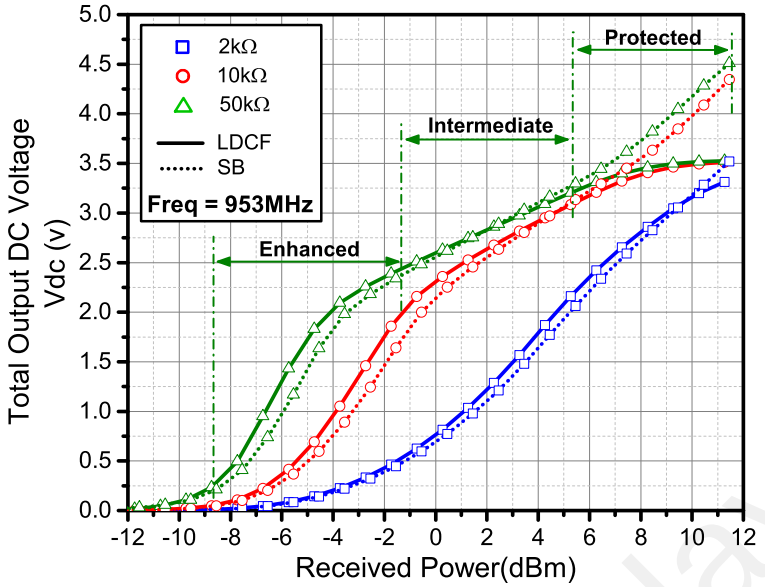
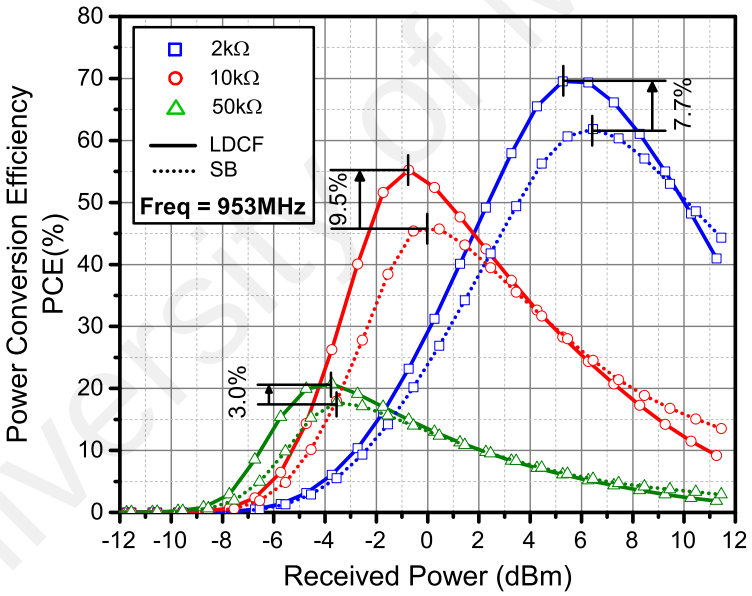


(a)



(b)

Figure 4.16: Measured performance of SB and LDCF rectifiers while they are driving different load resistances. a) V_{DC} and b) PCE as function of P_{rcv} at 953MHz.

To be more precise, the rectifier using LDCF technique improves the V_{DC} for smaller P_{rcv} since the V_{th} of p-type transistors in the structure has been mitigated by biasing the V_{sb} with a positive DC voltage in the enhanced region. The V_{sb} of p-type transistors increase as P_{rcv} increases, which causes the source-body PN junction starts to turn "on",

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and leads to source-body leakage current. In the intermediate region, the source-body leakage neutralizes the V_{th} mitigation and the LDCF rectifier performance becomes almost similar to the SB rectifier. In the protected region, V_{sb} of the p-type transistors in the LDCF rectifier reaches to 0.7 V (see Fig.4.12 for power > 5 dBm), which induces the PN junction between the source and the body of the p-type transistors completely turn "on" and shorts the input and output DC in both positive and negative rectifier cells with a voltage drop through the junction (see connections of the source and the body of P1-4 in Fig.3.7). Hence, the difference voltage between the DC_{in} and DC_{out} of each rectifier cell becomes almost equal to the voltage drop of the junction. Since the structure is in a double-rail three-stage configuration, each rail encounters three voltage drops with respect to the ground for each RF cycle. The LDCF rectifier in the protected region can be simplified with a model depicted in Fig.4.17 in which JPxn denotes the PN junction between the source and the body of p-type transistor x in stage n. As a result, V_{DC} in the protected region is almost equal to six voltage drops, which is theoretically expected to be 4.2 V. However, due to the undesirable parasitic effects, the voltage is limited at a lower level at the output of the LDCF rectifier. The turning "on" of the PN junction is a gradual process, which starts in the intermediate region and is completed in the protected region. From the behavior of the LDCF depicted in Fig.4.16(a), it can be concluded that the process of turning "on" is completed when the V_{DC} does not further increase with increase in P_{rcv}, which is at 3.5 V. This behavior can be accounted as an advantage since a voltage limiter is usually required in a far-field RFEH system to protect the succeeding circuitry when it is too close to the RF source. The V_{DC} in the FFNC RFEH systems hardly reaches up to 5.0 V with a small load (Ouda et al., 2013; Kotani et al., 2009; Hsieh et al., 2015). Such systems are usually supplied with a DC voltage around 1.2 V up to 1.8 V. An LDO voltage regulator is commonly used to stabilize the DC voltage fed by the rectifier, regulating towards the

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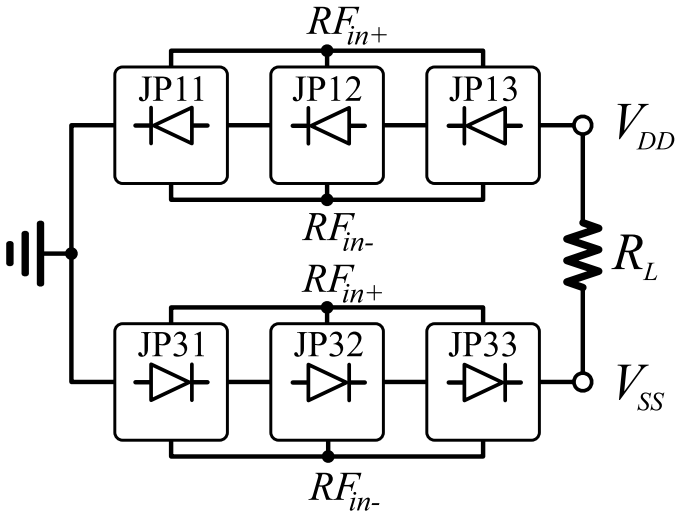
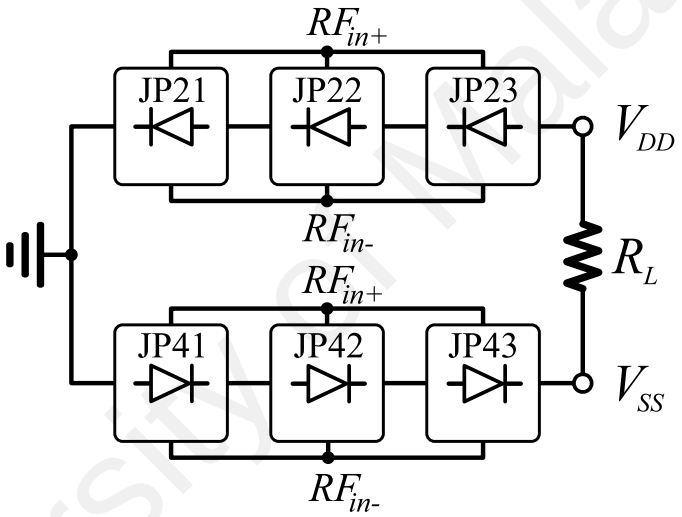


(a)



(b)

Figure 4.17: Simplified LDCF model in the protected region. a) positive RF cycle. b) negative RF cycle.

circuitry in the system. The level of 3.5 V is a sufficient DC voltage headroom, which allows the LDO to operate properly.

Fig.4.16(b) illustrates the PCE of both rectifiers as a function of received power under three different load resistances at the operating frequency of 953 MHz. The PCE increases with P_{rcv} until it reaches its peak and starts to drop with further increase in P_{rcv}. These fluctuations are caused by the leakage current of the transistors. According to the operation mechanism of the DDCCB rectifier, which has been explained in Sub-chapter

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2.5, for each RF cycle one n-type and one p-type transistors are "on", and the other two transistors are "off" in each rectifier cell regardless of being located in the positive or negative rail. For example, in the positive RF cycle and positive DDCCB rectifier cell, P_1 and N_2 are "on", which the drain-gate voltage of the "off" transistors (N_1, P_2) increases with larger P_{rcv} and forces the "off" transistors to turn "on". As a result, the current flows in the reverse direction and dissipates the power leading to less charge to be stored in the C_s. Similar behavior occurs to the negative DDCCB rectifier cell in which in the positive RF cycle P_3 and N_4 are "on" and P_4 and N_3 are "off". PCE increases for lower P_{rcv} region with an increase of load resistance while it degrades considerably at higher P_{rcv} region. The maximum PCE significantly decreases with larger load as well. The rectifiers under a larger load resistance generate a larger DC voltage, which again forces the "off" transistors (N_1, P_2 for the positive RF cycle and P_1 and N_2 for the negative RF cycle for the positive rectifier cell, and P_4 and N_3 in the positive, and P_3 and N_4 in the negative RF cycle for the negative rectifier cell) to turn "on" with higher P_{rcv}, which are supposed to be in "off" state while at lower P_{rcv}, less DC voltage is generated and the leakage current is suppressed. On the other hand, a smaller load resistance draws larger current at lower P_{rcv} while provides larger maximum PCE at higher P_{rcv} region compared to the larger load resistances.

As depicted in Fig.4.16(b), the rectifier with LDCF biasing technique operates with a superior PCE at lower P_{rcv} region and an inferior PCE at higher P_{rcv} region. In a typical rectifier (SB), the leakage current is mainly due to the source-to-drain leakage of n-type and p-type transistors, which are moderately suppressed by negatively biasing the n-type transistors' gate and positively biasing the transistors' p-type gate in the reverse bias condition for the DDCCB structure. However, another leakage affects the DDCCB rectifier using LDCF technique, which is associated with the PN-junction between the source and

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the body of the p-type transistors since the body of the transistors are independently biased. As P_{rcv} increases, the V_{th} of p-type transistors decreases, which also reduces the power loss and increases the PCE, compared to the SB rectifier, since the V_{th} reduction still does not cause the PN-junction to turn "on". Further increase in P_{rcv} causes excessive reduction in the V_{th} so that the p-type transistors become highly vulnerable to the reverse bias leakage, and the negative biasing of the gates will no longer be effective to suppress the reverse leakage current. In addition, the PN-junction between the source and the body of p-type transistors turns "on", and causes the current to leak even in the forward bias. Hence, the summation of the leakage in the forward and reverse bias becomes noticeable and the PCE considerably drops with steeper slope compared to the SB rectifier. This also explains the reasoning that why the rectifier behaves like a voltage limiter. The LDCF biasing technique improves the maximum PCE as well. The improvement of maximum PCE are 3.0%, 9.5% and 7.7% Under 2 kΩ, 10 kΩ and 50 kΩ load resistances, respectively compared to the rectifier with SB self-body-biasing technique. The maximum PCEs at this operating frequency for the LDCF rectifier are measured to be 69.5% at 5.26 dBm, 55.2% at -0.73 dBm and 20.7% at -3.73 dBm while driving a 2 kΩ, 10 kΩ and 50 kΩ respectively, which can be seen in Fig.4.16(b).

The LDCF rectifier performance at 2 GHz operating frequency is compared to the SB rectifier in Fig.4.18. The operation of LDCF rectifier at this frequency slightly differs as depicted in Fig.4.18(a). The output V_{DC} of the rectifiers rises almost equally as P_{rcv} increases while the LDCF rectifier still keeps its self-limiting characteristic and does not allow the V_{DC} to exceeds 3.5 V. At lower P_{rcv}, the SB rectifier operates with better PCE to some extent [see Fig.4.18(b)] but as P_{rcv} increases, the PCE of the LDCF rectifier becomes larger until it reaches to the maximum peak. Then, it starts to roll off with steeper slope leading to self-limiting at the output for higher P_{rcv}. The maximum PCE for the rectifier

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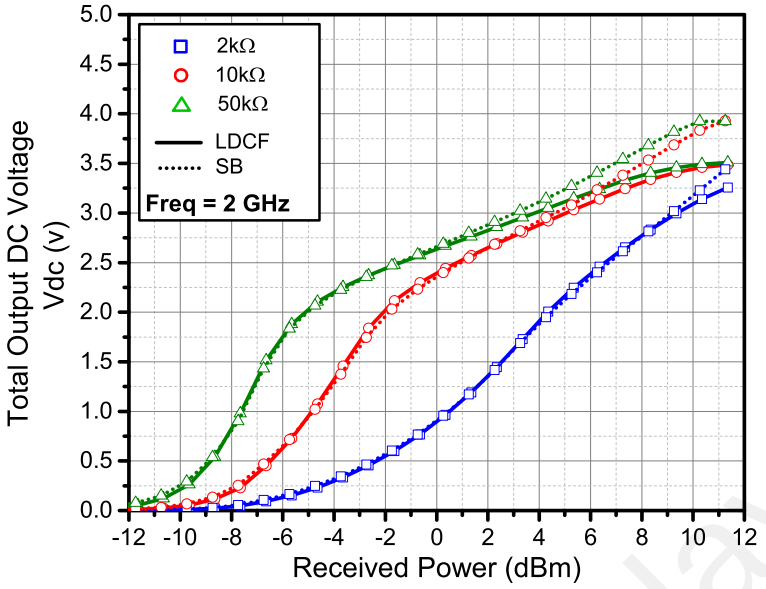
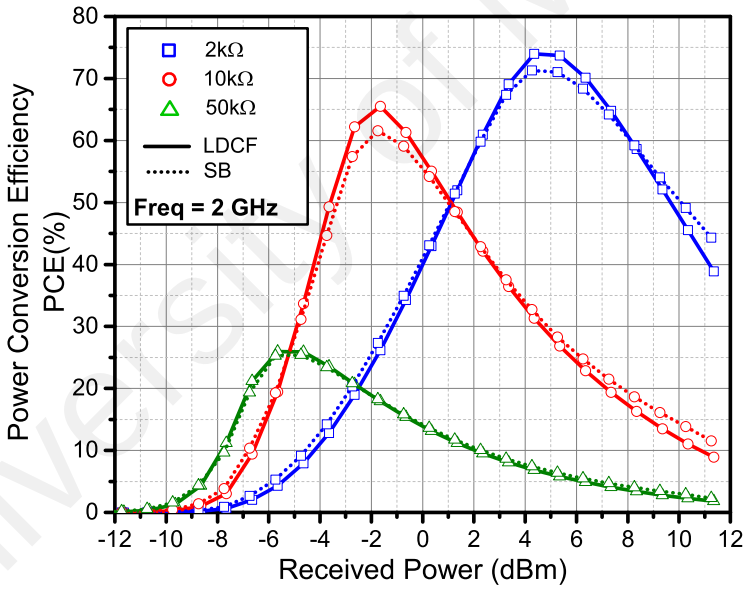


(a)



(b)

Figure 4.18: Measured performance of LDCF and SB rectifiers while they are driving different load resistances. a) V_{DC} and b) PCE as function of P_{rcv} at 2GHz.

using LDCF technique under 2 kΩ, 10 kΩ and 50 kΩ are 73.9% at 4.34 dBm, 65.5% at -1.65 dBm and 25.9% at -5.65 dBm respectively. Comparing the simulated and measured maximum PCE, the former is only higher by 17% at 953 MHz with R_L of 10 kΩ. Due to the structure of LDCF rectifier, a voltage difference between the source and the body

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of p-type transistors always exists causing considerable parasitic capacitance C_{sb}, which is suppressed in the SB rectifier as the source and the of p-type transistors are shorted. The effect of C_{sb} is negligible for lower frequencies but C_{sb} increases with an increase of frequency and causes the LDCF technique to become less effective in improving the PCE. This is the reason the LDCF rectifier is comparatively less effective at 2 GHz. However, the LDCF still exhibits higher maximum PCE compared to the SB rectifier.

The frequency response analysis for a DDCCB rectifier when the rectifier adopts the LDCF self-body biasing technique can be done for a specified condition. The performance of the rectifier strongly depends on the driving load and the operating frequency. One way to deliver a relatively an acceptable analysis is to select a specified load and analyze the rectifier in terms of the frequency response. The performance of the rectifiers has been analyzed with respect to the P_{rcv} at three different frequencies driving a 10 kΩ as a typical load. The measurement results are depicted in Fig.4.19.

The performance of both LDCF and SB rectifiers exhibits an improvement by raising the operating frequency from 500 MHz to 2 GHz. For the LDCF rectifier, the measured V_{DC} is slightly improved compared to the SB rectifier at smaller P_{rcv} region [see Fig.4.19(a)]. Fig.4.19(b) illustrates PCE of the rectifiers. As a perfect matching condition is assumed for the measurement,for the performance analysis it can be referred to the input impedance of the rectifiers for the selected frequencies, which is depicted in Fig.4.15 in which both rectifiers exhibit a fall and rise between 500 MHz and 3 GHz with a minimum point at approximately 1.75 GHz for the selected power and load. The input impedance is mainly under influence of the input reactance, which is predominated by the parasitic capacitances of the transistors in both rectifiers. Maximum PCE is observed at the frequency where the rectifiers' input impedance is minimum, which explains why increasing the frequency from 500 MHz to 2 GHz improves the PCE in Fig.4.19(b). However, a PCE

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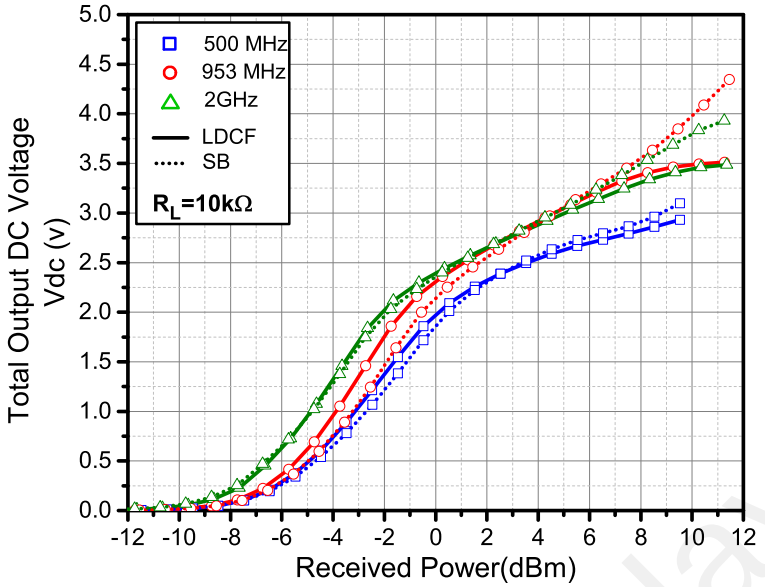
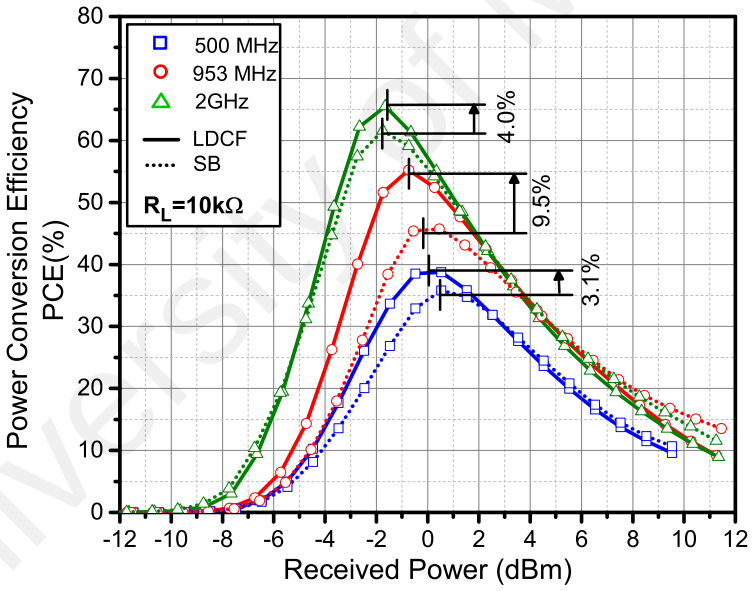


(a)



(b)

Figure 4.19: Measured performance of LDCF and SB rectifiers at different operating frequencies while driving a 10 kΩ load resistance. a) V_{DC} and b) PCE as function of P_{rcv}.

comparison indicates that the LDCF achieves the maximum improvement of 9.5% at 953 MHz, which was the preferred frequency for the optimization of design parameters in this work. In addition, the LDCF rectifier improves the PCE by 3.1% and 4% at 500 MHz and 2 GHz respectively.

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As a crucial measurement parameter in gauging the reliability of the fabricated samples, V_{DC} of 15 different samples of the fabricated LDCF rectifier was measured at two frequencies of 953 MHz and 2 GHz while driving a 10 kΩ load. The corresponding received power at 953 MHz and 2.0 GHz were calculated as 3.26 dBm and 3.34 dBm respectively. The results were fairly consistent as depicted in the Fig.4.20.

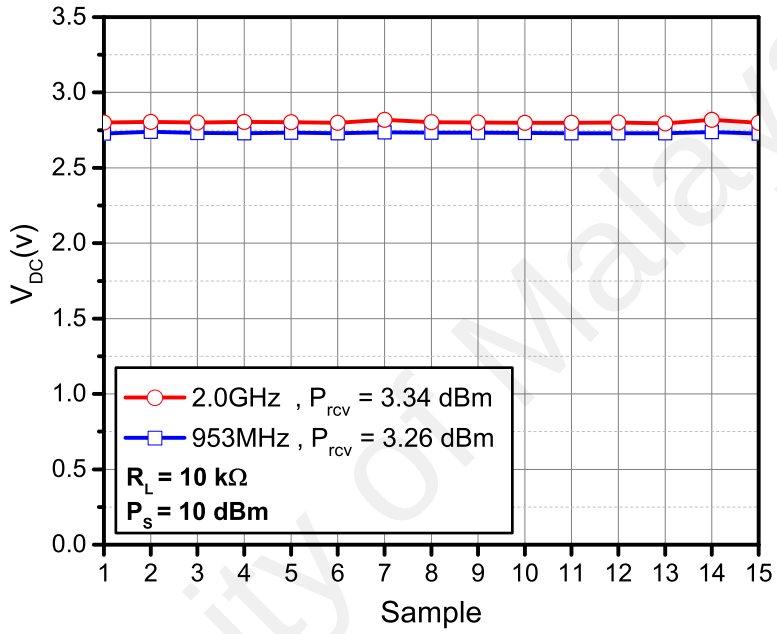

Figure 4.20: Measured output DC voltage V_{DC} of 15 different samples of LDCF rectifier.

The performance summary of the LDCF and SB rectifiers in this work is listed in Table 4.4 and compared with the state-of-the-art architectures (Hameed & Moez, 2015), (Hsieh et al., 2015) and (C. Y. Yao & Hsia, 2014). The LDCF rectifier in this work outperforms other works in terms of maximum efficiency while driving a heavy or smaller load with an inherent limitation capability, which none of the listed work offers. The simulated PCE reported in (Hsieh et al., 2015) is larger than measured PCE of the LDCF rectifier since in this work a double-rail three-stage rectifier is adopted in order to generate a symmetric DC voltage at the output. Hence, The LDCF rectifier faces more PCE degradation compared to single-rail single-stage architecture in (Hsieh et al., 2015). However, the maximum V_{DC}

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of the LDCF rectifier is comparatively larger.

Table 4.4: Performance summary and benchmark with the state-of-the-art work

	LDCF	SB	Hsieh et al.[1] (2015)	C. Y. Yao and Hsia (2014)	Hameed and Moez (2015)
Technology (nm)	**130**	130	180	180	130
Topology	**DDCCB**	DDCCB	DDCCB	Dickson-based	Dickson-based
Freq. (MHz)	**953**	953	900	433 & 925	902-928
Load (kΩ)	**2**	2	2	-	1000
Max PCE (%)	**69.5**	61.8	75	<50	32
Input (dBm)	**5.2**	6.4	-7	-15	-15
Max V_{DC} (V)	**3.5**	3.9	2.0	-	5.0
No. of stage	**6**	6	1	-	12
Self-Limiting	**Yes**	No	No	No	No
Symmetric	**Yes**	Yes	No	No	No

[1]The performance of the integrated rectifier is reported based on simulation results.

4.6 Summary

In this chapter, the procedures of implementing of the proposed self-body-biasing technique (LDCF) and its conventional counterpart (SB) have been thoroughly presented. In addition, the measurement procedures and setups have been explained in detail. The proposed and conventional techniques have been compared in terms of DC voltage at the output and efficiency. The proposed rectifier structure has been also compared with other state-of-the-art structures. In the next chapter, this thesis will be concluded with a suggestion for future work.

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CHAPTER 5: CONCLUSION

A novel symmetric CMOS rectifier was proposed in this research thesis based on differential-drive cross-coupled bridge (DDCCB) structure for far-field RF energy harvesting systems with the ability to self-limit the DC output voltage for the purpose of protection.

The structure of an RF energy harvester for far-field communication systems has been explained and discussed in which the rectifier plays a pivotal role in determining the performance of overall system in terms of communication distance. Basic concepts and a complementary literature review about rectifier design and its design parameters have been presented. According to the literature review, DDCCB structures have been recently proven considerably better performance in terms of efficiency compared to the Dickson-based structures.

An extra rectifier cell was proposed, which is referred to as negative rectifier to convert RF signals into a negative DC voltage at the output. A symmetric rectifier structure was proposed based on DDCCB circuit configuration by combining a positive and a negative rectifiers to convert the RF signal into a symmetric DC voltage. Conventionally, the source and the body of MOSFET transistors are connected to reduce the body effect, which is in this work referred to as SB technique. A new self-body-biasing scheme, which is referred to as LDCF, was proposed to bias the body of p-type MOSFET transistors in the rectifier structure. The LDCF technique allowed the p-type transistors in the proposed structure to operate with a dynamic threshold voltage depending on the received power at the rectifier input. Other self-body-biasing techniques were proposed to investigate other possible options for biasing the body of the transistors. However, none of which showed a considerable improvement in the performance of the DDCCB rectifier. Hence, they were not sent for the fabrication.

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The operating mechanism of the LDCF rectifier can be classified into 3 regions of operation. In enhanced region, the p-type MOSFET transistors operate normally and by moderately increasing the input power the biasing technique reduces the threshold voltage leading to an improvement in the PCE compared to the SB rectifier. By further increasing the power, the LDCF rectifier enters to the intermediate region in which the threshold voltage of the p-type transistors are extensively reduced and become considerably susceptible to the reverse leakage current. Hence, the leakage current neutralizes the threshold voltage reduction and the LDCF and SB rectifiers operate with an almost identical performance. Finally, in the protected region, due to the surplus power, the PN-junction between the source and the body of the p-type transistors in the LDCF rectifier turns "on", and causes the current to leaks through the body in the forward bias. Therefore, current leaks in both forward and reverse bias and induces each rectifier cell to behave as a diode. This capability allows the LDCF rectifier to self-limit its output voltage which is useful for far-field RF energy harvesting system for short distance communication to protect other circuitry blocks from being overpowered.

The proposed LDCF and the SB self-body-biasing techniques were implemented in a standard 130 nm CMOS technology. A comparison between the LDCF and the SB techniques was presented based on simulation and measurement results at the operation frequencies of 500 MHz, 953 MHz and 2 GHz along with a corresponding load of 2 kΩ, 10 kΩ and 50 kΩ. According to the simulation and the measurement results, the LDCF rectifier outperformed the SB body biasing technique, which verified the proposed rectifier structure and the body biasing technique. A 9.5% of maximum improvement is achieved at the peak PCE when the LDCF rectifier is operating at 953 MHz, and driving a 10 kΩ load. A peak PCE of 73.9% was achieved at 2 GHz when driving a 2 kΩ load. The LDCF technique also offers a self-limiting capability for its output voltage by reducing the PCE

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at larger received power. A limit-voltage level of 3.5 V was measured irrespective to the operating frequency and load.

5.1 Future work

In this research, the proposed LDCF self-body biasing was aimed for the p-type transistors in the rectifier structure. However, the standard DDCCB rectifier also includes n-type transistors. Another technique can be proposed to bias the body of both n-type and p-type transistors for the DDCCB rectifier structure. It should be noted that biasing the body of n-type MOSFET transistors requires triple-well CMOS process. Hence, another self-body-biasing technique can be implemented to regulate the V_{sb} and mitigate the threshold voltage of the n-type MOSFET transistors in a symmetric multi-stage DDCCB rectifier as well. To be more precise, the body of n-type MOSFET transistors should be connected to the output DC (DC_{out}) in the positive rectifier rail and to the input DC (DC_{in}) in the negative rectifier rail, which is referred to as symmetric DC feeding (SDCF) technique, which the structure is depicted in Fig.5.1. In SDCF technique, both p-type and n-type transistors' body is self-biased. Therefore, all transistors operate with a scalable V_{th} since the V_{sb} is no longer 0.

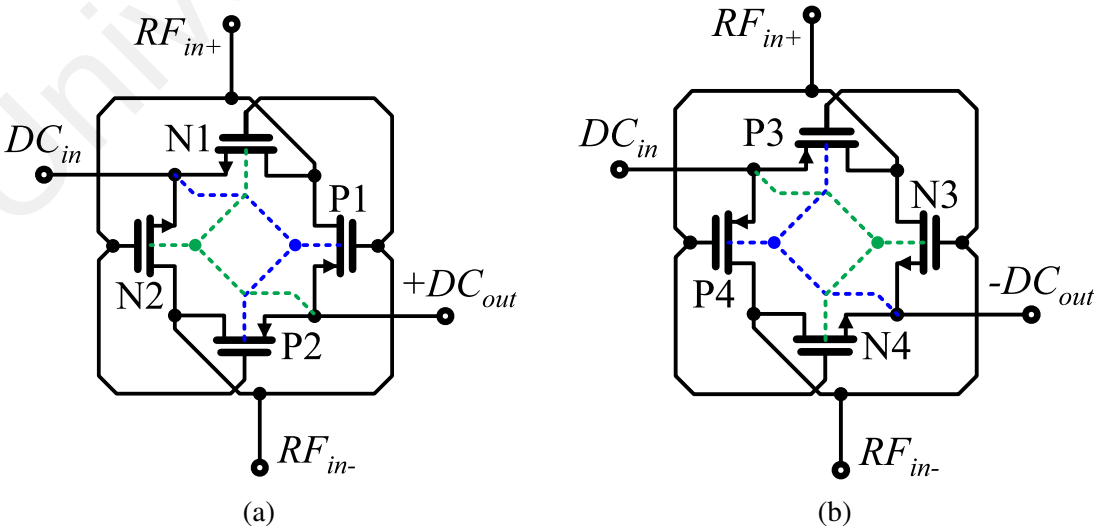

Figure 5.1: Circuit configuration of proposed SDCF body biasing technique for DDCCB rectifier. a) positive b) negative rectifier.

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The SDCF self-body-biasing technique requires more investigation and study in order to confirm its effectiveness for the DDCCB rectifier. It should be noted that triple-well or DNW fabrication process is required in order to implement the SDCF technique for the DDCCB rectifier.

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