DESIGN OF COMPLEMENTARY CLASS-C OSCILLATOR WITH TAIL CURRENT SOURCE FEEDBACK AND NOISE SUPPRESSION FOR WIRELESS APPLICATIONS

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KUALA LUMPUR

2019

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DISSERTATION SUBMITTED IN FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF MASTER OF ENGINEERING SCIENCE

FACULTY OF ENGINEERING
UNIVERSITY OF MALAYA
KUALA LUMPUR

2019

UNIVERSITY OF MALAYA

ORIGINAL LITERARY WORK DECLARATION

Name of Candidate: PRAVINAH NAIR A/P SHASIDHARAN

Matric No: KGA160013

Name of Degree: Master of Engineering Science

Title of Dissertation: DESIGN OF COMPLEMENTARY CLASS-C OSCILLATOR WITH TAIL CURRENT SOURCE FEEDBACK AND NOISE SUPPRESSION FOR WIRELESS APPLICATIONS

Field of Study: ELECTRONIC

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DESIGN OF COMPLEMENTARY CLASS-C OSCILLATOR WITH TAIL CURRENT SOURCE FEEDBACK AND NOISE SUPPRESSION FOR WIRELESS APPLICATIONS

ABSTRACT

The performance of low-powered transceivers are required to meet stringent specifications for an advanced wireless radio application. It is critical for a voltage-controlled oscillator (VCO) to meet multi-standard and multiband operation with low-power consumption and sufficient gain. This paper propose a novel technique for wide tuning range performance in a complementary class-C VCO employing a capacitive-source degeneration (CSD) to meet multi-standard operation for low-power transceivers. The technique which employs two sets of symmetrical split PMOS biased current source operating in subthreshold region achieves the desired low phase noise (PN) performance of below -120 dB/Hz at a tuning range of 2.2-to-2.9 GHz with a supply headroom of 1.2 V. The control of the dc bias point reduces the conduction angle which improves the current efficiency, power consumption and PN. Concurrently, an auxiliary $-g_m$ NMOS only class-B oscillator is incorporated to mitigate the start-up issue of the class-C VCO. At the center frequency of 2.45 GHz, the proposed VCO consumes a power of 1.73 mW, achieves a phase noise of -120 dBc/Hz at 1 MHz offset, and a figure - of - merit (FoM) of 185.41 dBc/Hz at 1 MHz. The total active chip area is only of 0.3-mm^2 excluding bond pads. The proposed VCO serves as a promising solution for low-power wireless communication systems.

Keywords : Class-C VCO, Capacitive Source Degeneration,(CSD) CMOS , gate bias, phase noise, (PN), startup

REKA BENTUK KELAS – C VCO PELENGKAP DENGAN PUNCA ARUS SUMBER SUAP BALIK DAN PENINDASAN HINGAR UNTUK RANGKAIAN WAYARLES

ABSTRAK

Prestasi transceiver berkuasa rendah diperlukan untuk memenuhi spesifikasi yang ketat untuk aplikasi radio wayarles yang lebih maju. Ia adalah penting untuk pengayun kawalan voltan (VCO) untuk memenuhi operasi frekuensi dalam pelbagai piawaian dan mengaplikasi penggunaan kuasa rendah dan gandaan yang mencukupi. Kajian ini membentangkan keluasan penalaan julat VCO-kelas-C pelengkap yang menggunakan teknik berkemuatan punca kemerosotan (CSD) dengan dua punca arus PMOS bersimetri dalam kealiran subambang untuk megurangkan tahap hingar yang lebih rendah. Teknik ini mengawal tahap pincang DC supaya dapat mengurangkan sudut pengaliran sekaligus meningkatkan kecekapan arus, dan menindaskan peningkatan hingar kerlipan. Pada masa yang sama, masalah permulaan dapat dikurangkan dengan menggabungkan gadingan silang kelas-B tambahan yang bersifat NMOS -g_m selari dengan kelas-C-VCO pelengkap yang direka dalam teknologi CMOS 180nm yang mempamerkan rangkaian keluasan penalaan sebanyak 2.2-2.9 GHz. Beroperasi di frekuensi tengah 2.45 GHz, penggunaan kuasa rendah ialah 1.73 mW. Tahap hingar yang dicapai adalah lebih rendah daripada -120 dBc / Hz pada 1MHz ofset manakala FoM sebanyak 185.41 dBc / Hz @ 1MHz ofset. Kawasan plat cip aktif ialah 0.3 mm^2. VCO yang dicadangkan berfungsi sebagai penyelesaian yang merangsangkan untuk sistem komunikasi wayarles berkuasa rendah.

Kata Kunci:Kelas-C VCO, berkemuatan punca kemerosotan, CMOS, pincang get, tahap hingar, (PN), permulaan

ACKNOWLEDGEMENTS

The journey of my entire research is very challenging and as said in the quote by Steve Jobs “The only way to do great work is to love what you do, if not do not settle”. I believe this quote is aptly describes the journey, like any journey as it had its ups and downs. I would like to have this opportunity to appreciate and express my very deepest gratitude to all of them.

First, I am grateful to my supervisors or more I can say my guider, friend and mentors, Dr Harikrishnan Ramiah and Dr Jagadheswaran Rajendran for giving me an opportunity to work together in their group. They are a perfect dynamic duo in many ways and perception. Dr Harikrishnan is very meticulous about all intricate details which I have learned a lot about the technical writing, organizing thoughts and conveying the ideas from never ending discussion I had with him. From his high expectation, which makes his students to perform the highest level of performance with meaningful results and deliver the best we could. Dr Jagadheswaran is a very enthusiastic person and whom very much eager on the engineering research and without his endless technical guidance and support, I would be unaware of the importance in this aspect of research. Both, taught me on the objective thinking and focusing on the basics which I am truly indebted to for all their opinions and teachings on numerous occasions and also on the chip measurement process.

Next, I would like to thank the Talent Corporation Malaysia for providing stipend every month which is very much helpful. This work would not have been possible without their financial support. I would also thank to the all experts from Silterra Malaysia Sdn Bhd and Intel for their sharing experiences and fabrication knowledge plus strategies which ease our entire project workflow.

Together in this journey, sailing in the same boat my University Science Malaysia, (USM) closed friend, Premmilaah and other University Malaya, (UM) research

members which I appreciated their continuous motivation, advises and assistance which have pushed me this far. In no particular order of preference I would like to mention another friends: Gabriel Chong, Ashwinder and Malarvathy, whom always encourage and help me a lot in my tough times. I would never forget them and truly grateful, without their help all this is not possible.

Finally, I want to thank my siblings and my parents especially my late father, Mr Shasidharan for everything he had been provided for me. I truly adore him as he behaves more like a friend, pouring so much care and meant a lot to me. Not forgetting my Mom, her endless love and nurturing helped me a lot in completing my project and she always encourages me to remain positive all the time. Last but not least, to God with His non-ending blessings and gracefulness which make me to never lose hope and constantly making impossible things to everything possible.

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LIST OF SYMBOLS AND ABBREVIATIONS

ABB	:	Active building blocks
AGC	:	Automatic gain control
AM	:	Amplitude Modulation
AM	:	Analog multipliers
BC	:	Barkhausen criterion
BPFTO	:	Band-pass filter-tuned oscillator
BDI	:	Bilinear discrete integrator
CCO	:	Current-controlled oscillator
CCMM	:	Current-controlled monostable multivibrator
CCPP	:	Current-controlled pulse generator
CM	:	Common mode triangular wave generator
CMO	:	Current-mode Oscillator
CMOS	:	Complementary Metal-Oxide -Semiconductor
COA	:	Current operational amplifier
CSD	:	Capacitive Source Degeneration
CS	:	Capacitor-switching
dB	:	Decibel
dBm	:	Decibel with respect to 1mW
DC	:	Direct Current
DC	:	DC bias current
DCO	:	Digital controlled oscillator
DISO	:	Differential -input single-output
DM	:	Differential mode
DVCCS	:	Differential voltage complimentary current

DSV	:	Drain Source Voltage
DUT	:	Device Under Test
ESD	:	Electrostatic Discharge
ECO	:	Electronically-controlled current-mode
ECO	:	Explicit current output
ENF	:	Excess Noise factor
F	:	Noise Factor
FM	:	Frequency Modulation
FLL	:	Frequency Locked Loop
FOSO	:	Fractional-order sinusoidal oscillators
FUSO	:	Fully uncoupled sinusoidal oscillators
FCR	:	Frequency-controlling resistor
FT	:	Fourier Transform
FRC	:	Free running oscillator
FSE	:	Fourier series expansion
FSE	:	Frequency selective element
FS	:	Frequency synthesizer
GBP	:	Gain bandwidth product
GCs	:	Grounded-capacitor
GFSK	:	Gaussian Phase Shift Keying
GND	:	Ground
GSGSG	:	Ground-Signal-Ground-Signal-Ground
GSO	:	Gate-source overdrive
Hz	:	Hertz
HB	:	Harmonic balance
HO	:	Harmonic oscillator

ICs	:	Integrated Circuits
ICFG	:	Integrated circuit function generators
IM	:	Intermodulation
IoE	:	Internet of Everything
IoT	:	Internet of Things
IR	:	Impulse response
ISF	:	Impulse sensitivity function
ISM	:	Industrial, Scientific, and Medical
JA	:	Jitter accumulation
JP	:	Jitter peaking
KCL	:	Kirchhoff's Current Law
KVL	:	Kirchhoff's voltage Law
LM	:	Leeson model
LO	:	Local Oscillator
LSB	:	Lower Side Band
LTI	:	Linear time-invariant
LTV	:	Linear time variant
MIM	:	Metal-Insulated-Metal
MOS	:	Metal Oxide Semiconductor
MSOs	:	Multiphase sinusoidal oscillator
NIC	:	Negative -impedance converter
NMOS	:	N-channel Metal-Oxide Semiconductor transistor
NMF	:	Noise modulating function
NSSG	:	Non-sinusoidal signal generator
NSWG	:	Non-sinusoidal waveform generator
PCB	:	Printed Circuit Board

PLL	:	Phase Locked Loop
PN	:	Phase Noise
PM	:	Phase Modulation
PMOS	:	P-channel Metal-Oxide Semiconductor transistor
PVT	:	Process, Voltage and Temperature
Q	:	Quality Factor
RF	:	Radio Frequency
RLC	:	Resistor-Inductor -Capacitor
RFIC	:	Radio Frequency Integrated Circuit
RMS	:	Root Mean Square
SA	:	Spectrum Analyzer
SAW	:	Surface Acoustic Wave
SDC	:	Single-to-Differential Circuit
SDR	:	Software Defined Radio
S_i	:	Silicon
SiGe	:	Silicon-Germanium
(S_iO_2)	:	Silicon Oxide
SSA	:	Signal Source Analyzer
SoC	:	System on Chip
USB	:	Upper Side Band
UWB	:	Ultra-Wideband
VCO	:	Voltage Controlled Oscillator
VGA	:	Variable-Gain Amplifier
VNA	:	Vector Network Analyzer
WiMAX	:	Worldwide Interoperability for Microwave Access
WLAN	:	Wireless Local Area Network

WPAN	:	Wireless Private Area Network
WUC	:	Wake-Up Circuit
$1/f$	:	Flicker Noise
$1/f^2$	:	Flicker noise in 20 dB in phase noise region
$1/f^3$	:	Flicker noise in 30 dB in phase noise region
C_{gs}	:	Gate-to-Source Parasitic Capacitance
C_{gd}	:	Gate –to-drain Parasitic Capacitance
C_{var}	:	Varactor capacitance
C_{OX}	:	Gate Oxide Capacitance
f	:	Frequency in Hz
f_T	:	Transit Frequency
g_m		Transconductance
L	:	Length of Transistor
V_{th}	:	Threshold Voltage of Transistor
W	:	Width of Transistor
ω	:	Frequency in rad/s
ω_C	:	Centre Frequency in rad/s

LIST OF APPENDICES

CHAPTER 1: INTRODUCTION

1.1 Thesis Motivation

The ever-increasing growth of the wireless communications, provoke eager research activity to continuously provide a solution for system optimization while providing optimal design trade-offs to acquire the best wireless operation. Since, radio frequency, RF defines the backbone of wireless communications especially in the transceivers system, frequency conversion mechanism relies heavily on the spectral purity of RF local oscillators (LOs), in accommodating an output with less distortion in the transceiver system under the licensed or unlicensed channel users across the frequency spectrum (P. N. Shasidharan, Ramiah, & Rajendran, 2018). In pass decades and years to come, there has been a tremendous demand in the silicon design environment which reflects a powerful communication and computational capabilities into mobile form factors. Today, wireless mobile systems has been made possible by technological advances in the field of integrated circuits (ICs) in Silicon Germanium (SiGe) and Gallium Arsenide (GaAs) allowing a high level of integration at low cost and low power dissipation and yet Silicon devices are still fueling the most innovative industrial applications and products of the future due to its low cost and versatility. Global mobility and worldwide communications between end user consumers and the devices becomes more complex, forming an Internet of Everything (IoE) community. This creates an unlimited opportunities to fundamentally improve quality of life while creating explosive growth in knowledge and wealth which is motivated in the realization of multi-mode, multi-band and multi-standard wireless communication system and application standards (Martins et al., 2019) dictating such high spectral purity given as,

- Wireless communication standards (including cellular, WLAN, WPAN, broadcast, positioning, etc.,) require a local oscillator which is capable of ultra – wide frequency tuning range (FTR) with sufficiently high spectrum purity to support diverse specification.
- Internet of Everything, (IoE) standards which incorporates ultra-portable health–care wearable devices for ultra-low power solutions.

Table 1.1 shows the defined communication standards' band and the targeted phase noise requirements in compliance to the cellular bands.

Table 1.1 Communication standards requirements

Standard	Frequency band (GHZ)	Required phase noise (dBc/Hz)
Bluetooth	2.402-2.480	-84 @ 1 MHz -114 @ 2 MHz -129 @ 3 MHz
GSM 900/1800	0.880-0.960 1.710-1.880	-122 @ 0.6 MHz -132 @ 1.6 MHz -139 @ 3 MHz
UMTS	1.920-2.170 1.900-2.025	-132 @ 3 MHz -132 @ 10 MHz -144 @ 15 MHz
WiFi	2.412-2.472 5.150-5.350 5.470-5.825	-102 @ 1 MHz -125 @ 25 MHz

(Shahmohammadi, Babaie, & Staszewski, 2016a)

In the expansion of mobile network capacity, the demand for a high mobile data rate is increasing massively. Current industries are looking towards the utilization in broad spectrum of wide range of bands instead of existing fashioned spectrum that has become scare lately. The RF PLL system need a significant amount of power to solve the tradeoff

between the phase noise and spurious requirement (Siriburanon et al., 2016). Compared to the Analog PLLs, an All-Digital Phase Locked Loop, (ADPLL) is more advantageous in nm -CMOS technologies. This explains the clarity and accuracy of the signal required for wireless standard. The Voltage Controlled Oscillator, (VCO) is integrated in a frequency or phase –locked loop configuration to obtain a precise and better output frequency, as shown in Figure 1.1. This FLL/PLL (Babaie et al., 2016) shown as a feedback loop consisting of an off chip, frequency reference quarts crystal that carries low frequency in kHz to MHz range function as a precision frequency source. The VCO output frequency tracks the frequency reference due to the feedback control mechanism.

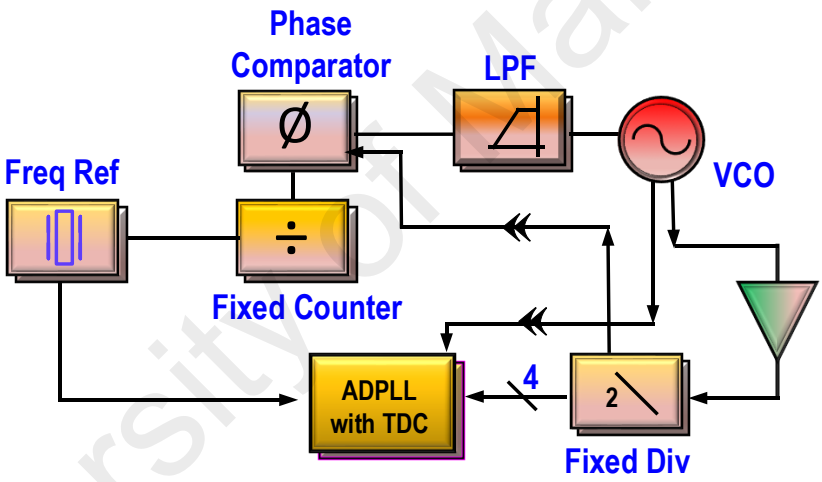

Figure 1.1 A phase or frequency locked loop architecture using a voltage controlled oscillator.

The different output frequencies are attainable through the division ratio set by the frequency divider producing different frequency channels. In this clock system, the wireless sensor node transmitting and receiving process is dependent on the oscillator output stability. In addition, the frequency reference startup time and LC VCO can dominates the idle power consumption in this loop system and so as the power consumption of the sensor node. It is difficult to ensure startup at a low voltage headroom due to the limited high bias voltage. However this outlays a research question deemed to

be necessary and motivates the researches to analyse the startup time under low power wireless application design.

A major challenge in the wireless industry is to achieve a low die area consumption in the high-level integration of functional blocks using low-process node technology of 180nm CMOS platform. Another challenge in the RF oscillator design is to achieve a wide tuning range while gaining a low phase noise performance. The implementation of switched capacitor array,(SCA) in (Sánchez-Azqueta, Aguirre, Gimeno, Aldea, & Celma, 2016) aids for wide tuning range for the VCO but the downside of it as it degrades the quality factor, Q due to the switching losses from the capacitor array. Among the efforts for the single-chip radio integration, is in the implementation of a low phase-noise, low power and small die area voltage-controlled oscillator (VCO) which determines the service quality in the information transfer function. As CMOS downscaling favors towards high level integration under minimum area consumption, the corner frequency (<100kHz) will increase, embarking an additional challenges in the implementation of Complementary VCO to achieve low power at high tuning range steadily across the frequency bandwidth. Moreover, the integration of a high Quality Factor, Q tank is not easy due to high losses in the silicon substrate affected from the transit frequency, f_T, thereby influence the phase-noise performance (Yi, Yu, Mak, Yin, & Martins, 2018a) . Designing a VCO with wide tuning range under the constraint of low power budget has become a research hotspot in VCO generation. A single on-chip wideband oscillator with minimum power consumption and low phase noise needed to be achieved to meet a desired target in an overall transceiver system as shown in Figure 1.2.

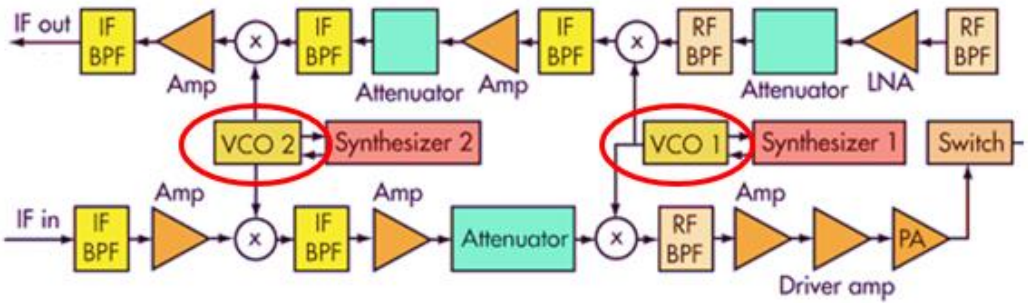

Figure 1.2 Overall RF Transceiver architecture.

The entire transceiver system (Rout, Acharya, & Sethi, 2018) improvisation is achievable by meeting the VCO specification in the frequency translation system. Therefore it is important for VCO to work under:

i. Less than miliwatt range of power consumption, for less battery power and energy constrain to achieve a longer battery life span through usage of a coined sized cell battery.
ii. Delivering high area efficiency of less than $1mm^2$ single on chip solution for transceiver system.
iii. Characterizing a standalone chipset IP to be integrated in Internet of Everything, (IoE) system.

1.2 Problem Statement

The current exponential growth in wireless communication has surpassed the demand for more available channels in mobile communication application. This has imposed stringent requirements on the performance of the VCO especially on its phase noise in which it degrades as the number of channels and frequency bandwidth increases. The phase noise improvisation depends on the Q factor enhancement. Integrating a highly Q resonant tank demands for more die area and it is an uphill task to ensure a high Q linear

operation across the wide bandwidth. Besides, battery-powered devices are in high development, and it is crucial for a system to drain low power for longevity and sustainability especially to suit into Internet of Everything, (IoE) transceiver solution. In addition, achieving a wide tuning range while maintaining better phase noise performance seems to be a bottleneck in the current trend of VCO oscillators (Xiaosong, Shuilong, Pufeng, & Haiying, 2010). RF researches face several limitations in improvising the sensitivity of oscillators towards achieving higher gain, fast startup (millisecond range) and persistently maintaining optimum current efficiency of less than 0.4π via reduction of the conduction angle.

1.3 Thesis Objectives

The first objective of the proposed work is to design a wide tuning range complementary Class–C VCO under low die area for 2.2 to 2.9 GHz wireless application.

The second objective is to attain a low phase noise under low power consumption and sufficient gain under 1.2 V voltage headroom achieving a comparable Figure of Merit (FoM).

The third objective to analyze and benchmark the reported state of the art hybrid VCO architectures and to develop a test bench for a low phase noise and with wideband VCO verification.

1.4 Thesis Outline

Chapter 2 illustrates the literature review which expounds on the current reported works on VCO oscillators implemented in silicon platform review in line to phase noise improvement with additional advantages of startup improvisation, robustivity and high power efficiency, large swing amplitude, *1/f* flicker noise up-conversion reduction, low power consumption and with wide tuning range techniques. Chapter 3 elaborates on the methodology of the proposed architecture which includes the quantitative analysis and description. Mathematical derivation and performance schematic based simulation with presented post-layout output results. This is followed by the measurement results and test bench set up in Chapter 4. Finally, Chapter 5 draws the conclusion and future works.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

Most RF transmitter or receivers (a.k.a Transceiver) requires a low phase noise oscillators for clean frequency generations. The challenging task is to achieve a reliable performance when supply voltage reduces for a low cost 180 nm CMOS technology and the performances of the oscillators are based on the transit frequency, f_T it possesses. Since oscillator performances are very important, this chapter elaborates the reported state of the art research works on the grounds to improve the crucial performances favoring towards better startup, *1/f* flicker noise up-conversion reduction, high swing oscillation with adequate gains and wide tuning range techniques implemented and the physical drawbacks encountered in the construction of the architecture.

2.2 Phase Noise of Electrical Oscillators based on LTV model

In this chapter, the linear time variant (LTV) system approximate to be the nearest approach in evaluating the phase noise. Impulse sensitivity function (ISF) is the expression accounted in evaluating the phase noise, (PN) based on the LTV system. The parameters defined the computation of the ISF explains the output's higher order harmonics on the phase and amplitude noise perturbation relationship along with the superposition method of the excess phase. These expressions are taken into consideration towards the LTV improvisation. A cosine based transfer function is entailed to model this excess phase at the output signal, resulting in an output PN. In this LTV model, flicker noise, *1/f* denoted as a white noise floor which is sub-divided by the corner frequency of the flicker noise response of the device and the corresponding phase noise which are

derived and considered reliable for the offset frequencies which appear to be lower than the corner frequency in the phase noise plot.

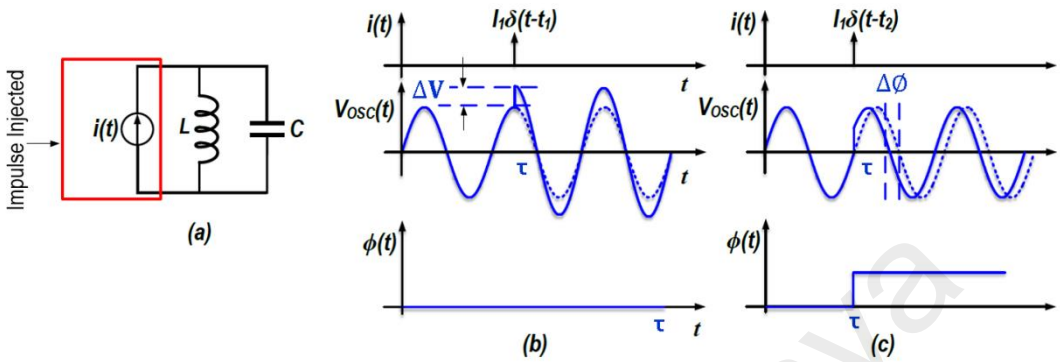

Figure 2.1: a) Current impulse perturbation on an ideal LC tank (b) amplitude shift response (c) phase shift response on the impulse injected into the resonator tank.

When the small injection of current impulse, i(t) into the oscillators output node at an arbitrary time,τ the resultant output phase shift , $\Delta\emptyset$ and amplitude shift, ΔV expressed as (Hajimiri & Lee, 2013);

$$\Delta\emptyset = \Gamma(\omega_o\tau)\frac{\Delta V}{V_o} = \Gamma(\omega_o\tau)\frac{\Delta q}{q_{max}} \tag{2.1}$$

where $\Delta q = \Delta V \cdot C$ is the effective charge introduced into the tank and C is the tank capacitance, $q_{max} = V_o C$ which is the maximum charge displacement at the equivalent capacitor, and $\Gamma(\omega_o\tau)$ being periodic and is a dimensionless time varying ISF parameter. This is sensitivity test case of an output phase deviation to the small charge introduced. Figure 2.1 shows when the current impulse injected, the oscillation amplitude will be appear at maximum whereas the phase is not disrupted. Apart from that, when the current impulse appear at the zero crossings, the phase shift is more significant that the amplitude shift. Amplitude shift usually considered negligible. The phase shift, $\Delta\emptyset$ is directly proportional to the amount of charge, Δq which is injected into the oscillator node. The

parameter of $\Gamma(\omega_o\tau)$ been normalized to q_{max} and are made to be independent to the output amplitudes. The resultant phase shift are sum of the excess phase and is expressed as;

$$\emptyset\,(t) = \int_{-\infty}^{t} i(\tau)\frac{\Gamma(\omega_o\tau)}{q_{max}}\;d\tau \tag{2.2}$$

Since ISF is a periodic function, the Fourier series has been expanded and expressed as $\Gamma(\omega_o\tau) = c_0 + \sum_{n=1}^{\infty} c_n \cos(n\omega_o\tau + \theta_n)$. The phase, θ_n is not significant for a random input noise and considered negligible. Therefore simplified as;

$$\emptyset\,(t) = \frac{1}{q_{max}}\left[c_0\int_{-\infty}^{t} i(\tau)\;d\tau\; + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau)\cos(\,n\omega_o\tau\,)d\tau \quad\right] \tag{2.3}$$

The low – frequency current noise, $i(t) = I_0\cos(\Delta\omega t)$ such that $\Delta\omega \ll \omega_0$ is injected to the oscillator node, and by replacing $i(t)$ in equation (2.3), the integrals at higher frequency than $\Delta\omega$ are attenuated via averaging of the integration, subsequently excluding the first integral which include c_0, and the dc value of an ISF function. This shows crucial significant term, $\emptyset\,(t)$ as;

$$\emptyset\,(t) = \frac{I_0 c_0}{q_{max}}\int_{-\infty}^{t}\cos(\Delta\omega\tau)d\tau = \frac{I_0 c_0\sin(\Delta\omega t)}{q_{max}\Delta\omega} \tag{2.4}$$

Therefore the resulted impulse at $\pm\Delta\omega$ in the Power Spectral Density, (PSD) of $\emptyset\,(t)$ are denoted by $S_{\emptyset}(\omega)$.Thefore, the current noise, $i(t) = I_n\cos(n\omega_0 + \Delta\omega)t$ close to the frequency will result in two sided band in $S_{\emptyset}(\omega)$. If the bandwidth of frequency, $\Delta\omega$ for flicker noise lower than ω_o and ω_{1/f^3}, the noises effect are considered by the dc value of the ISF and produced an excess phase in the output phase spectrum. Therefore, the phase noise in frequency radian expressed as;

$$L_W(\Delta\omega) = \left(\frac{\Gamma_{RMS}^2 \overline{\iota_{n,w}^2}/_{\Delta f}}{2q_{max}^2 \Delta\omega^2} \right) \quad (2.5)$$

where Γ_{RMS}^2 is the root mean square (RMS) value of the ISF and $\overline{\iota_{n,w}^2}/_{\Delta f}$ is the Power Spectral Density, (PSD) of the white noise. The -3 dB corner frequency in the phase noise margin expressed for frequency of $\Delta\omega \ll \omega_{0-3\,dB.}$ as;

$$\omega_{0-3\,dB} = \frac{\Gamma_{RMS}^2 \overline{\iota_{n,w}^2}/_{\Delta f}}{4q_{max}^2 \Delta\omega^2} \quad (2.6)$$

Considering $\overline{\iota_{n,1/f}^2} = \overline{\iota_{n,w}^2}\ {}^{\omega_{1/f}}/_{\Delta\omega}$, $\Delta\omega < \omega_{1/f}$,where the $\omega_{1/f}$ represent the flicker noise's corner frequency and the resultant of the phase noise can be derived as;

$$L_{1/f}(\Delta\omega) = 10\log\left(\frac{c_0^2 \left(\overline{\iota_{n,w}^2}/_{\Delta f} \right) \omega_{\frac{1}{f}}}{2q_{max}^2 \Delta\omega^3} \right) \quad (2.7)$$

The equation derived is valid for range of $\omega_{0-3\,dB.} < \Delta\omega < \omega_{1/f}$. An LC tank based oscillator are mainly adopted due to its inherent low phase noise. The thermal noise to phase noise up-conversion (20dB/dec region) is expressed as;

$$L(\Delta\omega) = 10\log\left(\frac{R_t kTF}{2Q_t^2 V_{osc}^2} \left(\frac{\omega_0}{\Delta\omega} \right)^2 \right) = 10\log\left(\frac{kT}{2Q_t^2 \alpha_I \alpha_V P_{DC}} F \left(\frac{\omega_0}{\Delta\omega} \right)^2 \right) \quad (2.8)$$

where, R_t is the equivalent parallel resistant of the LC tank, k is Boltzmann's constant, T is the absolute temperature. α_V and α_I denoted as $\frac{V_{osc}}{V_{DD}}$ and $\frac{I_{\omega 0}}{I_{DC}}$ respectively. This relationship thereby derives the noise factor, F as;

$$F = \sum_i \frac{R_t}{4kT\pi} \int_0^{2\pi} \Gamma_i^2(\emptyset) \overline{i_{n,i}^2}(\emptyset) d(\emptyset) \quad (2.9)$$

where Γ_i^2 is the ISF and $\overline{i_{n,i}^2}(\emptyset)$ is the source of noise.

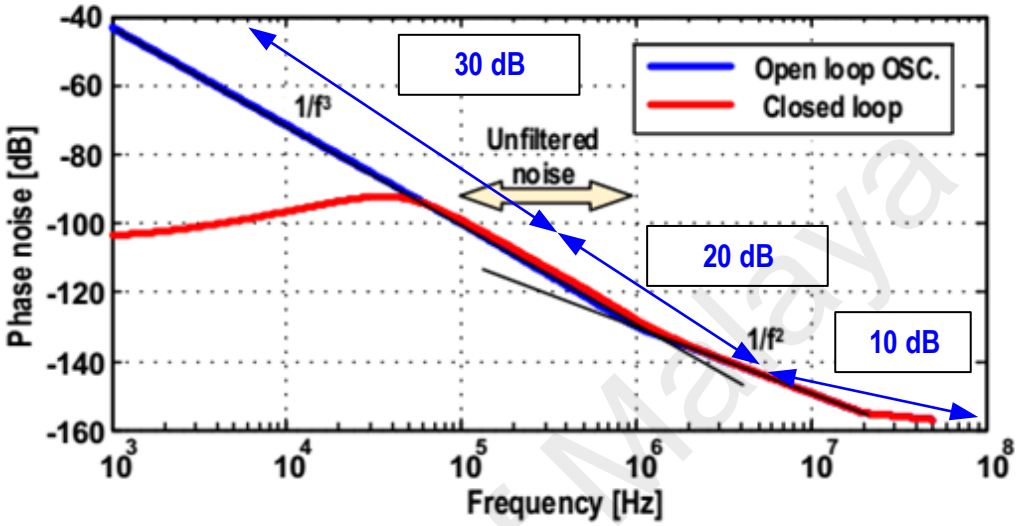

Figure 2.2: Phase noise region for open loop and closed loop oscillator against frequency offset

The noise perturbation from noise sources affects the phase noise versus frequency offset graph as shown in Figure 2.2. Since power spectrum, $S_\emptyset$ is inversely related to the square term of the frequency offset, ω_m which explains the $\frac{1}{\omega_m^2}$ (-20dB/dec slope) at the tail in reference to the white noise source, whereas $\frac{1}{\omega_m^3}$ presents as (-30dB/dec slope) which noted as $\frac{1}{f}$ flicker sources. Most asymmetric oscillation results in an impulse sensitivity function (ISF) of a non-zero dc value which ease the 1/f noise up-conversion into -30 dB/dec slope, $\frac{1}{\omega_m^3}$ region. To attain a much symmetric result, the fundamental resonance tank, ω_0 need to exhibit an auxiliary resonance, $2\omega_0$ to yield a more suppressed flicker noise up-conversion into the close in phase noise region.

2.3 Oscillator Research Works

Numerous research works has been carried out by current researchers to improve the stringent performance of the VCO, at the same time solving the tradeoff it compensate. Therefore it has been classified with their contribution accordingly which eventually helps in delivering the proposed VCO architecture under targeted performance.

2.3.1 Oscillators with Startup improvisation.

Class-C VCO encounter startup problem while achieving a stable output frequency. This results in the poor jitter in time domain and degrade the phase noise in frequency domain of the Power Spectral Density, (PSD) spectrum. Prior to that, the startup improvement often been done through the influenced of the biasing condition affecting the current efficiency as well. Therefore, few works has been explained accordingly with respective to startup and phase noise improvement.

2.3.1.1 Dual Conduction Class-C CMOS VCO

The architecture proposed by (Takeuchi, Okada, & Matsuzawa, 2011), shown in Figure 2.3 represents a dual conduction of Class-C CMOS VCO with ultra-low supply voltages. The two negative resistance form from the active cross-coupled NMOS pairs, M_1 and M_2 hybrid with M_3 and M_4 adopting different biasing condition, $V_{bias\,1}$ and $V_{bias\,2}$ .This has realize a impulse-like current waveform in order to improve the phase noise in low voltage supply headroom provided. This has been implemented under 0.18 µm CMOS technology platform where it oscillates at its carrier oscillation frequency of 4.5 GHz at 0.2 V voltage resulting in a measured phase noise of -104 dBc/Hz at 1 MHz offset under power consumption of 114 µW and a FoM of -187 dBc/Hz which as shown in Figure 2.4. This hybrid architecture are based on a single cross-couple pair configuration

implemented in (Amin, Yin, Mak, Member, & Martins, 2015) which improves the tradeoff by integrating an auxilliary Class B cross-couple pair in parallel to the cross-couple active core of Class-C VCO to ensure a robust startup at significantly low gate bias voltage, $V_{BIAS,N}$. However, the drawback encounter has low current efficiency due to fewer improvement in the current conduction angle as compared to the existing conventional Class C- VCO topology .

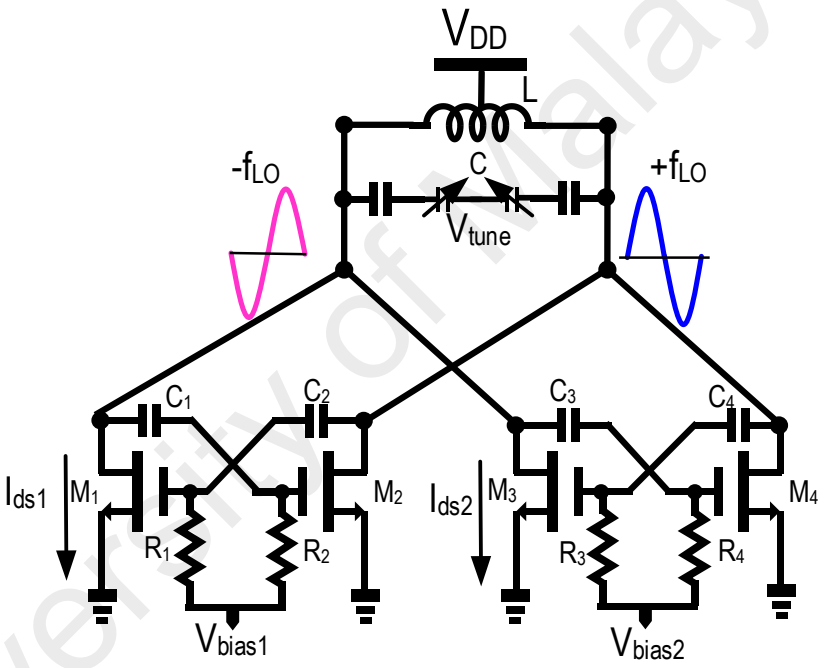

Figure 2.3: Schematic of a dual type conduction CMOS Class C-VCO

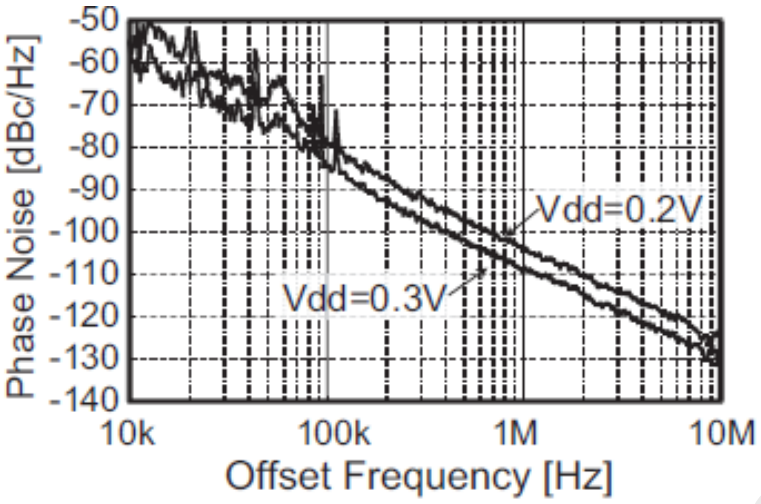

Figure 2.4: Measured phase noise at 4.5 GHz oscillation frequency.

(Takeuchi et al., 2011)

2.3.1.2 An Amplitude Feedback Loop Robust Startup and Enhance Oscillator Swing of Class-C VCO.

This architecture in Figure 2.5 reported by (Deng, Okada, & Matsuzawa, 2013) shows a feedback loop of Class-C VCO that entailed a robust start up and large oscillation amplitude. This architecture starts oscillating and transforms automatically into an amplitude enhanced class VCO at steady state condition in exhibiting an improved PN performance. The design is implemented in a 0.18 µm CMOS process and at 1 MHz measured -125 dBc/Hz of PN depicted in Figure 2.6, while dissipating entire power of only 3.4 mW at the oscillation frequency of 4.84 GHz. The figure of merit, (FoM) achieved is -193 dBc/Hz .The design has impede the quality factor,(Q) of the resonant tank due to additional blocks integrated by an amplitude detector in the negative feedback loop which adjust the biasing voltage, $V_{BIAS,N}$. This eventually leading to VCO tank loading effect with high power consumption, low reliability and narrow tuning range.

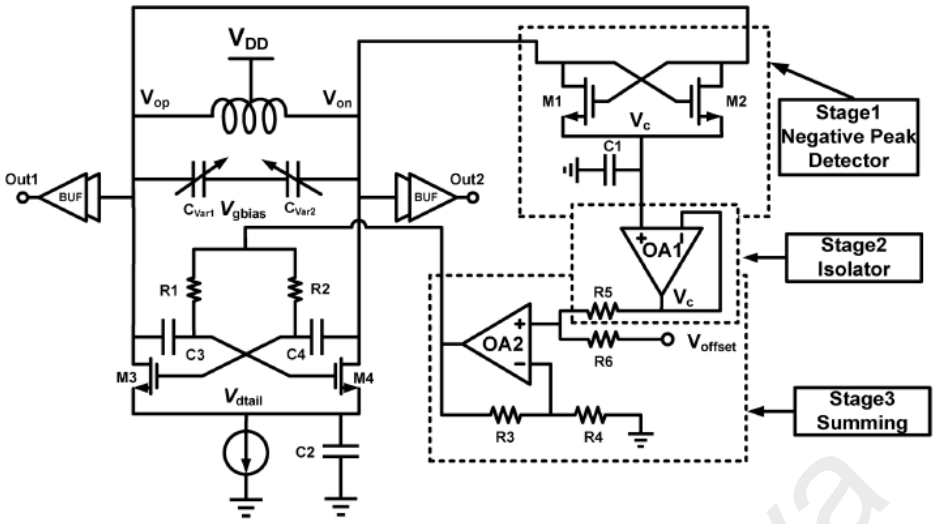

Figure 2.5: Feedback class C-VCO.

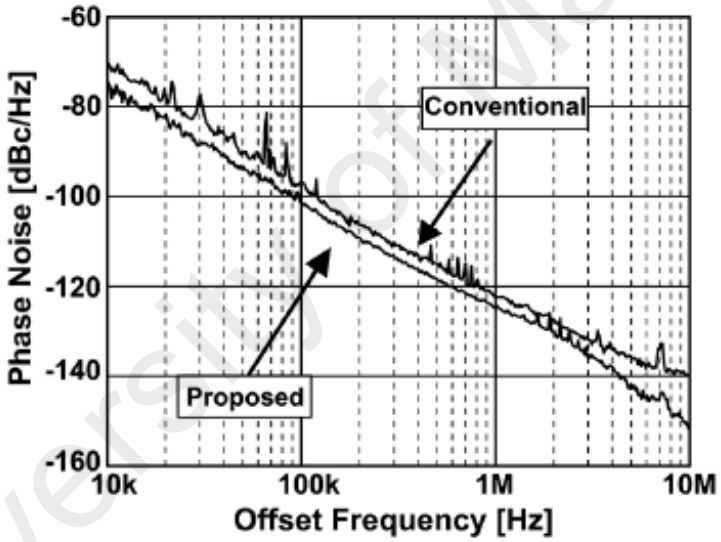

Figure 2.6: Measure PN characteristic: (upper) conventional Class C-VCO and (below) proposed VCO at 4.84 GHz.

(Deng et al., 2013)

2.3.1.3 Robust Startup Condition with Negative Feedback

This topology concept design invented by (Fanori & Andreani, 2012) is shown in Figure 2.7. This architecture designed in 90 nm CMOS platform able to achieved the

tuning range of 28 % in the bandwidth of 3.4- 4.5 GHz with the PN of -147 dBc/Hz at 10 MHz shown in Figure 2.8. It consist of two active cross-couple pair, M_1 and M_2 as the source of negative resistance function to replace the energy losses in the resonant tank which is integrated with coarse and continuous tuning circuit. The tail transistor, M_t controls the current of the circuit branch to ensure constant startup and sustaining the oscillation. The negative feedback sense the common mode voltage, V_{CM} at the common source node of M_1 and M_2, which controls the biasing voltage of M_1 and M_2 keeping both at fixed saturation point. This solve the startup problem and serve as a solution to keep the transistor in active region always. However, experienced a downside as it requires a huge amount of power around 6.6 mW and bad area efficiency due to complex tuning circuitry.

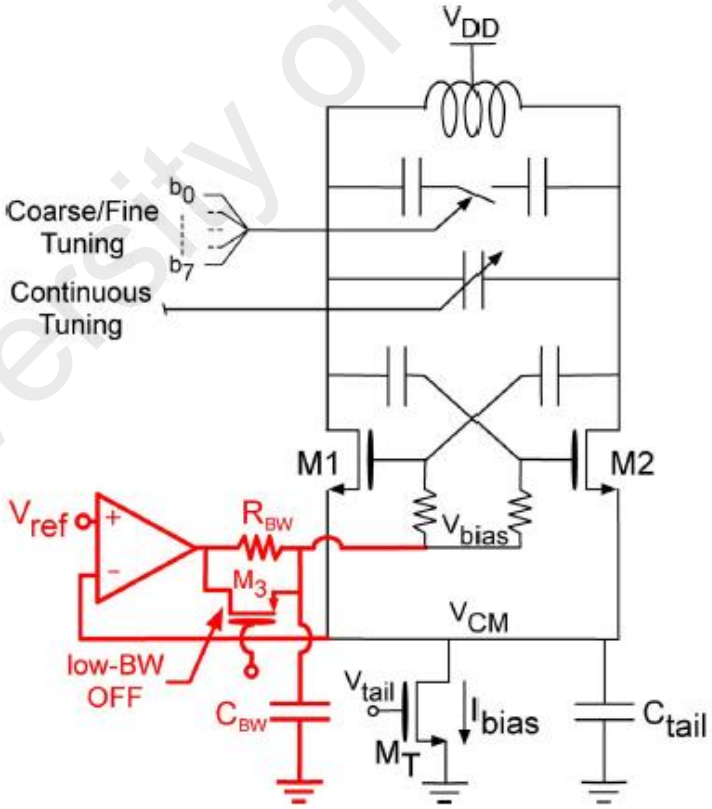

Figure 2.7 Class C-VCO with MOS tail current source

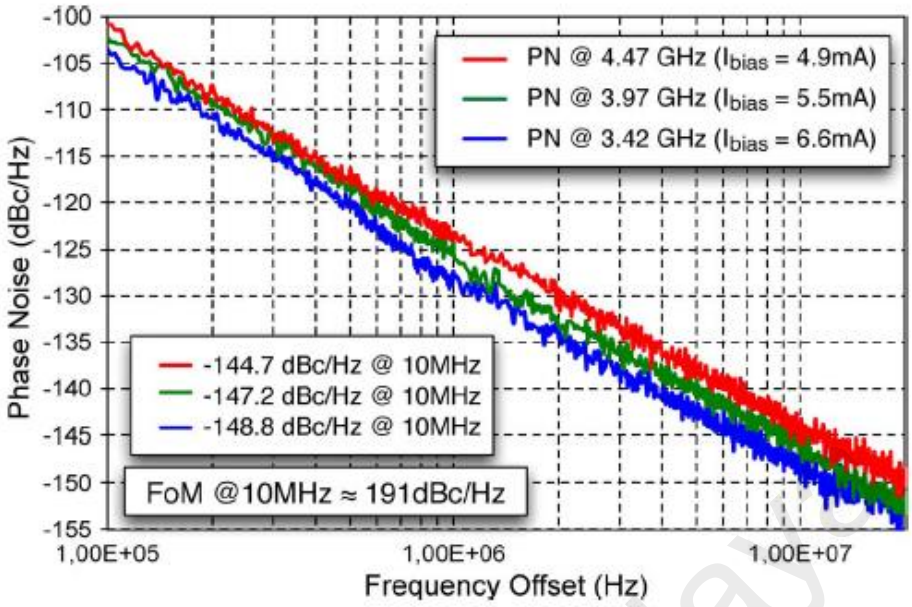

Figure 2.8: Phase noise measurement at minimum, middle and maximum oscillation frequency.

(Fanori & Andreani, 2012)

2.3.2 Robust and High Power Efficiency Oscillators

Class-B Oscillator are well known of its robustivity towards Process, Voltage and Temperature, (PVT) variations (Shahmohammadi, Babaie, & Staszewski, 2016b). The current efficiency is well achieved due to the gate biasing adopted leading towards better current and overall power efficiency.

2.3.2.1 Class-B Oscillators

Traditional class–B oscillators as illustrated in Figure 2.9 is the most robust architecture. Alternately Class B VCO phase noise and the performance of the power efficiency degrades significantly by substituting the ideal current source with a real active transistor of M_T at the tail. This is due to the nonlinearity harmonics of the tail transistor component, M_T which has injected into the Class-B resonant tank, slightly affecting the close in PN performance as compared to an ideal current source.

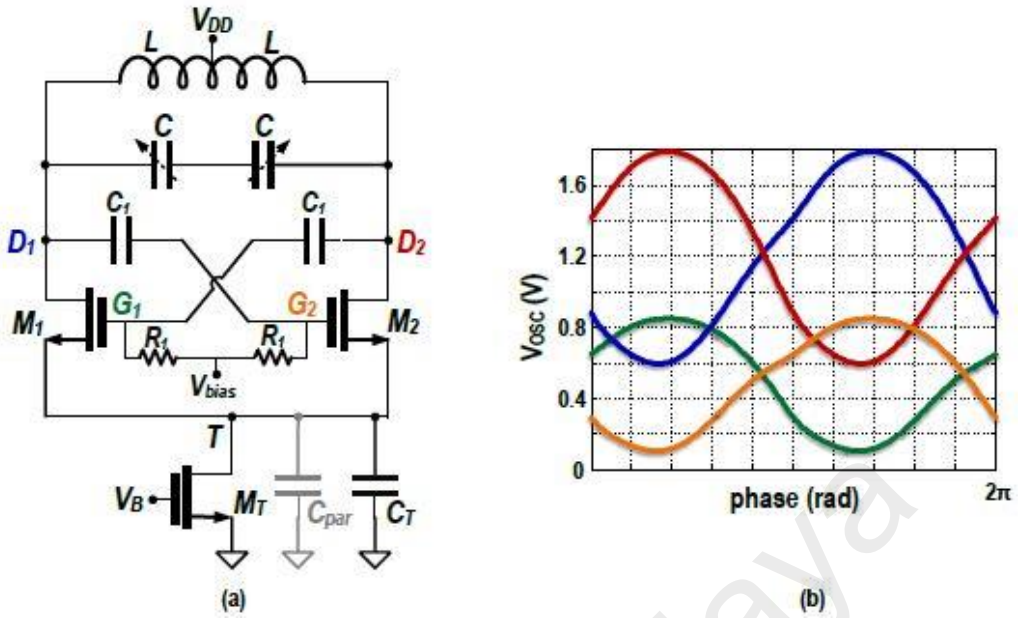

Figure 2.9 (a) Traditional class-B VCO (b) its voltage waveforms

(Murphy, Rael, & Abidi, 2010)

The traditional class- B oscillator, due to its simplicity and robustness, this structure able to reduce the PN and power consumption of the oscillator depending on the level of its efficiency. The noise factor in a class-B is equal to $y + 1$ (Murphy et al., 2010) where y is the channel noise factor which is ideal if M_T transistor acts an ideal current source. The current source does not produce phase noise, as it only offers a high level of impedance at the common source of the $-g_m$ transistors, M_1 and M_2 which are located at the drain of the tail transistor, M_T . This appear to be beneficial with increasing the tank's quality factor, (Q) which reduces the oscillator's phase noise. However, the tank's quality factor, Q_T depends on the both the inductive, Q_L and capacitive quality factors, Q_c as expressed;

$$\frac{1}{Q_T} = \frac{1}{Q_L} + \frac{1}{Q_c} \tag{2.10}$$

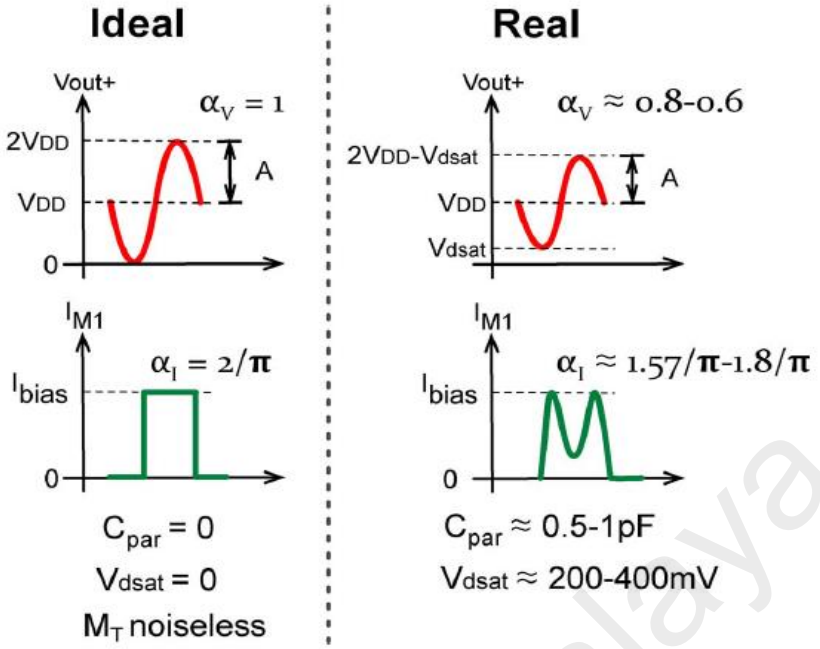

Figure 2.10: Differentiation between ideal and real class B VCO.

The contrast between ideal and real performance of Class B VCO shown in Figure 2.10 focuses on the voltage waveform at the output and on the current I_{M1} flowing through M_1. Output swing will be maximized, where the peak value becomes as high as V_{DD}, resulting in a voltage efficiency α_V equal to 1. In addition, M_1 and M_2 behaves like an ideal switch, resulting in an ultimate square waveform, making the fundamental harmonic component to multiply with the DC current biasing I_{bias} resulting in a current efficiency α_I equal to $2/\pi$. In equation (2.10) shows that the quality factor of the inductor, Q_L is limited by the resonator tank quality factor, Q_T (technology dependent). This parameter of Q_T are dependent on the capacitive and inductor quality factor where the parameter of the capacitive quality factor, Q_C, gives a significant effects towards the tuning range, (TR) and phase noise, (PN) of the oscillator depending on the frequency bandwidth. Besides, another approach adopted to improve the oscillator phase noise is by adequately sizing the tank inductance, L while preserving the quality factor as expressed;

$$R_t = L\omega Q_t \tag{2.11}$$

where lowering of the tank resistance, R_t adversely affects the power consumption of the oscillator, $P_{DC} = \frac{V_{osc}^2}{\alpha_I \alpha_V R_t}$ resulting in a constant Figure of Merit, (FoM). PN improvement via Q enhancement technique has been adopted by integrating a novel resonant circuit (Park, Lee, Choi, & Hong, 2008) or through harmonic filtering as proposed by (Hegazi, Sjöland, & Abidi, 2001). The harmonic filtering technique connects a noise filter by adopting a bulky inductor and capacitor at the drain of the tail current source to achieve an even order harmonic filtering which down-converts the VCO oscillation to the fundamental frequency in the mixing process. A harmonic tuned resonant tank employed in (Babaie & Staszewski, 2013) creates a third harmonic component via an additional impedance peak, producing a pseudo-square waveform thus improving the zero-crossing slope. This leads to shorter commutation time while achieving a lower effective noise factor. To circumvent the harmonics, (Men, Thangarasu, & Yeo, 2016) biased the tail current source transistor at $2f_{LO}$ to suppress the cyclostationary noise via accumulation and strong inversion pattern. Reducing the inductor size also affects critically which limits the quality factor due to tank interconnection losses. Since the tail current source controls the entire current flow of the circuit, and linearly dependable on the power consumption. The traditional oscillator reaches good performances for the oscillation amplitude at the nearest supply voltage.

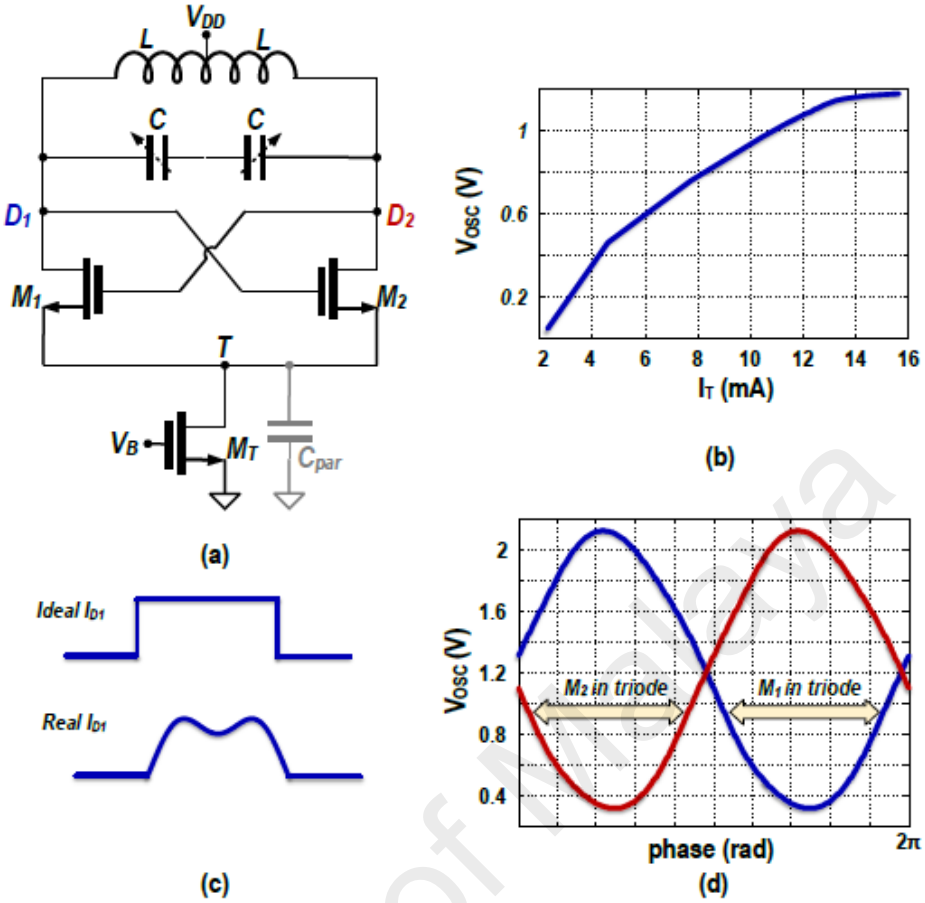

Figure 2.11: Class – B oscillator (a) schematic; (b) voltage oscillation amplitude versus tail current; (c) ideal and real drain current waveforms; (d) differential oscillation waveforms at point D_1 and D_2 respectively.

If active $-g_m$ negative resistance, M_1 and M_2 devices enter deep triode region, forming a low channel resistance which is about few tens of ohms. Besides that, Figure 2.11 shows that the tail parasitic capacitor, C_{par} are made large so as to act as a thermal noise filter and suppressed the even harmonics, thus making a low impedance pathway between node "T" and ground. The tank output nodes will eventually find a discharge path to the ground and degrade the performance of quality factor, Q of the tank. This event happens in alternative time between transistors operating at each oscillation period. Hence the phase noise improvement would be small or considered negligible by increasing the oscillation voltage swing when the active $-g_m$ devices enter into triode region and FoM drops

dramatically. Several architectures implemented a filtering mechanism using relatively large capacitor at node "T", which also creates a high impedance path preventing the discharge path back to the resonant tank. However, this implementation requires an extra space adding passive bulky component of an inductor despite being as part of effective noise reducing technique.

Thus, FoM of class B oscillators is heavily dependent on the technology-driven tank-Q, i.e., on the Q of inductor (s) and capacitor (s) and on-resistance, r_{on} of the MOS switches used for discrete frequency tuning. The tuning range of the VCO gets limited by the large MOS switch parasitic capacitance of M_1 and M_2.

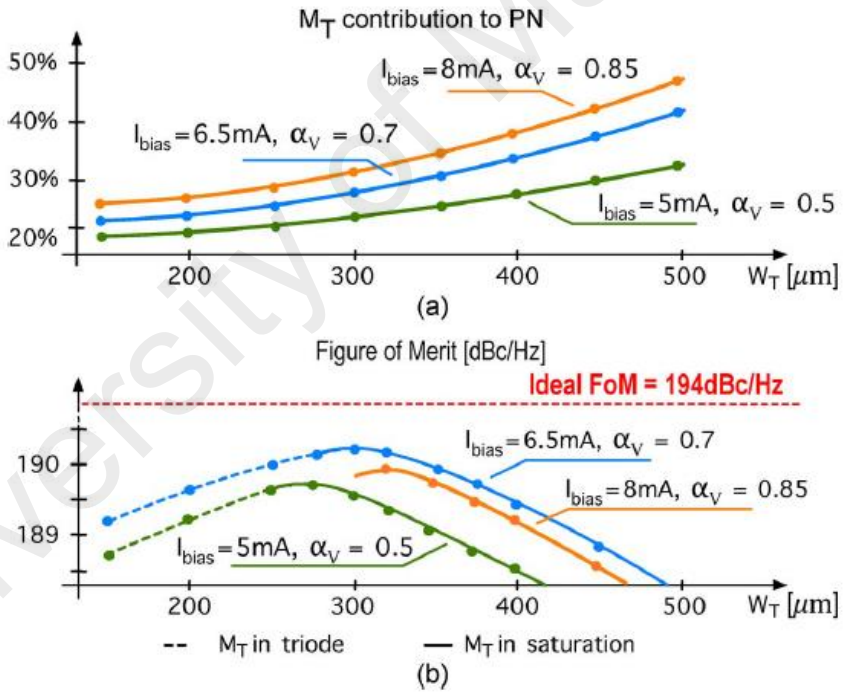

Figure 2.12: (a) M_T contribution towards PN plot (b) resulting FoM for different value of bias current, voltage efficiency and transistor's width.

The simulated thermal noise contribution of tail transistor, M_T to phase noise and the resulting FoM, as function of width of M_T for different values of α_V shown in Figure 2.12. The M_T will operate in triode region, providing a lower current than expected when the

width of M_T is made small. In order to achieve the best FoM for a given I_{bias}, the tail transistor, M_T width need to be made large enough and usually sized double to work in saturation region. Bias current, I_{bias} has a nullifying effect with larger width but instead it affects the transconductance and current noise more which degrades the phase noise performances. The VCO achieves maximum FoM for α_V below unity (< 1), due to increase in current noise generated by M_T, offsets the benefit of having larger amplitude. The optimum supply voltage value in state–of–the-art CMOS process is 0.6 - 0.8V, therefore the contribution of flicker noise, *1/f* up-conversion of M_T to phase noise region cannot be kept below 25-30% of the power consumption, thereby reducing the achievable maximum Figure of Merit, (FoM) by 2.8-3.5 dB, as compared to the ideal simulated FoM.

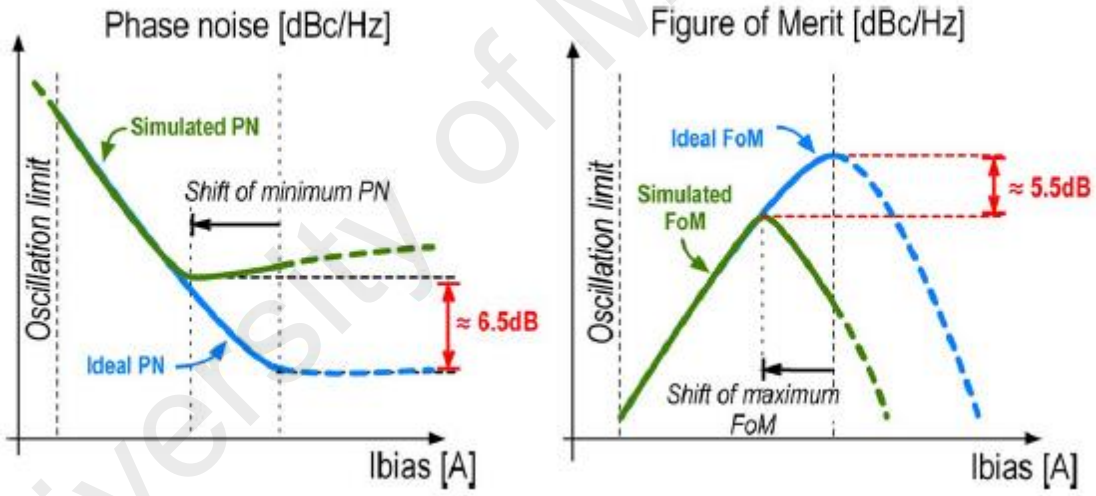

Figure 2.13: Phase noise and FoM comparison between ideal and simulated Class –B VCOs (minimum ideal phase noise and maximum ideal FoM are obtained for peak single –ended oscillation amplitude equal to V_{DD}).

The simulated FoM of Class-B VCO shown in Figure 2.13 degraded around 5 – 6 dB compared to the ideal FoM due to the noise contribution from the tail current and the non-linear harmonic introduced by the LC tank capacitance.

2.3.3 Large Swing Amplitude Oscillators

Class D VCO is specified for a high amplitude as the cross-couple active transistors are dependable to the voltage headroom from power supply. The output swing is not limited as the tail current source has been alleviated in this structure.

2.3.3.1 Class-D Oscillators

Class D oscillator employed by (Fanori & Andreani, 2013b) as shown in Figure 2.14 is achieved by removing the tail current source (current control circuitry), where the supply voltage, V_{dd} can be reduced down to as low as 0.35mV while still generating the output amplitude as large as 3 times the supply voltage by sizing the cross-coupled NMOS transistor pair, M_1 and M_2 higher.

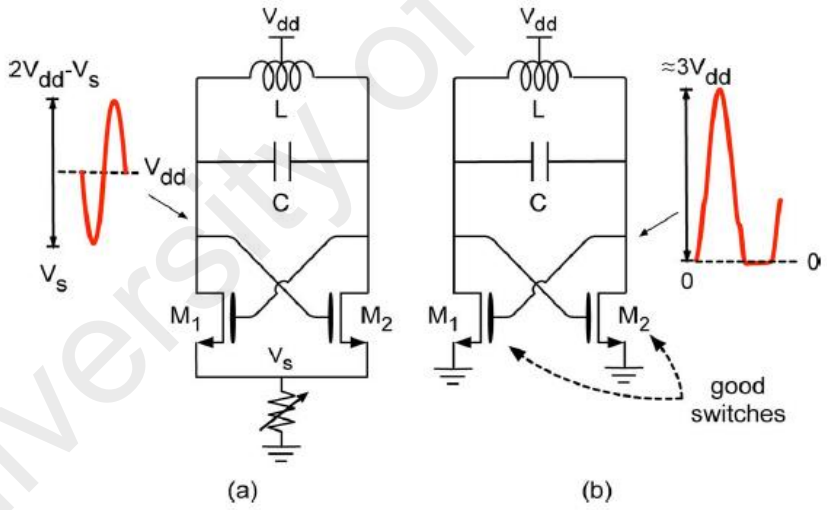

Figure 2.14: (a) Class B VCO with tail resistor (b) Class D VCO oscillator

(Fanori & Andreani, 2013b)

The Class D VCO has the benefit in providing high oscillation amplitude and suitable for low-voltage application. In addition, Class D architecture offers the benefit of an unsurpassed design simplicity apart from resonator LC tank, where this feature requires only two switched transistor (M_1 and M_2), where the performance encounter several

advantages of device scaling in CMOS technologies and disposes current-bias circuitry, typically needed as in class-B/C VCOs, (Fanori, Mattsson, & Andreani, 2014) which affects the dynamic tuning range and contributed to noise region.

The drawback encounters where the tuning range is reduced due to the presence of high intrinsic parasitic capacitance of gate to source, C_{gs} and gate to drain, C_{gd} from the active $-g_m$ device of the cross-coupled pair. Besides it also has weak supply pushing, which poses a difficulty in achieving high swing since being proportionally and sensitively dependent on the voltage headroom.

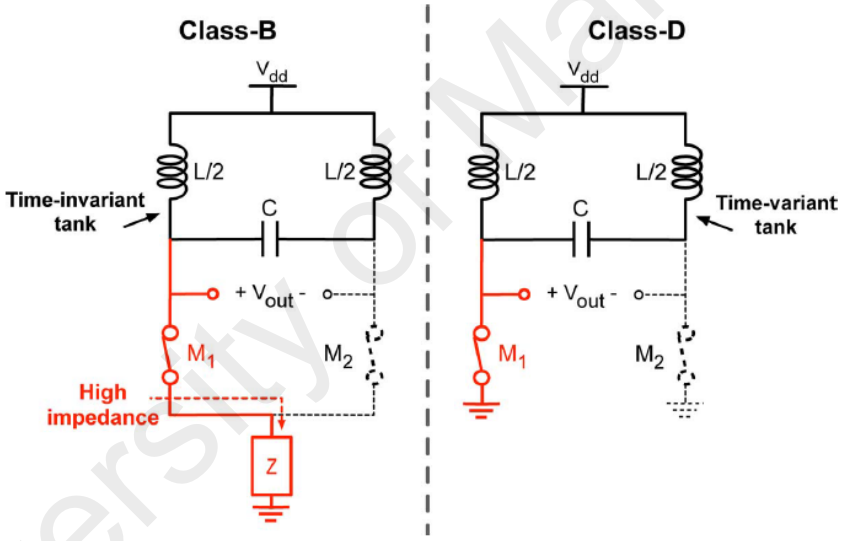

Figure 2.15: Time-invariant, LTI tank in class-B oscillator versus time-variant tank, LTV in class-D oscillator.

A key difference shown in Figure 2.15 between class-D and class-B/C oscillators is that the class-D based *LC* tank oscillator displays a LTV nature, which is quite distinct from that of the LTI of Class-B/C *LC* tank. Figure 2.15 explains the configuration of the resonator tank in the two cases. In the Class-B/C tank, passive components, L and C inductor lies in parallel with each other forming a LC tank and relatively creates a high tail impedance that decouples both from ground. Besides, Class-D tank transistor M_1 and

M_2 switches, short on each of the oscillator output to ground for half of the oscillation cycle, when the components decoupled from each other. It seems to show a marginal comparison producing a paramount impact on the Class-D oscillator's performance in terms of oscillation frequency, current consumption, and phase noise. The quality of time-variability exist from the combination of time-invariant inductors/capacitors and time-variant MOS switches. It also shows convenient use of a single parallel tank resistance assuming series losses in a LTI tank. The switching pair of the active devices, M_1 and M_2 is size comparable to the inductor. Furthermore due to low V_{dd}, the supply pushing is much sensitive than in Class –B/C VCOs exhibiting a challenge especially in designing with a low-dropout voltage regulator for high practical application.

2.3.3.2 High Swing Class C-VCO

The architecture proposed by (Tohidian, Fotowat-Ahmadi, Kamarei, & Ndagijimana, 2011), adopts a tail current source removal in Class-C VCO resulting in a high swing VCO core as shown in Figure 2.16. The transformer is been added into as an additional degree of freedom so that the bias control circuit controls the gate bias of the switching pair, M_1 and M_2 to a high voltage for large tank swing. Besides, this also helps in gain boosting, thus improving the signal swing.

This high efficiency topology combined with high output swing adds the advantage leading towards a superior PN performance. The VCO oscillating at 5.11 GHz draws 1.44 mA of current from 0.6 V power supply. The phase noise measured to be -127 dBc/Hz at 3 MHz offset frequency resulting in a FoM of 192.3 dB. The author is able to remove the tail current source altogether by generating $V_{bias\,1}$ via an elegant current mirror solution which enable in preserving the current consumption at a fixed level as desired. The robustness of the bias control circuit maximized the robustness of the startup functionality

since the two branch of the current mirror work in comparative signal excursion at the respective drains.

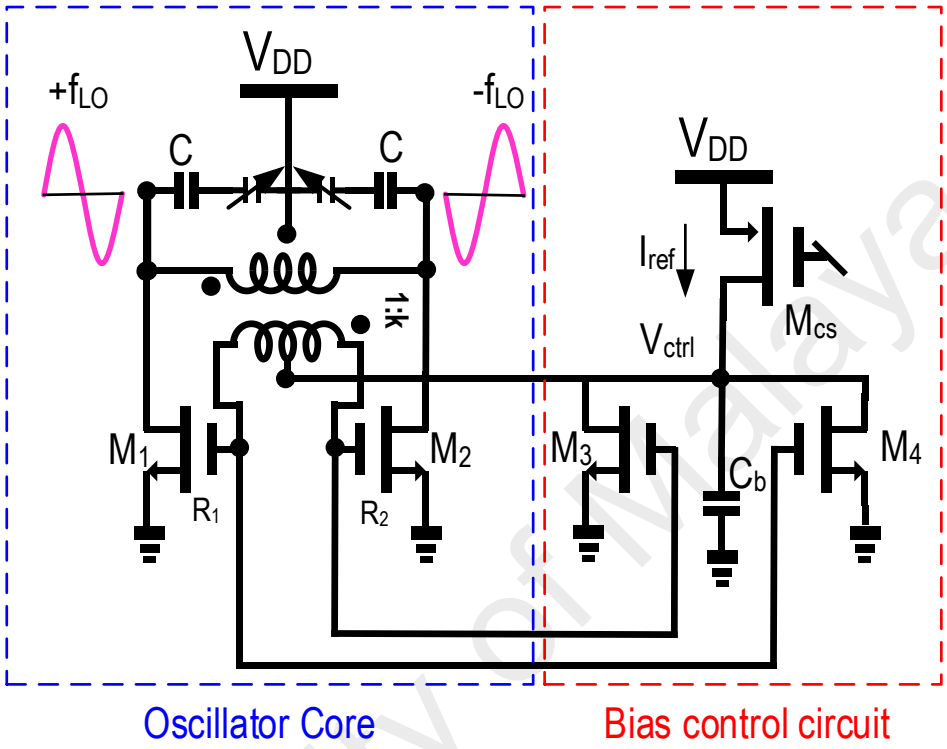

Figure 2.16: Proposed high-swing class-C VCO

(Tohidian et al., 2011)

2.3.4 1/f Flicker Noise Upconversion Reduction Techniques

The symmetrical rise and fall time of an oscillator waveform is achievable when auxiliary resonance at $2\omega_o$ is reached, thereby reducing the flicker noise, *1/f* up-conversion.

2.3.4.1 Current-Biased RF Oscillator

A typical oscillation generate asymmetric rise and fall times due to second harmonic current which flows into the capacitive low impedance path. This results in an asymmetric oscillation waveform and causes an ISF function of a non-zero dc value to up-convert the *1/f* flicker noise into the oscillator's $1/f^3$ phase noise region. The flicker noise up-conversion can be alleviated when the ω_o single resonance tank exhibits an auxiliary twice resonance, $2\omega_o$ diverting the current harmonic into the equivalent resistance of the $2\omega_o$, producing a more symmetrical output oscillation waveform. The auxiliary resonance is observed under low area at no extra bulky inductors and transformer based resonator tank. This exploits a different behaviors of such bulky components in two mode of differential and common mode excitation. In Figure 2.17, shows a current biased RF oscillator in class –B concept which always run in saturation resulting a slight reduction in *1/f* noise. The flicker noise contributor, M_T upconvert the PN via AM to PM conversion mechanism through non-linear capacitance of active device, M_1 and M_2 and varactors, C_V. Figure 2.18 initiates a solution to drive the oscillator towards a voltage-biased mode by removing the M_T or substituting with a resistor, R_T at the tail. This structure has improve the PN performance prominently shown in Figure 2.19 (left) whereas the Figure 2.19 (right) shows the PN performance when M_T enters triode (Levantino et al., 2002) while degrading the effective noise factor, ENF. However, eliminating the M_T would not be as a better improvement to reduce the *1/f* noise up-conversion.

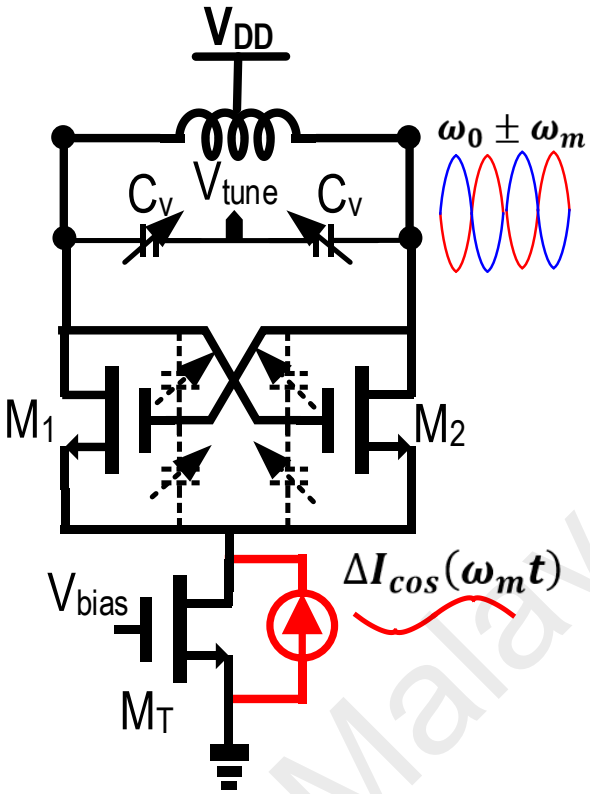

Figure 2.17: Class-B oscillator with flicker noise, $\frac{1}{f}$ contributor of M_T

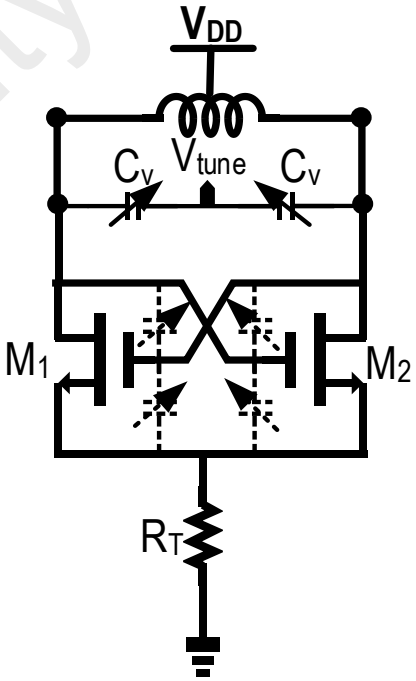

Figure 2.18: Class-B Oscillator with tail, M_T replaced by R_T

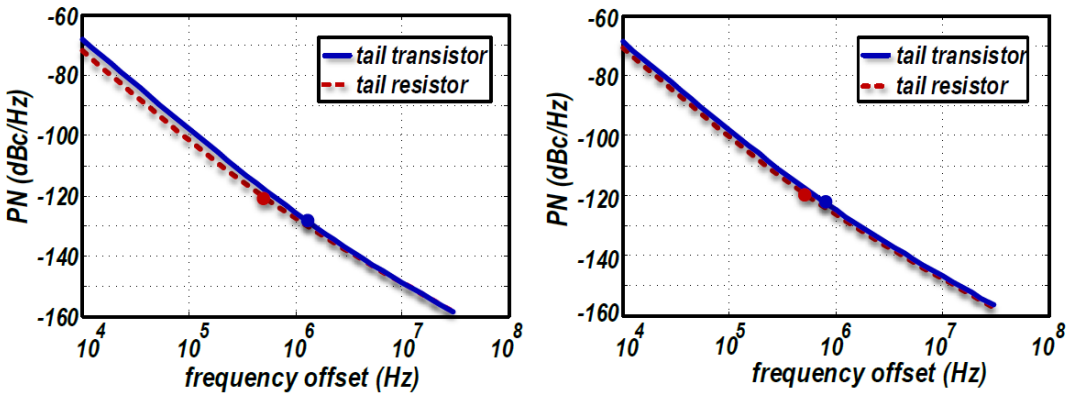

Figure 2.19: Class-B oscillator M_t (left) in saturation (right) in triode region.

2.3.5 Low Power Consumption in Oscillators

The oscillator is a power hungry block. Lowering the power consumption while targeting a fast startup and low phase noise is tough challenge adopted by the RF researches.

2.3.5.1 Dual-Conduction Class-C VCO using a Tail Resistor

(Takeuchi et al., 2011) , proposed a method shown in Figure 2.20 sets to improve the power consumption of dual conduction of Class-C VCO that has two pairs of cross – coupled transistors for a low voltage supply operation. It consists of two cross-couple of active core pair designed for Class-C operation and the other in an auxiliary pair of Class-B for startup purpose. This startup pair continues to operate after the VCO operates at the Class-C mode in a penalty of an additional power. Therefore a resistor, R_{tail} is added to the source node of the auxiliary pair to lower down the power consumption. The VCO is fabricated using 0.18 µm CMOS technology, oscillates at 5.4 GHz under 0.2V supply voltage, consumes 96 µW of power and achieves a FoM of -187 dBc/Hz. The drawback encountered when the auxiliary pair for startup solution operated Class C mode required a substantial additional power with higher gate bias, $V_{bias\,1}$ injected, thereby degrading the performance of the phase noise as depicted in Figure 2.21.

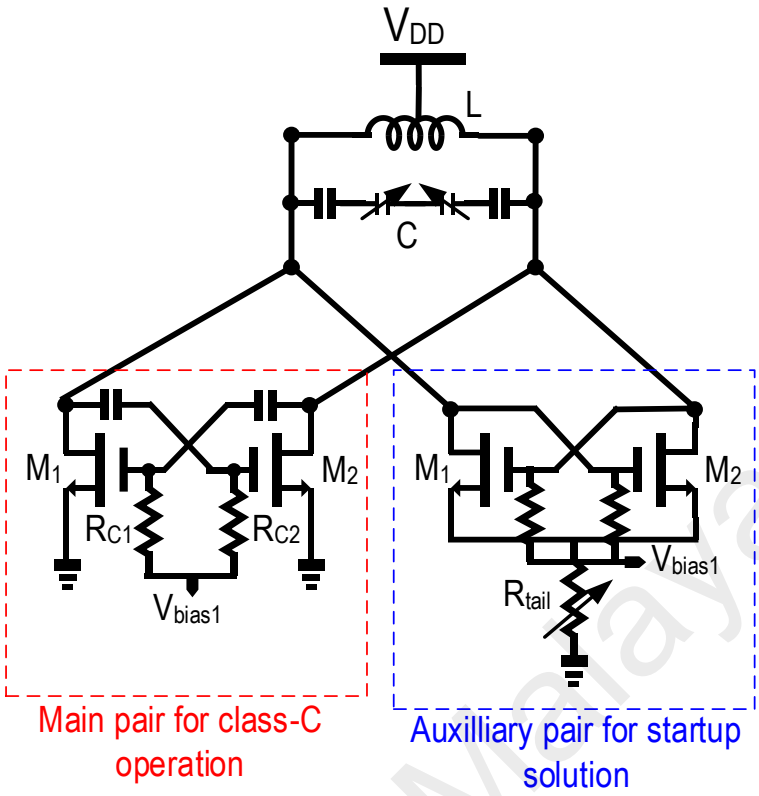

Figure 2.20: Resistor added dual-conduction class-C VCO.

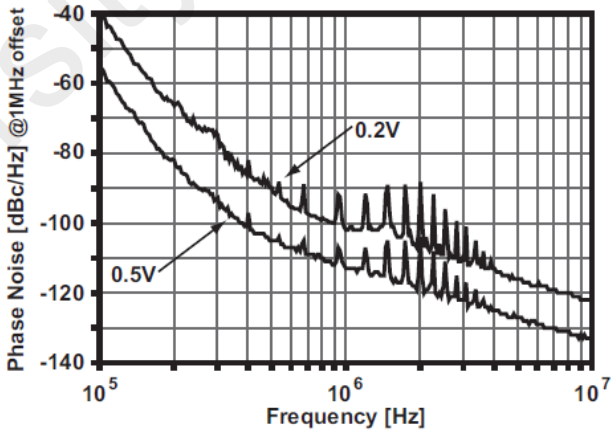

Figure 2.21: Measurement result of the phase noise.

(Takeuchi et al., 2011)

2.3.5.2 Push-Pull Class-C CMOS VCO

(Mazzanti & Andreani, 2013) , proposed a VCO employing differential transistor cross-couple pairs operating in Class-C push pull configuration as given in Figure 2.22. This VCO exhibits the same advantages by a complementary topology based on a single differential pair, yielding a substantial power consumption reduction. It is shown that, to achieve an optimal performance, both the complementary MOS, M_1 - M_4 should not be pushed into deep triode region by the resonator voltage to accommodate large oscillation swing. This structure implemented in a 0.18 µm CMOS platform which measures an oscillation frequency from 6.09 to 7.50 GHz. The phase noise shown at Figure 2.23, depicts that the 2 MHz offset is below -120 dBc/Hz consuming power of only 2.2mW for the Figure of Merit, FoM ranging from 189 to 191 dBc/Hz. This design unfortunately exhibits lack of compactness, requiring a high Q-factor inductive devices in this high performance VCO. Table 2.1 shows the Excess Noise Factor, ENF comparison and its current, voltage and power among the classes of reported VCO works.

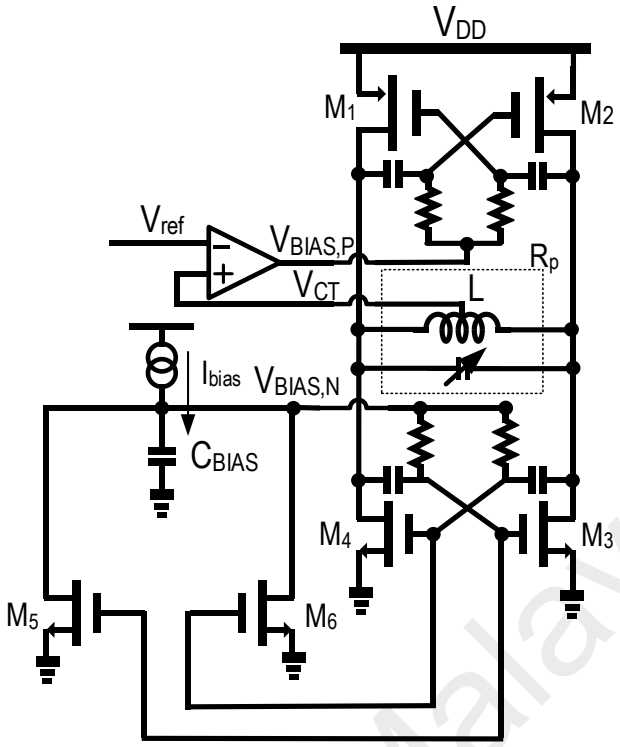

Figure 2.22: Proposed push -pull Class C-VCO

(Mazzanti & Andreani, 2013)

In reference to Figure 2.22, by assuming the parallel resonant tank resistance, $R_p = 2\pi f_{osc} L Q_{ind}$ where $Q_{ind} = (\omega_o L)/R_s$, the startup condition is expressed as;

$$\frac{(2\pi f_{osc})^2 L^2}{R_s} > \frac{2\alpha}{g_m} \tag{2.12}$$

where R_s is the inductor's series resistance, L is the inductance of the LC tank (Yoon, Lee, Kim, & Choi, 2014), f_{osc} is the VCO's oscillation frequency and α is the design factor selected to be larger than 1 for startup condition taking into account of the process-voltage-temperature (PVT) variation**.** Therefore, from the startup condition in (2.12), the frequency of oscillation for a low frequency (LF) band is denoted as;

$$f_{osc,low} = \frac{1}{2\pi}\sqrt{\frac{2\alpha R_s}{g_m L^2}} \tag{2.13}$$

Besides satisfying the startup condition, the flicker noise up-conversion from the tail transistor to the PN is a bottleneck in most conventional cross-coupled VCOs. Various efforts have been adopted to suppress the tail noise and to shape the tail current into a Class-C waveform**.** The technique in (Jafari & Sheikhaei, 2018) utilized a low-pass and a notch filter connected between the tail transistor and the common-source node of the switching transistor to suppress the second harmonic noise from the tail transistor. This prevents the VCO from down-converting to the oscillation frequency which improves the PN but at the cost of using a bulky inductor. Another approach in (Heng, Bansal, & Zheng, 2011) where the noise cancellation technique applied at the trans-conductance stage also results in noise suppression.

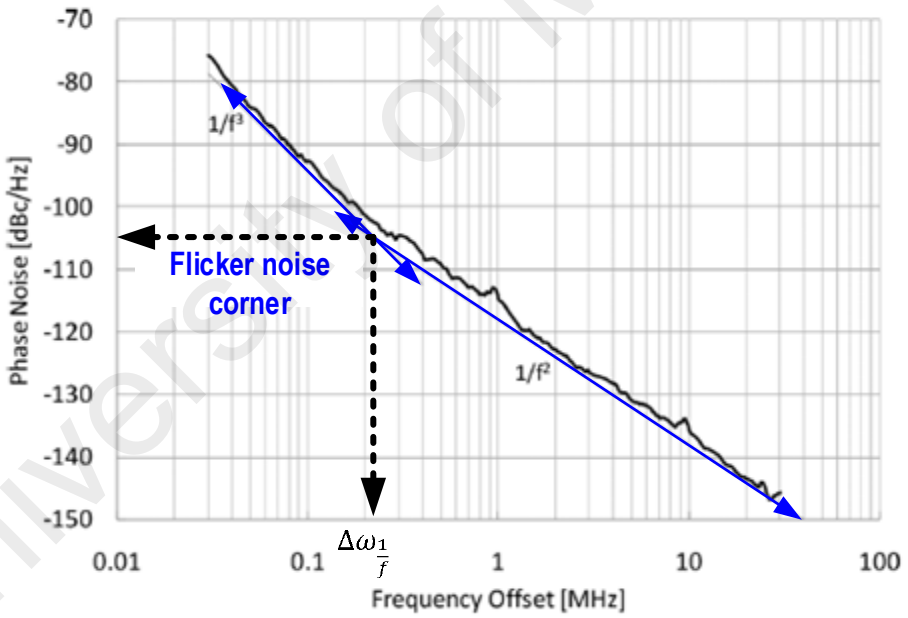

Figure 2.23: Measured phase noise, PN plot

Table 2.1 Excess Noise Factor, ENF with voltage, $n_{V,max}$, current, $n_{I,max}$ and power, $n_{P,max}$ efficiency comparison between classes of VCO.

Osc.Class	$n_{I,max}$	$n_{V,max}$	$n_{P,max}$	$ENF_{min}(dB)$
Class B	$\sqrt{2}/\pi$	$\sqrt{2}\left(1-\frac{V_{bias}}{V_{DD}}\right)$	$\frac{2}{\pi}\left(1-\frac{V_{bias}}{V_{DD}}\right)$	10
Class B-Bias	$\sqrt{2}/\pi$	$\sqrt{2}\left(1-\frac{V_{bias}}{V_{DD}}\right)$	$\frac{2}{\pi}\left(1-\frac{V_{bias}}{V_{DD}}\right)$	8.5
Class B-bias LC filter	$\sqrt{2}/\pi$	$\sqrt{2}\left(1-\frac{V_{bias}}{V_{DD}}\right)$	$\left(1-\frac{V_{bias}}{V_{DD}}\right)$	4.5
Class F	$\sqrt{2}/\pi$	$\frac{4\sqrt{2}}{\pi}\left(1-\frac{V_{bias}}{V_{DD}}\right)$	$\frac{8}{\pi^2}\left(1-\frac{V_{bias}}{V_{DD}}\right)$	8.5
Class C	$1/\sqrt{2}$	$1/\sqrt{2}$	$1/2$	6

2.3.6 Tuning Range Improvement techniques

The broadening of tuning range while achieving a low phase noise are challenging tradeoff for VCOs. Diligent tuning requires to minimize the amplitude modulation, (AM) to phase modulation, (PM) conversion.

2.3.6.1 Varactor Tuning

The varactor capacitance, C_V shown in Figure 2.24 are responsible in lowering the parasitic capacitance of the resonant tank and the active devices, since this influence the Q factor of the resonant tank at some critical point especially on the its fundamental frequency (Z. Chen, Hong, Chen, & Zhou, 2013). Therefore with adequate sizing of the varactor results in a broadening of dynamic tuning range of the frequencies .The amplitude modulation, (AM) to frequency modulation, (FM) conversion in this proposed structure are significant since fine tuning by the varactor are also responsible in lowering the effect of the parasitic capacitance of the active devices. This broadens the tuning range

of frequencies and enhance the Q factor rendering towards better PN performance. To reduce the fluctuations of the AM to FM noise, tuning voltage, V_{tune} are bias using extra filters for a clean dc noise filtering mechanism to lower down the phase noise to a reliable level. As the tuning voltage being noiseless, the varactor will detect a small envelope fluctuations in the AM to FM noise conversion which eventually suppresses the sidebands harmonics as shown Figure.2.25.

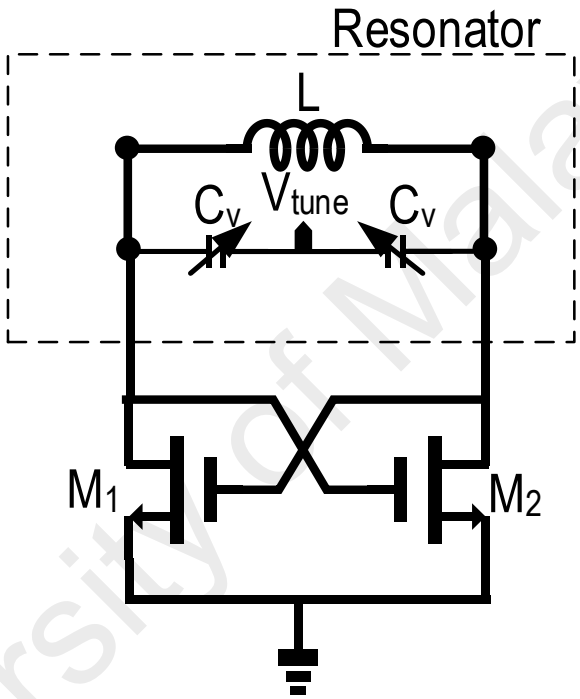

Figure 2.24: Class-D Oscillator with varactor fine tuning, C_V

(Z. Chen, Hong, Chen, & Zhou, 2013)

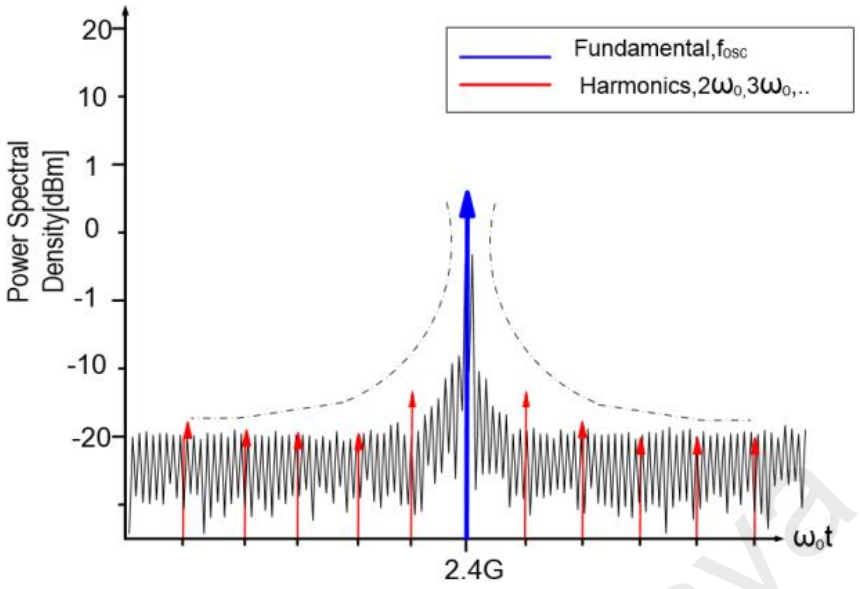

Figure 2.25: Lorentzian Power Spectral density, PSD at desired oscillation frequency

2.3.6.2 Switched Capacitor Tuning

Figure 2.26 shows a differential switched capacitor arrays which are integrated in the resonator LC tank to improve and widen the tuning range. Most capacitor banks adopts a transistor switching mechanism with integrated capacitor, C for discrete tuning depending on the conduction (Low/High (0/1)) of the transistor, M_1. This circuits are fitted in parallel to the resonator tank, switching alternately depending on the voltage level at the gate of the transistor, M_1. However, it encounters switching losses via excitation in OFF and ON mode, which affects the phase noise performance. Besides, it also bottlenecks in achieving area efficiency due to the circuit level complexity (Liu, Chen, & Chin, 2012). Switched capacitor arrays (Berny et al., 2005; S. Li, Kipnis, & Ismail, 2003; Moon, Roh, Jeong, & Yoo, 2009) and switched inductors (Geynet, Foucauld, Vincent, Jacquemod, & Einstein, 2006; Herzel, Erzgraber, & Ilkov, 2000; Kao, Yang, Chin, & McAlister, 2007; Yim & Kenneth K.O, 2006) are unique solution in VCO design for wide tuning range and multiple frequency operation. However, extra chip area with higher power consumption is required due to the increase in circuit complexity. An alternative method is by

employing a magnetic coupling effect to control the frequency tuning by an inductive switching to achieve a wide tuning range (Cusmal, Repossi, Albasini, & Svelto, 2007). This method requires an additional driving current which subsequently leads to lower energy efficiency.

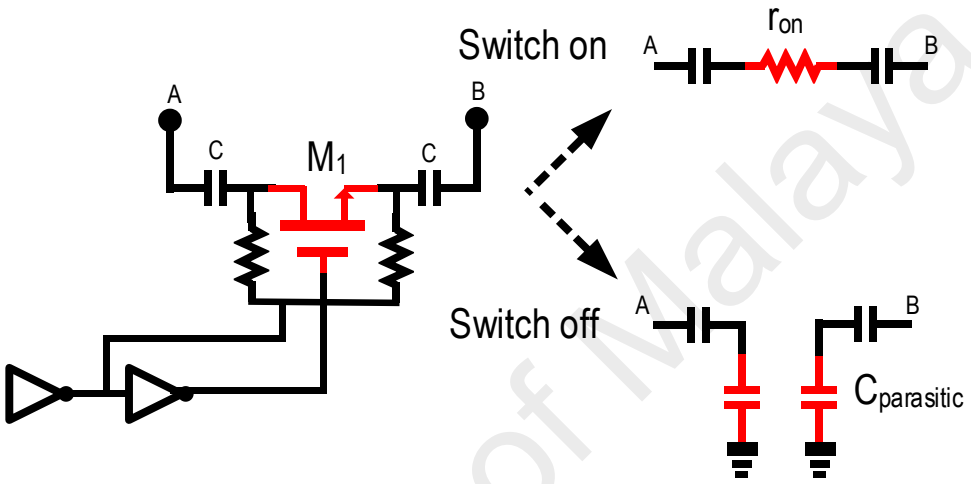

Figure 2.26: The differential switched –capacitor tuning when transistor is at OFF and ON state.

(Liu, Chen, & Chin, 2012)

2.3.6.3 6.7 to 9.2 GHz 55nm CMOS Hybrid Class B/Class-C Cellular TX VCO

The architecture by (Fanori, Liscidini, & Andreani, 2012) in Figure 2.27, is a design of a wide bandwidth CMOS VCO compliant with a non-trivial phase noise specification for cellular transmitter, especially considering GSM standard where the PN generated by the carrier signal required to be in several dB below -162 dBc/Hz at 20 MHz frequency offset from the carrier frequency shown in Figure 2.28.

This model is accomplished with the shift of the dc bias voltage $V_{bias\,1}$=V_{bias} at the gate of M_{C1} and M_{C2} which works very well in the low bias current medium, allowing the oscillation amplitude to be in large fraction of the main V_{DD} before transistor, M_{C1} and

M_{C2} are pushed towards linear region. However since this design adopts a static approach, hence it does not represent the ideal solution for achieving both robust and fast startup and low phase noise.

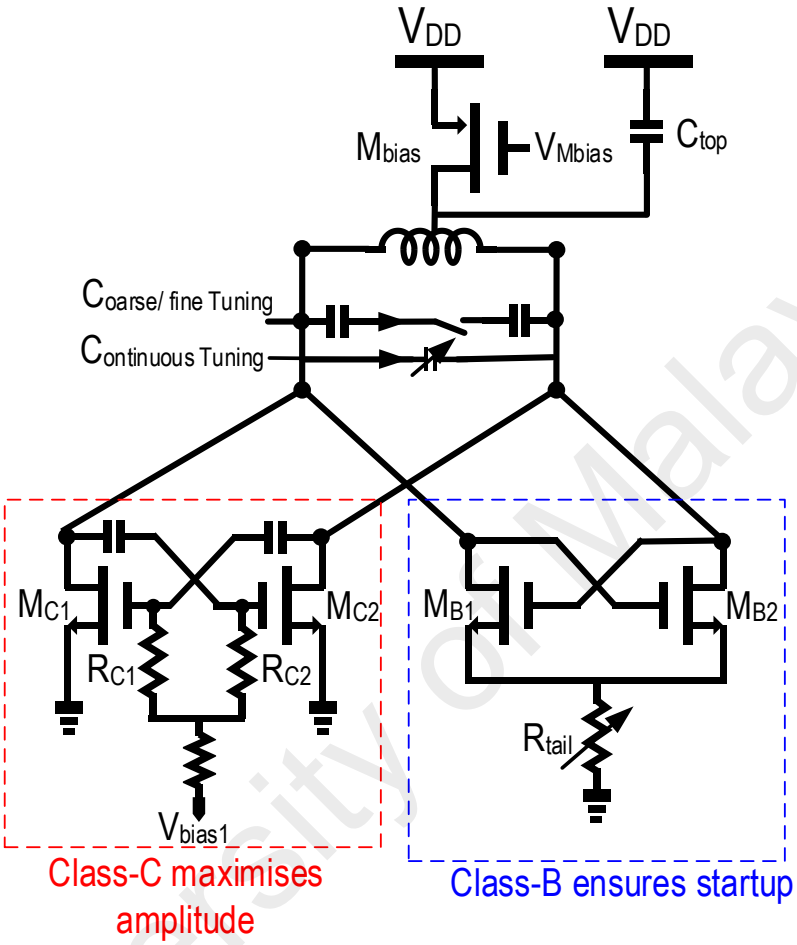

Figure 2.27: Hybrid class B/class-C oscillator.

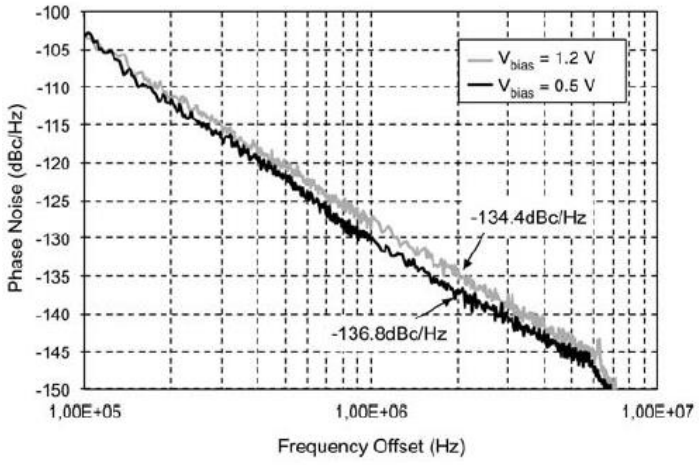

Figure 2.28: Phase noise measurements at mid band for $V_{bias\,1}$ = 1.2V (class B mode) and $V_{bias\,1}$ 0.5 V (Class-C mode)

(Fanori et al., 2012)

2.3.6.4 Class-B/Class-C Hybrid VCO in Oscillators

Class- C oscillators illustrate an attractive conversion architecture of Class-C from dynamic bias (Figure 2.29 (a) into hybrid architecture (Figure 2.29 (b) (Mazzanti & Andreani, 2008) ; (Fanori & Andreani, 2013a). that results in a better phase noise performance due to the active $-g_m$ devices of transistor, M_1 and M_2 of Class-C which prevails from entering into the triode region. This results in a better current conversion efficiency of the bias into fundamental harmonic current and the tank Q factor is preserved throughout the oscillation cycle. A 36% of power saving experienced from changing the drain current of a square wave to a tall and narrow pulse formation for Class-C mode. However, the challenge and prolong preservation of the transistors from entering the triode region limits towards achieving a maximum oscillation amplitude of the Class-C VCO to V_{DD}, for case when biasing voltage is at low threshold voltage of the active device. This concurrently translate to 6 and 3 dB phase noise and FoM of significant drop respectively. Performance comparison shown in Table 2.2.

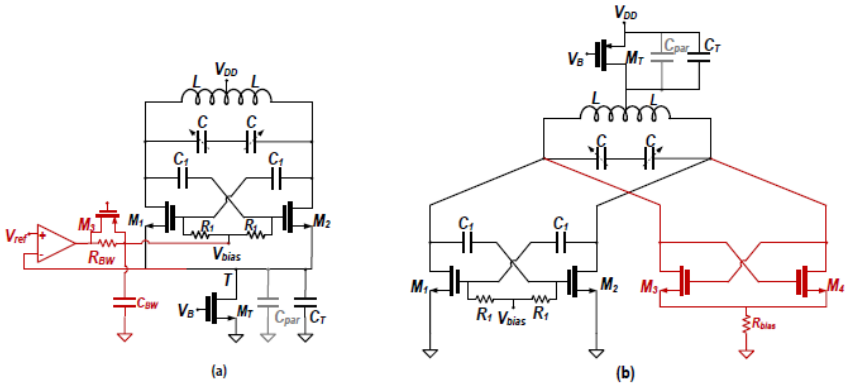

Figure 2.29: Class-C (a) with dynamic bias (b) hybrid Class-B /Class-C Oscillator

(Fanori & Andreani, 2013a).

Table 2.2: Performance summary of state-of-the-art of classes of VCO.

Oscillator Class (Reference)	Tech (nm)	V_{DD} (V)	P_{DC} (mW)	PN (dBc/Hz)	FoM (dBc/Hz)	f_{osc} (GHz)	FTR (%)
Takeuchi, Okada,& Matsuzawa, 2011	180	0.2	0.114	-102 @2MHz	-187	4.5	-
Deng, Okada, &Matsuzawa, 2013	180	1.2	3.4	-125	-193	4.84	-
Fanori,& Andreani, 2012	90	1.8	6.6	-147@ 10MHz	191	4.3	28
Fanori & Andreani, 2013c	65	0.4	7.0	-149.5 @10 MHz	190	4.0	15
Tohidian, Fotowat-Ahmadi, Kamarei, & Ndagijimana, 2011)	90	0.6	0.86	-127 @3MHz	192.3	5.1	-
Takeuchi et al., 2011	180	0.2	0.096	-102 @1MHz	187	5.4	-
Mazzanti & Andreani, 2013	180	1	2.16	-120 @2MHz	184		>10
(Fanori, Liscidini, & Andreani, 2012	55	1.5	27	-137 @2MHz	188	8.0	31

CHAPTER 3: PROPOSED COMPLEMENTARY CLASS-C DESIGN

3.1 Research Methodology on the Proposed Architecture

This research is carried out by benchmarking various reported literature review in analyzing various classes of VCO and their fundamental parameters. Numerous types of classes are compared with the advantages and disadvantages which been studied in detail to choose the most appropriate architecture. Current state of the art block are analyzed through detailed mathematical modelling and comparisons are made to identify the bottleneck that can be solved and further improvisation to be adopted.

Next, a basic VCO is analyzed followed by several derived architecture in appreciating their characteristic and the design process flow. The proposed architecture is designed constructively to preserve all challenging tradeoffs till the targeted specification are met. The initial designs procedure involve schematic level optimization enhancing the necessary performance parameter. Subsequently, physical layout verification is executed prior to the fabrication in CMOS 180nm technology process.

The fabricated VCO is physically validate at Collaborative Microelectronic Design Excellence Centre (CEDEC), Universiti Sains Malaysia using an on-chip probing technique. Upon full characterization, data are critically analyzed. Figure 3.1 shows the design flow for the proposed design.

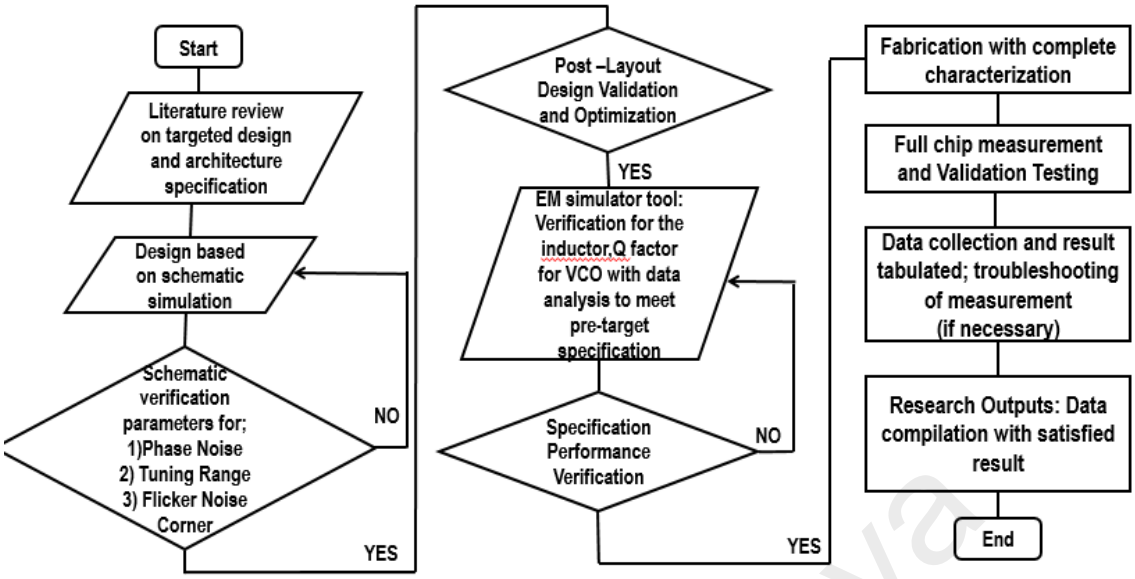

Figure 3.1 Design Process workflow

3.2 Circuit Operation

Figure 3.2 shows the proposed wideband complementary Class-C VCO architecture accommodated in parallel with the auxiliary class-B NMOS VCO only transistors, M_3 and M_4 as two sets of active VCO core working under the shared supply voltage, V_{DD} . The RC charging circuit, R_1C_1 and R_2C_2 connected at the active transistor's gates of the PMOS pair, M_1 and M_2 are biased at $V_{BIAS,P}$ to achieve saturation condition of $V_{DS,M1(M2)} < V_{BIAS,P} + |V_{th,P,M1(M2)}|$. The charger circuit, R_3C_4 and R_4C_3 which are connected at the gates of transistors M_5 and M_6 are biased at $V_{BIAS,N} \leq V_{th,N,M5(M6)}$ in subthreshold region which controls the dc power consumption of the entire VCO. The RC charging network time constant which satisfy the loop gain to sustain the oscillation is expressed as;

$$A_V \cdot R_p \parallel -\frac{g_m}{2} > 1 \tag{3.1}$$

where A_v is the loop gain approximated to 1 due to the absence of passive gain. The flicker noise, $1/f$ to PN up-conversion is prevented as the even-order harmonics are suppressed

significantly with the effect of a high impedance path along the biasing gate at $V_{BIAS,N}$. Therefore, a symmetric waveform is attained in the impulse sensitivity function (ISF), yielding to a zero dc value.

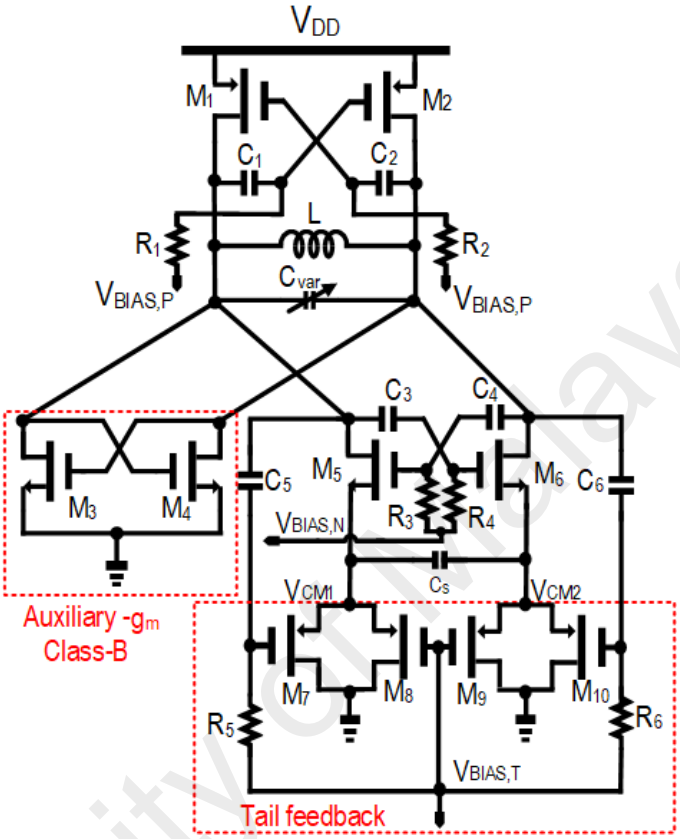

Figure 3.2: Schematic of the proposed architecture

The minimization of flicker noise is obtained from the advantage of the PMOS current source, M_7-M_{10} which stabilizes the bias condition at the source voltage ($V_{CM1}$and V_{CM2}) of the differential switching pair, M_5 and M_6 operating in the subthreshold region. High load impedance is observed in series with the switching pair, M_5 and M_6 (M_3 and M_4) which injects current noise perturbation into the resonant tank at the zero crossing point. The work in (Garampazzi et al., 2014) outlays a solution to remove the tail current source in alleviating the noise contribution or by substituting it with a tail resistor as reported in (Seok-Ju Yun, So-Bong Shin, Hyung-Chul Choi, & Sang-Gug Lee, 2005). This technique subjects the oscillator to be sensitive towards the supply voltage variation and driving the

differential switching pair active transistors into triode region. Therefore, it is preferred to retain and modify the tail current source in a way to serve minimum noise contribution. Figure 3.3 illustrates the block diagram of the circuit operation.

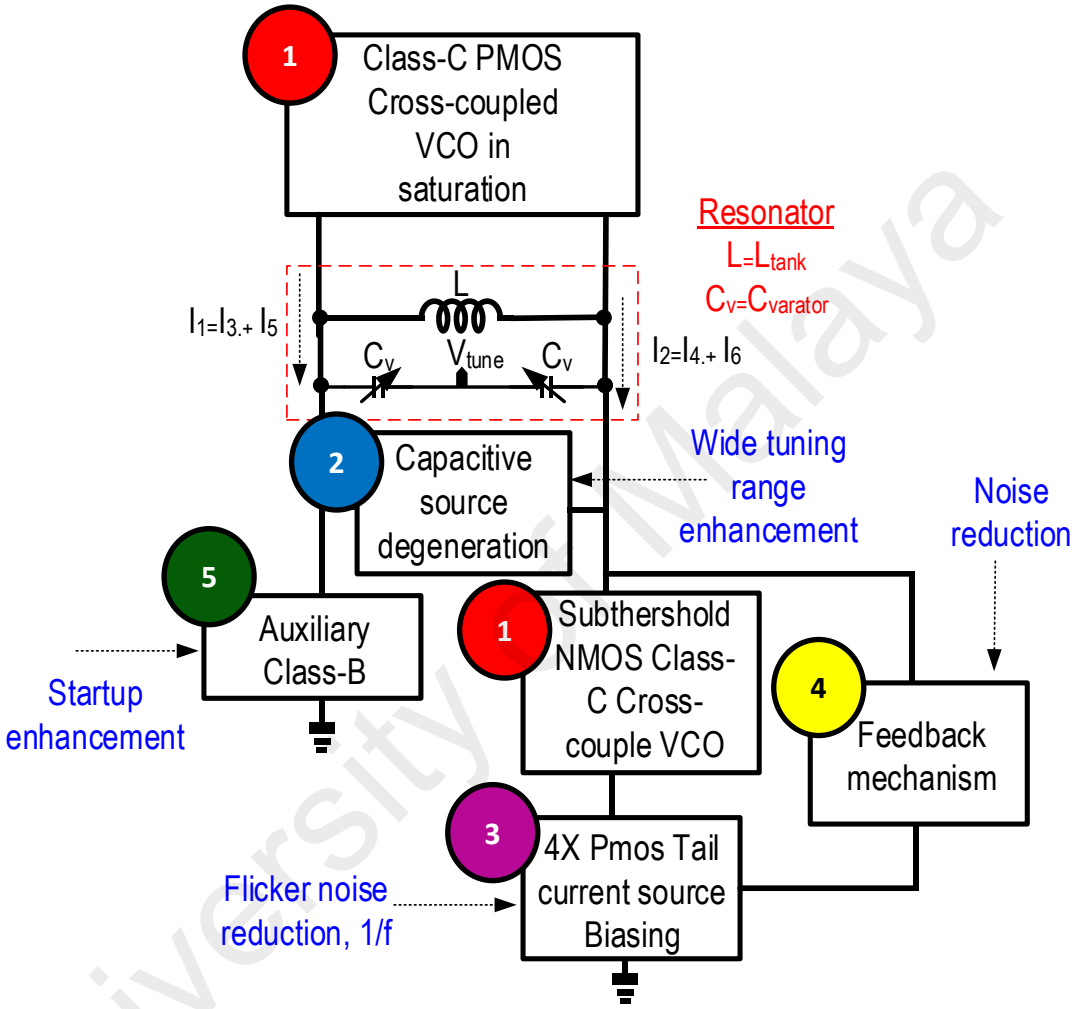

Figure 3.3: Block diagram of proposed architecture work

1 PMOS and NMOS cross-couple behaving as $-g_m$, cell which works as a negative resistance to cancel the parallel resistance, Rp losses from the LC resonator tank. $V_{BIAS,P}$ at the PMOS biased in saturation region whereas $V_{BIAS,N}$ at the NMOS biased in subthreshold region ensuring an overall low power consumption while achieving sufficient start-up and improve the current efficiency, thereby lowering the conduction angle.

2 Capacitive Source Degeneration, (CSD) reduces non-linear equivalent capacitance and increases negative resistance. This results in a tuning range of 28.6% over frequency bandwidth from 2.2 to 2.9 GHz under 1.73 mW power consumption from 1.2 V supply headroom.

3 PMOS Tail current source biasing bypass output noise via low impedance path.

4 Feedback Mechanism aided by the components R_5C_5 and R_6C_6 which provides a feedback path for driving the differential AC Signals. Helps to reduce the conduction angle and improve the current efficiency resulting in a lower phase noise.

5 Auxiliary Class-B VCO for sufficient trans-conductance, (extra -g_m) enough to ensure fast start-up and stability across all frequency range.

3.3 Capacitive Source Degeneration, (CSD) with 1/f Suppressing Effect

Conventional wide-band communication systems for multiple standards application adopts band-switching technique to achieve wide tuning range. This technique observes a penalty of an increase in circuit level and introduces switching loss, causing higher resistive sensitivity which degrades the Q of the circuit (Wei, Negra, Chang, & Chen, 2017). On lossy silicon substrate, the parasitic capacitances (C_{gs}, C_{gd}) of the cross coupled pair adjusted by varactor, C_{var} which tunes the oscillation resonant frequency for low frequency, (LF) band in (2.13) and high frequency, (HF) band in (3.2).

$$f_{osc,high} = \frac{1}{2\pi\sqrt{L.\left(\frac{2C_{var} + C_{gs} + 4C_{gd}}{2}\right)}} \tag{3.2}$$

Evidently, the parasitic capacitances are the limiting factor towards attaining a higher bandwidth given by the tuning range (TR) expressed as;

$$TR = \frac{C_{max} - C_P}{C_{min} - C_P} \tag{3.3}$$

where C_P is the sum of parasitic capacitance of the cross couple active MOS transistor and C_{max}/C_{min} refers to the tuning ratio of C_{var}. Hence, a tradeoff persist between a wide band operation and startup efficiency is apparent.

In LF band, the aspect ratio of the transistor are sized larger to increase the g_m to guarantee startup with a significant setback of parasitic effect; i.e., C_{gs} at high $V_{BIAS,N}$ (Narayanan, Kimura, Deng, Okada, & Matsuzawa, 2014). This is not feasible for HF as the size of the core needs to be minimized in order to widen the operating frequency range. Therefore, with the implementation of source degeneration capacitors, C_s as shown in Figure 3.4 (a), the equivalent parasitic capacitance can be reduced to achieve the desired frequency bandwidth.

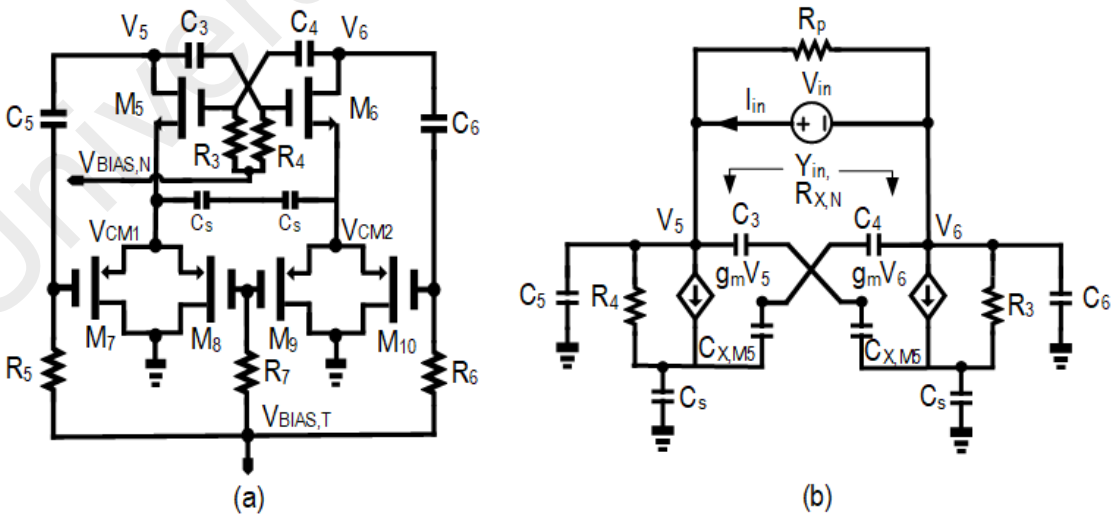

Figure 3.4: Class-C NMOS a) cross-coupling pair M_5 and M_6 with capacitive source degeneration, C_s and b) the equivalent circuit model.

Depending on the transition frequency of a signal, the parasitic capacitances and resistance need to be diligently sized concurrently to achieve a wideband operation with a small chip area. Considering a half circuit analysis as shown in Figure 3.4 (b), the parasitic capacitances of the NMOS class-C transistor, $C_{X,M5}$ lowers the capacitance tuning ratio and degrades the tuning range. The equivalent parasitic capacitance, $C_{X,M5}$ with the tank admittance, Y_P and the negative resistance, $-R$ of the NMOS class-C VCO consisting of $R_{X,N}$ are derived as;

$$C_{X,M5} = \frac{-\omega^2}{2}\left[4C_{gd} + C_{sb,M5} + C_{db,M5} + C_{gs,M5}\right] \tag{3.4}$$

$$Y_P = \frac{2}{j\omega L} + \frac{2}{R_p} + \frac{j\omega C_{var}}{2} \tag{3.5}$$

$$R_{X,N} = \frac{V_{in}}{I_{in}} = 2\left[\frac{1}{g_{d,M5}} - \frac{1}{g_{m,M5}}\right] \tag{3.6}$$

$g_{m,M5}$ is the trans-conductance of the transistor M_5 and C_s is the source degeneration capacitor. The input impedance, $Z_{in(j\omega)}$ is derived as;

$$Z_{in(j\omega)} = \frac{2}{j\omega\left(C_S + C_{X,M5}\right) - g_{m,M5}} \tag{3.7}$$

Therefore, by converting $Z_{in(j\omega)}$ to $Y_{in(j\omega)}$, the admittance of the transition frequency that contribute to achieve wide tuning range is given as (3.8).

$$Y_{in(j\omega)} = Re(Y_{in}) + jIm(Y_{in}) \tag{3.8}$$

$$= \frac{-\omega^2 C_s\left(2C_{X,M5} + C_s\right)g_{m,M5} + j\omega^2 C_s\left[-g_{m,M5}^2 - \omega^2\left(C_{X,M5} + C_s\right)\right]}{2\left[g_{m,M5}^2 + \omega^2\left(C_{X,M5} + C_s\right)^2\right]} \tag{3.9}$$

The parasitic of gate-to-drain, $(C_{gd,M5})$, source-to-bulk, $(C_{sb,M5})$ and drain-to-bulk, $(C_{db,M5})$ capacitance are neglected to simplify the transit frequency analysis. Hence, the equivalent resistance, R_{eq} and reactance, X_{eq} in (3.8) and (3.9) are attained as in (Wei et al., 2017), given as;

$$R_{eq} = -\frac{2C_{X,M5}}{g_{m,M5}\,C_s}\left[\frac{1+\left(\frac{\omega}{\omega_T}\right)^2\left(1+\frac{C_s}{C_{X,M5}}\right)^2}{\left(\frac{\omega}{\omega_T}\right)^2 2\left(1+\frac{C_s}{2C_{X,M5}}\right)^2}\right] \tag{3.10}$$

$$X_{eq} = \frac{2}{\omega^2}\left[\frac{1+\left(\frac{\omega}{\omega_T}\right)^2\left(1+\frac{C_s}{C_{X,M5}}\right)^2}{1-\left(\frac{\omega}{\omega_T}\right)^2 C_s\left(1+\frac{C_s}{C_{X,M5}}\right)^2}\right] \tag{3.11}$$

where $\omega_T = g_{m,M5}/C_{gs,M5}$ is the unity gain frequency and $\omega_{tran} = \left(g_{m,M5}/C_{gs,M5}\right)\left(C_{gs,M5}/C_{gs,M5}+C_s\right)^{1/2}$ is the transition frequency which determines the mobility (inductive to capacitive) of the impedance. As observed in (3.9), the transition frequency reduces when C_s increases adding into the denominator value and setting as $\omega^2\left(C_{X,M5}+C_s\right)^2 > g_{m,M5}^2$. Through this implementation, the negative resistance reduces. Therefore, the transistor size of M_5 and M_6 need to be sized diligently to reduce the feedback path effect (Figure 3.5) contributed by the parasitic capacitances at a large $V_{BIAS,N}$, thereby, reducing both $1/f^2$ and $1/f^3$ noises.

If C_s is sized optimally large, the VCO will be unstable leading towards squegging phenomenon which will deteriorate the PN performances and cause startup problem. This CSD technique solely reduces the nonlinear equivalent capacitance of $C_{X,M5}$ while increasing the negative resistance, $R_{X,N}$. A conventional VCO commonly utilizes a single current source of stacked NMOS transistor for the tail biasing. Therefore, by further splitting the tail current source transistors to an equal half, forms a lower amplitude of the

common mode voltages, V_{CM1} and V_{CM2} compared to the conventional architecture (Mostajeran, Bakhtiar, & Afshari, 2015)**,** benefiting from C_s. To sustain the VCO in class-C operation mode, the output voltage amplitude of the tank in the boundary condition of saturation and subthreshold (Mazzanti & Andreani, 2013) are expressed in (3.12) and (3.13), respectively as;

$$A_T < \frac{V_{DD} - |V_{BIAS,P}| - V_{th,P}}{2} \tag{3.12}$$

$$A_T < \frac{V_{BIAS,N} - V_{CM1/CM2} - V_{th,N}}{2} \tag{3.13}$$

A_T is the maximum voltage amplitude, $V_{BIAS,N}$ is the gate bias voltage of the NMOS Class-C cross-coupled pairs of M_5 and M_6 , V_{th} , threshold voltage and V_{DD} is the drain supply voltage. Referring to (3.12) and (3.13), the overall maximum tank voltage swing attained without transistors driven into triode region expressed as;

$$A_T < \frac{V_{DD} + |V_{BIAS,P} - V_{th,P}| + |V_{BIAS,N} - V_{th,N}| - V_{CM1/CM2}}{2} \tag{3.14}$$

Therefore the PN of the class-C VCO is expressed in (3.15) respective to the overall value of A_T and R_P $\left({Y_p}^{-1}\right)$ given in equation (3.14) and (3.5), respectively;

$$L(\Delta\omega) = 10\ log\left[\frac{k_B T(1+\gamma)R_p}{NQ^2A_T^2}\frac{\omega^2}{\Delta\omega^2}\right] \tag{3.15}$$

N is the number of resonators (*N*=1 for single ended and *N*=2 for differential oscillator with a single LC tank) (Babaie & Staszewski, 2013), k_B is the Boltzmann's constant, T is the absolute temperature, γ is the MOS channel noise factor and R_P is the parallel tank impedance. The conduction angle becomes narrower as both PMOS pair (M_1 and M_2) and NMOS pair (M_5 and M_6) acquire different transistor gain operating in different gate voltage biasing condition at the saturation and subthreshold point of $V_{BIAS,P}$ and $V_{BIAS,N}$,

respectively. The aspect ratio of PMOS-NMOS gain can be adjusted to achieve an equilibrium gain and achieve fast startup.

3.4 Low Noise and Low Power Contribution in Subthreshold Conduction

Figure 3.6 shows the low-power complementary class-C circuit operating under subthreshold region adopting PMOS transistors as the MOS current source. The operation yields a higher trans-conductance to power dissipation ratio which results in a decent noise performance. A substantial low impedance path of resistance to ground is formed at V_{CM1} and V_{CM2} which bypasses the output noise, thus improving the effective ISF (Mostajeran et al., 2015). Furthermore, the components of R_5C_5 and R_6C_6 provide a feedback path for driving the AC signals, $+f_{LO}$ $(-f_{LO})$ from the output to the respective gates of the PMOS tail current source, M_7-M_{10}. The feedback components are sized adequately to be insensitive towards PN and to achieve die area optimization.

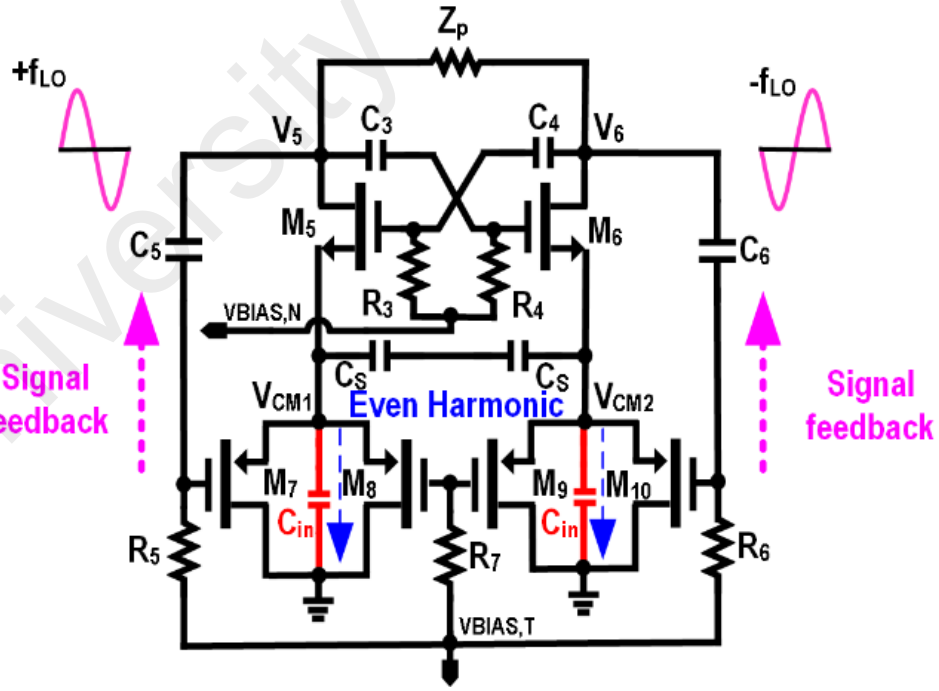

Figure 3.5: Subthreshold conduction with PMOS split current source.

Subsequently, the intrinsic parasitic capacitance, C_{in} exist between each split tail current source pair suppresses the even order second harmonic ($2f_{LO}$) from the common mode nodes (V_{CM1} and V_{CM2}), improving the phase noise, (PN) performance. V_{CM1} and V_{CM2} in (3.14) adjust the threshold voltage of the differential class-C NMOS transistors results in a higher headroom for larger output voltage swing. Furthermore, the dc bias point, $V_{BIAS,T}$ favor towards the subthreshold biasing condition, $V_{GS} \approx V_{BIAS,T} \leq V_{th}$ improving the current efficiency simultaneously with an adequate active subthreshold MOS negative conductance, g_{sub} of the complementary class-C VCO, expressed as;

$$g_{sub} = \frac{-\mathrm{g}_{m5}}{2} = \frac{I_{DS \cdot q}}{nk_B T} \tag{3.16}$$

g_{sub} of a class-C VCO in subthreshold region is computed from the subthreshold drain current, I_{DS} and is exponentially related to the gate voltage(V_G), source voltage (V_S) and drain voltage(V_D) of the NMOS transistor, M_5 and M_6 expressed as ;

$$I_{DS,M5(M6)} = I_0 e^{\frac{V_G}{nU_T}} \left(e^{\frac{V_S}{U_T}} - e^{\frac{V_D}{U_T}} \right) \tag{3.17}$$

in which subthreshold drain current, I_0 is defined as;

$$I_o = 2n\mu_e C_{ox} \frac{W_e}{L_e} U_T^2 e^{\frac{-V_{th}}{nU_T}} \tag{3.18}$$

q is the electronic charge, k_B is the Boltzmann's constant, T is the absolute temperature and n is the subthreshold slop factor dependent to process parameters and bias conditions denoted as $n = 1 + C_{dep}/C_{ox}$. The capacitors C_{dep} and C_{ox} are the surface depletion capacitor and gate oxide capacitor, respectively. It is evident from (3.16) with a low bias $\left(V_{GS} \approx V_{BIAS,N}\right)$, the efficiency denoted by $\eta = P_{RF}/P_{DC}$ improves linearly which contributes towards a negligible amount of noise. The effective aspect ratio of M_5 and

M_6 are adequately sized to improve I_0 . The parameter μ_e is an effective carrier mobility in channel and $U_T = kT/q$ is the thermodynamic voltage. The output negative trans-conductance, G_{neg} at the output node voltage, V_5 is derived as;

$$G_{neg} = -\frac{g_m + j\omega\left(C_{gs,M2} + C_s + C_{ds,M5}\right)}{2} \tag{3.19}$$

$$\sum R_{eq} = \left[\frac{-2}{g_m + j\omega\left(C_{gs,M2} + C_s + C_{ds,M5}\right)}\right] \parallel R_p \tag{3.20}$$

Therefore, the output voltage under subthreshold bias condition in (3.16) and (3.17) reduces to as;

$$V_5 = \left(R_{eq}\right) \cdot I_0 e^{\frac{V_G}{nU_T}} \left(e^{\frac{V_S}{U_T}} - e^{\frac{V_D}{U_T}}\right) \tag{3.21}$$

3.5 Phase Noise

PN degradation via $1/f^2$and $1/f^3$upconversion are mainly contributed by the active noise sources in the oscillator. However, with subthreshold biasing and substitution of PMOS device as tail transistors, the respective tail noise has dual path flow which is through M_5 and M_6 and back to the signal output shown in Figure 3.6. Alternately, the second pathway is via M_7 and M_8 (M_9 and M_{10}) to ground. A low impedance path seen from the each source of M_5 and M_6 attracts considerably the tail noises as compared to the drain of M_7 and M_8 (M_9 and M_{10}). In reference to (Mostajeran et al., 2015), the effective ISF, $\Gamma_{tail,eff}$ becomes smaller in amplitude since low injection of the tail noise flows to the output leading towards phase insensitivity at the tail transistors.

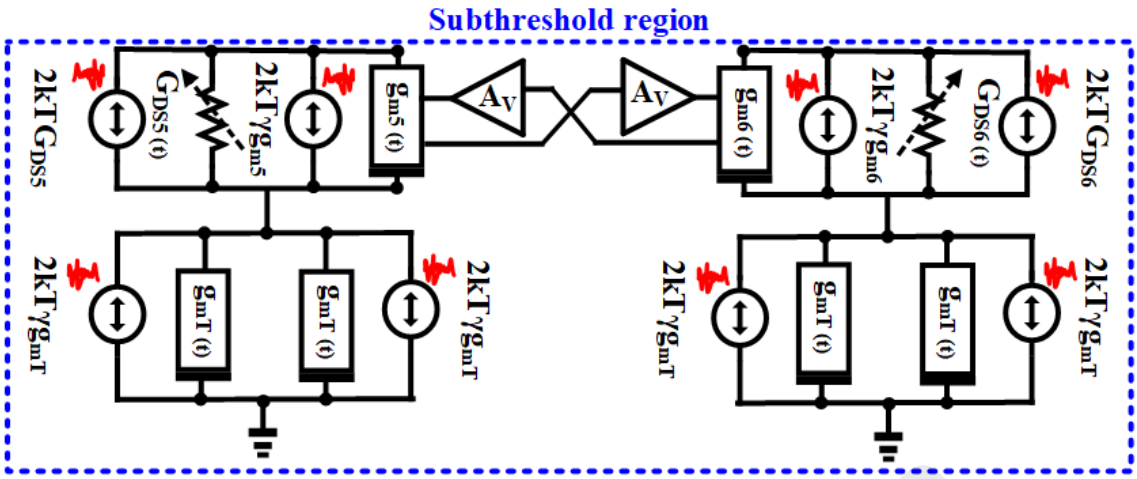

Figure 3.6: Noise sources model of the proposed subthreshold circuit.

The smaller $\Gamma_{tail,eff}$ brings an advantage of a lower amplitude in the second order harmonic current noise or negligible with the presence of the low common mode oscillation point, V_{CM1} and V_{CM2} . In weak inversion region, the presence of shot noise and drain current noise of the PMOS (NMOS) directly proportional to the gate voltage, $V_{BIAS,T}$ that are shared within the transistors. Figure 3.6 illustrates a simplified model of the noise sources of the proposed subthreshold architecture classifying the noise contribution from the NMOS cross-couple transconductance and PMOS current biasing transistors. Noise model where $g_{m5(m6)}(t)$ and $G_{DS\,5(6)}(t)$ represent the trans-conductance and channel conductance of transistor M_5 and M_6 respectively. Apart from it, g_{mT} is the transconductance of PMOS current source transistor for M_7 and M_8 (M_9 and M_{10}).

The equation (3.22) expresses the weak inversion mode drain noise current in the subthreshold region of transistor M_5 and M_6;

$$\overline{I_{nd}^{2+}} = \frac{4kTC_{ox}\rho}{f} + 2qI_{DS} \qquad (3.22)$$

where $k_f = 4kTC_{ox}\rho$ is the empirical coefficient and I_{DS} is the net drain current. In comparison to the superthreshold regime in proposed in (Lee & Mohammadi, 2007), the effective thermal noises, $\overline{I_{nd}^{2+}}/\Delta f = 4kT\gamma g_m$ are still comparable with the shot noise in weak inversion mode. Equation (3.22) proves that the shot noise dominates the white noise present in the MOS transistors as the carriers generate the dc current flow through diffusion mechanism at the source channel barrier crossings (Fathi & Nejad, 2013)**.** Moreover, as this region accommodates PMOS transistors, a reduction in power consumption and a high potential of trans-conductance to the bias current is observed. The PMOS current source transistors are linearly dependent on the bias condition, $V_{BIAS,T}$ while the $1/f$ up-conversion subsequently reduced by increasing the device dimension as expressed as;

$$\gamma = \frac{2n_1}{3 + \left(\frac{g_m}{I_{DS}} n_1 U_T\right)} \tag{3.23}$$

γ is the correction factor, U_T denotes the thermodynamic voltage and n_1 is the slope factor. Therefore the noise current for the M_5 and M_6 in the subthreshold region is given as;

$$\frac{\overline{I_{nd}^{2+}}}{\Delta f} = 2kTqg_m \tag{3.24}$$

where q is the electron charge. Hence, the output noise voltages reduced as computed under this region comprises a half circuit analysis as ;

$$\overline{V_{n,M5(M6)}^2} = 2kT\left(1 + \frac{g_m}{g_{mb}}\right)\left[\frac{Y_P^2 + G_m^2}{(Y_P^2 - G_m^2)^2}\right]\Delta f \tag{3.25}$$

where the G_m is the conductance of M_5 and Y_P^2 is the squaring tank admittance equated in (3.5) .

3.6 Device Under Test configuration and method placement.

The setup for the Device Under Test, (DUT) is arranged as shown in Figure 3.7. The power supply, V_{DD} are supplied from the parameter analyzer directly to Device Under Test, DUT .The sinusoidal output signal are measured using Agilent Infiniium DS081004B oscilloscope. The span and resolution of the oscilloscope and signal source analyzer are set appropriately for the ease of the measurement. This test configuration that were used to measure the block labeled as "DUT" in which the testing chip is placed at the near the probe tip platform using G-S-G-S-G configuration shown in Figure 3.8. Table 3.1 shows the targeted VCO architecture specification needed to achieve.

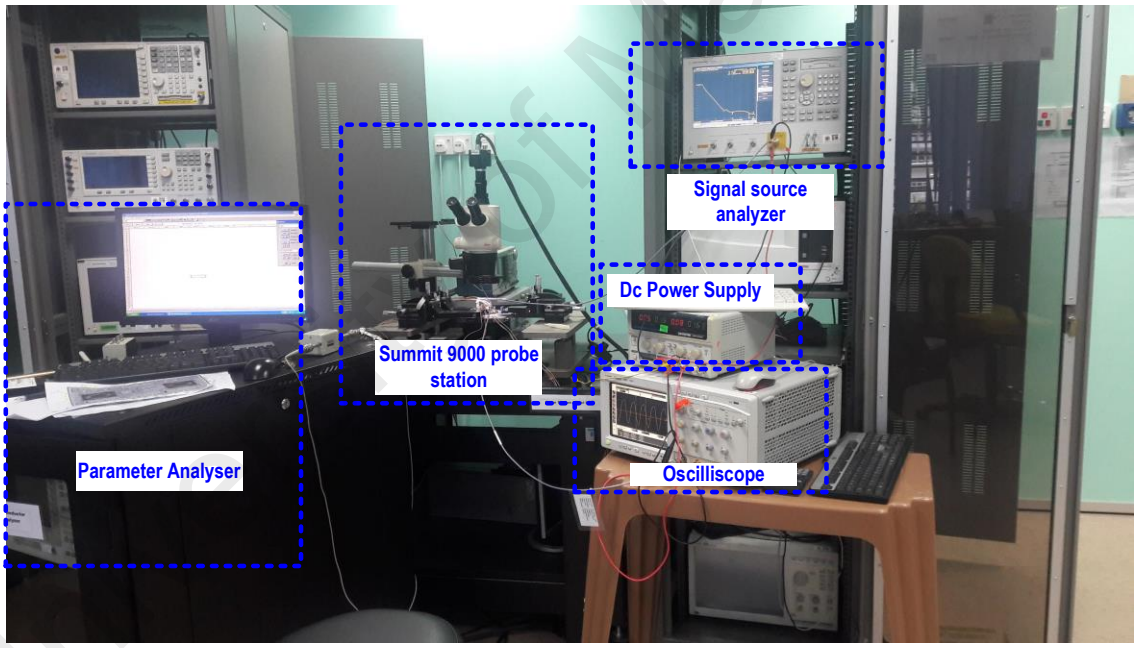

Figure 3.7: Measurement set up

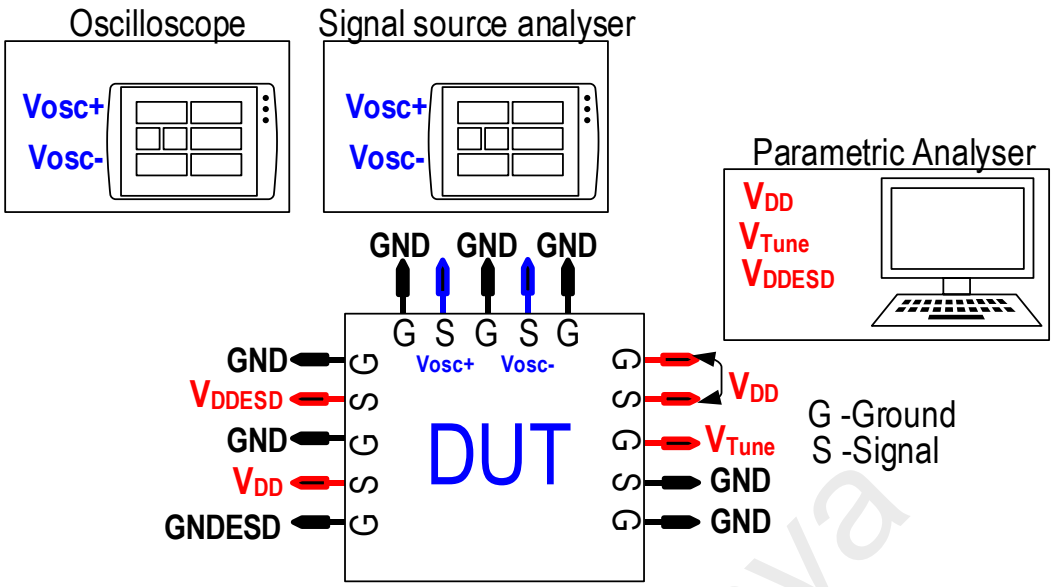

Figure 3.8: Block diagram of the test setup configuration for this measurement

Table 3.1: VCO Design Specification Performance

VCO DESIGN SPECIFICATION PERFORMANCE	
Performance	**CMOS VCO**
Submicron Technology,nm	**180**
Voltage Supply,V	**<1.8**
Operating Frequency,GHz	**2.45**
Phase Noise, dBc/Hz @1 MHz	**<-119**
Figure of Merit, FoM ,dBc/Hz	**>180**
Tuning Range, %	**>20**
Flicker Noise Corner, MHz	**<300**
Signal Power, dBm	**> 0**
Q factor	**>10**

CHAPTER 4: SIMULATION RESULT

4.1 Introduction

This chapter focuses on the post layout simulation results for all the individual proposed blocks.

4.2 Post-Layout simulation results

The proposed design of the complementary class-C oscillator with tail current source feedback and noise suppression for wireless applications was realized on 180nm CMOS technology platform and simulated using Cadence Spectre-RF simulator. The physical layout is realized with Cadence Layout Editor followed by the RC Parasitic extraction using Calibre Platform. In of the following section, the performances of the individual blocks are presented and further discussed. Since, the nonlinearity introduced from the implementation of RF transistors, they are substantially sensitive towards Process, Voltage and Temperature, (PVT) variation. In the layout design, internally an additional dummy poly are added to ensure a more symmetrical flow of current and to save guard the device from suffering any mismatches during the fabrication process. Metal-Insulated Metal (MIM) capacitors are utilized rather than Metal –Oxide –Metal, MOM capacitors due to the low losses level. The metal routings need to be diligently done by using the highest metal level for the critical path of supply and signal. Therefore, several level of verification and constant optimization required in the layout design in order to achieve high accuracy level of the performance parameters during the measurement process.

4.2.1 Capacitive Source Degeneration, (CSD) results

Figure. 4.1 shows the simulated nonlinear equivalent capacitance of $C_{X,M5}$ and the negative resistance $R_{X,M5}$ with different value of C_S. For $C_{X,M5} < 0.03$ pF, the range of C_s falls between 0.38 pF to 0.8 pF. For simplicity, a particularly nonlinear gate to source capacitance, $C_{gs,M5}$ is taken into account as it brings significant effect towards the change in the instantaneous transit frequency expressed in (3.12) and (3.13). A well balanced and lower value point (sweet spot) is attained in the defined range with suitable value of C_s favoring towards the tuning of the varactor and benefitting the wide tuning range. In Figure 4.2, in the chosen value of C_s at the range of 0.2-0.8 pF, the negative resistance shows an increasing value and reaches constant favorably towards adequate startup. At C_s goes beyond 0.48pF, the negative resistance experiences a continuous increment, providing a high gain thus eliminating the impact of the extra buffer stage which brings parasitic effect to the LC tank. Figure 4.3 shows that utilizing a varactor replacing Cs degrades the phase noise of the VCO, due to the reduction of the quality factor, Q in the LC tank circuit.

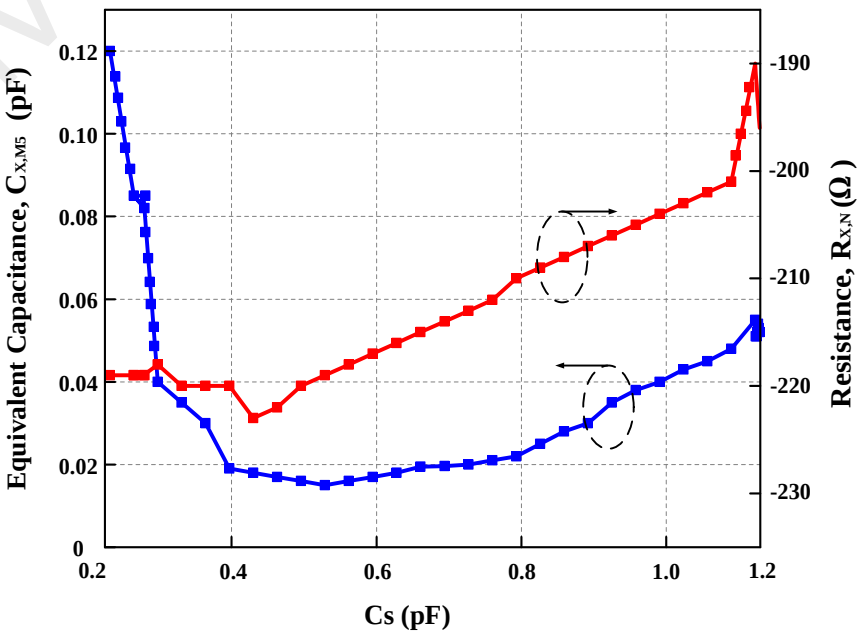

Figure 4.1: Simulated equivalent capacitance, $C_{X,M5}$in subthreshold conduction with different values of source – degeneration capacitance, C_s

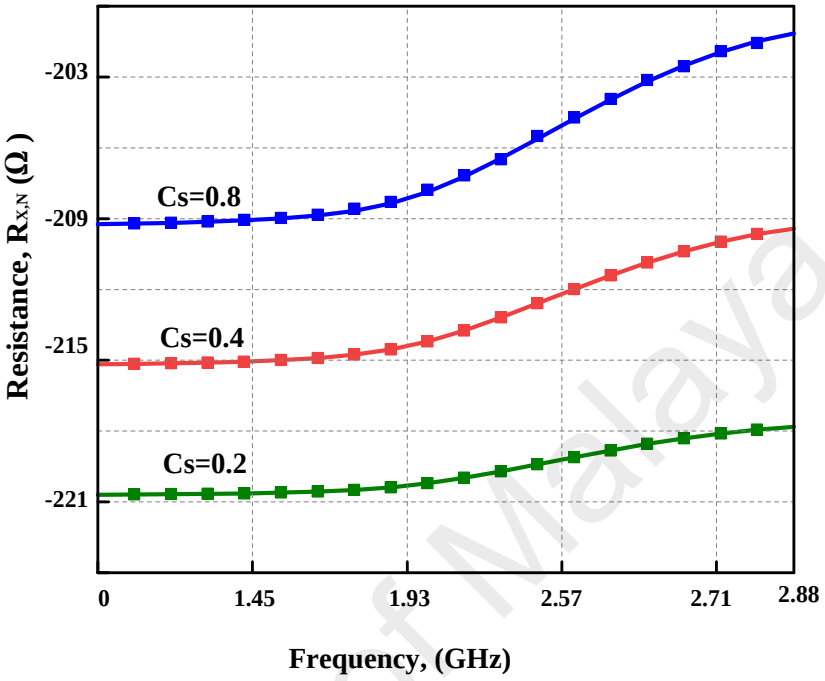

Figure 4.2: Simulated large-signal negative resistance, $R_{X,N}$ in subthreshold conduction under wide tuning range with different values of source – degeneration capacitance, $\boldsymbol{C_s}$in particular value of 0.2,0.4 and 0.8 pF.

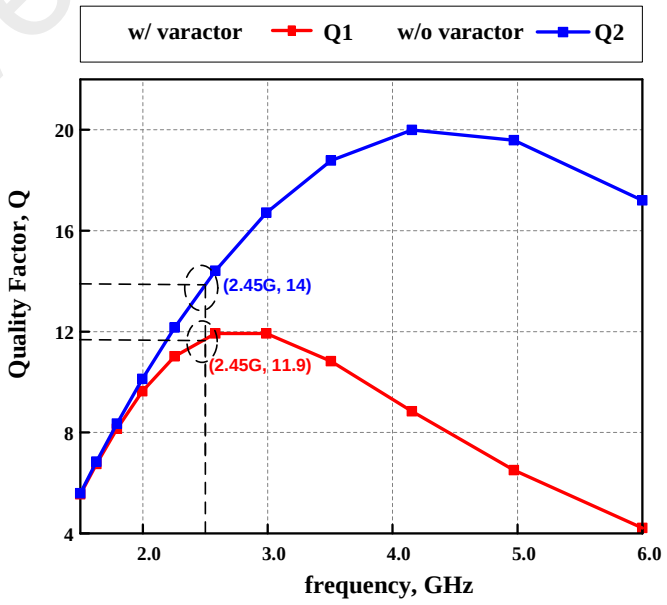

Figure 4.3: Simulated Q factor effect towards varactor replacement as CSD.

4.2.2 High Output Swing with Current Source Feedback.

Figure 4.4 illustrates the simulated differential output voltage swing at steady state with $V_{BIAS,N}$ biasing at M_5 and M_6 to operate in subthreshold region. This results in a large voltage swing which lowers the current commutation time, improving the effective ISF waveform shown in Figure 4.5.

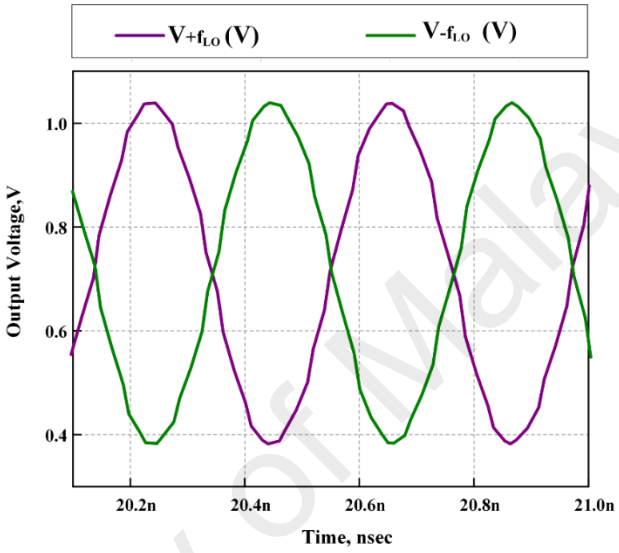

Figure 4.4: Simulated differential output voltage swing.

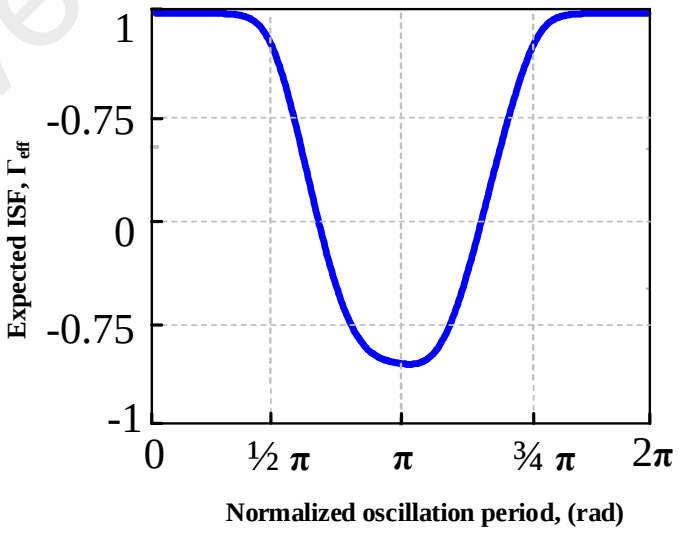

Figure 4.5: Estimated simulated effective ISF..

When commutation time reduced, the switching losses and harmonics level of the transistors also becomes lower favoring towards a more satisfied phase noise performance. Alternatively, Figure 4.6 shows the asymmetric oscillation of the simulated transient voltage waveforms of the drain voltage, $V_{DS,M5(M6)}$ and gate voltage, $V_{GS,M5(M6)}$ of M_5 and M_6. Point A and B shows the $1/f$ flicker noise up-conversion into the $1/f^3$ close in phase noise region. When the gate voltage, $V_{GS,M5(M6)}$ and drain voltage,$V_{DS,M5(M6)}$ are same, the VCO will be more sensitive to the injected noise, thereby resulting in zero crossing point differ in between this two operating voltages. Without the tail feedback with external biasing, the cross-coupled transistor are subjected into triode region, generating a significant amount of noise, causing an amplitude distortion as shown in point C. Figure 4.7 shows a more balanced symmetric waveform attained with the advantage of the tail feedback and aided through the symmetrical auxiliary $-g_m$ class-B oscillator under low power operation.

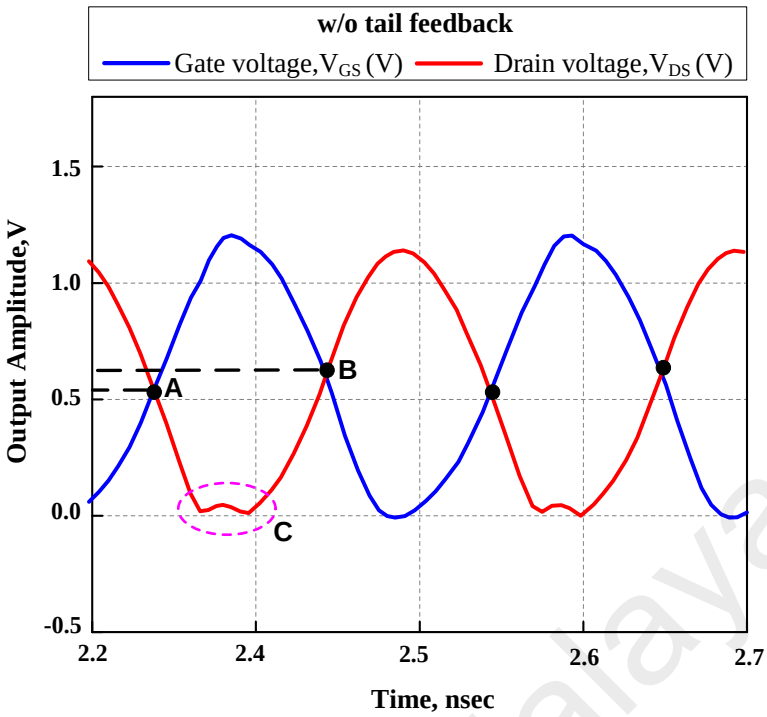

Figure 4.6: Simulated gate and drain voltage without tail feedback.

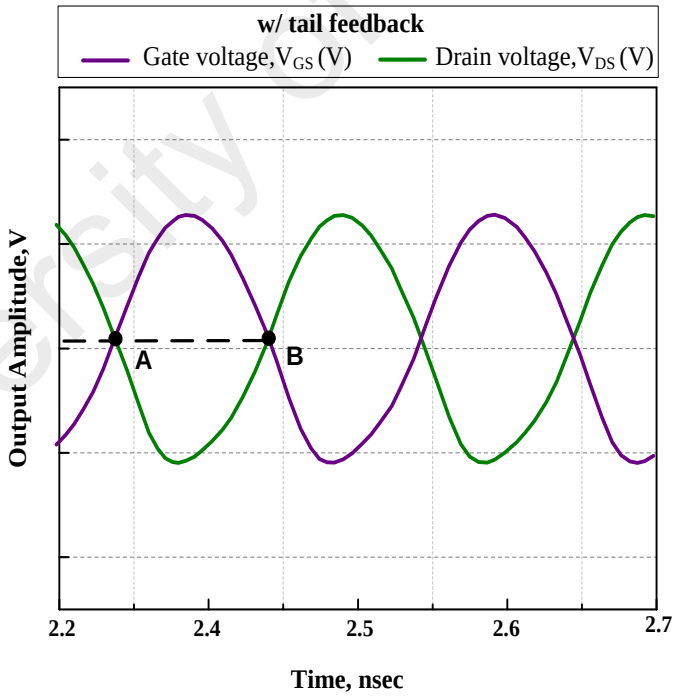

Figure 4.7: Simulated gate and drain voltage with tail feedback.

4.2.3 Simulated Phase Noise with and without Tail Current Source Feedback

The PN performance with and without the tail feedback is shown in Figure 4.8 where at 1 MHz offset, the proposed architecture demonstrates approximately 14 dB of phase noise,(PN) improvement compared to the conventional Class-C oscillator (Fanori & Andreani, 2013a) operating at the same 2.45 GHz oscillation frequency.

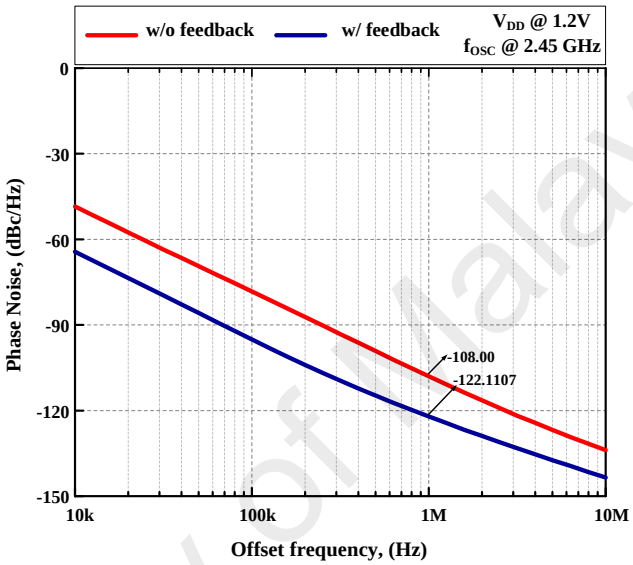

Figure 4.8: Simulated phase noise with and without tail feedback.

4.2.4 Proposed Oscillator Startup Result

Figure 4.9 explains on the startup time across steady state accommodated by the auxiliary Class-B M_3 and M_4 nMOS transistor. The startup is 2.0 ns when $V_{BIAS,N} = 0.35V$ is fixed at the gate of the cross-coupled transistor, M_5 and M_6 under the voltage supply headroom, V_{DD} of 1.2V. The output drain voltages of transistor, M_3 and M_4 yield 600mV peak to peak producing high voltage efficiency compared to conventional complementary architecture in (Amin et al., 2015). Figure 4.10 depicts the simulated drain current at $V_{BIAS,N}$ near the transistor threshold voltage value which is shown to secure sufficient gain while ensuring an appropriate startup with the oscillation swing being enhanced. The current efficiency improves beyond >60% in the effect of a narrower

conduction angle of 0.31π with better phase noise, (PN) performance since three biasing point ($V_{BIAS,P,}$ $V_{BIAS,N}$, $V_{BIAS,T}$) are adopted. The drain current achieve a tall and narrow pulse working under Class-C mode.

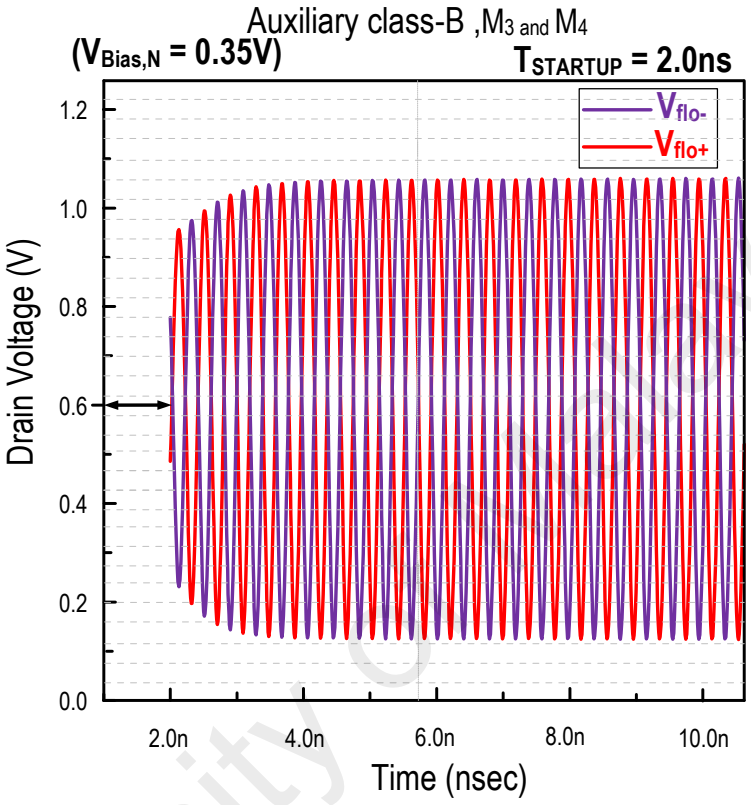

Figure 4.9: Startup time of the proposed circuit

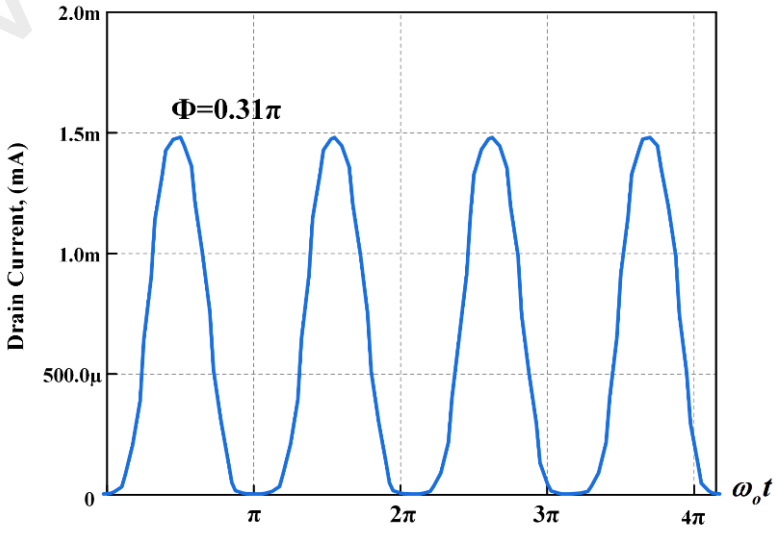

Figure 4.10: Simulated drain current of the proposed circuit.

4.2.5 Device Corner analysis

The corner analysis procedure are done in the post layout verification stage to test the proposed design robustness and to validate its sensitivity and reliability under different corner process during fabrication. Three corners which are tested Fast, Fast (FF), Typical,Typical, (TT) and Slow,Slow, (SS). Table 4.1 shows the phase noise performance towards these variations under standard room temperature of 27°C. These corner analysis are simulated with the current changes of 0.2 mA drop at Slow,Slow, (SS) corner and 0.2mA above for Fast,Fast, (FF) corner according to the built in Bsim 3v3 model of the pdk.

Table 4.1: Process corner analysis

Process Corner at Vdd=1.2, Vtune=0.6	**Slow, SS**	**Typical, TT**	**Fast, FF**
PN (dBc/Hz) @ 1MHz offset	**-114.85**	**-119.0**	**-120.0**
Signal Power, (dBm)	**<3**	**>3**	**>3**
F (GHz)	**2.27**	**2.39**	**2.45**

4.2.6 Ambient Temperature analysis

Figure 4.11 and Figure 4.12 shows the effect of the power consumption, (P_{DC}), phase noise (PN), frequency, (GHz) and output power (dBm) towards the effect of ambient temperature particularly at 20°C to 22 °C under the range of [-20,100] temperature variation. These parameters shows a minimal degradation effect benefited from the PMOS tail current source feedback operated under the subthreshold conduction. Under this operation, the trans-conductance, g_m is higher aided with the auxiliary class-B VCO resulting in an overall low power, low phase noise and fast startup throughout the temperature.

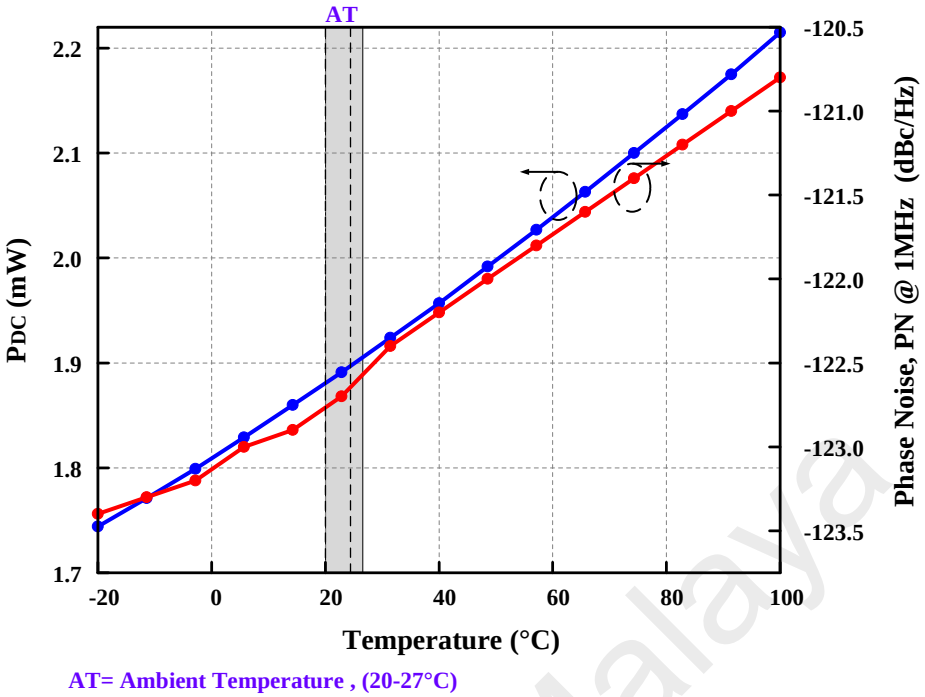

Figure 4.11: Simulated power consumption, $P_{DC,}$(mW) and phase noise, PN over ambient temperature, (°C)

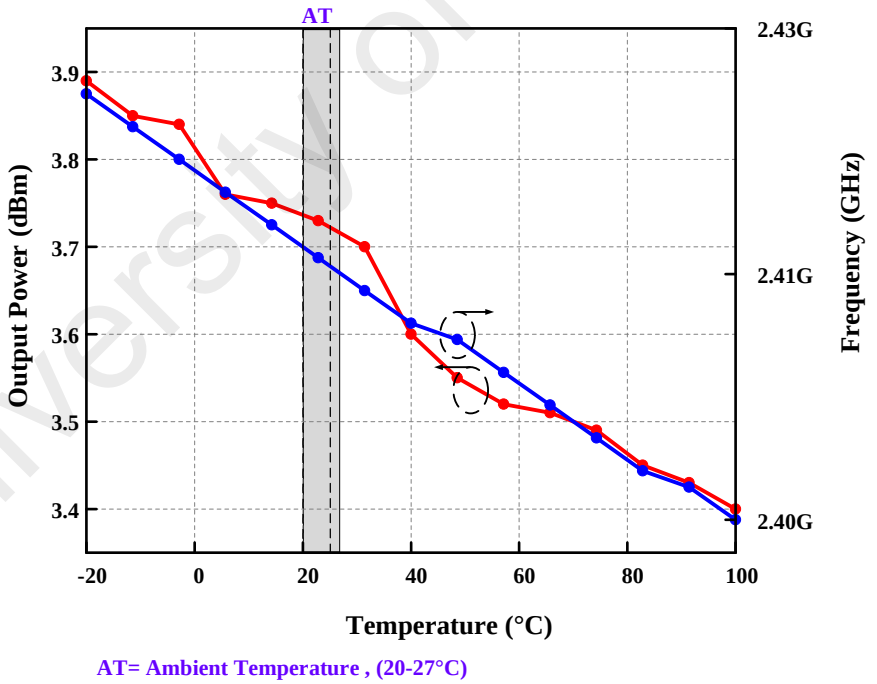

Figure 4.12: Simulated output power,(dBm) and frequency, (GHz) over ambient temperature, (°C).

CHAPTER 5: MEASUREMENT RESULT

5.1 Introduction

This chapter focuses on the post layout simulation results for all the individual proposed blocks. This is followed with the measurement results for entire circuitry.

5.2 Measurement results

The layout done were fabricated under Silterra 180 nm CMOS technology and done under on wafer probing platform and Figure 5.1 shows the pictomicrograph of the fabricated design which occupies of only 0.3 mm^2 of active silicon area and consumes an average core power of 1.73mW under 1.2 V supply voltage headroom. All of the measured result were collected from the on wafer probing measurement instrument using the Probe station Summit 9000 from Cascade Microtech shown in Figure 5.2.

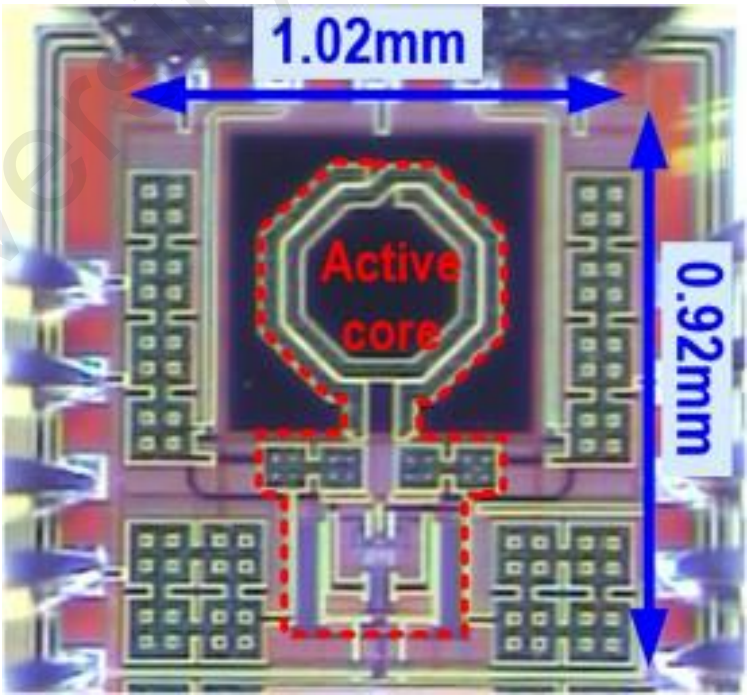

Figure 5.1: Photomicrograph of fabricated proposed oscillator

Figure 5.2: Summit 9000 Probe station from Cascade Microtech

Before performing a measurement test, the instrumentation are properly calibrated to exclude the cable insertion losses and are set up in a standard 50 Ω environment. The measurement of the insertion losses is very crucial as to compute the tolerance level and acquired an actual VCO's output signal power. Several test cases adopted to measure the reliability of the design as follows;

a) Frequency pushing
b) Output power and frequency
c) Harmonics and spurious level

5.2.1 Frequency pushing

The proposed designed are measured under on-wafer probing, where the measured PN at f_{MIN} is 2.2 GHz and f_{MAX} is 2.9 GHz are shown in Figure 5.3, 5.4, and 5.5 under the supply variation of 1.1 V, 1.2 V and 1.3 V respectively. The frequency tuning range, FTR achieved is 28.6 % across the 2.2 to 2.9 GHz bandwidth. The supply pushing method are also tested with the difference of ± 0.1 V from the power supply to test the device response

towards the power supply variation in the case for real life application of battery diminution across time .Table 5.1 shows the effect of phase noise when voltage supply is reduced or increase 0.1 V of their V_{DD} in post layout and measured comparison.

Table 5.1: Frequency pushing table for oscillator under supply voltage variation

VDD (V)	1.1		1.2		1.3	
PN (dBc/Hz) @ 1MHz offset	**Post Sim.**	**Meas.**	**Post Sim.**	**Meas.**	**Post Sim.**	**Meas.**
Fmin (GHz)= 2.2 GHz	**-121.73**	**-119.3**	**-122.9**	**-120**	**-123.60**	**-120.27**
Fmax (GHz)= 2.9 GHz	**-120.78**	**-117.2**	**-120.1**	**-118.9**	**-121.62**	**-119.5**

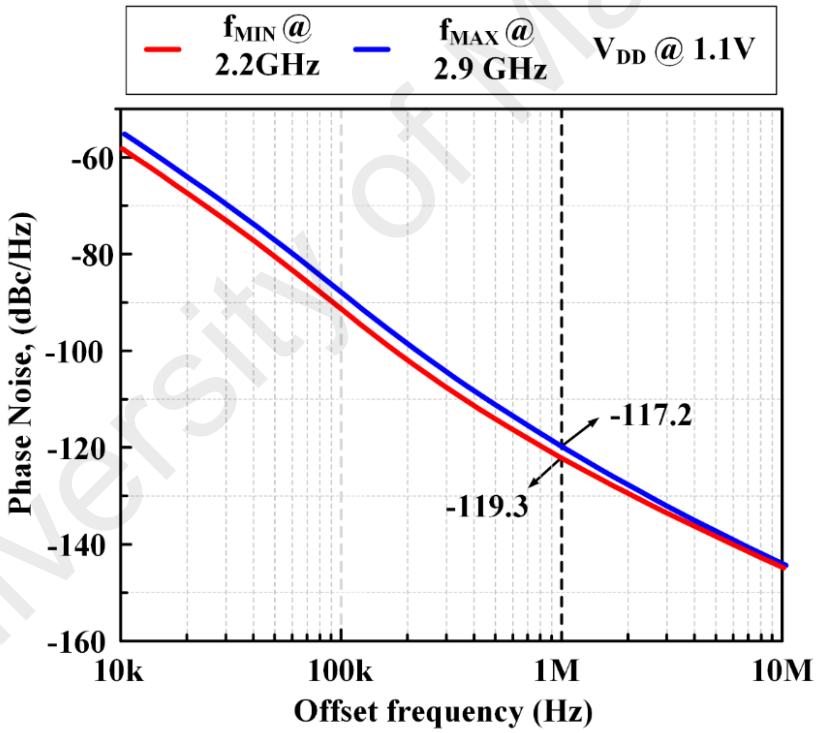

Figure 5.3: Measured phase noise against offset frequency when the V_{DD} is reduce to 1.1V

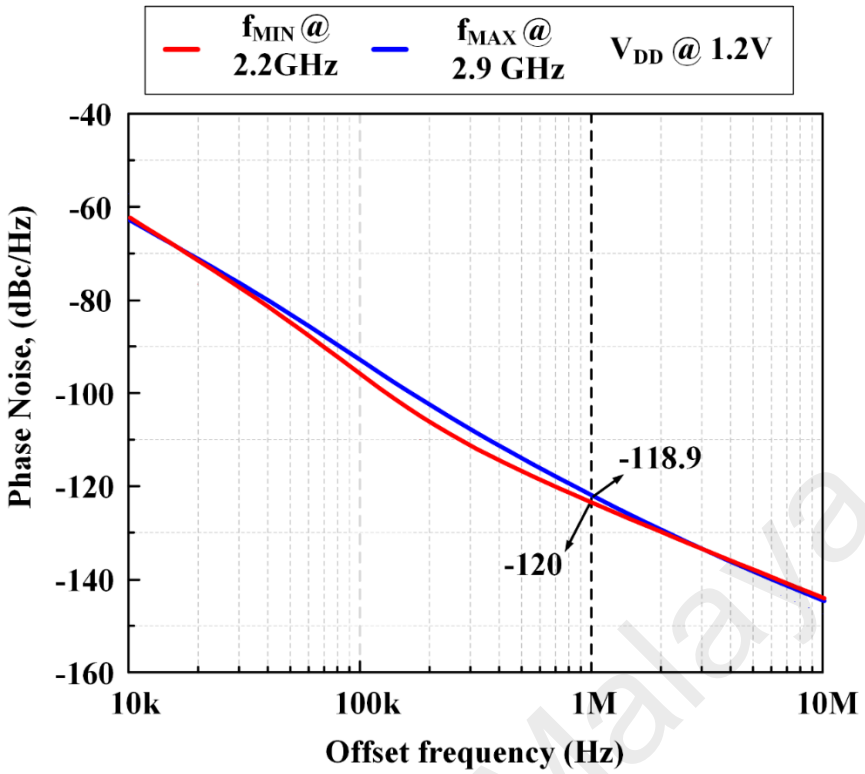

Figure 5.4: Measured phase noise against offset frequency when the V_{DD} is reduce to 1.2 V

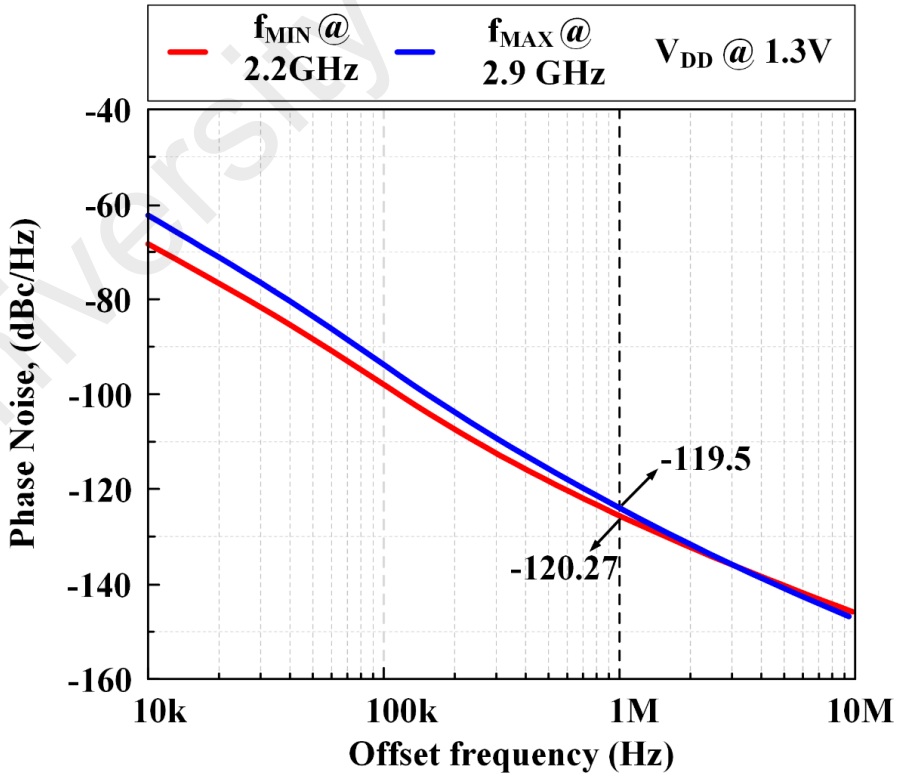

Figure 5.5: Measured phase noise against offset frequency when the V_{DD} is reduce to 1.3V

5.2.2 Output Power and Frequency

Figure 5.6 shows the measured output power of frequency, at f_{MIN} = 2.2 GHz and f_{MAX} = 2.9 GHz when the tuning voltage, V_{TUNE} are sweep from 0.2 V to 1.2 V under voltage supply , V_{DD} of 1.2. It shows that the measured output power of 3.85 dBm under the tuning voltage of 600mV. Achieving a wide tuning range of 28.6 % (2.9-2.2/2.45) GHz, the simulated and measured power level agrees and intercept closely when the tuning voltage, V_{TUNE} at 0.7 V, whereas for the simulated and measured carrier of frequency relate closely at V_{TUNE} = 0.9 V , thus explains the reliability level and close variance in gaining a special target. Since the V_{TUNE} are controlled in the parameter analyzer, this creates a degree of freedom to set the tuning voltage in order to achieve a desired frequency within the bandwidth. The measured output power level shown in Figure 5.7 and 5.8 at 2.45 GHz operating frequency under voltage supply, V_{DD} of 1.25V and 1.3V using Agilent Spectrum Analyzer.

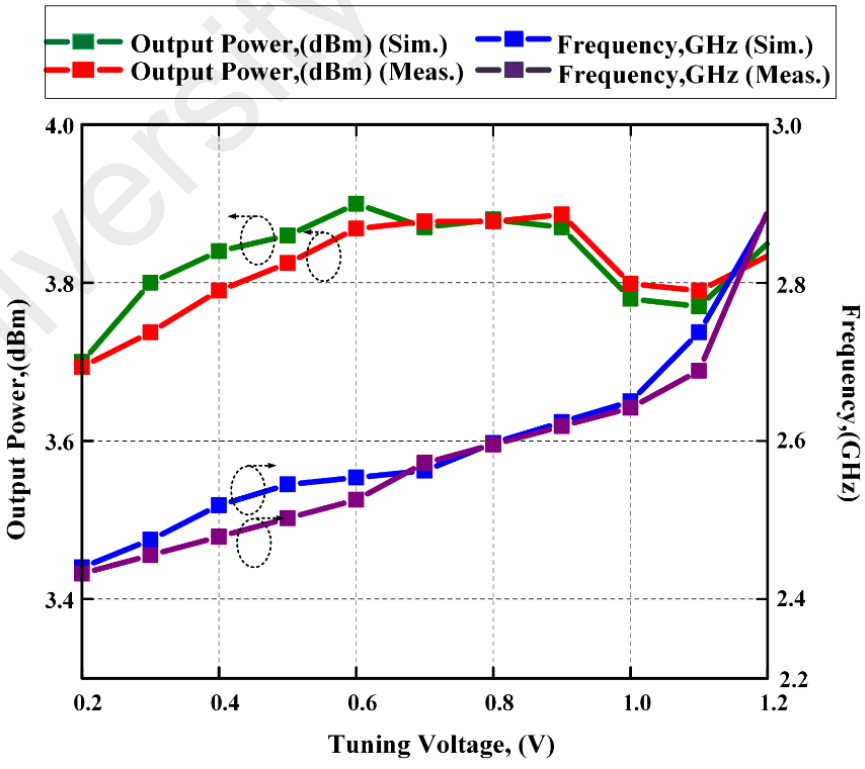

Figure 5.6: Measured and simulated output power, dBm and frequency, GHz against tuning voltage, V

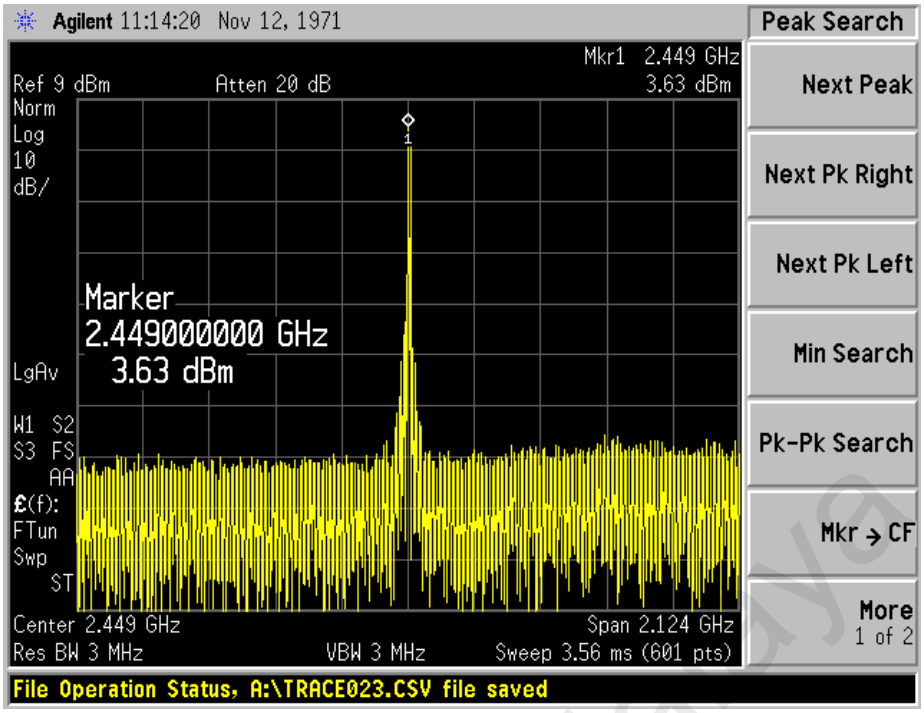

Figure 5.7: Measured output power, dBm at center frequency, 2.45 GHz at V_{DD}= 1.25V

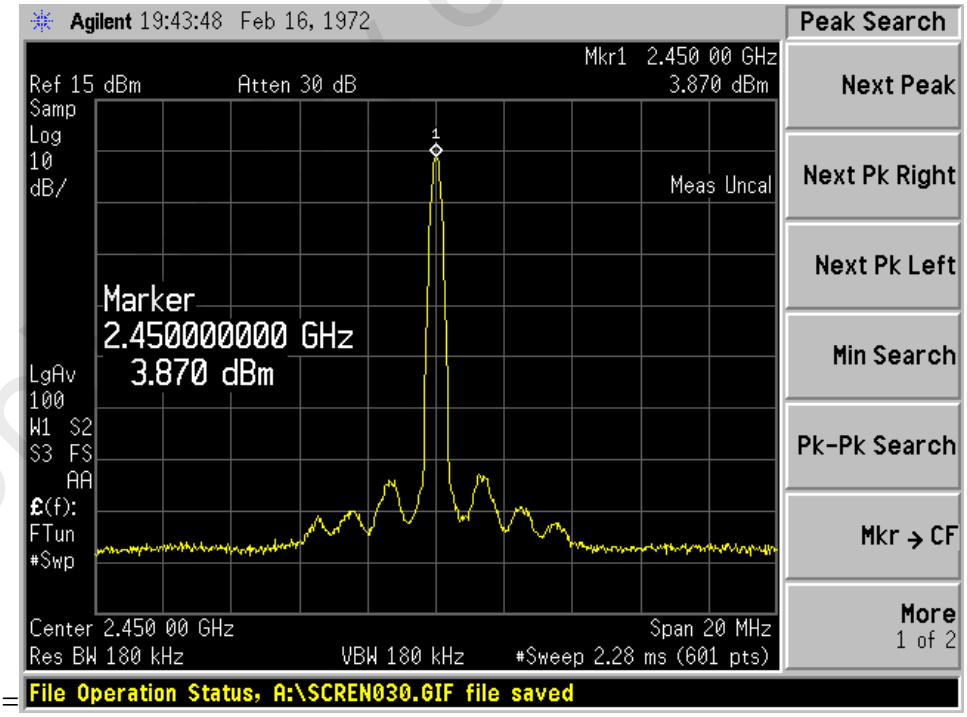

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Figure 5.8: Measured output power, dBm at center frequency, 2.45 GHz at V_{DD}= 1.3V

Finally, Figure 5.9 and Figure 5.10 depicts the measured phase noise, PN performance and Figure of Merit, FoM respectively across the tuning frequency in the range of 2.1 to 2.9 GHz where it was normalized until 2.8 GHz span for accuracy purpose. After 2.8 GHz span, the VCO shows a saturation point (not shown) and behaves steadily. The designed VCO achieves an excellent phase noise target around -120 dBc/Hz at 1 MHz offset frequency. At 3 MHz and 10 MHz, the acquired PN is about -132 dBc/Hz and – 143 dBc/Hz respectively taken at the carrier frequency of 2.45 GHz. The proposed VCO achieves an excellent PN performance which translates to a FoM of 185.41 dBc/Hz at the frequency of 2.45 GHz and interpolated for 1 MHz, 3 MHz and 10 MHz at the same FoM value. This shows that the FoM does not appear to change a lot at the stated offset frequency. As the bandwidth widens, the FoM substantially reduced but still remain above 177 dBc/Hz across frequency bandwidth which expounds the stability and high sensitivity of the VCO.

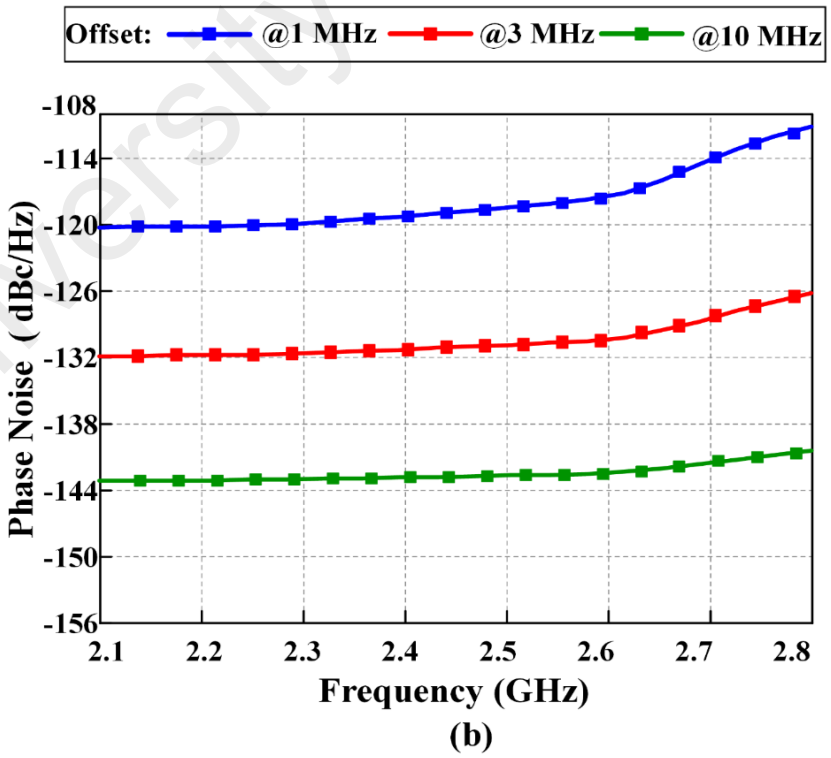

Figure 5.9: Measured Figure of Merit (FoM) against tuning frequency of the proposed VCO architecture

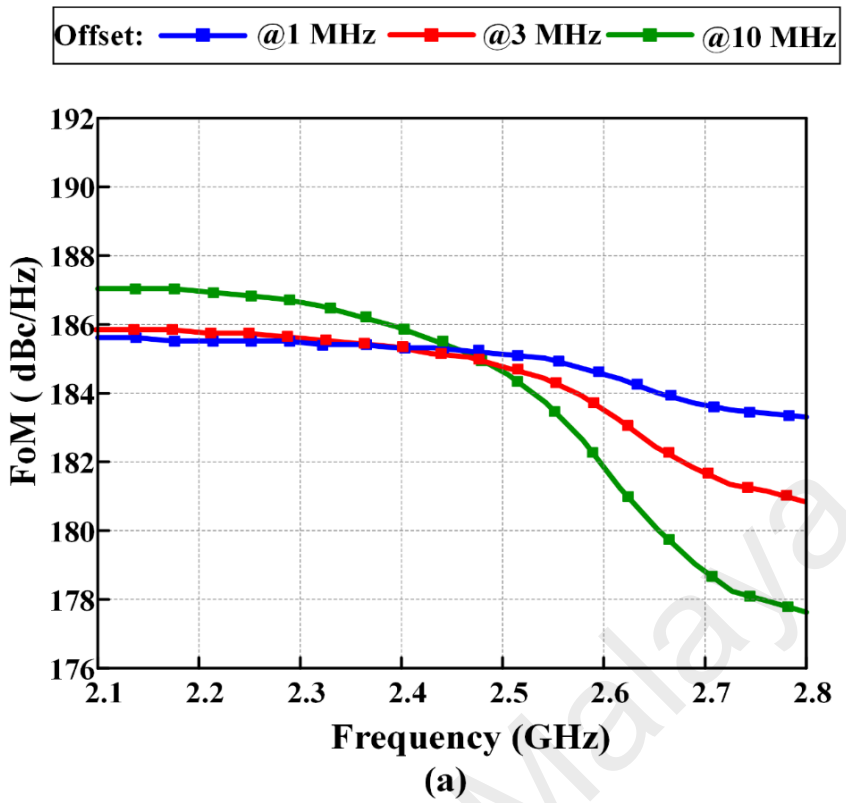

Figure 5.10: Measured Phase Noise, (PN) against tuning frequency of the proposed VCO architecture.

5.2.3 Harmonics and Spurious level

Figure 5.11 shows the measure output power spectrum using Agilent Spectrum Analyzer. The first and fundamental harmonic lies at the frequency of 2.47 GHz at -1.627 dBm whereas the second harmonic (twice the fundamental) at the 4.94 GHz which appears to be much lower amplitude than fundamental in the value of -23.6 dBm harmonic power level. This fundamental and the second harmonic resonance occurred when the tuning of the voltage around 0.6 – 0.9 V.

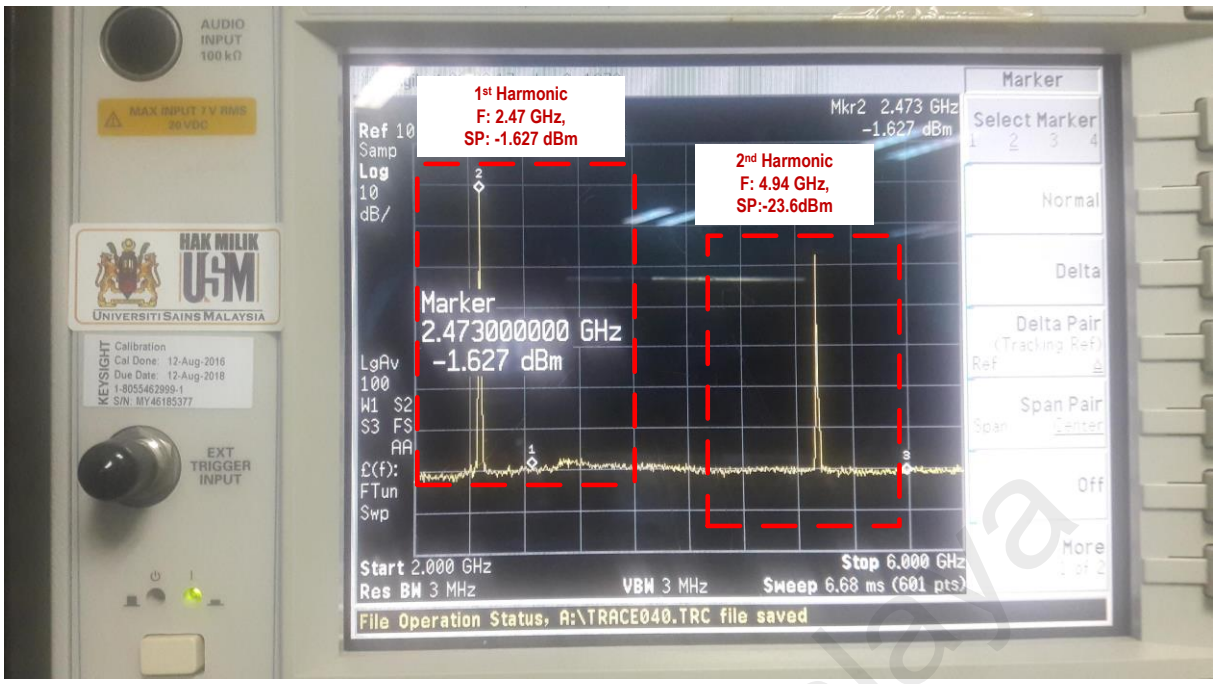

Figure 5.11: Measured Output Spectrum using Agilent Spectrum Analyzer.

5.2.4 Performance Summary of the Proposed Architecture and its Comparison with State-Of-The- Art Recent Reported Works.

Table 5.2 shows the performance of each important parameters for the proposed architecture. The measured $1/f^3$ flicker corner attained is 247 kHz offset frequency and the phase noise at 1 MHz is -120dBc/Hz at 1 MHz offset frequency. This is due to the flicker noise suppression aided by the PMOS tail current source with RC components as a driving AC signal feedback mechanism. The performance parameters achieved a comparable result.

Table 5.2: Performance summary of the proposed architecture.

Parameters	Results
Submicron Technology, nm	180
Operating Frequency, GHz	2.45
Frequency Bandwidth, GHz	2.2 – 2.9
Phase Noise(PN), dBc/Hz @ 1 MHz	-120
Phase Noise(PN), dBc/Hz @ 3 MHz	-132.10
Phase Noise(PN), dBc/Hz @ 10 MHz	-142.12
Figure of Merit(FoM), dBc/Hz @ 1MHz	185.41
Figure of Merit(FoM), dBc/Hz @ 3MHz	185.45
Figure of Merit(FoM) dBc/Hz @ 10MHz	187.52
Tuning Range(TR), %	28.60
$1/f^3$ Flicker Noise Corner, kHz (Sim.)	200
$1/f^3$ Flicker Noise Corner, kHz (Meas.)	247
Frequency Pushing, MHz/V (Sim.)	75
Output Power, dBm (Meas.)	3.63 @ 2.47 GHz
Voltage Supply, V_{DD}	1.2
Power Consumption, P_{DC}	1.73
Current conversion efficiency, α_I	>0.6
Active core area, mm^2	0.3
Startup time, ns	2.0

Table 5.3 shows the recent work comparison with the proposed architecture. (Fathi & Nejad, 2013) and (Shahmohammadi et al., 2016a) operates their proposed oscillator even under low V_{DD} resulting in a comparative phase noise performance. (D. Li, Yang, Zhu, & Shi, 2015) achieve similar level of phase noise as the proposed architecture .However reported a high power consumption and low tuning range despite being area efficient. Furthermore, (Hsu, Chen, & Lee, 2014) able to attained a better tuning range as compared to the former work but the attempt to improve the power consumption is successful in their proposed ZigBee transceiver system since single a core VCO only requires 2.5mW of power as compared to the power needed by (D. Li et al., 2015)**,** (Sánchez-Azqueta, Aguirre, Gimeno, Aldea, & Celma, 2016) and

(Shahmohammadi et al., 2016a)**.** Therefore, there is a room for improving the VCO power consumption, phase noise and the tuning range entirely. In spite of that, the proposed architecture in this research work able to counteract the tradeoff delivering better tuning range of 28.6 % and attained a power consumption of just 1.73 mW under 1.2 V supply. The tuning range has been enhanced and widen with the aid of the Capacitive Source Degeneration, (CSD) technique which relaxes the design from using a more complex circuit of switched capacitor array and switched inductor array. Furthermore, low power consumption is acquired when the complementary Class-C VCO adopted different biasing value under saturation and subthreshold condition. The biasing point are adjusted such a way to save power while achieving a better phase noise performance. The comparison value in the table shows that the proposed architecture are well suited in the wireless application without much constraint compared to the other similar reported works.

Table 5.3: Performance comparison with recent reported works.

Specification		This Work	(Fathi & Nejad, 2013)	(Hsu et al., 2014)	(D. Li et al., 2015)	(Sánchez-Azqueta et al., 2016)	(Shahmohammadi et al., 2016a)
Frequency Range (GHz)		**2.2 – 2.9**	10.53-11.35	4.92-5.7	4.67-5.18	2.05-2.75	5.4-7.0
Tuning Range (%)		**28.6**	7.5	14.7	10.3	29	25
V_{DD} (V)		**1.2**	0.46	1.4	1.8	1.8	1
CMOS Technology (nm)		**180**	180	180	180	180	40
VCO Core Area (mm^2)		**0.3**	N/A	[@]0.98	0.285	N/A	0.13
Frequency (GHz)		**2.45**	10.94	5.31	4.925	2.4	5.4
Power,P_{DC} (mW)		**1.73**	0.346	2.5[&]	8.46	18	12
PN (dBc/Hz)	**1 MHz**	**-120**	-107.8	-118	-120.0	-119.5	-124.5 @ 5 GHz
	10 MHz	**-142.12**	-123[*]	-120[*]	-145[*]	-139[*]	-144.5
FoM (dBc/Hz)	**1 MHz**	**185.40**	193.2	188.52	184.58	174.55	188.36
	10 MHz	**187.52**	188.39	170.52	189.58	174.05	188.36
FoM_T (dBc/Hz)	**1 MHz**	**194.52**	190.70	191.87	184.84	183.80	196.32
	10 MHz	**196.65**	185.89	173.87	189.84	183.30	196.32
Passives		**1 Inductor**	1 Inductor	1 Inductor	SVA	1 Inductor	1 Inductor and 1 Transformer

[&]Only VCO core considered [*]Normalized from 10 MHz offset [@]Include test pad

SVA: Switched Varactor Array

1: $FoM - PN + 20\,log(f_o/\Delta f) - 10\log(P_{DC}/1mW)$

2 : FoM_T: $FoM + 20\log\left(TR\%/_{10}\right)$

CHAPTER 6: CONCLUSION

6.1 Summary and Conclusion

In this dissertation, numerous research works on LC oscillators have been explored and studied. This works creates a much more favorable platform towards the design of this novel circuit.

In chapter 3, the architecture of complementary class-C oscillator with tail current source feedback and noise suppression has been presented for wireless application. The feasibility of the design has been validated via numerous test chip samples taken during measurement. The adopted technique of the Capacitive Source Degeneration, (CSD) implied to enhance the tuning range of 28.6 % at the bandwidth of 2.2 to 2.9 GHz and thus, suppressing the *1/f* flicker noise up-conversion which improves the phase noise measured -120 dBc/ Hz at 1 MHz offset. The power consumption of 1.73 mW designed are low under minimum silicon die area of 0.3mm^2 compared to the recent reported art works adopting switched capacitor and switched inductor array methods. This serve as part of the solution to counteract the tradeoff between low phase noise and wide tuning range. The complementary oscillator, oscillating at 2.47 GHz frequency, attained a sufficient power gain of 3.63 dBm and swing in the range of 600 -700 mV was chosen as best reported value under the 1.2V supply headroom. The RC charging network integrated at the complementary class-C VCO structure implemented a modified biasing of saturation and subthreshold at the cross-coupled PMOS and NMOS respectively. This results in an improved conduction angle of 0.31π performance under low power medium. The split PMOS pair which works as a tail current source feedback been utilized to reduce the flicker noise upconversion into 1/f^3 close in phase noise and also create a stabilized output when the common mode voltages are suppressed effectively. Fast startup is also

ensured when an auxiliary – g_m stage has been integrated to cancel the parasitic resistance of the resonant tank.

6.2 Future Works

This design can be further improved by employing at different classes architecture and incorporated inside the PLL to enhance the investigation on the flicker noise upconversion. Besides a further extension of phase jitter of a PLL and phasor based analysis approach for all classes of oscillator can be developed. Another method possible is to design a transceiver that possess a low power consumption with fast data rate where VCO connected in the PLL attempts to lock the oscillation frequency compensating a lower systematic error and possible variations in the signal transfer. In addition, the PLL built in, will work very fast in the modulation (de) system. The feedback path in the proposed design result in a reduced common-mode resonant frequency but can be suppressed even more with the implementation of high Q resonant tank consequently improves the phase noise further. Besides, we should design an oscillator that can accommodate a wide bandwidth having a tuning range beyond 60 % with minimal area and power consumption. Future work towards incorporating a prototype RF transceiver can de designed for a much accurate and satisfied performance. It will be suitable for base station or an infra-structure sensor networks since requires a lower size constraint and more stringent linearity specifications.

REFERENCES

Amin, T., Yin, J., Mak, P., Member, S., & Martins, R. P. (2015). Class-B / C Hybrid VCO Achieving, *25*(7), 2–4.

Babaie, M., Kuo, F. W., Chen, H. N. R., Cho, L. C., Jou, C. P., Hsueh, F. L., … Staszewski, R. B. (2016). A Fully Integrated Bluetooth Low-Energy Transmitter in 28 nm CMOS With 36% System Efficiency at 3 dBm. *IEEE Journal of Solid-State Circuits*, *51*(7), 1547–1565. https://doi.org/10.1109/JSSC.2016.2551738

Babaie, M., & Staszewski, R. B. (2013). A class-F CMOS oscillator. *IEEE Journal of Solid-State Circuits*, *48*(12), 3120–3133. https://doi.org/10.1109/JSSC.2013.2273823

Berny, A. D., Member, S., Niknejad, A. M., Meyer, R. G., Lc, A. a, & Constraint, a F. S. (2005). A 1.8 - GHz LC VCO With 1.3-GHz and Digital Amplitude Calibration. *Electrical Engineering*, *40*(4), 909–917.

Chen, J., Jonsson, F., Carlsson, M., Hedenäs, C., & Zheng, L. R. (2011). A low power, startup ensured and constant amplitude class-C VCO in 0.18 μm CMOS. *IEEE Microwave and Wireless Components Letters*, *21*(8), 427–429. https://doi.org/10.1109/LMWC.2011.2160620

Chen, Z., Hong, W., Chen, J., & Zhou, J. (2013). Design of high-Q tunable SIW resonator and its application to low phase noise VCO. *IEEE Microwave and Wireless Components Letters*, *23*(1), 43–45. https://doi.org/10.1109/LMWC.2012.2234088

Cusmal, G., Repossi, M., Albasini, G., & Svelto, F. (2007). A 3.2-to-7.3GHz quadrature oscillator with magnetic tuning. *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, 11–13. https://doi.org/10.1109/ISSCC.2007.373603

Deng, W., Okada, K., & Matsuzawa, A. (2013). Class-C VCO with amplitude feedback loop for robust start-up and enhanced oscillation swing. *IEEE Journal of Solid-State Circuits*, *48*(2), 429–440. https://doi.org/10.1109/JSSC.2012.2227603

Fanori, L., & Andreani, P. (2012). Class-C CMOS VCOs with a FoM of 191dBc / Hz Class-B VCO, *IEEE Journal of Solid-State Circuits*, 4–7.

Fanori, L., & Andreani, P. (2013a). A high-swing complementary class-C VCO. *2013 Proceedings of the ESSCIRC (ESSCIRC)*, 407–410. https://doi.org/10.1109/ESSCIRC.2013.6649159

Fanori, L., & Andreani, P. (2013b). Class-D CMOS oscillators. *IEEE Journal of Solid-State Circuits*, *48*(12), 3105–3119. https://doi.org/10.1109/JSSC.2013.2271531

Fanori, L., Liscidini, A., & Andreani, P. (2012). A 6.7-to-9.2GHz 55nm CMOS hybrid Class-B/Class-C cellular TX VCO. *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, *55*(3), 354–355. https://doi.org/10.1109/ISSCC.2012.6177049

Fanori, L., Mattsson, T., & Andreani, P. (2014). A Class-D CMOS DCO with an on-chip LDO. *European Solid-State Circuits Conference*, 335–338. https://doi.org/10.1109/ESSCIRC.2014.6942090

Fathi, D., & Nejad, A. G. (2013). Ultra-Low Power, Low Phase Noise 10 GHz LC VCO in the Subthreshold Regime. *Circuits and Systems*, *04*(04), 350–355. https://doi.org/10.4236/cs.2013.44047

Garampazzi, M., Dal Toso, S., Liscidini, A., Manstretta, D., Mendez, P., Romano, L., & Castello, R. (2014). An intuitive analysis of phase noise fundamental limits suitable for benchmarking LC oscillators. *IEEE Journal of Solid-State Circuits*, *49*(3), 635–645. https://doi.org/10.1109/JSSC.2014.2301760

Geynet, L., Foucauld, E. De, Vincent, P., Jacquemod, G., & Einstein, A. (2006). Fully-Integrated Multi-Standard VCOs with switched LC tank and Power Controlled by Body Voltage in 130nm CMOS / SOI. *IEEE Radio Frequency Integrated Circuits Symposium*, 11–13. https://doi.org/10.1109/RFIC.2006.1651103

Hegazi, E., Sjöland, H., & Abidi, A. A. (2001). A filtering technique to lower LC oscillator phase noise. *IEEE Journal of Solid-State Circuits*, *36*(12), 1921–1930. https://doi.org/10.1109/4.972142

Heng, C. H., Bansal, A., & Zheng, Y. (2011). Design of 1.94-GHz CMOS noise-cancellation VCO. *IEEE Transactions on Microwave Theory and Techniques*, *59*(2), 368–374. https://doi.org/10.1109/TMTT.2010.2097715

Herzel, F., Erzgraber, H., & Ilkov, N. (2000). A new approach to fully integrated CMOS LC-oscillators with a very\nlarge tuning range. *Proceedings of the IEEE 2000 Custom Integrated Circuits Conference (Cat. No.00CH37044)*, 573–576. https://doi.org/10.1109/CICC.2000.852733

Hsu, M. T., Chen, P. H., & Lee, Y. Y. (2014). Design of 5 GHz low-power CMOS LC VCO based on complementary cross-coupled topology with modified tail current-shaping technique. *International Journal of Microwave and Wireless Technologies*, *6*(6), 573–580. https://doi.org/10.1017/S1759078714000300

Jafari, B., & Sheikhaei, S. (2018). Phase noise reduction in LC cross coupled oscillators using sinusoidal tail current shaping technique. *Analog Integrated Circuits and Signal Processing*, *96*(1), 125–132. https://doi.org/10.1007/s10470-018-1181-x

Kao, H. L., Yang, D. Y., Chin, A., & McAlister, S. P. (2007). A 2.4/5 GHz dual-band VCO using a variable inductor and switched resonator. *IEEE MTT-S International Microwave Symposium Digest*, *2*, 1533–1536. https://doi.org/10.1109/MWSYM.2007.380565

Lee, H., & Mohammadi, S. (2007). A subthreshold low phase noise CMOS LC VCO for ultra low power applications. *IEEE Microwave and Wireless Components Letters*, *17*(11), 796–798. https://doi.org/10.1109/LMWC.2007.908057

Levantino, S., Samori, C., Bonfanti, A., Gierkink, S. L. J., Lacaita, A. L., & Boccuzzi, V. (2002). Frequency dependence on bias current in 5-GHz CMOS VCOs: Impact on tuning range and flicker noise upconversion. *IEEE Journal of Solid-State Circuits*,

37(8), 1003–1011. https://doi.org/10.1109/JSSC.2002.800969

Li, D., Yang, Y. T., Zhu, Z. M., & Shi, Z. C. (2015). A 5-GHz LC VCO with digital AAC and AFBS for 2.4 GHz ZigBee transceiver applications. *Microelectronics Journal*, *46*(6), 415–421. https://doi.org/10.1016/j.mejo.2015.03.017

Li, S., Kipnis, I., & Ismail, M. (2003). A 10-GHz CMOS Quadrature LC-VCO for Multirate Optical Applications. *IEEE Journal of Solid-State Circuits*, *38*(10), 1626–1634.

Liu, S. L., Chen, K. H., & Chin, A. (2012). A dual-resonant mode 10/22-GHz vco with a novel inductive switching approach. *IEEE Transactions on Microwave Theory and Techniques*, *60*(7), 2165–2177. https://doi.org/10.1109/TMTT.2012.2195674

Martins, R., Lourenco, N., Horta, N., Yin, J., Mak, P. I., & Martins, R. P. (2019). Many-objective sizing optimization of a class-C/D VCO for ultralow-power iot and ultralow-phase-noise cellular applications. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *27*(1), 69–82. https://doi.org/10.1109/TVLSI.2018.2872410

Mazzanti, A., & Andreani, P. (2008). Class-C harmonic CMOS VCOs, with a general result on phase noise. *IEEE Journal of Solid-State Circuits*, *43*(12), 2716–2729. https://doi.org/10.1109/JSSC.2008.2004867

Mazzanti, A., & Andreani, P. (2013). A push-pull class-C CMOS VCO. *IEEE Journal of Solid-State Circuits*, *48*(3), 724–732. https://doi.org/10.1109/JSSC.2012.2230542

Men, K., Thangarasu, B. K., & Yeo, K. S. (2016). A VCO phase noise reduction technique to suppress the active device contribution. *Proceedings - International NanoElectronics Conference, INEC*, *2016-Octob*, 1–2. https://doi.org/10.1109/INEC.2016.7589433

Moon, Y., Roh, Y., Jeong, C., & Yoo, C. (2009). A 4.39-5.26 GHz LC-Tank CMOS Voltage-Controlled Oscillator With Small VCO-Gain Variation. *IEEE Microwave and Wireless Components Letters*, *19*(8), 524–526.

Mostajeran, A., Bakhtiar, M. S., & Afshari, E. (2015). A 2.4GHz VCO with FOM of 190dBc/Hz at 10kHz-to-2MHz offset frequencies in 0.13µm CMOS using an ISF manipulation technique. *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, *58*, 452–453. https://doi.org/10.1109/ISSCC.2015.7063121

Murphy, D., Rael, J. J., & Abidi, A. A. (2010). Phase Noise in LC Oscillator: A Phasor Based Analysis of a General Result and of Loaded Q. *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS- I)*, *57*(6), 1187–1203. https://doi.org/10.1109/TCSI.2009.2030110

Narayanan, A. T., Kimura, K., Deng, W., Okada, K., & Matsuzawa, A. (2014). A pulse-driven LC-VCO with a figure-of-merit of -192dBc/Hz. *European Solid-State Circuits Conference*, 343–346. https://doi.org/10.1109/ESSCIRC.2014.6942092

Okada, K., Nomiyama, Y., Murakami, R., & Matsuzawa, A. (2009). A 0.114-mW dual-conduction class-C CMOS VCO with 0.2-V power supply. *2009 Symposium on*

VLSI Circuits, (3), 228–229.

Park, B., Lee, S., Choi, S., & Hong, S. (2008). A 12-GHz fully integrated cascode CMOS LC VCO with Q-enhancement circuit. *IEEE Microwave and Wireless Components Letters*, *18*(2), 133–135. https://doi.org/10.1109/LMWC.2007.915136

Rout, S. S., Acharya, S., & Sethi, K. (2018). A low phase noise gm-boosted DTMOS VCO design in 180 nm CMOS technology. *Karbala International Journal of Modern Science*, *4*(2), 228–236. https://doi.org/10.1016/j.kijoms.2018.03.001

Sánchez-Azqueta, C., Aguirre, J., Gimeno, C., Aldea, C., & Celma, S. (2016). High-resolution wide-band LC-VCO for reliable operation in phase-locked loops. *Microelectronics Reliability*, *63*, 251–255. https://doi.org/10.1016/j.microrel.2016.06.018

Seok-Ju Yun, So-Bong Shin, Hyung-Chul Choi, & Sang-Gug Lee. (2005). A 1mw current-reuse CMOS differential LC-VCO with low phase noise. *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005.*, *49*(1), 540–542. https://doi.org/10.1109/ISSCC.2005.1494108

Shahmohammadi, M., Babaie, M., & Staszewski, R. B. (2016a). A 1/f Noise Upconversion Reduction Technique for Voltage-Biased RF CMOS Oscillators. *IEEE Journal of Solid-State Circuits*, *51*(11), 2610–2624. https://doi.org/10.1109/JSSC.2016.2602214

Shasidharan, P. N., Ramiah, H., & Rajendran, J. (2018). Integrated Class C-VCO - Mixer for 2.45 GHz transmitter in 180nm CMOS technology. *Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics*, *2017-October*, 73–76. https://doi.org/10.1109/PRIMEASIA.2017.8280367

Shasidharan, P., Ramiah, H., & Rajendran, J. (2019). A 2.2 to 2.9 GHz Complementary Class-C VCO with PMOS Tail-Current Source Feedback Achieving -120 dBc/Hz Phase Noise at 1MHz offset. *IEEE Access*, *PP*, 1–1. https://doi.org/10.1109/ACCESS.2019.2927031

Takeuchi, Y., Okada, K., & Matsuzawa, A. (2011). An improved dual-conduction class-C VCO using a tail resistor. *European Microwave Integrated Circuits Conference (EuMIC)*, (October), 204–207. Retrieved from http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6102829

Tohidian, M., Fotowat-Ahmadi, A., Kamarei, M., & Ndagijimana, F. (2011). High-swing class-C VCO. *European Solid-State Circuits Conference*, 495–498. https://doi.org/10.1109/ESSCIRC.2011.6045015

Wei, M. D., Negra, R., Chang, S. F., & Chen, C. S. (2017). Wideband complementary CMOS VCO with capacitive-source-degeneration technique. *17th IEEE International Conference on Smart Technologies, EUROCON 2017 - Conference Proceedings*, (July), 287–291. https://doi.org/10.1109/EUROCON.2017.8011121

Xiaosong, W., Shuilong, H., Pufeng, C., & Haiying, Z. (2010). A 1.8-2.6 GHz CMOS VCO with switched capacitor array and switched inductor array. *Journal of Semiconductors*, *31*(2), 0–4. https://doi.org/10.1088/1674-4926/31/2/025001

Yi, H., Yu, W. H., Mak, P. I., Yin, J., & Martins, R. P. (2018a). A 0.18-V 382-μ W Bluetooth Low-Energy Receiver Front-End with 1.33-nW Sleep Power for Energy-Harvesting Applications in 28-nm CMOS. *IEEE Journal of Solid-State Circuits*, *53*(6), 1618–1627. https://doi.org/10.1109/JSSC.2018.2815987

Yi, H., Yu, W. H., Mak, P. I., Yin, J., & Martins, R. P. (2018b). A 0.18-V 382-μ W Bluetooth Low-Energy Receiver Front-End with 1.33-nW Sleep Power for Energy-Harvesting Applications in 28-nm CMOS. *IEEE Journal of Solid-State Circuits*, *53*(6), 1618–1627. https://doi.org/10.1109/JSSC.2018.2815987

Yim, S.-M., & Kenneth K.O. (2006). Switched Resonators and Their Applications in a Dual-Band Monolithic CMOS LC-Tuned VCO. *IEEE Transactions on Microwave Theory and Techniques*, *54*. https://doi.org/10.1029/2004JC002633

Yoon, H., Lee, Y., Kim, J. J., & Choi, J. (2014). A wideband dual-mode LC-VCO with a switchable gate-biased active core. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *61*(5), 289–293. https://doi.org/10.1109/TCSII.2014.2305216

LIST OF PUBLICATIONS, PAPERS PRESENTED AND AWARDS

Conferences Paper

Shasidharan, P. N., & Ramiah, H. (2017). Integrated Class C -VCO - Mixer for 2 . 45GHz Transmitter in 180nm CMOS Technology, 77–80.

ISI Journal

Shasidharan, P., Ramiah, H., & Rajendran, J. (2019). A 2.2 to 2.9 GHz Complementary Class-C VCO with PMOS Tail-Current Source Feedback Achieving -120 dBc/Hz Phase Noise at 1MHz offset. *IEEE Access*, *PP*, 1–1. https://doi.org/10.1109/ACCESS.2019.2927031.

Co authored Journal

Balan, Z., Ramiah, H., Rajendran, J., Vitee, N., & Nair, P. (2019.). Bluetooth Low Energy / ZigBee Receiver consuming 2mA. *Integration,the VLSI Journal*