HIGH EFFICIENCY RF POWER AMPLIFIER WITH CLOSED LOOP SYSTEM FOR PUBLIC SAFETY RADIO COMMUNICATIONS

LOKESH ANAND A/L VIJAYAKUMARAN

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LOKESH ANAND A/L VIJAYAKUMARAN

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HIGH EFFICIENCY RF POWER AMPLIFIER WITH CLOSED LOOP SYSTEM FOR PUBLIC SAFETY RADIO COMMUNICATIONS

ABSTRACT

The design of transmitter line up for public safety radio communications entails many challenges at both architecture and circuit levels. The key point in this research work concerns the development of RF PA line up where the research introduces 3 design methodologies which is not available in current conventional 2 -way radio design. Firstly, a parallel-combined impedance matching technique is introduced where it enables the designers to develop broadband PA with actual PA device impedance. Since developing a RF PA line up alone is not enough, and a fast output power ramp up is needed for a quick data transmission during mission critical operation. So a new technique to characterize the behavioural response of multistage RF PA is explored. For that, a simplified design methodology of closed loop PA with DC current sensing of multistage PA (cascaded) and voltage shaping algorithm is used in this work. The above two methodologies are combined and a novel closed-loop adaptive power amplifier (PA) design which provides constant efficiency across wide power level is developed (state of art of current work). Experimental results demonstrated output power of ~80 W and gain of 42 dB over the bandwidth of interest. Constant efficiency (48%) and transient timing response of 1.1 ms is achieved while maintaining good transient power of less than -50 dB over the frequency range of 400 to 520 MHz. This work allows the public safety and mission critical two-way radio products been accepted widely since the users have the platform for building interoperability into their systems. Since transmitting is the most energy intensive operation, the adaptive RF PA design can typically function 40% longer in terms of battery life than the non-adaptive conventional architecture of two-way radios.

Keywords : efficiency, transient power, closed loop

ABSTRAK

Reka bentuk pemancar yang sesuai untuk komunikasi radio keselamatan awam mempunyai banyak cabaran di dalam implementasi dan juga rekabentuk litar. Titik utama dalam reka bentuk RF PA melibatkan peringkat terakhir di mana penyelidikan memperkenalkan metodologi reka bentuk berdasarkan teknik pemadanan impedans yang selari yang membolehkan rekaan penguat kuasa jalur lebar dengan impedans peranti PA sebenar. Di samping itu, teknik baru untuk mencirikan tindak balas penguat kuasa diperkenalkan. Metodologi reka bentuk mudah penguat kuasa gelung tertutup dengan pengesan arus elektrik (arus terus) dan algoritma membentuk voltan digunakan dalam kerja ini. Bagi kecekapan berterusan, pengesan logaritmik dicadangkan. Keunikan penyelidikan ini ada dalam merealisasikan bentuk penguat kuasa adaptif gelung tertutup untuk memberikan kecekapan berterusan merentasi tahap kuasa yang luas. Analisis kestabilan isyarat besar, dalam teknik pengecam kutub-sifar tertentu digunakan untuk menyiasat ayunan sebelum membina papan prototaip dan disahkan pada tahap pengukuran. Keputusan eksperimen menunjukkan kuasa output ~ 80 W dan keuntungan 42 dB sepanjan lebar jalur yang diuji. Kecekapan berterusan (48%) dan tindak balas masa sementara 1.1 ms dicapai sambil mengekalkan ACTP yang baik kurang daripada -50 dB di dalam julat frekuensi 400 hingga 520 MHz. Kerja ini membolehkan produk radio dua hala kritikal keselamatan dan misi diterima secara meluas kerana pengguna mempunyai platform untuk membina operasi saling kendalian ke dalam sistem mereka. Oleh kerana penghantaran isyarat akan mengunakan tenaga, reka bentuk penguat kuasa dalam penyelidikan ini akan berfungsi 40% lebih lama dari segi tempoh hayat bateri berbanding dengan seni bina konvensional

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Pursuing the doctoral degree begins with a great deal of excitement and expectations. However, after years of endeavours, the initial love and devotions to the research topic gradually become frustrations by the overwhelming obstacle and adversity, and I start to realize that this journey would never be fulfilled without the support of many people.

First and foremost, praises and thanks to the God, the Almighty, for His showers of blessings throughout my research work to complete the research successfully. Following in the list, I would like to express my sincere gratitude and appreciation to my supervisor, Associate Professor Dr. Narendra Kumar. Without his continuous guidance and encouragement, my research work towards this thesis would never be possible. I would also like to thank my second supervisor, Associate Professor Dr. Jeevan for his assistance throughout the years, as his knowledge and experience were also valuable.

This work has benefited from the contributions of many other individuals. Special thanks to Dr. Hari Narayanan and Mr. Solomon Lorthu for giving an opportunity to me to pursue PhD studies while I am attached to Motorola Solutions, Research & Development Department. Their enthusiastic help and encouragement are greatly acknowledged.

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LIST OF SYMBOLS AND ABBREVIATIONS

ACTP	:	Adjacent Channel Transient Power
BFSK	:	Binary Frequency Shift Keying
BPF	:	Band Pass Filter
CMOS	:	Complementary Metal Oxide Semiconductor
CPWG	:	Coplanar Wave Guide
DAC	:	Digital to Analog Converter
FET	:	Field Effect Transistor
IEEE	:	Institute of Electrical and Electronics Engineers
IF	:	Intermediate Frequency
LDMOS	:	Lateral Diffusion Metal Oxide Semiconductor
LO	:	Local Oscillator
LPF	:	Low Pass Filter
MIMO	:	Multiple Input Multiple Output
OFDM	:	Orthogonal Frequency Division Multiplexing
PAE	:	Power Added Efficiency
PCB	:	Printed Circuit Board
RF PA	:	Radio Frequency Power Amplifier
TDMA	:	Time-Division Multiple Access
UWB	:	Ultra Wideband
VCCS	:	Voltage Control Current Source
VCO	:	Voltage Control Oscillator
VCVS	:	Voltage Control Voltage Source
WLAN	:	Wireless Local Area Network

LIST OF APPENDICES

CHAPTER 1 : INTRODUCTION

1.1 2-way radio communications

Many claimed the first official 2-way radio to the invention of Donald Hingins and some say it was Alfred Gross who patented the technology in 1938. Other sources give credit to Galvin Manufacturing (now known as Motorola Solutions) who created the first device named walkie talkie in their SCR300 model. But regardless who was the first, it is well accepted that Motorola Inc. has been the most successful organization in developing the radio technology.

Initially the technology was driven by military need and gradually progressed into devices which are compact and lightweight with advance functional features. Today, 2-way radio models typically offer channels with multiple frequencies and other advancements such as hands-free applications, wireless charging and digital vocoder. The flexibility and robustness of the 2-way radio makes it to be great choice for number of purposes which include professional and personal usage as well as public safety.

1.2 2-way radio – current solution for current needs

2-way radio offers certain advantages which make it a clear choice for the mobile professionals eventhough with the presence of evolving technologies such as cellular, push to talk over cellular and voice over WLAN. Advantages of 2-way radio include

- **Low total cost of ownership** – 2-way radio solutions requires no recurring monthly fees and can typically pay for itself in less than 18 months compared to cellular solutions that require recurring monthly fees.
- **Customizable coverage and features** – The ability to tailor a 2-way radio solution to meet the needs of business is still unbeatable. Quick, reliable, one to

one, one to many and many to many communications capability of 2-way radio solutions remains unequaled.

- **Reliable and simple implementation** – On site solutions often require no infrastructure at all. Users simply turn on their radios and talk directly to each other in the range of few miles using rugged devices. For group voice calls, with coverage requirements measured in miles, 2-way radio solutions continue to provide simplicity and reliability better than cellular and other competing technologies.

In transportation, energy, government, hospitality and many other industries, 2-way radio system offer capabilities that no other mobile technology can provide. 2-way radio can offer instant, private and cost effective communication virtually in any environment, anywhere, anytime. With 2-way radio, there is no need to deploy supporting infrastructure in a field situation or rely on subscriber based public networks that may be under supported or even unavailable at certain circumstances. Since its inception, 2-way radio has been an analog medium but now the digital technology starts to offer several advantages over the analog systems of the past

1.3 Motivation - Next Generation 2-Way Radios For Professional Tier

Next generation radio system is a digital communications platform that combines the best of 2-way radio with digital technology based on TDMA to deliver increased capacity and spectral efficiency. The radios are designed to meet the requirements of professional organizations that need a mission critical communication solutions. The next generation radio design demands many capabilities and features. For example,

- Need of high performance and robustness in the field
- Radio communications requires a fast data transmission especially for the mission critical product portfolio
- Enable longer battery life in the field by requiring an adaptive transmit power with specific method and power management technologies used in the device.

Looking into the demand, next generation 2-way radio will continue to be the technology of choice tomorrow. This research is centered towards designing a transmitter architecture for next generation 2-way radio bringing together real world experience, customers' insight and technological innovations. With new design models, the transmitter architecture brings a whole range of new capabilities to make the communication more efficient and more productive.

1.4 RF Front End

The core element for the 2-way portable radio communications system is perhaps the RF front-end. The RF front-end consist of electronic circuitry and an antenna. Its function is to convert electrical signals to electromagnetic waves, which is subsequently transmitted (transmitter) and received (receiver) through the air. Early implementation of the transmitter consisted of an oscillator which emits continuously a train of undamped waves. By interrupting these undamped waves into long and short pulses, the information to be transmitted/received was included. In early years, the active element in the oscillator was a vacuum tube and today in commercial RF transmitters for wireless communication, the vacuum tube has been replaced by the solid state transistor.

Modern RF transmitters can be viewed as composition of several sub-circuits (see Figure 1.1), namely power amplifier, base band circuitry, oscillators, mixers, filters and circulators. These blocks are often implemented in different technologies, and often

the main goal is to optimize on cost, part count and size. These goals are the driving forces for high levels of integration.

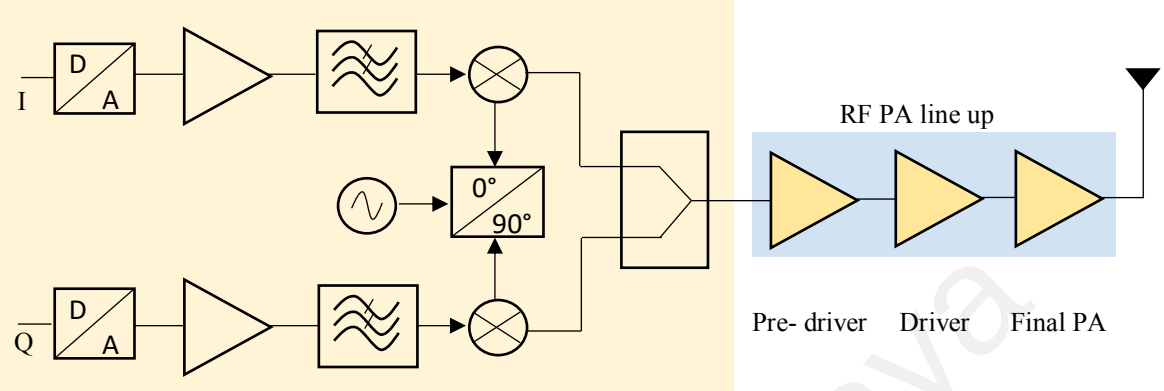


Figure 1.1: Direct conversion transmitter architecture

1.4.1 RF Power Amplifier

Power amplifier (PA) is a very crucial component in the transmitter as it is the last active link between the small signal path of the components and the antenna. A technical definition might be a transmitter is designed to produce radio waves with an antenna. The transmitter itself generates a radio frequency (RF) current whereby when excited, radiates radio waves through antenna. But in practice, by a "transmitter architecture" means high levels of integration. A RF transmitter performs modulation, upconversion and power amplification (Razavi, 1999) and requires a great understanding of architecture because of their influence on the choice of power control scheme and closed loop system. The choice of a RF PA line up is determined by few important factors; output power level, operating bandwidth, modulation scheme and number of external filters

The amount space available on PCB, the restrictions on unwanted emissions, the trade-off between output power and efficiency, the trade-off between fast ramping and transient power directly impact the choice of the transmitter topology. The implementation of each circuit block would be a great challenge too.

The design of transmitter line up for 2-way radio solutions entails many challenges at both architecture and circuit levels. The amount space available on PCB, the restrictions on unwanted emissions, the trade-off between output power and efficiency, the trade-off between fast ramping and transient power directly impact the choice of the transmitter topology. The implementation of each circuit block would be a great challenge too.

A logical starting point for a research on 2 way radio design would be to define what a transmitter architecture actually is. A technical definition might be a transmitter is designed to produce radio waves with an antenna. The transmitter itself generates a radio frequency (RF) current whereby when excited, radiates radio waves through antenna. But in practice, by a "transmitter architecture" means high levels of integration. A RF transmitter performs modulation, upconversion and power amplification and requires a great understanding of architecture because of their influence on the choice of power control scheme and closed loop system. The choice of a transmitter architecture is determined by few important factors; output power level, operating bandwidth, modulation scheme and number of external filters.

Till to date, many efforts have been made to construct transmitter architecture and its application in wireless systems. Gebreyohannes proposed a configurable baseband transmitter architecture for IEEE 802.11ac and 803. 11ad standards (Gebreyohannes, Frappé, & Kaiser, 2016). In this work a configurable mixed signal digital to analog converter (DAC) which operates on the oversampled WiFi and raw WiGig data at a common 3.52GHz clock frequency is designed . The architecture can meet the IEEE standards with maximum hardware sharing but in a small form factor. For a railroad wireless application, Choi did a survey and introduce a novel concept on dual band polar transmitter architecture to reduce the dual band phase modulation bandwidth (Choi, Cho,

Kim, & Ryu, 2015). His work proves that at low frequency, complex signal processing efficiently employs the polar transmitter

On the other hand, BFSK transmitter architecture that uses mixing and image rejection enables low power consumption in the frequency band of 401 – 457 MHz also available. This is achieved by avoiding fast settling time requirements for the frequency locked loop (Ibrahim & Onabajo, 2017). A digital centric IF- DAC based heterodyne transmitter architecture, provides a spurious free band around the center frequency of 2.4 GHz. (bandwidth of 40 MHz) – (Hanay, Bayram, & Negra, 2017) . Looking into signal amplification on a LINC transmitter architecture, a work presented by Aref develops an algorithm to optimize the multiple symmetrical levels of signal to improve system efficiency in general (Aref, Askar, Nafe, Tarar, & Negra, 2012). The traded off between efficiency and linearity is well defined where the use of spectral efficient modulation schemes in corporation with linearization techniques in LINC transmitter architecture gives the best option for nano satellite applications (Karunanithi, Verhoeven, & Lubbers, 2015).

For a space-frequency block coding (SFBC) MIMO – OFDM systems, a low complexity transmitter architecture is developed by generating by utilizing time-domain signal properties and signal correlations among the various transmitter antennas. The level of complexity is reduced by 50% compared to the traditional SFBC MIMO-OFDM transmitter architecture (Li, Wang, & Tsai, 2010) . As the technology evolved further, variety requirements on the system design are put in place for future wireless communication system. For higher data rate, researchers still expecting better transmission schemes with efficient usage of available spectrum. Recent work on filter bank based multicarrier (FBMC) transmitter architecture shows that with modified inverse fast Fourier transform algorithm gives good signal properties with sufficient room for system design (Madheswaran, Abraham, & Sharma, 2017). On the other hand,

security in mm-wave communication is critical too due to the nature of signal broadcasting. Having said that, a new transmitter architecture called switched phased array (SPA) is developed recently to improve the physical layer security (Alotaibi & Hamdi, 2016).

1.5 Problem Statement

As there are number of transmitter architectures been developed for various requirements and standards, this work takes a step forward to explore the transmission schemes which best suits for a two-way communication radio. In general, the RF PA line up in any public safety radio architecture suffers from multiple constraints and limitations as listed below.

1. The need for high power RF PA line up to ensure a good communication distance without any loss of transmitted data
2. A fast output power ramp up is needed for a quick data transmission since the information should be conveyed as fast as possible during mission critical operation. At the same time, the transmitted power should not interfere the adjacent channels within the operating bands. It is a design limitation to achieve fast power ramping and to keep adjacent channel power low.
3. An adaptive power adjustment is required to achieve optimum or constant efficiency over wide dynamic power level. Constant efficiency ensures a good battery life.
    - A good battery life means the 2 way radio can sustain for longer usage especially during mission critical operations. A missed call or dead battery can cause dissatisfaction, lowered productivity and loss of business

In order to meet the above requirements in a single design architecture, an extensive research work is needed in developing the RF PA line up. Having said that, this research

work aims to develop a RF PA line up that meets the current 2-way radio needs which is not available in current conventional design.

1.6 Research Objective

This research work is carried out mainly to resolve the constraints and limitations with the currently available conventional 2-way radio design. In addition, the research is centred towards meeting the design requirements of professional organizations that need a mission critical and public safety communication solution. Having said that, this research work is tailored based on design goals mentioned below.

1. To design of broadband (760 – 870 MHz) high performance power amplifier line up for two-way radio applications.
    - The expected total output power of the line up is 80W with an efficiency of 50%
    - To introduce a design methodology which can fit into a small form factor PCB board
2. To design a circuit that which can gives a fast output power ramp up and ramp down for a quick access on data transmission
    - No interference at the adjacent channels within the operating bands since a fast output power ramping can create splatters (noise) which caused disturbance for the users
3. To design an adaptive power adjustment circuitry to achieve optimum or constant efficiency of more than 45% over wide dynamic power level.
    - The adaptive power circuitry should give a battery life improvement up to 40% compare to battery life achievement using a conventional design.

The above mentioned research objectives are well experimented and explained in Chapter 3, 4 and 5. All the research outcomes and challenges are included as well.

1.7 Thesis Outline

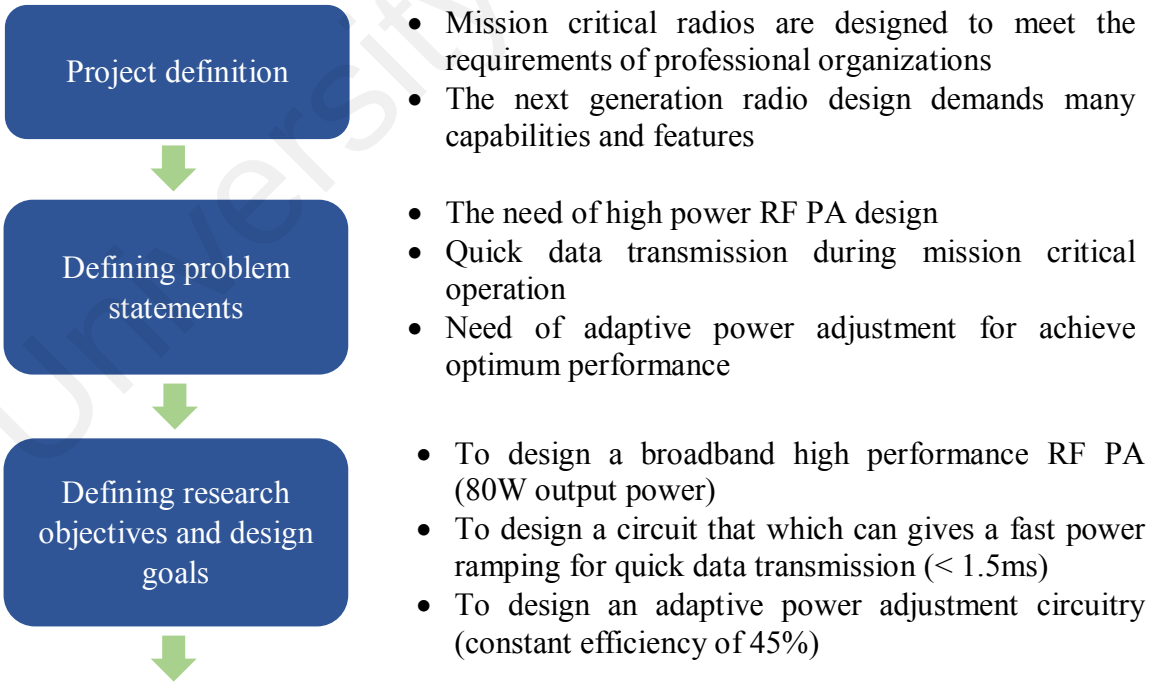
This thesis is presented in article style format which consists of 6 chapters. Each of the chapter was written according to the progress of the report. Chapter 1 is the introduction part of the project which covers the objective of the project. In order to get a better view of the work, an overview of 2-way radio communications and its technology advancements are included. The research scope is well defined with some explanations with regards to design goal both at circuit and architecture level.

Chapter 2 revisits some basic theory and fundamentals of transmitter architecture design for 2-way radios which is generally a complicated procedure to design an effective impedance matching depending on technical requirement and operation conditions, stability in operation, efficiency, output power, gain and ease in practical implementation. Therefore, at the beginning of some sections, the key definitions of technical terms are included as well. Chapter 2 takes the attempt to study on different types of transmitter architecture design which is indeed a backbone of this thesis.

The detailed circuit design and analysis of transmitter architecture are described in Chapter 3, 4 and 5. To be specific, Chapter 3 describes the design of broadband high performance power amplifier (PA) line up for mobile two-way radio applications. The key point in the design of the PA line up concerns the final stage where the chapter introduces a design methodology based on parallel-combined impedance matching technique which enables the designers to develop broadband PA with actual PA device impedance. Chapter 4 highlights a new technique to characterize the behavioural response of multistage RF PA. A simplified design methodology of closed loop PA with DC

current sensing of multistage PA (cascaded) and voltage shaping algorithm is introduced in this work. Part III covers closed-loop adaptive PA design to provide constant efficiency across wide power level and fast power ramping from noise level to steady state while meeting adjacent channel transient power (ACTP). For the constant efficiency, a gate stage controlled with logarithmic detector is proposed. As for the fast transient power, the time of the ramping is achieved with integration of the PA current sensing and voltage shaping algorithm. In a nutshell, Chapter 5 basically combines high performance PA design (Part I) and transient behavioural characterization (Part II) with an introduction of closed loop adaptive PA design. The combinations of Chapter 3, 4 and 5 completes the RF PA line up for next generation 2-way radio communications. The conclusions and future work recommendation are presented in Chapter 6.

The overall thesis outline is been summarized in flow chart below



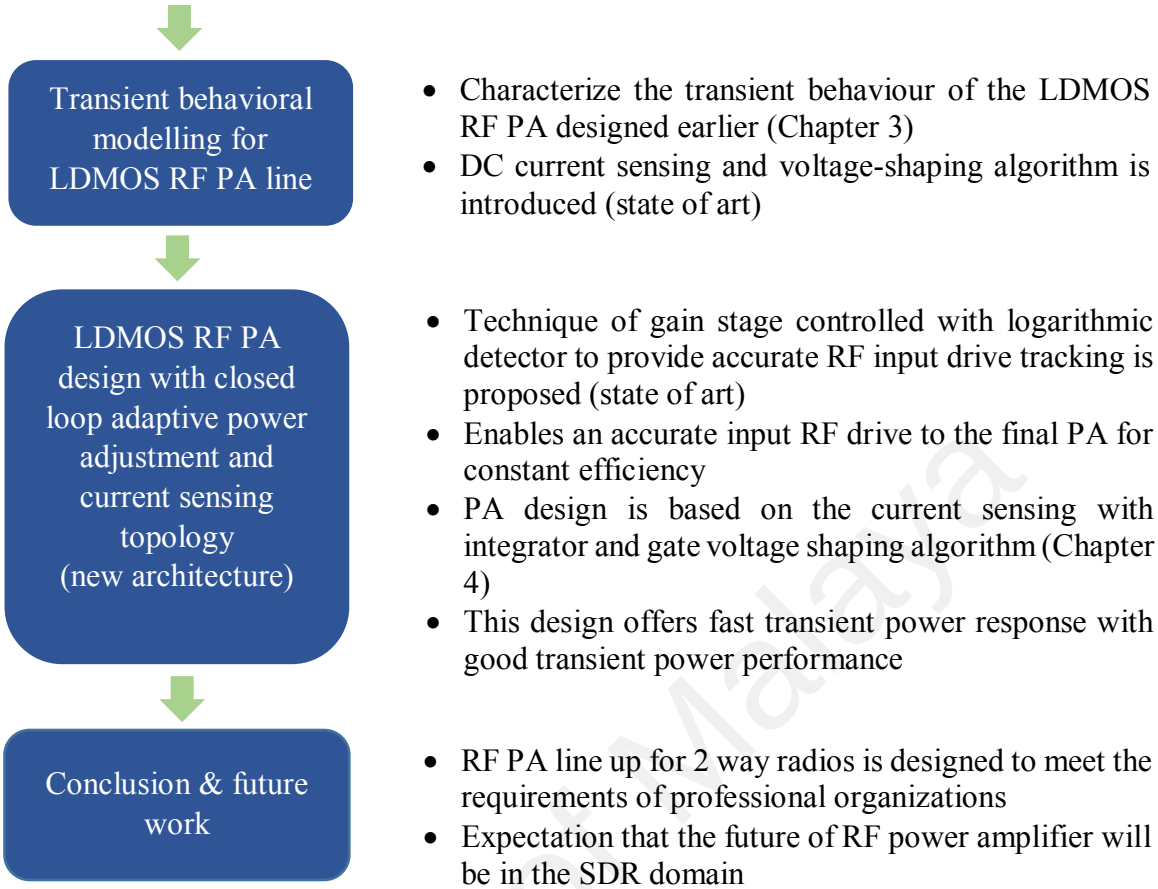


Figure 1.2: Flowchart of thesis outlines

CHAPTER 2 : LITERATURE REVIEW

2.1 RF PA Line Up Architecture and Circuits

The construction of RF transmitters for wireless application are tedious indeed and faces many challenges at both architecture and implementation levels. The topology is very much dependent to restriction on unwanted emissions, trade off between maximum output power and efficiency as well linearity (Razavi, 1999). This section provides an in depth study of different topology of transmitter architecture and state-of-art of current work.

2.1.1 Wireless Communication Transmitter

Several architectures can be proposed for wireless communication mobile transmitters depending on the performance requirements (Razavi, 1996, 1999). In direct conversion transmitter architecture, the LO frequency is equal to the output carrier frequency. This topology offers high level of integration due to its simplicity as far as hardware implementation is concern. In a Cartesian-type transmitter, the quadrature *I* and *Q* baseband components are mixed with a quadrature LO signals.

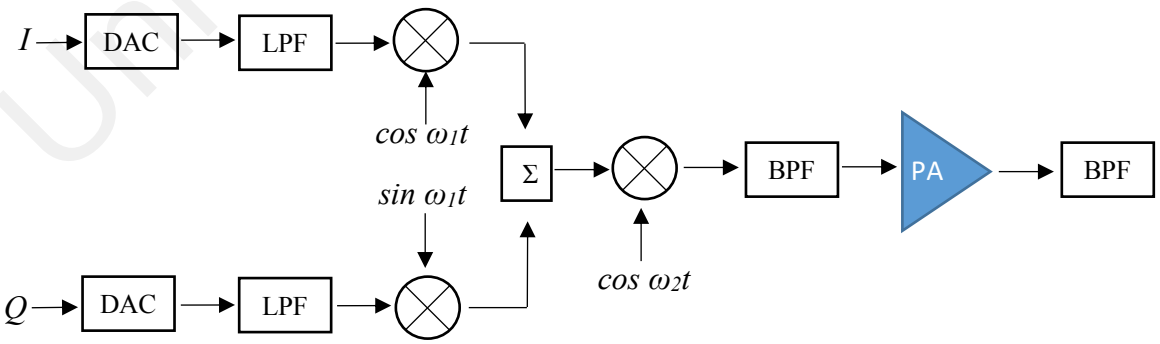


Figure 2.1: Double conversion RF PA line up

In this case, the baseband components are usually generated in the digital domain followed by the digital-to-analog converters (DAC) and LPF to provide delivery of the analog baseband signals to low-frequency inputs of the mixers. The upconversion can be done in one or two steps. Figure 2.1 shows the superheterodyne transmitter with two-step upconversion where the modulation is done at IF frequency and then subsequently upconverted to the transmitting frequency by an RF mixer. This architecture requires a significant amount of circuitry, which usually includes both the low-pass IF and bandpass RF filters to properly suppress noise and spurious components. In addition, to provide a significant dynamic range of output powers up to 80 dB depending on the communication standard, it is necessary to apply the variable power control scheme directly at RF prior to the PA. The direct-conversion architecture shown in Figure 2.2 minimizes the number of circuit blocks providing the best compromise of performance versus power consumption and circuit complexity (Loke & Ali, 2002) . However, it may require an RF SAW filter to suppress noise floor in the receiver band before feeding the signal into the PA. Also, direct-conversion transmitters suffer from any mismatch in the phase and amplitude of the baseband signals, and any dc offset in the baseband signal can result in LO leakage to the output, thus degrading the transmit signal quality. In both architectures, the PA requires a good linearity, compromising the overall transmitter efficiency and complicating output power control.

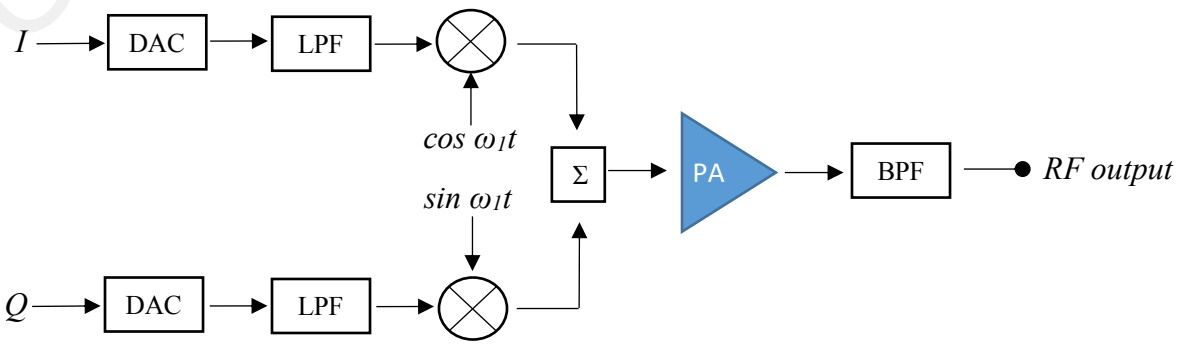


Figure 2.2: Direct conversion RF PA line up architecture

The PA output is a high power signal and in a modulated waveform which centered around LO frequency. Eventhough there many isolation techniques which can be deployed such as shielding, the high output power still interfere the LO spectrum. In some circumstances where the noise frequency is near to LO natural frequency, the output will be disturbed tremendously as the magnitude of noise increase rapidly. Eventually when the noise is as low as 40 dB below the oscillation level, the noise frequency is locked and create major disturbance. This phenomenon can be fixed if the PA output frequency has a higher isolation or far from the LO frequency

2.1.2 Two Step Architecture

The LO pulling issue in direct conversion topology can be avoided by upconverting the baseband signal in two or more steps to ensure the PA output frequency is isolated from the VCO frequency. As shown in Figure 2.3 below, the baseband signals (I & Q) undergo a quadrature modulation at low frequency, ω_1 or intermediate frequency (IF).

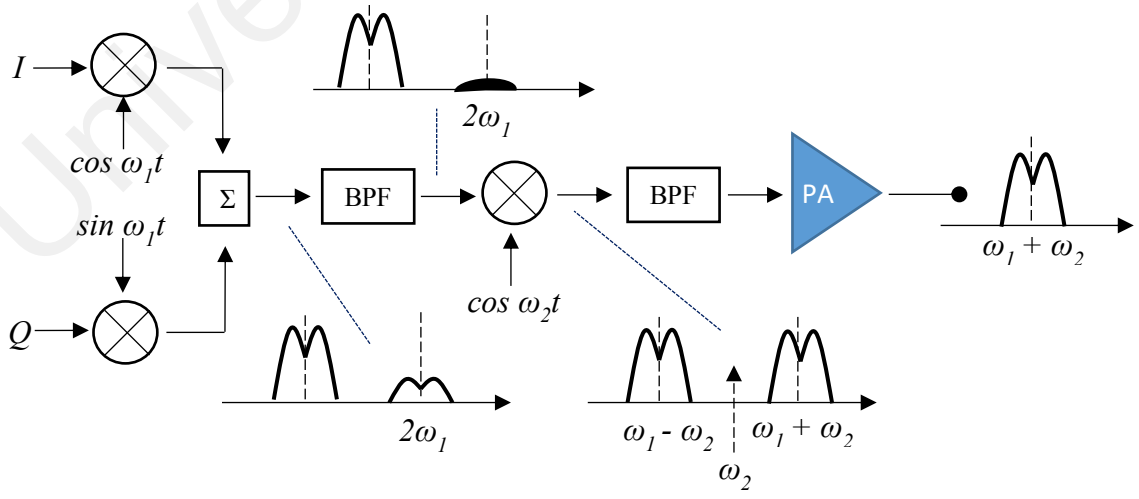


Figure 2.3: Two step transmitter architecture

The output is upconverted to $\omega_1 + \omega_1$ through mixing and band pass filtering. The pre band pass filter (BPF_1) will suppress the harmonics of the IF signal whereas the post band pass filter (BPF_2) removes the unwanted sideband spurious emission centered at ω_1 - ω_1. Since the quadrature modulation is performed at low frequencies, I and Q matching is ideal which reduces the cross-talk issues between two channels. This topology takes an advantage over the direct conversion architecture. The challenging part of this approach is that the post bandpass filter at the second up conversion must reject the spurious emission or unwanted sideband signals by typically 50 to 60dB. A high rejection is indeed needed because the signal mixing process produces both wanted and unwanted signal with equal magnitude.

2.1.3 Single Sideband Transmitter

Single sideband transmitter is constructed by letting the output of carrier suppression system to pass through series of filter circuits that are selective to transmit one sideband frequency while suppressing the other. The challenge in designing such transmitter topology is that the filters should have a very effective rejection. As in practical design, even with a well designed filters, such effective rejection or sharp roll off is possible only if carrier frequency is low enough. Having said that, the filter method is suitable for relatively low or moderate carrier frequency.

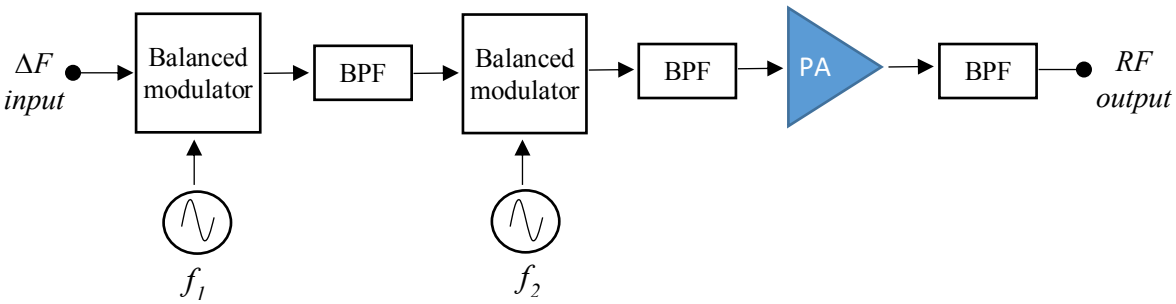


Figure 2.4: Single sideband transmitter block diagram

For an application where the sideband is designed to be located at high frequency spectrum, then it must be translated in frequency by heterodyne step which results in multiple conversion transmitter architecture mostly based on the discrete band and broadband methods.

The SSB transmitter can generally provide a capability of multichannel transmission. Its two-channel structure is shown in Figure 2.3 (b), where *N*1 and *N*2 are the audio modulating signals of the first and second channels, respectively. At the output of the first balanced modulators, the high sideband is selected by one filter and the low sideband is selected by another filter. Then, both these sidebands are combined and translated to higher frequencies by the second balanced modulator followed by the filter whose passband must include both telephone channels.

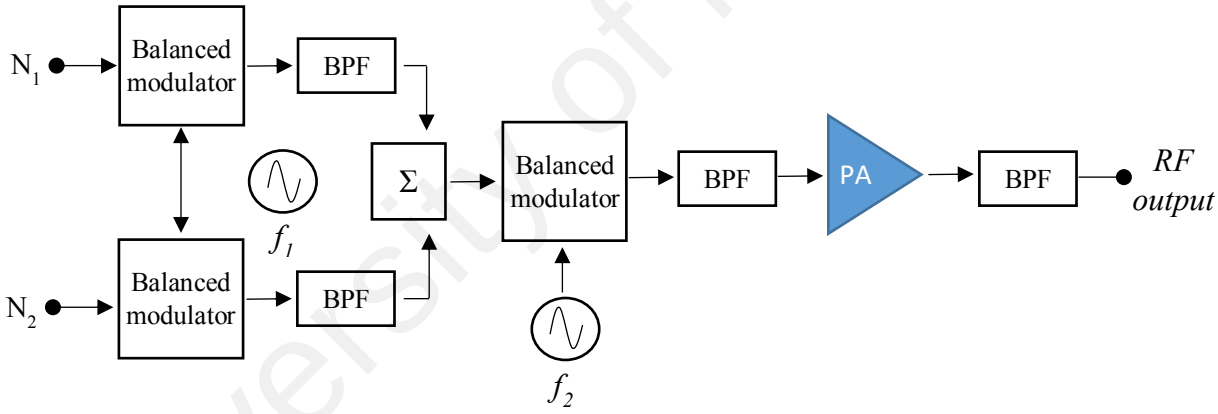


Figure 2.5: Single sideband transmitter with multichannel transmission

2.1.4 Ultra Wideband (UWB) Communication Transmitter

UWB technology was mainly used for radar-based applications because of the wideband nature of the signal that results in very accurate timing information. By the early 1970s, the system concept and basic components such as pulse train generators and modulators, detection receivers and wideband antennas were available (Reed, 2005). However, due to recent developments in high-speed switching and narrowband pulse

generation technology, UWB has become more attractive for low-cost communications applications, representing many wireless transmission scheme that occupies a transmission frequency bandwidth of more than 20% of a center frequency, or more than 500 MHz (Roy, Foerster, Somayazulu, & Leeper, 2004).

Such large bandwidths are achieved by using very narrow time-duration baseband pulses of appropriate shape and duration, including the family of Gaussian shaped pulses and their derivatives. Larger transmission bandwidths are preferred to achieve higher data rates without the need to increase transmitting power, resulting in the ability for increasingly fine resolution for multipath arrivals, which leads to reduced fading per resolved path since the impulsive nature of the transmitted waveforms prevents significant overlap and, hence, reduces possibility of destructive combining. A key advantage of UWB designs is that highly linear PAs are generally not required because the UWB pulse generator need only to produce a peak-to-peak voltage swing on the order of 100 mV to meet spectral mask requirements that can

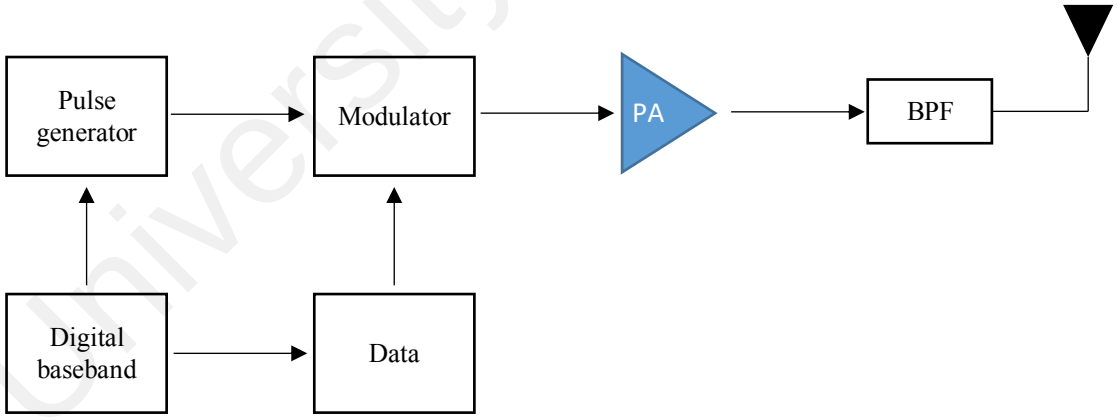


Figure 2.6: Generic UWB transmitter architecture

2.1.5 Closed Loop Adaptive RF PA Line Up Architecture – State of art

Next generation two-way radio communication systems require an adaptive power adjustment to achieve optimum efficiency over wide dynamic power level and fast transient timing response while meeting the adjacent channel transient power ACTP (as recommended by communication bodies). Both need stringent approach due to the regulatory requirements.

A novel technique of gain stage controlled with logarithmic detector to provide accurate RF input drive tracking is proposed in this work (Narendra, Mediano, Paoloni, & Limiti, 2008), [5]. Driver amplifier gain control and the logarithmic RF power detector circuitry enables an accurate input RF drive to the final PA in order to achieve constant efficiency across wide power levels. As far as voltage controlled current source (VCVS) of LDMOS device is concerned, the output RF output from the device will grow up with incremental of the gate bias voltage. Therefore, an analytical explanation with regards to PA current sense tracking accuracy and the transient response of the closed-loop integrator with voltage shaping algorithm are discussed. In terms of practical realization, the PA design is based on the current sensing with integrator and gate voltage shaping algorithm (Prakash C., Narendra K., 2004). This design offers fast transient power response with good ACTP performance. In addition to accurate tracking, this topology offers low cost implementation. However, there are several sensing mechanism that are been implemented in real products, including power and VSWR sensing (Kosaka et al., 2014) (Serhan, Lauga-Larroze, & Fournier, 2015) with huge space and cost requirements. In addition, measurement challenges associated with the closed-loop RF PA system design to meet two-way radio stringent requirement particularly constant efficiency over wide dynamic power level and adjacent channel transient power (ACTP) in small form factor design are discussed. The proposed work also offers low cost implementation for public safety product portfolios. Adaptive power requirements in two-way radio

applications refers to change in output power level in accordance to communication distance. Low output power is sufficient for shorter communication distance but for longer distance, higher output power is required.

Due to this requirement, to maintain constant efficiency over the wide output power level and achieve longer battery life is a real challenge. In conventional two-way radio design, the VCO output signal is typically fixed. Therefore, to maintain constant efficiency for the wide output power level and lower ACTP level as well as longer battery life when the PA line up is operating at low output power are indeed challenging. More detail on the architecture will be discussed in Chapter 5.

2.2 High performance power amplifier design methodologies

In consideration of transmitter design, it is appropriate to recall briefly the design perspective of RF power amplifier (RFPA) design methodologies. In general, RFPA requires an accurate active device modelling, impedance matching depending on the technical requirements and operation conditions, stability in operation, and simplicity in practical implementation. Today's wireless systems impose challenging requirements on PA design. Initially, the PA is considered in the context of a radio transmitter. Then several performance metrics, like output power, drain efficiency, and power-added efficiency, of a PA are introduced, which are then followed by a description of PA classes and how they operate. The PA classes covered are the transconductance amplifiers, like class A, AB, B, and C, and the switched mode classes D, E, and F.

Power amplifiers are widely used in wireless communication applications and radar applications. Due to the variety of applications, there is a great variety of requirements for power amplifiers. Some of the most basic requirements in power amplifier design include frequency of operation, output power level, bandwidth,

efficiency, gain, linearity, size, and cost. It is almost never possible to simultaneously maximize all design criteria at the same time. Thereby trade-offs must be made, and only a subset of the requirements can be satisfied. Some of the classic tradeoffs include: gain vs. bandwidth, operating frequency vs.output power, and linearity vs. efficiency.

A typical attempt to optimize a subset of design criteria is the introduction of different classes of power amplifiers. It is worth noting that there are a lot of confusion and debates over the classification of power amplifiers. Some classes overlap others; some classes can be thought of as a limiting case of other amplifiers. Nevertheless, the current classification gives a good starting point for basic understanding of these amplifiers. As knowledge of power amplifiers accumulates, many different classes of power amplifiers have evolved over the years. Generally speaking, power amplifiers are divided into two types: transconductance amplifiers and switching-mode amplifiers. Conventional transconductance amplifiers include Class-A, Class-AB, Class-B, and Class-C amplifiers. Conventional switching-mode amplifiers include Class-D, Class-E, and Class-F amplifiers. Each of the power amplifier classes optimizes a certain subset of design criteria. While some classes of amplifiers have advantages over other classes, they also have disadvantages. Several classes of amplifiers attempt to combine advantages of two different classes. These classes are typically denoted as "Class-XY" amplifiers. Some examples of these intermediate classes of amplifiers include: Class-BD (F. H. Raab, 1977), Class-CE (M. K. Kazimierczuk & Tabisz, 1989), and Class-DE (Koizumi et al., 1996). Another class of amplifiers combines the advantages of Class-E and Class F amplifiers, and it is called the Class-E/F amplifiers. This particular class was invented by Scott Kee at Caltech (Kee, Aoki, Hajimiri, & Rutledge, 2003).

The classic tradeoff between the transconductance amplifiers and switching-mode amplifiers are linearity and efficiency. While Class-A amplifiers are the most linear power

amplifiers, they can achieve a maximum efficiency of 50%. Switching-mode amplifiers can achieve an ideal efficiency of 100%, but they are strongly nonlinear amplifiers. Class-AB, Class-B, and Class-C amplifiers are compromises in between as shown in Figure 2.6.

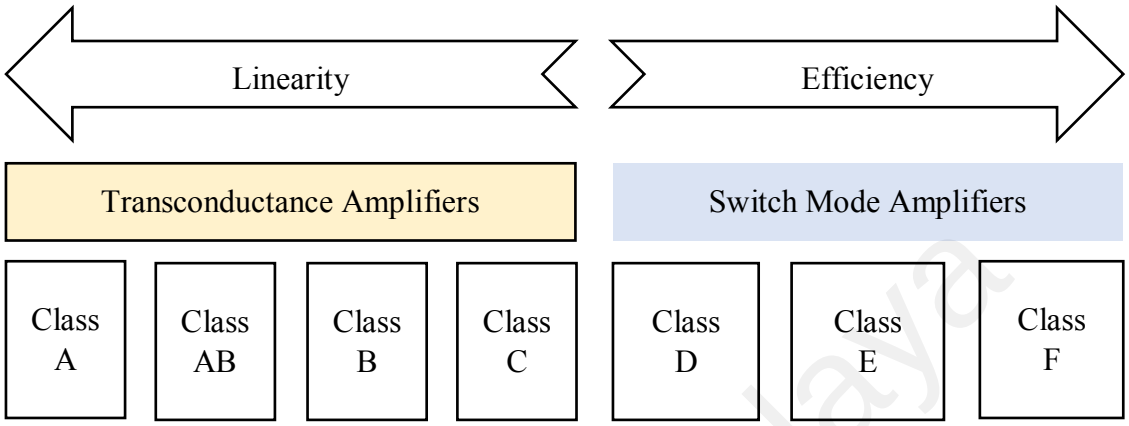


Figure 2.7: The linearity-efficiency tradeoff between transconductance amplifiers and switching-mode amplifiers

The problem is that many applications require that high linearity and high efficiency be achieved at the same time. Naturally, some PA designers choose to start from the left side of Figure 2.1 and use a Class-A or a Class-AB amplifier as the starting point, and then try to find a solution to improve efficiency without compromising the linearity. Some other PA designers choose to start from a switching-mode topology of the amplifier with high efficiency, and then investigate complicated linearization techniques. These techniques include Envelope Elimination and Restoration (EER) technique (Kahn, 1952) (F. H. Raab, 1987) (F. H. Raab, Sigmon, Myers, & Jackson, 1998) (F. H. Raab, 1996), Doherty (Doherty, 1936) (Jeonghyeon, Jangheon, Bumman, Jong Sung, & Sang Hoon, 2004), Chireix (F. Raab, 1985) (Hakala et al., 2005) and even digital pre- or post-distortion techniques (Sperlich, Sills, & Kenney, 2003) (Horiguchi et al., 2004) (Sperlich, Park, Copeland, & Kenney, 2004). These techniques are beyond the scope of the thesis. Since the power amplifiers described in the thesis will be used in applications where highly

nonlinear effects can be tolerated, we will only focus on the techniques that improve the efficiency of the amplifiers. D-1

Two of the most noteworthy schools of high-efficiency PA design are: (1) voltage and current waveform shaping using time-domain techniques, as in Class-E amplifiers; (2) voltage and current waveform shaping using frequency-domain or harmonic-tuning techniques as in Class-F amplifiers. It is important to look beyond the class nomenclature, and often it is easier to understand the newer techniques based on these two theories. In this chapter, several typical classes of power amplifiers are reviewed. Discussions emphasize on high-efficiency design techniques used in switching-mode amplifiers. In this thesis, only common-source or common-emitter configurations are considered.

2.3 Transconductance power amplifiers

Transconductance power amplifiers are extensions from linear transconductance amplifiers. These amplifiers use active transistors as controlled current sources. Class-A, Class-AB, Class-B, and Class-C amplifiers are conventional transconductance amplifiers. They are widely used in today's wireless transmitters, and they have been discussed in detail in several books (Krauss, Bostian, & Raab, 1980) (Cripps, 2006) (M.K. Kazimierczuk, 2014)

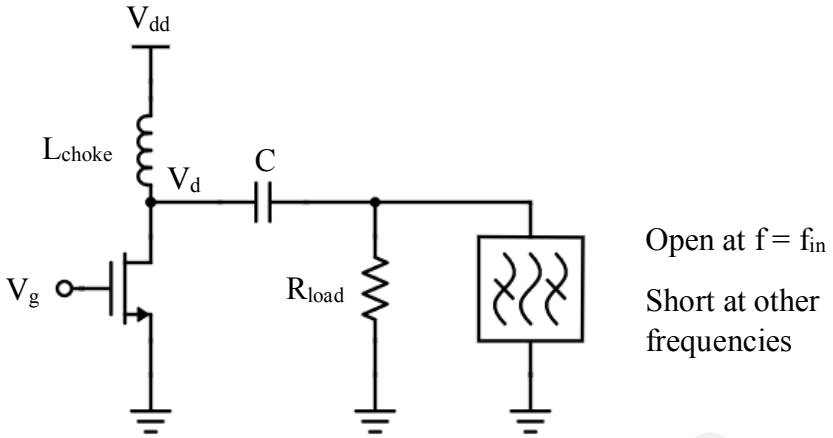


Figure 2.8: Circuit diagram of Class-A, Class-AB, Class-B, Class-C amplifiers

2.3.1 Class A amplifiers

The most simplistic way to distinguish these classical transconductance amplifiers is theconduction angle. Class-A amplifiers have a conduction angle of $\theta C = 2\pi$; Class-AB amplifiers have a conduction angle of $\pi < \theta C < 2\pi$; Class-B amplifiers have a conduction angle of π ; Class-C amplifiers have a conduction angle of $0 < \theta C < \pi$. Figure 2.3 shows the voltage and waveforms of a Class-A amplifier. The Class-A amplifier is the most linear and the most "well-behaved" amplifier.

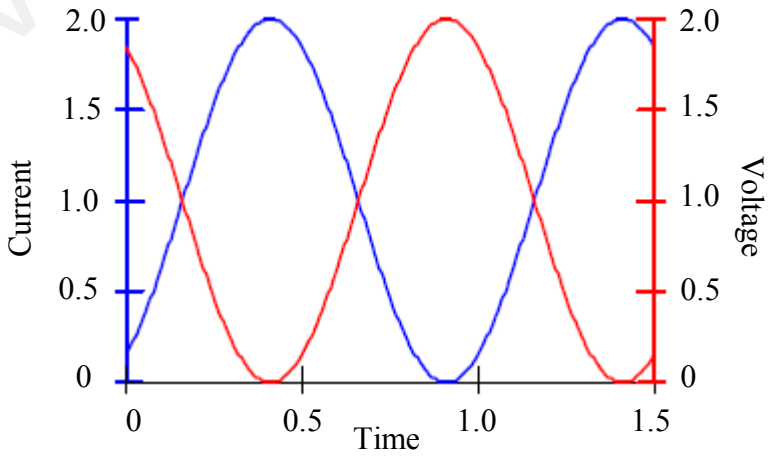


Figure 2.9: Class-A voltage and current waveforms.

However, the biggest drawback of the Class-A amplifier is the ideal maximum efficiency of 50%. This efficiency number, in practice, is reduced significantly to about 35% for Lband applications. Let us take 33% drain efficiency as an example. If the output power of the amplifier is 100 W, the total power consumption of the power amplifier is 300 W, and 200 W is dissipated power. This number is usually well beyond the heat-handling capability of a common-source transistor package. This is the reason why Class-A amplifiers are not suitable for L-band high-power amplifiers.

In today's technology, the use of Class-A amplifiers is only popular at high microwave frequency beyond 5 GHz up to millimeter-wave territory. The advantage of the Class-A amplifier at higher frequency range is that it requires considerably less drive power and has higher gain than other classes of power amplifiers. Since at higher frequency, the power gain is usually the limiting factor in PA design, Class-A is much more suitable.

2.3.2 Class B, Class AB and Class C amplifiers

The voltage and the current waveforms of a Class-AB amplifier are shown in Figure 2.4. Since the gate bias level is reduced from Class-A amplifier, the current clipping occurs. Although current clipping generates harmonics and nonlinear effects, Class-AB amplifiers are popular candidates for L-band power amplifiers. Higher efficiency than Class-A amplifiers can be obtained without much compromise in the power gain and the linearity. Many PA designers use Class-AB amplifiers as a starting point, and apply harmonic control techniques to improve efficiency. These techniques are discussed in the later part of the chapter.

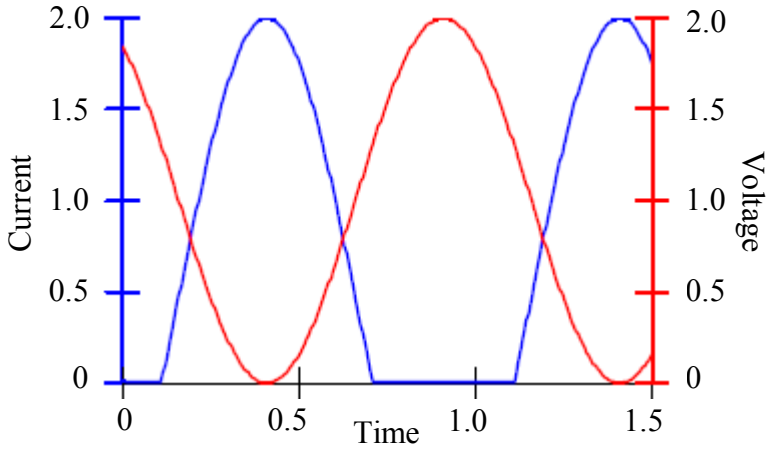


Figure 2.10: Class-AB voltage and current waveforms

We can look at a Class-B amplifier as a transition between a Class-AB and a Class-C amplifier. The ideal maximum drain efficiency of a Class-B amplifier is 78.5%, which is significantly higher than the Class-A amplifier. Practically, an L-band high-power Class-B amplifier can achieve a drain efficiency of 60%. If we take the same case as before, we see that for an output power of 100W, a practical Class-B amplifier only dissipates about 60W of power. We can easily see that is a great reduction from 200W in the Class-A case.

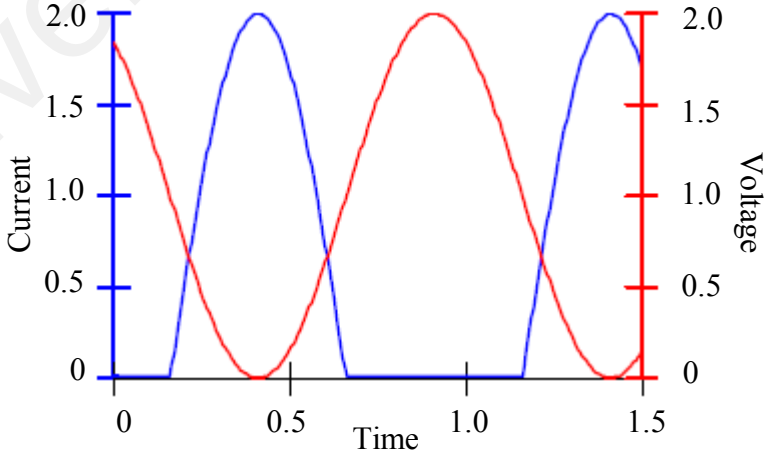


Figure 2.11: Class-B voltage and current waveforms.

Class-C amplifiers are high-efficiency amplifiers, with an ideal efficiency of 100%. However, there are several problems for an L-band Class-C implementation. The first drawback of this amplifier is the efficiency comes at the expense of the power gain. In fact, in the classic definition of Class-C amplifier, the output power approaches to zero, as the efficiency approaches to 100%. At microwave frequency, this approach is typically not desired, since high power gain is difficult to obtain. The second drawback is that the amplifier is highly nonlinear, so it can be used only in applications that can tolerate a high degree of nonlinearity, or it must be used with linearization techniques.

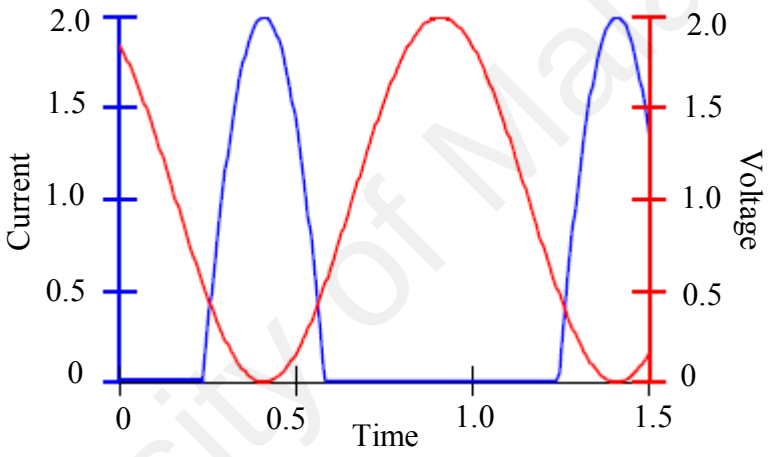


Figure 2.12: Class-C voltage and current waveforms

2.4 Switching mode power amplifiers

Switching-mode power amplifiers use active transistors as switches. That is, the active device is ideally fully on (short-circuit) or fully off (open-circuit). These circuits are commonly found in switching power supplies, but only recently have they been exploited as RF amplifiers due to the availability of transistors with substantial gain and power at microwave frequencies. The theoretical efficiency for Class-E and Class-E/F amplifiers is 100%; practical efficiencies of 70-90% have been demonstrated at VHF and UHF frequencies (Kee, Aoki, & Rutledge, 2001) (Sokal, 1998). In ideal switching-mode

amplifiers, the transition between the on-state and the off-state can be achieved instantaneously. The switching-mode amplifiers differ from the traditional classes of amplifiers, which use the active devices as controlled current sources. Since ideally the device is either fully on or fully off, the voltage and the current will never be nonzero simultaneously as shown in Figure 2.7. Therefore, ideally no power is dissipated, and the efficiency is 100%. This theoretical number is significantly higher than the traditional Class-A and Class-AB amplifiers. To optimize the efficiency, we need to reduce the overlap between the voltage and the current. In fact, we see that from the transconductance amplifiers already. If we compare the voltage and the current waveforms from the four different transconductance classes discussed in the previous section, we see that in Class-A amplifier, the current and the voltage are both non-zero at all time, and the Class-A amplifier has the lowest efficiency; Class-C amplifier has the highest efficiency due to the least overlap between nonzero voltage and current region.

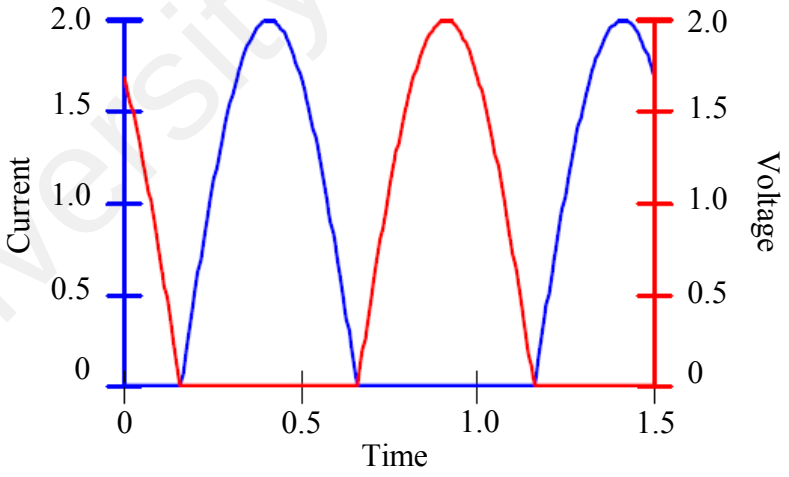


Figure 2.13: Sample voltage and current waveforms for an ideal switching-mode amplifier

Note that the current and the voltage do not overlap. To see how to achieve no overlapping between the voltage and the current, we will start from one of the simpler approaches of switching-mode amplifiers- Class-D amplifiers.

2.4.1 Class D amplifiers

Class-D and Class-D-1 (also called inverse Class-D or current-mode Class-D) amplifiers use two active devices driven as switches at 180 degree out of phase (in a push-pull configuration). The load circuit consists of a band-pass or a band-stop filter. Class-D amplifier's band-pass filter has a short circuit at the fundamental frequency and an open circuit at other frequencies. The voltage waveform is a square wave, while the current waveform is sinusoidal.

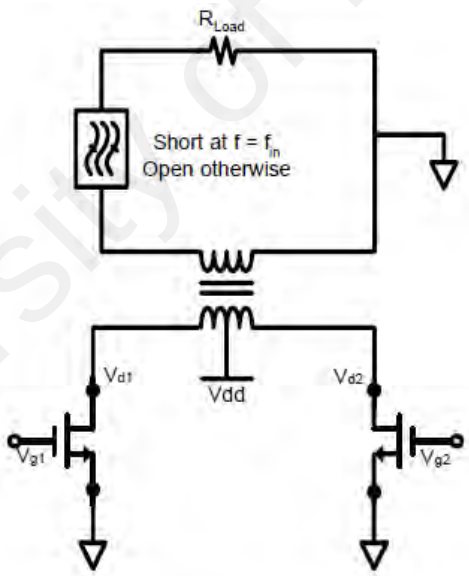


Figure 2.14: Schematics of Class-D

The waveforms of Class-D are shown in Figure 2.15.

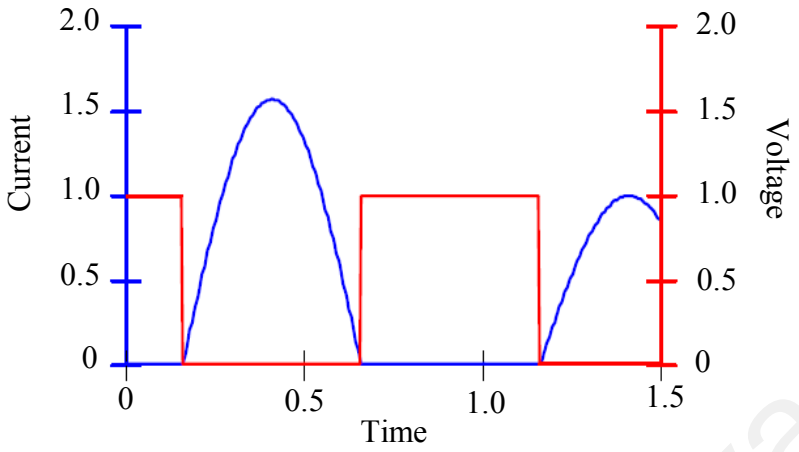


Figure 2.15: Voltage and current waveforms of Class-D amplifiers

Under ideal conditions, Class-D can achieve 100% efficiency. However, one of the assumptions of Class-D amplifiers is that the transistors have zero output capacitance. In high-power amplifiers, the devices are typically large in size, and thereby having a large output capacitance. The susceptance of the output capacitance also increases with frequency, so at UHF and microwave frequencies, the effect by the output capacitance cannot be ignored. In Class-D configuration, the loss due to large output capacitance can be very large in microwave frequency, thereby the use of this type of power amplifiers are mostly limited to audio amplifiers.

It is also assumed that in Class-D amplifiers, the transistors behave as switches, which can be toggled between ON state and OFF state instantaneously. This is certainly not the case in microwave transistors. Within the finite turn-on and turn-off time, the voltage and the current waveforms overlap, and increase the transistor loss. This drawback is addressed in the time-domain design and analysis in Class-E amplifiers.

2.4.2 Class E amplifiers

The Class-E amplifiers were invented by N. O. Sokal and A. D. Sokal (Sokal & Sokal, 1975). The Class-E amplifier consists of a single-ended transistor as a switch with an output load circuit. The output load circuit has a series resonant circuit at the fundamental frequency along with load impedance which is tuned slightly inductive. This basic circuit is shown in Figure2.10.

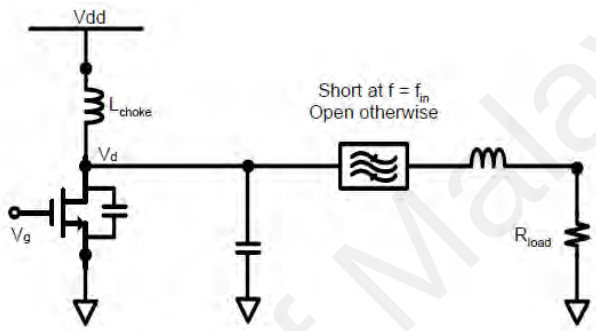


Figure 2.16: Circuit schematic of a Class-E amplifier

The main advantages of Class-E amplifiers are: (1) "soft-switching" to reduce loss, (2) "absorption of output capacitor" in the output circuit, (3) relatively simple circuit compared to Class-F amplifier.

Since the switching time of the transistors is not instantaneous, a Class-D amplifier suffers power loss due to the voltage and the current are simultaneously nonzero. At microwave frequency, the switching time may be a significant fraction of the cycle, and the loss may be too great to tolerate. This adverse effect can be significantly reduced in Class-E tuning, when the inventors include an inductive load. From the time-domain waveform of the voltage, Class-E tuning reduces the slope of the voltage waveform before the switch turns on. This feature, sometimes referred to as soft-

switching or zero-voltage-derivative switching (ZdVS), minimizes the level of the voltage during the turn-on of the switch. Another beauty of Class-E amplifier is the relatively simple circuit topology for an easy implementation. Also, unlike Class-D amplifiers, which assume a zero output capacitance of the active device, Class-E amplifier design equations take into account the output capacitance.

The Class-E amplifier is not quite the perfect solution for high-efficiency PA. The amplifier suffers from relatively high peak voltage and high rms current. Also the efficiency of the amplifier reduces significantly as the output capacitance of the transistor becomes large.

2.4.3 Class F amplifiers

Class F power amplifiers based on waveform shaping using multiple harmonic resonators. To the first order, this is a frequency-domain technique compared to the time-domain technique of Class-E amplifiers. The amplifiers achieve high efficiency by shaping the drain voltage or drain current waveforms using these harmonic open or short circuits shown in Figure 2.11.

The ideal waveforms of a Class-F amplifiers are very similar to those of a Class-D amplifiers shown in Figure 2.9. If we take the Class-F-1 as an example, it has low peak voltage, so the amplifier can be operated in a higher bias voltage without exceeding the breakdown voltage of the transistor. This improves the output power level of the amplifier. The current waveform has a lower rms value, which reduces the resistive loss of the transistor, and in turn improves the efficiency.

We can look at Class-D-1 amplifiers as a special implementation of the Class-F-1 amplifiers. The reason for this similarity is symmetric topology of Class-D-1 design. At the line of symmetry, the switch is terminated with virtual short circuits for odd harmonics, and the switch is terminated with a virtual open circuit for even harmonics. In

practice, the output capacitance of the transistor cannot be omitted. In this case, the even harmonics are being terminated with the output capacitance. This causes undesired effects, which will be discussed in the next section.

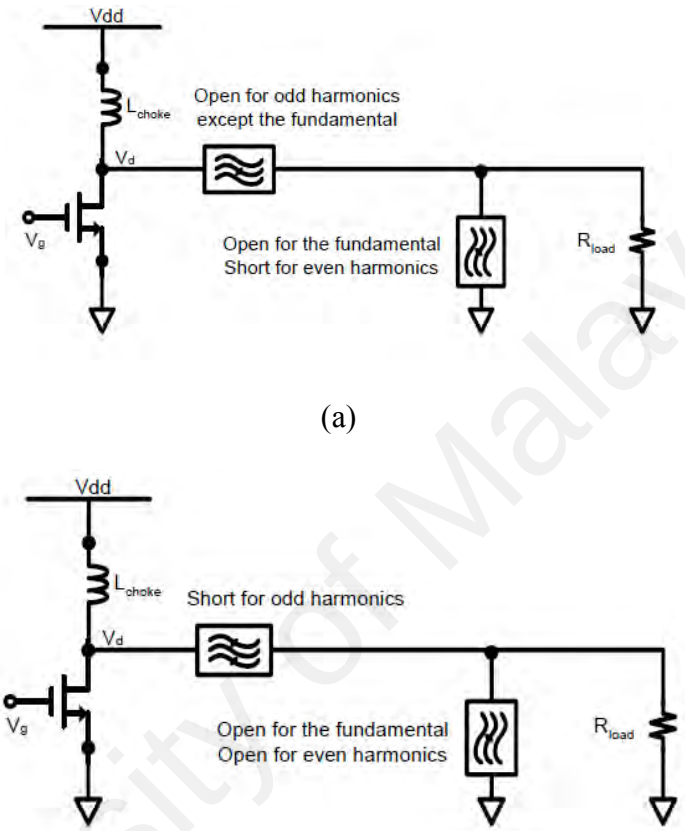


Figure 2.17: The circuit schematics of (a) Class-F and (b) Class-F-1 amplifiers.

(Waldstein, Kortright, & Simons, 2017)

It is also clear from the schematic in Figure 2.11 that the circuit requires infinite number of harmonic-control circuits to achieve the ideal Class-F tuning. In practice, it translates into a complex circuit, which is difficult to implement. A solution to achieve desired harmonic tuning with simple circuits like Class-D and Class-E amplifiers is in the next section.

CHAPTER 3 :
HIGH POWER BROADBAND LDMOS RF POWER AMPLIFIER DESIGN

3.1 Overview

This section highlights achievement of broadband high performance power amplifier (PA) line up for mobile two-way radio applications. In typical two-way radio applications the input RF signal to the first PA stage comes directly from the VCO (voltage controlled oscillator), with typically 3 dBm power. Due to high output power requirement (~80 W) of mobile radio applications, up to three PA device stages are normally cascaded (pre-driver, driver and final PA stage). The key point in the design of the PA line up concerns the final stage. Here, this section introduces a design methodology based on parallel-combined impedance matching technique (from theoretical derivation) enables the designers to develop broadband PA with actual PA device impedance (implementation of new generation LDMOS device).

3.2 Introduction

Modern mobile two-way radio communication must meet high performance and robustness criteria in the field. One of the key challenges in system architecture is the transmitter chain, specifically the PA line up. In order to meet high performance and robust design, while minimizing costs of the whole transmitter chain, power device selection and circuit topology should be carefully analyzed. In typical two-way radio applications, a constant pre-defined envelope modulated Radio Frequency (RF) signal (either Frequency Modulation or Frequency Shift Keying) is injected directly from the VCO to the PA. Due to low signal level from VCO (~3 dBm) and high output power requirements of the two-way radio product up to three PA device stages are normally cascaded, i.e. the PA consists of pre-driver, driver and final PA stage. The key focus of

this thesis is the final PA design stage, particularly, final PA output impedance matching transformation having parallel combining technique (Yoo, Kim, Kim, & Yoon, 2010) (J. Kim et al., 2011) (from analytical approach), followed by the design methodology employing source and load-pull technique (Ghannouchi & Hashmi, 2011) (Cripps, 2002), and implementation of high power new generation LDMOS device technology. Practical design concept to meet thermal management is taken into consideration (heat-sink design) (Naz, Naeem, Farooqui, & Shah, 2012) (Yu, Buttay, & É, 2017)

Bandwidth limitation in designing a broadband amplifier can be addressed through circuit design and device characteristics (Pennisi, Scotti, & Trifiletti, 2012). Broadband amplifiers need to be designed over a broad frequency range which indeed requires proper matching networks. This is to ensure a reasonable compensation for the variations of forward transmission S_{21} with frequency. Common techniques used to design broadband amplifiers are matching network compensation (J. Kim, Hoyos, & Silva-Martinez, 2010), negative feedback (Gruner, Sorge, Markos, Bengtsson, & Boeck, 2010), etc. Matching network compensation involves mismatching the input and output networks to compensate the changes with $|S_{21}|$, and the networks must provide the best input and output VSWR (Cripps, 2006) (Quaglia & Cripps, 2018).

Large-scale RF and microwave power device production is actually based on Silicon (Si), Gallium Arsenide (GaAs), Lateral Diffusion MOSFET (LDMOS) (Barbieri & Noori, 2013), (Gruner, Sorge, Bengtsson, Tanany, & Boeck, 2010) (Maassen, Rautschke, Huellen, & Boeck, 2016) (Berrached, Bouw, Camiade, & Barataud, 2013). In addition, great research interest is devoted to high power density devices using wide-bandgap materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) (Florian, Cignani, Santarelli, Filicori, & Longo, 2013) (S. Chen, Reese, & Nguyen, 2012) (Hui, Bathich, Bengtsson, & Boeck, 2010). A higher bandgap corresponds to a higher breakdown field, which in turns implies the capability of the device to allow higher output

voltage swings and thus attain higher output power levels. Moreover, high breakdown voltage results in larger output impedance values for a given current density, making the device matching easier for broadband applications (Waldstein et al., 2017). Therefore, the selection of high f_τ-V_{bk} device technology is a good solution (Waldstein et al., 2017). GaN devices offer a superior power density. Reasonable power can be obtained from comparatively small GaN devices with high source and load impedances and complexity of the matching networks can be reduced. However, they have the drawback of running with high supply voltage values. Typically 28 V or higher supply voltage will be used for GaN devices (Hui et al., 2010). For mobile radio communications, 13 V is a favorable voltage due to the fact that the product can be used in automobile. In this regard, LDMOS would be an interesting choice.

In this work, a new prototype has been designed and fabricated with a demonstrated drain efficiency of 55% at operating power of 80 W for frequency range of 760-870 MHz. Note that three PA stages are cascaded (pre-driver, driver and final PA stage) and overall gain reported more than 45 dB across frequency. The final PA stage has been built with new high power LDMOS device technology process from Freescale Inc. Additional performance test such as stability and robustness are carried out in laboratory. Power amplifier is very stable and the transistor was not damaged by operating into 10:1 VSWR termination (with varying phase angle of the load termination). This amplifier demonstrated high energy conversion (high efficiency) with 13 V DC supply (operating at 80 W) in UHF broadband frequency. Additionally, the amplifier requires small size area form factor and has a low cost implementation which is suitable to be integrated in mobile two-way radio applications.

3.3 Circuit Principle

3.3.1 LDMOS Characterization and Selection

To achieve broadband performance from a single ended PA device, the load impedance $R_{L,opt}$ must be close to ~50 Ω over wide frequency range.

$$R_{L,opt} = \left[\frac{(V_{bk} - V_k)^2}{2P_{out}} \right], \tag{3.1}$$

P_{out} is output power from the device, where V_{bk} *and* V_k are breakdown and knee voltage, respectively. Therefore, scaling the device periphery is possible to achieve $R_{L,opt}$ ~50 Ω by means of DC voltage. But this may imply lower output power. One can increase output power with the increase of DC voltage while keeping $R_{L,opt}$ ~50 Ω. In this work, low DC supply of 13 V is selected due to product design requirement. Therefore, when PA device is running at 13 V (can be approximated to V_{bk} - V_k) and delivering P_{out} of 90 W, the $R_{L,opt}$ will be approximately ~0.9 Ω. As a matter of fact, the design of a broadband frequency from 760-880 MHz (having loaded quality factor, Q_L of 2) with low DC supply and small $R_{L,opt}$, it is real challenge. As the result, impedance matching transformation network from $R_{L,opt}$ to 50 Ω termination will be complicated.

Due to high output power requirement (~80 W) and using 13 V DC supply, there is no single ended LDMOS PA device available. However, new generation LDMOS device running with 13 V supply, new generation high power LDMOS device (n-channel enhancement lateral MOSFET)) from Freescale Inc. is employed (Narendra et al., 2012). Source and load pull characterization are carried out, where best trade off point between efficiency and output power of 71.8% and 44.3 dBm, respectively are recorded over the entire desired frequency bandwidth, (See Table 3.1). It is a technology limitation to have a highest efficiency, highest output power and highest gain in a single device. Indeed, the efficiency performance (at power of 45 W) of the device is high and combining two

devices in parallel 80 W output power could be reasonable expected. One must take note that impedance matching transformation must be carefully considered here due to the fact that the overall impedance will be divided by half in parallel combination. The principle analysis will be discussed in the following sub-section.

3.3.2 Output Impedance Analysis – Design via Source and Load Pull Determination

Parallel-combining impedance matching (Yoo et al., 2010) (Boaventura, Collado, Georgiadis, & Carvalho, 2014) technique is introduced in this paper to achieve high output power while preserving high efficiency over the broadband frequency operating range. When two PA devices are placed in parallel configuration, both RF current generated from the devices must be carefully combined without having loading effect (Narendra et al., 2012) (M. K. Kazimierczuk, 1992). Let us consider i_1 and i_2 as the current source of each PA device, and $Z_a(\omega)$ and $Z_b(\omega)$ the optimum output impedances of the PA device as a function of frequency (Fig. 3.1 (a)). DC-RF conversion is assumed here, where RF output power of each device is generated from DC source as a function of frequency. One should take note that $Z_a(\omega)$ and $Z_b(\omega)$ are equal if the devices are identical. The following output voltage and current equations can be deduced from Fig. 3.1, for an example $Z_a(\omega)$ and $Z_b(\omega)$, and terminated to single load $Z_{oL}(\omega)$.

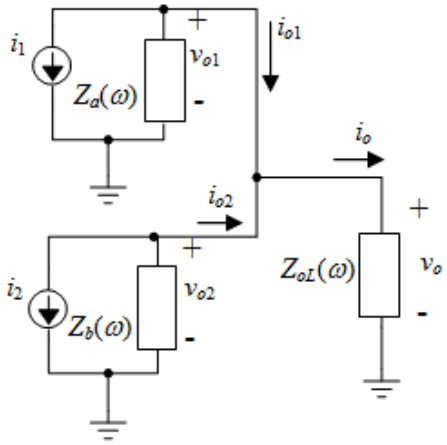


Figure 3.1: Each current source is loaded with the output impedance

$$i_o = i_1 + i_2, \tag{3.2}$$

$$v_o = v_{o1} = v_{o2}. \tag{3.3}$$

Therefore, output RF power can be written as following,

$$P_{o=}0.5\{real(v_o.i_o{}^*)\}, \tag{3.4}$$

$$or \quad P_{o=}0.5\{real((v_{o1}).(i_{o1}+i_{o2})^*)\} \tag{3.5}$$

In frequency domain, RF output power is given as following,

$$P_o = 0.5\frac{{v_{o1}}^2}{real\{Z_{OL}\}} \tag{3.6}$$

$$= 0.5[i_{o1}+i_{o2}]^2 real\{Z_{oL}\} \tag{3.7}$$

where $Z_{oL}(\omega)$ is matched to the impedance terminated due to the present of $Z_a(\omega)$ and $Z_b(\omega)$, in which $Z_{oL}(\omega)$ typically is half of $Z_a(\omega)$ if the two PAs are identical.

From (3.7), to have maximum current combining i_o from i_1 and i_2 contributions, it is important that the magnitude and phase properties of i_1 and i_2 must be controlled with proper termination of $Z_{oL}(\omega)$. Let us analyze this in more detail. Having two current sources in parallel with output impedances, as depicted in Figure 3.2, $Z_{oL}(\omega)$ is the result of injected current source at each active device output (Narendra et al., 2012). Fig. 3.3 is the simplification connection of two devices, represented each by the respective Norton

current source and impedance, (i_1, $Z_a(\omega)$) and (i_2, $Z_b(\omega)$) respectively, and injecting their output in a common node, terminated by $Z_{oL}(\omega)$. Such equivalent description of the device output is valid up to moderate frequencies, where reactive effects (namely the device output reactance) can be neglected, thus considering a purely real output impedance.

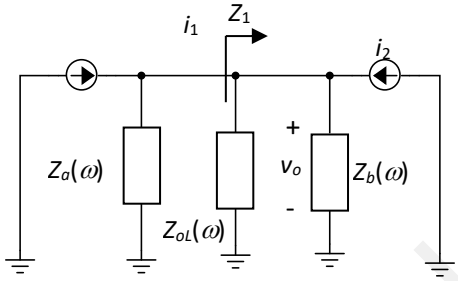


Figure 3.2: Two current sources combining at a single output node

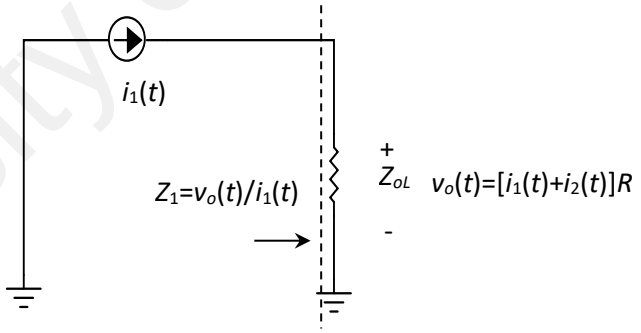


Figure 3.3: Simplification of Fig. 3.1 for understanding of virtual impedance Z_1.

Further, to a first approximation, $Z_a(\omega)$ and , $Z_b(\omega)$ may be neglected, assuming that the device loading effect is not significant when absorbed into the drain line. Such simplifying assumption can be however easily removed by absorbing the device output impedances into the $Z_{oL}(\omega)$, and will be adopted here for the sake of simplicity. The

overall impedance loading each current source, due to the effect of the other injected sources, can be considered as virtual impedance (Narendra et al., 2012)

The resulting current $i(t)$ through the load $Z_{oL}(\omega)$ is the sum of the two sources $i_1(t)$ and $i_2(t)$, represented as

$$i_1(t) = \Re\left\{I_1 e^{j(\omega t+\theta_1)}\right\} = I_1 \cos(\omega t + \theta_1), \tag{3.8}$$

$$i_2(t) = \Re\left\{I_2 e^{j(\omega t+\theta_2)}\right\} = I_2 \cos(\omega t + \theta_2) \tag{3.9}$$

where $\Re$ is the operator providing the argument's real part, I_1 and I_2 represent the magnitudes of the complex current sources and θ_1 and θ_2 are independent phase values. The virtual impedance Z_1 loading the i_1 current source can be obtained by looking into the common node with i_2(t) in parallel with $Z_{oL}(\omega)$ (Narendra et al., 2012),

$$Z_1 = \frac{v_o}{I_1 e^{j\theta_1}} = Z_{OL}\frac{\left(I_1 e^{j\theta_1} + I_2 e^{j\theta_2}\right)}{I_1 e^{j\theta_1}} = Z_{OL}\left[1 + \frac{I_2}{I_1} e^{j(\theta_2-\theta_1)}\right] \tag{3.10}$$

If there is no phase offset or in-phase combining (i.e. $\theta_2 = \theta_1$) is imposed in the DA, the virtual impedance Z_1 is real positive, then,

$$Z_1 = Z_{OL}\left[1 + \frac{I_2}{I_1}\right] \tag{3.11}$$

From (3.11), to achieve optimum performance, one can explain that Z_1 is depending on the magnitude of the both current sources and Z_{oL} for the case of in-phase combining. In other words, the current source must be loaded with appropriate impedance and proper gate biasing to preserve efficiency and high output power operation (for FET devices).

One should take note that in practical application, $Z_a(\omega)$ and $Z_b(\omega)$ will not be considered as high impedance. but this imply much lower as dictated in Table 3.1 (measured source

and load impedance data). The performance is recorded at optimum performance; best efficiency at desired output power. Therefore, knowing the I_1 and I_2, and $Z_{oL}(\omega)$ properties from optimum power performance of the load pull measurement, Z_1 can be determined (Narendra et al., 2010). As explained before, $Z_{oL}(\omega)$ typically is half of $Z_a(\omega)$ or $Z_b(\omega)$ due to identical PA device. As a result, the impedance matching network can be designed to transform from the current source of the PA device to $Z_{OL}(\omega)$. Refer to Appendix A for instruments setup for source and load pull measurement

Table 3.1: Summary of source and load pull measurement characterization of the new generation MV9 LDMOS device over the frequency of interest

Frequency (MHz)	*Drain Voltage* (V)	I_{DQ} (mA)	*Optimum source impedance,* Zs(Ω)	*Optimum load impedance,* Z_L (Ω)	*Pout* (dBm)	*Gain* (dB)	*Efficiency* (%)
740	14	483	0.4 - j1.2	1.2 - j0.5	44.1	20.8	72.5
768	14	483	0.4 - j1.4	1.2 - j0.7	44.1	20.4	72.6
790	14	483	0.4 - j1.5	1.2 - j0.8	43.8	20.5	70.8
806	14	482	0.4 - j1.6	1.2 - j1.1	44.3	19.8	70.9
822	14	483	0.4 - j1.8	1.2 - j1.3	44.3	19.6	71.8
860	14	483	0.4 - j2.0	1.2 - j1.5	43.5	19.5	70.5

3.4 Design Methodology for Final PA Stage

Due to parallel combining technique, two PA units of the new generation high power LDMOS devices are taken into consideration. The input drive signal from VCO is ~ 3 dBm. The overall PA line up architecture is highlighted in this paper, this consists pre-driver (H01 from Freescale Inc.) and driver stage (MRF1507 from Freescale Inc.) amplifiers as well. Both are LDMOS medium power devices. Therefore, one can expect the operating gain of the PA line up can hit more than 45 dB. The PA architecture line up

is shown in Fig. 3.4. Direct matching technique was used for inter-stage matching between PA stages. The section will focus on the output final PA stage impedance transformation to 50 Ω load termination.

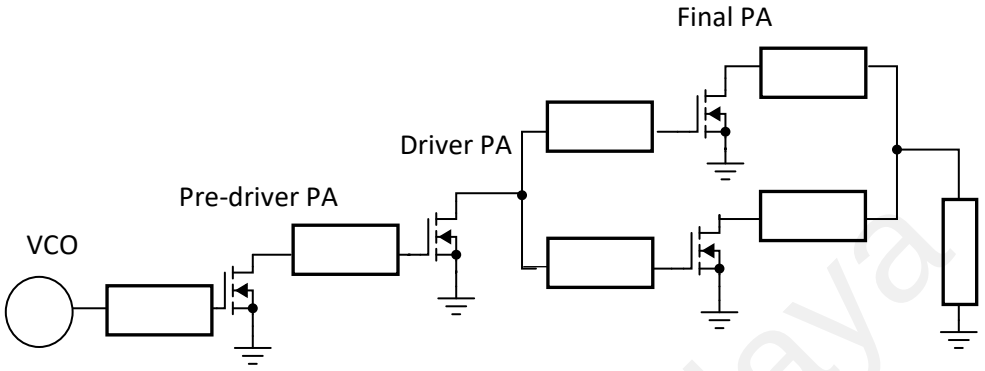


Figure 3.4: Complete PA architecture line up. Direct matching technique will take place between pre-driver and driver PA, and driver PA to final PA

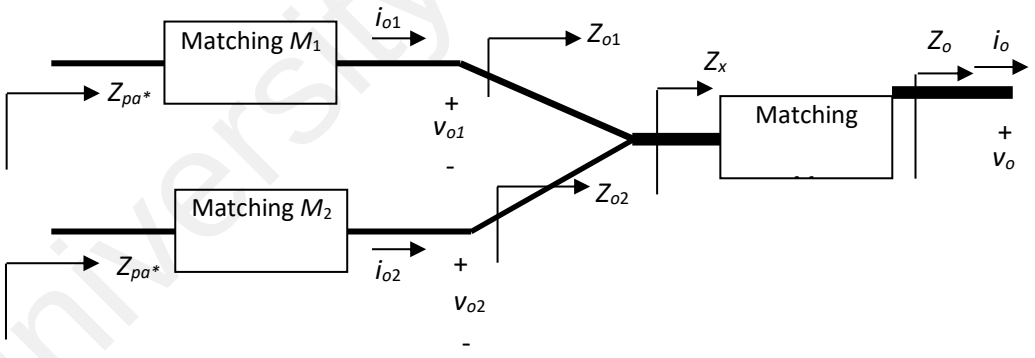


Figure 3.5: Impedance matching transformation of two devices in parallel

Design methodology with parallel-combine impedance matching technique will be discussed here, where two PA devices are placed in parallel configuration (refer to Figure 3.5). Two primary impedance transformation networks are important, M_1 and M_3, since M_1 and M_2 are typically similar. The first network M_1 transforms from the PA optimum

impedance $Z_{pa}^*(\omega)$ to $Z_{o1}(\omega)$. $Z_{pa}(\omega)^*$ is the conjugate impedance determined from the load pull measurement (given in Table 3.1). For simplicity, $Z_{pa}^*(\omega)$ of 1.2+j1.3 Ω at 822 MHz is selected. Note that $Im\{Z_{pa}^*(\omega)\}$ = -j1.3Ω, which gives about 150 pF at 822 MHz. This indicate that the net of capacitance is higher (inclusion of wire-bonding & package effect), where some capacitance will resonant out with drain pad or multiple PCB (printed circuit board) inductances (via-hole) (Abdul-Gaffoor, Smith, Kishk, & Glisson, 2002) (Gil & Fernández-García, 2012) (Yarman, Kopru, Kumar, & Prakash, 2014), hence, an accurate PA device impedance can be identified using.

Justification of $Z_{o1}(\omega)$ shall be made to ensure design complexity between both transformation networks, for instance in this design example, $Z_{o1}(\omega)$ of 14-j24 Ω is chosen. The value is selected so that the matching components obtained from Smith Chart is within quality factor of 1. Lower quality factor ensures wider bandwidth. Clearly, $Z_x(\omega)$ which is half of $Z_{o1}(\omega)$ in this case. Note that Z_o typically will be terminated to 50 Ω load. The elements of the impedance matching network can be determined from the Smith Chart given in Figure 3.6, where the first matching element from the PA device is the capacitor and this must be high Q series, typically will be divided into few values to improve current handling (heat issues). Fig. 3.7 shows the complete proposal of the impedance matching transformation to transform $Z_{pa}^*(\omega)$ to Z_{o1}. Mixed-lumped design approach is adopted here (Yarman et al., 2014) combination of distributed and lumped elements is selected to minimize size area and cost of the product. Coplanar waveguide with grounded (CPWG) (Verma, Moyra, Sen, & Kumar, 2017) (Horestani, Durán-Sindreu, Naqui, Fumeaux, & Martín, 2014) is a suitable element as a serial connection replacing air-wound coil inductance, which is an advantage over size and no cost incurred. CPWG is used on printed circuit board (PCB) as an alternative to microstrip line. The gap s between the strip and ground is usually more than the thickness h of the substrate, so

the CPWG field is concentrated between the strip and the substrate ground plane, and CPWG behaves like microstrip (Bahl, 2003). With vias connecting the ground planes, CPWG is less prone to radiate and has higher isolation than microstrip (Bahl, 2033). The CPWG allows lumped element to be integrated along the line, since dedicated grounding to the lumped element can be fulfilled. As a quick comparison, microstrip circuitry features a signal conductor fabricated on top of a dielectric layer, with a conductive metal ground plane on the bottom of the dielectric material. GCPW achieves an extra level of grounding and isolation by fabricating a signal conductor in between two ground conductors, all on the top of a dielectric layer, with an additional ground plane on the bottom of the dielectric layer. Conductive-metal-filled via holes connect the top-layer and bottom-layer ground planes for consistent ground performance. In addition, many GCPW circuits employ ground straps to provide electrical connections for the two top-layer ground conductors for consistency around circuit discontinuities, such as junctions

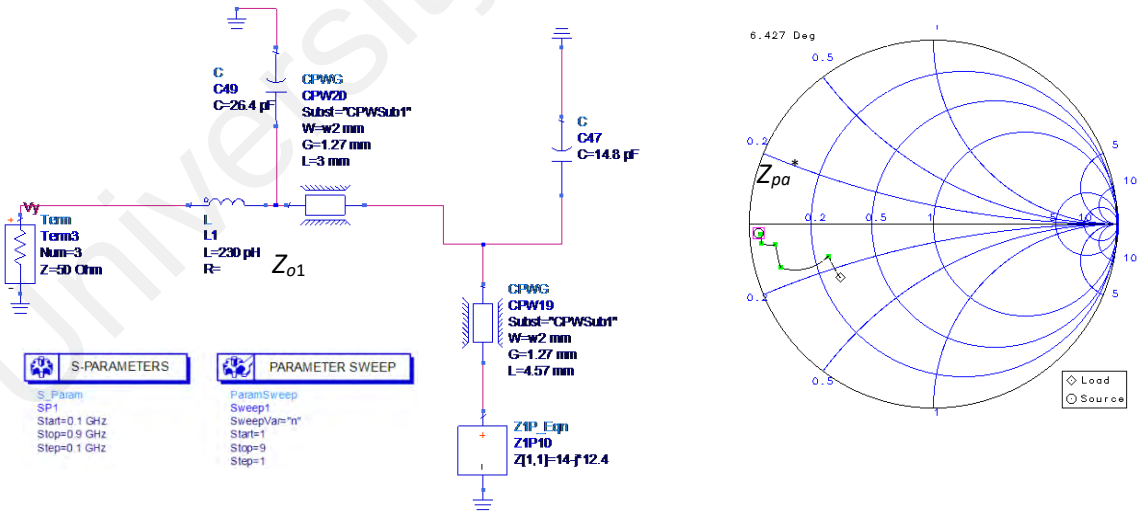


Figure 3.6: Mixed-lumped design elements for matching transformation from Z_{pa}*(ω) to Zo1 and graphical representation in Smith Chart.

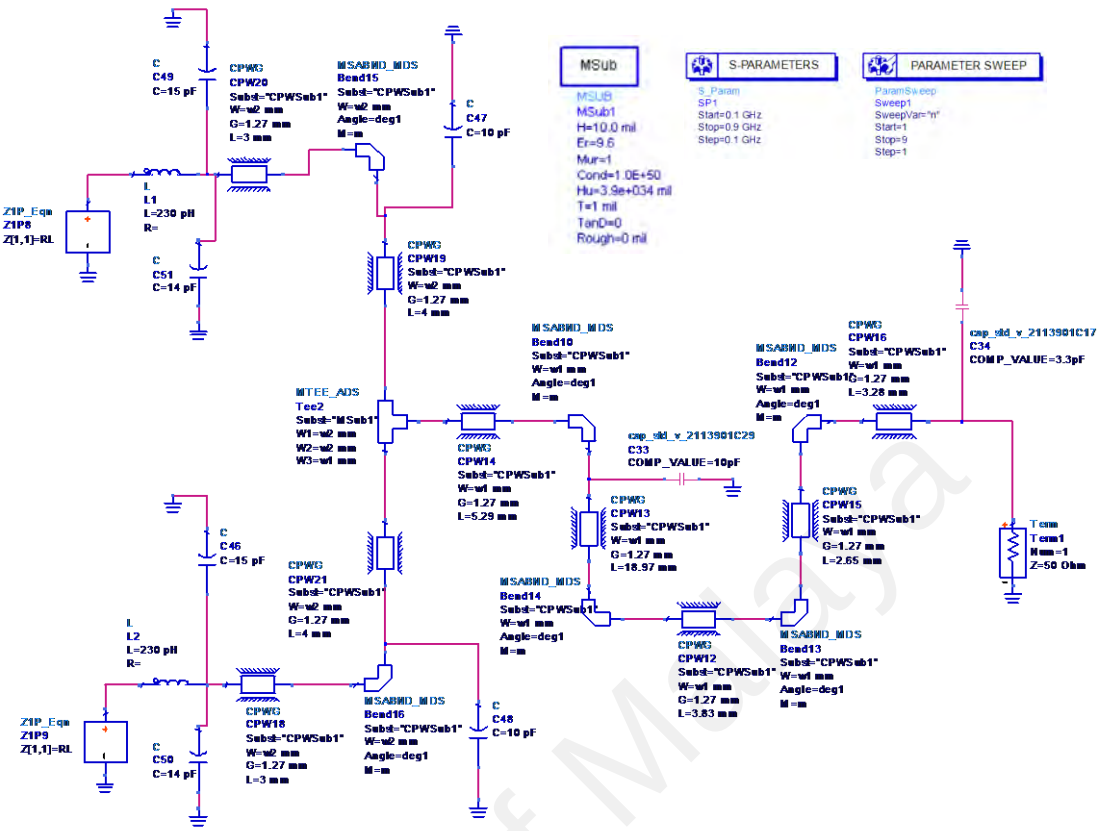


Figure 3.7: Complete matching transformation network from $Z_{pa}^*(\omega)$ to 50 Ω termination

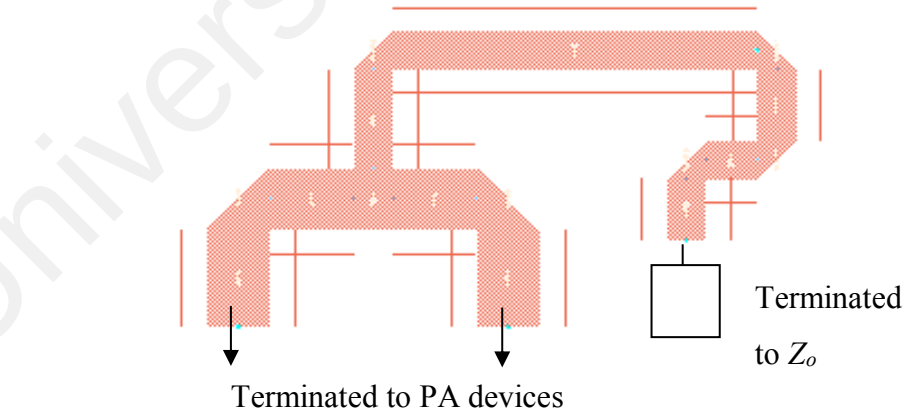


Figure 3.8: The actual physical orientation of the output PA matching network generated from Cadence tool

Note that the layout is fully designed based on CPWG and the side plane is grounding filled

Additionally $Z_x(\omega)$ to Z_o transformation (referring to M_3) is made from 7-j12 Ω to 50 Ω. Note that $Z_x(\omega)$ is half of the $Z_{O1}(\omega)$. Mixed-lumped design approach is adopted as well. Transformation ratio from real part of 7 Ω to 50 Ω requires more elements due to the fact of impedance transformation ratio are higher. The overall matching transformation to provide complete matching transformation from $Z_{pa}^*(\omega)$ to 50 Ω termination, which is depicted in Figure. 3.7. Bending of CPWG is taken into consideration in the design stage so that the size area of the matching transformation can be kept in small form factor. The actual physical orientation of the matching network generated from Cadence tool is shown Figure. 3.8. In order to examine the proposed output PA matching transformation network, S-parameters is simulated in Advanced Design System (ADS). $Z_{pa}^*(\omega)$ for wide frequency response, 760-870 MHz, (as given in Table 3.1) is included in the simulation. Real component models and layout information (from Cadence) of the output PA matching network is used to get the most accurate prediction. S-parameter assisted with 3D-EM simulator (CST) is performed with component optimization for good return loss S_{11}. The result showed good return loss over the entire bandwidth, as shown in Figure 3.9 (comparison between ideal concept and reality elements with 3D-EM simulator). One should take note that -10 dB is the guidelines of the return loss to ensure the matching has minimum reflected wave at particular point.

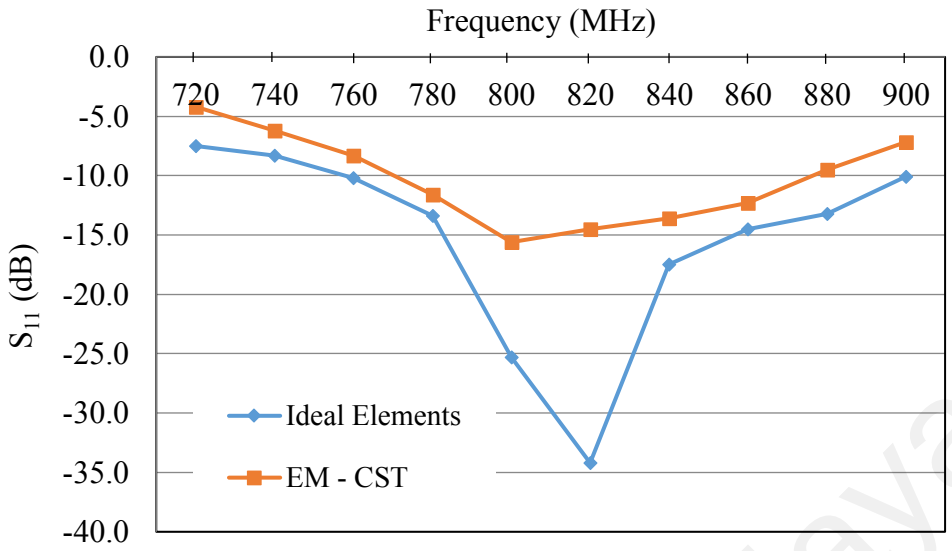


Figure 3.9: Simulation results of return loss over the frequency response of the complete matching transformation network

Additionally, the RF energy flow is carefully taken into consideration here due to the high output RF power that will be generated from the final PA device. The proposed final PA output match is reasonably good to cater RF flow and maintaining small form factor of the product. Some fraction of the heat from the final stage PA will be trapped in the heat sink and the remaining will flow in the PCB surface towards 50 Ω load termination. To find best compromise between stability and circuit performance it is essential to combine the large-signal stability analysis with judicious stabilization strategy (Narendra, Collantes, Paoloni, & Limiti, 2009). The gain expansion of deep class AB bias is required in order to achieve high efficiency performance, but typically causes oscillation issues (Narendra et al., 2009).

3.4 Measurement results

In order to validate the concept experimentally, a prototype board of the high gain stage (the total gain is more than 40 dB across frequency amplifier) together with pre-driver, diver and final PA were designed and fabricated. This is due to the fact the RF drive from Voltage Controlled Oscillator (VCO) is low ~3 dBm. The PCB (FR-4 material) has a dielectric ε_r of 4.5 and a thickness h of 14 mils. Heat sink is mounted at the bottom of driver and final PA in PCB. A photograph of the prototype board is shown in Fig. 3.10. 9 V supply voltage was used for the pre-driver (H01 from Freescale Inc.) and driver stage (MRF1507 from Freescale Inc.) amplifier, and class AB is selected to provide appropriate RF drive to the final PA stage while keeping minimum oscillation or unwanted spurs over the temperature and voltage changes. The supply voltage of the final PA is 13 V and biased with class AB

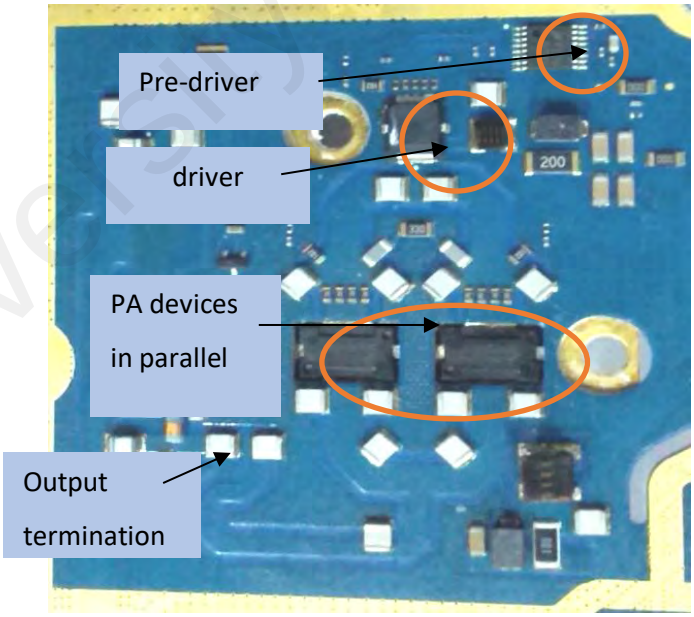


Figure 3.10: Photograph of the prototype board. The board consists of pre-driver, driver and final PA stage

Table 3.2: Summary of power performance over the frequency response which obtained from source and load pull measurement

Parameters	Performance
Operating Bandwidth (MHz)	760- 870
Output Power (W)	80
Efficiency (%)	55
Gain (dB)	46
Stability with 8:1 VSWR	Stable
Robustness with 10:1 VSWR	No degradation in PA

The drain efficiency and PAE equations are given as following

$$Drain\ Eff = P_{out} / (V_{dc} * I_{dc}) * 100\%, \tag{3.12}$$

and

$$PAE = P_{out} / [(V_{dc} * I_{dc}) - P_{in}] * 100\%. \tag{3.13}$$

where V_{dc} * I_{dc} are referring to the DC power consumption. P_{in} is the input power drive.

The power performance (output power and drain efficiency) of the final PA stage is shown in Figure. 3.11. It is shown that output power is more than 75 W across the entire frequency, hitting 80 W the higher end of the frequency band. In the other hand, drain efficiency of the final PA about 55% is recorded experimentally. The DC power is characterized over the bandwidth of interest, as shown in Figure 3.12. The DC power consumption of the final PA is approximately 140W over the frequency bandwidth operation. Therefore, PAE can be calculated from (3.13), where the PAE performance is more than 44% across the bandwidth operation. Refer to Appendix C for output power, gain and efficiency measurement setup.

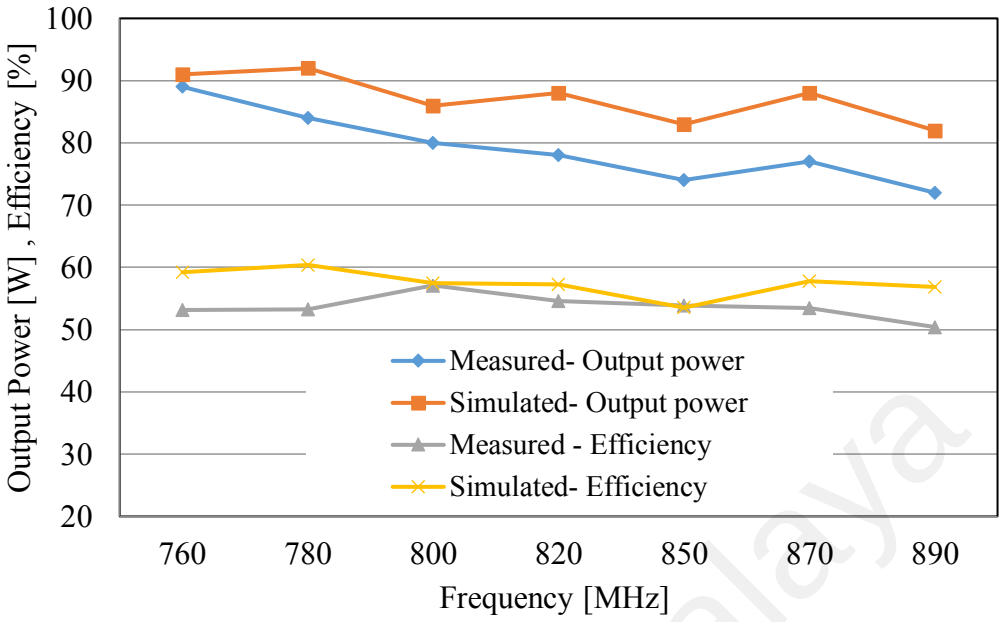


Figure 3.11: Simulated vs. measured results of output power across frequency bandwidth.

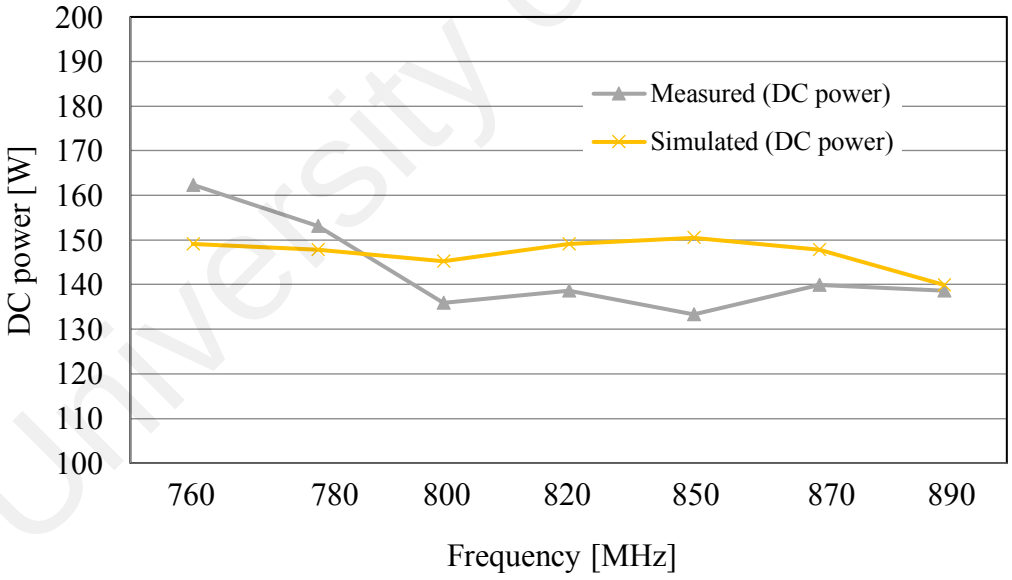


Figure 3.12: Simulated vs. measured results of DC power level across frequency bandwidth

As overall PA system characterization, input drive of 3 dBm is injected to the input of the pre-driver stage, and overall gain more than 40 dB is achieved over the bandwidth interest, as shown in Figure 3.13. As a requirement of the two-way radio communication, suppression or attenuation level at harmonic frequencies are measured. Second and third harmonic attenuation levels across the bandwidth demonstrated shown in Figure 3.14. Very good minimum second and third harmonic suppressions, respectively more than 36 dBc are achieved in measurement level. Refer to Appendix D for measurement setup of spurious emissions.

Oscillation of the overall PA system is checked experimentally. Stable operation without parasitic oscillations is ensured in measurement stage. A ferrite bead is implemented at drain line together with 10 uF (tantalum capacitor) and 22 pF (ceramic capacitor) as a precaution of low frequency parasitic oscillation. A crucial stability test with termination of 8:1 VSWR was carried out. No oscillation is reported under this condition and the power amplifier operation is stable. Robustness test is performed in measurement level with termination of 10:1 VSWR with continuous transmission for 20 minutes. Maximum peak of drain voltage was measured to ensure lower than break down voltage V_{BK} (Narendra, Prakash, Andrei, Paoloni, & Mediano, 2008). No degradation in performance such as power and efficiency is reported. Table 3.2 summarizes the overall performance results of the amplifier line up. Other works related to the broadband high power amplifier also discussed by other researchers (Hayat, Kashif, Azam, Mehmood, & Imran, 2013) (Dettmann, Lei, & Berroth, 2005)

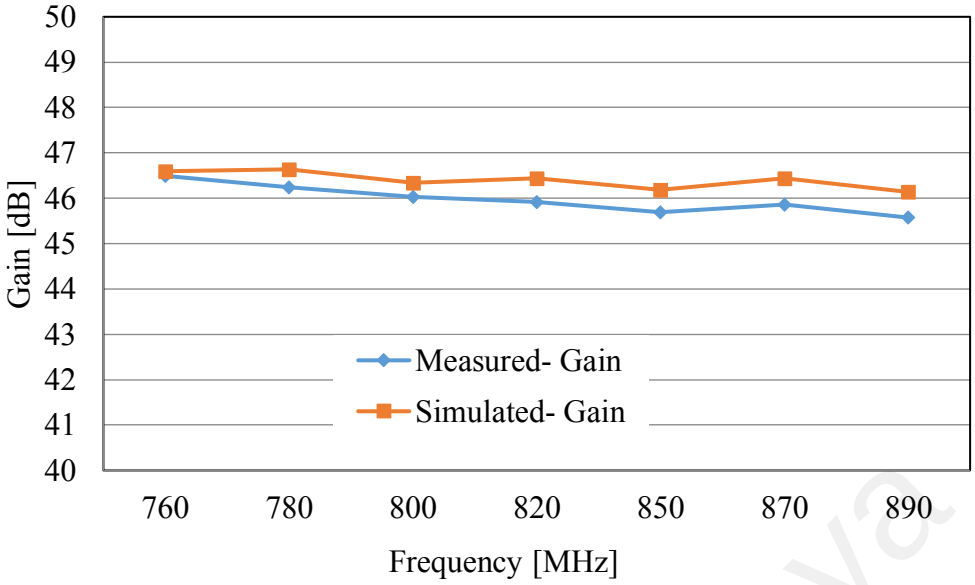


Figure 3.13: Simulated vs. measured results of overall gain performance (pre-driver, driver and final PA stage) across frequency bandwidth

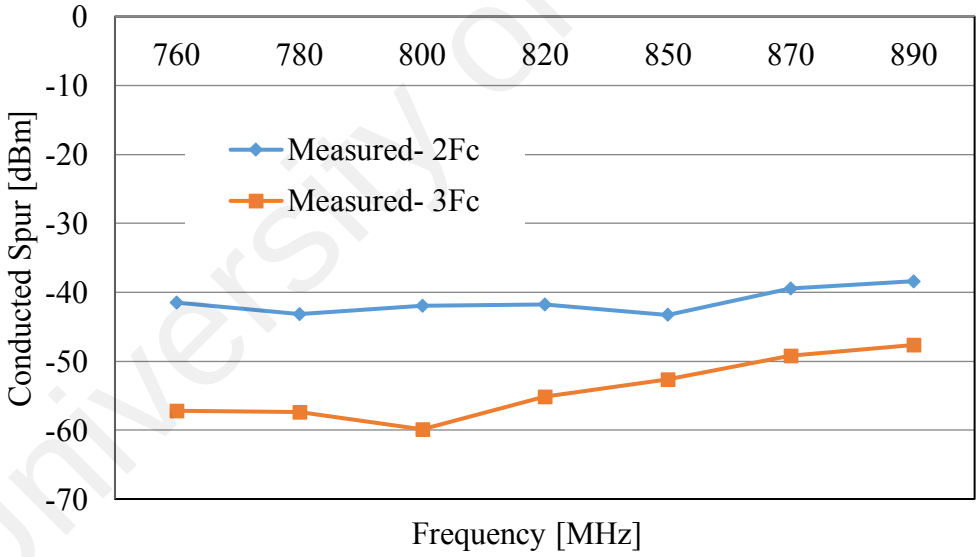


Figure 3.14: Measured results of second and third harmonic level across frequency bandwidth

3.5 Conclusions

A new broadband high performance power amplifier (PA) line up for mobile radio applications is presented. Due to high output power requirement (~80 W) of mobile radio applications, three PA device stages are cascaded i.e. consists of pre-driver, driver and final PA stage. The key design of the PA line up is final PA, where design methodology employing load-pull technique and new generation LDMOS device technology are adopted. Large-signal stability analysis, in specific pole-zero identification technique is employed to investigate oscillation before build the prototype board and this verified in measurement level. Practical design consideration for high power including thermal design aspect is discussed. Experimental results demonstrated output power of ~80 W and gain of 42 dB, while preserving efficiency of 55% over the bandwidth from 760-870 MHz. The proposed topology concept is suitable for the mobile two-way radio applications due to the advantage of the low cost and size area implementation.

CHAPTER 4 : TRANSIENT BEHAVIOURAL CHARACTERIZATION OF MULTISTAGE RF POWER AMPLIFIER

4.1 Introduction

The next generation two-way radio communication, particularly in software defined radio (SDR) systems (Narendra et al., 2012) (Narendra et al., 2010) (Maheshwarappa & Bridges, 2014) (Pinto, Afghah, Radhakrishnan, & Edmonson, 2015) requires a fast transient timing response while meeting the adjacent channel transient power ACTP. A fast ramp up timing is needed for a fast data transmission. Ramp up timing refers to the time required for the active PA device's RF energy to rise from noise level to desired steady-state output level. Similarly ramp down time refers to the time for the PA device's RF energy to downfall from steady state level to noise floor level.

These ramping times have to be less than 1.5 ms while maintaining good ACTP performance of less than -50 dB as per European regulatory standards and Federal Communication Commission (FCC) in USA. Generally, this is an extremely difficult task to achieve, as there is a trade-off between the transient response timing and ACTP performances . One must take note that the ACTP or in specific the gradient slope of the transient power, must be controlled in order to minimize disturbance at away channel; for an example at 12.5kHz . As far as the multistage PA device is concerned, the RF output power from the individual device will grow up with incremental of the gate bias voltage (beyond threshold voltage). But to control the transient behavior of the multistage PA is indeed a great challenge as the individual PA devices has its own different threshold voltages. The ramping profile of individual PA devices should be balanced due to different threshold levels. This is to avoid transient power splatter (transient ACTP) of RF output power at away channels. High transient splatters generate more interference which results in amplitude and phase deviation of the RF output power (England et al., 2013).

In terms of practical realization, the multistage PA design is based on the current sensing with second order integrator and gate voltage shaping algorithm (Prakash C., Narendra K., 2004) This design offers fast transient power response and an efficient way to reduce transient power spectral (transient ACTP) for 2-way radio communication. The proposed work offers low cost implementation in a small size PCB for public safety product portfolios.

4.2 Literature Survey

There are several sensing mechanisms that are been implemented in real products, including power and VSWR sensing with huge space and cost requirements. A VSWR protected ISM-band PA was fabricated using a BST based varactor for detuning of the input matching. The varactor bias voltage of up to 20V can sustain an output VSWR levels of 30:1. The PA delivers 47 dBm output power at a maximum PAE of 49% (Ferretti, Preis, Heinrich, & Bengtsson, 2016). In an another work, a low power, low voltage RF/analog frond end architecture for LF RFID tags with a dynamic power sensing scheme is introduced. Input RF power is converted into DC using a power management system that adjust its performance according to the available RF power. A maximum 3μA DC current consumption over a wide range of input RF power is achieved (Xiaodong & Bayoumi, 2006). In terms of cognitive radio network, the distance of the secondary user from the primary user is determined first in such a way that the secondary user could use the channels without spectrum sensing. The work proposed a way to optimize the secondary user's sensing parameters and transmission power based on its relative distance to the primary user in order to maximize its throughput (Peh, Liang, & Zeng, 2012).

In this work, we focus on method to characterize the transient behaviour of the closed-loop PA including ramping energy from noise level to steady state level and ACTP

for wideband multistage RF PA operation (400-520 MHz). Multistage closed-loop PA with DC current sensing and voltage-shaping algorithm is introduced. The proposed topology is an extension from our previous work (Prakash C., Narendra K., 2004). A prototype board of 3-stages PA line-up (pre-driver, driver and final PAs) which driven by VCO (voltage controlled oscillator) is developed which offering 35 dB gain with constant efficiency of 50% across wide power level. The measurement results demonstrated transient timing response of 1 ms with good ACTP of less than -60 dB over the wide frequency range (400-520 MHz). This is suitable for broadband UHF two-way radio applications particularly for public safety and mission critical product portfolio. In terms of practical implementation, the design offers a low cost solution in a small form factor PCB.

4.2 Circuit Principle

In this section, a novel closed-loop PA circuitry is proposed (Prakash C., Narendra K.,2004). In order to track and maintain RF output power in terms of transient and steady response, respectively, a closed-loop feedback having accurate sensing mechanism coupled to the PA is proposed, refer to Fig. 4.1. Few available sensing mechanisms typically are power and VSWR sensing (Ferretti et al., 2016) (Xiaodong & Bayoumi, 2006) (Peh et al., 2012), however, this is an expensive solution and requires huge size area. For instance, power sensing approach needs RF sampling circuitry and RF to low frequency converter (Peh et al., 2012). Nevertheless, DC current sensing is an alternative approach due to the fact this is simple, requires small size area and low cost implementations

Integration of closed-loop DC sensing with gate voltage shaping V_o is highlighted Figure 4.1 (Prakash C., Narendra K., 2004). The DC current of the PA is sensed by the

current sense resistor. Typically, the sensed resistor has to be large in size to handle high operating power and depending on the DC current consumption. The sensed current is then converted to a voltage by the *I-V* converter. The sensed voltage is then compared against the reference voltage, V_{ref}. The error voltage that is generated during the comparison is integrated by the integrator to generate the control voltage of the amplifier (V_o). The V_o will be adjusted until the desired current is achieved.

The V_{ref} known in state-of-art (i.e. sinusoidal, Gaussian, and root-raised cosine) is used as the transient reference voltage (Narendra, Mediano, et al., 2008). This response is integrated by the integrator such that the rise and fall time of the power response is gentle enough to meet the ETS transient splatter. The integrated error voltage due to the shaped V_{ref} resulted in a higher order shaped power response. The output transient response of closed-loop integrator is determined due to the response of V_{ref} and V_{det} (Franco, 2014) where V_{det} is the detection voltage from the DC current (tie to the PA). The R_{sense} is tied to sense total PA stages current and the output power of the PA line up is proportional to the total DC current that sensed via R_{sense} (pre-driver, drive and final PA). The transient response control of the integrator using *RC* time constant to determine the transient slope of the output response V_o (*t*) is explained here. Few papers have discussed on the transient study of the PA as given in (Yu & Siek, 2015) (Qu, Zhou, & Zhang, 2015) (Chi, Lai, & Du, 2015) (Luo & Siek, 2015).

A basic understanding of the integrator is presented here, where any shape of V_{ref} signal is applied at the non-inverting input of the operational amplifier. The $V_o(t)$ is sampled and coupled to the gain feedback (to the inverting input of the operational amplifier). Based on circuitry shown in Fig. 4.1, a basic mathematic expressions are derived using Laplace's equation (Dagang, Qiong, Mingliang, & Xiao Yu, 2015).

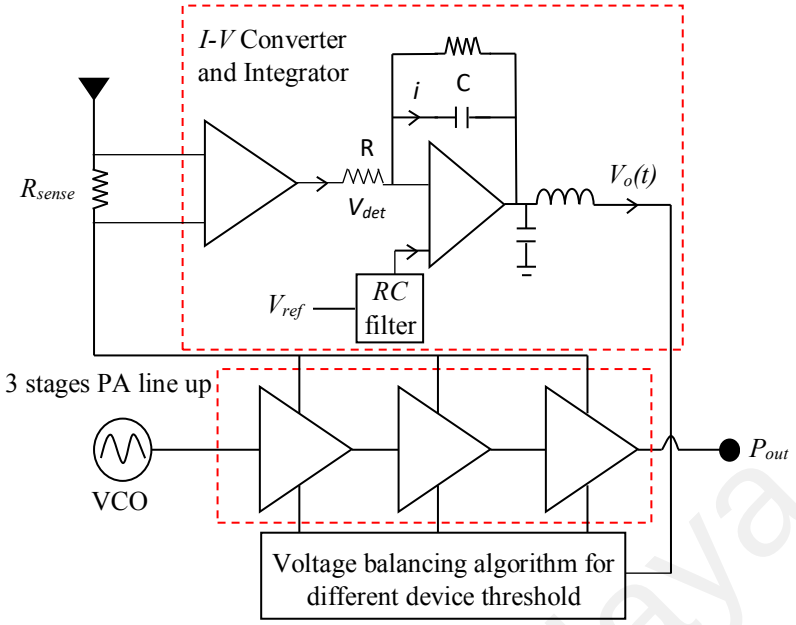


Figure 4.1: Simplified closed loop transient and DC sensing RF power (Prakash C., Narendra K., 2004)

The V_{ref} is defined as $Au(t)$, where $u(t)$ is step voltage. The current i flows across the capacitor C is the rate of voltage charge across it with respect to the time, thus

$$i = \frac{Au(t) - kVo(t)}{R} = C\frac{d}{dt}[Vo(t) - Au(t)], \tag{4.1}$$

Thus, one can define $Vo(0^-) = 0$ since no charge in capacitor before t=0, as following and the result summarized in Fig. 3.

$$Vo(s) = \frac{sA + c}{s(s+b)} \quad , \tag{4.2}$$

where $b = \frac{k}{RC}$ and $c = \frac{A}{RC}$.

Using partial fraction expansion

$$Vo(s) = \frac{X_1}{s} + \frac{X_2}{s+b} \tag{4.3}$$

Taking inverse Laplace transform of (4.3), the output voltage can be deduced as

$$Vo(t) = \frac{A}{k}u(t) + A\left(1 - \frac{1}{k}\right)e^{-\frac{kt}{RC}} \tag{4.4}$$

From (4.4), a simple step unit response shape is given at $V_{ref}(t)$, the voltage response of the V_o(t) can be dictated as shown in Figure 4.2. This is good start of the analysis to understand of the $V_o(t)$ behavior with present of $V_{ref}(t)$. Nevertheless, the analysis can be used to explain complex signal of $V_{ref}(t)$. For instance, if the complexity of the $V_{ref}(t)$ is increased as sinusoidal function, the $V_o(t)$ is given as in Figure 4.2. By knowing the transient behaviour of actual PA device the $V_{ref}(t)$ response will be adjusted for optimum performance.

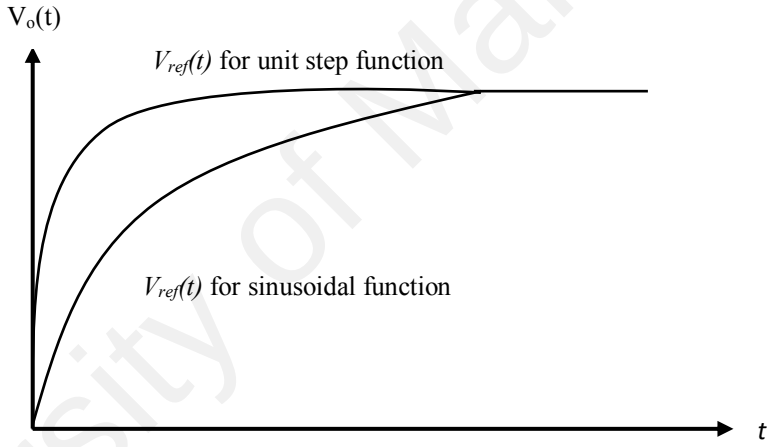


Figure 4.2: Output voltage characteristics of closed loop integrator with feedback for the V_{ref} (t) with step and sinusoidal response

4.3 Transient behavioural characterization

Transient behavioural characterizations of multi-stages PA line up to meet requirements of two-way radio applications are discussed in this section. Due to unavailability, the PA device model is being replaced with behavioural model. The behavioural model is characterized based on actual PA line up performance under linear and non-linear regimes over wide frequency response. It is represented with non-linear

controlled sources in the CAD tool. Typically, two types of the non-linear controlled sources; non-linear voltage controlled current source (VCCS) and non-linear voltage controlled voltage source (VCVS) are used. Curve fitting method is adopted to determine a set of polynomial coefficient of the respective PA characteristics (Dagang et al., 2015). As far as the curve fitting method is concerned, it is a process of constructing a curve or mathematical function that has the best fit to a complex series of dataset points (Arif & Anand, 2015). Consider the higher order polynomial equation is shown as

$$f(x) = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + \ldots + a_j x^j = a_0 + \sum_{k=1}^{j} a_k x^k \tag{4.5}$$

where a_0 and a_k polynomial coefficients for the order from k=1 and up to j.

The polynomial coefficient is determined by quantifying the error function in the curve fitting. In order to achieve high accuracy of the polynomial coefficients, the error function has to be minimized and one of the approach with lease square (Arif & Anand, 2015). The generalized equation of the error function is given by

$$err = \sum (d_i)^2 = (y_1 - f(x_1))^2 + (y_2 - f(x_2))^2 + (y_3 - f(x_3))^2 + (y_4 - f(x_4))_2 \tag{4.6}$$

By substituting (12) into (13), then error function can be simplified to

$$err = \sum_{i=1}^{n} (y_i - (a_0 + a_1 x_i + a_2 x_i^{\ 2} + a_3 x_i^{\ 3} + \ldots + a_j x_i^{\ j}))^2 \tag{4.7}$$

where: *n* is number of data points given, *i* is the current data point being summed and *j* is the polynomial order. To minimize (4.7), the derivation with respect to each coefficient is set to zero as shown in Eq. (15).

$$\frac{\partial err}{\partial a_0} = -2 \sum_{i=1}^{n} (y_i - (a_0 + \sum_{k=1}^{j} a_k x^k)) x^r = 0 \tag{4.8}$$

Where $r = 0,1,2,3 \ldots j$

By optimizing the error function referring to (4.8) with available computational tool, Matlab for an instance, the polynomial coefficient of the equation will be determined.

In this work, the input power will be injected from VCO with 3 dBm level. The pre-driver, driver and final PA are built with LDMOS technology with drain supply of 7.5 V with 16 dB and 10 dB (driver & final PA) gain respectively. Therefore, the multistage PA line-up is capable to deliver up to 38 dBm with efficiency of more than 50%.

Referring to Figure. 4.1 for the general diagram of 3-stages PA line up with closed-loop feedback (e.g. I-V converter and the integrator). The test prototype board will be discussed in the measurement section. The PA line up has an operating power of ~6 W range from 400-520 MHz, and input signal is driven by the VCO with output power of 3 dBm. Therefore, the PA line up is performing at 44% of efficiency with a 35 dB of gain (output power of 6 W) over the bandwidth operation, see Figure 4.3.

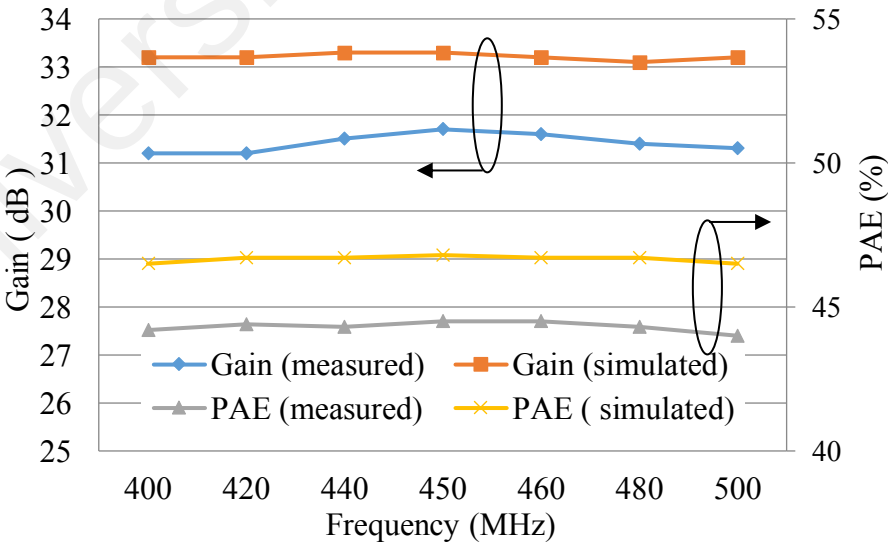


Figure 4.3: Complete measured performance of the 3-stages PA line up; PAE and gain over the entire bandwidth response

The simplified behaviour model representation with 3-stage PA models (non-linear controlled sources) is shown in Fig. 4.4. The curve fitting method use to represent the 3 stages PA model using nonlinear voltage controlled current source (VCCS) and non-linear voltage controlled voltage source (VCVS). Current sense topology assumes that the PA drain current is proportional to the output power. The PA current is a function of the output voltage, V_o. The output voltage is coupled to the 50 Ω load termination where the output power will be delivered. This output voltage is represented by a set of polynomial coefficient used in the non-linear VCVS equation. The polynomial coefficient of the P_{out} vs. V_o is determined with reference to the measured performance, with an assumption of output power is function of V_o.

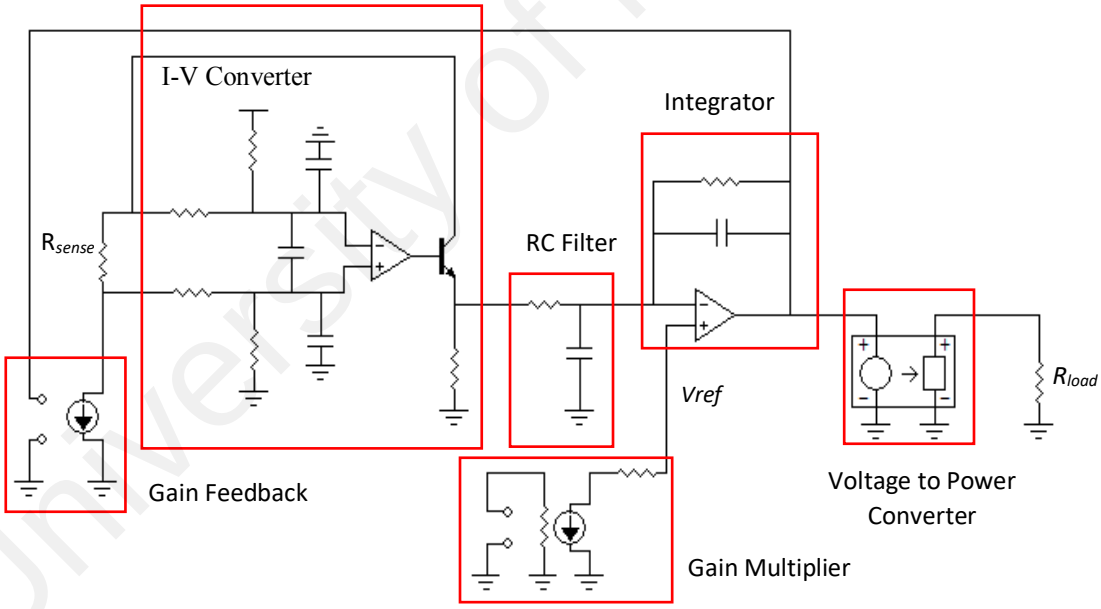


Figure 4.4: Simplified diagram of the 3-stages PA line up using non-linear controlled source (VCCS and VCVS) and closed loop feedback (I-V converter, gain feedback and integrator)

At the same time, the output power of the PA is represented as a polynomial coefficient of a nonlinear VCCS also (P_{out} *vs.* V_{ref}). For an accurate transient

characterization, V_{ref} is generated using arbitrary waveform generator (AWG) in ADS. Data access component (DAC) in ADS is used to extract or interpolate the time domain waveform of AWG in the simulation.

With the obtained polynomial coefficients from (4.8), the PA current and output power are modelled in a non-linear equation as a function of closed-loop feedback's output voltage. To use the non-linear controlled source model in ADS, the PA current versus V_o need to be derived from the sets of measured data. Refer to Figure 4.5 (a) for the polynomial coefficient method determination from measured data collected and Figure 4.5 (b) the presentation of the PA output power versus closed-loop feedback's output voltage polynomial coefficient in the DAC (in ADS). By increasing the order of the polynomial coefficient best fitting to the measured data can be achieved. All necessary polynomial coefficients that required for all nonlinear controlled sources are inserted, as shown in the Figure 4.5. The polynomial fit is obtained through LabVIEW software where the test code demonstrates fitting data to polynomial. The test code is able to give best fit based on polynomial orders which is specified. Please refer to Appendix F for the test code and equation created to fit the raw data.

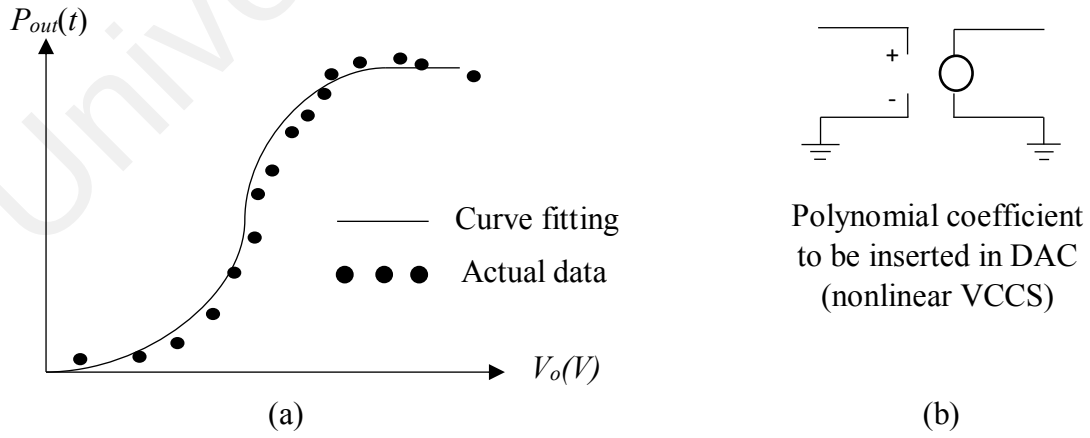


Figure 4.5: a) Polynomial coefficient method determination from measured data collected output power vs Vo

b) representation of polynomial coefficient in the DAC (in ADS) for the PA output power versus Vo

Below the PA threshold voltage, V_o response will be the integration of the V_{ref}. However, above the PA threshold, the V_o response will change which typically become gentler in shape due to the V_{det} response (the PA started to turn on). The boundary condition must take into account to control the rate of change of power. In experimental test, as given in Fig. 4.6, with a step function shaped V_{ref}, the multistage amplifier power and voltage response rise too rapidly as shown in the blue and turquoise trace respectively. This response will generate excessive ACTP and could not meet the specifications. With a sine wave ramp of V_{ref}, the integration output has created a second order power and voltage response as shown in the violet and red trace respectively. This response can meet the ETS specification. The measured data of this scheme is shown below. However, the shape of the V_{ref} must be determined based on the PA device characteristics such as threshold level. Certainly this approach give flexibility to the designers to optimize the software instead of tedious optimization in board level.

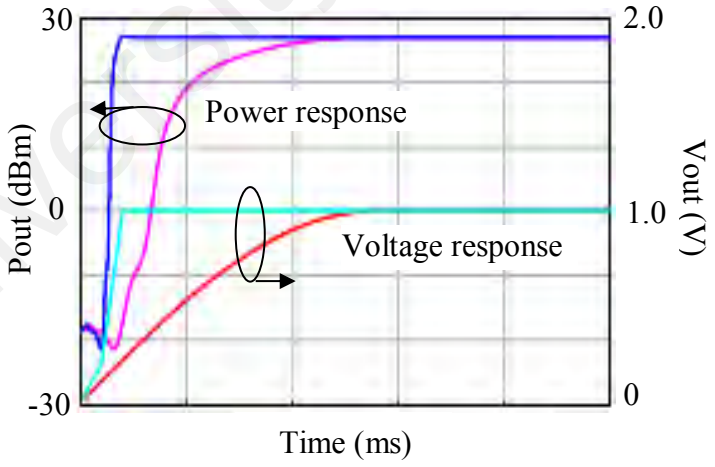


Figure 4.6: Experimental characterization of the output power from voltage to power converter due to step function and sine wave ramp of V_{ref}

4.4 Measurement results

In order to experimentally validate the proposed technique, a prototype board of the closed-loop feedback with 3-stages PA line up using multi-layers FR4 material has been fabricated. The PA line up and the closed-loop feedback are integrated within small form factor with low cost solution. Open grounding area with adequate via-hole, and DC/ RF routing are well isolated in PCB for minimum spurious. As part of EMC requirements, it is necessary to have the DC layer below the RF grounding layer. This is to avoid DC noise couple into RF signal which can cause spurious emissions (Mehri, Heidari, & Masoumi, 2016). The thickness of the DC routing is computed to carry adequate DC current to feed the appropriate transistor. To make placement of the components, top and bottom of the PCB layout are utilized. The photograph of the prototype board is given in Fig. 4.7, where (a) is referring to the low frequency and DC sections; i.e. (a) closed-loop feedback, (b) the placement of the RF section; pre-driver, driver and final PAs. Heatsink is mounted at the bottom of PCB to provide good heat from the PA (Yu et al., 2017). The capacitors represent ceramic and tantalum types, and inductors represent air wound type.

With transient simulation, the complete transient behaviour such as ramping up and ACTP are simulated and good correlation is established over the frequency response. ACTP measurement is being the ratio of the energy produced in the wanted and adjacent channels when the transmitter is keyed up or down. In this work it is referred to 3 stages PA line up and the measurement is done in frequency domain. When the PA stages are powered up or down, there are some momentarily increase in unwanted power. These unwanted power are produced at the adjacent channels (± 12.5 kHz). The sweep time in spectrum analyser is set to 40ms to cover the whole pulse (ramp up and down) and center frequency as 10.7 MHz. The PA stages are keyed up, the spectrum will show frequency domain signal as shown in Fig 4.8. Firstly, the channel power in the middle of the burst

is read as P_1 dBm. Secondly, the center frequency 10.7 MHz is added with ± 12.5 kHz and the peak power is recorded as P_2 dBm. The ACTP is recorded as $P_1 - P_2$ dBc. The same steps are repeated for the other side of the channel. The graphical illustration of the ramping up and down, and ACTP performance is shown in Fig. 4.8 using Agilent PSA Series Spectrum Analyzer E4445A

The ramping up time is referred to time from initial triggering (Tx enable) point to -1dBc of steady state power. The ramping down time is the time taken from -1 dBc of rated power to -60 dBc. Figure 4.9 and Figure 4.10 show the results of ramping up and ACTP over the entire bandwidth (400-520 MHz), respectively, whereby the ramping up time is less than 1 ms and the ACTP is less than -60 dB, respectively. The ramping down is measured and the result indicated in similar trend. The steady-state power is typically 6 W. Refer to Appendix B for adjacent channel transient power (ACTP) and output power ramp up down timing measurement setup

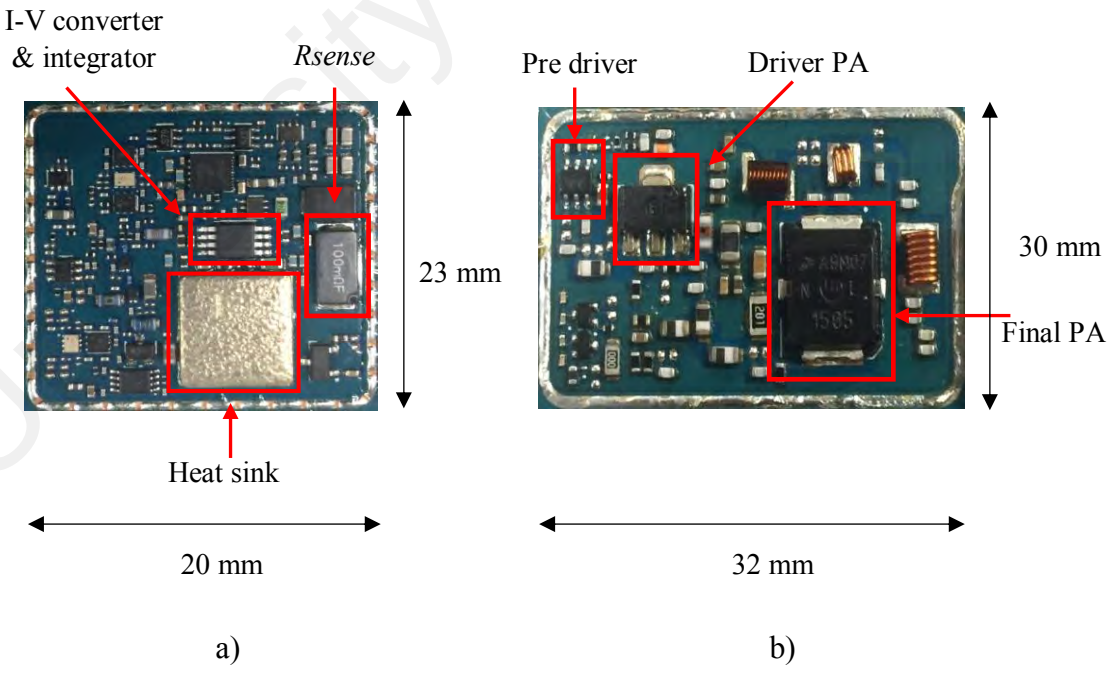


Figure 4.7: Prototype board of the closed-loop feedback with 3-stage PA line up

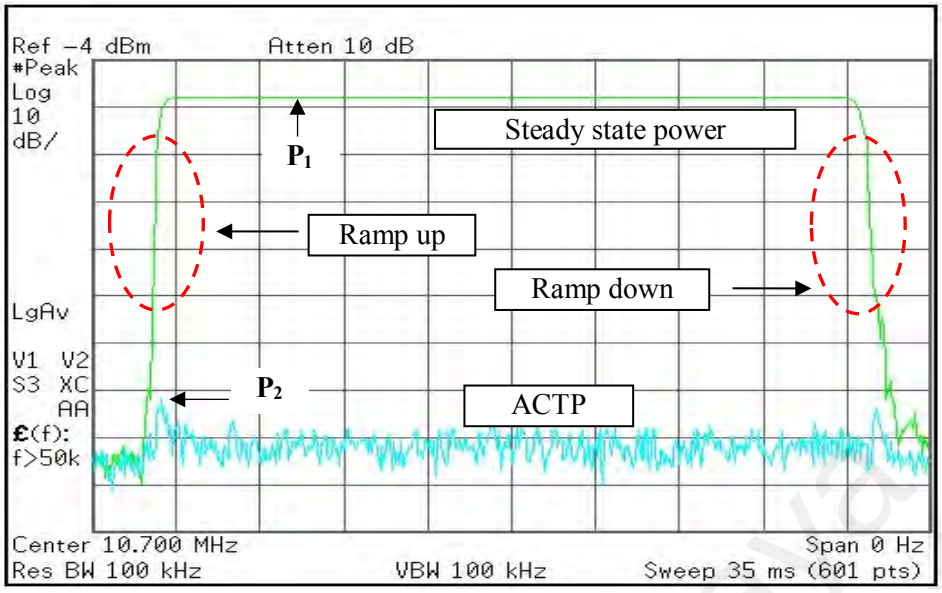


Figure 4.8: The transient performance of ramp up and ramp down, and ACTP measurement at 450 MHz as reference

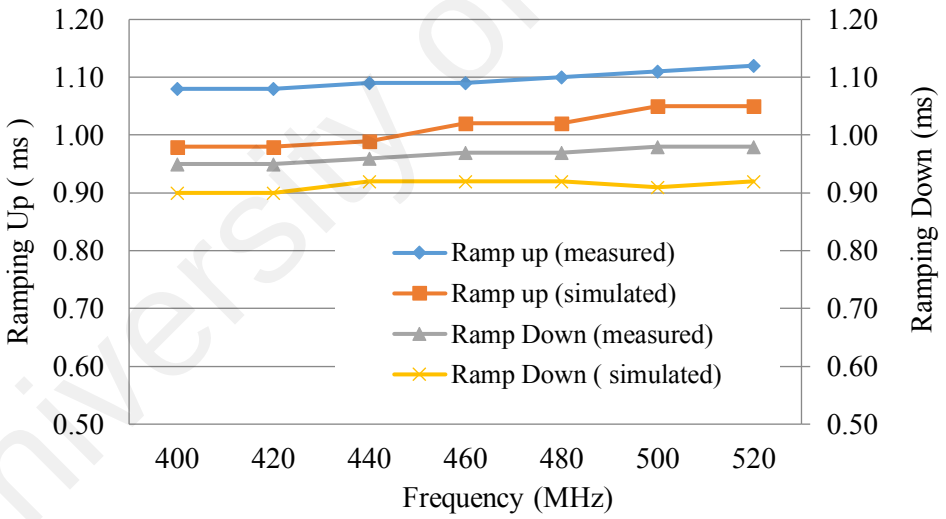


Figure 4.9: Comparison between measured and simulated result of ramping timing

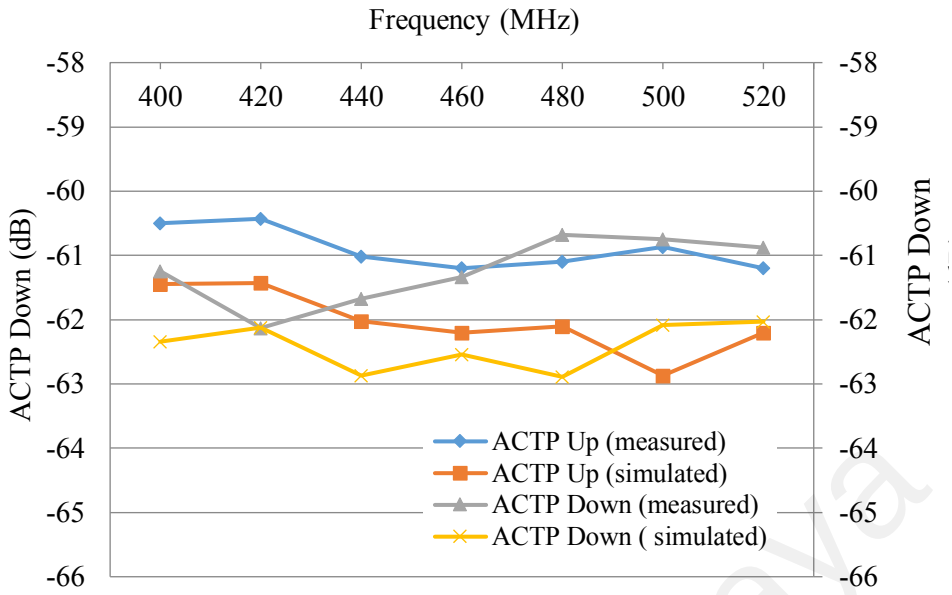


Figure 4.10: Comparison between measured and simulated result of ACTP

Stable operation without parasitic oscillations is provided with feedback network and gate loading resistor at the input of the amplifier (Mori et al., 2016). The feedback value of 100 Ω (resistor) and 0.1 μF (ceramic capacitor) are predicted in design level. Gate loading resistors of 2 Ω (in parallel form) are placed at gate of the amplifier. A crucial stability test with termination of 10:1 VSWR was carried out. No oscillation is reported under this condition and the PA line up operation is very stable.

4.5 Conclusion

A technique to predict transient behavioral response of RF PA is presented, whereby a novel topology with of DC current sensing and voltage shaping algorithm is proposed. An accurate transient behavioral modelling including ramping energy from noise level to steady state level, and adjacent channel transient power (ACTP) established high degree of correlation with measurement level for wideband RF PA operation (400-520 MHz). Experimental results demonstrated good performance; transient timing

response of 1 ms is achieved while maintaining good ACTP of less than -60 dB over the wide frequency range of 400-520 MHz. This is a good solution for 2-way radio application with small form factor and low cost solution.

CHAPTER 5 : A NEW ARCHITECTURE OF RF POWER AMPLIFIER FOR NEXT GENERATION PUBLIC SAFETY TWO-WAY RADIOS

5.1 Introduction

There is a vast and growing market for professional and mission critical users who need high quality yet affordable tool that takes advantage of the power and communication range. Professional two-way radio users very much expect a reliable mode of communications especially for public safety and mission critical purposes. A missed call or dead battery can cause dissatisfaction, lowered productivity and loss of business. Due to inherent nature of RF, conventional two-way radios can suffer from several limitations. The most referred standard for professional and business critical applications of two-way radio is the European Telecommunications Standards Institute, ETSI. In two-way radio standards and markets, one of the most important components of the ETSI standard is the adaptive power requirement and fast transient timing response. The next generation two-way radio communication systems require an adaptive power adjustment to achieve optimum efficiency over wide dynamic power level. Adaptive power means that the output power level is adjusted accordingly from point to point communication distance; for a nearer communication distance, the output power level of the amplifier should be lower and vice versa (Narendra, Mediano, et al., 2008)

In the two-way portable radio applications, a constant predefined envelope modulated RF signal is injected from Voltage Controlled Oscillator (VCO) and that constant envelope modulation is typically either a Frequency Modulation (FM) or Frequency Shift Keying (FSK). Analysis showed that fixing an input RF drive to the amplifier is an inefficient method of achieving constant PAE for wide power levels (Narendra, Mediano, et al., 2008). For any required power level, drain supply and the RF input drive at an amplifier must be carefully selected and ideally maintained during the circuit operation (Narendra, Mediano, et al., 2008). Constant efficiency can be achieved

for wider range of power levels with supply or load adjustment but few studies have been reported on these methods (Narendra et al., 2012) (Ji, Jianyi, Zhiqiang, & Binqi, 2015) (Tamjid, Ghahremani, Richardson, & Fathy, 2017)

A novel technique of gain stage controlled with logarithmic detector to provide accurate RF input drive tracking is proposed (Narendra, Mediano, et al., 2008). Driver amplifier gain control and the logarithmic RF power detector circuitry enables an accurate input RF drive to the final PA in order to achieve constant efficiency across wide power levels. Drain supply adjustment and class AB bias scheme for the PA is adopted. Due to nonlinear behavior of transconductance (g_m) of the LDMOS PA device at low drain supply voltage (Narendra, Anand, Joshua, Tan, & Boeck, 2007), a slight increment of gate bias voltage is useful to increase the gain of the PA.

As far as voltage controlled current source (VCVS) of LDMOS device is concerned, the output RF output from the device will grow up with incremental of the gate bias voltage. Therefore, an analytical explanation with regards to PA current sense tracking accuracy and the transient response of the closed-loop integrator with voltage shaping algorithm are discussed. In terms of practical realization, the PA design is based on the current sensing with integrator and gate voltage shaping algorithm (Prakash C., Narendra K., 2004). This design offers fast transient power response with good ACTP performance. In addition to accurate tracking, this topology offers low cost implementation.

Comprehensive theoretical approach, design methodology and practical realization are presented in this work. In addition, measurement challenges associated with the closed-loop RF PA system design to meet two-way radio stringent requirement particularly constant efficiency over wide dynamic power level and adjacent channel transient power (ACTP) in small form factor design are discussed. The proposed work

also offers low cost implementation for public safety product portfolios. Adaptive power requirements in two-way radio applications refers to change in output power level in accordance to communication distance. Low output power is sufficient for shorter communication distance but for longer distance, higher output power is required. Due to this requirement, to maintain constant efficiency over the wide output power level and achieve longer battery life is a real challenge. In conventional two-way radio design, the VCO output signal is typically fixed. Therefore, to maintain constant efficiency for the wide output power level and lower ACTP level as well as longer battery life when the PA line up is operating at low output power are indeed challenging.

5.2 Gain stage controlled with logarithmic detector

5.2.1 Principle Operation of the gain stage controlled with RF detector

The PA efficiency becomes a maximum in the extended saturation region (Narendra, Mediano, et al., 2008). Hence, controlling the saturation point can produce constant efficiency across varying power levels (Khan, Sarbishaei, & Boumaiza, 2014). In principle, to achieve constant i.e. power aided efficiency (PAE) across wide power levels requires input drive P_{RF} to change according to the required output power P_{out} for drain voltage, V_{DS} adjustment method while having fixed load impedance R_{OL} (Narendra, Mediano, et al., 2008). A simple analysis to investigate input RF drive requirement to achieve wide power levels (0.5 to 6.5 W) with a commercial non-linear LDMOS PA, model (RD07MUS1 from Mitsubishi) is carried out. To achieve P_{out} of 6.5 W, the V_{DS} is set to 8V and P_{RF} adjusted for maximum PAE. Similarly it can be done to achieve P_{out} of 0.5 W.

Input drive to the driver PA requires dynamic range of 10 dB to maintain constant PAE (~52%) for wide power levels (0.5 to 6.5 W) at 430 MHz, as shown in

Figure 5.1. For maximum efficiency, the PA transistor's drain voltage V_{DS} and drain current I_D must swing towards two times of supply voltage and I_{max} (defined by maximum FET current), respectively at desired output power level. The optimum drain supply voltage V_{DSopt} for any power P_{out} level (Kosaka et al., 2014) can be expressed as

$$V_{DSopt} = \sqrt{2P_{OUT}R_{OL}} + V_K \tag{5.1}$$

where R_{OL} and V_k are optimum load resistance and turn-on or *knee* voltage, respectively. V_k can be obtained from the I_d-V_{DS} transfer characteristics plot either from simulation or from measurement. V_k can be approximated to $0.2 \cdot V_{DSopt}$ for many practical LDMOS FET cases (Kosaka et al., 2014).

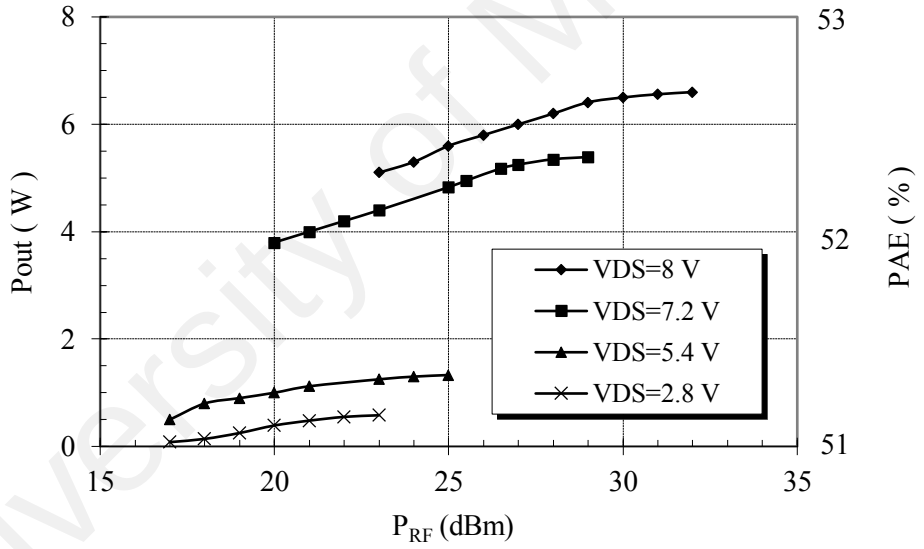


Figure 5.1: Analysis of P_{RF} required across wide power levels (0.5 to 6.5 W) for V_{DS} adjustment method to achieve constant PAE over wide dynamic power level.

One should take note that for each output power level, the V_{DS} and P_{RF} must be adjusted accordingly. For constant envelope modulation such as FM or FSK (in most two-way radio applications), P_{RF} will be fixed from VCO. In this regard, a novel gain stage controlled was proposed (Narendra, Mediano, et al., 2008), a driver amplifier, Q_1 and

logarithmic RF power detector to provide accurate RF input drive to the final PA (refer to Figure. 5.2). The matching networks associated with the M_1 and M_2 are shown in Fig. 2 as well, where 1and 2 are for Q_1 and Q_2, respectively.

A logarithmic amplifier provides a type of compression in which a signal having a large range of amplitudes are converted to one of smaller range (Simon, Weigel, Neurauter, & Marzinger, 2004). The use of the logarithmic function in this application uniquely results in the output representing the decibel values of the input and expressed with fundamental equation below

$$I_{DET} = I_{SLP} \log_{10} \frac{V_{RF\,IN}}{V_Z}, \tag{5.2}$$

where I_{DET} is the partially filtered demodulated signal, whose exact average value will be extracted; I_{SLP} is the current mode slope; V_{RFIN} is the input in volts-rms; and V_Z is intercept

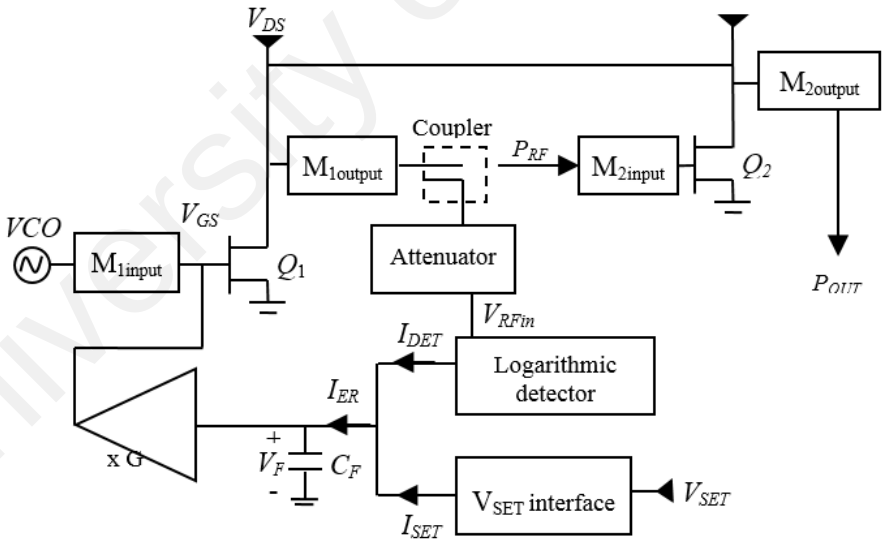


Figure 5.2: Overview of the gain stage controlled circuitry with logarithmic RF power detector ((Narendra, Mediano, et al., 2008)

The generated set point interface with resistance, R is simply:

$$I_{SET} = \frac{V_{SET}}{R} . \tag{5.3}$$

where V_{SET} is the set point interface input voltage. The difference between I_{DET} and I_{SET} called as error signal (in a form of current, I_{ER}) is applied to loop filter capacitor C_F. The voltage appearing on this capacitor is given below:

$$V_F(s) = \frac{(I_{SET} - I_{DET})}{sC_F} , \text{ and} \tag{5.4}$$

$$V_F(s) = \frac{(V_{SET}/R) - I_{SLP}\log_{10}(V_{IN}/V_Z)}{sC_F} , \tag{5.5}$$

C_F integrates the error signal I_{ER} to set loop bandwidth and ensure loop stability (Narendra, Mediano, et al., 2008). V_F will rail to the positive supply value for any value of V_{SET} greater than V_{RFIN} in close loop form. Logarithmic detector seeks for V_{RFIN} to its maximum value whenever it falls below the V_{SET} (Narendra, Mediano, et al., 2008). The logarithmic detection law would ideally result in a step change for V_{SET} or V_{RFIN}. Additional buffer with the gain is added to control the gain of the Q_1. It provides required P_{RF} to the Q_2. The gain is adjusted using driver gate voltage, V_{GS}. The losses of directional coupler and attenuator must be taken into account in order to fit into the logarithmic conformance region.

Biasing the PA device in class AB mode is effective with respect to the controlling of the gate biasing to achieve constant amplifier gain. Knowing the I_D of an N-channel MOSFET, one can derive the g_m in saturation region (Narendra et al., 2007) as shown below

$$g_m = \frac{W\mu_n C_{OX}}{L}(V_{GS} - V_T) , \tag{5.6}$$

and to increase g_m, channel width W of the transistor can be increased but this also increases the channel length L and reduces oxide thickness (Baylis, Dunleavy, &

Connick, 2009). As explained in (Narendra et al., 2007), weak decrease of g_m with V_{DS} below 4.8 V can be compensated by slightly enhanced V_{GS} for the Q_2 (the PA device). So, in addition to the reduction of V_{DS} and P_{RF}, a small increase (more positive) of the gate voltage is helpful for increasing the average g_m (Narendra, Mediano, et al., 2008). Thus, this will increase gain and PAE.

5.2.2 Characterization of the gain stage controlled with logarithmic detector

The proposed design concept is validated on board measurements with an accurate input RF drive tracking as proposed in Figure 5.2. For the driver amplifier (Q_1) a low output power LDMOS device (RD01MVS1) and the PA (Q_2) with RD07MUS1, both from Mitsubishi Inc. and using LDMOS technology. In Figure 5.3, AD8315 logarithmic power detector (from Analog Devices Inc.) was chosen and measurements showed detection range from -49 to +2 dBm under 50 Ω impedance, intercept at –60 dBm and logarithmic slope of 23 mV/dB.

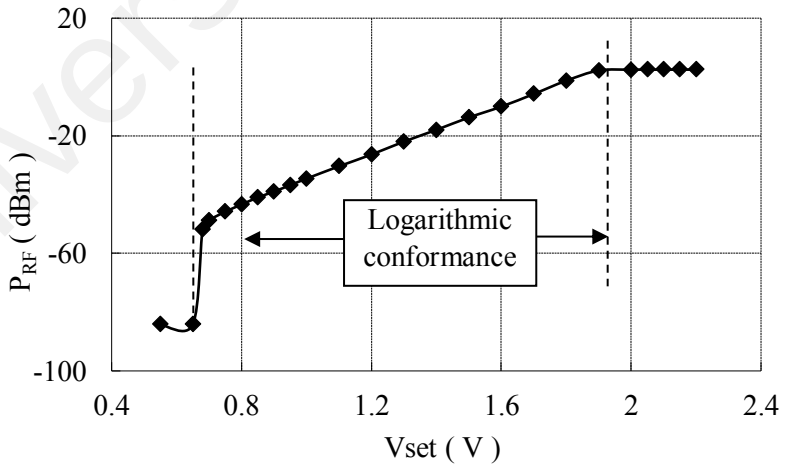


Figure 5.3: Experimental of the gain stage controlled characteristic with the logarithmic detector

V_{RFIN} versus V_{SET} curve showed logarithmic conformance region of 50 dB (-50 to 0 dBm) and the curve was used to set V_{SET} value to provide accurate input RF drive to the PA. A 20 dB directional coupler and 15 dB pi-resistive attenuator are designed to fit the detected power in logarithmic conformance region.

Figure 5.4 shows that to control the P_{RF}, the proper selection of V_{set} of the logarithmic detector shall be made. For the case of power level of 6.5 W, the voltage reference shall be set to the threshold and with right selection of V_{set} the power level of Q_2 will be reduced to 0.5 W. Therefore, the optimum P_{RF} would be injected to the input of Q_2 for optimum efficiency across wide power level. Figure 5.4 shows that efficiency (PAE) response characteristic of the PA over wide dynamic power level (with adjustment of P_{RF}), which referred from 400-500 MHz. This indicates that constant efficiency is achievable over the wide power level and with further proper adjustment of the P_{RF} it is possible to obtain over wide frequency operation as well. Refer to Appendix C for measurement setup

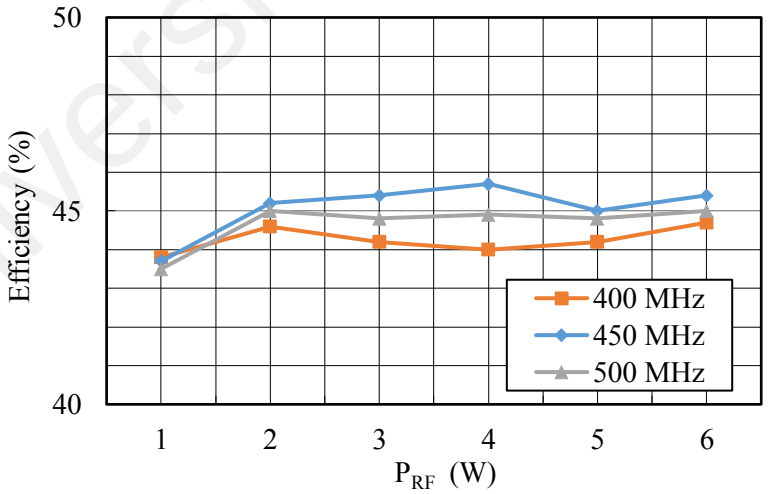


Figure 5.4: Experimental characterization of efficiency of Q_2 with respect of P_{RF} at 400 MHz, 450 MHz and 500 MHz

5.2.3 Battery Life Measurement

Many business portfolios rely on two-way radio communication, both for workforce efficiency and safety. Battery life is therefore critical. The gate stage controlled with logarithmic detector provides a constant efficiency as discussed earlier. In addition, since transmitting is the most energy intensive operation, the measurement results shows that the adaptive RF PA design can typically function 40% longer in terms of battery life than the non-adaptive conventional architecture of two-way radios.

In radio communications industry, battery life is referred to radios being on a specific cycle. It's called the 5-5-90% cycle time assumption. That basically means when the radio is under operation, 5% of time is spent for transmitting, 5% for receiving and 90% on standby with reference to 1 minute. In other words, the device under test would be in transmitting and receiving mode for 3 seconds. The remaining 54 seconds are for standby mode (idle mode). Since the radio communication is half duplex, this cycle profile is preferred. By using this system on a radio, and not always having to simultaneously talk and listen, you save battery. Mobile phone struggle to compete with radios when it comes to battery life. If a user goes over the 5-5-90 cycle time, then a two-way radio with a higher capacity battery may be needed. Mobile phones only really have two states, in call or on standby (in use or not in use). However, radios have three states, in-use where it's transmitting, receiving a call or on standby.

Figure 5.5 below shows the comparison of battery life measurement data in between conventional method of RF PA design and gain stage controlled method. The data shows there is a battery life improvement of 40% in average from 0.5 to 6.5W

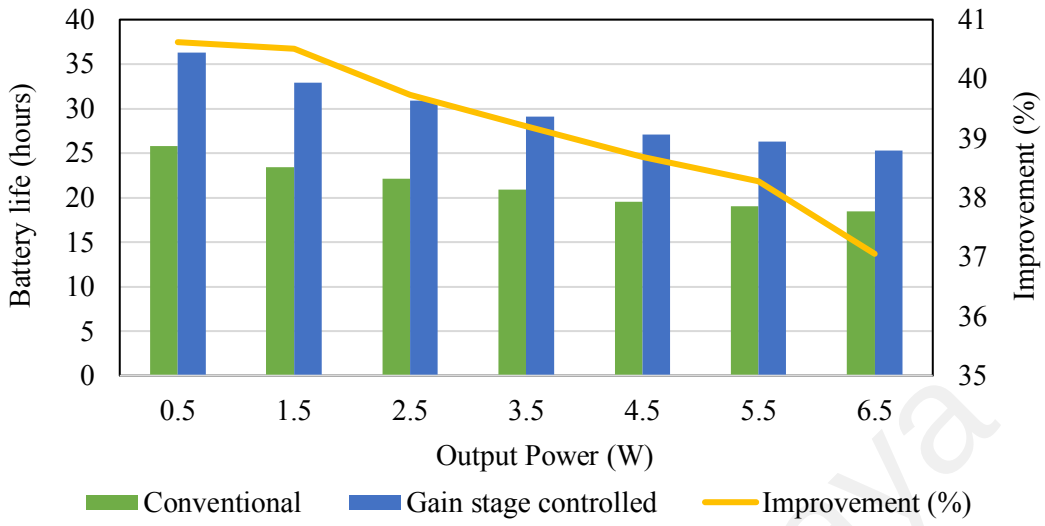


Figure 5.5: Battery life measurement data under 5-5-90 duty cycle

5. 3 Fast Transient Energy Ramping

5.3.1 Accuracy Current Sensing with respect to RF Power

In order to track and maintain RF output power in terms of transient and steady response, respectively, a closed-loop feedback having accurate sensing mechanism coupled to the PA is proposed. Few available sensing mechanism typically are power and VSWR sensing (Serhan et al., 2015) (Kosaka et al., 2014) (C. Chen, Chen, & Wang, 2013), however, this is an expensive solution and requires huge size area. For instance, power sensing approach needs RF sampling circuitry and RF to low frequency converter (Shao et al., 2014). Nevertheless, DC current sensing is an alternative approach due to the fact this is simple, requires low size area and low cost approach. The following paragraph will give an explanation of DC current sensing accuracy with respect to RF output power.

Typically the FET device is biased to a quiescent point beyond the class A and towards cutoff. It is clear that sufficiently large amplitude of RF drive will swing the

device beyond its cutoff point V_t, on the negative portion of the RF cycle (Zai, Dongxue, Schafer, & Popovic, 2014). It is clear also that in order for the current to swing up to idealized saturation point, I_{max} the drive level has to be increased from class A (Zai et al., 2014). The current in the device has truncated sine-wave appearance. The conduction angle $\alpha/2$ indicate the proportion of RF cycle for which conduction occurs.

In this paper, it will be assumed that the quiescent bias point is varied RF input drive is fixed. Thus, I_{max} is not maintained as explained in (Zai et al., 2014). The work is extended with a Fourier analysis of the waveform to evaluate DC and fundamental AC components of the drain current. The RF current waveform can be expressed as:

$$i_d(\omega t) = I_{DQ} + I_m \cos(\omega t), \quad -\frac{\alpha}{2} < \omega t < \frac{\alpha}{2} \tag{5.7}$$

$$= 0, \qquad \frac{\alpha}{2} < \omega t < 2\pi - \frac{\alpha}{2}$$

where $$I_{DQ} = \frac{-I_{\max}\cos(\frac{\alpha}{2})}{1-\cos(\frac{\alpha}{2})} \tag{5.8}$$

and $$I_m = \frac{I_{\max}}{1-\cos(\frac{\alpha}{2})}. \tag{5.9}$$

Substituting equation (5.8) and (5.9) into (5.7) leads to

$$i_d(\omega t) = I_m[\cos(\omega t) - \cos(\frac{\alpha}{2})] \tag{5.10}$$

FET drain current waveform for any conduction angle is illustrated in Figure 5.5. Two first output current components, DC and fundamental can be evaluated through Fourier series expansion with sufficient accuracy. The DC (I_{DC}) and fundamental AC current (I_1) can be deduced as following:

$$I_{DC} = \frac{I_m}{2\pi}[2\sin(\frac{\alpha}{2}) - \alpha\cos(\frac{\alpha}{2})], \text{ and} \tag{5.11}$$

$$I_1 = \frac{I_m}{\pi}[-\cos(\frac{\alpha}{2})\sin(\frac{\alpha}{2}) + \frac{\alpha}{2}]\cos(\omega_o t) \cdot \tag{5.12}$$

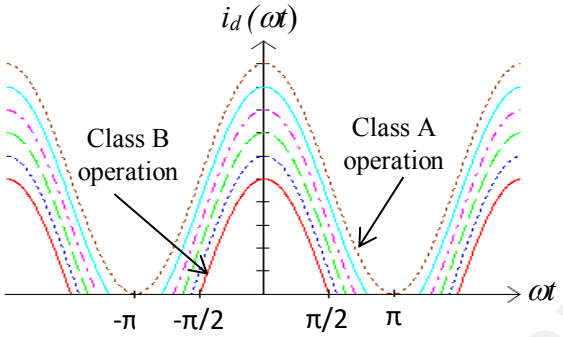


Figure 5.6: FET drain current waveform for fixed I_m

The results from the evaluation of these integrals are summarized in Figure 5.6. In order to maintain the fundamental RF energy (I_1^2R), I_{DC} tracking is sufficient since the relation has linear proportional as shown in Figure 5.7. This is strong evident to highlight that DC current sensing is adequate to maintain RF output power from the PA. Furthermore, this approach is not frequency dependent which can mitigate the need of RF sampling circuitry such as a directional coupler.

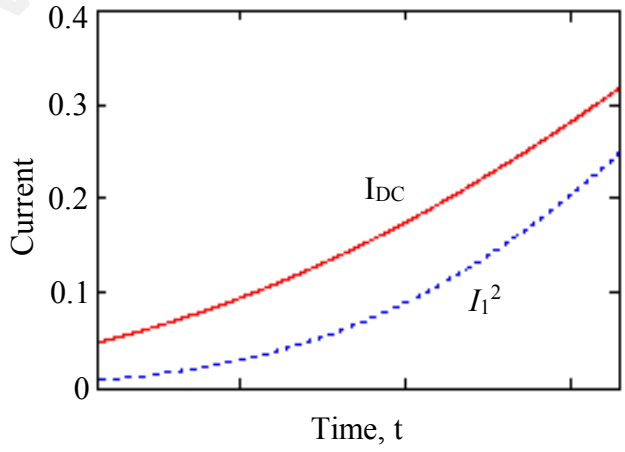


Figure 5.7: DC (red colour) and fundamental AC component with squared (blue colour)

5.3.2 Transient Response Analysis of Integrator Circuit

In next generation of two-way radio applications, especially for digital radio, the rate of change of output power must be controlled to ensure minimum transient energy at adjacent channel frequency, which is inversely proportional to the rate of power change (Narendra, Mediano, et al., 2008). The European type approval (ETS) body has set a tight specification for the transient power response and ACTP which are less than 1.5 ms and -50 dB, respectively. In the protocol is dictated a requirement for a fast rate of change of power while meeting the requirement of ETS specification of ACTP, indeed this is a real challenge task.

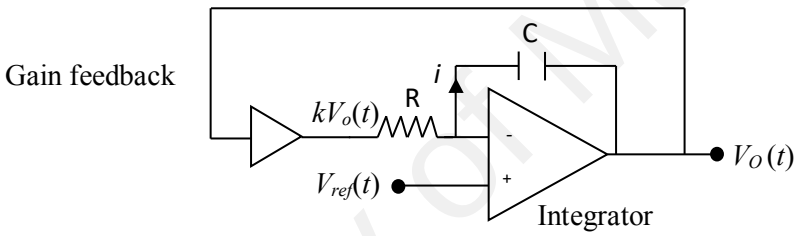


Figure 5.8: A basic closed-loop feedback integrator with RC elements

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This section discusses on the transient response control of the integrator using *RC* time constant to determine the transient slope of the output response $V_O(t)$. Few papers have discussed on the transient study of the PA as given in (Kamel, Mohieldin, Hasaneen, & Hamed, 2017) (Chi et al., 2015) (England et al., 2013). As a start a basic understanding of the integrator is presented in Figure 5.8. Any shape of V_{ref} signal is applied at the non-inverting input of the operational amplifier. The $V_O(t)$ is sampled and coupled to the gain feedback (to the inverting input of the operational amplifier).

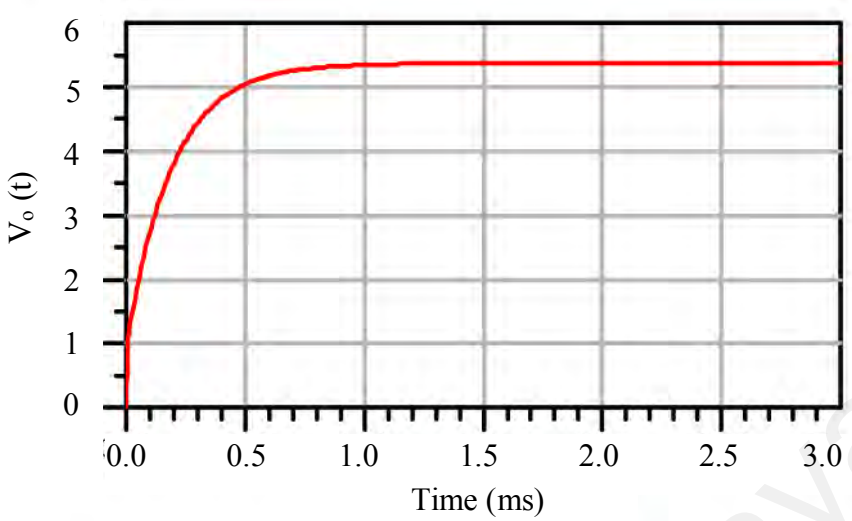

Figure 5.9: Output voltage characteristics of closed loop integrator with feedback

The basic circuit as shown in Figure 5.8, we need to show a basic mathematic using Laplace's equation (Dyke, 2014). The V_{ref} is defined as $Au(t)$, where $u(t)$ is step voltage. The current i flows across the capacitor C is the rate of voltage charge across it with respect to the time, thus

$$i = \frac{Au(t) - kVo(t)}{R} = C\frac{d}{dt}[Vo(t) - Au(t)] \tag{5.13}$$

$$\frac{d}{dt}Vo(t) + \frac{kVo(t)}{RC} = \frac{Au(t)}{RC} + A\delta(t) \tag{5.14}$$

Taking a Laplace transform of (16),

$$sVo(s) - Vo(0^-) + \frac{kVo(s)}{RC} = \frac{A}{RCs} + A \tag{5.15}$$

One can define $Vo(0^-) = 0$ since no charge in capacitor before t=0, thus

$$Vo(s) = \frac{sA + c}{s(s + b)} \tag{5.16}$$

where $b = \frac{k}{RC}$ and $c = \frac{A}{RC}$, and using partial fraction expansion

$$Vo(s) = \frac{X_1}{s} + \frac{X_2}{s+b} \tag{5.17}$$

Solving (5.17),

$$Vo(s) = \frac{\left(\frac{c}{b}\right)}{s} + \frac{\left(A - \frac{c}{b}\right)}{s+b} \tag{5.18}$$

and taking inverse Laplace transform of (5.18),

$$Vo(t) = \frac{A}{k}u(t) + A\left(1 - \frac{1}{k}\right)e^{-\frac{kt}{RC}} \tag{5.19}$$

From (5.19), a simple step unit response shape is given at V_{ref}, the voltage response of the V_o(t) can be dictated as shown in Figure 5.9. This is good start of the analysis to understand of the $V_o(t)$ behavior with present of V_{ref} . Nevertheless, the analysis can be used to explain complex signal of V_{ref}.

5.3.3 Integration of closed-loop DC sensing and transient circuitry

Integration of closed-loop DC sensing with gate voltage shaping V_{ctrl} is highlighted Figure 5.10. The DC current of the PA is sensed by the current sense resistor. The sensed current is then converted to a voltage by the *I-V* converter.

The sensed voltage is then compared against the V_{ref}. The error voltage that is generated during the comparison is integrated by the integrator to generate the control voltage of the amplifier. The V_{ctrl} will be adjusted until the desired current is achieved.

The V_{ref} known in state-of-art (i.e. sinusoidal, Gaussian, and root-raised cosine) is used as the transient reference voltage (Junrui & Liao, 2009). This response is integrated by the integrator such that the rise and fall time of the power response is gentle enough to meet the ETS transient splatter. The integrated error voltage due to the shaped V_{ref} resulted in a higher order shaped power response. The output transient response of closed-loop integrator is determined due to the response of V_{ref} and V_{det} (Kusuda, 2016), where V_{det} is the detection voltage from the DC current (tie to the PA). This is valid explanation since fundamental RF current has linear function with respect to the DC current sensed.

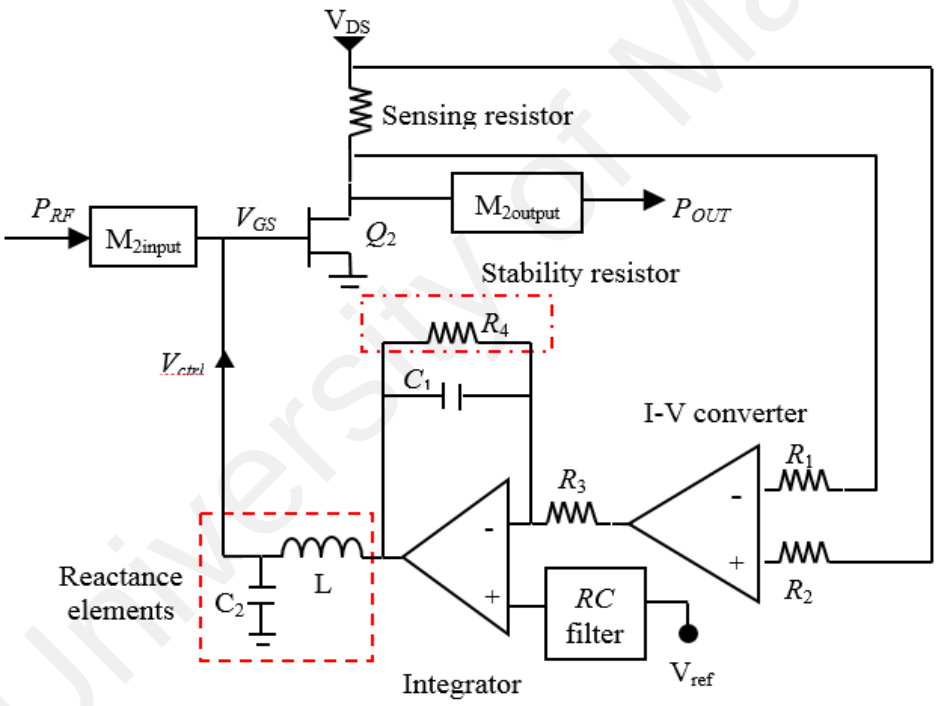

Figure 5.10: Simplified closed loop transient and DC sensing RF power

5.3.4 Characterization of the transient integrator circuit and practical issues

The V_{ref} provides a time dependent pre-defined voltage characteristic that supplies a time varying ramp up transition reference voltage during a transition from zero volts to

a steady state condition. The shape of the ramp up transition is substantially any shape of the signal e.g. sinusoidal or any complex shape. There is also a substantially sinusoidal ramp down transition for removal of the voltage V_{ref}.

Below the PA threshold voltage, V_{ctrl} response will be the integration of the V_{ref}. However, above the PA threshold, the V_{ctrl} response will change which typically become gentler in shape due to the V_{det} response (the PA started to turn on). The boundary condition must take into account to control the rate of change of power. In experimental test, as given in Figure 5.11, with a step function shaped V_{ref} the amplifier Q_2 power and voltage response rise too rapidly as shown in the blue and turquoise trace respectively. This response will generate excessive ACTP and could not meet the specifications. With a sine wave ramp of V_{ref}, the integration output has created a second order power and voltage response as shown in the violet and red trace respectively. This response can meet the ETS specification. The measured data of this scheme is shown below. However, the shape of the V_{ref} must be determined based on the PA device characteristics such as threshold level. Certainly this approach give flexibility to the designers to optimize the software instead of tedious optimization in board level

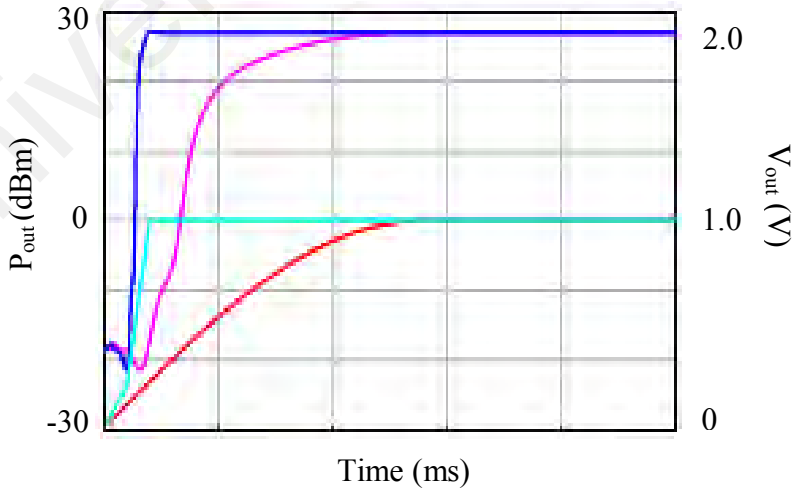

Figure 5.11: Experimental characterization of the output power from Q_2 due to step function and sine wave ramp of V_{ref}

During the product testing stage, software ramping profile is developed. Due to limitation of number of points of software ramping profile from digital to analog converter IC, a step interval is introduced, see Figure 5.12. Higher step resolution can be minimized or filtered with low pass filter network. Therefore, a basic low pass filter with *RC* is implemented at the non-inverting input of integrator to smoothen the shape of ramping without much delay, as shown in Figure 5.12. The ramping voltage V_{ref} was smoothened with the low pass filter. Green color is referred to voltage from digital to analog converter IC and red color is output of low pass (input to the integrator). However with optimization of *RC* filter, the ramping time can be kept within the specification.

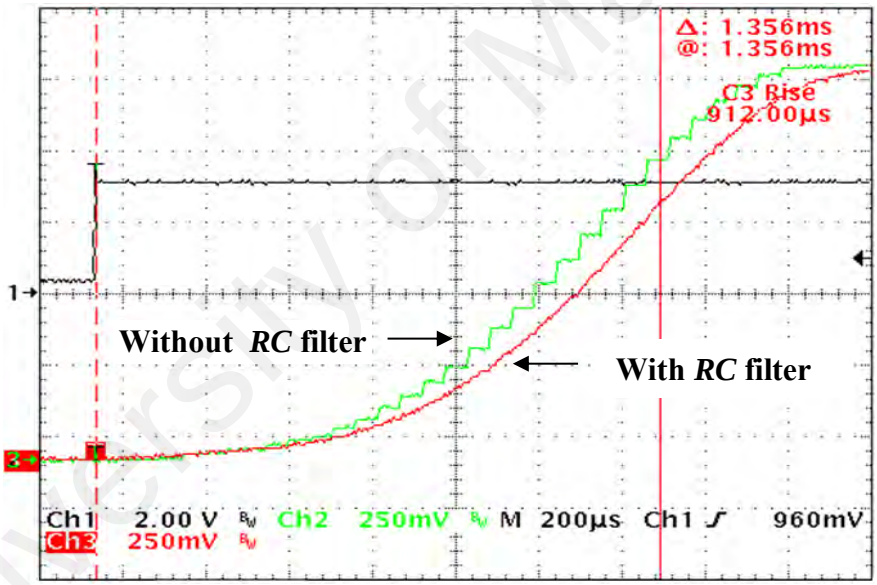

Figure 5.12: Ramping voltage with (red color) and without (green color) the RC filter

Additionally, with the integrator, the output voltage is oscillating during the transient response. The output of the operational amplifier is connected to RF choke and bypass capacitor (reactance elements in Figure 5.10). The load of reactance element would interact with operational amplifier‘s output resistance to create additional pole and

caused the operational amplifier to be unstable (Narendra et al., 2009). However, to resolve this issue a pull up resistor at output of op amp is needed (Figure 5.13). The value of stability resistor (approximately 100 Ω) was chosen to compromise between stability and ramp timing of the output voltage. Refer to Figure 5.13 for the stability of output voltage with and without the stability

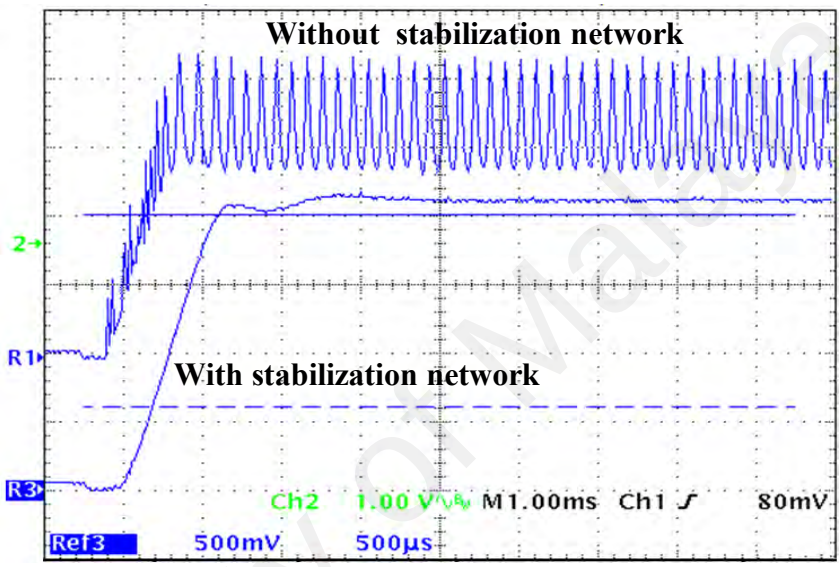

Figure 5.13: Output voltage of integrator with and without stability compensation

5.4 Measurement results

Complete schematic design of the closed-loop adaptive RF PA can be referred to Figure 5.14. In order to experimentally validate the proposed technique, a prototype board of the design using multi-layers FR4 material has been fabricated. Open grounding area with adequate via-hole, and DC / RF routing are well isolated in PCB for minimum spurious. As part of EMC requirements, it is necessary to have the DC layer below the RF grounding layer. This is to avoid DC noise couple into RF signal which can cause spurious emissions. The thickness of the DC routing is computed to carry adequate DC current to feed the appropriate transistor.

The DC biasing terminals are bypassed to ground with multiple chip capacitors (e.g. 100 pF, 33 nF, 10 uF) for each transistor. To make placement of the components, top and bottom of the PCB layout are utilized. The photograph of the prototype board is given in Figure 5.15, where (a) is referring to the low frequency and DC sections; i.e. operational amplifiers, (b) the placement of the RF section; Q_1 and Q_2 devices and RF matching network. Heatsink is mounted at the bottom of PCB to provide good heat from the PA. The capacitors represent ceramic and tantalum type, and inductors represent air wound type.

Measurement results of PA current and PAE across wide power levels (0.5 W to 6.5 W) are shown in Figure 5.16. Constant PAE of 44% (flatness of ±1%) across 0.5 W to 6.5 W is demonstrated experimentally for a frequency range of 400 to 500 MHz (Figure 5.15 which is referring to 430 MHz). The PA current is the key contributor of the total current in the radio system. At low power operation, for instance at 0.5 W, the PA current is approximately 0.4 A, that translating battery life improvement by 40% compared with the conventional method.

The gain of the PA system line up (Q_1 and Q_2, respectively) across power level is shown in Figure 5.17. The gain is quite constant across the power level. It demonstrated high gain about 31 dB over the wide dynamic power level.

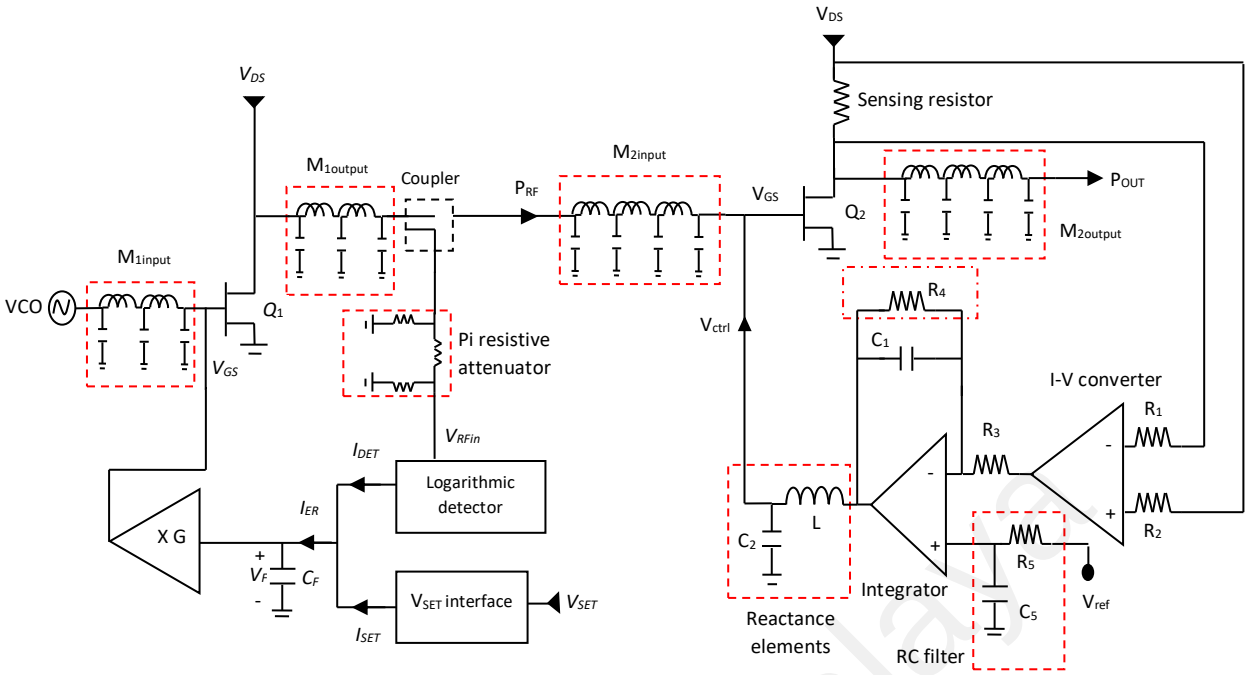

Figure 5.14: Full schematic of the closed-loop adaptive RF gain stage controlled circuitry with logarithmic RF power detector integrated with closed loop transient and DC sensing

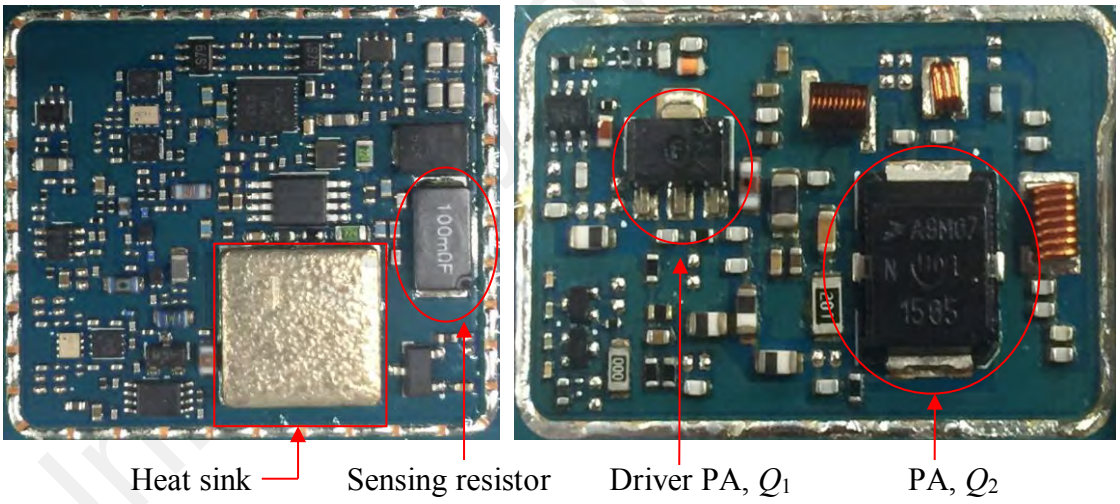

Figure 5.15: Prototype board of the closed-loop adaptive LDMOS PA (a) bottom side: DC current sensing and transient voltage shaping; (b) top side: RF

However, a slight decrease in gain was experienced below 3 W (it is corresponding to the drain supply set to 4.8 V which was already predicted through

calculation and simulation due to the g_m dropping of the device in this region). The g_m can be boosted with some incremental of gate biasing.

The power performance of the close-loop PA over the wide frequency is characterized. As shown in Figure 5.18, good bandwidth performance is achieved within 400-500 MHz. The gain performance is approximately 30 dB and efficiency more than 46% across bandwidth tare achieved. However, due to the bandwidth operation associated to the coupler and matching networks, the overall system bandwidth can be improved with sutale design technique such real-frequency technique (RFT) (Aridas, Yarman, & Chacko, 2014)

Measured example spectrum of complete ramping up and down, together with transient ACTP performance is recorded in Figure 5.18 with Agilent PSA Series Spectrum Analyzer E4445A. The results of transient power ramp and adjacent channel power for wide frequency range are summarized in Figure 5.19. The ramp and down timing is about 1.1 ms (within the ETS specifications) across the entire frequency range. ACTP result for 12.5 kHz is more than -50 dB over the frequency band.

Stable operation without parasitic oscillations is provided with feedback network and gate loading resistor at the input of the amplifier. The feedback value of 100 Ω (resistor) and 0.1 μF (ceramic capacitor) are predicted in design level. Gate loading resistors of 2 Ω (in parallel form) are placed at gate of the amplifier. In addition, a ferrite bead is implemented at drain line together with 10 uF (tantalum capacitor) and 22 pF (ceramic capacitor) as a precaution of low frequency parasitic oscillation. A crucial stability test with termination of 10:1 VSWR. was carried out. No oscillation is reported under this condition and the power amplifier operation is very stable. Robustness test is performed in measurement level with termination of 10:1 VSWR with continuously transmission for 20 minutes. Refer to Figure 5.20 for the stability spectrum of the PA

system at 400MHz. Refer to Appendix C for measurement setup to measure PA output power, gain and efficiency. Refer to Appendix D for measurement setup to check PA stability

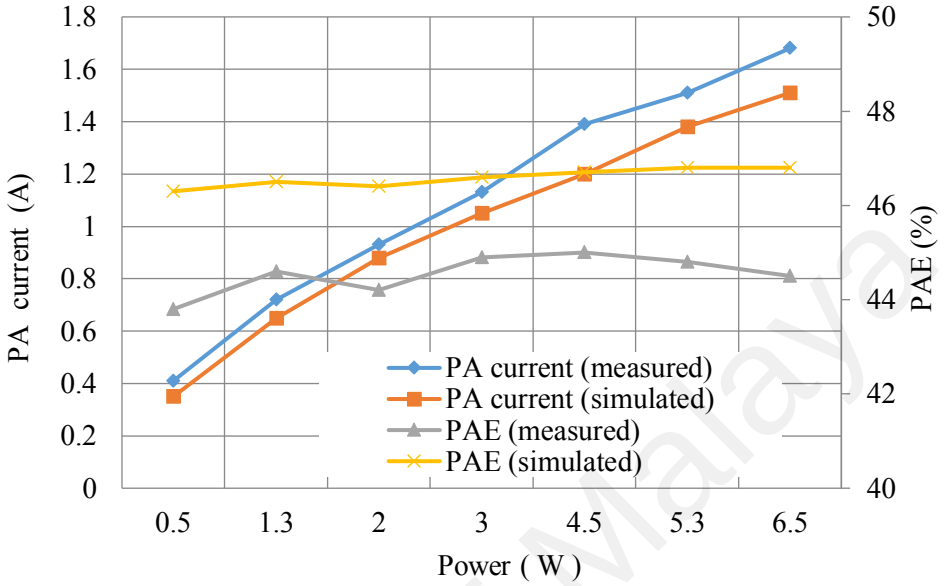

Figure 5.16: Comparison between measured and simulated results of the PA current and PAE of the PA across wide power level at 450 MHz

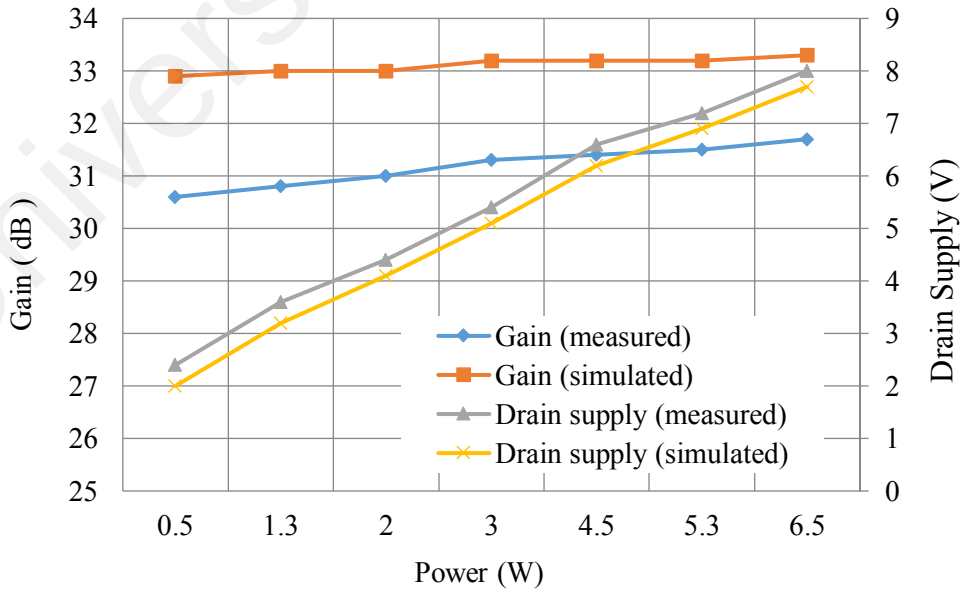

Figure 5.17: Comparison between measured and simulated results of gain and drain supply voltage of the PA across wide power level at 450 MHz

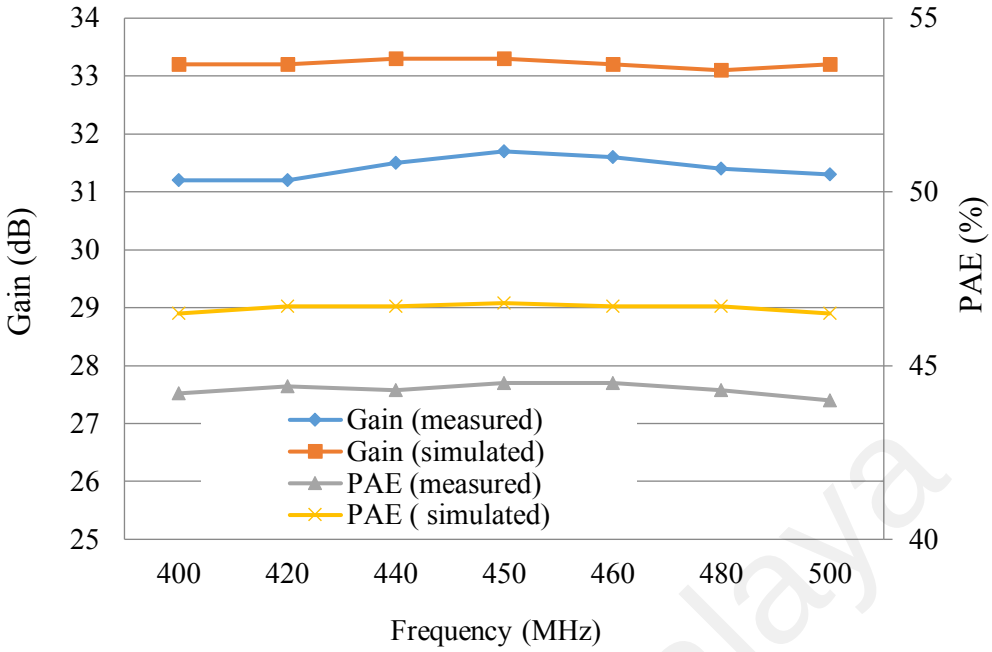

Figure 5.18: Power performance of the closed-loop PA system across bandwidth operation

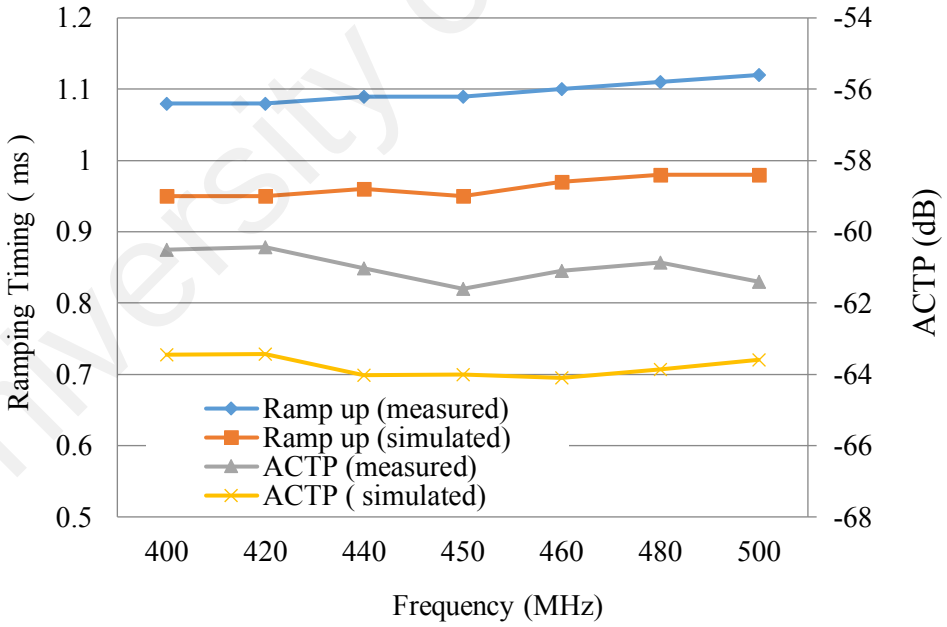

Figure 5.19: Comparison between measured and simulated result of ramping up timing (ramping down timing similar to the ramping up) and ACTP from 400 – 500 MHz

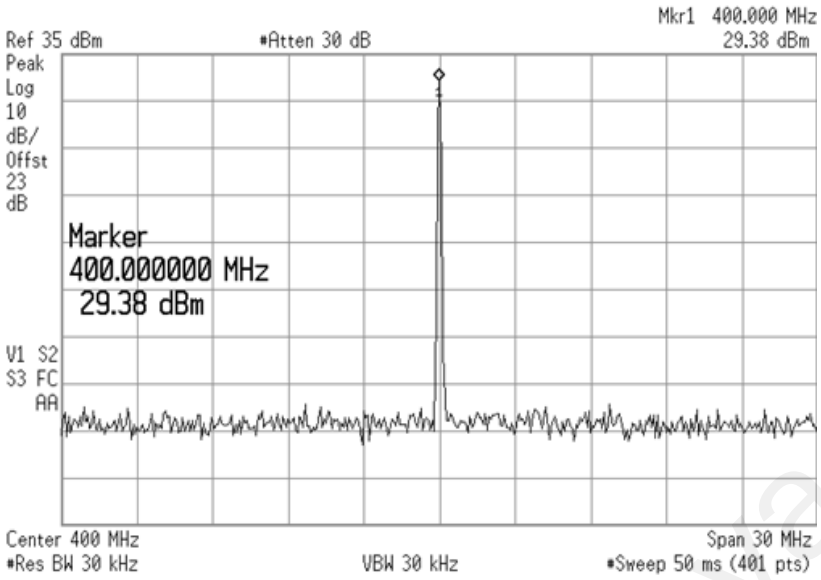

Figure 5.20: Example of measured of power spectra at 400 MHz and there is no oscillation is reported

5.5 Conclusion

A novel closed-loop adaptive PA design to provide constant efficiency across wide power level and fast power ramping from noise level to steady state while meeting ACTP is introduced here. For the constant efficiency, gate stage controlled with logarithmic detector is proposed. As for the fast transient power, the time of the ramping is achieved with integration of the PA current sensing and voltage shaping algorithm. A prototype board is developed and measurement results demonstrated good performance; constant efficiency (48%) across 0.5 to 6.5 W and transient timing response of 1.1 ms is achieved while maintaining good ACTP of less than -50 dB over the frequency range of 400 to 500 MHz. This work allows the public safety and mission critical two-way radio products been accepted widely since the users have the platform for building interoperability into their systems. Since transmitting is the most energy intensive operation, the adaptive RF PA design can typically function 40% longer in terms of battery life than the non-adaptive conventional architecture of two-way radios.

CHAPTER 6: CONCLUSIONS AND FUTURE WORK

6.1 Overview

The objectives of this thesis work is to investigate innovative design solutions for transmitter architecture for 2 way portable radio which provide high efficient and fast transient response with adaptive power operation. Besides these basic requirements, future 2 way radios need to provide multi-band operation which requires adjustments in the broadcast frequency. For base station amplifiers emphasis is put on linear and efficient operation at very high output power levels (> 80W), while operating with signals that are characterized by a high peak-to-average power ratios.

6.2 Overall conclusions

In order to achieve the research objectives, the traditional class AB amplifier is first considered and searched for ways to make this his power operation mode to have high efficiency without scarifying its linearity. In view of this, a new broadband high performance power amplifier (PA) line up for mobile radio applications is presented. The key design of the PA line up is final PA, where design methodology employing load-pull technique and new generation LDMOS device technology are adopted. Large-signal stability analysis, in specific pole-zero identification technique is employed to investigate oscillation before build the prototype board and this verified in measurement level. Practical design consideration for high power including thermal design aspect is discussed. Experimental results demonstrated output power of ~80 W and gain of 42 dB, while preserving efficiency of 55% over the bandwidth from 760-870 MHz.

Chapter 4 introduces a technique to predict transient behavioral response of RF PA, whereby a novel topology with of DC current sensing and voltage shaping algorithm is proposed. An accurate transient behavioral modeling including ramping energy from

noise level to steady state level, and adjacent channel transient power (ACTP) established high degree of correlation with measurement level for wideband RF PA operation (400-520 MHz). Experimental results demonstrated good performance; transient timing response of 1 ms is achieved while maintaining good ACTP of less than -60 dB over the wide frequency range of 400-520 MHz.

Chapter 5 explains a novel closed-loop adaptive PA design to provide constant efficiency across wide power level. Fast power ramping technique from noise level to steady state while meeting ACTP measurements are also presented here. For the constant efficiency, gate stage controlled with logarithmic detector is proposed. As for the fast transient power, the time of the ramping is achieved with integration of the PA current sensing and voltage shaping algorithm. A prototype board is developed and measurement results demonstrated good performance; constant efficiency (48%) across 0.5 to 6.5 W and transient timing response of 1.1 ms is achieved while maintaining good ACTP of less than -50 dB over the frequency range of 400 to 520 MHz. This work allows the public safety and mission critical two-way radio products been accepted widely since the users have the platform for building interoperability into their systems. Since transmitting is the most energy intensive operation, the adaptive RF PA design can typically function 40% longer in terms of battery life than the non-adaptive conventional architecture of two-way radios.

In a nutshell, in this work a transmitter architecture for 2 way radios is designed to meet the requirements of professional organizations that need a mission critical communication solutions. The next generation radio design meets the many capabilities and features as explained in Chapter 1 earlier. Looking into the demand, next generation 2-way radio will continue to be the technology of choice tomorrow. This research work enables the next generation 2-way radio to bring together real world experience, customers' insight and technological innovations. With new design models, the

transmitter architecture brings a whole range of new capabilities to make the communication more efficient and more productive.

6.3 Future work

One of the saying in the wireless communication community today is the Software Defined Radio (SDR). The concept of SDR as visualized by the author in (Pawlan, 2015) consists of a transmitter that is capable of characterizing the propagation path, adapt the signal to best suit the propagation environment, set the optimal power level of the signal to be transmitted before the actual transmission takes place. Likewise the receiver should be able to detect the frequency of the broad casted signal of interest.

It is clear from this description that such an implementation will require tremendous amount of computing power for the signal processing and control (FPGAs and DSPs are usually deployed). On the RF/analogue end, the challenge is to move the digital interface as close to the antenna as possible. For the transmitter, the ideal situation would be to just have the power amplifier stage as the only remaining analogue part, which is directly driven by fast (D/A) converter. As such, the proposed SDR architecture these days uses a digital IF interface, where channel selection and filtering can done in digital domain. To easily change operating frequency and make band-switching feasible, low loss tunable matching elements are required (Gómez-García et al., 2017) (Kamaleldin et al., 2017) (Yüksel et al., 2017).

It is clear from the explanation given in this section, that following a SDR approach brings performance advantages since it relaxes design specifications on the analogue/RF part as error can be corrected easily within the software. It is therefore our expectation that the future of RF power amplifier will be in the SDR domain, where full use of the advancements in digital signal processing will result in power amplifier that

are more efficient, more linear and reconfigurable (Liang, Zhao, Chu, & Chen, 2017). Consequently, the day that a typical RF amplifier will have a digital I-Q baseband inputs is closer than ever before.

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