

**DESIGN OF LOW POWER FRONT-END RECEIVER FOR  
BLUETOOTH LOW ENERGY/ZIGBEE IN NANO-SCALE  
CMOS TECHNOLOGY**

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FOR BLUETOOTH LOW ENERGY/ZIGBEE IN NANO-  
SCALE CMOS TECHNOLOGY**

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**DISSERTATION SUBMITTED IN FULFILMENT OF  
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Field of Study: ELECTRONIC

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# **DESIGN OF LOW POWER FRONT-END RECEIVER FOR BLUETOOTH LOW ENERGY/ZIGBEE IN NANO-SCALE CMOS TECHNOLOGY**

## **ABSTRACT**

With the increasing need for the internet of things (IoT), Bluetooth low energy (BLE) and ZigBee standards have become popular solutions for wireless devices. In the tremendous growth of wireless application, low voltage and low power consumption have become a major consideration in radio frequency integrated circuit (RFIC). The development of low power transceiver is driven by the need of withstanding longer battery life time and reduced cost, catering towards mobile application. The continuous downscaling of deep-submicron CMOS technologies to reduce overall power consumption and enable high frequency operation outlays design challenges in the construction of RF front end blocks, which results in less voltage headroom available for circuits to operate. This has driven the need in exploration of new low power/low voltage design technique for RF architecture. The performance of a receiver is dependent on that of the individual blocks such as low noise amplifier (LNA), mixer and voltage controlled oscillator (VCO). This dissertation focuses on the design and implementation of a 1.5V ultra-low power 2.4-GHz CMOS receiver powered by a coin battery. The proposed receiver is relaxed in the use of a low dropout regulator (LDO). By effective merging of the quadrature low noise amplifier (QLNA), in phase and quadrature (I/Q) mixers, VCO and trans-impedance amplifier (TIA) in one cell, while removing the LDO, the available 1.5-V voltage supply is fully utilized for current reuse between blocks, minimizing the dc current consumption. Specifically, a quadrature LNA operating as both common-source and common drain topologies provides the I/Q outputs in the RF signal path. The forward body bias technique is applied to the transconductance stage of the I/Q mixers to relax its voltage headroom consumption. Implemented in 180-nm CMOS technology, the receiver exhibits a conversion gain (CG) of 24 dB, a noise figure (NF) of 13.8 dB and an input-referred

3rd-order intercept point (IIP3) of -14 dBm while consuming only 2 mA. The phase noise of the VCO is -118.5 dBc/Hz at 2.5 MHz offset. The low-cost technology and low current consumption renders the receiver suitable for Internet of Things (IoT) devices using the Bluetooth Low Energy (BLE) or ZigBee standards.

Keywords: CMOS, IQ Receiver, Low power, ZigBee, Bluetooth low energy (BLE).

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**REKA BENTUK PENERIMA BAHAGIAN DEPAN BERKUASA RENDAH  
UNTUK BLUETOOTH TENAGA RENDAH / ZIGBEE DALAM TEKNOLOGI  
CMOS SKALA-NANO**

**ABSTRAK**

Dengan peningkatan keperluan internet IoT, piawai Bluetooth tenaga rendah (BLE) dan ZigBee telah menjadi penyelesaian yang popular untuk peranti tanpa wayar. Dalam pertumbuhan aplikasi tanpa wayar yang tinggi, voltan rendah dan penggunaan kuasa rendah menjadi pertimbangan utama dalam litar bersepadu frekuensi radio (RFIC). Perkembangan pemancar-penerima kuasa rendah didorong oleh keperluan masa hayat bateri yang lebih lama dan pengurangan kos, memenuhi keperluan aplikasi mudah alih. Pengcilan skala berterusan teknologi CMOS untuk mengurangkan penggunaan kuasa keseluruhan dan membolehkan operasi frekuensi tinggi menghasilkan cabaran kepada reka bentuk pembinaan blok bahagian depan RF, akibat voltan yang kurang untuk litar beroperasi. Ini telah mendorong keperluan dalam penerokaan teknik reka bentuk baru untuk seni bina RF. Prestasi penerima bergantung kepada blok individu seperti penguat hingar rendah (LNA), pencampur dan pengayun terkawal voltan (VCO). Disertai ini memberi tumpuan kepada reka bentuk dan pelaksanaan penerima CMOS 2.4-GHz kuasa ultra rendah 1.5V yang dikuasakan oleh bateri syiling. Penerima yang dicadangkan adalah santai dalam penggunaan pengatur cecir rendah (LDO). Dengan menggabungkan secara efektif penguat hingar rendah kuadrat (QLNA), pencampur dalam fasa dan kuadrat (I / Q), VCO dan penguat trans-impedan (TIA) dalam satu sel, dengan LDO dikeluarkan, bekalan voltan 1.5-V yang tersedia digunakan sepenuhnya untuk penggunaan semula arus antara blok, meminimumkan penggunaan arus dc. Secara khususnya, LNA kuadratur beroperasi sebagai kedua-dua topologi sumber sepunya dan salir sepunya, menyediakan output I / Q dalam laluan isyarat RF. Teknik pincang badan ke depan digunakan pada peringkat transkonduktans pencampur I / Q untuk melonggarkan penggunaan ruang

kepala voltannya. Dilaksanakan dalam teknologi CMOS 180-nm, penerima mempamerkan gandaan penukaran (CG) 24 dB, angka hingar (NF) 13.8 dB dan titik pintasan tertib ke-3 (IIP3) merujuk masukan -14 dBm dengan hanya menggunakan 2 mA. Hingar fasa VCO ialah -118.5 dBc / Hz pada offset 2.5 MHz. Teknologi kos rendah dan penggunaan arus yang rendah menjadikan penerima sesuai untuk peranti IoT menggunakan standard Bluetooth Tenaga Rendah (BLE) atau ZigBee.

Kata Kunci: CMOS, Penerima IQ, Kuasa rendah, Zigbee, Bluetooth tenaga rendah (BLE).

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## LIST OF SYMBOLS AND ABBREVIATIONS

AC	:	Alternating Current
ADC	:	Analog-to-Digital Converter
AM	:	Amplitude Modulation
BER	:	Bit Error Rate
BiCMOS	:	Bipolar and CMOS
BLE	:	Bluetooth Low Energy
BPSK	:	Binary Phase Shift Keying
BT	:	Classic Bluetooth
CG	:	Conversion Gain
CMOS	:	Complementary Metal-Oxid -Semiconductor
CS	:	Common Source
dB	:	Decibel
dBm	:	Decibel with respect to 1mW
DC	:	Direct Current
DCQ	:	DC Quadrant
DMD	:	Dual-Mode Demodulator
DSSS	:	Direct Sequence Spread Spectrum
DUT	:	Device Under Test
ESD	:	Electrostatic Discharge
F	:	Noise Factor
FM	:	Frequency Modulation
FSPSM	:	Folded Semi-Passive Subharmonic Mixer
GFSK	:	Gaussian Phase Shift Keying
GND	:	Ground



GSGSG	:	Ground-Signal-Ground-Signal-Ground
Hz	:	Hertz
I	:	In Phase
IF	:	Intermediate Frequency
IIP3	:	Input-referred Third-order Intercept Point
IM	:	Intermodulation
IM3	:	Third – order Intermodulation
IoT	:	Internet of Things
IP3	:	Third-order Intercept Point
IQ	:	In Phase and Quadrature
ISM	:	Industrial, Scientific, and Medical
KCL	:	Kirchhoff's Current Law
KVL	:	Kirchhoff's voltage Law
LDO	:	Low Dropout Regulator
LNA	:	Low Noise Amplifier
LMV	:	LNA+Mixer+VCO
LO	:	Local Oscillator
LSB	:	Lower Side Band
MGLNA	:	Multiple-Gated Low Noise Amplifier
MIM	:	Metal-Insulated-Metal
MOS	:	Mosfet
NEF	:	Noise Excess Factor
NF	:	Noise Figure
NFA	:	Noise Figure Analyzer
NMOS	:	N-channel Mosfet
OIP3	:	Output-referred Third-order Intercept Point

QPSK	:	Offset Quadrature Phase Shift Keying
P1dB	:	1db Compression Point
PCB	:	Printed Circuit Board
PM	:	Phase Modulation
PMOS	:	P-channel Mosfet
PPF	:	Poly-Phase Filter
PVT	:	Process, Voltage and Temperature
Q	:	Quadrature Phase
Q-fac	:	Quality Factor
QLNA	:	Quadrature Low Noise Amplifier
QVCO	:	Quadrature Voltage Controlled Oscillator
RF	:	Radio Frequency
RFIC	:	Radio Frequency Integrated Circuit
RMS	:	Root Mean Square
S-Par	:	Scattering Parameter
SA	:	Spectrum Analyzer
SAW	:	Surface Acoustic Wave
SDC	:	Single-to-Differential Circuit
$S_i$	:	Silicon
SiGe	:	Silicon-Germanium
$(S_iO_2)$	:	Silicon Oxide
SNR	:	Signal-to-Noise Ratio
SSA	:	Signal Source Analyzer
SoC	:	System on Chip
TIA	:	Trans-impedance Amplifier
USB	:	Upper Side Band

UWB	:	Ultra-Wideband
VCO	:	Voltage Controlled Oscillator
VGA	:	Variable-Gain Amplifier
VNA	:	Vector Network Analyzer
WPAN	:	Wireless Private Area Network
WSN	:	Wireless Sensor Network
WUC	:	Wake-Up Circuit
$\Omega$	:	Ohm
$1/f$	:	Flicker Noise
$C_{gs}$	:	Gate-Source Parasitic Capacitance
$C_{ox}$	:	Gate Oxide Capacitance
$f$	:	Frequency in Hz
$f_T$	:	Transit Frequency
$G$	:	Power Gain
$g_m$	:	Transconductance
$L$	:	Length of Transistor
$S$	:	$j\omega$
$V_{th}$	:	Threshold Voltage of Transistor
$W$	:	Width of Transistor
$\omega$	:	Frequency in rad/s
$\omega_c$	:	Centre Frequency in rad/s

## **LIST OF APPENDICES**

Appendix A: Derivation of the input impedance of the QLNA

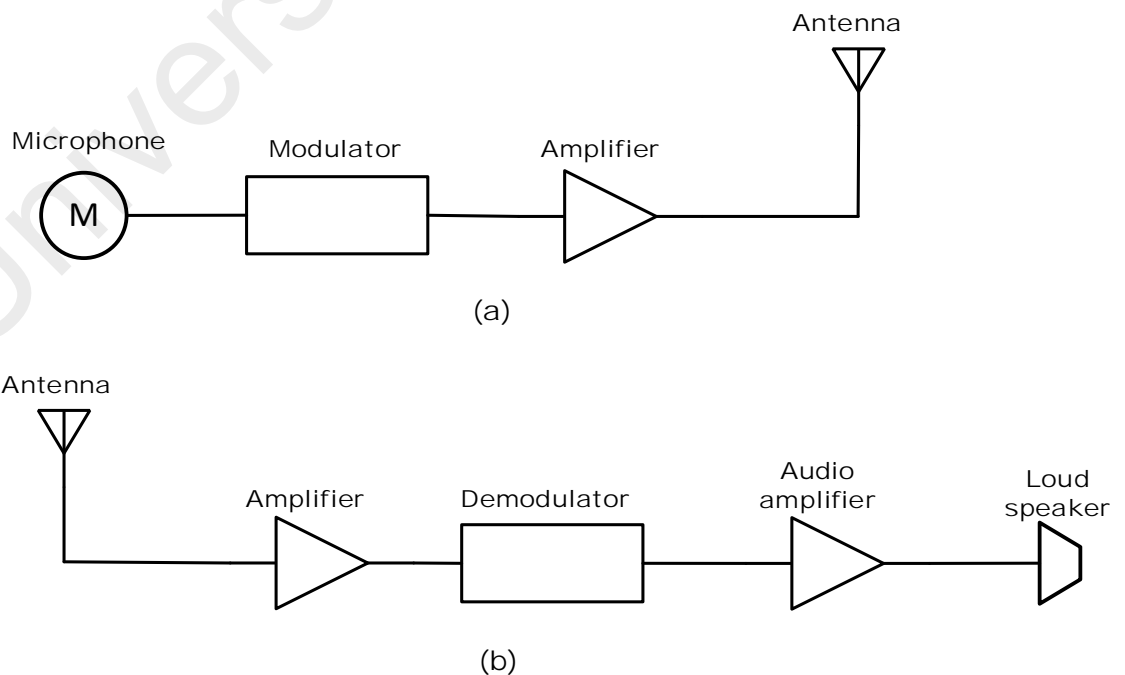
Appendix B: Derivation of the negative resistance of Nmos VCO and complementary VCO

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## CHAPTER 1: INTRODUCTION

Wireless communication is swiftly developing within the last few years. This form of communication is favoured instead of the traditional wired communication because it avoids the necessity of physical connection among multiple devices, therefore reducing system size and decreasing overall price (Iwai, 2000). A few other advantages due to wireless communication are it allows users to move freely, permits utilization of small size portable devices, can handle large amount of users due to no limitation by a specific number of port connections and instant transfer of information (Andreas, 2011).

A radio is an example of wireless communication as it enables information to be transferred wirelessly. This radio in its simplest form, consist of a transceiver which has a transmitter that transmits information to free space medium and a receiver that receives the information. Below is a simple block diagram of a wireless transceiver. In the transmitter side, voice/data (information) is detected via the microphone and converted to electrical signal. This signal with information is modulated onto a carrier. Then this



**Figure 1.1: Block diagram of radio (a): Transmitter, (b) Receiver**

modulated signal is amplified to a certain power level so that it can travel greater distances. This signal will then be delivered to the antenna which converts this electrical signal to electromagnetic radiation in the form of radio waves. These waves will then propagate through free space medium carrying the information along with them. In the receiver, the transmitted signal is received by the receiving antenna, but in a weak and susceptible state due to free-space path loss. The antenna converts the electromagnetic radio waves to electrical signal which is then amplified in order to boost the power level for ease of processing in the subsequent stages in retrieving the original information. This electrical signal is then demodulated from the carrier and sent to another amplifier to process it to an acceptable level. This signal is then dispatched to an output which converts the electrical signal back to voice information (Haesik, 2015b).

It can be observed that in the transmitting path, there is not much of a design challenge as the received signal is already in an acceptable form and simply needs to be boosted in power so that the signal can travel greater distances. But in the receiver path, the received signal will usually be very weak, distorted and with excessive levels of noise, hence it needed to be handled with care, so that the original information can be retrieved from the signal. Therefore, the receiver design normally is a challenging task in electronic systems (Tatsuo et al., 2001). This dissertation will focus on the receiver part of the front end radio for wireless communication.

## **1.1 Motivation**

In current years, the growth of wireless communication is fascinating. This growth is further aided with the continuous progress in the microelectronic discipline, which include enhancements on cost effective technology and development of new architectures, which gives rise to the wireless world we live in today (Al-Rousan & AlQurem, 2014). Previous decade saw the near complete integration of wireless

transceiver and the rise of complementary metal oxide semiconductor (CMOS) as the technology preferred to realize the system on chip (SoC) concept (Nishimura, 2000).

A SoC encompass two or more complex microelectronic component integrated in a single silicon die, where previously complex functionalities require large discrete components to be connected on a printed circuit board (PCB), which results in huge size. In order to connect multiple blocks in a PCB, usually a power hungry buffer is needed for optimum power transfer between blocks and impedance matching. Moreover, this buffers are lossy and bulky (Shaeffer & Lee, 1997). This SoC idea is further enabled due to the advances in CMOS silicon process technology permitting a complete system to be designed on a single silicon die. While technologies such as Silicon Germanium (SiGe) and Bipolar-CMOS (BiCMOS) provide better performance than CMOS for high speed analogue electronics, CMOS offers two crucial benefits which are lower cost, and the ability to be easily integrated with digital electronics in a single chip. Furthermore the rapid scaling of CMOS compare to SiGe and Bipolar-BiCMOS has brought in the analog and radio frequency (RF) performance on par with the other technologies in terms of speed and performance, providing the ability to easily integrate with the digital part thus realizing SoC (Nishimura, 2000). As CMOS technology scales down, performance and speed is improved drastically (Abou-Allam et al., 2000). One catch to the advantages are the price of the new node technologies which also increases proportionally. This phenomena impacts the overall cost of the chip and hence the

**Table 1.1: Price comparison of CMOS technologies node**

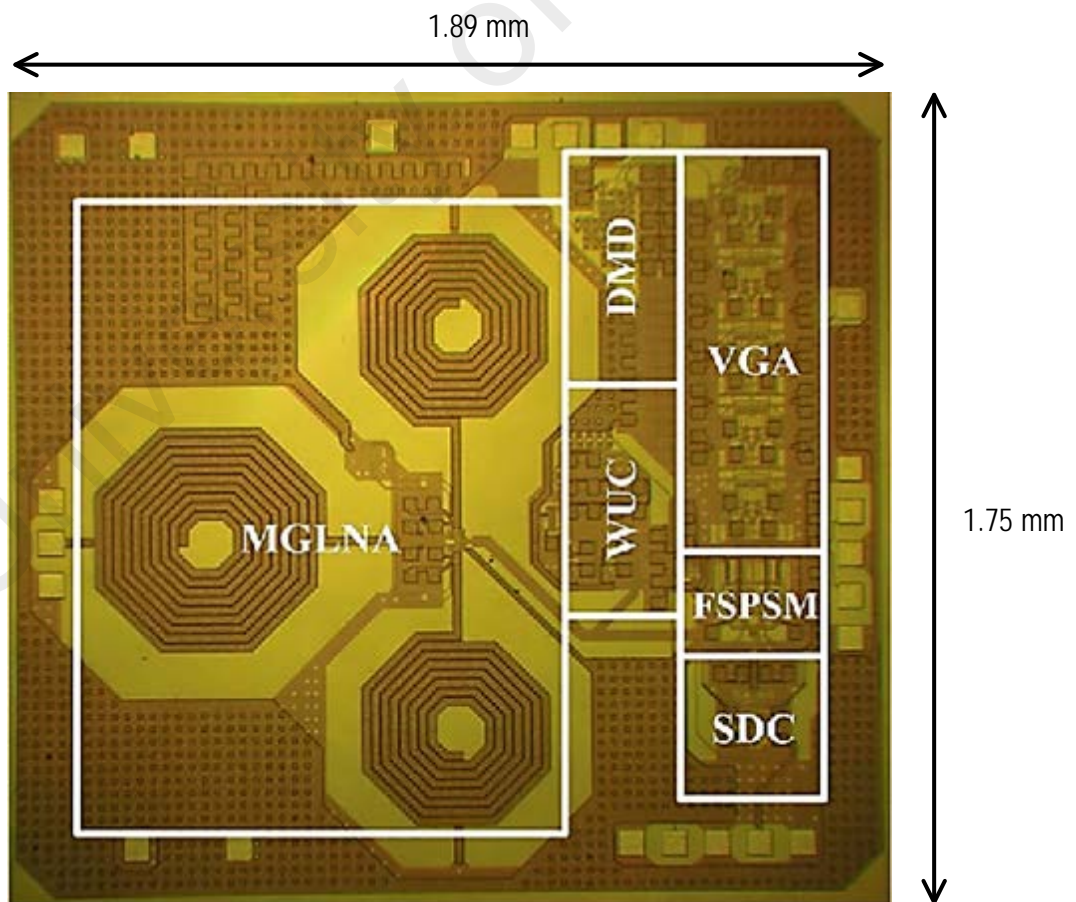
Technology (nm)	Price (USD,\$)
28	4,000/ $mm^2$
65	2,000/ $mm^2$
90	1350/ $mm^2$
130	750/ $mm^2$
180	300/ $mm^2$

consumer end product. Table 1.1 dispatches the comparison of different types of CMOS technology nodes and its price for CMC Microsystems foundry(Canadian Microelectronics Corporation, 2018). Consequently, a suitable node needs to be chosen, which gives balance in terms of cost and performance taking into account the desired operating frequency.

The "Internet of things" (IoT) is becoming an increasingly growing topic lately. It is a concept that not only has the potential to impact how we live but additionally how we work (Miraz et al., 2015). The IoT is made up of devices, from simple sensors to smartphones and wearables connected collectively. By combining these linked devices with automated systems, it is feasible to acquire information, analyze it and create an action to assist someone with a particular task, or learn from a process. In such a system, low cost and low power solutions are the main requirement to realize the IoT. It calls for smaller devices which store and transmit smaller packet data on a regular basis, in which longevity and portability are key requirements to be met. The wireless personal area network (WPAN) application is specifically designed for this, to permit circuit designers to attain new low levels of power consumption and cost (Allen, Bezzam, & Richmond, 1997). Two main standards in WPAN, which are ZigBee and Bluetooth low energy (BLE) will be studied more extensively in the following chapter. In ZigBee/BLE systems, the high density of units, formed by autonomous short range wireless nodes make the system more flexible and relaxes the sensitivity of the receiver. As a result, performance can be exchanged with the feasibility of having longer active usage and cost effective devices (Selvakumar et al., 2015). BLE/ZigBee based transceivers with its relaxed specifications, makes it ideal for reducing cost and power consumption, thus putting it as the front runner standard to realize IoT. Hence, the receiver to be designed in this dissertation will cater towards BLE and ZigBee compliant.



In the silicon world, area is reflected proportionally to cost. By reducing the active area of the silicon die, cost can be decreased, thus making the whole system small and portable. Figure.1.2 shows the teardown of a photomicrograph of a wireless CMOS receiver (Hsieh et al., 2016). It can be observed that inductors consume massive area of the silicon. However, these resonant elements are vital for narrowband applications such as ZigBee/BLE for low power consumption, low noise, good linearity and filtering. Power is likewise conventionally reduced via scaling the voltage supply (Tan et al., 2017), but in reality, most consumer end portable products are still powered by a coin cell battery which has nominal voltages around 1.5V and 3V (Emami, 2014). The difference in supply voltage requirements, dictates an extra component referred to as a low dropout regulator (LDO)



**Figure 1.2: Photomicrograph of a CMOS receiver (Hsieh et al., 2016)**

in order to supply the required voltage. The additional block increases the complexity of the design and introduce losses (Masuch et al., 2012). High efficiency and low cost alternate-off with each other. Use of resonant elements decrease power consumption, but an inductor free method saves die area, ensuing in cheaper devices. In a nut shell, the improvement of low power transceiver is motivated in the following areas:

- i. Low power consumption, in order that the system can withstand longer battery life time and be compatible with coin size battery.
- ii. Small active chip area, so that the product size will be small, catering in the direction of ease of mobility, portability and lower cost.
- iii. Low cost, as a way to be affordable to consumers
- iv. Multiple capabilities integrated in a single chip product, which realizes SoC and IoT.

To address the issues, the exploration of new design techniques in the RF front-end circuit is the prime motivation in executing this study and dissertation. In spite of the advances in low power receiver design, there is still adequate room for further power and cost reduction through both novel circuit design and system planning.

## **1.2 Objectives**

The main goals of this dissertation are to address the issues stated within the motivation part and is given as:

- i. To design a low power fully integrated receiver using a standard CMOS process which can comply with the required physical specification of IEEE 802.15.4 and BLE. The proposed receiver should achieve:
  - Low power consumption
  - Small size and low cost

- Multiple blocks fully integrated with no external components providing an SoC solution
- ii. Characterize the fabricated CMOS receiver and to verify its performance parameters against the theoretical/simulated results along with recent state of the art works.

### **1.3 Scope**

In this work, a 1.5-V, LDO free ultra-low power 2.4 GHz CMOS receiver for direct-powering by a coin battery specifically optimized for BLE and ZigBee applications is proposed. It is headed by a single-ended QLNA, which alleviates the need of an on-chip balun, while providing I/Q outputs. The resultant I/Q signals are routed to the cascaded single-balanced I/Q mixers which are driven with an LC VCO. The TIA is stacked on top of each mixer via current-reuse principal to complete the design. Low IF reception, 100MHz is chosen to lessen the flicker noise effect of CMOS devices, since the BLE and ZigBee are both narrowband standards. To validate the proposed concept and verify the simulation outcome, the design was fabricated using a commercial CMOS 180nm technology platform. On-wafer measurement using probe station equipped with a vector network analyzer (VNA), spectrum analyzer (SA), noise figure analyzer (NFA), signal generator, signal source analyzer (SSA), oscilloscope and parameter analyzer was performed to characterize the hardware.

### **1.4 Dissertation Organization**

This dissertation is divided into six chapters which are organized as follows:

The introduction to transceivers, motivations and objectives of this study are presented in chapter 1 along with the dissertation outline.

Chapter 2 provides a brief literature review. In order to gain a proper appreciation of the rest of the chapters, some fundamental concepts are first introduced in radio frequency integrated circuit (RFIC), followed by different possible wireless receiver architectures bringing up the pros and cons of each architecture. Then, the functions of each building block of the receiver, particularly the LNA, mixer and VCO is briefly explained. Subsequently, the BLE and ZigBee wireless technology standards are derived, accompanied by system level receiver specifications to be compliant with BLE and ZigBee standards. Further optimization methods such as quadrature generation techniques and body bias method are discussed at the end of this chapter. The chapter closes with a brief discussion of the state of the art designs.

Chapter 3 describes the circuit level design of the proposed receiver. Each building block of the proposed receiver is introduced and covered showing the design parameters trade-offs and design considerations for each circuit design executed, beginning from the system specifications right down to the circuit metrics. The analysis consist of the receiver front end QLNA, down-conversion IQ mixers, and complementary VCO.

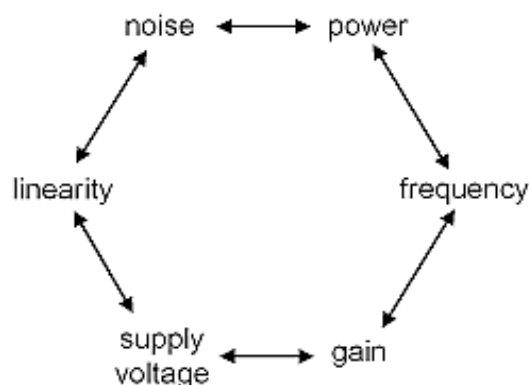
Chapter 4 starts with a brief of the measurement set up and equipment used for characterization of the proposed receiver chip. The measurements results are then presented and complete characterization of the proposed receiver prototype. The outcomes are tabulated and discussed, while comparison with other reported works are reviewed at the end of the chapter.

Finally, in Chapter 5, a summary of the accomplishments of this dissertation project is defined and the dissertation is concluded with potential future works.

## CHAPTER 2: LITERATURE REVIEW

The conventional blocks of a wireless receiver front end are the low noise amplifier (LNA), mixer and the voltage controlled oscillator (VCO). Section 2.1 gives a brief explanation on the fundamental parameters of a RF receiver. In section 2.2, an overview of the three primary traditional receiver architectures, specifically, heterodyne, homodyne and low-IF is reviewed, along with some benefits and drawbacks, characteristics and conclusions. The following segment elaborates into the primary building blocks of the receiver in particular, the LNA, mixer and VCO. Section 2.4 provides the radio spectrum and standards. Section 2.5 offers the target specifications while the subsequent section introduces quadrature generation techniques. The body bias approach which helps to minimize supply voltage headroom is explained in section 2.7. The final segment offers an overview of the state of the art designs.

Despite many decades of works and researches on RFIC and microwave theory, the design and implementation of RF circuits and transceivers continue to be challenging. As illustrated in Figure 2.1, RF design draws upon a multitude of disciplines, hence it deals with numerous trade-offs. Based on target applications, the tradeoffs that we can afford will vary. Therefore, new design strategies are needed to minimize these tradeoffs.



**Figure 2.1: The disciplines associated with RFIC design**

## 2.1 RF Fundamentals

### 2.1.1 Impedance Matching

The transmission line is one of the essential focus of a complex structure of an RF circuit. The signal that goes through the transmission line has to ensure that the impedance of output block is identical to the characteristic impedance of the subsequent block. Any mismatch of the impedances causes a reflected voltage and current which reduces the transmitted energy between blocks, consequently reducing power transfer (Boglione et al., 1996). The characteristic impedance of the transmission line is expressed by means of the Ohm's law as:

$$Z_0 = \frac{V_i}{I_i} = \frac{V_r}{I_r} = \frac{R + j\omega L}{\gamma} \quad (2.1)$$

where,  $\omega$  is the operating frequency,  $L$  is the inductance along the transmission line and  $\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}$ . The expression  $\gamma$ , represents the propagation constant with the resistance  $R$ , which represents the conductor loss and the conductance  $G$ , which is the dielectric loss between the two conductors. The load impedance at the end of the transmission line is:

$$Z_L = \frac{V_o}{I_o} = \frac{V_i + V_r}{V_i - V_r} Z_0 \quad (2.2)$$

The reflection coefficient is the ratio between the normalized reflection and the incident waves of the load impedance,  $Z_L$  at the end of the transmission line expressed as;

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (2.3)$$

The reflection coefficient is inexistent ( $R_L = 0$ ) when the characteristic impedance,  $Z_0$  is

equal to the load impedance ( $Z_L = Z_0$ ) which maximizes the energy transferred between the blocks. Generally, the antenna is an external device and will have an impedance of  $50 \Omega$ . Hence, in a RF receiver system, the first block which is typically an LNA, need to coincide with a standard impedance of  $50 \Omega$  (Hu, 2004).

### 2.1.2 Scattering Parameters

The traditional system characterization is carried out through two approaches. At low frequencies, the system uses measurements of open and short-circuits to determine the admittance and hybrid parameters. While at high frequencies, the methods used by the system at low frequencies are not feasible due to the port voltages or currents measurements that consist of magnitude and phase of the travelling waves. Consequently, the S-parameters, also referred to as scattering parameters, are used to characterize the inputs and outputs variables of systems operating at high frequencies, in order to auxiliary the adaptation of impedance matching, to offer the maximum value gain, the input and the output impedance and even possible instabilities (Suto & Matsui, 2016). The scattering parameters relate the electromagnetic waves at the input and output,  $a_1$ ,  $b_1$ ,  $b_2$  and  $a_2$  as shown in the Figure 2.2, when the system is viewed as a diport. These waves are generated by the input and output ports from the diport who represents the system.



**Figure 2.2: S-parameters of a diport system**

The S-parameters relate the electromagnetic waves as follows:

$$S_{11} = \frac{b_1}{a_1} (a_2 = 0) \quad (2.4)$$

$$S_{12} = \frac{b_1}{a_2} (a_1 = 0) \quad (2.5)$$

$$S_{21} = \frac{b_2}{a_1} (a_2 = 0) \quad (2.6)$$

$$S_{22} = \frac{b_2}{a_2} (a_1 = 0) \quad (2.7)$$

Therefore, the S-parameters have the following designation: the  $S_{11}$  is the input reflection coefficient, whilst  $S_{21}$  is the transmission gain since it relates the output wave ( $b_2$ ) to an input wave ( $a_1$ ). The  $S_{12}$  corresponds to the reverse transmission gain considering the input and output diport swapped, which means the electromagnetic wave that enters on the diport is  $a_2$  and not  $a_1$ . Finally, the last S-parameter is  $S_{22}$ , the output reflection coefficient. The calculations of the S-parameters are made pertaining the terms of incident and reflected voltages of electromagnetic waves  $a_1$ ,  $a_2$ ,  $b_1$  and  $b_2$ , permitting the development of design circuit without internal detailed understanding. From this S-parameter, we are able to get the input matching, output matching, stability and conversion gain of a block (Razavi, 2012).

### 2.1.3 Noise

Noise is one of the most vital parameter in analog design, more precisely in RF circuits. This parameter is liable for the degradation of circuit performance and its appearance is as a result of external interference or by the intrinsic nature of the circuit materials. Apart from the external random noise such as atmospheric noise from free space environment



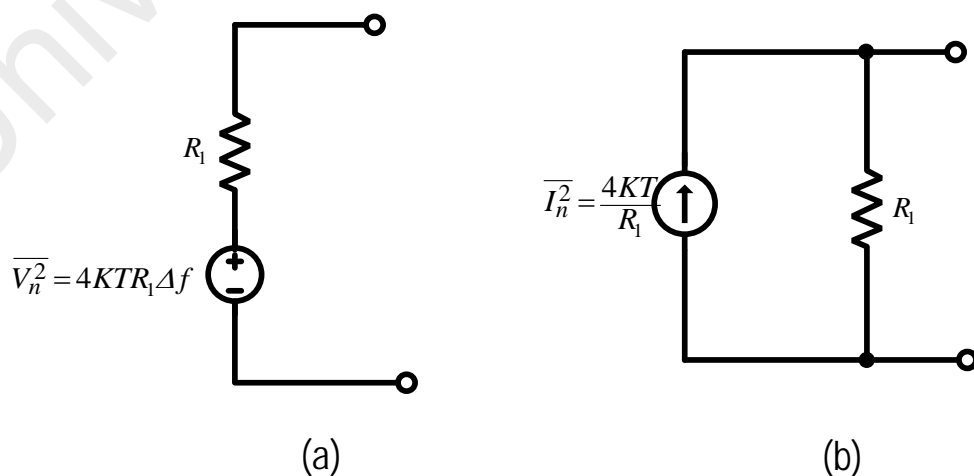
acquired at the receiver, additional noise from component devices further degrades the quality of the processed signal (Jordan & Jordan, 1965). Due to its random behaviour and difficult prediction, noise implies undesirable signals added to the desired signal. The common sources of noise present in CMOS technologies are thermal noise and flicker noise (Manku, 1999).

### 2.1.3.1 Thermal Noise

The thermal noise relies upon the temperature that causes variation in the resulting current which is generated by the random motion of electrons that pass through an ohmic resistance device. As the temperature of the device increases, the random motion of the molecules increase, and so does the corresponding noise level. Therefore, it is referred to as thermal noise (Tedja et al., 1994). The average noise power remains almost independent of frequency and can be adequately approximated as:

$$\overline{V_n^2} = 4KTR\Delta f \quad (2.8)$$

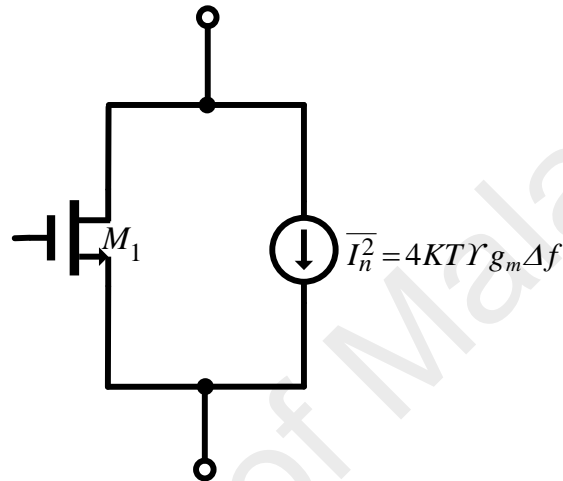
in which T is the absolute temperature (in Kelvin), R is the resistance of the conductor material, K is the Boltzmann constant and the bandwidth of the system is  $\Delta f$ . This can



**Figure 2.3: Representation of thermal noise source of a resistance: (a) via a voltage source, (b) via a current source**

be quantified by a series voltage source using the Thevenin equivalent, or by a parallel current source using the Norton equivalent as shown in Figure 2.3.

The thermal noise additionally appears in MOSFET (MOS) transistors due to the carrier motion through the channel and is represented as shown in Figure 2.4 by a parallel current source to the conduction channel (Jindal, 2006).



**Figure 2.4: Representation of thermal noise of mosfet via a current source**

The noise current of the MOSFET is given by:

$$\overline{I_n^2} = 4KT\gamma g_m \Delta f \quad (2.9)$$

Here  $\gamma$  is the Noise Excess Factor (NEF) and is roughly equal to  $2/3$  for long channel devices, where else  $g_m$  is the transconductance of the transistor.

### 2.1.3.2 Flicker Noise

The flicker noise or  $1/f$  noise is a low-frequency noise resulted by the surface and gate effects within the semi-conductor material, more specifically by the interface between the gate oxide ( $S_iO_2$ ) and the silicon substrate ( $S_i$ ). The measured noise power in MOS

devices has a dependence on the gate bias and the oxide thickness (Wei et al., 2000). The flicker noise equation that is presented in 2.10, has parameters like the process dependent constant  $k_f$ , the gate oxide capacitance per unit area ( $C_{OX}$ ), the width (W) and length (L) of the transistor.

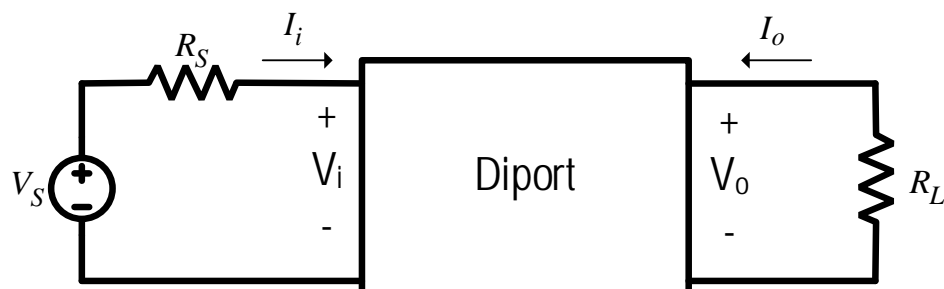
$$\overline{V_n f^2} = \frac{k_f}{C_{OX} W L f^{\alpha f}} \quad (2.10)$$

This kind of noise becomes more critical in low frequencies and is the bottleneck in providing sufficient dynamic range and better circuit performance (Izpurá, 2009).

One of the most essential parameter in a RF circuit is the noise factor (F), which represents the ratio of the total output noise and the input noise of a system (Lee, 2004). When a system is modelled as a diport, as represented in Figure 2.5, the measurements are relative to the entire noise power between the output, input and its gain for each frequency. The noise factor can be expressed by:

$$F = \frac{N_o}{A^2 N_i} \quad (2.11)$$

where A is the gain of the system,  $N_o$  is the output noise power and  $N_i$  is the input noise power of the system. The noise factor can also be expressed as the power ratio between the desired signal to the total noise (unwanted signal), which is achieved through the ratio



**Figure 2.5: Input and output noise power of a diport system**

of signal-to-noise ratio (SNR) at the input and at the output. This expression demonstrates how much the SNR degrades as the signal passes through the system as shown below,

$$F = \frac{SNR_{in}}{SNR_{out}} \quad (2.12)$$

The noise figure (NF), a general parameter used in the electronic world, is the noise factor when calculated in decibels (dB). Therefore, the NF of a system is given as,

$$NF = 10 \log \left( \frac{SNR_{in}}{SNR_{out}} \right) \quad (2.13)$$

#### 2.1.4 Gain

Gain is defined as the ratio of the output signal to the input wherein it could be expressed in terms of voltage or power (Behzad Razavi, 2016). The voltage gain is described as the ratio of the root mean square (RMS) voltage of output signal to the RMS voltage of the input signal. Power gain is defined as the ratio of power delivered to the load and the power available from the source. Both voltage and power conversion gain are typically given in dB as,

$$voltage_{gain}(dB) = 20 \log \frac{V_{out}}{V_{in}} \quad (2.14)$$

$$Power_{gain}(dB) = 10 \log \frac{V_{out}}{V_{in}} \quad (2.15)$$

If the input source resistance ( $R_S$ ) and the output load resistance ( $R_L$ ) are matched, ( $R_S = R_L$ ), then voltage gain is equal to power gain as stated by,

$$\begin{aligned} \text{Gain(dB)} &= 10 \log \frac{P_{\text{out}}}{P_{\text{in}}} = 10 \log \left( \frac{\frac{V_{\text{out}}^2}{R_L}}{V_{\text{in}}^2/R_S} \right) \\ &= 10 \log \left( \frac{V_{\text{out}}^2}{V_{\text{in}}^2} \right) + 10 \log \left( \frac{R_S}{R_L} \right) = 20 \log \frac{V_{\text{out}}}{V_{\text{in}}} \end{aligned} \quad (2.16)$$

### 2.1.5 Linearity

The measurement of the RF system linearity is virtually crucial to understand the effect of nonlinear devices have towards the output signal. The linearity can be characterized with the aid of the 1 dB compression point and by the third-order intermodulation product (Sanghoon et al., 2003). The RF circuits are constituted by devices exhibiting nonlinear characteristics, such as MOS transistors, which in addition to this feature they are also memoryless, time invariant and their output response when exhibited by an input signal can be represented by the Taylor series:

$$y(t) = a_0 + a_1x(t) + a_2x^2(t) + \dots + a_nx^n(t) \quad (2.17)$$

Nonlinear devices produce the same harmonic as the order of their nonlinearities with multiples of the fundamental frequency. The order coefficients, have different effects on the nonlinear devices, where when odd, the order coefficients have impact on the amplitude of the fundamental frequency, while for even order coefficients, the impact is on the DC component (Razavi, 2012). If two sinusoidal signals are applied at the nonlinear device input with different fundamental frequencies as described below,

$$x(t) = A \cos(\omega_1 t) + B \cos(\omega_2 t) \quad (2.18)$$

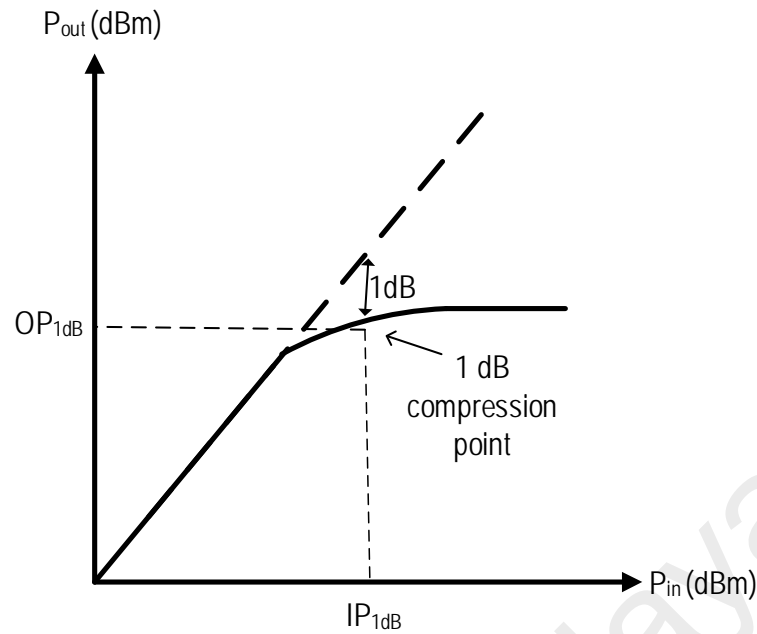
The intermodulation products that are generated at the output signal is given by:

$$\begin{aligned}
y(t) = & a_0 + a_1[A \cos(\omega_1 t) + B \cos(\omega_2 t)] + \\
& a_2 \left[ \frac{A^2}{2} (1 + \cos(2\omega_1 t)) + \frac{B^2}{2} (1 + \cos(2\omega_2 t)) + \right. \\
& \left. AB(\cos(\omega_1 + \omega_2)t) + \cos((\omega_1 - \omega_2)t) \right] + \\
& a_3 \left[ \left( \left( \frac{3}{4}A^3 + \frac{3}{2}AB^2 \right) \cos(\omega_1 t) \right) + \left( \left( \frac{3}{4}B^3 + \frac{3}{2}BA^2 \right) \cos(\omega_2 t) \right) + \right. \\
& \left. \frac{3}{4}A^2B(\cos(2\omega_1 + \omega_2)t) + \cos(2\omega_1 - \omega_2)t + \frac{3}{4}B^2A(\cos(2\omega_2 + \omega_1)t) + \right. \\
& \left. \cos(2\omega_2 - \omega_1)t + \left( \frac{3}{4}A^3(\cos(3\omega_1)t) + \frac{3}{4}B^3(\cos(3\omega_2)t) \right) \right] \quad (2.19)
\end{aligned}$$

which illustrates the operations between the input signal frequencies and their multiples of the fundamental frequency. The nonlinearity of order three (IM3) becomes very susceptible in the mixer (Esmael et al., 2016). The mixer down converts a high frequency signal to a lower frequency commonly called an IF. If  $\omega_1$  and  $\omega_2$  are close enough, then the intermodulation component will be closed to the desired IF outputs. More on this phenomena will be explained later in the mixer part. This is an example that the intermodulation product appearing in the frequency band of interest and can't be removed by a filter easily (Razavi, 2012).

#### 2.1.5.1 1dB Compression Point

The 1 dB compression point (P1dB) is a linearity measure of the dynamic range (linear proportional operation range) of a circuit and is additionally also known as gain compression or saturation. Their effect takes into consideration the gain of the circuit, the relation between the output and input power, by checking its linearity measure. The conversion gain is typically equal for small input signals. However a strong RF signal can cause the gain to saturate (Lu & ZhiHua, 2006). Through Figure 2.6, it is visible that the ideal linear characteristic is identical with the real characteristic of the circuit over a limited range. As the input signal power increases, its real characteristic begins to

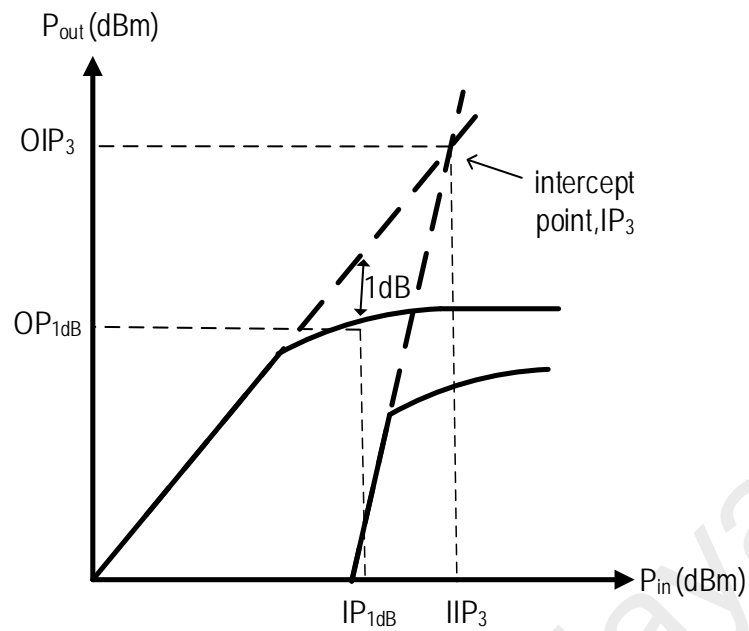


**Figure 2.6: Illustration of 1dB compression point**

saturate, resulting in reduced gain. To check the circuit's linearity measure, the compression point 1dB is defined through the difference of 1dB from the ideal linear characteristic. The higher the 1dB compression point is, the larger RF input signal the system is capable to handle before the nonlinear products degrade the output power (Kachare et al., 2005).

### 2.1.5.2 Third-Order Intercept Point

The third-order intercept point, denoted as IP<sub>3</sub>, is the intersection point where the hypothetical extrapolated idealized responses of output power of the first-order and the intermodulation product of third-order intersect, typically at a point above the onset of compression. This third-order intersection point can be designated as either an input power level (IIP<sub>3</sub>) or an output power level (OIP<sub>3</sub>). This effect can be seen in Figure 2.7, where the amplitude of the fundamental frequency would be equal to the amplitude of the intermodulation product of third-order. The point of third-order intercept (IP<sub>3</sub>) occurs at



**Figure 2.7: Graphical representation of IIP3 and OIP3**

a higher power level than the 1 dB compression point, being applied a practical rule that IP3 is 10-15 dB greater than the 1 dB compression point (Woo Young et al., 2004 ). This parameter shows how, specifically the third order intermodulation effects the circuit. It degrades circuit performance.

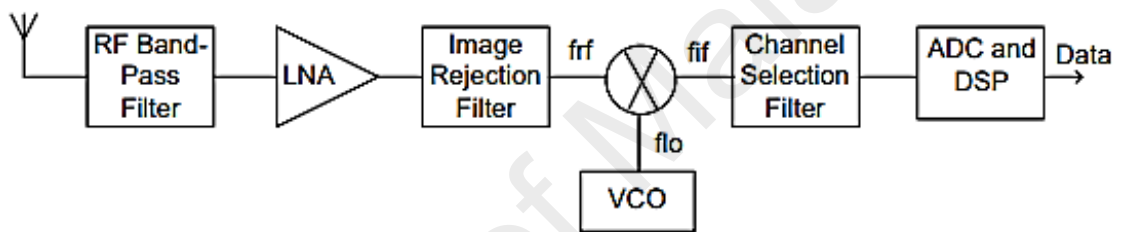
## 2.2 Receiver Architectures

A receiver receives attenuated RF signal from an antenna. The weak RF signal has to be amplified by the receiver, while at the same time also liable for filtering eventual interferences. After amplification, the receiver converts the input RF signal to baseband, in order to demodulate and access the original information (Haesik, 2015a). There are three predominant conventional receiver architectures, namely, heterodyne, homodyne and low-IF.



### 2.2.1 Heterodyne Receiver

The heterodyne receiver is broadly used in the wireless world as shown in Figure 2.8. The RF signal from the transmitter is received by the antenna and filtered through a band-pass filter, which removes the unwanted frequencies. The weak acquired signal is then amplified by a LNA. After that, the signal goes through an image rejection filter to attenuate image band frequencies resulting from the LNA. The down-converted process shifts the signal frequency to an intermediate frequency (IF), which is done via a signal multiplier (Mixer) that is driven by the output signal of a Local Oscillator (LO). A



**Figure 2.8: Block diagram of a heterodyne receiver architecture**

baseband filter called channel selection filter is used at the output of the mixer that isolates the desired signal from the other adjacent IF signals from nearby channels. Finally the Analog to Digital Converter (ADC) is accountable to convert the analog signal to digital and demodulate the information. The heterodyne receiver typically inherits superior performance in overall. It additionally gives the possibility of dual IF conversion, hence more freedom in frequency planning. This approach avoids the appearance of spurious signals (Baki & El-Gamal, 2004). One downside of this architecture is in the extensive filtering required due to the image frequency (Razavi, 2001). Implementation of this filters on chip in the silicon technologies are very difficult as on-chip components have considerable component variations especially the inductors, generally have very low

quality factor (Q) values, rarely exceeding 20. This bottlenecks the filtering properties of the RF filters, and therefore the image reject filter will have poor performance. Commonly, an external image reject filter will be connected. The IF filter is likewise an issue since the inductors required to construct a passive filter at low frequency could be very huge which will increase chip area. The RF bandpass filter is also often implemented off-chip using a SAW filter to lessen the image filtering requirements. These external components are the primary bottleneck in SoC design (Mirzaei et al., 2011). Filter bandwidths are commonly proportional to the center frequency, thus sharper cut-off filters are less complicated to be designed at lower frequencies.

### **2.2.2 Homodyne Receiver**

The direct conversion architecture is an attractive solution for low cost and low power solution. The concept is fundamentally similar to the heterodyne receiver, with the primary distinction that the IF frequency is zero hence, the signal is directly down converted to baseband. This architecture is also referred as a zero IF receiver as shown in Figure 2.9. This structure may be appealing for a couple of reasons. Firstly, the image frequency does not pose any hassle, since it coincides with the frequency of the desired signal, thus casting off the bulky image rejection filters (Zhan et al., 2007). This also means that twice as much of the wanted signal power enters the mixer enhancing the SNR by 3dB. Secondly the output signal is now baseband, as a result, the circuits after the mixer will be operating at the lowest possible frequency which permits them to be implemented in a power efficient way (Kim & Silva-Martinez, 2013). Finally it only needs a low pass channel selection IF filter that is much easier to implement on-chip. The direct conversion receiver does require some additional circuitry to function properly. Since both the upper and lower sidebands of the RF signal are converted to the identical output frequencies, extra measures are needed to maintain the information apart. This is

achieved with a quadrature mixer, which is essentially two separate mixers operated with LO signals  $90^\circ$  aside (Andriesei, 2013). The direct converter architecture has some drawbacks which prevent it from being used extensively, such as high flicker noise at low frequencies, LO leakage, DC offsets, intermodulation and quadrature mismatch.

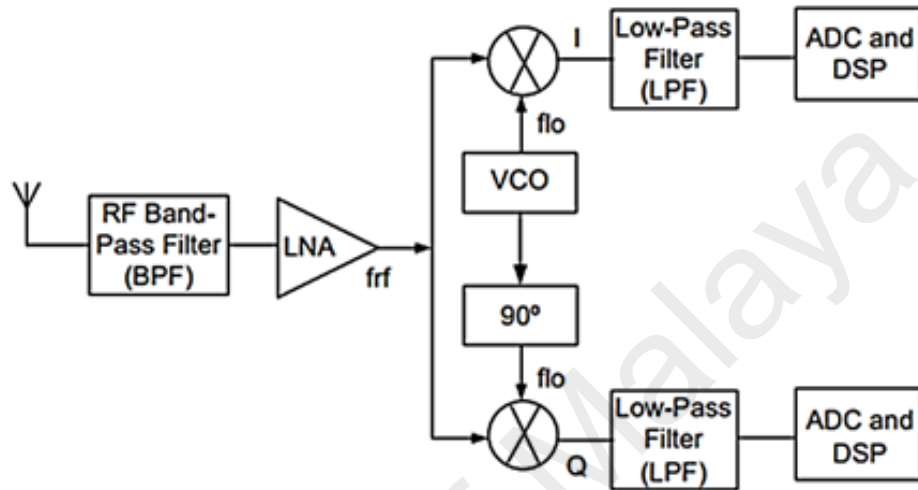


Figure 2.9: Block diagram of a homodyne receiver architecture

### 2.2.3 Low IF Receiver

The previous two architectures were useful, but the combination of both advantages gave

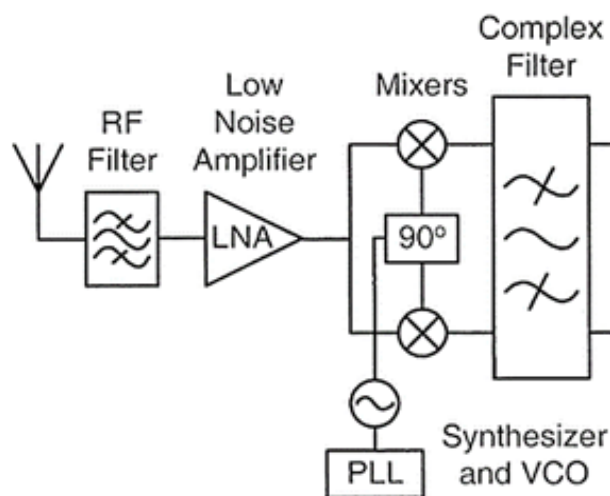


Figure 2.10: Block diagram of a low-IF receiver architecture

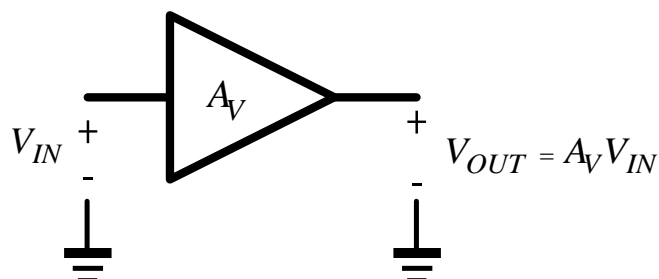
the Low-IF receiver as illustrated in Figure 2.10. This type of receiver cancels the image frequency via the use of quadrature mixing technique with quadrature architectures consequently getting rid of the image problem associated with the heterodyne receiver (Bao-lin et al., 2009). It additionally allows selection of a low intermediate frequency, which enables it to avoid the issues that arise in the homodyne receiver such as flicker noise, LO leakage and DC offsets that affects baseband signals (Li et al., 2005 ). This structure integrates IQ mixers for quadrature mixing, hence eliminating the need of image filters to suppress image frequencies. Either the RF signal or the LO signal needs to be in quadrature phase to suppress the image (Tedeschi et al., 2010). Finally, this receiver calls for a complex filter for channel selection to complete the architecture, which is simple to build at low IF frequency. This architecture is broadly utilized for narrowband applications such as ZigBee and BLE compliant receivers.

### 2.3 Basic Building Blocks of a Receiver

The conventional blocks of a wireless receiver front end are the LNA, mixer and the VCO.

#### 2.3.1 Low Noise Amplifier

An amplifier is a device that amplifies an input signal. This block is used extensively in the analog and RF domain. Below is a block diagram of a typical amplifier.



**Figure 2.11: Block diagram of an amplifier**

Hence, amplification factor is the gain of the amplifier, usually denoted as  $A_V$ ,

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (2.20)$$

The Low Noise Amplifier (LNA), is an essential building block for receivers of wireless circuit. The signals received at the receiving antennas are usually very weak and should be amplified in order that they can be handled by the subsequent processing stages (Wu et al., 2012). This amplification, however, needs to be done with care to lessen noise, and amplify the desired signal to a moderate output. In this manner, the signal proceeding to the rest of the circuit will be in the best viable conditions and can be processed easily to get the correct information. Therefore, according to the Friis' formula, which indicates the relation between the signal-to-noise ratios (SNR) of multiple cascaded systems, the noise factor (F) of these circuits can be represented in cascade stages as,

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_m - 1}{G_1 G_2 \dots G_m - 1} \quad (2.21)$$

wherein  $F_m$  and  $G_m$  are the noise factor and the available power gain of the subsequent stage, respectively. From the above equation, it can be observed that the noise factor of the first stage (LNA) is dominant, becoming essential to increase the gain to reduce the noise contribution of the subsequent stages. To maximize the gain, power transmission ought to be maximized. This occurs when there is no reflected wave either in the input or output of the LNA, which means ideal impedance matching. In turn, the absence of reflection ensures the adaptation of the source impedance with the load impedance, which ensures optimal noise impedance (Trung-Kien et al., 2004 ).

Another parameter that is represented by the cascade stages is the linearity that can be characterized via the following equation as shown below:

$$\frac{1}{IIP_3} = \frac{1}{IIP_3} + \frac{G_1}{IIP_{3,2}} + \frac{G_1 G_2}{IIP_{3,3}} \quad (2.22)$$

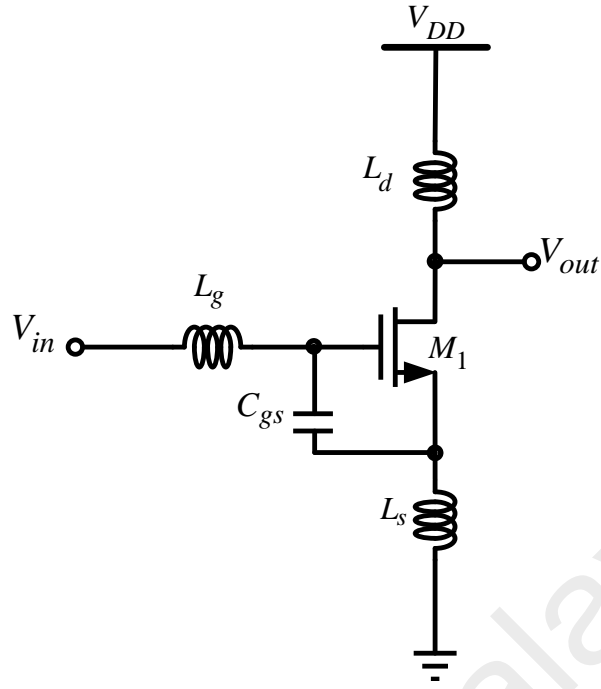
where IIP3 is the input referred of the third-order intercept point, expressed in power, and G is the power gain. From the evaluation of the above expression, the gain of the preceding stages influences directly the IIP3 of the last stage, but a low noise figure demands a high gain for the first stage. This results in a tradeoff between noise and linearity which limits the dynamic range and the overall performance of a receiver (Azizan et al., 2014). The 1 dB compression point is a linearity measure of the circuit and is also known as gain compression or saturation. This 1dB point indicates at what input signal level, the LNA begins to behave nonlinear. If the first stage gain is very high, then the subsequent stages linearity will degrade, consequently effecting the whole system linearity performance. Hence the most crucial parameter for a LNA is the input matching, noise and gain. The two most widely used LNA topology are the common source LNA with source degeneration and the common gate LNA. Below is a brief description regarding the working concepts of this these LNAs.

### 2.3.1.1 Common Source LNA with Source Degeneration

The inductively degenerated Common Source (CS) LNA, is illustrated in Figure 2.12. It is the most popular LNA topology for narrowband applications, as it is capable of achieving good noise performance, easy input matching and moderate gain with linearity (Shaeffer & Lee, 1997). The input impedance is given by (2.23), assuming ideal inductors.

$$Z_{in} = L_s \frac{g_m}{C_{gs}} + \frac{1}{j\omega C_{gs}} + j\omega(L_s + L_g) \quad (2.23)$$

Here,  $g_m$  is the transconductance of transistor  $M_1$ . Inductor  $L_s$  and the gate-source capacitance,  $C_{gs}$  of transistor  $M_1$ , form a feedback path from the transistor drain current to the input current, which results in a resistive part of the input impedance equal to:



**Figure 2.12: CS LNA with source degeneration topology**

$$L_s \frac{g_m}{C_{gs}} = L_s \omega_T \quad (2.24)$$

$L_s$  is chosen to provide a desired input resistance, typically  $50 \Omega$ .  $L_g$  is chosen such that it resonates with the gate source capacitance,  $C_{gs}$  of the transistor and  $L_s$ , making the input impedance completely resistive at the operating frequency. Hence the noise performance is optimum, because resistors are eliminated for matching purpose and inductors are ideally noiseless. The gain of this topology with parasitic capacitances neglected for simplicity is given as:

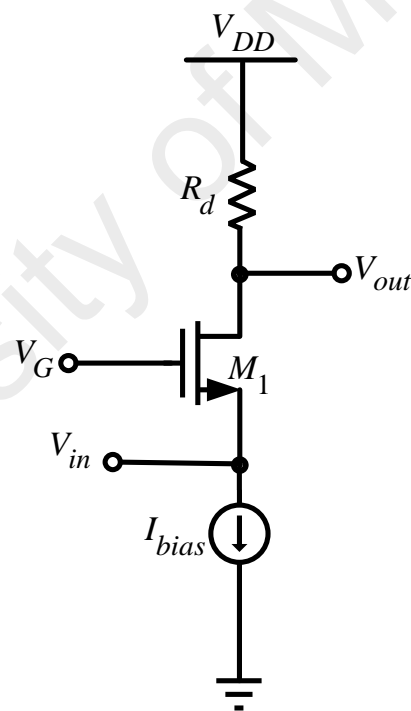
$$A_V = - \frac{L_d}{\frac{1}{g_m} + L_s} \quad (2.25)$$

It can be observed that the output is inverted  $180^\circ$  from the input. The  $L_d$  is selected such that it resonates with the parasitic capacitances at the output terminal of the mosfet

at the preferred operating frequency. Therefore at the desired frequency, the parallel resonant tank at the output will exhibit a very high impedance, hence boosting the gain. Another transistor could be stacked on top of the amplifying transistor which offers further benefits such as increased stability and output resistance. This topology is referred as the cascode common source LNA with source degeneration (Balan et al., 2017). The downside of this topology, is the greater voltage headroom required to accommodate the cascode transistor and more parasitic capacitances.

### 2.3.1.2 Common Gate LNA

The common gate LNA as illustrated in Figure 2.13 provides a resistive input while being



**Figure 2.13: CG LNA topology**

both simple and inductorless (Jeong et al., 2011). If the device, and hence the gate source capacitance  $C_{gs}$ , is small, the input impedance,  $Z_{in}$  is equal to,

$$Z_{in} = \frac{1}{(g_m + g_{mb})} \quad (2.26)$$



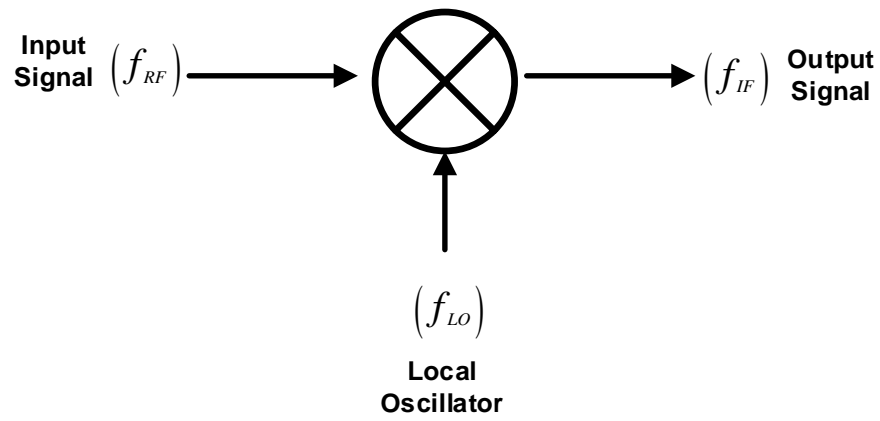
where  $g_m$  is the transconductance of the MOS  $M_1$  and  $g_{mb}$  is the body effect transconductance, neglecting source terminal capacitance and drain-source conductance. It can be observed that the input impedance may be predominantly resistive over a very wide frequency range, making this topology specifically well suited for ultra-wideband (UWB) applications (Wang et al., 2009). The input impedance is almost entirely dependent on the transconductance  $g_m$ , consequently making it susceptible to process, voltage and temperature (PVT) variations. By using a resistive load, the gain additionally could provide a wideband response. The gain of this LNA is given by neglecting parasitic capacitances for simplicity as,

$$A_V = (g_m + g_{mb})R_d \quad (2.27)$$

### 2.3.2 Mixer

The mixer acts to transform a signal from one frequency band to some other frequency band. In a receiver front-end, it converts the RF signal to a much lower frequency in which it may be more easily amplified and processed (Haesik, 2015b). The mixing is essentially a time domain multiplication of the signal with a tone of some different frequency. Figure 2.14 illustrates a block diagram of a mixer. The mixer has two input ports and one output port. Ideally, a mixer yields a sum and difference frequency at the single output port when two different input frequencies of signal are applied into the two other input ports. Due to this, the mixer is generally used in the transmitter to upconvert a baseband signal to a higher RF signal, where else in a receiver, the mixer is used to downconvert a high frequency signal to baseband (Jouri et al., 2010 ). Specifically in the case of down conversion, when  $f_{RF}$  and  $f_{LO}$  are the two input signal frequencies, the output  $f_{IF}$  signal can be expressed as:

$$f_{IF} = f_{RF} - f_{LO} \quad (\text{low side injection}) \quad (2.28)$$



**Figure 2.14: Symbol view of a mixer with the signal flow**

$$f_{IF} = f_{LO} - f_{RF} \quad (\text{high side injection}) \quad (2.29)$$

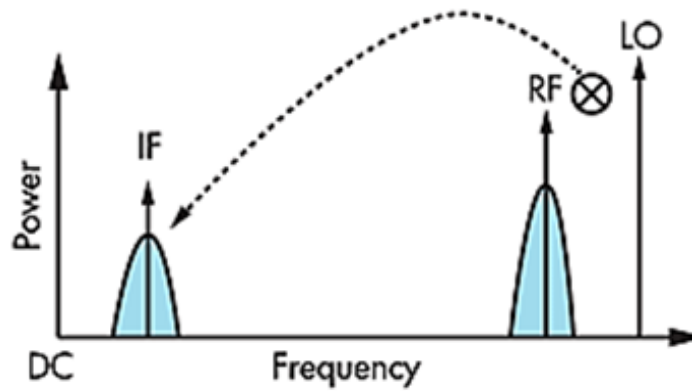
The mixing for downconversion via high side injection operation in the frequency domain is illustrated in the Figure 2.15, where the LO signal is located at a higher frequency than the RF signal. Meanwhile for low side injection, the RF signal will be located at a higher frequency than the LO signal. Generally, low side injection is commonly preferred so that the IF spectrum does not get mirrored (Mollaalipour & Miar-Naimi, 2013). The detailed frequency translation operation for down conversion mixer is described in the following mathematical expressions. When an input RF signal  $V_{RF}(t) = (V_{RF} \cos \omega_{RF}t)$  and LO input signal  $V_{LO}(t) = (V_{LO} \cos \omega_{LO}t)$  are multiplied, the outcome becomes,

$$V_{IF}(t) = V_{RF}(t) \cdot V_{LO}(t) = (V_{RF} \cos \omega_{RF}t)(V_{LO} \cos \omega_{LO}t) \quad (2.30)$$

By solving equation (2.30) using trigonometry, it can be expressed as,

$$V_{IF}(t) = \frac{V_{RF} \cdot V_{LO}}{2} \left[ \underbrace{\cos(\omega_{RF} - \omega_{LO})t}_{\text{LSB}} + \underbrace{\cos(\omega_{RF} + \omega_{LO})t}_{\text{USB}} \right] \quad (2.31)$$

Here it could be observed, that the output incorporates two component. For



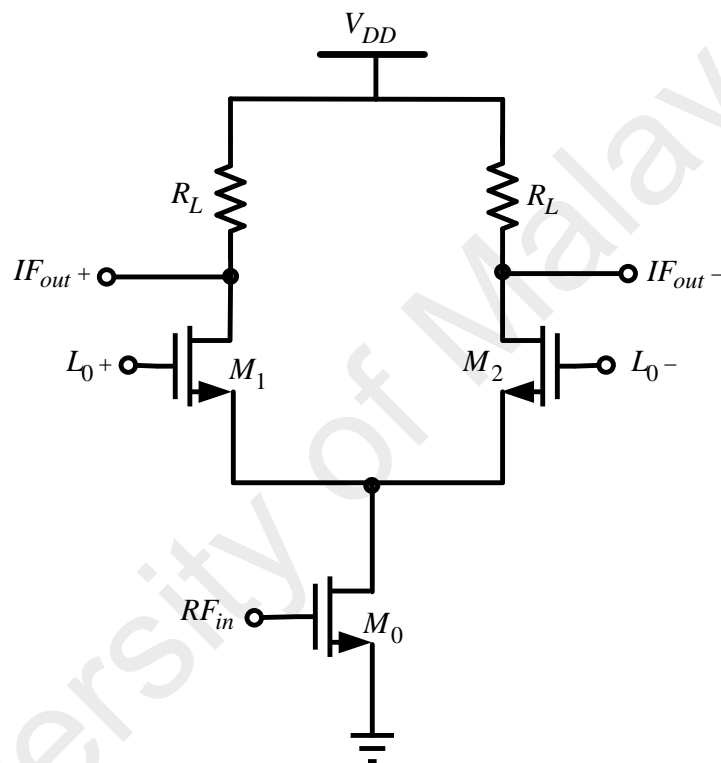
**Figure 2.15: Graphical representation of high side injection for mixing**

down conversion mixing operation, the desired component,  $(\omega_{RF} - \omega_{LO})$  is kept, while the undesired frequency component,  $(\omega_{RF} + \omega_{LO})$  may be filtered out. Even though this operation can be accomplished with pretty much any non-linear device, because of its high performance, the most prominent approach is to adopt transistors as switches, swiftly switching the polarity of the signal as it passes from input to output.

A mixer may be implemented with just a single device, but this approach suffers from a lack of isolation between the RF and LO signals (Lee, 2004). The single balanced mixer provides this isolation, and with a differential output, it is much better suited in conveying IF signals close to DC. Placing two single balanced mixers side by side, operating with opposite phase of RF and LO signals and combining the outputs, a double balanced mixer is obtained, where all ports are differential. The primary advantage of this mixers is RF to IF leakage is attenuated. The penalty are the extra power needed for two identical mixers. In low power design, a single ended RF port is commonly favoured because it generally requires less power for the same noise performance, and extra circuit complexity is avoided, especially since most antennas do not offer balanced signals (Yadav & Chaturvedi, 2014). Mixers have different varieties of possible implementations which are the active and passive mixers.

### 2.3.2.1 Active Mixer

Active mixers provide gain to the IF signal, as the signal is routed to the subsequent blocks in the receiver (Tan et al., 2014). They are typically based in differential pair and may be single balanced or double-balanced, relying on whether the RF signal coming from the LNA is balanced or unbalanced. The single-balanced active mixer, represented in Figure 2.16, has a differential output, with the inputs driven by the LO signals, applied



**Figure 2.16: Single balanced active mixer topology**

on each gates of the switching transistors  $M_1$ ,  $M_2$ , and a current source,  $M_0$  controlled by the RF unbalanced signal. The RF input voltage is converted to current by transistor  $M_0$ . This current is drawn alternately via the two sides of the differential pair consisting of  $M_1$  and  $M_2$  and they preferably switched between saturation region and off states depending on the polarity of the LO voltage. For this mixer, the output spectrum includes the LO frequency. The conversion gain of this mixer assuming LO signal is square wave is given as;

$$A_V = -\frac{2}{\pi} g_{m0} R_L \quad (2.32)$$

in which  $g_{m0}$  is the transconductance of transistor  $M_0$  and  $R_L$  is the load resistance. It is a simple active mixer that has moderate gain and noise figure, high input impedance, moderate 1 dB compression point, IIP3 and port-to-port isolation (Yoon et al., 2008).

### 2.3.2.2 Passive Mixer

The simplest single balanced passive mixer configuration is CMOS transistors implemented as switch, shown in Figure 2.17, whose gate is driven by the LO signal, with the RF signal being applied at its source and the IF signal being sensed at its drain. This passive mixer has no DC consumption, no gain and presents high linearity and bandwidth. The implemented switch operates between the driving and cut-off region, since the LO power is applied on the gate of the transistors at the oscillation frequency, presenting a channel resistance varying with time (Molnar & Andrews, 2012). The downside of this mixers although with excellent linearity performance, they require very strong LO signals for proper switching and they outlays conversion loss. The primary advantage of passive

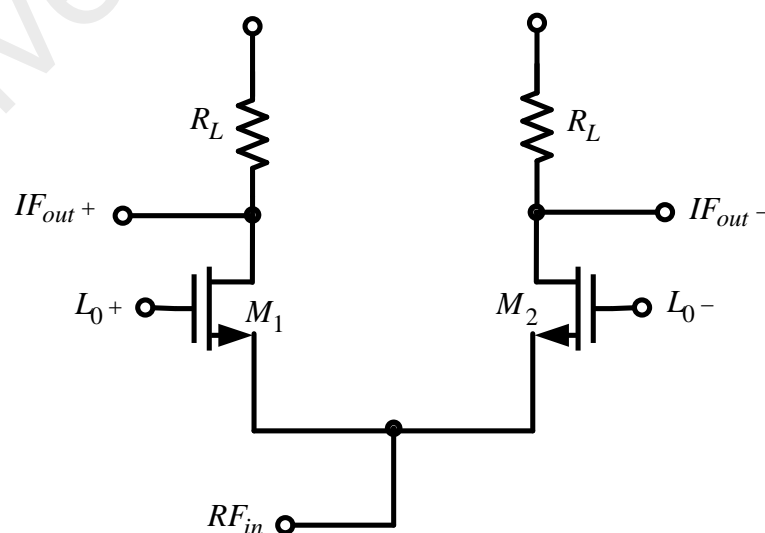


Figure 2.17: Passive mixer topology

mixers is the lack of  $1/f$  noise, making it specifically suited for direct conversion receivers (Liu & Rabaey, 2011).

### 2.3.3 Oscillator

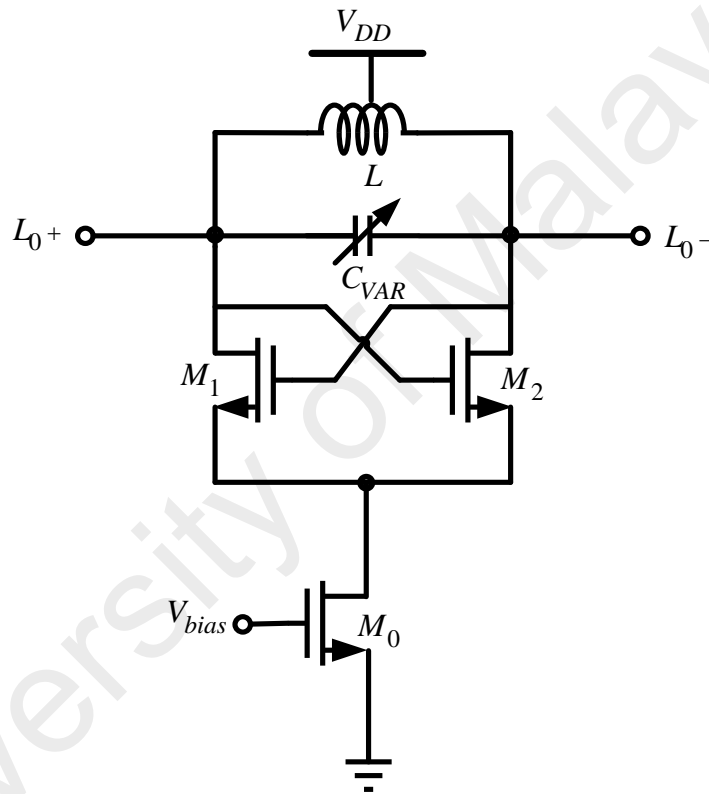
An oscillator is a circuit that produces a periodic signal at a certain frequency. The frequency of the oscillator determines the intermediate frequency of the receiver. RF oscillators are commonly tunable with an input voltage, such as the voltage controlled oscillator (VCO). Oscillators may be close to linear or nonlinear. A linear (harmonic) produces a largely sinusoidal output, and is tuned to a well-defined frequency by a reactive load or feedback network. Linear oscillators include negative resistance, Colpitts, Clapp, Hartly, Wien Bridge and Pierce oscillators (Razavi, 2012). A nonlinear (relaxation) oscillator can also produce other waveforms which include triangle or square waves. A typical relaxation oscillator is the ring oscillator, which consists of an odd number of inverting gain stages linked in a ring shape. Relaxation oscillators generally have inferior phase noise performance due to the fact they have poor (low Q) filtering and they cannot store as much energy from one oscillation period to the following as an LC oscillator can. Consequently, this type of oscillators are not preferred in high frequency wireless applications (Lee, 2004).

The most common high frequency oscillator which are implemented on chip is the differential LC negative resistance oscillator, as depicted in Figure 2.18. The negative resistance is provided by two cross-coupled transistors. The differential pair will replenish energy to the LC tank that is lost in each period, counteracting the damping (Yang et al., 2011). For the oscillation to start up, the Barkhausen criterion needs to be satisfied. Eventually, as the oscillation grows, the differential pair will saturate, reducing the effective  $g_m$ , and the oscillation will stay at a constant amplitude, given by:

$$|\hat{V}| = i \cdot R' = \frac{4}{\pi} I_{bias} \omega_0 Q L \quad (2.33)$$

where,  $Q$  is the quality factor of the inductor  $L$ ,  $I_{bias}$  is the bias current set by the tail transistor and  $\omega_0$  is the center frequency of the LC tank and can be set by :

$$\omega_0 = \frac{1}{2\pi\sqrt{LC_{VAR}}} \quad (2.34)$$



**Figure 2.18: NMOS based, -gm LC negative resistance VCO topology**

Center frequencies, tuning range, phase noise, and power consumption are the key metrics of a VCO. Center frequency and tuning range may differ for different applications and is typically influenced by temperature and other conditions, thus a wide tuning range is desirable (Jeong et al., 2012). A varactor is a voltage controlled capacitor used to tune the center frequency. VCO phase noise have a direct and negative effect on the overall performance of a wireless communication systems. In the receiver path, large blockers

and interferers at some offset frequency from the desired RF frequency would be folded into the frequency band of the desired signal through reciprocal mixing with the phase noise of the VCO at the same frequency offset (Jang & Wang, 2017). For quadrature mixing operation, a quadrature voltage controlled oscillator (QVCO) can be utilized (Jeong et al., 2006).

## **2.4 Wireless Standards**

The function of a radio receiver is to sense and extract selectively a desired signal within the electromagnetic spectrum. This selectivity, in the presence of many interfering signals and noise drives many trade-offs inherent in radio designs. The scarcity of the spectrum has grown gradually over the years. These days, the electromagnetic spectrum is crowded with literally millions of radio signals, thus interfering signals often lie in close proximity with the desired signal in frequency, thereby exacerbating the task of rejecting unwanted signals (Andreas, 2011). Lower frequency communication require huge antennas for efficient radiation, while signal losses tend to increase with higher frequency operation. The 2.4 GHz ISM (Industrial, Scientific, and Medical) band (2400-2483 MHz) is deemed to provide a fair trade-off in terms of cost, size and distance of communication, but more importantly the ISM band presents 80MHz of unlicensed bandwidth. The most common radio standards that utilize the 2.4 GHz band is the Bluetooth low energy (BLE) and ZigBee standards (Kazem et al., 2007). Hence the proposed design is tailored towards BLE and ZigBee standards.

Bluetooth low energy has a data rate of 1 Mbit/s with an average throughput of 270 kbit/s. It uses frequency hopping and Gaussian phase shift keying (GFSK) modulation, similar to classic Bluetooth (BT), but at a higher modulation index (0.5 instead of 0.35). This ensures the signal is easier to demodulate, but outcomes in a larger signal bandwidth.



It is configured in a star-bus hybrid network topology (Chang & Shin, 2016).

ZigBee is a standard from 2003, based on the 802.15.4 standard. It can operate in the 868MHz (Europe), 915MHz (North America) and 2.4GHz ISM bands, and it supports a mesh network topology with up to 65,536 nodes. Binary phase shift keying (BPSK) is used for lower data rates, and offset quadrature phase shift keying (OQPSK) for the highest data rate (Li et al., 2012). To improve resistance to interference, the signal is spread over a 5MHz wide channel using direct sequence spread spectrum (DSSS).

## **2.5 Receiver Specification**

In order for a receiver to be ZigBee and BLE compliant, it must satisfy a set of criterion as dictated by their corresponding standards. The following constraints form the major specifications for the design of the proposed front end (Pipino et al., 2015 ; Selvakumar et al., 2015; Tedeschi et al., 2010).

### **2.5.1 Sensitivity**

Receiver sensitivity is defined as the minimum signal power that can be detected by the receiver based on a designated accuracy. This accuracy commonly refers to the bit error rate (BER), which is the percentage of incorrectly measured bits over the transmission system. Incorrectly measured bits can be the due to the result of a weakly transmitted signal in the presence of large noise interferences in the air link or at the circuit level. The minimum sensitivity of a ZigBee compliant receiver is equal to  $-85\text{dBm}$  while a BLE compliant receiver is  $-70\text{dBm}$ . The sensitivity is mainly controlled by the NF of a system. To increase the sensitivity, the noise generated by a system needs to be decreased (Zhang et al., 2013).

### 2.5.2 Noise Figure

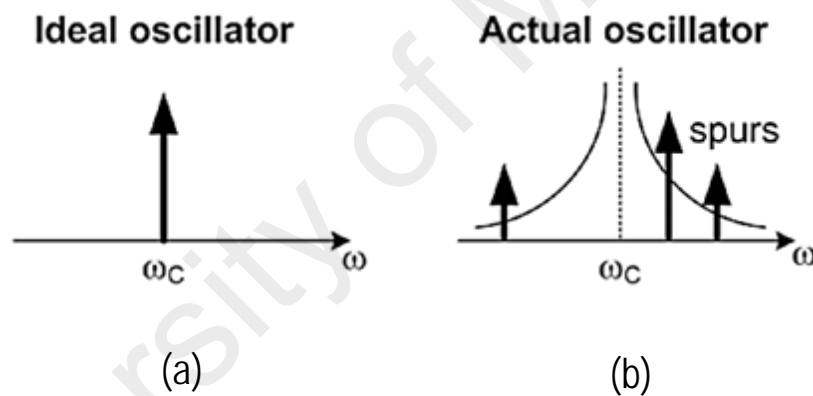
The receiver noise figure (NF) requirement can be calculated from the sensitivity test defined by the standard. NF indicates the SNR degradation from the circuit input to its output (Lee, 2004). With a 2MHz channel bandwidth, the noise figure of a ZigBee compliant receiver has to be lower than 20dB. For a BLE receiver with a BLE signal bandwidth of 1 MHz, the receiver NF should be lower than 30dB.

### 2.5.3 System Linearity

A receiver's susceptibility to interference can be described by its linearity performance. All semiconductor devices experience some level of non-linearity by producing undesirable harmonics at the output from a pure tone input. When two or more signals tones are fed into a non-linear device, intermodulation (IM) products are generated that may fall in-band with the desired signal, hence deteriorating the SNR. The source of these tones could be nearby signals that are picked up by the radio antenna. Specifically, the third order IM products in particular, are of special interest because they often fall very close to or within the favoured channel (Liu & Rabaey, 2011). For this reason the linearity of a receiver is often characterized via the IP3. This is often tested by the two-tone test, where two blockers are fed into a system to create the IM in the in-band of the signal. Higher IIP3 indicates weak intermodulation products with respect to the fundamental tone, and therefore a more linear system. Based on the respective standards, the minimum IIP3 of the Bluetooth Low Energy Receiver must be -37 dBm and resulting IIP3 requirement for ZigBee is -36.5dBm (Selvakumar et al., 2015). Because of the mixing phenomena, which translate frequency of a signal to a lower frequency, image frequency components exist and they have to be suppressed. This specification is called image rejection ratio. Based on required SNR and channel spacing of the respective standards, the image rejection ratio for BLE receiver is 21dB while for ZigBee receiver is 15dB.

### 2.5.4 Phase Noise

The RF front end down-converts the RF input signal to a lower frequency, through a mixing with a local-oscillator tone. Although ideally, the LO signal should be a single precise tone in frequency, an actual oscillator can only approximate it, generating a larger spectrum with some spurs (Razavi, 2012), as illustrated in Figure 2.19 . The spectrum enlarging is due to a random variation within the phase of the sinusoid at the oscillator output, and can be evaluated through the phase noise parameter in the frequency domain (Jang & Wang, 2017). This spectrum non-ideality reduces the SNR. In reality, at the receiver, the signal of interest may be accompanied by a large interferer in an adjacent channel. When the two signals are combined with the LO input, the down- converted



**Figure 2.19: (a) Ideal oscillator frequency spectrum, (b) Actual oscillator frequency spectrum**

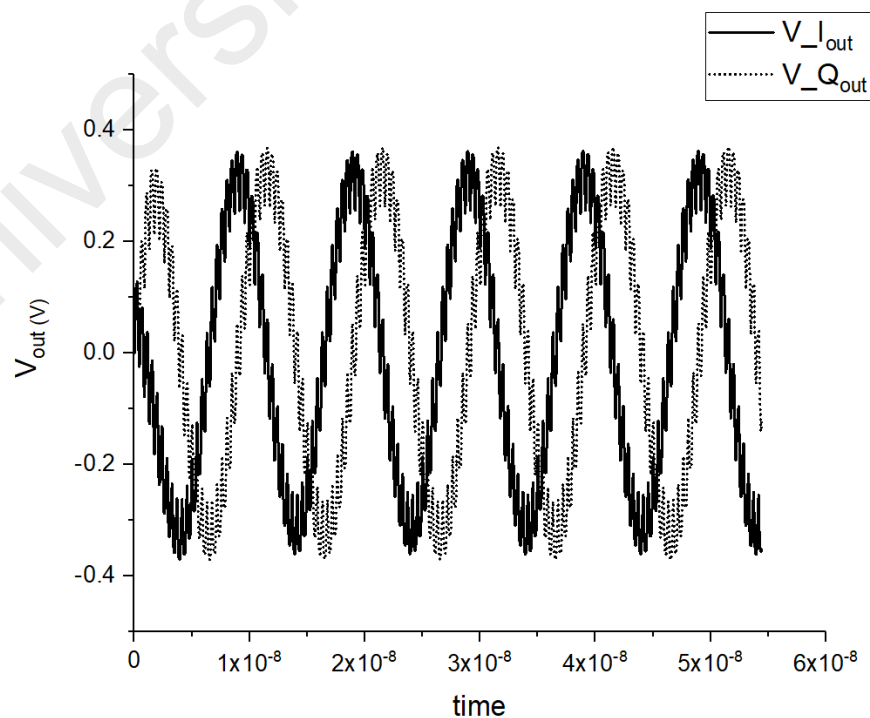
band consists of two overlapping spectra, with the wanted signal suffering from significant noise due to the tail of the interferer (Yao-Huang & Meng-Ting, 2005). This effect, is referred to as reciprocal mixing. This phenomena degrades the phase noise, which in turn causes the SNR of the output desired signal to deteriorate. The phase noise target of a ZigBee receiver at 1MHz offset from carrier frequency is -86dBc/Hz while for BLE receiver its -96dBc/Hz. Table 2.1 summarizes the key performance specifications required to be met by a BLE and ZigBee compliant receiver.

**Table 2.1: Target specification for BLE and ZigBee compliant receiver**

Design Parameter	ZigBee Target	BLE Target
Noise Figure	< 20dB	< 30dB
IIP3	> -36.5dBm	> -37dB
Image Rejection	> 15dB	> 21dB
Phase Noise @ 1MHz offset	< -86dBc/Hz	< -96dBc/Hz

## 2.6 Quadrature Mixing

With millions of cell phone subscribers gobbling up greater voice bandwidth, a modulation method that could efficiently transfer information in a reliable manner is required. New modulation techniques were developed in the past few years, schemes that are simply combinations of the original three modulation methods which are Amplitude Modulation (AM), Frequency Modulation (FM) and Phase Modulation (PM).

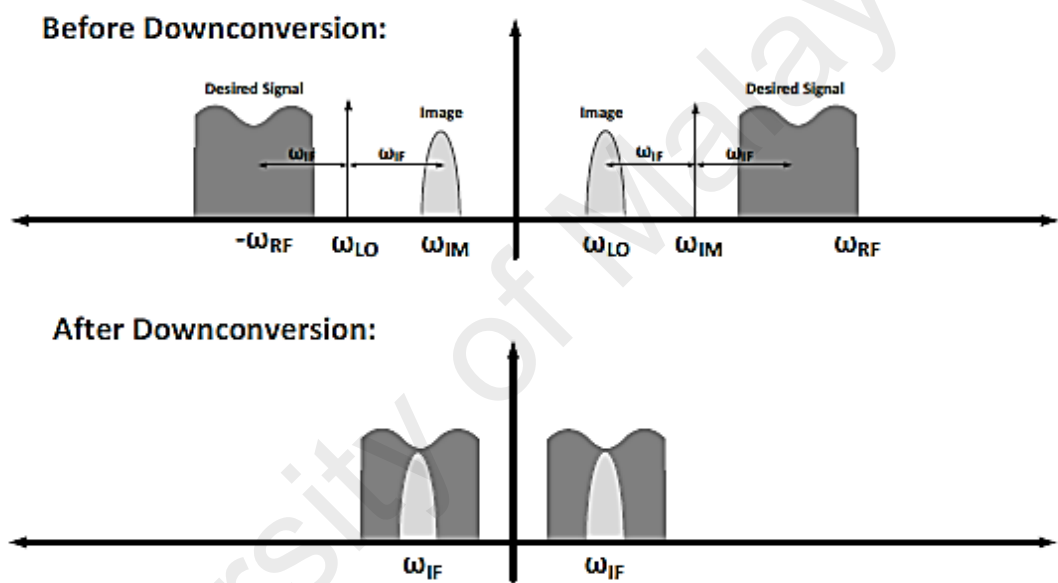


**Figure 2.20: IQ transient signal waveform**

Combined with other digital techniques, these newly affordable methods give more spectrum efficiency. One modulation technique that lends itself neatly to digital processes is known as IQ modulation, where "I" is the in-phase component of the waveform, and "Q" represents the quadrature component. In its diverse forms, IQ modulation is an efficient manner to transfer information, and it additionally works well with digital formats.

An IQ modulator can virtually create any type of analog modulation such as AM, FM and PM. Figure 2.20 illustrates an image of a pair of quadrature output signal. Therefore, in order not to lose any information, quadrature mixing is required in the receiver path to recreate back the baseband IQ signals. This IQ approach preserves all the information in the transmitted carrier signal (Lee, 2004). Based on the previous section, it is concluded that a low IF receiver architecture is the best candidate for low power and low cost solution. The Low-IF architecture adapts a low intermediate frequency, in the order of a few Megahertz. By doing so, a major challenge arises in terms of the image. Since the LO is located very close to the signal of interest, the image may also be closely placed to the signal, resulting preselection and channel filtering particularly difficult. Below in Figure 2.21 is the graphical illustration of the issues created because of image frequency components in which  $\omega_{RF}$  is the desired signal,  $\omega_{LO}$  is the oscillator signal,  $\omega_{IM}$  is the image signal and  $\omega_{IF}$  is the down converted signal after mixing. It could be observed that if the image frequency is down converted on top of the original desired signal IF band, this may substantially corrupt the desired signal if not dealt with carefully, as the two signals which lie within the same band are indistinguishable. However, by adapting quadrature mixing in the receiver path, the image can be suppressed, by creating two phase shifted copies of the image-corrupted signal which can then be used to reconstruct the original signal. With the use of trigonometric identities, the image can be removed without the need of any post-LNA image-reject filtering. The system makes use of two

mixers with their local oscillators or RF signal in a quadrature phase relationship, which separates the IF signal into in-phase (I) and quadrature (Q) components. The system then shifts the Q component by  $90^\circ$  before recombining the two paths, where the desired signal, present in both paths with identical polarities, is reinforced, while the image, present in both paths with opposite polarities, is cancelled out. To perform quadrature mixing in the receiver part, either RF or the LO signal needs to be phase shifted 90 degrees (Tedeschi et al., 2010). Conventionally, the quadrature signal is generated in the LO path because

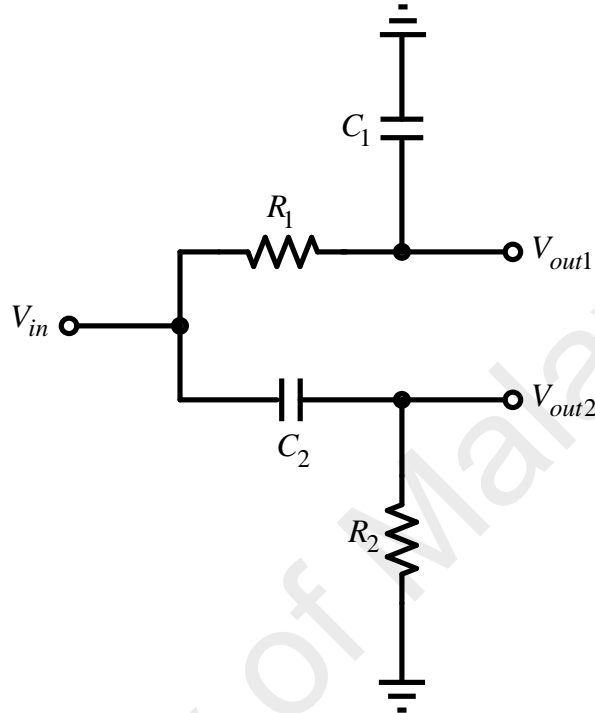


**Figure 2.21: Graphical view of image problem due to mixing**

the signal in the RF path is generally received in a vulnerable state, as it has propagated in air and hence is typically low in power. However in current years, with new standards arising up such as WPAN, in which performance such as sensitivity of receiver is not stringent, quadrature signal generation is being executed within the RF path to further save power and cost (Selvakumar et al., 2015). Below are some of the most common techniques used to generated quadrature signals.

### 2.6.1 RC-CR Network

Traditionally, the IQ outputs are generated by using a RC-CR phase shifter collectively with power-consuming phase correction circuits (Kluge et al., 2006). This technique



**Figure 2.22: RC-CR network topology**

utilizes passive resistor and capacitor. Figure 2.22 indicates a simple RC-CR network topology, which behaves as low pass and high pass filters. The two outputs are given as;

$$V_{out1} = \frac{1}{1 + sR_1C_1} \quad (2.35)$$

$$V_{out2} = \frac{sR_2C_2}{1 + sR_2C_2} \quad (2.36)$$

Hence, the resulting net outputs are  $90^\circ$  off each other. It can be easily observed that the phase variation between  $V_{out1}$  and  $V_{out2}$  is  $90^\circ$  for all frequencies. The output amplitudes are equal only at  $\omega = 1/(RC)$ , where,  $R=R_1, R_2$  and  $C= C_1, C_2$ . Since the absolute value

of RC varies with temperature and process, the frequency varies at the point of identical amplitude quadrature signals. The downside of this network is the low input impedance that it offers. This low impedance will load the preceding or subsequent block connected to this network. Therefore, a power hungry buffer is generally required in between this network. This will increase the overall power consumption of the system. Furthermore, this network introduces a 3dB insertion loss, which will further reduce the power of the signal.

### 2.6.2 RC Polyphase Filter

A polyphaser filter is used as another common way to generate quadrature signal. The implementation uses a single stage RC polyphaser filter which consist of four identical resistors and capacitors as illustrated in Figure 2.23 below. More stages could be added for more quadrature and amplitude accuracy (Behbahani et al., 2001 ). The working principle of a poly phase filter is the same as a RC-CR network; the only the difference is, that it needs to be driven by differential input signals which are 180° phase shifted

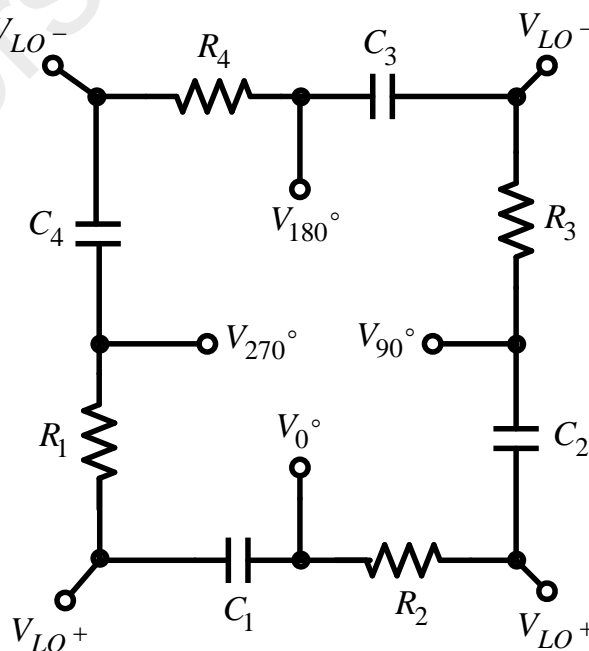


Figure 2.23: RC polyphase filter topology



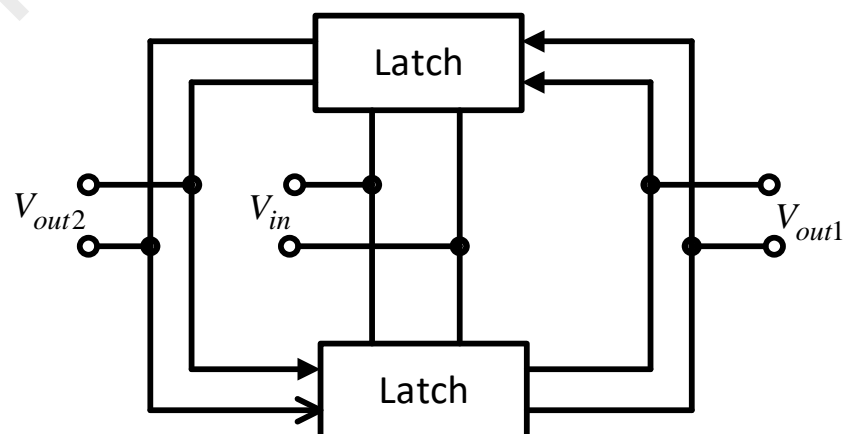
relative to each other. The poly phase filter generates four outputs which are  $0^\circ$ ,  $90^\circ$ ,  $180^\circ$  and  $270^\circ$ . This polyphase filter is widely used if a differential double balanced mixer is preferred. The operating frequency of the filter can be determined by:

$$\omega_0 = \frac{1}{2\pi R_i C_i} \quad (2.37)$$

where  $i= 1,2,3,4$ . The insertion loss associated with this filter is 3dB. An additional disadvantage of this filter is that it also needs a buffer in between blocks connected to the filter to prevent loading effect thus increasing the overall power consumption of the system. Moreover, it requires differential input signals which needed to be generated using power hungry bulky baluns.

### 2.6.3 Frequency Divider

An alternative approach in generating quadrature signals, is through frequency dividers as visible in Figure 2.24. The circuit is to use a master-slave flip flop to divide an input signal operating at twice its required operating frequency. The output signals frequency will be divided by a factor of two. If  $V_{in}$  has a 50% duty cycle, then  $V_{out1}$  and  $V_{out2}$  are  $0^\circ$  and  $90^\circ$  out of phase. Conventionally, this method is used with a VCO



**Figure 2.24: Frequency divider topology using flip flop**

operating at twice the operation frequency. It is easy to generate LO signal with high frequency in newer technology due to the high Q resonating tank it offers (Perumal et al., 2011). The drawback of this approach is the power required to sustain the higher tank oscillation frequency especially in low cost technologies. Furthermore, the master–slave flip flops, which have to be designed for the twice the frequency consume excessive power in current widely used CMOS technologies.

#### 2.6.4 Quadrature Voltage Controlled Oscillator

The most commonly used quadrature generation technique is the coupling of two symmetric LC-tank VCOs to each other, known as the quadrature voltage controlled oscillator (QVCO). As exemplified by the block schematic in Figure 2.25, the combination of a direct connection and a cross (inverting) connection forces the two VCOs to oscillate in quadrature. This produces  $0^\circ$ ,  $90^\circ$ ,  $180^\circ$  and  $270^\circ$  signals at the output (Huang et al., 2011).

The downside of this method is the increased power consumption to sustain the two tank oscillators. Moreover, it calls for two inductors in the VCO tank, thus the active area consumption of the full chip is enlarged, which subsequently increases the cost.

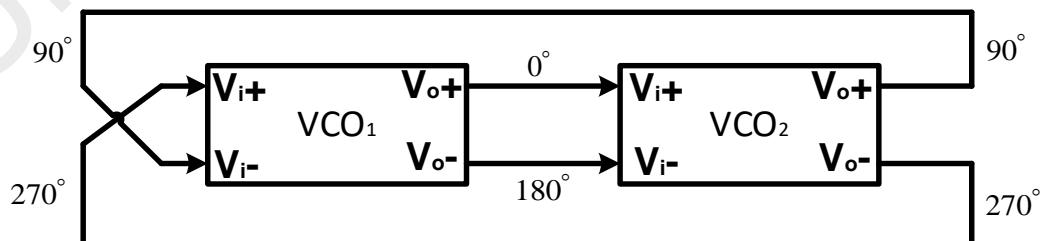


Figure 2.25: Quadrature VCO topology

## 2.7 Forward Body Bias

Body bias is used to dynamically regulate the threshold voltage ( $V_{th}$ ) of a CMOS transistor. While CMOS transistors are commonly thought of as a three terminal devices, with terminals for the source, gate, and drain, it's increasingly common to have a fourth terminal connected to the body (substrate) (Behzad Razavi, 2016). The voltage difference between the source voltage ( $V_s$ ) and body voltage ( $V_b$ ) impacts the  $V_{th}$ . Due to this, the body may be thought of as a second gate that helps determine how a transistor turns on and off. When the bulk voltage is higher than the source terminal voltage, the threshold voltage will reduce. This is called forward body bias and is given as,

$$V_{th} = V_{th0} + \gamma \left( \sqrt{|2\Phi_F + V_{sb}|} - \sqrt{|2\Phi_F|} \right) \quad (2.38)$$

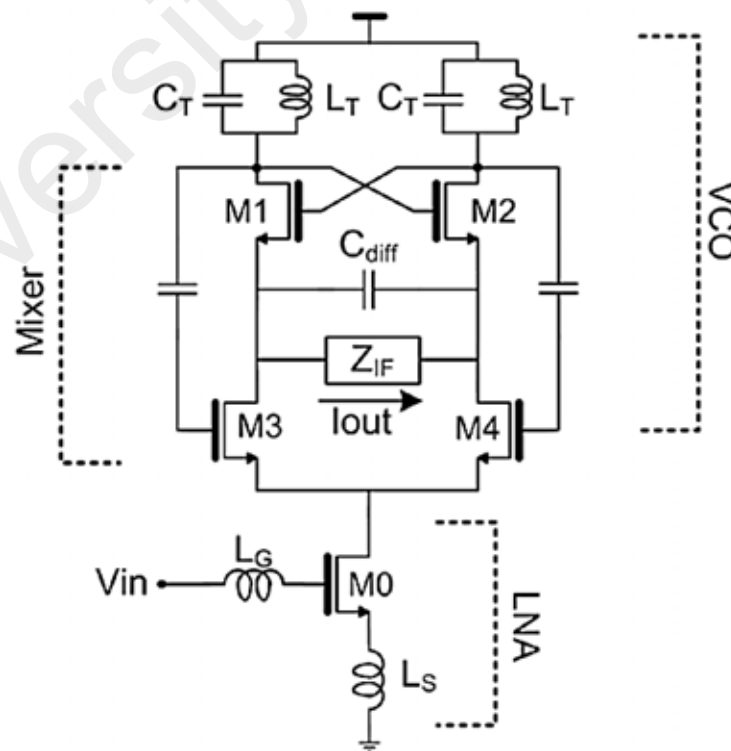
where  $V_{th0}$  is the initial threshold voltage without body voltage,  $V_{sb}$  is the source-bulk terminal potential difference,  $q$  is the electron charge,  $\epsilon_{si}$  denotes the dielectric constant of silicon,  $N_{sub}$  is the doping density of substrate,  $C_{ox}$  is the gate-oxide capacitance per unit area,  $\Phi_F = \left(\frac{kT}{q}\right) \ln\left(\frac{N_{sub}}{N_i}\right)$ , and  $\gamma = \sqrt{2q\epsilon_{si}N_{sub}}/C_{ox}$ . By applying this technique, the supply voltage could also be decreased to lessen the power consumption. For silicon based CMOS technology, the body voltage could go up to 0.7V with negligible leakage (Tan et al., 2017).

## 2.8 State of the Art Review

WPAN applications like ZigBee and BLE demands less sensitivity, hence performance merit is often sacrificed for extended battery life and cost reduction (Masuch & Delgado-Restituto, 2013). Efficient power consumption can be achieved by sacrificing some voltage headroom. A number of ultra-low-voltage and ultra-low-power receivers have been reported recently (Lin et al., 2014b; Wang & Li, 2015; Wang et al., 2016 ; Zhang et al., 2013) . The supply voltage was reduced down to 0.5 V in (Chong et al., 2014, ), with

a penalty of a higher current consumption due to the folded topology. The drawback is the high bias current cannot be reused. In (Zhang et al., 2013), many bulky passive and resonant elements which consume less voltage drop are entailed to facilitate the bias and tune out the parasitics due to headroom reduction down to 0.3 V. It is observed that reducing the supply voltage is more promising in advanced technologies due to the low threshold voltage and high transit frequency it offers. Thus, each block can be cascaded and tuned independently to improve the performance. But this advanced technologies nodes also come with high fabrication cost.

For long channel devices in older processes, an efficient way to reduce the power is by cascading the blocks to reuse the bias current. (Liscidini et al., 2006), introduced the first full receiver block which allows the LNA, VCO and Mixers to share the same bias current as dispatched in the Figure 2.26. Known as the LMV (LNA + Mixer + VCO) cell, it allows significant power reduction and enables the bias current to be reused between



**Figure 2.26: Original LMV cell topology**

blocks making use of the currents more efficiently. The drawback is that it uses simple mixing operation hence not suitable for recent IQ modulation techniques. Furthermore it also adopts two LC tank, which increases the area of the overall system. Tedeschi et al., (2010), reports that with a low quality factor (Q) inductor, the VCO and LNA bias current is almost equal (Tedeschi et al., 2010). By cascoding both of the blocks via bias current reuse, quadrature generation could be generated in the RF path in contrary to the conventional method of quadrature LO path using QVCO or frequency dividers. This enables significant power and cost reduction compared to the original LMV (LNA + Mixer + VCO) cell. Hence, this work took the LMV cell one step further by improving the cell as shown in Figure. 2.27. The design incorporates only a single differential LC tank, and the quadrature signal is generated in the RF path. The drawback of these topologies are in the use of off-chip inductors to facilitate matching and current incompatibility. The LNA usually requires large bias current for amplification and low noise, where else the mixers requires less bias current for proper switching and to reduce

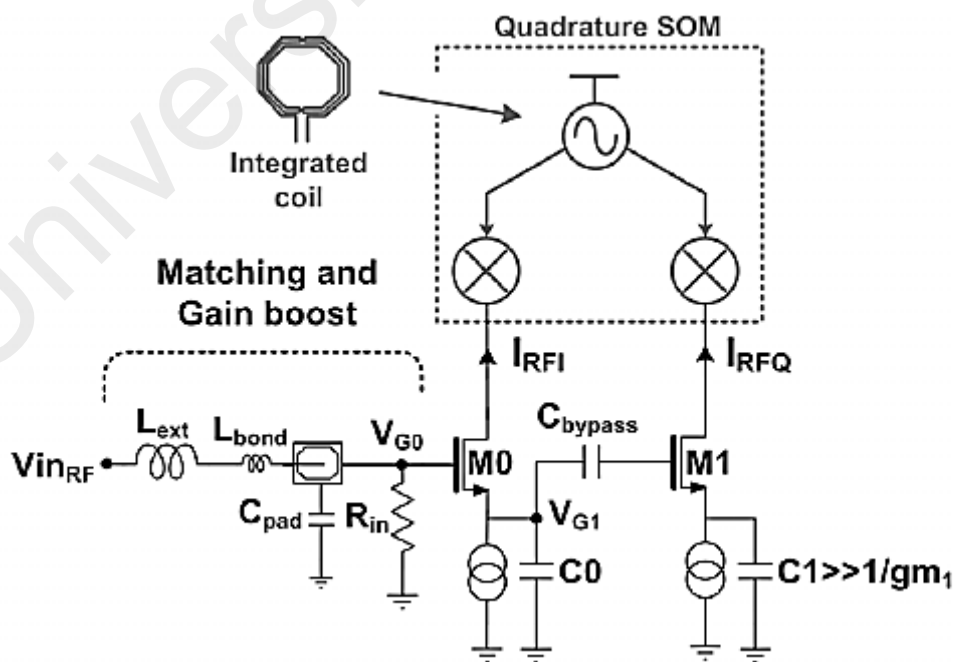
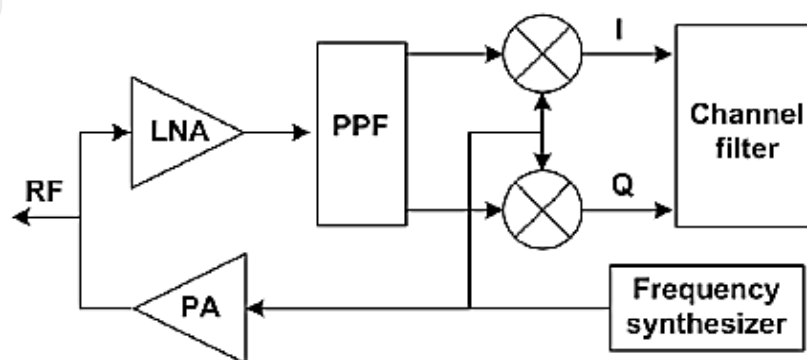


Figure 2.27: Improved LMV cell topology

flicker noise. Also, by using the inherent mixing capability of VCO as mixers (self-oscillating mixer, SOM), the LO-RF leakage due to parasitic coupling will deteriorate the linearity and overall system performance as the same transistors are used for the mixer and VCO. Furthermore, by reusing the LNA as the tail current source of the VCO as in (Selvakumar et al., 2015), the sizing of the transistor introduces tradeoff. The VCO tail current source usually is sized large to reduce its flicker noise contribution, but for RF operation, the sizing should be small to reduce the parasitic.

It can be observed that by generating quadrature signals in the RF path, power and cost could be reduced significantly. Another architecture which offers quadrature generation at the RF path is shown in Figure 2.28 as given by (Kluge et al., 2006). Here a single stage polyphaser filter was used directly after the LNA to generate the quadrature signal. The drawbacks are in the losses associated by the filter. To compensate the loss, a high gain LNA was used which consumed considerably high power. Furthermore the high bias current is not effectively utilized due to the cascading of blocks. Meanwhile in (Lin et al., 2014b), a mixed supply voltage approach is used for optimum performance. This technique alleviates the design trade off of RF and baseband blocks but the complexity of the power management block and cost is increased due to the need of extra power management such as DC-DC converter and LDO (Peng et al., 2018). Table 2.2



**Figure 2.28: Kluge's Low IF quadrature receiver block diagram**

summarized the review of state of the art architectures discussed in this section.

**Table 2.2: Summary review of state of the art architectures**

Ref.	(Chong et al., 2014)	(Tedeschi et al., 2010)	(Selvakumar et al., 2015)	(Kluge et al., 2006)	(Lin et al., 2014a)
VDD (V)	0.5	1.2	0.8	1.8-3.6	0.6/1.2
PDC (mW)	0.9	3.6	1	10	0.9
External Matching	no	yes	yes	yes	no
Require LDO	yes	yes	yes	yes	yes
BB Method	no I/Q	With I/Q	With I/Q	With I/Q	With I/Q
CMOS technology	130nm	90nm	130nm	180nm	65nm
Sub-Blocks	LNA + Mixer	LMV+ TIA+ Complex filter	LMV+ TIA+ Complex filter	LNA+ PA+PPF+ VCO +IQ Mixer+ Complex Filter	Blixer+ Hybrid filter+ PPF

## CHAPTER 3: CMOS RECEIVER DESIGN

### 3.1 Introduction

WPAN applications like ZigBee and BLE demands less sensitivity, therefore performance merit is often sacrificed for prolonged battery life and cost reduction (Selvakumar et al., 2015). This makes ZigBee and BLE ideal for low cost, low power and portable coin battery operated devices which helps facilitate IoT. Saving the power consumption may be accomplished by sacrificing some voltage headroom. However, a nominal coin battery voltage is 1.5V, and hence a more appropriate manner to save power is to lessen the current drawn by the battery. This may be achieved through reusing the bias current among multiple blocks. Therefore, the proposed receiver will be operated by a 1.5V coin battery, thus eliminating the need of an on-chip LDO. The current is decreased by employing the benefits of cascode and cascade principles. Cascode permits bias current reuse, while cascade provides good isolation between blocks and hence, each block can be tuned independently. Moreover, quadrature generation is generated within the RF path, thus eliminating the need of QVCO or the power hungry frequency dividers.

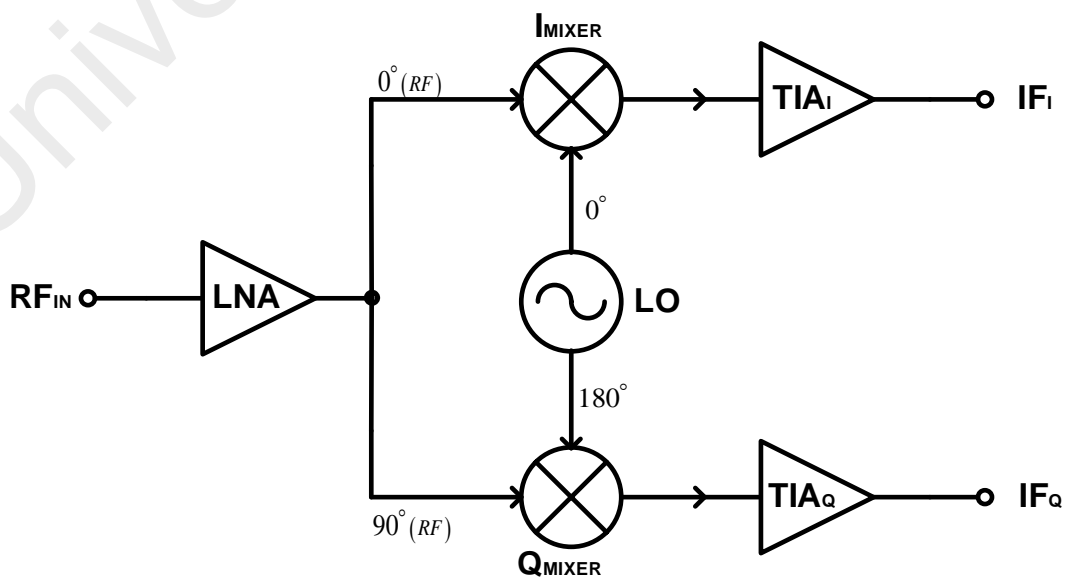
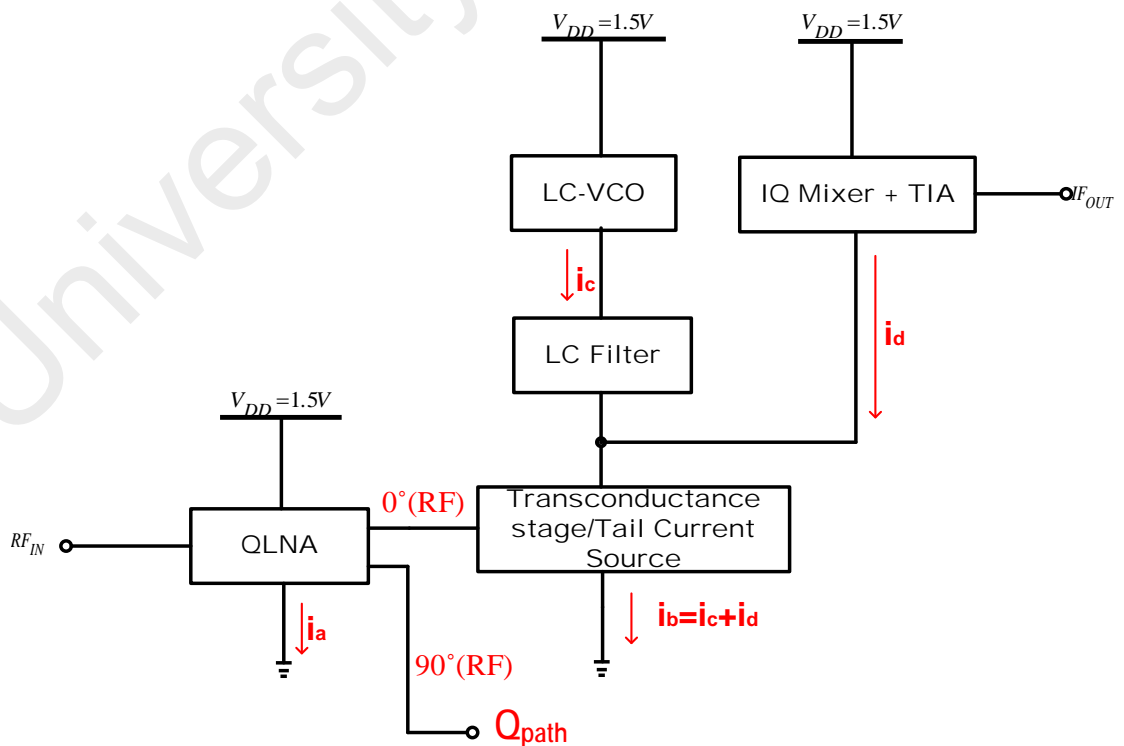


Figure 3.1: Conceptual view of the proposed low IF receiver



This in addition, reduces further the cost and power. The process technology of standard CMOS 180nm is adapted, as it offers an exceptional balance between performance and cost, catering towards BLE/ZigBee compliant devices, and additionally realizing the SoC concept. Fig. 3.1 indicates the conceptual view of the proposed front end receiver block. It is headed by a single-ended QLNA to avoid the balun, while offering I/Q outputs. The resultant I/Q signals are routed to the cascaded single-balanced I/Q mixers which are driven with a LC VCO. The trans-impedance amplifier (TIA) is stacked on top of each mixer through current-reuse principle to complete the design. Low-intermediate frequency (IF) reception, 100MHz is selected to reduce the flicker noise effect of CMOS devices, since the BLE and ZigBee are both in narrowband standards. Figure 3.2 illustrates the block diagram representation of the working principal of the proposed receiver, where the essential RF and baseband functions are merged in one cell for current reuse. It can be observed that the LNA is employed in a cascade structure. As a result, it can be optimized independently and this offers the possibility to embed the quadrature



**Figure 3.2: Block diagram of the working principle of proposed receiver**

generation scheme into the LNA. By cascading the active IQ mixer with the LC VCO, the device reuse and bias current reuse approach is adopted. The transconductance stage of the mixer is reused as the tail current source of the VCO while the bias current of the switching stage of the mixer is redirected back to the VCO.

### 3.2 Proposed Receiver Design

The detailed schematic of the proposed receiver is depicted in Figure 3.3. The RF signal ( $RF_{IN}$ ) is firstly amplified by transistor  $M_0$ , which provides the I/Q outputs at  $V_{OUT1}$  and  $V_{OUT2}$ . The resultant I/Q signals is further amplified by the single-balanced active I/Q mixers consisting of transistors  $M_1$  and  $M_2$  (transconductance stage of active mixers), before translating the signal to low-IF frequency output via transistors  $M_7, M_8, M_{11}$  and  $M_{12}$  (switching stage of active mixers). Two TIAs are stacked atop the I/Q mixers and the mixing signal is generated with the aid of a complementary LC VCO. The key techniques used are: 1) A single-transistor quadrature LNA which allows both input

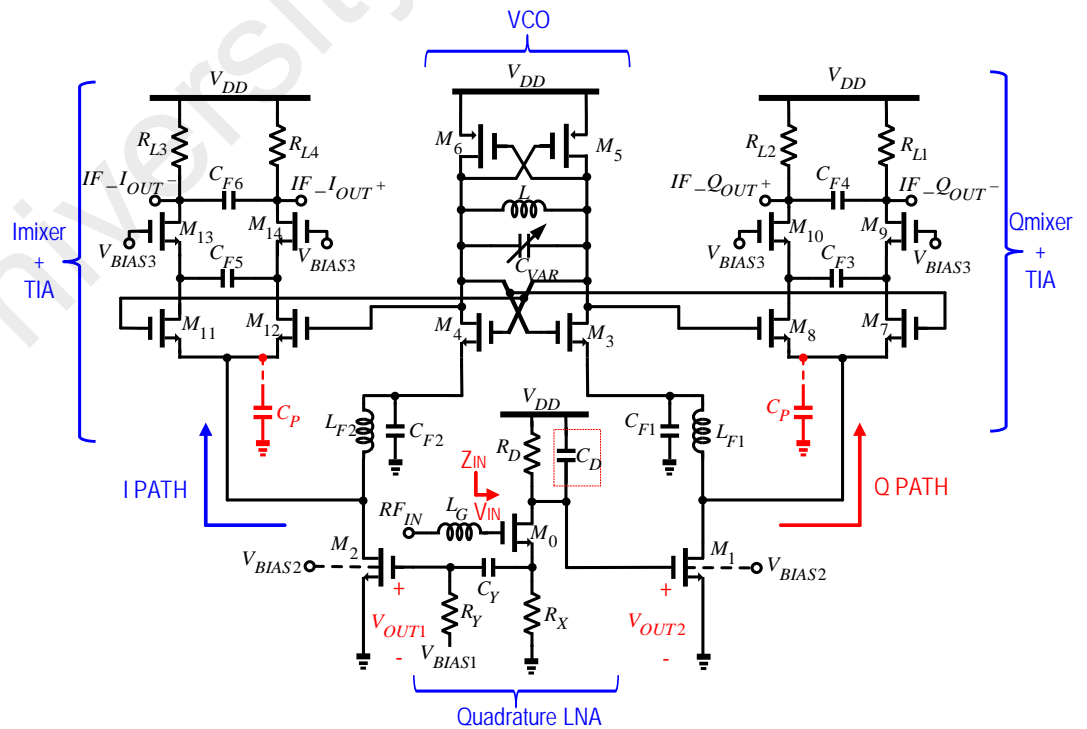


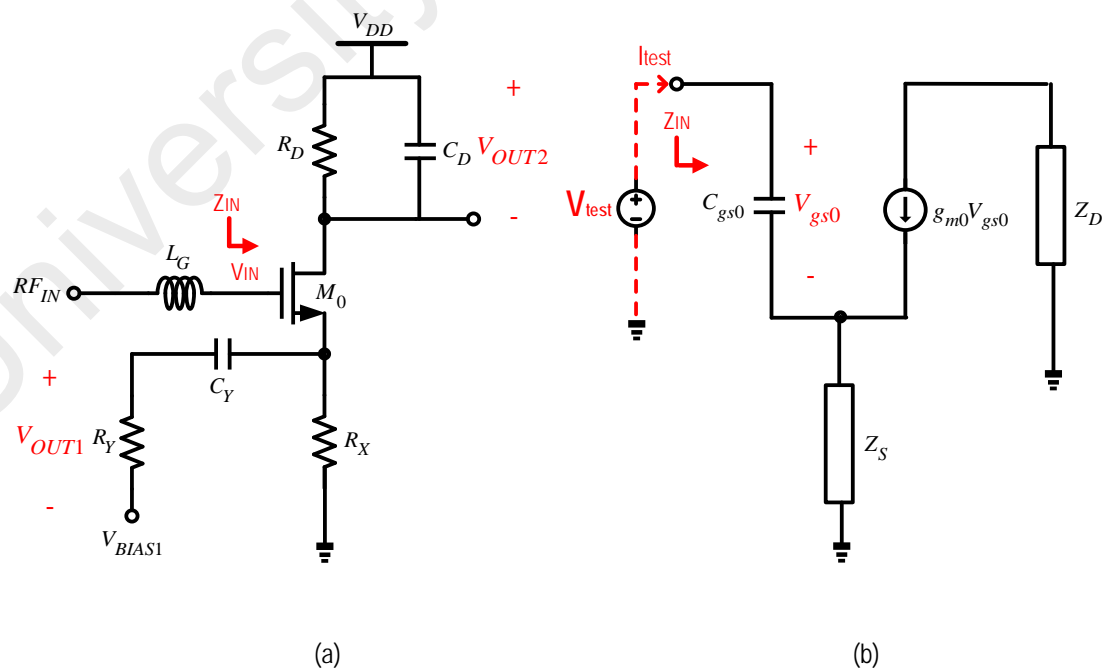
Figure 3.3: Complete schematic of the proposed receiver

impedance matching and passive I/Q generation; 2) The advantages of cascode and cascade are fully utilized in this receiver architecture; 3) A LC filter is formed in the mixer- VCO interface that improves the phase noise, linearity and isolation, and 4) a TIA as the load of the mixer improving the conversion gain and out-of-band filtering. Detailed description of each building block are given in the sub-subsequent sections below.

### 3.2.1 Quadrature LNA

In WPAN applications, performance and sensitivity **are** not stringent, where else cost and power are more critical (i.e., can have NF ~30 dB) (Selvakumar et al., 2015; Tedeschi et al., 2010). Hence NF will not be analyzed further due to the lenient sensitivity requirements. This opens up the opportunity to use resistors to aid in generating the I/Q signals in the RF path, as opposed to the conventional way of I/Q LO generation. Thus, a trade-off is achieved between noise and area favouring towards low cost implementation.

Figure 3.4 (a) illustrates the proposed quadrature LNA. A simple single transistor



**Figure 3.4: (a) Proposed QLNA circuit topology, (b) Small signal analysis of the QLNA for input impedance analysis**

topology consisting of  $M_0$  with resistive degeneration and load is adapted for the LNA which exhibits low power, ease of input impedance matching, adequate gain and linearity, moderate noise and also providing quadrature outputs. By cascading the LNA to the subsequent block rather than cascoding,  $M_0$  can be scaled independently to optimize the performance.  $M_0$  acts as a common-source and common-drain amplifier simultaneously, in reference to the input RF signal. It generates differential signals in the output with unbalanced amplitudes with the aid of  $R_D$  and  $R_X$  (active balun). The ac coupling capacitor,  $C_Y$  and bias resistor,  $R_Y$  of the LNA are used to transform the differential outputs to a quadrature output as opposed to the conventional poly-phase RC-CR filter. An additional capacitor,  $C_D$  is added to increase the gate source capacitance of subsequent stage of  $M_1$ . To calculate the input impedance of the proposed QLNA for matching and maximum power transfer, the small signal analysis is done as dispatched in Figure 3.4 (b). A test voltage  $V_{test}$  is connected to the input of the QLNA and the resulting current  $I_{test}$  is analyzed to compute the input impedance. The resultant of the analysis of the input impedance in the LNA is shown in (3.1), where  $g_{m0}$  is the transconductance of transistor  $M_0$ . The complete derivation is shown in Appendix A.

$$Z_{IN} = \frac{R_X \left( C_{gs0} \left( 1 + \omega^2 C_Y^2 R_Y (R_Y + R_X) \right) - g_{m0} C_Y R_X \right)}{C_{gs0} \left( 1 + \omega^2 C_Y^2 (R_Y + R_X)^2 \right)} - j \left[ \frac{\left( (g_{m0} R_Y + 1) R_X + R_Y \right) (R_Y + R_X) C_Y + R_X^2 C_{gs0}}{\omega C_{gs0} \left( 1 + \omega^2 C_Y^2 (R_Y + R_X)^2 \right)} C_Y \omega^2 + g_{m0} R_X + 1 \right] \quad (3.1)$$

To simplify (3.1), the following assumptions can be made over the operating frequency of interest:

$$\omega^2 C_Y^2 (R_Y + R_X)^2 \gg 1 \quad (3.2)$$

$$\omega^2 C_Y^2 R_Y (R_Y + R_X) \gg 1 \quad (3.3)$$

After simplification, by equating the real part of the input impedance to  $50 \Omega$  at the desired resonance frequency,  $\omega_0$  as shown in

$$R_X \parallel R_Y \left[ 1 - \frac{g_{m0} R_X}{\omega_0^2 C_{gs0} R_Y C_Y (R_Y + R_X)} \right] = 50 \Omega \quad (3.4)$$

and adding a single gate inductor  $L_G$  to cancel out the imaginary part losses,

$$L_G = \frac{1}{\omega_0^2 C_{gs0}} \left[ 1 + (R_X \parallel R_Y)^2 \left( \frac{C_{gs0}}{R_Y^2 C_Y} \right) + g_{m0} (R_X \parallel R_Y) \right] \quad (3.5)$$

adequate matching is obtained at the desired operating frequency for maximum, power transfer. The negative term in (3.4) for the operating frequency is much lesser than the positive term here, thus the stability is guaranteed. The  $L_G$  value can be approximated from (3.5). The two outputs of the LNA are given as

$$V_{OUT1} = \frac{g_{m0} R_X}{g_{m0} R_X + 1} \left[ \frac{s R_Y C_Y}{\left( \frac{R_Y C_Y + R_X C_Y + g_{m0} R_X R_Y C_Y}{g_{m0} R_X + 1} \right) s + 1} V_{IN} \right] \quad (3.6)$$

$$V_{OUT2} = - \frac{g_{m0} R_D}{[(R_D C_D) s + 1] (g_{m0} R_X + 1)} \left[ \frac{(R_X C_Y + R_Y C_Y) s + 1}{\left( \frac{R_Y C_Y + R_X C_Y + g_{m0} R_X R_Y C_Y}{g_{m0} R_X + 1} \right) s + 1} V_{IN} \right] \quad (3.7)$$

It can be observed that both the output responses are high-pass. Setting  $R_D C_D = R_X C_Y + R_Y C_Y$  ( $C_D$  aids to set this condition), the response of  $V_{OUT2}$  can be transformed to low-pass given as,

$$V_{OUT2}' = - \frac{g_{m0} R_D}{g_{m0} R_X + 1} \left[ \frac{1}{\left( \frac{R_Y C_Y + R_X C_Y + g_{m0} R_X R_Y C_Y}{g_{m0} R_X + 1} \right) s + 1} V_{IN} \right] \quad (3.8)$$

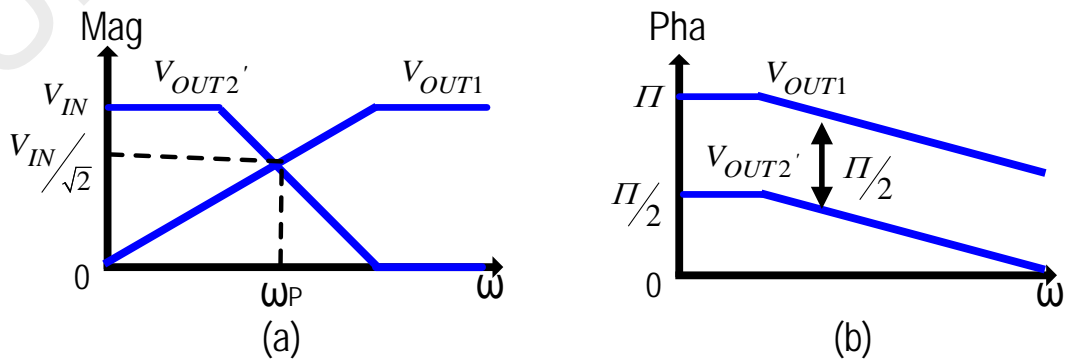
Here  $V_{OUT2}'$  is the output voltage at the drain terminal of  $M_0$  after the transformation. Under this condition, both outputs show a common cut-off frequency. The low-pass and high-pass responses ensure robust quadrature phase relationship is obtained over a reasonable range of frequency (i.e., the 2.4-GHz ISM band only has an 80 MHz bandwidth). The cut-off frequency  $\omega_C$  could be set at the desired operating frequency by

$$C_Y = \frac{g_{m0}R_X + 1}{(R_X + R_Y + g_{m0}R_X R_Y)\omega_C} \quad (3.9)$$

Amplitude matching could be obtained by choosing

$$R_D = \frac{R_X R_Y}{R_Y + \frac{R_X}{g_{m0}R_X + 1}} \quad (3.10)$$

The losses of the quadrature generation circuit is compensated by the passive gain obtained by the series input-matching network. This matching network also creates a narrowband filter at the input that benefits in avoiding any large blockers, interferers and injection-locking phenomena. Amplitude matching is only obtained at the cutoff frequency but the quadrature relationship is maintained for a large range of frequency as illustrated in Figure 3.5. In this topology, by choosing  $R_D$  and  $C_Y$  diligently, amplitude matching and quadrature relationship could be obtained allowing easier calibration with

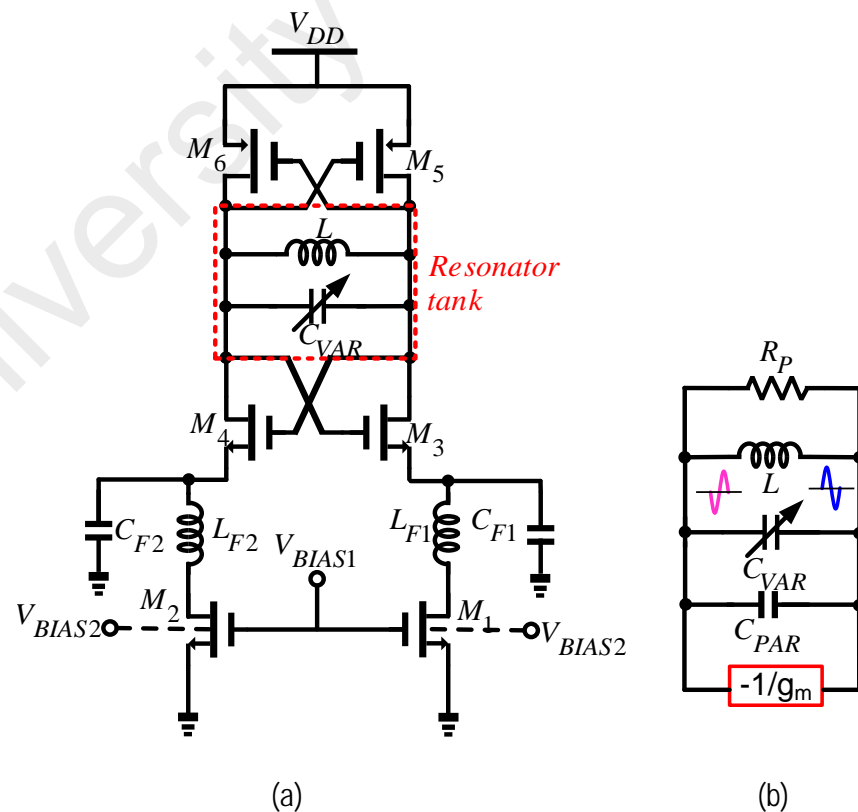


**Figure 3.5: (a) output amplitude response of the QLNA (b) output phase response of the QLNA**

a single resistor and capacitor. Furthermore, the proposed topology only utilizes one inductor as compared to the conventional low noise amplifier with source degeneration topology which requires at least three, catering towards low cost and small size.

### 3.2.2 VCO

LC tank based VCO is adopted in this design due to the inherent better phase noise performance it offers compare to the ring oscillator counterparts in wireless applications. Current consumption is dependent to the Q of the resonator tank, hence full complementary VCO is favored over the NMOS-only designs, due to the extra negative resistance it offers with the same bias current. The proposed complementary VCO is depicted in Figure 3.6(a).  $M_1$  and  $M_2$  act as the tail current source to set the bias current. The compensating transconductance,  $g_m$  stages consist of  $M_3 - M_6$ . Figure 3.6 (b) shows the equivalent model of the VCO at resonance, which is a lossy LC tank consisting of



**Figure 3.6: (a) Proposed LC-Complementary VCO with integrated filter, (b) The equivalent small signal model of the VCO**

inductor  $L$ , parasitic resistance of the inductor  $R_P$ ,  $C_{PAR}$  and varactor,  $C_{VAR}$ . Capacitor  $C_{PAR}$  models all the parasitic capacitances induced by the VCO active devices and the subsequent I/Q mixers. The negative transconductance,  $-1/g_m$ , is the equivalent transconductance of the cross coupled active devices. In the steady state, the tank parallel loss,  $R_P$ , and the negative active resistance,  $-1/g_m$ , cancels each other in order that the remaining circuit is ideally a lossless LC tank with a variable capacitor (varactor). In CMOS implementations, generally, the tank loss is dominated by the inductor loss and is given as,

$$R_P = 2Q_L L \omega_C \quad (3.11)$$

where  $L$  is the inductor value in the oscillator tank,  $Q_L$  is the quality factor of that inductor and  $\omega_C$  is the operating frequency. To sustain the oscillation, the minimum  $g_m$  required to cancel the parasitic resistance  $R_P$  is given as,

$$-\frac{1}{g_m} = 2Q_L L \omega_C \quad (3.12)$$

hence,

$$g_{m\_min} = \frac{1}{2Q_L L \omega_C} \quad (3.13)$$

Contrary, the NMOS only VCO design offers negative resistance of  $-2/g_m$ , which in turn requires a  $g_{m\_min}$  of double the complementary VCO to cancel the same parasitic resistance and sustain oscillation. Therefore, complementary VCO halves the power half which caters towards low power operation. A derivation on this is given in Appendix B. The drawback of the additional transconductance stage (complementary) is the noise and parasitic capacitance of these additional devices. For WPAN applications, the bandwidth and noise requirements is relaxed, thus a trade-off is balanced between power with the



tuning range and phase noise favoring towards low power. The oscillating frequency is set by,

$$f_c = \frac{1}{2\pi\sqrt{L(C_{VAR} + C_{PAR})}} \quad (3.14)$$

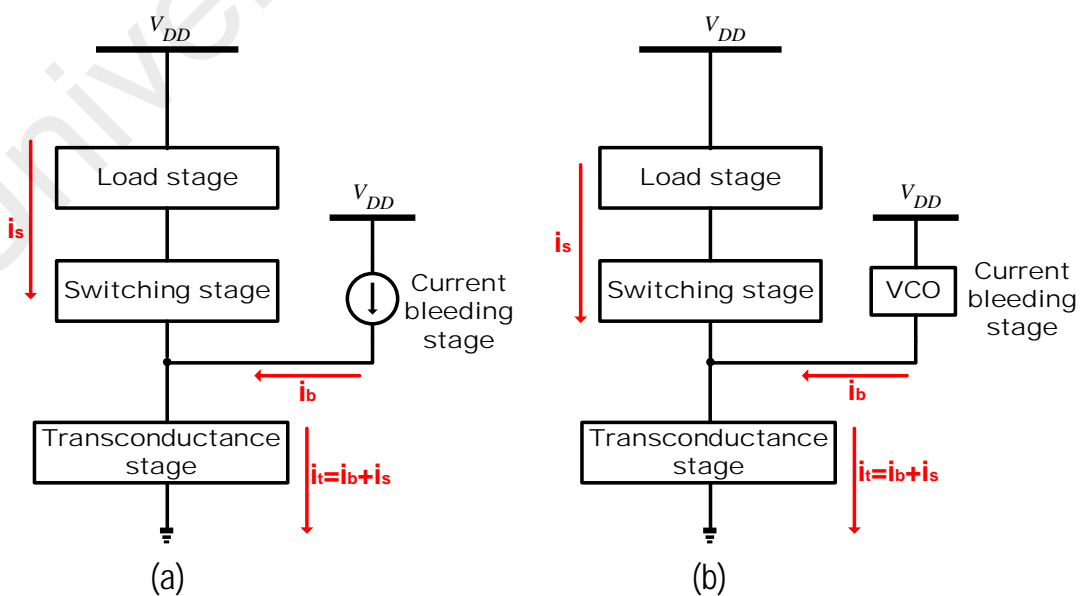
The varactor size is chosen slightly higher than the parasitic capacitance,  $C_{PAR}$  so that the tuning of frequency is preserved. NMOS varactor is favored for analog frequency tuning due to its low capacitive loading. An inductor of 1.9 nH is chosen to minimize the power consumption while still maintaining a reasonable 8.3% frequency tuning range from 2.3 to 2.5 GHz. Furthermore, the sizing of the active  $-g_m$  devices were done diligently to ensure less parasitic capacitances and ensure maximum output amplitude is obtained to reduce the subsequent stage I/Q mixers noise and linearity.

By integrating an independent LNA at the first stage, the tail current source of the VCO can be sized optimally for an independent VCO performance. This tail current source is split into two. The advantage of this technique along with I/Q generation in the RF path is that it opens the possibility to use a single LC tank to drive the I/Q mixers to save both power and area. An LC filter consisting of  $L_{F1}$ ,  $C_{F1}$  and  $L_{F2}$ ,  $C_{F2}$  are integrated between the tail current source and the complementary transconductance stage. This filter prevents the VCO signal to leak out and also ward off other signals from entering into the VCO and degrading the oscillating signal. Furthermore, this also allows the current source transistors  $M_1$  and  $M_2$  to be reused for other operation, hence facilitating device reuse principal. The extra area induced by the filter is justified in the subsequent section. Dimensions of both the tail current source  $M_1$  and  $M_2$  are identical.

### 3.2.3 IQ Mixers + TIA

Single-balanced I/Q mixers are employed due to the low power and area constraint.

Active mixers are preferred to compensate for the losses in the preceding quadrature generation circuit. In an active mixer, usually the transconductance stage requires large bias current for amplification, where else the switching stage requires less bias current to reduce flicker noise (Song et al., 2007). The conventional method of achieving this in single-balanced mixer is by deploying the current-bleeding technique. This technique is adopted here but rather than adopting charge injection technique using additional current sources, the VCO is used as the current source by taking advantage of the LC filter used in the mixer-VCO interface. The innovation is illustrated in the block diagram in Figure 3.7. The transconductance stage is responsible for the conversion gain in active mixers and transconductance scales proportionally with bias current. Hence, by deploying this technique, the bias current in the transconductance stage is  $i_t = i_b + i_s$  where  $i_t$  is the total bias current in the transconductance stage,  $i_b$  is the bleeding current offered by the vco and  $i_s$  is the bias current in the switching stage. Hence, the switching stage current can now be minimized by increasing the bleeding current to acquire the preferred conversion gain. Furthermore, the bias current of the VCO to sustain the oscillation is generally high, hence this indirectly benefits the transconductance stage.



**Figure 3.7: (a) The conventional current bleeding technique in mixer, (b) Proposed current bleeding technique via VCO**

Figure 3.8 shows the proposed IQ single balanced mixer loaded with TIA. The incoming quadrature RF signal from the QLNA is firstly amplified by the transconductance stage of the mixer via transistor  $M_1$  and  $M_2$ . The signals are then routed to the low DC current switching stage consists of  $M_7 - M_8$  and  $M_{11} - M_{12}$ , while the VCO bias current is led to the transconductance stage via the inductors  $L_{F1}$  and  $L_{F2}$ . This also enables the current source of the VCO with high bias current to be used as the transconductance stage of the mixer to amplify the incoming quadrature RF signal thus, enabling the current and device reuse technique.  $M_1$  and  $M_2$  are forward body biased to improve its amplification, noise performance and relaxes the I/Q mixers voltage headroom consumption. The switching quads are biased in the vicinity of the threshold voltage to enable low bias current, thus reducing thermal noise, flicker noise and gate-source capacitance offering a better switching efficiency. Acknowledging that transistors are nonlinear devices, the LC filter also provides isolation between RF and LO path.  $L_{F1} - L_{F2}$  in Figure 3.8 provides a high

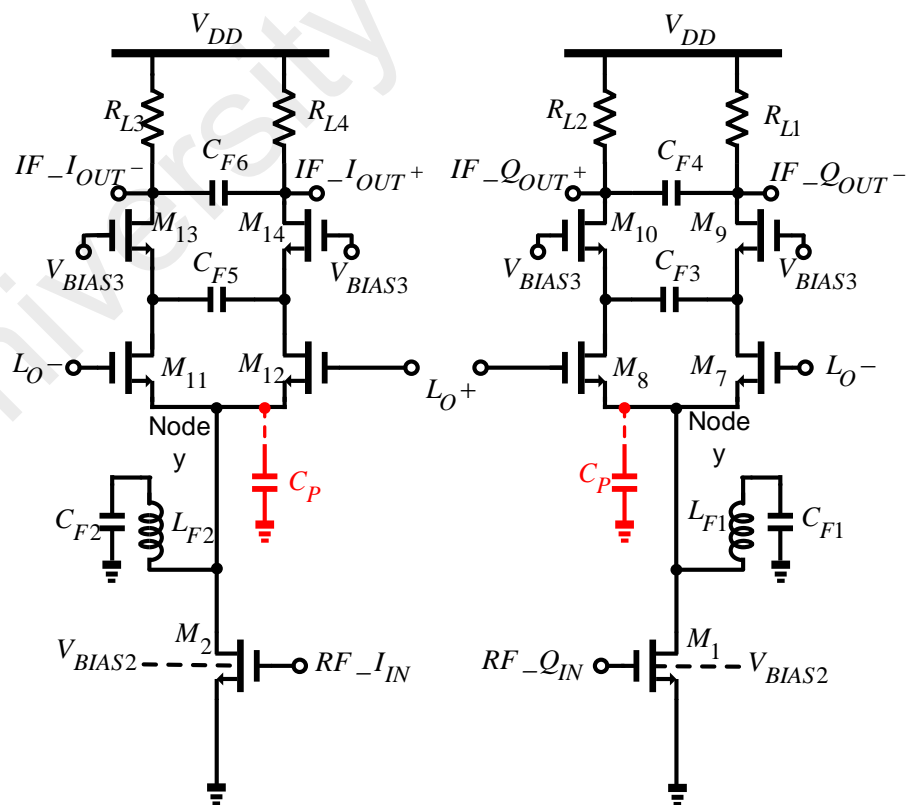


Figure 3.8: Proposed IQ mixer loaded with TIA schematic

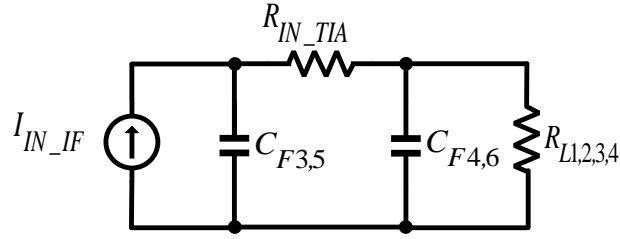
impedance to the higher-order harmonics generated from the LNA and transconductance stage from going into the VCO tank and degrading the phase noise, while the capacitors  $C_{F1} - C_{F2}$  shorts any leakage of RF or LO signals to ground. Generally the mixing point of the mixer, denoted as 'Node y' in Figure 3.8, is the point where many parasitic capacitances connect. Hence this node is usually the bottleneck of high conversion gain in high frequency operation. The parasitic capacitances in that node, lumped represented as  $C_p$ , provides a low impedance path and leaks the RF signal current to ground rather than to the switching stage of mixer. Hence in the proposed topology,  $L_{F1} - L_{F2}$  also resonates with the total parasitic capacitance at the mixing point of the source terminal in the switching quads, improving the conversion gain and minimizing leakage. The mixer switching stage bias current is then routed back to the transconductance stage which also serve as the VCO's current source thus improving the gain and phase noise performance. Thus the quadrature current from the I and Q paths going into the I/Q mixers switching stage is given as:

$$I_I = -g_{m2}V_{OUT1} \quad (3.15)$$

$$I_Q = -g_{m1}V_{OUT2}' \quad (3.16)$$

where,  $V_{OUT2}'$  is the output voltage at the drain terminal of  $M_0$  after the transformation.

A transimpedance amplifier (TIA) consisting of  $M_9 - M_{10}$  and  $M_{13} - M_{14}$  is integrated at the top of the mixers with additional capacitors  $C_{F3}$ ,  $C_{F4}$  and  $C_{F5}$ ,  $C_{F6}$  to ensure there is sufficient filtering in the current mode. This TIA also acts as a cascode amplifier, hence boosting the output impedance which results in higher conversion gain. Large resistive loads  $R_{L1} - R_{L4}$  are added to each TIA to convert the resultant output signal to voltage and is given, neglecting parasitic capacitances for simplicity as,



**Figure 3.9: Conceptual view of filtering effect obtained due to TIA**

$$A_{V_I} = \frac{2}{\pi} g_{m2} (R_{L3,4} \parallel R_{out}) \quad (3.17)$$

$$A_{V_Q} = \frac{2}{\pi} g_{m1} (R_{L1,2} \parallel R_{out}) \quad (3.18)$$

Figure 3.9 illustrates the conceptual view of the filtering effect obtained due to the use of TIA. The additional capacitors filter out the RF, LO and other high-frequency components from the output signal. Proper sizing of the TIA and capacitors results in a cut-off at ~100 MHz given as,

$$f_c = \frac{1}{2\pi \sqrt{R_{IN\_TIA} C_{F3,5} R_{L1,2,3,4} C_{F4,6}}} \quad (3.19)$$

where  $R_{IN\_TIA}$  is the input impedance of the TIA,  $C_{F1,3}$  are the capacitors connected to the source terminal of the TIA transistor,  $C_{F4,6}$  are the capacitors connected to the drain terminal of the TIA transistor and  $R_{L1,2,3,4}$  are the load resistors.

This approach proves that by adopting the LC filters, a single block is capable of generating LO signal, RF signal amplification, mixing and filtering using the same bias current. It also enables the use of a large resistive load to improve the conversion gain and also lowers the noise contribution of the mixer, thus minimizing the tradeoff between conversion gain and linearity.

### 3.3 IF Output Balun + Buffer

The RF signal which was fed to the receiver, produces quadrature balanced differential IF signals. In order to measure the performances of the receiver, this quadrature IF signals needs to be combined, for the ease of measurement. Acknowledging that the signals are now at low frequency, hence active baluns are preferred to minimize losses. Furthermore, the external measurement devices have a standard impedance of  $50\ \Omega$ , hence buffers are needed to match the impedances of the balun to the measurement devices for maximum power transfer. Since the IF frequency is relatively low at 100MHz, a simple differential amplifier is adapted as the balun followed by a source follower topology functioning as a buffer. The schematic is shown in Figure 3.10. The balun is directly connected to the output port of the receiver for self-biasing and the gain is set slightly above one to compensate the losses associated by the subsequent buffer, external devices and cable losses. The output of the balun is directly connected to the buffer, which is designed such that the output reflection coefficient matches with  $50\ \Omega$  in order to achieve maximum power transfer.

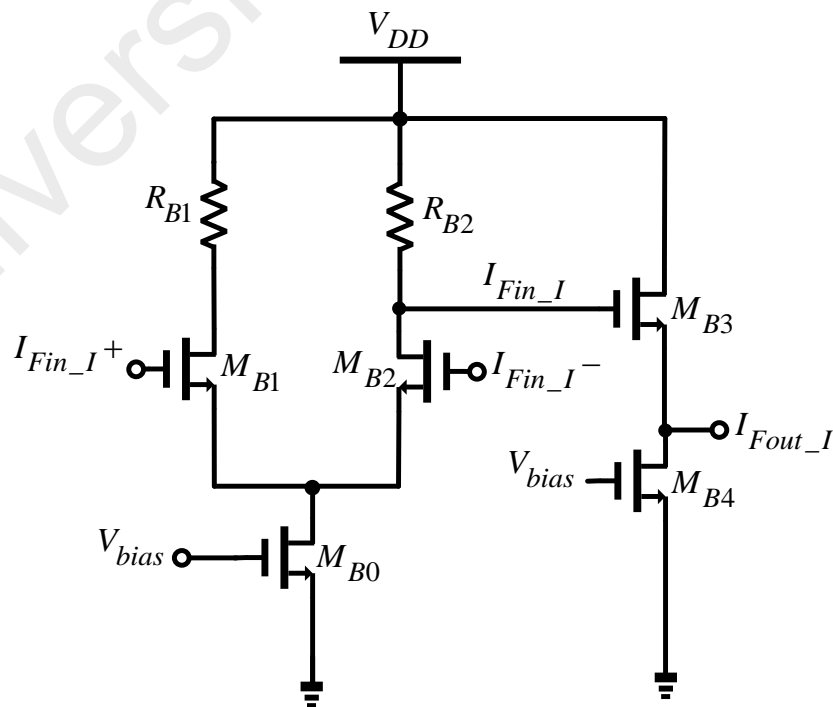
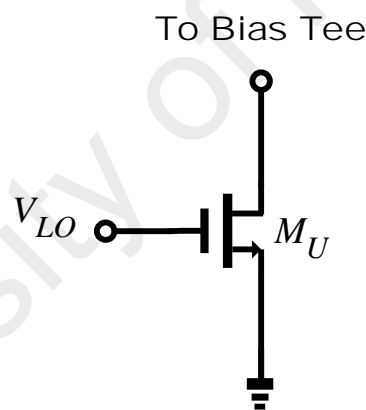


Figure 3.10: Schematic of balun + buffer for measurement purpose

### 3.4 Open Drain Buffer

To measure the VCO frequency and output signal power, two open drain buffer, as depicted in Figure 3.11 is connected to the VCO differential outputs, where  $V_{LO}$  is the differential oscillation signal of the VCO. This buffer adapts a common source topology, but here the load is left open. During measurement, an external bias tee will be connected to the open drain buffer to activate the circuit and connect the VCO to a signal source analyser, which measures the VCO performance. It is also used for frequency tuning across the BLE and ZigBee channels. The open drain buffer is designed as small size as possible, so that the parasitics does not affect the tuning range of the VCO and the gain is set to unity.

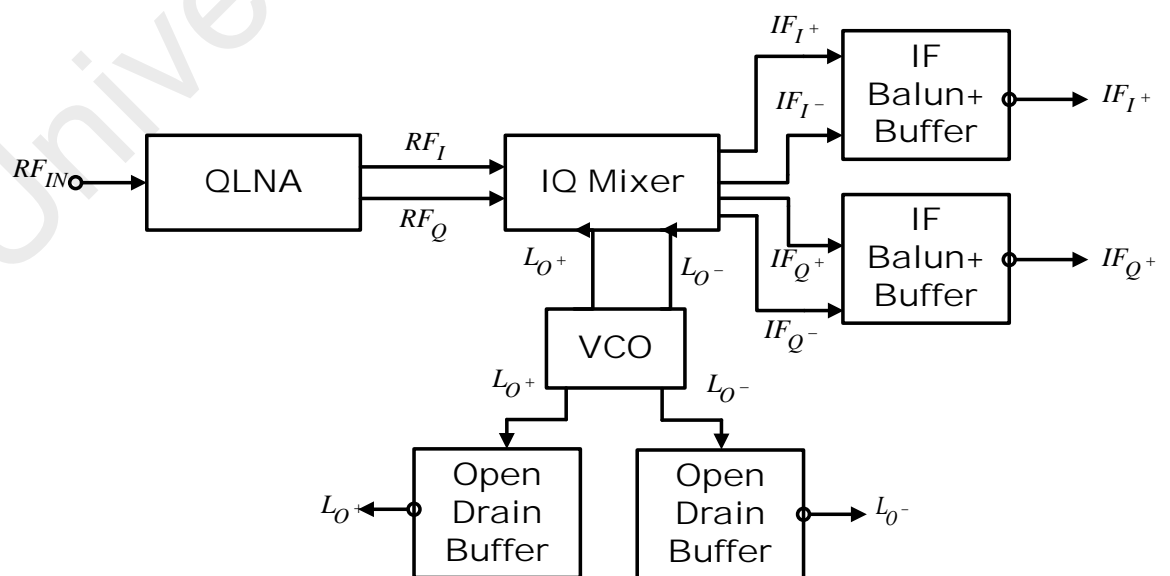


**Figure 3.11: Schematic of open drain buffer for measurement purpose**

### 3.5 Complete circuit integration

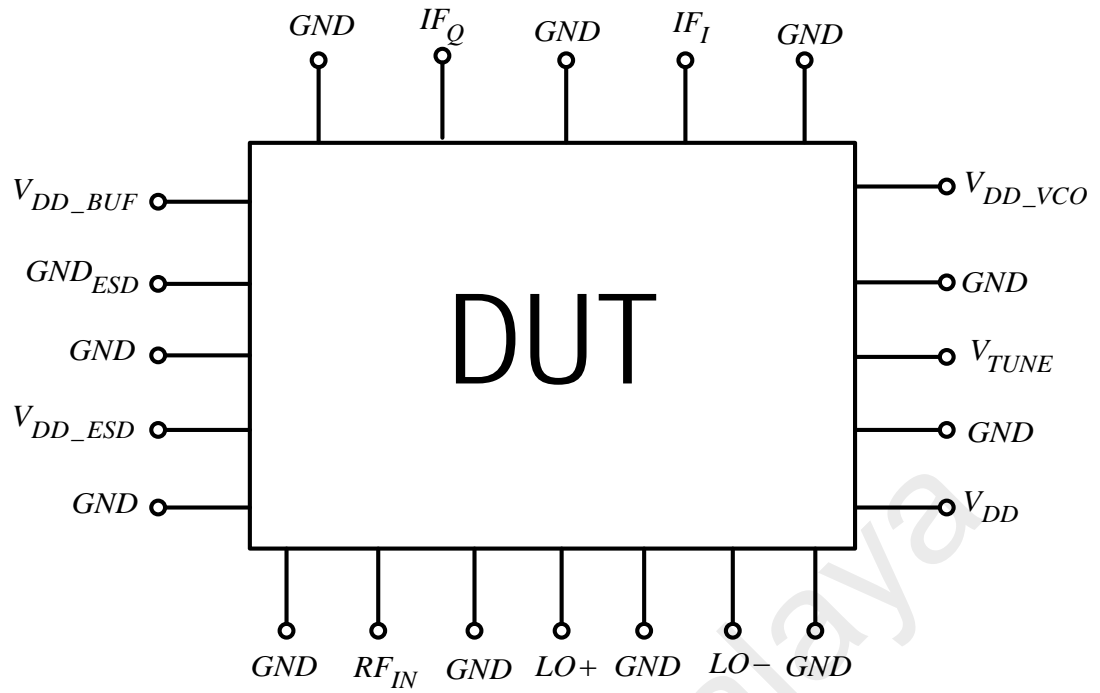
All the blocks presented in this chapter are integrated on chip, forming a complete CMOS receiver circuit architecture. The complete design ready for measurement is represented as a block diagram, demonstrated in the Figure 3.12. As there are multiple input and output ports, and also taking into account the measurement equipment's limitation, a

careful floor planning and block placements are necessary in order to ease the characterization of hardware. In IC design, area is impending cost. Hence each building block is properly located, taking into account the length of interconnect, and signal self-interference. RF and LO signals, which are high frequency signals, are placed as far as possible since both signals are categorized as critical signals which contain information. The proposed arrangement of the input and output ports for measurement set up of the receiver is given in the Figure 3.13. Here,  $V_{DD}$  is the main supply for the receiver consisting of the LNA and IQ mixers. The VCO is a very sensitive block. Phase noise is very prone to voltage supply noise, hence we have dedicated two external voltage supplies for the VCO which are  $V_{DD\_VCO}$  for powering it up and  $V_{TUNE}$  for frequency tuning purpose. These two external supplies are connected to large capacitors for adequate supply noise filtering. For the balun and buffers, which are only needed for measurement purpose, they have their own external supply voltage,  $V_{DD\_BUF}$ . For the ESD protection circuits, an independent  $V_{DD\_ESD}$  and  $GND\_ESD$  are designated. This circuits protects the chip from sudden voltage and current spikes. The proposed physical layout is designed to be as compact as possible to reduce active area of the silicon. The



**Figure 3.12: Block diagram of full integration receiver for measurement**





**Figure 3.13: Device under test for measurement purpose**

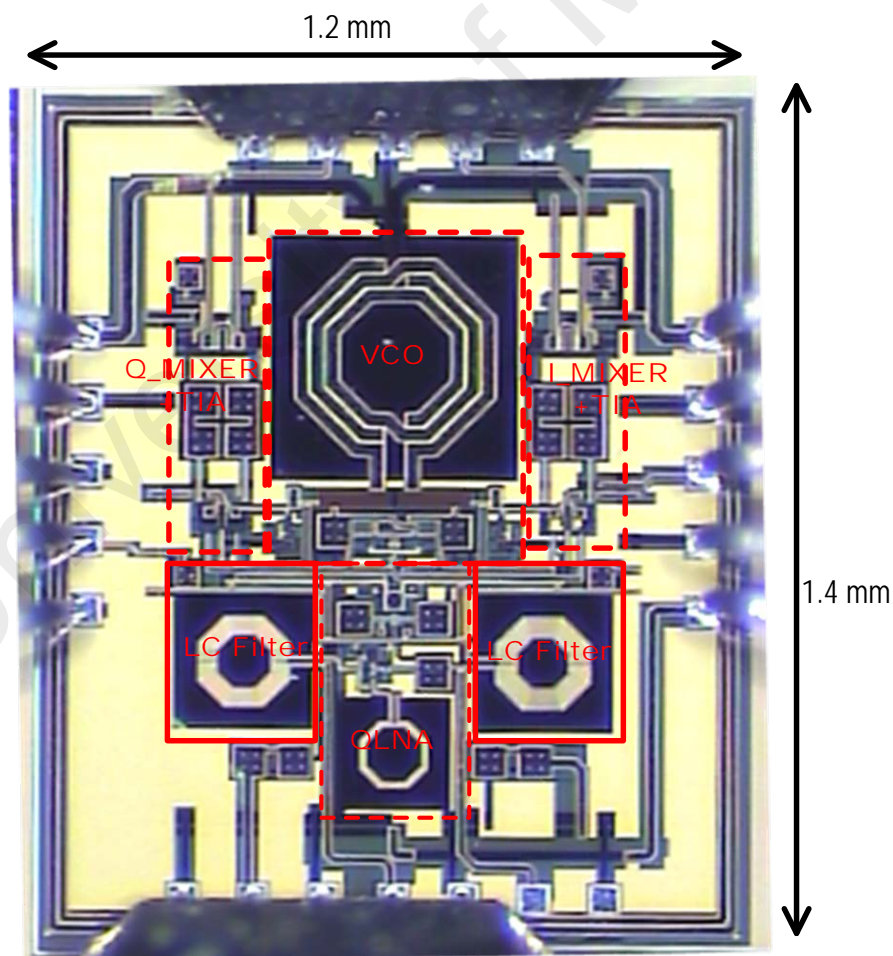
proposed receiver integrated with baluns and buffers consumes  $1.2 \text{ mm} \times 1.4 \text{ mm}$  chip area including the RF bond pads. RF probes with GSGSG (Ground-Signal-Ground-Signal-Ground) configuration and pitch size of  $0.15 \text{ mm}$  are adapted in the measurement set up. Multi finger RF transistors are used to reduce gate resistance, hence improving the noise performance. Acknowledging that RF transistors are prone to PVT, dummy poly gates are adopted in the RF transistors to minimize device mismatch after fabrication. Metal- Insulated Metal (MIM) capacitors are preferred due to their superior accuracy to process variation at high frequency operations and larger capacitance density, hence smaller size. High sheet resistance in poly resistor with dummy poly layer is selected to minimize area and withstand process variations. In the layout configuration, I/Q mixers are placed closed to the VCO in layout to reduce the routing length. This prevent loading effect and reduced tuning range while the LNA is spatially separated for better isolation and reduced magnetic couplings (Baker, 2010).

## CHAPTER 4: RESULTS

This chapter discusses the measurement results obtained for the proposed low IF CMOS receiver. This design was simulated using Cadence Spectre-RF. The physical layout was realized using cadence layout editor and RC parasitic extraction was performed using Mentor Calibre platform. The original measurement result plots have been smoothed by taking the averages for easier observation of the behaviour of the system across the BLE and ZigBee channels.

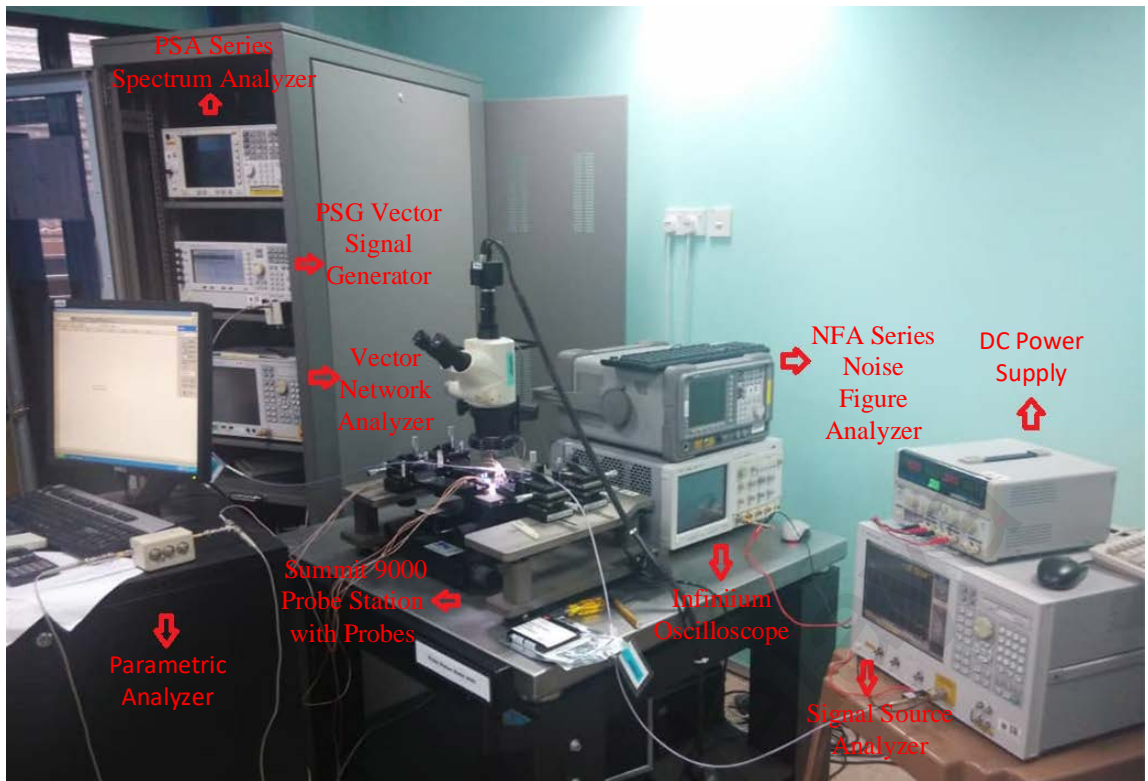
### 4.1 Measurement Results

The mask layout of the proposed design was fabricated using a commercial single poly



**Figure 4.1: Photomicrograph of the fabricated proposed receiver**

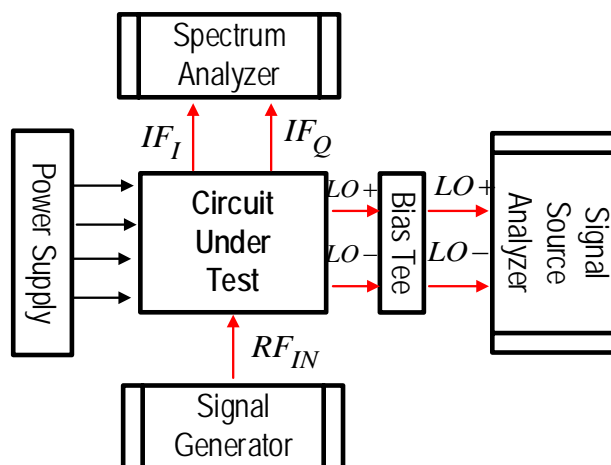
six metal layer 180nm CMOS technology which also offers twin well technology. The microphotograph of the fabricated chip which occupies a die area of 1.2 mm × 1.4 mm is illustrated in Figure 4.1. On-wafer measurement probing was carried out to characterize the proposed receiver and acquire the measurement data. Probe station Summit 9000 from Cascade Microtech was utilized as the measurement platform to measure the fabricated chip. The RF probe tips from Cascade Microtech under Air Coplanar Probe (ACO) family with GSGSG pattern are used to provide and measure the RF/IF signals. Here, G is ground and S is signal. To provide DC supply and ground signal, the DC probe series from Cascade Microtech under multi-contact DC Quadrant (DCQ) power probe series was utilized and the supply was generated by the Precision Semiconductor parameter analyzer. This parameter analyzer supply the voltages to power up the on-chip devices and is capable of handling voltages up to 40V and DC current up to 200mA. It additionally provides real time monitoring and tracking of selected voltage and currents flowing into the chip. Both the DC and RF probes have five tips with a pitch distance of 0.15mm. A Vector Network Analyzer (VNA) was used to measure the impedance matching, power transfer and the S-parameters. The PSG vector signal generator (250 kHz - 44GHz) was used to generate the RF input signal to measure the behavior of the proposed design. To measure the output IF signals, the 4 channel based Infiniium oscilloscope was adopted to measure the quadrature response where else a PSA series spectrum analyzer was used to measure the linearity and conversion gain performance. The noise performance was captured using a NFA series Noise Figure Analyzer (NFA) equipped with a noise source. The VCO performance was measured using a Signal Source Analyzer (SSA). The measurement setup used to measure the proposed receiver are illustrated in Figure 4.2. Large DC blocks capacitors are used to protect the measurement devices from DC voltages. The graphical test set up configuration to measure each performance parameter will be briefly discussed in the following section along with measurement results.



**Figure 4.2: Complete measurement set up**

#### 4.1.1 Conversion Gain (CG)

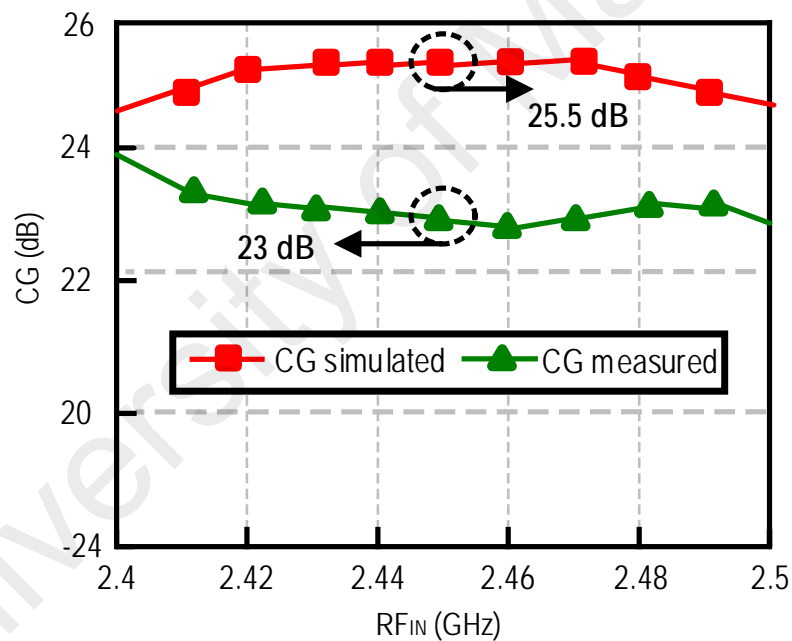
The measurement setup used to characterize the conversion gain of the proposed design is conceptually illustrated in Figure 4.3. The signal generator feeds the RF signal into the input of the proposed design chip. The receiver is powered on by a VDD of 1.5V supplied



**Figure 4.3: Test setup for CG measurement**

by the power supply and it generates quadrature balanced IF outputs. These I and Q outputs are then fed into the spectrum analyzer to measure the conversion gain. The VCO's output is connected to a signal source analyzer via a bias tee to tune to the desired channel. Measurements for all BLE/ZigBee input frequencies was done by sweeping the incoming RF signal frequency from 2.4GHz to 2.5GHz and adjusting the LO frequency via the varactor tuning to bring the resulting IF frequency to 100 MHz. This is done to cover the whole BLE/ZigBee channel bandwidth. The down conversion of RF input signal is governed by the following expression:

$$f_{IF} = f_{RF} - f_{LO} \quad (\text{low side injection}) \quad (4.1)$$



**Figure 4.4: Post layout simulation and measurement results of CG**

Hence, for an input RF signal of 2.4GHz, the VCO is tuned to oscillate at 2.3GHz to downconvert the RF signal to 100MHz IF. Likewise, for a RF input signal of 2.45GHz, the VCO is retune to 2.35GHz to convert the resulting input signal to 100MHz IF. This measurement set up was also used for P1dB and IIP3 characterization. The conversion

gain (CG) acquired for all BLE/ZigBee channels are illustrated in the Figure 4.4. Meanwhile, Figure 4.5 shows the measured result obtained from the spectrum analyzer for an input frequency of 2.4GHz with power level of -20dBm. The output signal is obtained around 100MHz with a power level of 4 dBm, hence resulting towards a conversion gain of about 24dB. The discrepancy between simulation and measured results is about 2.5 dB, which might be due to signal loss and PVT.

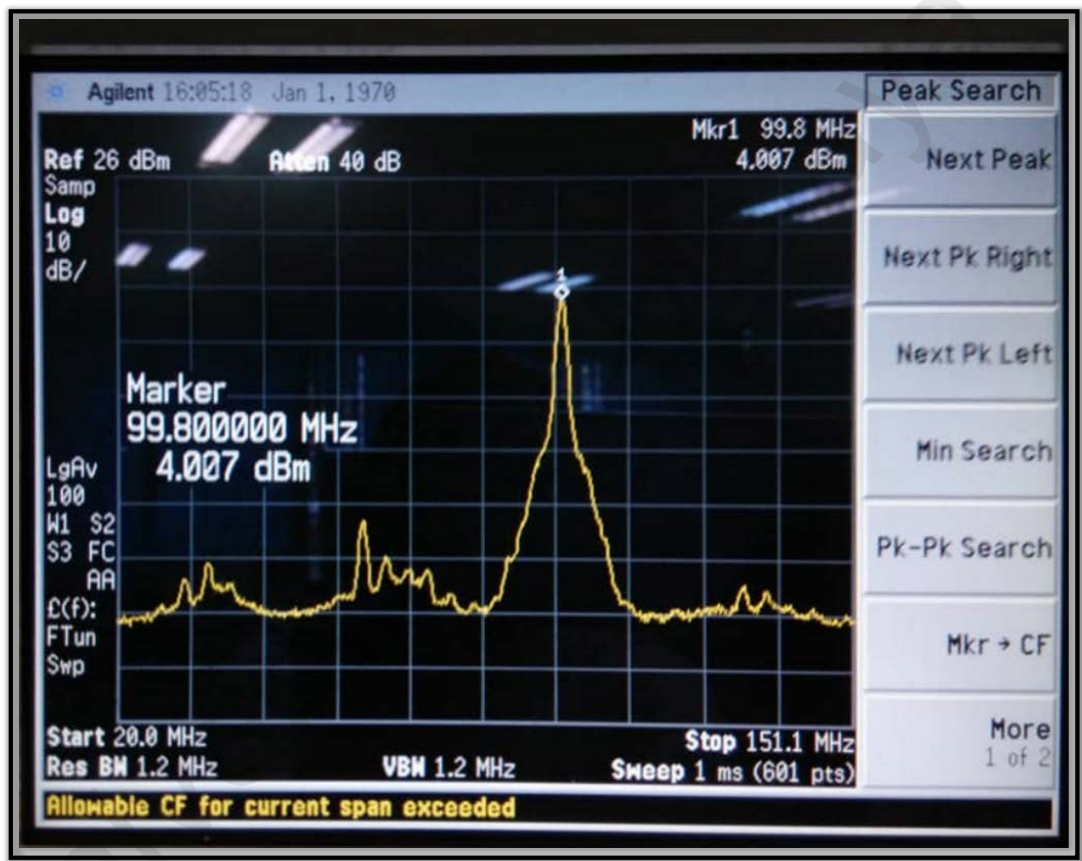
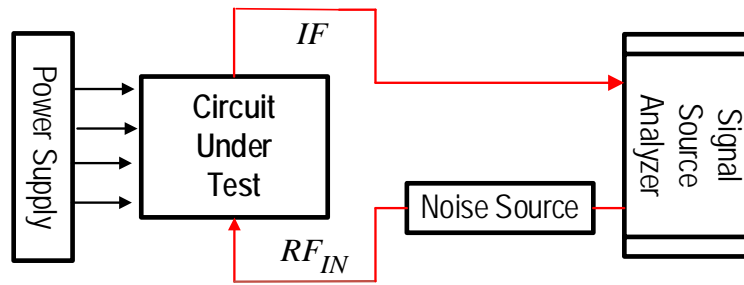


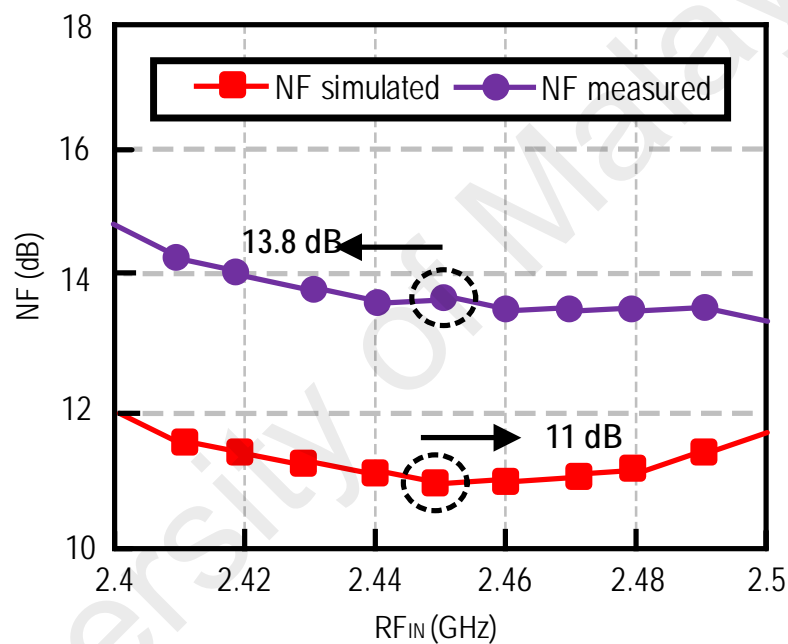
Figure 4.5: Measured data of conversion gain from spectrum analyzer

#### 4.1.2 Noise Figure (NF)

The measurement setup used to characterize the noise figure of the proposed design is illustrated in Figure 4.6. The input port of the NFA is connected to the input of the proposed design via a noise source N4002A, where else the IF output is connected to the



**Figure 4.6: Test setup for NF measurement**

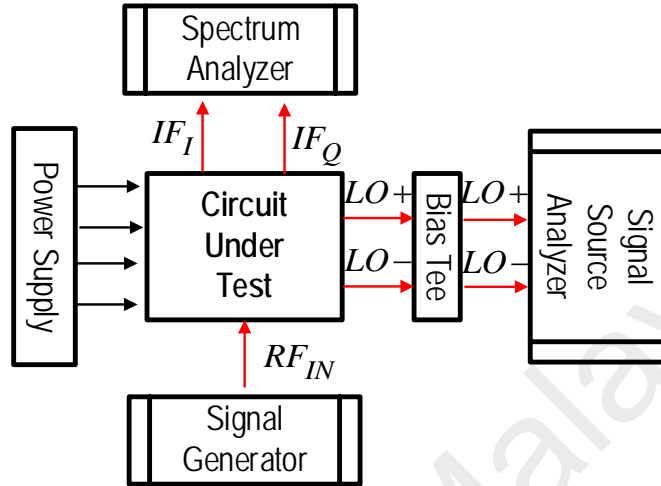


**Figure 4.7: Post layout simulation and measurement results of NF**

output port of the NFA to capture the noise performance. The NF acquired for all BLE/ZigBee channels are illustrated in the Figure 4.7 and is around 13.8dB at 100MHz. The discrepancy between simulation and measured results is about 3 dB which might be due to signal loss, extra parasitic from connectors cable and PVT.

### 4.1.3 Linearity

The measurement setup used to characterize the linearity performance of the proposed design is illustrated in the figure below.



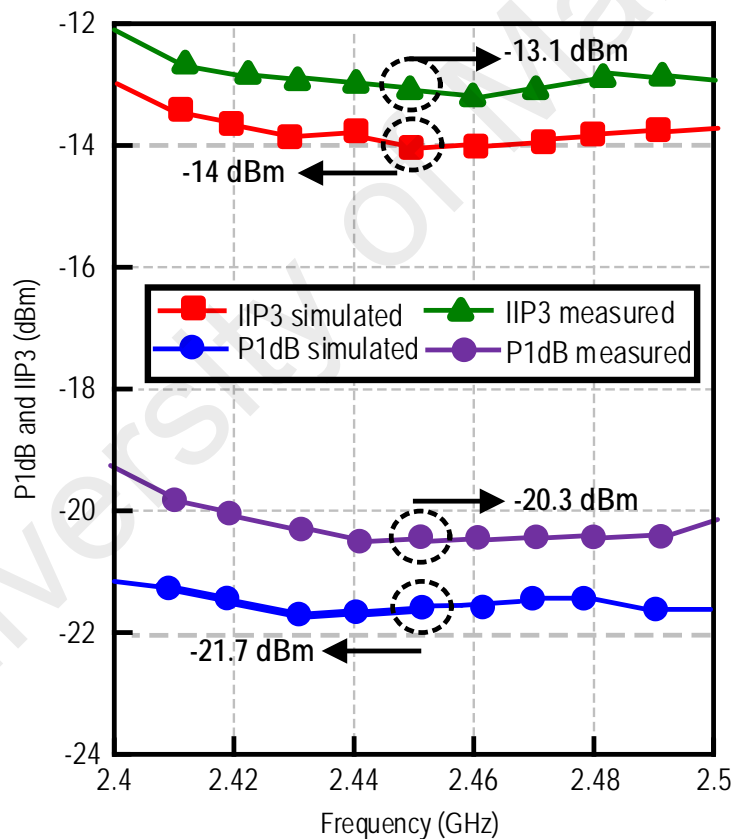
**Figure 4.8: Test setup for P1dB and IIP3 measurement**

The signal generator generates the RF input signal and feeds it into the input of the proposed design. The receiver is powered on by a  $V_{DD}$  of 1.5V supplied by the power supply and it generates quadrature balanced IF outputs. This I and Q outputs are then fed into the spectrum analyzer to measure the conversion gain. To measure the P1dB, the RF input power is swept from -30 dBm to 0 dBm. This is done for all BLE and ZigBee frequencies. The distortion due to higher order components nonlinearity can be observed as the input signal power is increased. The P1dB measured is around -20.3 dBm as shown in Figure 4.9. The discrepancy between simulation and measured results is about 1.5 dBm which might be due to signal loss and PVT.

For the IIP3 measurement, the same setup as shown in Figure 4.8 is used. The two tone test was performed to measure the input third order intermodulation point of the proposed design. The two tone feature of the signal generator is utilized. When this



feature is activated, the signal generator generates two RF input signal and combines both the signal using a built in power combiner. This combined signal is then fed into the input port of the proposed design and the IF output is measured in the spectrum analyzer. The first signal is set to the fundamental carrier BLE/ZigBee frequency and the second signal is set at 100 kHz offset from the first signal frequency. 100 KHz offset is chosen to meet the most stringent requirement for worst case scenarios in BLE and ZigBee applications (Pipino et al., 2015) . This process is repeated for all BLE/ZigBee channels. The measurement result of IIP3 is indicated around -13.1 dBm as shown in Figure 4.9. The P1dB and IIP3 results are within the BLE/ZigBee standard requirements for all channels.



**Figure 4.9: Post layout simulation and measurement results of P1dB and IIP3**

#### 4.1.4 Input Return Loss

The measurement setup used to characterize the input impedance matching of the proposed design is illustrated in the Figure 4.10. To measure the input impedance of the chip, the input port of the proposed design is directly connected to the VNA and the input reflection coefficient is obtained. The  $S_{11}$  acquired for all BLE/ZigBee channels are

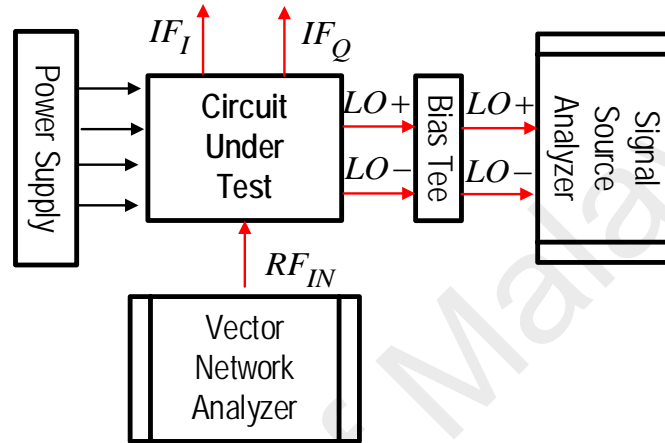


Figure 4.10: Test setup for  $S_{11}$  measurement

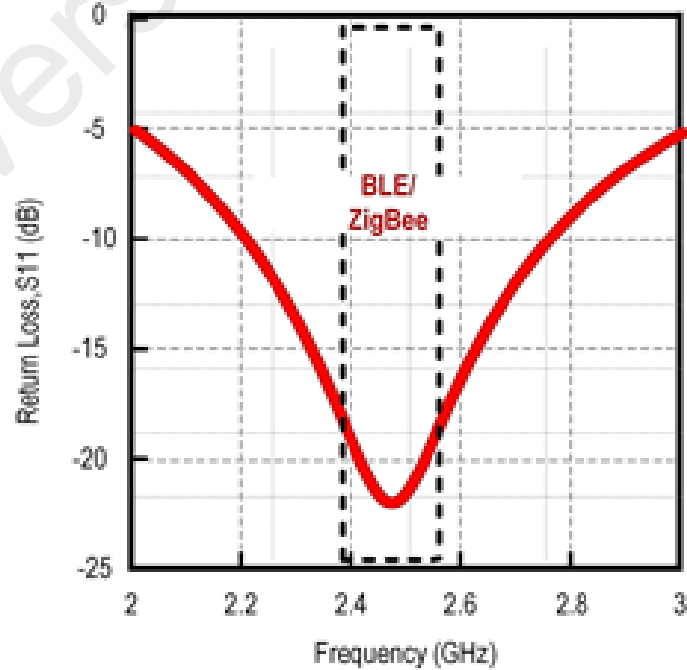


Figure 4.11: Measured input return loss

below -15 dB as shown in Figure 4.11, which shows good impedance match and maximum power transfer from source to load.

#### 4.1.5 VCO Tuning Range and Phase Noise

The measurement set used to characterize the VCO performance of the proposed design is illustrated in the Figure 4.12 below. To tune and capture the VCO performance such as phase noise, power of signal and oscillating frequency range, the VCO's output is connected to a signal source analyzer via a bias tee. VCO phase noise is susceptible to the DC supply noise, hence this bias tee acts as a filter and also powers up the open drain buffer only during VCO characterization and tuning. The signal source analyzer monitors the oscillating frequency, the power of the signal and the phase noise performance for that particular frequency. The VCO is used to tune to other channels of the BLE/ZigBee band and down convert it to 100MHz IF frequency. The tuning is done by a tuning voltage dedicated for VCO tuning. This voltage is tuned from 0V to the max of supply voltage which is 1.5V. Based on Figure 4.13, the measured tuning frequency is from 2.3GHz-2.4GHz which is sufficient to downconvert all the BLE and ZigBee channels to the desired IF frequency giving a tuning range of 8.3%. The power of the oscillation signal is around -2.5dB while the measured phase noise performance at 2.5MHz offset of center frequency of 2.4GHz is around -118.5dBc/Hz as illustrated in Figure 4.14. The good

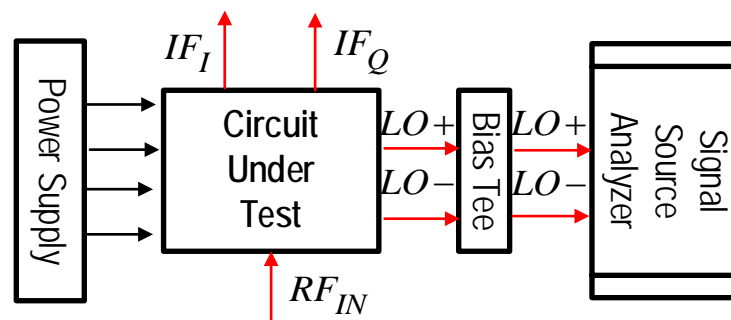


Figure 4.12: Test setup for VCO parameters measurement

performance of the VCO results from the LC filter used in the VCO-mixer interface. This filter attenuates the spurious harmonics generated by the non-linear active devices. The

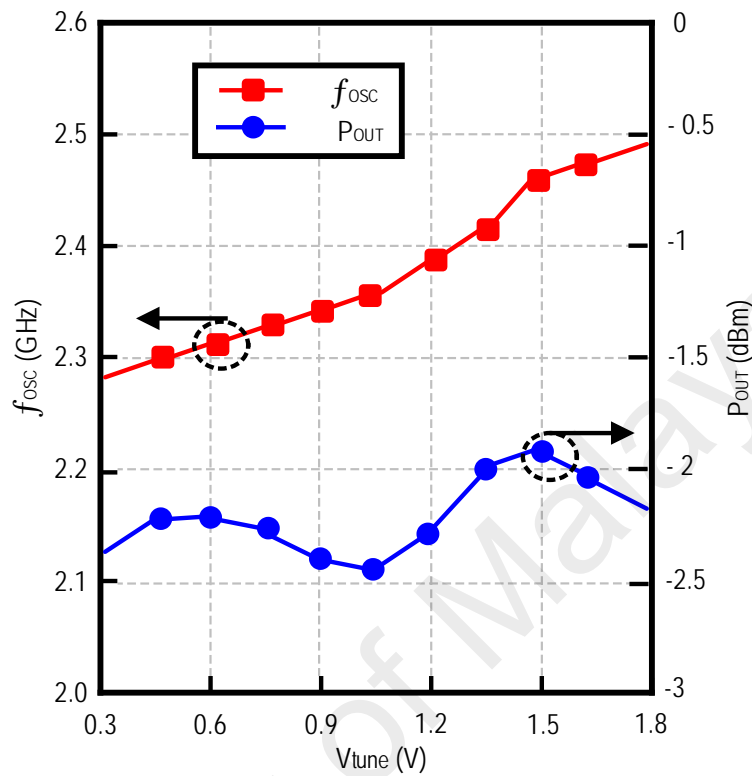


Figure 4.13: Measured tuning frequency of VCO and the output signal power

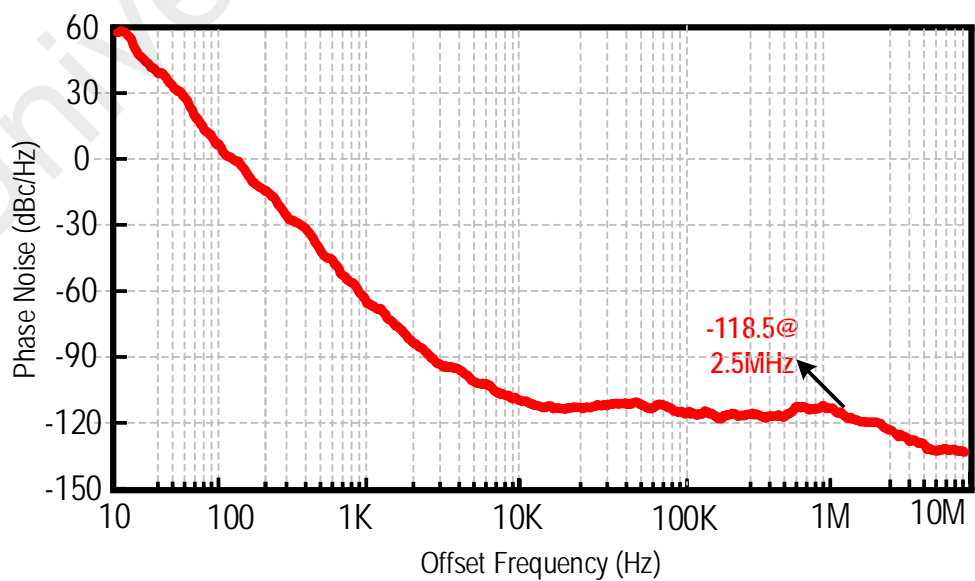
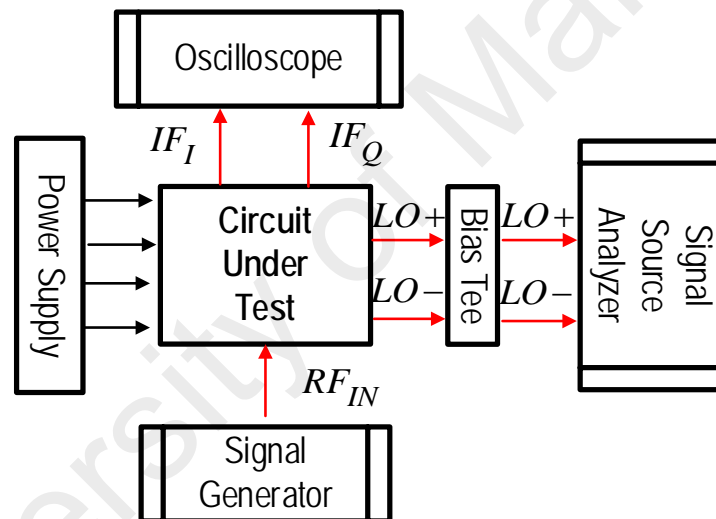


Figure 4.14: Measured phase noise at 2.5MHz offset of 2.4GHz

small, signal power deviation along the 2.4GHz band is due to the parasitics changing with frequency along with signal loss and PVT. This is due to the transfer function of the block consisting of mainly capacitance and inductance, whose impedance varies with frequency. The phase noise discrepancy between simulation and measured results is about 8 dBc/Hz. This may be due to cable and connector losses and PVT.

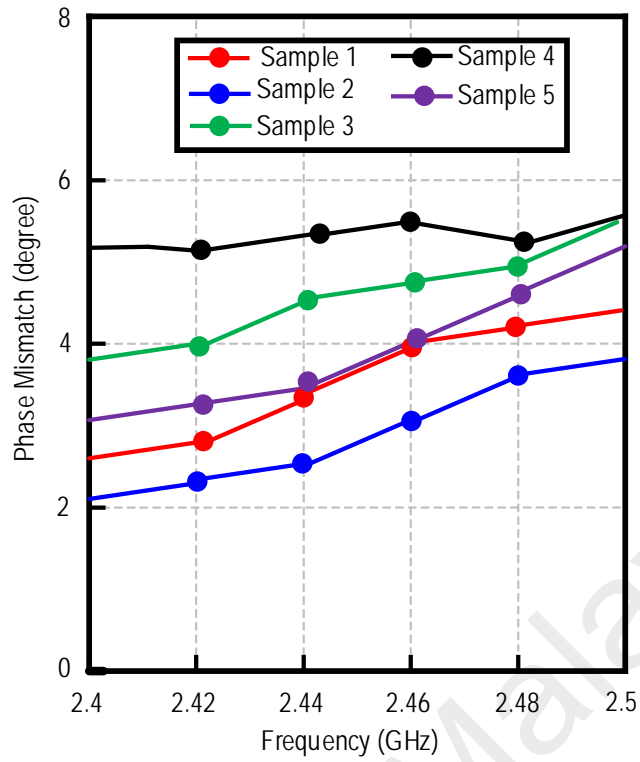
#### 4.1.6 Amplitude and Phase Mismatch

The measurement set used to characterize the I and Q signals of the IF output of the proposed design is illustrated in the figure below.

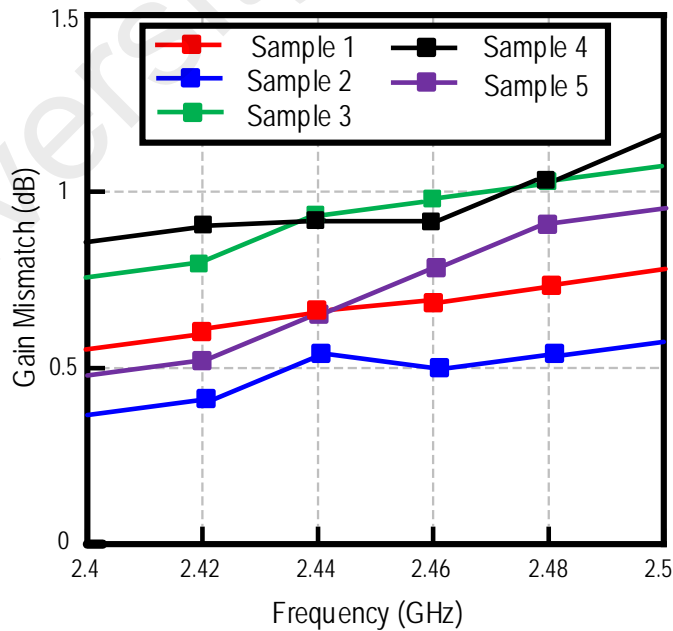


**Figure 4.15: Test setup for the  $IF_I$  and  $IF_Q$  amplitude and phase mismatches measurement**

The signal generator generates the RF input signal and feeds it into the input of the proposed design. The receiver generates quadrature balanced IF outputs. The I and Q balanced outputs are connected to the 2 channel oscilloscope to observe the output in the time domain. Hence the amplitude and phase mismatch of the I and Q signal output can be observed as shown in the Figure 4.16 and 4.17. Multiple measurement results for five different chips were taken to observe the mismatches due to process variation. The worst



**Figure 4.16: Measurement results for 5 samples of phase mismatch at output against input frequency**



**Figure 4.17: Measurement results for 5 samples of gain mismatch at output against input frequency**

I/Q gain and phase mismatch across five samples at 100 MHz output are 1.2 dB and 6°, respectively. The discrepancy between simulation and measured results for gain mismatch is around 1dB and the phase mismatch is around 5°. The mismatch are caused by frequency dependent parasitic from device modelling, and measurement instruments. This parasitic also causes deviation in the 2.4GHz channel bandwidth.

The aim of this design is to make the proposed receiver compatible to be powered by a 1.5V standard commercial coin size cell battery, hence eliminating the need of LDO. However, in reality the coin battery voltage gradually diminishes with the use time. Accounting this, the proposed design is also measured for a lower supply voltages. Based on measurement results, the proposed receiver can operate for  $V_{DD}$  as low as 1.2 V with respectable performance. Table 4.1 tabulates the performance summary of the proposed design (at 2.45GHz input RF signal) for 1.2 V and 1.5 V supply voltage headroom. Each measurement results are taken at the centre of the 2.4GHz band at 2.45GHz. Comparison with other works are tabulated in Table 4.2. Direct comparison with other designs are difficult given the varying technologies used and different level of integration with functionality. Nevertheless, it can still be observed that the proposed receiver is comparable to the recent arts. The proposed receiver, fabricated on an 180nm low cost CMOS technology draws only 2mA current from a 1.5V supply voltage. By using the benefit of cascade and cascode while merging three individual blocks into one single

**Table 4.1: Performance summary of the proposed design for 1.2 V and 1.5 V**

VDD (V)	<b>1.2</b>	<b>1.5</b>
RFin (GHz)	<b>2.4-2.5</b>	<b>2.4-2.5</b>
Tuning Range (%)	<b>6.9</b>	<b>8.3</b>
PN (dBc/Hz) @ offset	<b>-111.2</b> <b>@2.5MHz</b>	<b>-118.5</b> <b>@2.5MHz</b>
P1dB (dBm)	<b>-29.3</b>	<b>-21.5</b>
IIP3 (dBm)	<b>-21.8</b>	<b>-14</b>
NF (dB)	<b>16.2</b>	<b>13.8</b>
CG (dB)	<b>18.7</b>	<b>24</b>

block, the proposed receiver offers a CG of 24 dB, NF of 13.8 dB, IIP3 of -10.8dBm and P1dB of -21.5dBm. By utilizing the complementary VCO topology, the proposed receiver also gives a phase noise of -118.5dBc/Hz with a tuning range of 8.5% sufficient to convert all BLE and ZigBee channels to the desired 100MHz IF. In (Chong et al., 2014), the NF is low at around 7.2 dB due to the exclusion of VCO which normally

**Table 4.2: Performance comparison with other reported works**

Ref.	This Work	(Chong et al., 2014)	(Selvakumar et al., 2015)	(Lin et al., 2014b)	(Lin et al., 2014)	(Javadi et al., 2013)
RF input (GHz)	<b>2.4-2.5</b>	2.4	2.4	2.25-3.55	2.4	2.4
Application	<b>BLE/ ZigBee</b>	ZigBee	BLE	ZigBee	ZigBee/ WPAN	WSN
VDD (V)	<b>1.5</b>	0.5	0.8	0.6/1.2	0.6/1.2	1.2
Tuning Range (%)	<b>8.3</b>	-	20	-	21	-
PN(dBc/Hz)@ offset	<b>-118.5 @ 2.5MHz</b>	-	-109.5 @ 2.5MHz	-115.5 @ 3.5MHz	-111.5 @ 3.5MHz	-117 @ 1MHz
P1dB (dBm)	<b>-21.5</b>	-22.3	-	-	-	-5
IIP3 (dBm)	<b>-14</b>	-10.8	-15.8	-6	-7	-7
NF (dB)	<b>13.8</b>	7.2	15.1	9	8.8	4.7
CG (dB)	<b>24</b>	22.3	55 *	55 *	32	30
IDC (mA)	<b>2</b>	1.8	0.8	1@0.6V + 0.22@1.2 V	1.2@0.6V + 0.53@1.2 V	0.8 #
External Matching	<b>no</b>	no	lind + lcap	no	no	no
Require LDO	<b>no</b>	yes	yes	yes	yes	yes
BB Method	<b>with I/Q</b>	no I/Q	With I/Q	With I/Q	With I/Q	With I/Q
CMOS technology	<b>180nm</b>	130nm	130nm	65nm	65nm	180nm
Sub-Blocks	<b>QLNA+ IQ Mixer +VCO +TIA</b>	LNA + Mixer	LMV+ TIA+ Complex filter	Blixer+ Hybrid filter+ PPF	LNTA+ Passive mixer +TIA +VCO	LNA+ passive mixer+ QVCO

\*Include IF post amplification #simulation



degrades the overall noise performance due to phase noise. Otherwise, in (Javadi et al., 2013), a low NF is achieved with low power dissipation, but this is only simulation results, and the design was never fabricated. In (Selvakumar et al., 2015) and (Lin et al., 2014b), very high conversion gain is achieved because of the inclusion of baseband stage using active filters which offers high baseband amplification. Furthermore, in (Selvakumar et al., 2015), the low current drawn by the low supply is assisted by the external matching components used. Likewise, (Lin et al., 2014b) and (Lin et al., 2014) utilized the low transit frequency that newer technologies offer, to obtain good performance with lower power consumption. The drawback is the high cost associated with the newer technologies which should be more suited for very high frequency operation. Overall, the proposed receiver gives comparable performance with recent state of the art designs. New circuit techniques were used to implement lower supply voltage and current for low power operation. The reduced number of passives used had helped in cutting the design area and therefore, the cost. Further cost reduction is achieved as the design was implemented using a matured technology, as opposed to newer and costlier technologies.

## CHAPTER 5: CONCLUSION

### 5.1 Summary and Conclusion

This dissertation presents an alternative way of integrating the LNA, I/Q Mixers, VCO and TIA's into one unified cell, thus enabling current reuse between blocks. The proposed BLE/ZigBee compliant receiver is designed using CMOS technology. It was simulated, fabricated and then characterized to compare with recent state of the art works.

To lessen the power consumption, the supply voltage or the current drawn by the supply needs to be decreased. The supply voltage is set to 1.5 V to allow the system to be directly powered by a coin battery, thus doing away with the need of an LDO. To ensure that the battery can last for an extended time, the current drawn by the battery need to be minimized. By effectively merging the quadrature low noise amplifier (QLNA), in phase and quadrature (I/Q) mixers, voltage controlled oscillator (VCO) and trans-impedance amplifier (TIA) in one cell, while putting off the LDO, the available 1.5-V voltage supply is fully utilized for current-reuse between blocks, minimizing the direct current (DC) current consumption of the complete system. The proposed receiver only consumed 2mA of current.

By reducing the use of resonant passive element especially inductor, the active area of the silicon chip was optimized, thus reducing cost. By taking advantage of the lenient overall performance requirements of WPAN standards, the inductor count in the proposed design has been decreased, sacrificing overall performance for cost. Moreover, quadrature generation is generated in the RF path in contrary to the conventional method of quadrature local oscillator (LO) path using quadrature voltage controlled oscillator (QVCO) or frequency dividers. This approach in addition reduces the inductor count in the full system design. To further reduce cost, a lower node CMOS technology is chosen,

180nm which offers sufficient speed and performance for BLE/ZigBee compliant receiver.

A fully integrated solution is adapted, in which the bulky external components are eliminated. A low IF receiver architecture is selected with an intermediate frequency (IF) of 100MHz, which offers the best optimized performance for the RF and baseband blocks in the complete system, alleviating the need of of the bulky and lossy Surface Acoustic Wave (SAW) filter together with the image reject filters. The proposed receiver was implemented in a combination of cascode and cascade topology, capitalizing in their respective advantages. It is headed by a novel single-ended quadrature LNA, which enables simultaneous input impedance matching and I/Q generation in the RF path without any external components, thus avoiding the bulky QVCO and power hungry voltage dividers. This QLNA is then cascaded to an active single balanced IQ mixer which shares its bias current with a cascoded complementary VCO through current reuse principal. The transconductance stage of I/Q mixers act as amplifier and also set the bias current of the VCO through device reuse principal. The TIA acts as the load of the active mixer, thanks to the LC filter inserted between VCO and mixer interface completes the design with a high IF voltage gain and filtering. Forward body biasing technique was adapted to reduce the supply voltage down to 1.5V. Measurement shows that the prototyped receiver still achieves a comparable performance with the recent state of the art architectures, exhibiting a CG of 24 dB, a NF of 13.8 dB and a IIP3 of -14 dBm. The phase noise of the VCO is -118.5 dBc/Hz at 2.5 MHz off-set while consuming just 2mA from a 1.5 V supply, directly being compatible with the commercial coin-sized battery. As the coin battery voltage gradually decreases with the usage time, the proposed receiver can operate for  $V_{DD}$  as low as 1.2 V with respectable performance making it deem favorable for WPAN applications like BLE and ZigBee. The low-cost technology and complete integration permits the full system to accommodate the SoC concept

subsequently reducing size and cost, while the low current consumption renders the receiver suitable for IoT devices using the BLE or ZigBee standards.

## **5.2 Future Works**

The way forward should encourage the integration of complex filter in the mixer-TIA interface reusing the same bias current to complete the front end low IF receiver. The complex filtering profile could be achieved by using the parasitic capacitance of the MOS with extra additional components added.

To maintain the performance even when the coin battery voltage diminishes with usage, additional compensation schemes could be integrated to attain full battery capacity usage. This schemes could be done by having feedback systems which automatically will adjust the performance, when the voltage of the supply reduces.

The QLNA gain could also be increased using gain boosting topologies, so that passive mixers could be utilized to improve linearity performance of the overall receiver.

Inductors consume the most active area in the chip. An inductorless receiver could be designed which will reduce chip size. This will further decrease the cost of fabrication of the overall chip and the small size will increase portability.

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## LIST OF PUBLICATIONS AND PAPERS PRESENTED

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