TRAP-ASSISTED TUNNELING MECHANISM OF ZIRCONIUM OXYNITRIDE (ZRON) THIN FILM ON SILICON CARBIDE

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ABSTRACT

This research is a study on the possibilities of trap-assisted tunneling conduction mechanism in Zirconium Oxynitride (ZrON) after Zirconium (Zr) with thickness 5nm was sputtered on Silicon Carbide (SiC) substrate which then underwent simultaneous nitridation and oxidation in Nitrous Oxide (N_2O) for 15 minutes in 4 different ambient temperatures of 400°C, 500°C, 700°C, 900°C. Electrical properties of the samples were then characterized by fabricating Al-gate MOS capacitors onto the film surface. Of all 4 samples, sample that was oxidized/nitrided at 500°C demonstrated to have the highest dielectric breakdown (E_B) of 5.05 MV/cm and lowest E_B was by sample that was oxidized/nitrided at 900°C. The 1st step breakdown in *J-E* curve by samples oxidized/nitrided at 500°C, 700°C and 900°C were minor but there were also 2nd step breakdown and this explains that those samples could be a trap assisted tunneling (TAT) conduction mechanism. From graph of ln (*JE)* vs 1/*E*, the intercept and slope from the regression line have given the value for lowest trap density and highest trap energy at -35.8 x 10^{21} cm^{-3} and 5.92eV, respectively.

Keywords: Thin film, Trap Density, Trap Energy, Dielectric.

MEKANISME PERANGKAP TEROWONG TERBANTU OLEH FILEM NIPIS ZIRKONIUM OXYNITRIDA PADA KARBIDA SILIKON

ABSTRAK

Penyelidikan ini adalah kajian mengenai kemungkinan mekanisme perangkap terowong terbantu dalam Zirkonium Oxynitrida (ZrON) setelah Zirkonium (Zr) dengan ketebalan 5nm disalurkan pada substratum Karbida Silikon yang kemudian mengalami nitridasi dan oksidasi serentak dalam Oxsida Nitrat selama 15 minit dalam 4 suhu persekitaran yang berbeza iaitu 400°C, 500°C, 700ºC, 900°C. Sifat elektrik sampel kemudian dicirikan dengan membuat kapasitor semikonduktor logam-oksida dengan saluran gerbang aluminium ke permukaan filem. Dari semua 4 sampel, sampel yang dioksida/dinitrida pada 500°C terbukti mempunyai pecahan dielektrik tertinggi sebanyak 5.05 MV/cm dan pecahan dielektrik terendah adalah dari sampel yang dioksida/dinitrida pada 900°C. Pecahan langkah pertama yang kecil dalam lengkungan *JE* berlaku pada sampel yang dioksida/dinitrida pada 500°C, 700°C dan 900°C tetapi terdapat juga pemecahan langkah kedua dan ini mungkin menjelaskan bahawa sampel tersebut mungkin merupakan mekanisme perangkap terowong terbantu. Dari graf ln (*JE*) dan 1/*E*, pintasan dan cerun dari garis regresi telah memberikan nilai untuk ketumpatan perangkap terendah dan tenaga perangkap tertinggi masing-masing pada $-35.8 \times 10^{21} cm^{-3}$ dan 5.92eV.

Kata kunci: Filem nipis, Ketumpatan Perangkap, Tenaga Perangkap, Dielektrik.

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And last but not least, my sincere thanks to my course mates who have provided continuous motivation throughout completion this project.

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LIST OF SYMBOLS AND ABBREVIATIONS

Al	: Aluminium
Ar	: Argon
E_{BR}	: Electric breakdown
E_c	: Conduction Band
E_f	: Fermi level
E_v	: Valence Band
FN	: Fowler-Nordheim
HF	: Hydrofluoric
HfO_2	: Hafnium Dioxide
La_2O_3	: Lanthanum oxide
MIS	: Metal Insulated Semiconductor
MOS	: Metal Oxide Semiconductor
MOSFET	: Metal Oxide Semiconductor Field Effect Transistor
N_2O	: Nitrous Oxide
PF	: Poole Frenkel
RCA	: Radio Corporation of America
Si	: Silicon
SiC	: Silicon Carbide
SILC	: Stress Induced Leakage Current
SiO_2	: Silicon Dioxide
Ta_2O_5	: Tantalum Pentoxide
TAT	: Trap Assisted Tunneling
TFT	: Thin Film Transistor
TiO_2	: Titanium Dioxide
V_g	: Gate Voltage
Zr	: Zirconium
ZrO_2	: Zirconium Dioxide
ZrON	: Zirconium Oxynitride

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Graphs plotted in Sigma Plot Software

Raw data calculation in Microsoft Excel

CHAPTER 1: INTRODUCTION

1.1 Background Study

Electronic devices with high reliability, longer lifespan, and suits for high temperature application are highly demanded these days by industries such as manufacturing, nuclear, aerospace, automotive and power plants. This is mainly because of how fast the world is moving towards digitalization, storing every data and information, working in a fast pace with higher productivity and good accuracy. A microelectronic device in this era is considered good if its MOS structure is made of materials that can withstand high voltage and not break down easily. Substrate of a MOS structure plays an important role too as it must be a good semiconductor, where it can conduct electricity and act as an insulator, depending on the application. One of the most promising material that is used as substrate till date is Silicon (Si), for its unique properties of being able to balance itself as a semiconductor. And over the years, Silicon Carbide (SiC) slowly took over Si for its advantage on having good electrical and thermal properties. As for the gate oxide, or in other word known as dielectric, needs to be made of material that will be able to prevent charges flow from gate to source drain channel as this could lead to failure of device in long run, it acts as an insulator between gate metal and substrate. Researches have been working onto this thin film properties to ensure its thickness will be suitable to be used for microelectronic devices without jeopardizing its properties.

1.2 Problem Statement

Due to the ongoing trend of using smaller electronic device (Atherton, 1984), the semiconductor industry had to work on several directions to be able to follow the trend and keep up with the market demand by focusing on to downscaling circuit elements, increasing production/operation speed, reducing power consumption by the electronic devices and also devices with good tolerance temperature range (Yew Hoong Wong K. Y., 2012).

One of the expectation from the extreme miniaturization of electronic components such as the metal-oxide-semiconductor (MOS) device is to pack more transistors in a chip and that simply means there will be reduction in the oxide layer in MOS structure, and downscaling them without causing any damage to its electrical design will be an important measure (Yew Hoong Wong K. , 2011). Even though there is an advantage from the directional proportional relationship between threshold voltage and oxide layer thickness, where the thinner the thickness of oxide layer, the lower the threshold voltage (Jung-Chuan Fan, 2016), however, there are number of problems arise due to reduction in oxide layer thickness, and amongst many, tunneling leakage current that increases exponentially is the most critical (Kian Heng Goh Y. A., 2016) through the source/drain and substrate and attributing to tunneling assisted by traps in the interfacial layer between semiconductor and oxide (Jung-Chuan Fan, 2016).

To attend to this problem, researches have tested to scale down the most used gate oxide layer, which is the silicon dioxide (SiO2). From the study and research, it was found when the oxide thickness gets lower than 1.2nm, there is possibility of a huge leakage current due to tunneling of carriers.

Therefore, to overcome this challenge, alternative gate oxides with higher K were studied. There are many alternative gate oxides such as Hafnium Dioxide (HfO_2), Lanthanum oxide (La_2O_3), Titanium Dioxide (TiO_2), Tantalum Pentoxide (Ta_2O_5), Yttrium (III) (Kian Heng Goh Y. A., 2016) but most of them have got stability issue (C.H. Chen, 2002). From recent study, Zirconium Dioxide (ZrO_2) has proven to be one a suitable gate oxide due to the high dielectric constant, k value of (22-25) but it had its own drawback as it came along with interfacial layer (IL) that is undesirable. It was then found, that by incorporating nitrogen into the film of ZrO_2, it can eliminate IL and at the same time improving electrical properties of the film itself. Therefore, in a Nitrogen Dioxide (N_2O) ambient, sputtered Zr was transformed into ZrO_2 and then to ZrON via simultaneous oxidation and nitridation technique and that is how ZrON thin film has formed (Yew Hoong Wong K. , 2013). From many studies, ZrON that was oxidized/nitrided at 500°C has been discussed that may be a reliable and suitable gate oxide as it has fulfilled many of the parameters such as high breakdown field, low interface trap, high barrier height and etc (Kuan Yew Cheong, 2012).

When a large electric field is applied onto the dielectric, there will be a conduction current flowing through the film. Of many conduction mechanisms, this research aims to study if trap-assisted tunneling conduction will be a possible conduction.

1.3 Project Objectives

(i) To determine the possibility for trap-assisted tunneling mechanism to exist in the oxynitride material when oxidized/nitrided in different temperatures.

(ii) To compute the trap energy and trap density in the oxynitride material in trap-assisted tunneling mechanisms.

1.4 Scope Of Study

In this study, Zirconium (Zr) was used as a thin film to be sputtered on Silicon Carbide (SiC substrate). Under Ar ambient of 4 different temperatures the thin film underwent simultaneous oxidation and nitridation in Nitrous Oxide to obtain a layer of ZrON as an oxide layer. Using electrical properties that were obtained in the form of raw data, graphs were plotted using SigmaPlot to further study.

CHAPTER 2: LITERATURE REVIEW

2.1 Silicon Carbide (SiC) as an Alternative Substrate For Si

SiC has band gap that is diverse due its 200 crystalline forms, some of the common ones with its respective band gap energy are as below (Madelung, 2004);

- 3C (2.20 eV)
- 6H (3.02 eV)
- 4H (3.20 eV)

These band gap energies are considered high and more suitable than Si that has a band gap energy of 1.12 eV (T. Sahu, 2012). Band gap energy simply means the differences between conduction band at bottom (E_c) and valence band that is at the top (E_v) and it is the minimum energy needed to excite an electron to participate in a conduction state. When thermally oxidized, it can turn into a suitable material to be used in metal oxide semiconductor structure (Sanjeev Kumar, 2012).

(S. Charpentier, 1999) and (M. Makowska-Janusik, 2005) have stated due to Silicon Carbide's ability to adopt different types of crystalline polytypes, which can monitor band gap along with other electronic properties, it will well suit for the use high performance optical devices and electronic devices.

2.2 Gate Dielectrics

A good gate dielectric has below characteristics (Salvador Duenas, 2012)

- High-k value as it provides high gate capacitance
- Moderated thickness layers
- High bandgap energy. The larger the bandgap energy, the larger the conduction. But leakage current due to insufficient barrier height at interface will be observed when the range is 5-6eV.
- An adequate barrier height and band offset with SiC to reduce the carrier chare injection into the band (Sanjeev Kumar, 2012)
- Smaller leakage currents
- High breakdown fields

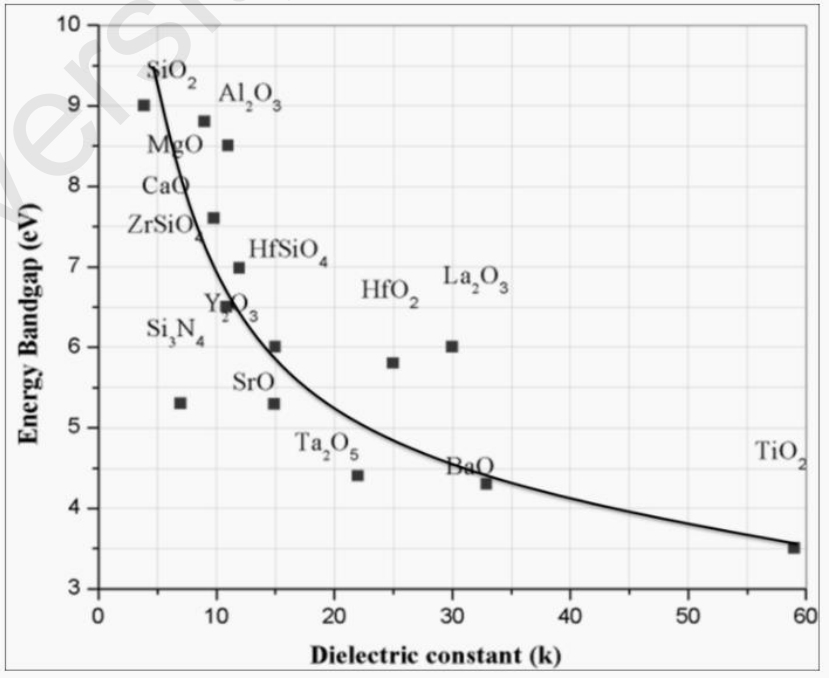


Figure 2.1 Various dielectric materials (eV vs k) (Sanjeev Kumar, 2012)

2.3 Dielectric Breakdown Field

With good dielectric strength, and capability of sustaining high electric field can help prevent device breakdown. The maximum limit of electric field that a dielectric can withstand under the supply of high voltage is called the dielectric breakdown, E_{BR}. It can be defined using the below formula (Sanjeev Kumar, 2012).

$$E_{BR} = \frac{V_{BR}}{d}$$

- V_{BR} = Breakdown voltage
- d = dielectric thickness

A simple example would be if let's say the silicon dioxide's dielectric breakdown is $6x10^6$ V/cm, and the dielectric thickness is 60nm, then the breakdown voltage will be 36V. Calculation as below

$V_{BR} = E_{BR} \times d$

$= 6x10^6$ V/cm x $60x10^{-7}$ cm

= 36 V

This means, when 36 V of gate voltage is applied onto the dielectric, it can breakdown and conduct current. To avoid this, a safety factor will normally be applied, for instance, in this same case, if a safety factor of 3 is applied, then whenever this MOSFET is operated, the gate voltage applied onto the oxide/dielectric shall not exceed 12V.

2.4 Factors Affecting Dielectric Constant

Research by (Cheong, 2012) states that there are several factors that can affect dielectric constant, they are as below

i. Type of substrate
ii. Material of substrate
iii. Oxide deposition method
iv. Oxide-substrate interface characteristics.

This is because two researches were conducted using same oxide and substrate which are ZrO_2 and Si respectively but obtained two different dielectric constant ranges. (Weifeng Li, 2007) obtained dielectric constant between 7.5 – 55.0 whereas (Kuan Yew Cheong, 2012) obtained between 10.58 – 21.82. These differences are due to the factors stated above.

2.5 Conduction Mechanisms

Properties of dielectric such as list below affects performance of MOS devices (Salvador Duenas, 2012);

i. Film composition
ii. Film processing
iii. Film thickness
iv. Energy levels/trap energy
v. Densities of trap/trap density

When there is an electric field, dielectric materials do not conduct current (Sanjeev Kumar, 2012). From the study conducted by (Chiu, 2014), it was stated that the electrons in a dielectric are tightly bonded, has low conductivity and band gap of 3eV to 5eV. A noticeable conduction current through the dielectric film will be noticed when a huge electric field is applied and they are known as electrode, bulk, and tunnel limited conduction mechanism (Salvador Duenas, 2012). Each conduction mechanism has its own types, and each have got different energy band gap and other ways of penetrating through the oxide layer.

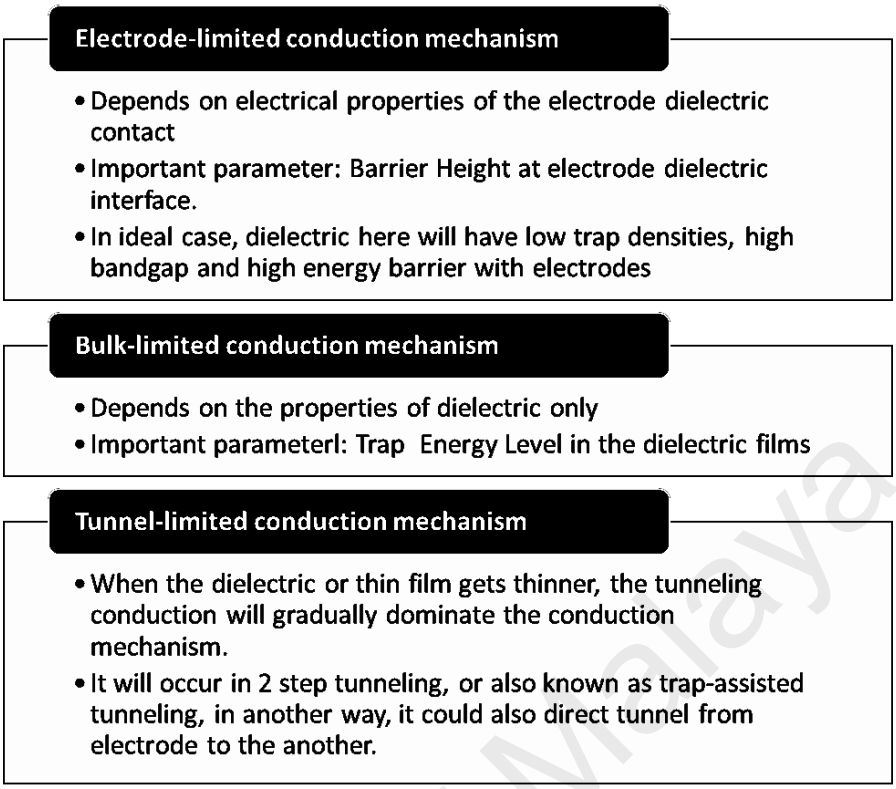


Figure 2.2 Three main types of conduction mechanisms (Chiu, 2014)

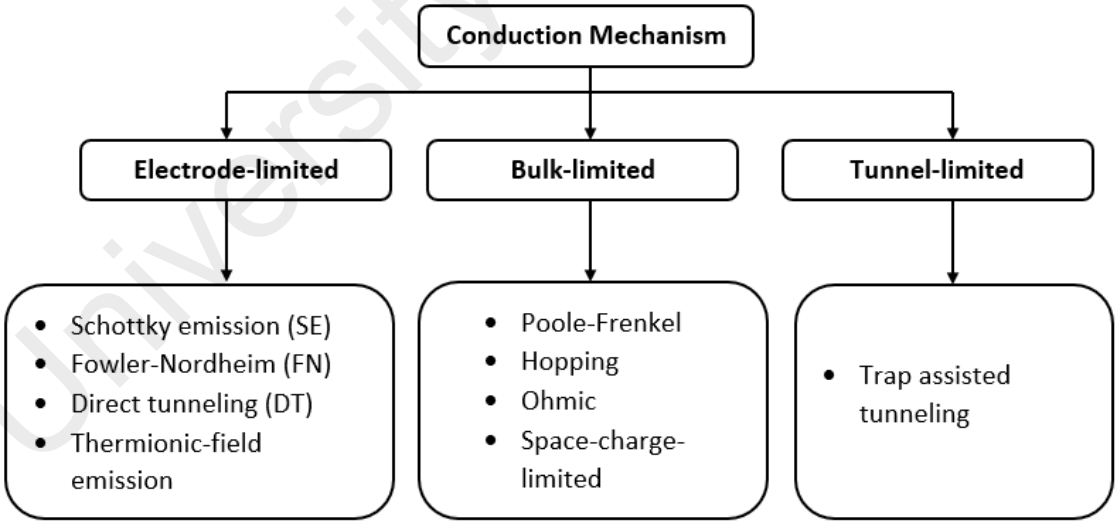


Figure 2.3 Types of basic conduction mechanisms in dielectric films (Chiu, 2014)

2.5.1 Energy band diagram of different conduction mechanism

Describes about movement of electrons in the metal, oxide, and semiconductor structure. Involves key energy bands known as valence band (E_v) and conduction band (E_c), and fermi level (E_f).

2.5.1.1 Schottky Emission

The electrons in metal will be able to overcome energy barrier if the electrons obtained enough thermal activation.

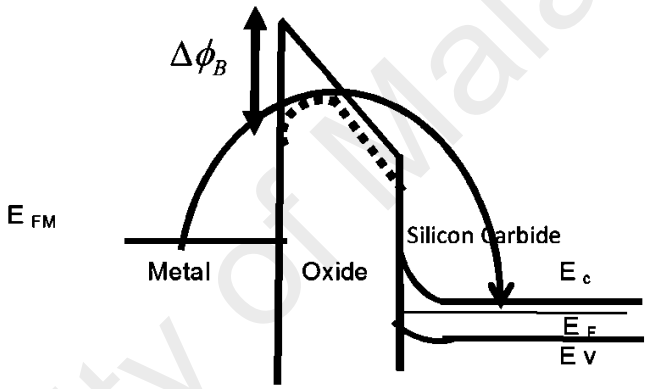


Figure 2.4 Schottky emission energy band diagram (Sanjeev Kumar, 2012)

2.5.1.2 Fowler-Nordheim Tunneling

It tunnels through triangular barrier into conduction band of the insulator

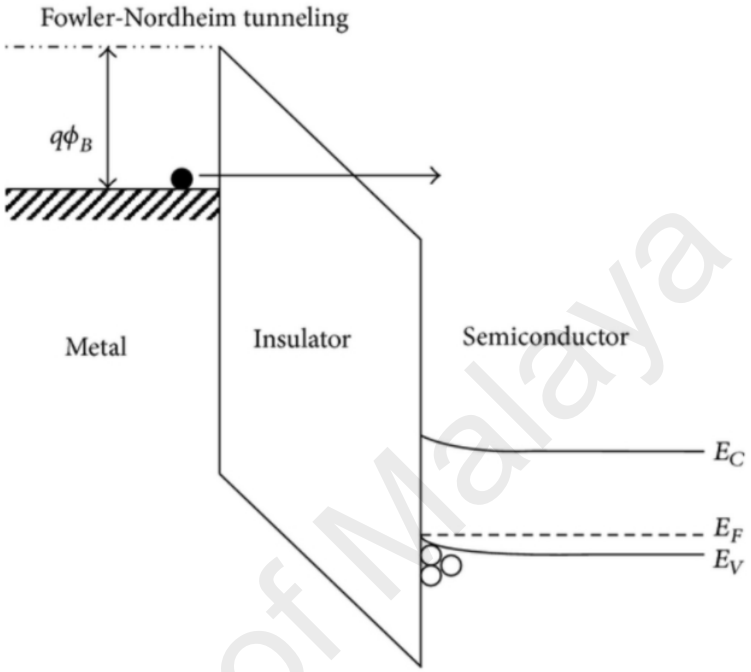


Figure 2.5 Fowler-Nordheim energy band diagram (Kian Heng Goh A. H., 2016)

2.5.1.3 Direct Tunneling

When the width of potential barrier decreases, chances for electrons and holes to penetrate through the barrier rises exponentially and this occurs when the oxide layer thickness is lower than 5 nm. It tunnels through square of trapezoidal barrier. The insulator or oxide will be thinner compared to F-N tunneling.

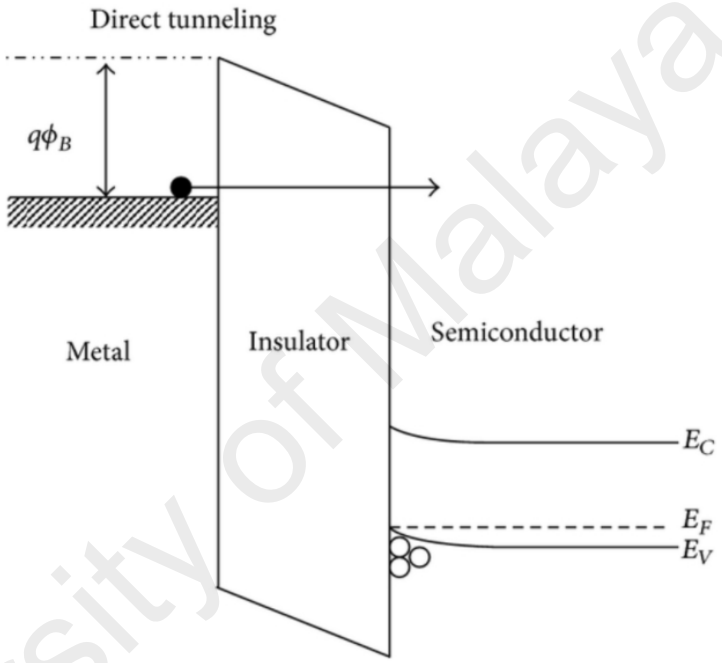


Figure 2.6 Direct tunneling energy band diagram (Chiu, 2014)

2.5.1.4 Thermionic Field Emission

Occurs between of Schottky and Field Emission. Requires high heat to emit electrons and are limited by space charge effect.

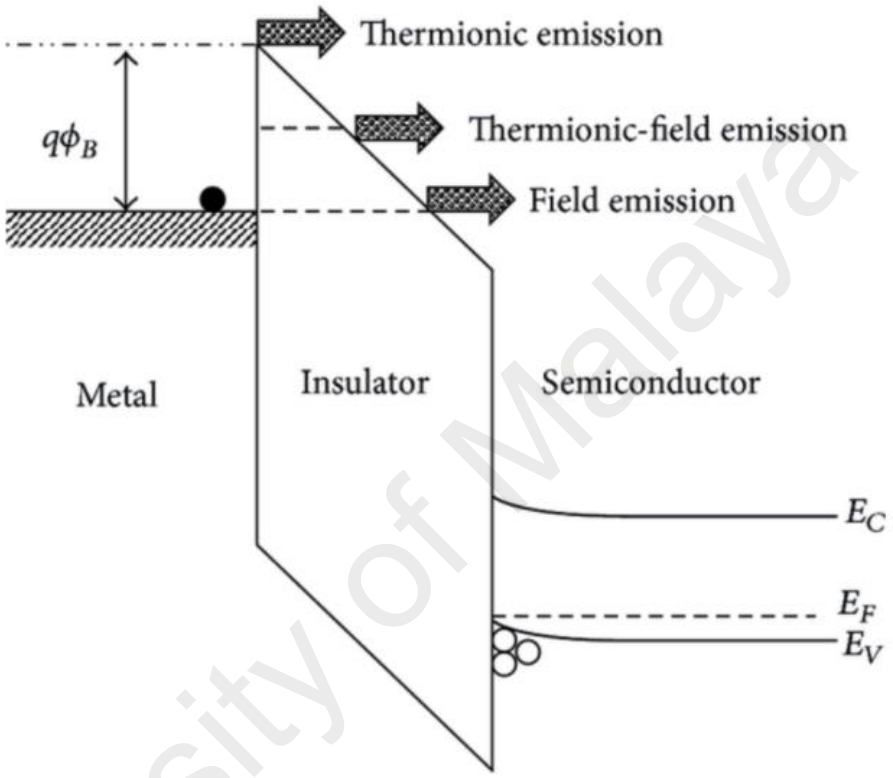


Figure 2.7 Thermionic-field emission energy band diagram (Chiu, 2014)

2.5.2 Bulk-limited conduction mechanism

2.5.2.1 Poole Frenkel (P-F) emission

When electrons are in fixed state in the insulator, it will not be able to move around unless a thermally activated.

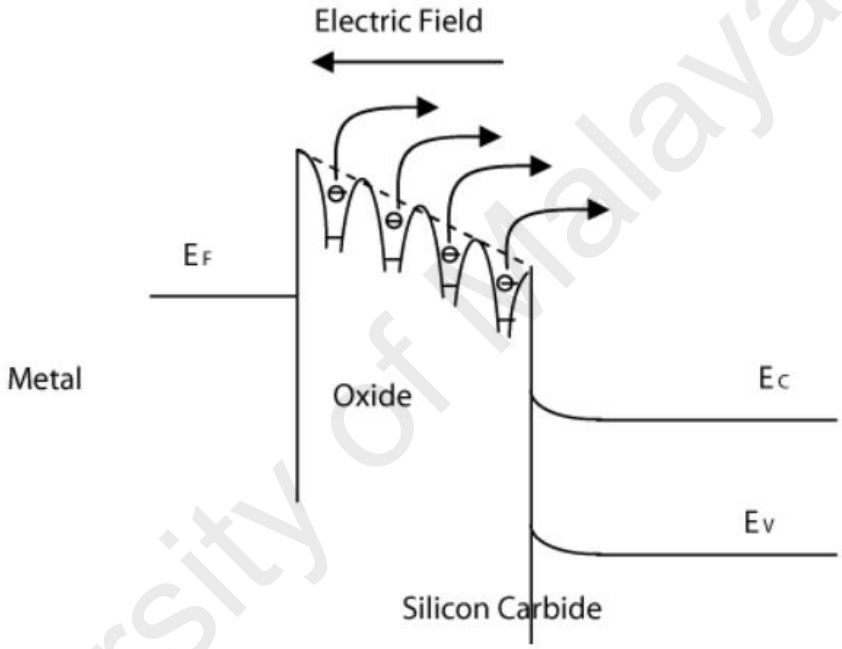


Figure 2.8 Poole Frenkel energy band diagram (Chiu, 2014)

2.5.2.2 Hopping Conduction

It is because of tunneling effect of trapped electrons that hops from one side where it is trapped to another side where there is dielectric film.

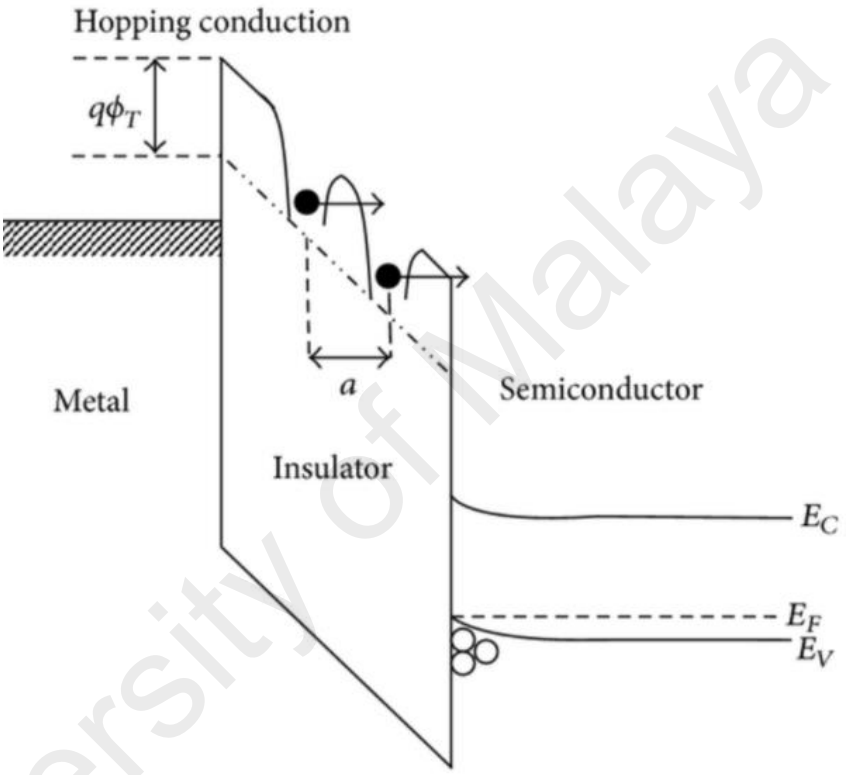


Figure 2.9 Hopping conduction's energy band diagram (Chiu, 2014)

2.5.2.3 Ohmic conduction

Applied electric field and temperature are important factors that affects ohmic emission. Possibilities on some carrier generation due to thermal excitation despite the big dielectric energy band gap (Chiu, 2014).

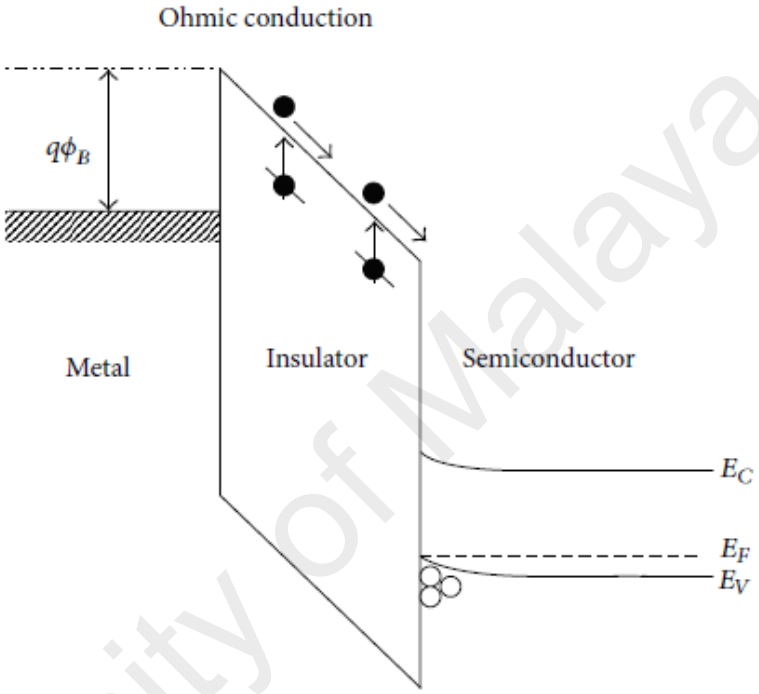


Figure 2.10 Band diagram of Ohmic Conduction in MIS structure (Chiu, 2014)

2.5.3 Trap-Assisted Tunneling (TAT) Mechanism

TAT is like modified F-N but in TAT, the presence of traps within the insulator makes the tunneling event as a 2-step process. When compared to the modified F-N, the involvement of the trap simply means the transit time of charge strongly depends on time the charge will spend bound to the trap site. Traps are capable of keeping the charges, if charge is located somewhere within insulator, it causes changes in energy diagram, charges go in, trapped, and released.

TAT occurs at very low electric fields. Leakage of current happens when trap density is high. Stress induced leakage current (SILC) is the associated leakage.

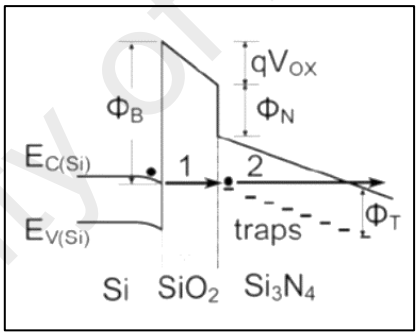


Figure 2.11 Example of 2-step TAT mechanism

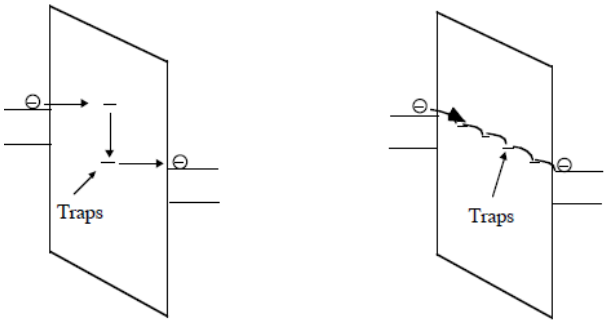


Figure 2.12 MOS structure and Trap Assisted Tunneling energy band diagram

2.6 Advantage of ZrON over ZrO_2

Dielectric constant plays an important role for a gate oxide, the higher the k value, the better its ability into stabilizing charges. ZrO_2 was one amongst many that has gained attention for its high k value that is between 22 to 25. Besides, it has huge energy bandgap ranged between 5.8 to 7.8eV, and this bandgap simply means the gap between conduction and valence band of the oxide layer and the further they are, the lower changes for current leakage, and the better they are as an insulator. Nevertheless, it came with its own drawback where due to oxidation induced interface and surface defects, leakage current occurs, and this may reduce lifespan of the MOS device (S. Mudanai, 2002). To further enhance this gate oxide, researches introduced nitrogen into film of ZrO_2 and results obtained showed the thinner interfacial layer formed and smaller interface trap density.

2.7 Transistor

A transistor is one of the semiconductor devices that has many functions and plays a key role in the electronics world. Its functions are to amplify signals, switching electronic signals such as current and voltage. Transistors can be categorized as bipolar junction and field effect.

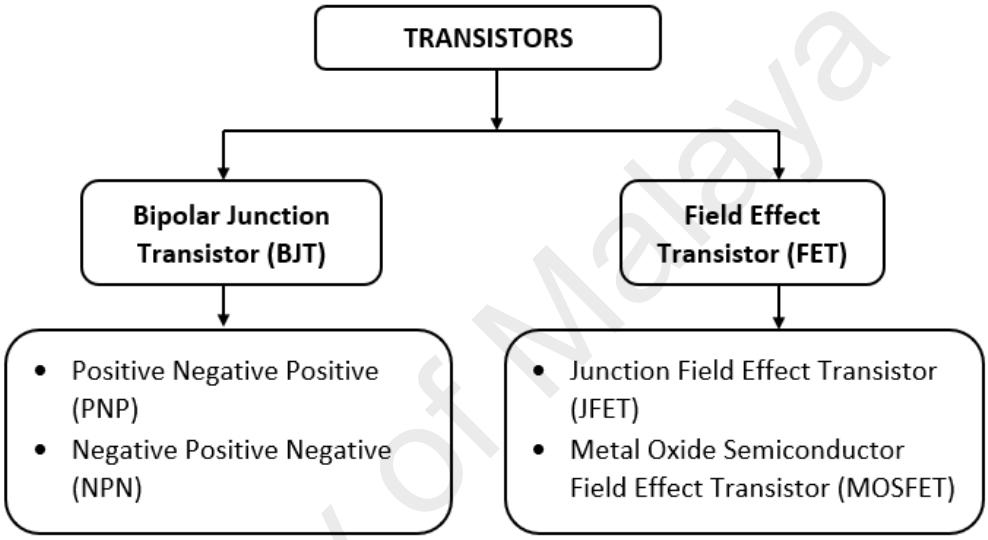


Figure 2.13 Types of Transistors

2.7.1 MOSFET

(MOSFET) is a compact device that can be miniaturized and produced in mass production. In general, it is made of 4 terminals, such as below.

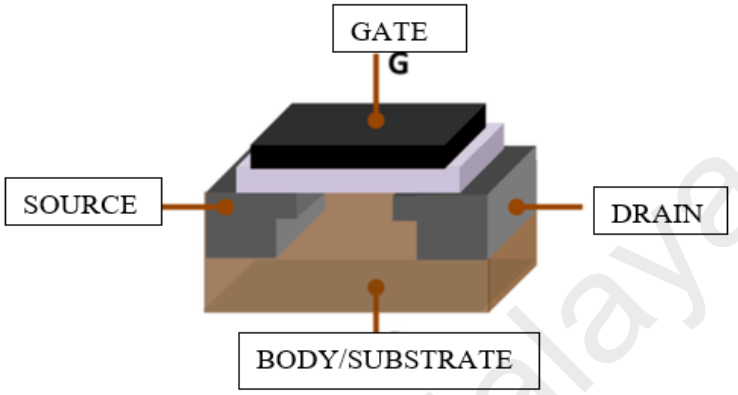


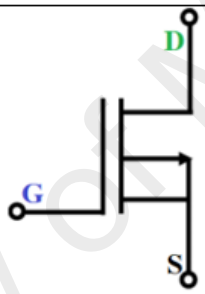
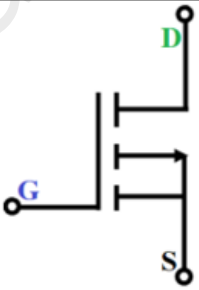
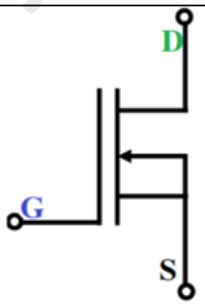
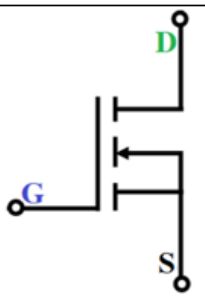
Figure 2.14 MOSFET structure

It looks like a 'sandwich' as its made of a few layers such as wafer as the substrate, an oxide layer, a layer of control electrode, and channels at the end of each side known as the source and drain (Ahmad Sabirin Zoolfakar and Hashimah Hashim, 2008).

It is widely used to amplify electronic signals and for switching signals. Basic way of how it functions is its charge carriers will enter the channel via source terminal and exit via drain. The channel width is controlled by voltage of gate. The gate is insulated using a thin metal oxide layer from the underlying terminals of source and drain. The oxide layer will act as a dielectric layer or electrical insulator to allow the gate to be able to sustain high transverse electric field.

MOSFET has two mode of functions, they are known as depletion mode and enhancement mode (Ahmad Sabirin Zoolfakar and Hashimah Hashim, 2008).

Table 2.1 Depletion enhancement mode (Ahmad Sabirin Zoolfakar and Hashimah Hashim, 2008)

	Depletion 'Normally closed switch'	Enhancement 'Normally open switch'
P-channel MOSFET		
N-channel MOSFET		

2.8 Thin Film Transistors (TFT)

Thin film, or also known in few other names, such as insulator, gate dielectric material or gate oxide, is an electronic device, and a type of MOSFET that has an active layer made of semiconductor, electrodes and dielectric and comes with thickness ranging from nanometer to micrometers. It is deposited onto a non-active substrate, placed in between the source drain channel and the gate; this is to ensure current is flowing from source to drain and prevent it flowing to the gate. Substrate in a TFT does not interfere on the electrical characteristics but merely to provide mechanical support to the structure (João P. Braga, 2018).

There are two characteristics that evaluates the electrical performance of the TFT, they are known as current-voltage curves, named as the output curve and transfer curve (João P. Braga, 2018).

A) Output curve

   Defined by current of drain-source vs voltage of drain-source (IDS vs VDS) when the constant values of gate voltage (Vg) is different

B) Transfer curve

   Defined by current of drain-source vs gate voltage (IDS vs Vg) when the constant value of VDS is different.

CHAPTER 3: METHODOLOGY

3.1 Experiment Flowchart

This chapter discusses on the experimental flowchart into obtaining the Zirconium Oxynitride thin film on a Silicon Carbide substrate via several processes and finally obtaining the characteristics via characterization.

There were total of 6 processes involved before characterizing the thin film, and these processes involved various usage of different materials and equipment such as chemicals, Edwards Auto 500 Radio Frequency sputtering, semiconductor parameter analyzer etc.

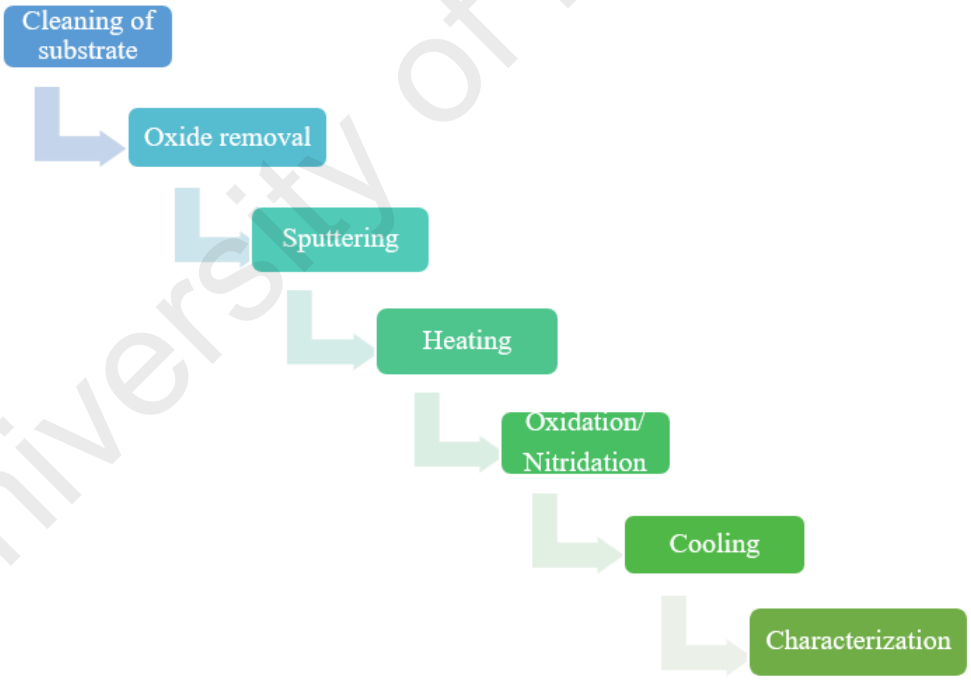


Figure 3.1 Project Flowchart

3.2 Experimental Procedures

3.2.1 Cleaning of substrate

Using Radio Corporation of America (RCA) method, substrate was cleaned.

RCA Method

- Step 1: Standard clean (Organic clean + Particle clean), ultrasonically degrease the wafer
- Step 2: Oxide strip
- Step 3: Standard clean (Ionic clean)
- Step 4: Rinsing and drying

3.2.2 Oxide Removal

Hydrofluoric acid (HF) solution with ratio 1 HF: 50 H_20 was used to remove oxide layer on surface of substrate

3.2.3 Sputtering

Using Edwards Auto 500 Radio Frequency sputtering, Zirconium film with thickness of 5 nm was sputtered on the cleaned Silicon Carbide substrates. Working pressure of 1.2 x 10^{-7} Torr, Radio Frequency Power of 170 W and inert Ar gas flow at 20cm^3/min were parameters that got recorded during sputtering process.

3.2.4 Heating

Samples were then heated in a furnace with Ar flow ambient at 4 different temperature (400ºC, 500ºC, 700ºC and 900ºC) and the heating rate was set to be at a constant of 10ºC/min. The activation energy to oxidize falls between range 400ºC to 1000ºC, and therefore four different temperatures within this range were objectively chosen to obtain a comparable trend.

3.2.5 Oxidation/Nitridation

N_2O was introduced with a flow rate of 150mL/min for 15 minutes once the set temperature was achieved for each sample.

3.2.6 Cooling

Samples were cooled down in a room temperature after oxidation and nitridation process.

3.2.7 Characterization

Al-gate was fabricated on top of the film for characterization purposes. By using semiconductor parameter analyzer (SPA), electrical properties were recorder.

3.2.8 Calculation

SigmaPlot and Microsoft Excel were two main software used to calculate all the results using obtained raw data.

CHAPTER 4: RESULTS AND DISCUSSIONS

4.1 Leakage current density (J) vs Electric Field (E)

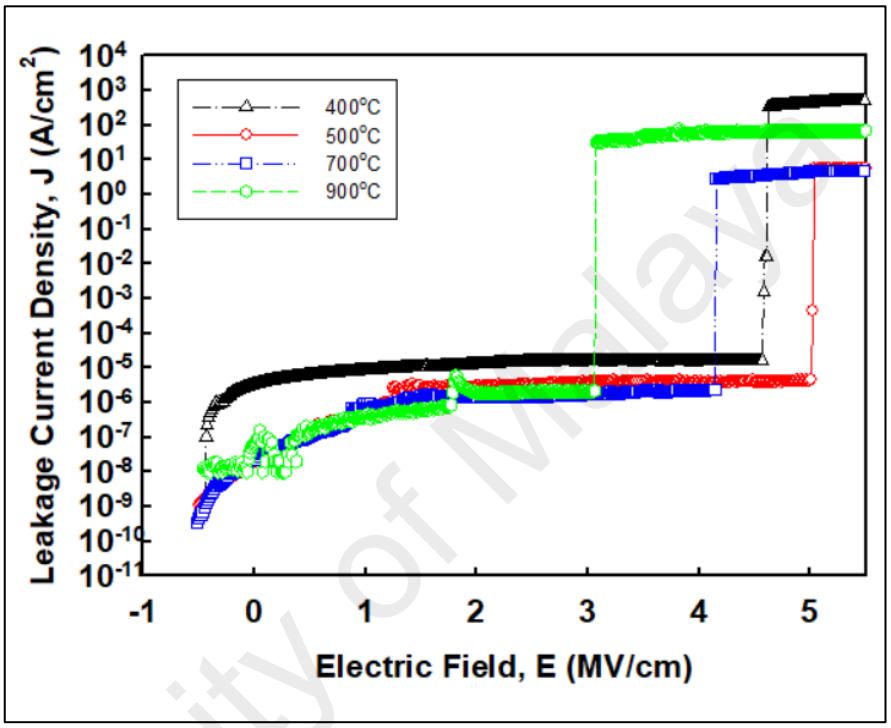


Figure 4.1 J-E characteristics of samples oxidized/nitrided at various temperatures

Plot above shows the relationship between leakage current-density (J) and electric breakdown field (E) when the samples were oxidized/nitrided at 4 different temperatures of (400ºC, 500ºC, 700ºC and 900ºC). The reason *J-E* characteristics was plotted is to study the effects of oxidation temperature on the electrical properties of the samples (Zhen Ce Lei, 2017).

Using the computer-controlled SPA system, (I-V) measurement was converted into *J-E* plot. The E value was calculated using the below formula (Kuan Yew Cheong, 2012).

$$E_B = V_g - V_{FB} / t_{ox}$$

Where E_B = Dielectric breakdown

Vg = Gate Voltage

V_{FB} = Flatband Voltage

t_{ox} = Oxide thickness

From the plot, it can be seen at sample of 500ºC, highest E_B value of 5.05 MV/cm with a leakage current density of 10^{-6} A/cm^2 was obtained The reason high dielectric breakdown is necessary is because, the higher the dielectric breakdown, it simply means the longer it takes for the oxide layer to breakdown, which also means it doesn't conduct current that easily.

4.2 Trap assisted tunneling

From the leakage current density vs electric field curve (*J-E*), possibilities of trap assisted tunneling was observed. If the dielectric layer has got defects, then the breakdown steps could be more than 1. The J-E curve was plotted for each temperature separately to be able to see the trend.

4.2.1 *J-E* curve at 400 ºC

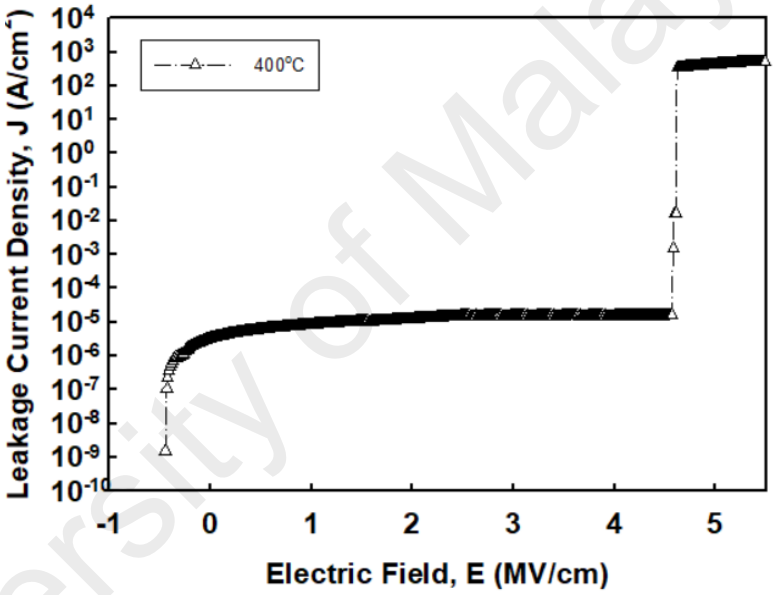


Figure 4.2 J-E curve at 400°C

When sample was oxidized/nitrided at 400°C, there was no 2-step breakdown observed which also means there may not be any trap assisted tunneling (TAT). The possible conduction mechanisms that may have contributed to those leakages could be Ohmic, Trap Field Limited (TFL), Child's Law, Schottky Emission, Poole Frenkel, and finally Fowler Nordheim where breakdown happens.

4.2.2 *J-E* curve at 500 ºC

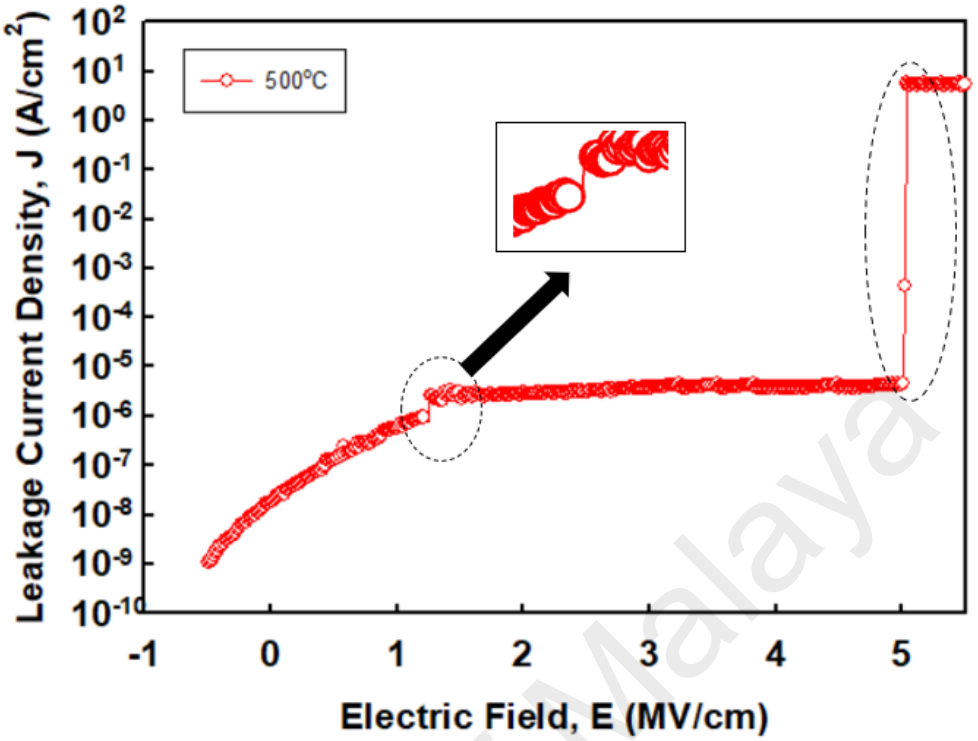


Figure 4.3 J-E curve at 500 ºC

When sample was oxidized/nitrided at 500°C, two step breakdowns were observed, and this explains it could be a TAT. The first breakdown was very minor, and the electric field was between the range of 1.20 MV/cm to 1.26 MV/cm. And for the 2nd breakdown, the change in order of magnitude from was large, changing from 10^{-6} to 10^{1} before reaching Fowler Nordheim where it breaks down completely.

4.2.3 *J-E* curve at 700 ºC

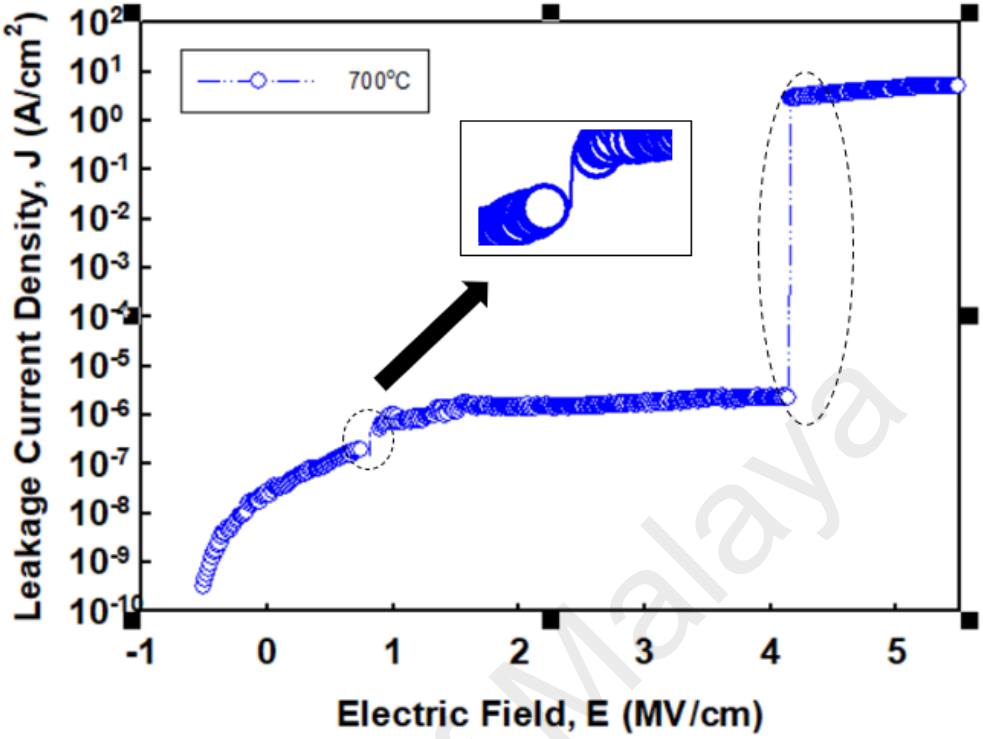


Figure 4.4 J-E curve at 700 ºC

When sample was oxidized/nitrided at 700°C, two step breakdowns were also observed, and this explains it could be a TAT. The first breakdown was very minimal, and the electric field was between the range of 0.73 MV/cm to 0.89 MV/cm. And for the 2nd breakdown, the change in order of magnitude was large, similar with sample of 600ºC, where it changed from 10^{-6} to 10^{1} before reaching Fowler Nordheim where it breaks down completely.

4.2.4 *J-E* curve at 900 ºC

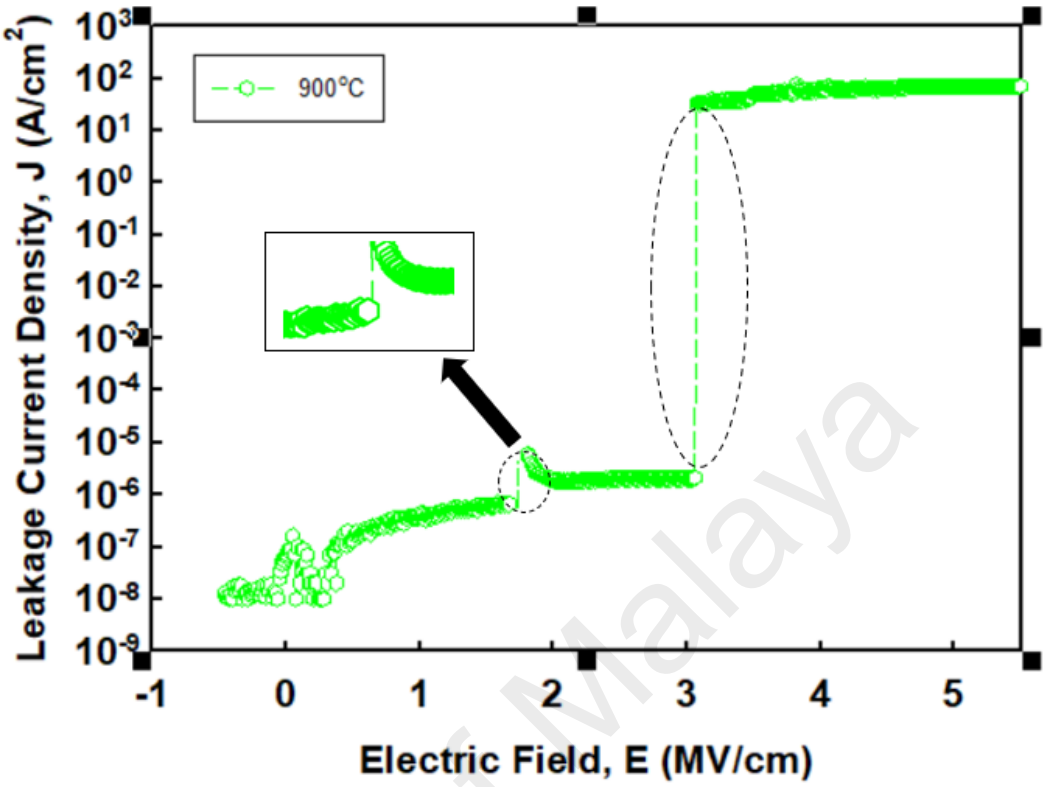


Figure 4.5 J-E curve at 900 ºC

When sample was oxidized/nitrided at 900°C, two step breakdowns were also observed, and again, could be a possibility of a TAT. The first breakdown was also very minimal, where the electric field was between the range of 1.75 MV/cm to 1.80 MV/cm. And for the 2nd breakdown, the change in order of magnitude was large, similar to both samples of 500ºC and 700ºC, where it changed from 10^{-6} to 10^{1} before reaching Fowler Nordheim where it breaks down completely.

As overall of *J-E* curve, samples of 400°C, 500°C, and 700°C have shown to be a possible TAT mechanism. A ln *JE* vs 1/*E* curve was plotted to check the possible trap energy and trap density in those samples.

4.3 Trap Energy And Trap Density

A curve of ln (*JE*) vs 1/*E* was plotted to be able to see the goodness of fit and obtain the slope and intercept which that can be used as values of both traps.

4.3.1 ln (*JE*) vs 1/*E*

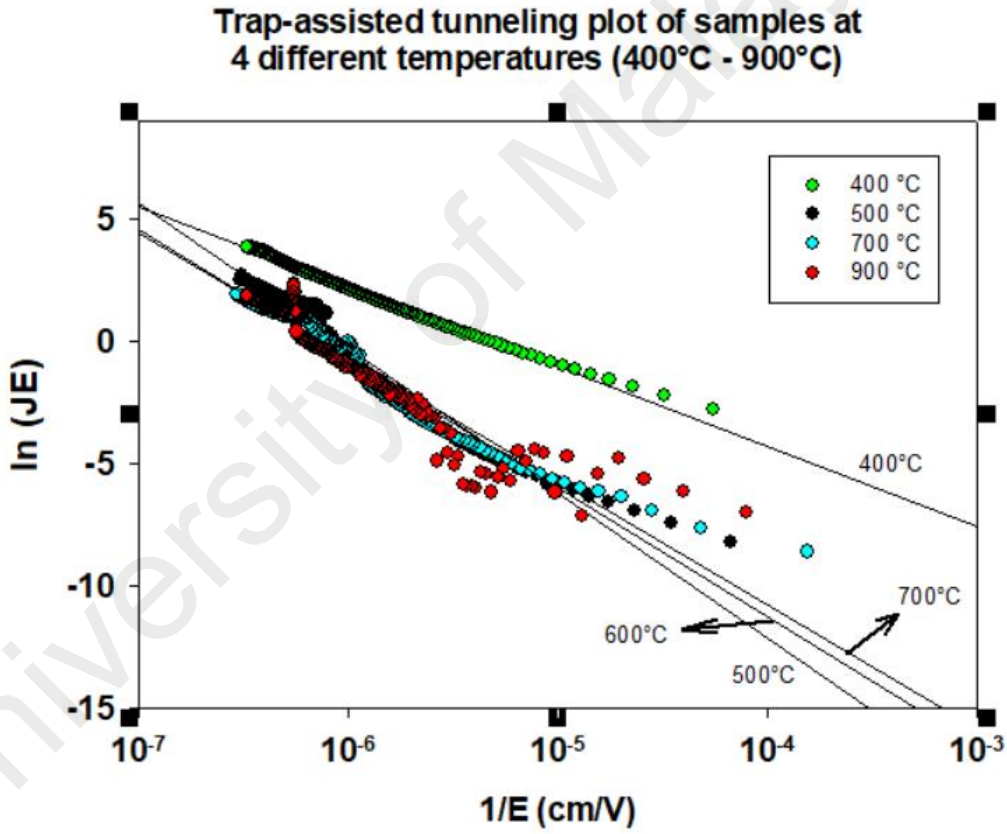


Figure 4.6 Trap-assisted tunneling plot of samples at 4 different temperatures

Simplified tunneling equation is as follow

$$\ln(JE) = \left(-A\phi_t^{3/2}\right)(1/E) + \ln(G)$$

- Where G = (2/3) (C_t N_t q ϕ_t).
- ϕ_t is the trap energy, and can be calculated from the slope of ln *JE* vs 1/*E*
- Nt is the trap density and can be calculated from the y-intercept of ln *JE* vs 1/*E*

From the plot, the r^2 value for sample at 400°C has shown to have the highest value of 0.99, which is 99% closely fitted data and this could be due to it is a one-step breaking process and not a TAT. This will be further explained in the next section below.

4.3.2 Slope and Intercept

From the plot, (Kian Heng Goh Y. A., 2016) discusses that from *JE* vs 1/*E*, the, slope of the graph indicates trap energy ($ø_t$) and intercept indicates trap density (*Nt*).

Trap energy was the slope from the regression line result, or known as b [1], whereas trap density was the intercept from the regression line, known as b [0]. A table was plotted for all values of b [0] and b [1] for all four different samples.

Table 4.1 Trap energy and trap density

Temperature, ^{0}C	b [0]	b [1]	r^2
400	-17.3890280522	3.2689500707	0.9941660878
500	-35.8064711124	5.9214630244	0.9645139568
700	-31.0219837782	5.0622034443	0.958996267
900	-32.3500905732	5.2709151048	0.910015955

4.3.2.1 Trap density of 4 different samples

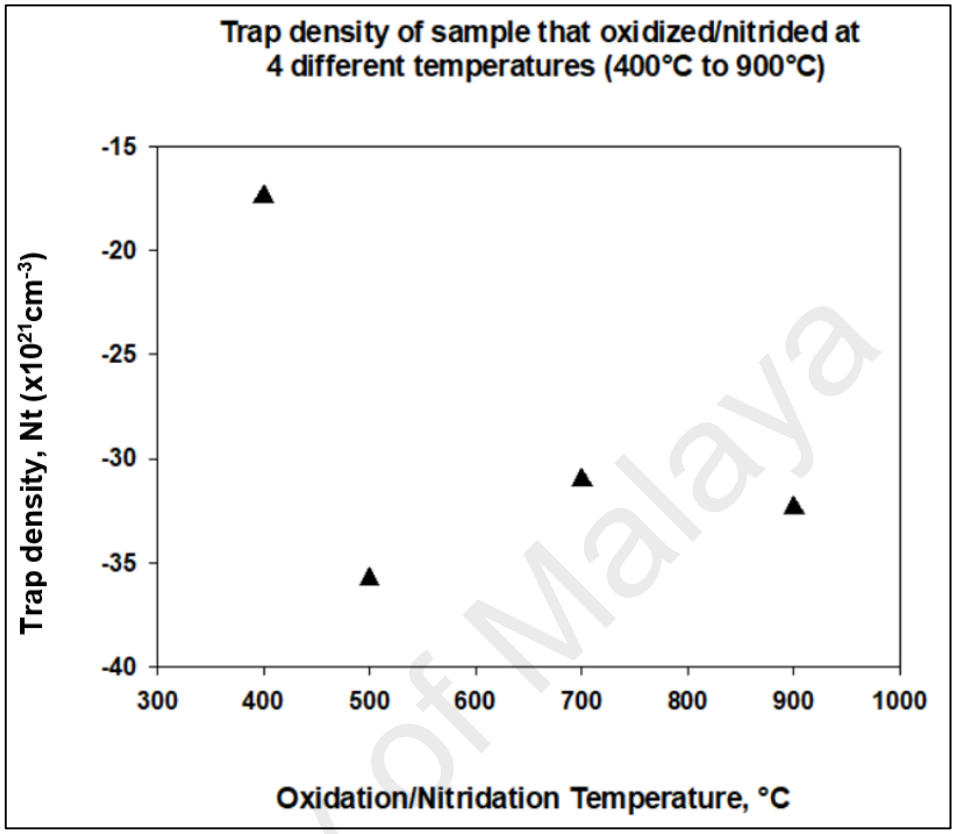


Figure 4.7 Trap density of 4 different samples

This figure shows trap density of 4 samples with different oxidation/nitridation temperature. From the plot, the trap density was lowest for sample at 500ºC, at a value of -35.8 x 10^{21} cm^{-3} and the highest was by sample 400ºC at a value of -17.38 x $10^{21}cm^{-3}$. Low trap density means low leakage current density and a large trap density can affect the mobility of electrons a MOSFET device that uses SiC. In this case, sample at 500°C could be considered to be the best among other temperatures in this study. Besides, as discussed earlier in *J-E* curve, only sample at 400°C has shown that may not be a TAT and that could be a reason on why it has a huge drop and it does not follow the trend the other three samples have got.

4.3.2.2 Trap energy of 4 different samples

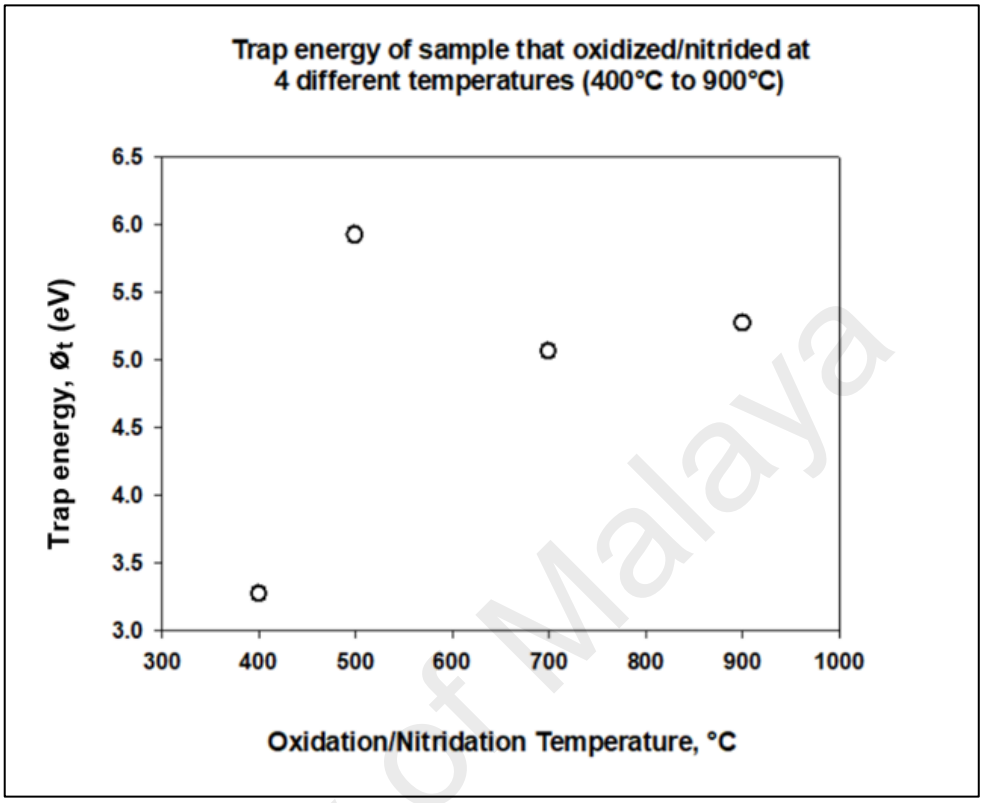


Figure 4.8 Trap energy at 4 different samples

This figure shows trap energy of 4 different oxidation/nitridation temperature and the trap energy was highest for sample at 500ºC, at a value of 5.92 eV. Trap energies normally has a reversed plot when compared to trap density. High trap energy simply means it has higher capability into storing charges.

4.3.2.3 Combined plots of the traps

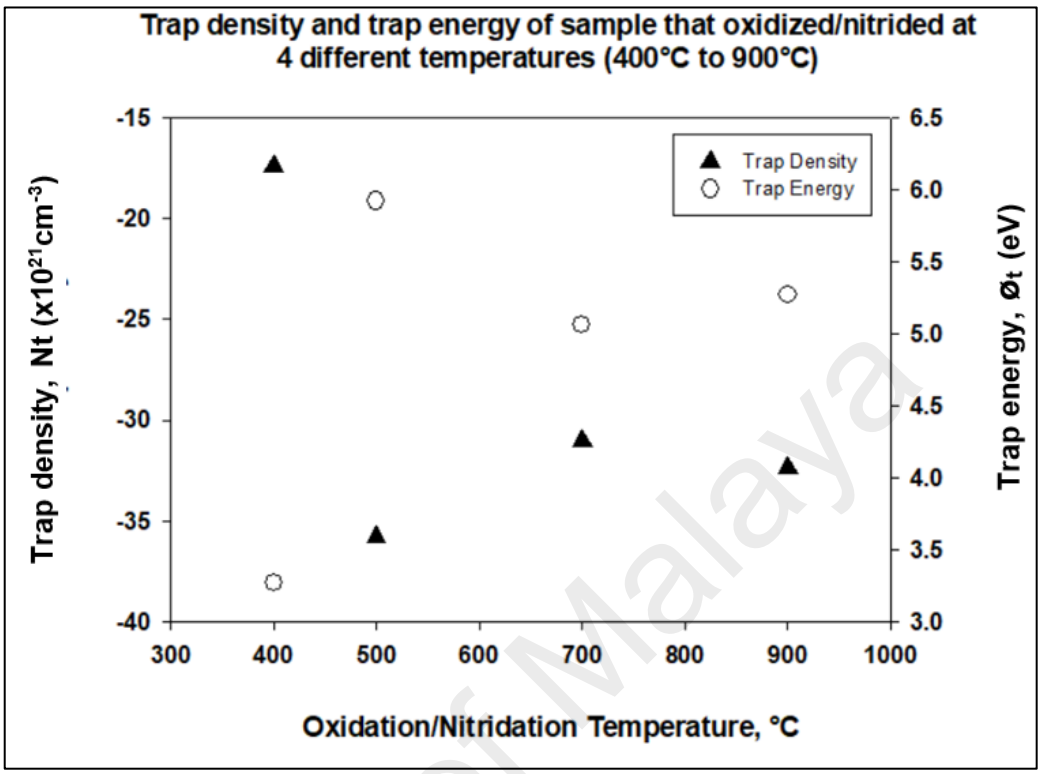


Figure 4.9 Trap density and trap energy of all 4 samples

This plot is a combination of both the trap density and trap energy and as can be seen, they are both in the opposite direction.

It can be concluded that when the sample is oxidized/nitrided at 500ºC, it has the highest trap energy and lowest trap density, therefore contributing to the lowest leakage current density.

CHAPTER 5: CONCLUSION

From *J-E* curve, sample oxidized and nitrided at 500°C, 700°C and 900°C shows possibilities of trap assisted tunneling (TAT) due to its two steps break down. From *J-E* values, a graph of ln (*JE*) vs 1/*E* was plotted to obtain details of trap energy and trap density.

Slope and intercept value were obtained from the regression line and slope here indicates trap energy whereas intercept indicates trap density. From the plot for sample oxidized/nitrided at 500°C, trap density was the lowest at a value of -35.8 x 10^{21} cm^{-3} and trap energy was the highest at value of 5.92eV. Both these results indicate the current leakage is low and the ability for it to store charges are quite high.

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