ANALYSIS OF SPACE-CHARGE-LIMITED CONDUCTION MECHANISMS IN ZRON/SIC SYSTEM

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ANALYSIS OF SPACE-CHARGE-LIMITED CONDUCTION MECHANISMS IN ZRON/SIC SYSTEM

ABSTRACT

In this study, current conduction mechanism by space-charge-limited conduction (SCLC) and Poole-Frenkel (PF) emission on ZrON/SiC system that was oxidized and nitrided in N_2O at various temperatures (400-900˚C) were analysed. The current-voltage (I-V) measurements were performed in Al-gate metal-oxide-semiconductor (MOS) capacitor by sputtering of Al film on top of the film and at the back of the substrate. Then, characterization of electrical properties was done according to two types of bulk-limited conduction, which are space-charge-limited conduction and Poole-Frenkel emission conduction. Space-charge-limited conduction and Poole-Frenkel emission have been systematically evaluated through data analysis method by the fitting of linear regression according to Ohm's Law model in J-V_g plot and Poole-Frenkel model in ln (J/E)-$E^{1/2}$ plot. The mechanisms of the interface traps and the current conducted through oxides were affected by the temperature of simultaneous oxidation and nitridation performed on the sputtered Zr on SiC substrate. Electrical results showed that sample that was oxidized/nitrided Zr/SiC for 15-min duration at 500˚C recorded the highest electric field breakdown (E_B) of 5.05 MV/cm at 10^{-6} A/cm^2. Based on the current density and electric field (J-E) plot, the space-charge-limited conduction mechanism by Ohm's law was analysed. It is found that Ohm's law conduction occurs at low electric field (-0.4 – 0.05 MV/cm). As for Poole-Frenkel emission, the conduction mechanism occurs at higher electric field range (0.6-1.65 MV/cm). The effect of different oxidation and nitridation temperature on leakage current and electric field breakdown at were compared and discussed.

Keywords: Space-Charge-Limited Conduction, Poole-Frenkel emission, Ohm’s law, Current leakage

KAJIAN MEKANISMA KONDUKSI RUANGAN-CAS-TERHAD DI DALAM SISTEM ZRON/SIC

ABSTRAK

Di dalam kajian ini, konduksi arus elektrik oleh ruangan-cas –terhad di dalam sistem zirconium oxinitrat di atas silicon karbida (ZrON/SiC) yang telah menjalani pengoksidaan dan penitridaan serentak dengan menggunakan gas N_2O pada pelbagai tahap suhu pengoksidaan/penitridaan (400-900˚C) telah dianalisis. Hubungan antara arus elektrik dan voltan diukur dan dijalankan melalui proses filem nipis Aluminium (Al) dipercikkan di permukaan atas filem teroksida dan di permukaan belakang lapisan semikonduktor. Kemudian, pencirian oleh sifat elektrik dijalankan melalui dua jenis konduksi pukal-terhad iaitu konduksi oleh ruangan-cas-terhad dan konduksi pancaran Poole-Frenkel. Konduksi arus elektrik oleh ruangan-cas-terhad dan pancaran Poole-Frenkel telah dievaluasi secara sistematik berdasarkan kaedah analisis data oleh penyesuaian graf regresi linear mengikut model hukum Ohm di dalam plot J-E dan model Poole-Frenkel di dalam plot ln (J/E)-$E^{1/2}$. Mekanisma perangkap antara muka dan arus elektrik melalui lapisan oksida dipengaruhi oleh tahap suhu pengoksidaan/penitridaan serentak terhadap zirconium yang telah dipercikkan di atas silicon karbida telah dijalankan. Keputusan elektrik menunjukkan pengoksidaan/penitridaan ke atas Zr/Si selama 15 minit pada suhu 500˚C mencatat medan pecah tebat (E_B) yang tertinggi iaitu sebanyak 5.05 MV/cm pada arus bocor sebanyak 10^{-6} A/cm^2. Berdasarkan graf hubungan antara ketumpatan arus dan medan elektrik, konduksi ruangan-cas-terhad oleh hukum Ohm telah dianalisis. Kajian menunjukkan mengikut hukum Ohm, konduksinya akan berlaku pada medan elektrik rendah (-0.4 – 0.05 MV/cm). Bagi mekanisma konduksi pancaran Poole-Frenkel pula akan berlaku pada skala medan elektrik yang lebih tinggi (0.6-1.65 MV/cm). Akhir sekali, kesan lapisan teroksida yang diperoleh daripada pengoksidaan/penitridaan ke

atas Zr/SiC ke atas arus bocor dan medan pecah tebat pada pada pelbagai tahap suhu dibincangkan.

Kata kunci: Konduksi ruang-cas-terhad, Pancaran Poole-Frenkel, hukum Ohm, Arus bocor

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LIST OF SYMBOLS AND ABBREVIATIONS

C-V	:	Capacitance-voltage
DI	:	Deionized
E_B	:	Dielectric breakdown
EFTEM	:	Energy-filtered transmission electron microscopy
EOT	:	Equivalent gate oxide thickness
FN	:	Fowler-Nordheim
GaAs	:	Gallium Arsenide
GaN	:	Gallium Nitride
HF	:	Hydrofluoric acid
IL	:	Interfacial layer
I-V	:	Current-voltage
J	:	Current density
J-E	:	Current density and electric field
J-V	:	Current density and voltage
$J\text{-}V_g$	:	Current density and gate voltage
MOS	:	Metal-oxide-semiconductor
PF	:	Poole-Frenkel
RF	:	Radio frequency
SCLC	:	Space-charge-limited conduction
SCS	:	Semiconductor characterization system
SPA	:	Semiconductor parameter analyzer
TFL	:	Trap-filled-limit
t_{ox}	:	Oxide thickness
V_{fb}	:	Flat band voltage

V_g	:	Gate voltage
ZrSiON	:	Zr-silicate oxynitride
SiO_2	:	Silicon dioxide
Z_rON	:	Zirconium oxynitride
SiC	:	Silicon carbide
N_2O	:	Nitrous oxide
NO	:	Nitrogen oxide
Al	:	Aluminium
Zr	:	Zirconium
ZrO_2	:	Zirconium dioxide

CHAPTER 1: INTRODUCTION

1.1 Background

Semiconductor comprises a broad product category, such as integrated circuits, microprocessors, and chips constructed from materials that demonstrate intermediate properties between conductors and insulators. This peculiar property renders semiconductors a decent medium for electrical current control. Scaling down of the metal-oxide semiconductor (MOS) has continuously bring forward the evolution of Si-based semiconductor to have a very good performance at lower cost and circuit functionality. It also has led to many improvements in the semiconductor industry. The MOS structure dimension must be reduced proportionally, without compromising its electrical properties (Robertson, 2004). Consequently, to keep up with the development of semiconductor industry, microelectronics devices size has been scaled down and typical materials that form such devices exceed their fundamental material limits.

At present, SiC-based semiconductor is widely used in devices since they are more reliable and have higher performance. Based on Marckx et. Al (2006), silicon carbide (SiC) has superior physical properties with higher bandgap energy, higher breakdown field and thermal conductivity compared to silicon (Si), gallium arsenide (GaAs).

The fabrication of these devices is also very important which can also affect the electrical properties of the gate oxide. The gate oxide must be able to bear a high transverse electric field and be of excellent reliability, so that the leakage current through the gate oxide could be minimized (Wong & Cheong, 2012). Therefore, high dielectric-constant materials have attracted a great deal of attention from industries as the alternative to conventional SiO2 gate dielectrics. Consequently, fabrication technique which can produce higher dielectric constants are desired. Electrical properties of MOS devices can be improved via simultaneous oxidation and nitridation

using nitrous oxide gas (N_2O) (Wong & Cheong, 2012). Incorporation of N_2O in the ZrO stack has been reported to prevent the increase of equivalent oxide thickness (EOT) in MOS device fabrication (Nieh et. Al, 2003).

The understanding of conduction mechanism across ZrON/SiC system is important in order to evaluate the current leakage and breakdown of the MOS devices. The conduction of current through the system depends on the voltage applied across the sample, surface roughness, grain size and its temperature (Chenari et. Al, 2011). In this study, two types of bulk-limited conduction mechanisms will be analyzed which are the space-charge-limited conduction by Ohm's Law and Poole-Frenkel emission conduction.

1.2 Problem Statement

High leakage current in nanometer-sized technology has become a significant problem due to the rapid scaling of MOS devices and the large amount of transistors on a chip. The resulting leakage current due to its scaling has become a dominant factor in overall consumption of chip power. There are many types of current leakage mechanisms. Leakage of the gate oxide tunneling is one of the most challenging problems associated with the scaling of future devices. To reduce the equivalent gate oxide thickness (EOT), while having a physically thicker gate oxide, new gate-dielectric materials with higher dielectric constants (κ) are needed to reduce the gate oxide tunneling leakage current.

A good understanding along with precise modeling of the conduction mechanisms in these materials is essential for the successful integration of these materials into future technologies. Reliability and lifetime of a MOS device depends on the interface traps, barrier heights and charges in the oxide layer where major source to current leakage

occurs. Thus, the current conduction through the MOS before the breakdown should be analysed in terms of its interface traps, barrier heights and charges across the MOS structure which characterizes the electrical properties. Analysis and understanding of charge conduction mechanism will help to estimate leakage characteristics of ZrON/SiC system to realize its reliability and electrical properties as a highly reliable device.

Bulk-limited conduction mechanism is temperature dependent. Thus, simultaneous oxidation and nitridation temperature during fabrication is also an important variable in the analysis of electrical properties characterization of the current conduction across the system. The different temperature affects the excitation of electrons injection into the oxide layer. Therefore, this study was conducted to analyse the current leakage through charge conduction mechanisms at various temperatures of oxidation and nitridation temperatures.

1.3 Research Objectives

There are two objectives to be achieved in this study:

1. To study Ohm's law behaviour in ZrON/SiC system.
2. To investigate the possible existence of Poole-Frenkel conduction mechanisms in ZrON/SiC system.

1.4 Scope of Study

In this study, Zirconium (Zr) film was sputtered on SiC substrates and sent for simultaneous oxidation and nitridation in N_2O ambient to form oxidized/nitrided Zr on SiC substrates.

Current density and electric field (J-E) characterization of oxidized/nitrided Zr thin films were conducted from current-voltage (I-V) measurement done through Al gate electrode metallization process to form an Ohmic back contact.

The effects of simultaneous oxidation and nitridation temperatures on Zr/SiC with space-charge-limited conduction mechanisms are analysed.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

As the world's technologies in electronic devices revolve, semiconductor industries have been focusing in four parallel directions in order to fulfill the demands on microelectronic devices. The industry have been putting their focus to downscale the circuit elements, reduce power consumption, increase operating speed and increase tolerance-temperature range (Wilk, Wallace, & Anthony. 2001; Wong & Cheong, 2010). Effect of simultaneous oxidation and nitridation of Zr in nitrous oxide ambient at various temperatures for a constant duration on space-charge conduction mechanisms are the main area of interest.

This chapter reviews the conduction mechanisms in MOS structure generally and ZrON/SiC system. This review is started with the introduction to basic structure of MOS. Then, ZrON as an alternative dielectric film is summarized. Next, the mechanism of the formation of dielectric by oxidation and the nitridation using the nitrous oxide gas in order to produce zirconium oxynitride is also reviewed. It is followed by comparison of differences between different types of substrate materials. Lastly, the conduction mechanisms in dielectrics are reviewed.

2.2 Metal-Oxide-Semiconductor (MOS)

2.2.1 MOS Structure

The structure of the metal-oxide semiconductor or MOS is the origin of modern microelectronics. The MOS composes of three layers as illustrated by Figure 2.1 Shown is the conductive metal electrode at the top layer, a gate oxide in the center layer, and the bottom layer of a semiconductor substrate. This structure, particularly in integrated circuits, is one of the most important and commonly used structures in electronic

devices. The two-terminal MOS capacitor is the simplest of all MOS devices. It is typically manufactured and used for electrical components. Under various static biasing conditions, the charge, electric field, as well as energy band inside the MOS capacitor can be quantitatively visualized (Pierret, 1990).

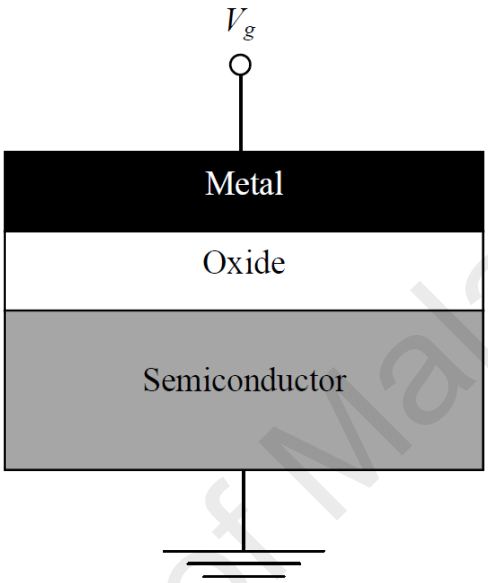

Figure 2.1: The Structure of MOS Capacitor diagram

2.3 ZrON as an Alternative Dielectric to SiO_2

It is necessary to scale down SiO_2, which was used as a gate dielectric in MOS devices for decades. The presence of fairly huge leakage current through the oxide is extremely probable due to direct carriers tunneling as the thickness of the oxide is less than 1.2nm (Wong & Cheong, 2010; Robertson, 2004; Kurniawan et al., 2011a, Kurniawan et al., 2011b). To address the challenge, a high dielectric constant (κ) oxide has been developed that acts as an alternative dielectric to replace SiO_2. The physical thickness of the high κ oxide must demonstrate considerably better MOS characteristics compared to SiO_2 (Robertson, 2004; Quah et al. 2010).

ZrO_2 has advantages such as high κ-value ranges from 22 to 25 (Wilk et al., 2001; Wong & Cheong, 2010; Robertson, 2004), fairly large bandgap (5.8–7.8 eV) (Wong & Cheong, 2010), good thermodynamic stability (Wong & Cheong, 2010; Copel, Gribelyuk, & Gusev, 2000, Gribelyuk, Callegari, Gusev, Copel, & Buchanan, 2002; Jeon, White, & Kwong, 2001), minimal lattice mismatch with Si(100) (Wong, 2012), as well as easily stabilized in the form of cubic or tetragonal polymorphs, which may improve its effective κ-value (Wong & Cheong, 2010; Jõgi et al., 2010; Weinreich et al., 2009). Nevertheless, ZrO_2/Si interfaces are also considered non-ideal due to interface defects caused by defects in structural-surface, defects by oxidation-induced or defects by radiation induced (Mudanai et al. 2002; Schroder 2006; Cheng et al., 2006).

This is because interface trap has a considerable impact or effect on the reliability and lifetime of a MOS device. The interface traps are also the main source of leakage current other than the characteristics of the oxide itself. To minimize the interface trap density to an accepted level, it is important to control the thickness and composition of the interfacial layer (IL) in between the gate oxide and semiconductor. Therefore, good electrical properties can be attained if the interface traps is controlled.

In the previous works of Wong and Cheong (2011a, 2011b, 2011c), simultaneous thermal oxidation and nitridation of sputtered Zr on Si using N_2O gas has formed bulk ZrO_2 and IL of Zr-silicate oxynitride (ZrSiON). The study has resulted an improved electrical properties to the MOS device due to the nitridation effect.

2.3.1 Role of Nitrogen in Gate Oxides

The thickness and composition of the interfacial layer (IL) between the oxide and the semiconductor were regulated by different deposition techniques. By doing so, appropriate degree of trap density of the interface can be attained. It is stated that interface traps can be effectively removed by nitridation of a Si surface before

deposition of ZrO_2 film or by incorporating nitrogen in ZrO_2 film (Chen, Lai, & Chen, 2007; Koyama et al., 2001).

Based on studies that were already done previously, incorporation of nitrogen into the film could assist in prevention of the growth of IL and consequently improved the electrical properties of the film (Koyama et al., 2001; Chen et al., 2002; de Almeida, & Baumvol, 2003). Most common gas used to perform simultaneous oxidation and nitridation are NO and N_2O (de Almeida, & Baumvol, 2003). However, between those two, N_2O is preferable due to its less toxic properties (Dimitrijev, Harisson, Tanner, Cheong, & Han, 2004). Researchers also hypothesized that dilution of N_2O may also be a possible way to adequately produce a better quality of oxide based on its study on thermally nitride and oxidized Si film on SiC substrate to form nitride SiO_2 gate (McPherson & Mogul, 1998; Schlund, Suehle, Messick, Chaparala, 1996; Suehle, Chaparala, Messick, Miller, & Boyko, 1994; Helms & Poindexter, 1994; Kimura, 1997). The incorporation of nitrogen gas into the process enhanced the removal of carbon that has been accumulated at the interface during thermal oxidation. By mixing both oxygen and nitrogen together have helped to improve the surface condition to have lesser defects compared to when it was only undergoing oxidation process. (Dimitrijev et al. 2004).

2.4 Comparison Between Si and SiC Substrate

Lipkin and Palmour (1999) mentioned that high κ-oxides are used on Si to solve the scaling issues. This means using Si as a substrate would be very beneficial when designing a smaller scale of MOS devices. On the other hand, SiC is used to lower the electric field that was disturbing the gate oxide. High electric field is a disadvantage to a MOS device since it can cause failure in the long run. This explained different substrate has different functions according to applications.

The comparison of the electrical properties between oxidized and nitrided Zr thin film on Si and SiC in nitrous oxide gas is shown as in Table 2.1. The comparison is given in terms of capacitance and voltage (C-V), leakage current density and electric field (J-E) characteristics (Puthenkovilakam, Carter, & Chang, 2004). The table shows that based on C-V characteristics measurement, oxidized and nitrided sputtered Zr film on SiC based substrate possessed higher κ-value with 49.68 compared to Si substrate with κ-value of 21.82. The capacitance of oxide, C_{ox} for SiC-based sample is also higher than Si-based sample with 2147pF and 1731pF respectively. The higher C_{ox} value for SiC-based sample is caused by higher κ-value and reduced of IL thickness. Other than that, the J-E characteristics measurement shows that SiC-based and Si-based sample have same leakage current density, J at 10^{-6} Acm^{-2} (Wong & Cheong, 2013).

Table 2.1 : Comparison of electrical properties of sputtered Zr between Si and Sic substrate (Wong & Cheong, 2013)

Measure-ments	**Properties**	**Unit**	**Si-based**	**SiC-based**
C-V	C_{ox}	pF	1731	2147
	Q_{eff}	cm^{-2}	$+4.50 \times 10^{11}$	-5.00×10^{13}
	STD	cm^{-2}	4.62×10^{11}	$+6.00 \times 10^{12}$
	D_{it} at (E_c-E)=0.15-0.25 eV	$eV^{-1}cm^{-2}$	Mid 10^{12}-10^{13}	1014
	D_{total}	cm^{-2}	7.00×10^{12}	3.7×10^{13}
	κ	-	21.82	49.68
	E_{HDB}	MV/cm	13.60	5.05
J-E	J	Acm^{-2}	10^{-6}	10^{-6}
	ϕ_B	eV	1.33	1.67

2.5 Conduction Mechanisms in Dielectric Films

Conduction mechanism in dielectric film plays an important role to identify types of breakdown that can happen to a device when a certain voltage is applied. Conduction mechanisms in dielectric films are divided into two categories. The first mechanism is electrode-limited conduction mechanism. The second mechanism is bulk-limited conduction mechanism as shown in Figure 2.2. The electrode-limited conduction

mechanism consists of Schottky emission, Fowler-Nordheim (FN) tunneling, Thermionic-field emission and Direct Tunneling. The electrode-limited conduction mechanism depends on the electrical properties at the electrode-dielectric interface. Whereas, bulk-electrode limited conduction mechanism consists of Poole-Frenkel emission, Hopping conduction, Ohmic conduction, Space-charge-limited conduction, Ionic conduction and Grain-boundary-limited conduction. This type of conduction mechanism depends on the electrical properties of the dielectric (Chiu, 2014).

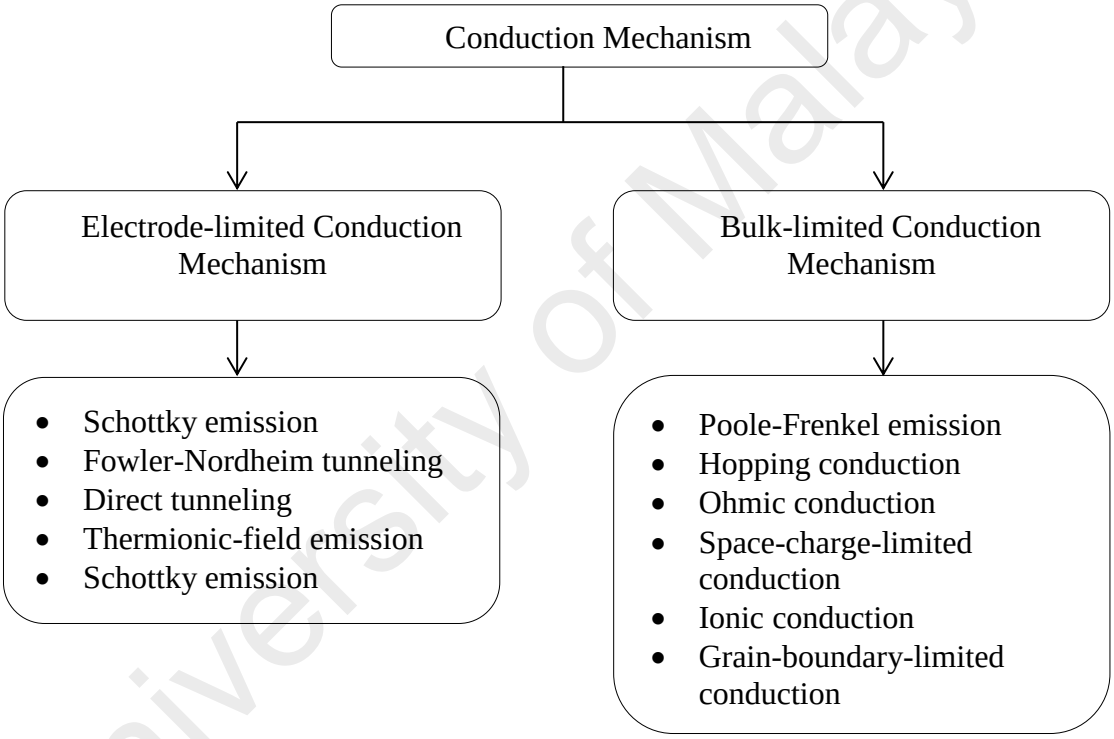

Figure 2.2 : Conduction mechanisms in dielectrics (Chiu, 2014)

Lampert (1956) stated that low density of free carriers which leads to the production of charge unbalanced by electric fields are caused by impurity and defect states in insulators. The following injection of electrons into the oxide which caused the unbalance charges in the oxide to form a space charge region which will limit further

injection into the oxide. The space-charge-limited conduction (SCLC) increases as the localized oxide and oxide-semiconductor interface trap density increases.

Following the SCLC theory by Lampert, at low gate voltage, the current density voltage (J-V) characteristic are constricted in the logarithm of J-V curve (Lampert, 1956; Cheong, Moon, Kim, Bahng, & Kim, 2008; Chiu, Chou, & Lee, 2005a). The characteristics are controlled by three limiting mechanisms which are Ohm's Law, trap-filled-limit (TFL) conduction and lastly Child's Law. The three types of conduction mechanisms can be mathematically modeled as follows:

$$J_{ohm} = \frac{qn_o \mu V_g}{t_{ox}} \tag{2.1}$$

$$J_{TFL} = B \frac{{V_g}^{l+1}}{{t_{ox}}^{2l+1}} \tag{2.2}$$

$$J_{Child} = \frac{9\mu\kappa {V_g}^2}{8{t_{ox}}^3} \tag{2.3}$$

Where,

n_o : concentration of free charge carriers in thermal equilibrium

μ : electronic mobility in the oxide

κ : dielectric constant of the oxide

B : l-dependent parameter l = (T_C/T), T_C is a characteristic temperature related to trap distribution

T : absolute temperature

J : current density of each type of conduction mechanisms which are due to Ohm's Law, TFL conduction and Child's Law respectively

2.5.1 Ohm's Law

Space charge limited conduction mechanism is also a well-known current mechanism that is frequently used to explain current conduction in an insulator and a semiconductor. The free carrier concentration can be increased under an applied field due to the injected carriers in the vicinity of a junction created by several materials (Ng, 2002). The space charge limited conduction is said to occur when the injected carrier concentration is larger than its thermal equilibrium value thus causing leakage of the current.

Ohmic contact between the semiconductor and oxide is formed when positive gate voltage is applied on the gate electrode which caused electrons to be accumulated as the majority carriers in n-type. This has resulted in higher accumulated electrons density than the free carrier density in the oxide, therefore, initiates injection of more electrons into the oxide.

The injection of electrons into the oxide happens at an extremely low voltage due to the density of free carrier in the oxide being extremely low than the density of the accumulated electrons in the forward-biased semiconductor. This is to say that before the electrons tunnels through the oxide at high voltage, they will be forced into the oxide at ultralow gate voltage (Wong & Cheong, 2011).

In order to observe the Ohmic conduction mechanism in the oxide, graph of typical logarithm J-V is used. The (J-V) plot is fitted with Ohm's Law where current density, J is proportional to and gate voltage, V_g ($J \alpha V_g$) (Wong & Cheong, 2011). The gradient of the slope, S must be equal to 1 to be ideal and obeying Ohm's Law (Lampert, 1956; Cheong et al. 2008).

2.5.2 Trap-Filled-Limit and Child's Law

The trap-filled limit (TFL) conduction is the condition for the transition to the trap-free J-V characteristics from the trapped J-V. It is visualized as the subsequently injected carriers will be free to move in the dielectric films after all traps are filled up. This will cause subthreshold (V_{TFL}) to set on this transition and eventually the current will jump rapidly from its low trap-limited value to a high trap free space-charge-limited current. V_{TFL} is the required voltage to fill the traps (Chiu, 2014).

In the fitting of J-V_g plot, as the electric field continue to increase, the oxide experiences TFL conduction process. The gradient, n of (J-V_g) plot is around $n \approx 2$. The value of n depends on the thickness of interfacial layer (IL). As the thickness of IL decreases, the n value decreases (Wong & Cheong, 2011). The reduction value of n value shows that the density of the oxide and oxide-semiconductor interface traps is also reduced. Therefore, this means that higher n value is not desirable.

Child's law is also one of the conduction mechanisms that occur at ultralow applied voltage. This conduction will occur in the case of a very strong injection of carriers that all traps are filled and then become the space-charge-limited (Child's Law). When the traps get gradually saturated, further injection of free carriers in the dielectric is limited because the current is fully controlled by the space charge (Chiu, 2014).

2.6 Poole-Frenkel Emission

According to Frenkel (1938), Poole-Frenkel (PF) effect is a well-known conduction mechanism that is frequently used to describe current flow in a dielectric or semiconductor. The PF effect mechanism is the thermal emission of charge carriers from Coulombic traps in the bulk of a material enhanced by an electric field (Harrell, 1994). The height of the barrier on one side of the trap decreased when an electric field

is applied. This decrease in the height of the barrier increases the electron's probability of escaping from the trap.

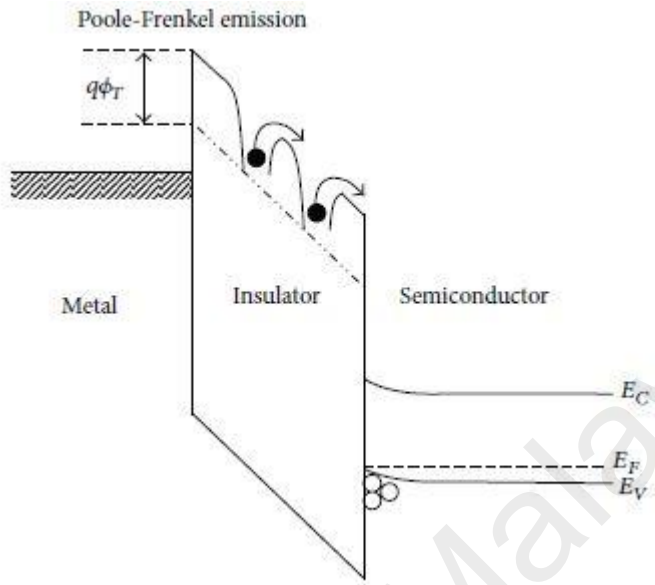

Figure 2.3: Schematic drawing of energy band diagram of Poole-Frenkel emission (Chiu, 2014)

Thermal excitation of electrons emission from traps into the conduction band of dielectric is called Poole-Frenkel emission conduction. This mechanism is also called as internal Schottky emission since they are very similar to each other. The mechanism occurs when an electron is trapped in a trapping center causing the Coulomb potential energy across the dielectric film to be reduced by an applied electric field. As shown in the schematic of P-F emission energy band diagram in Figure 2.3, the probability of an electron to be thermally excited out of the trap into the conduction band of the dielectric increases when the potential energy is reduced (Chiu, 2014). As stated by Chiu et al. (2005b), PF emission conduction was identified at low electric fields ($E \leq 0.6$ MV/cm).

The Poole-Frenkel emission conduction mechanisms can be modeled as in Equation 2.4

$$J_{PF} = (qN_c\mu)Eexp\{-q[\phi_t - (qE/\pi k_r\varepsilon_o)^{\frac{1}{2}}]\}/kT \quad (2.4)$$

Where,

μ : electronic mobility in the oxide

k : dielectric constant of the oxide

T : absolute temperature

J : current density of Poole-Frenkel emission

N_c : density of states in the conduction band

ϕ_t : trap energy level in the oxide

E : electric field across the dielectric

q : electronic charge

ε_o : permittivity in vacuum

CHAPTER 3: METHODOLOGY

3.1 Introduction

This chapter describes the materials and methodology. Figure 3.1 represents an overview of this project research. This chapter consists of three main parts:

i. Type of materials used

ii. Fabrication process and experimental procedures

iii. Characterization of electrical properties

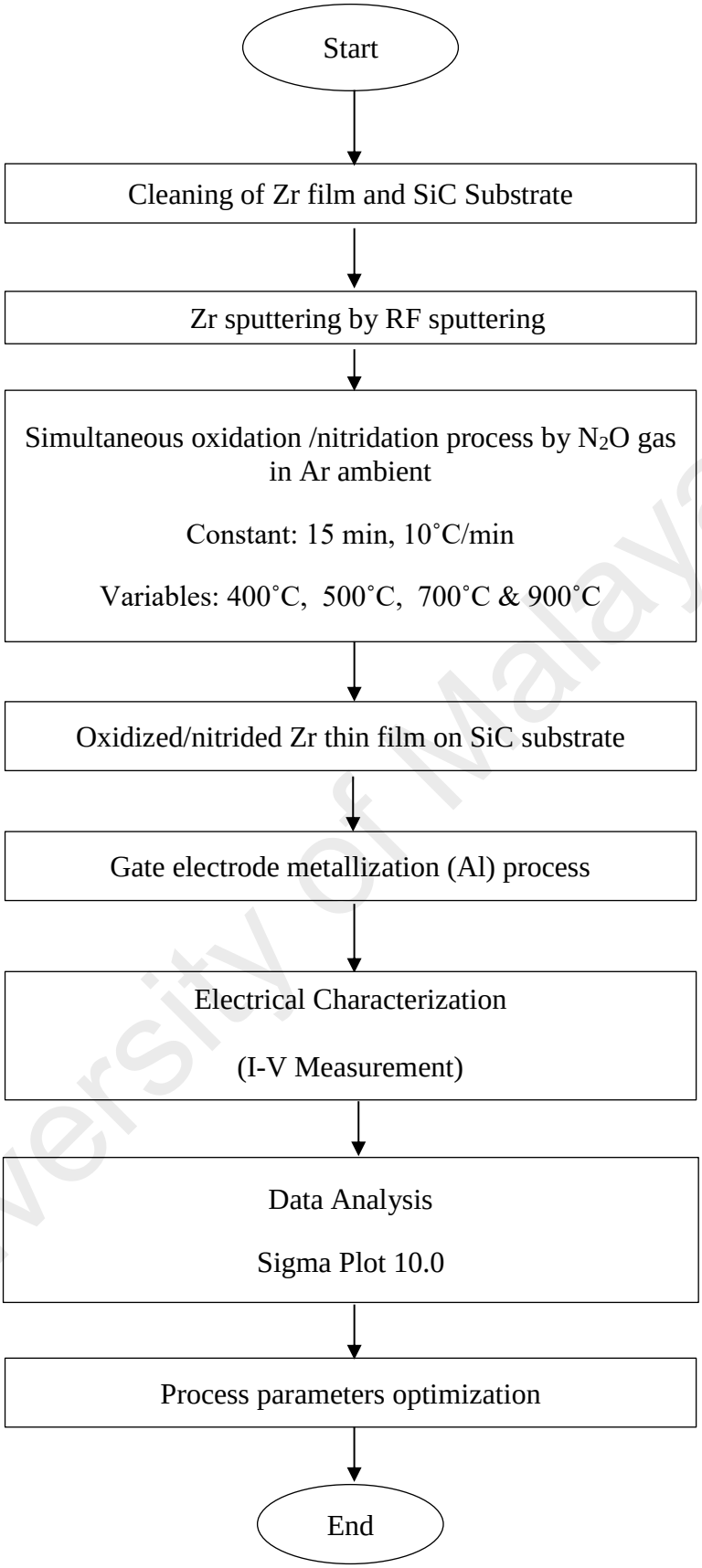

Figure 3.1: An.overview of project

3.2 Type of Materials Used

3.2.1 Substrate Material

The starting substrate used precut Si-faced SiC wafer with (001) orientation, 4.09˚-off axis, 0.020 Ωcm resistivity and 1μm thickness of n-type epitaxial layer doped with nitrogen at concentration of (1-4) $x10^{16}$ cm^{-3} were purchased commercially from CREE Inc. (USA).

3.2.2 Material used in SiC substrate dip-cleaning process

The chemicals used for dip cleaning process are hydrofluoric acid. (HF) solution with ratio (1:50 HF: H_2O) and deionized (DI) water.

3.2.3 Materials used in Zr and Al sputtering process

Zr and Al metallic layer are sputtered on SiC substrate by using TF 450 PVD radio frequencies (RF) sputtering system. Zr target, Al target and argon (Ar) gas were used during the sputtering and metallization process.

3.2.4 Materials used in thermal oxidation/nitridation process

The main material involved in simultaneous oxidation/nitridation process is nitrous oxide, N_2O gas with a flow rate of 150 mL/min for 15 min. This process is performed in a furnace with Ar gas as the ambient gas during heating and cooling process. Table 3.1 is the details of gases used in simultaneous oxidation/nitridation process.

Table 3.1 Gases used in simultaneous.oxidation and nitridation process

No	Material	Specifications
1	N_2O	Purity: 99.9%
2	Ar	Purity: 99.9%

3.2.5 Materials used in electrical properties characterization process

Aluminum (Al) film with thickness of 100nm was deposited on top of the film and at the back of the SiC substrate each.

The Al film deposited on top of the film acts as the Al-gate MOS capacitor. The area of Al-gate MOS capacitor on top of the film is defined photolithographically at 9×10^{-4} cm^2 with length and width of 0.03 cm, respectively. While the Al film that was deposited at the back of substrate was to obtain on Ohmic back contact.

High frequency of 1MHz capacitance-voltage(C-V) was conducted by a computer-controlled Agilent HP4284 LCR meter while current-voltage (I-V) measurements were conducted by HP4155-6C semiconductor parameter analyzer (SPA), respectively. The temperature-dependence of leakage currents was performed in a closed vacuum chamber at temperatures ranged between 400˚C and 900˚C.

3.3 Fabrication and experimental procedures

3.3.1 SiC substrate dip-cleaning process

The SiC wafer is cut into 4 samples with size of 1 cm x 1 cm for each sample. The samples were then going for dip-cleaning process to obtain the impurity-free samples. Two different beakers are prepared with HF acid solution and DI water. Then, a sample is soaked into HF acid solution and DI water for about 10 seconds for each solution. Then, by using paper towel, the sample is then being wiped clean. The dip-cleaning process is repeated for all samples.

3.3.2 Zr thin film sputtering process on SiC substrate

Metallic Zr layer is sputtered on the samples from the Zr target by RF sputtering process with room temperature or Ar gas flow. The power supply, pressure in the chamber and Ar gas flow rate are set to 170 W, 3×10^{-5} mbar and 25 ml/min.

3.3.3 Thermal oxidation/nitridation of sputtered Zr thin film on SiC substrate

The thermal oxidation and nitridation was done out simultaneously by nitrous oxide N_2O gas. The samples were heated up in Ar gas with heating rate 10°C/min to a set of four different temperatures which are 400, 500, 700 and 900°C. The N_2O gas is introduced into the quartz tube inside the horizontal tube furnace when the set temperature reached. The N_2O gas used for simultaneous oxidation and nitridation was flown for 15 min at 150ml/min of flow rate. After 15 minutes, the samples are cooled down to room temperature before they are taken out from the furnace in Ar ambient. The oxidized/nitrided samples are then proceeded with the electrical characterization

process. The fabrication procedures of the gate dielectric thin film are illustrated in Figure 3.2.

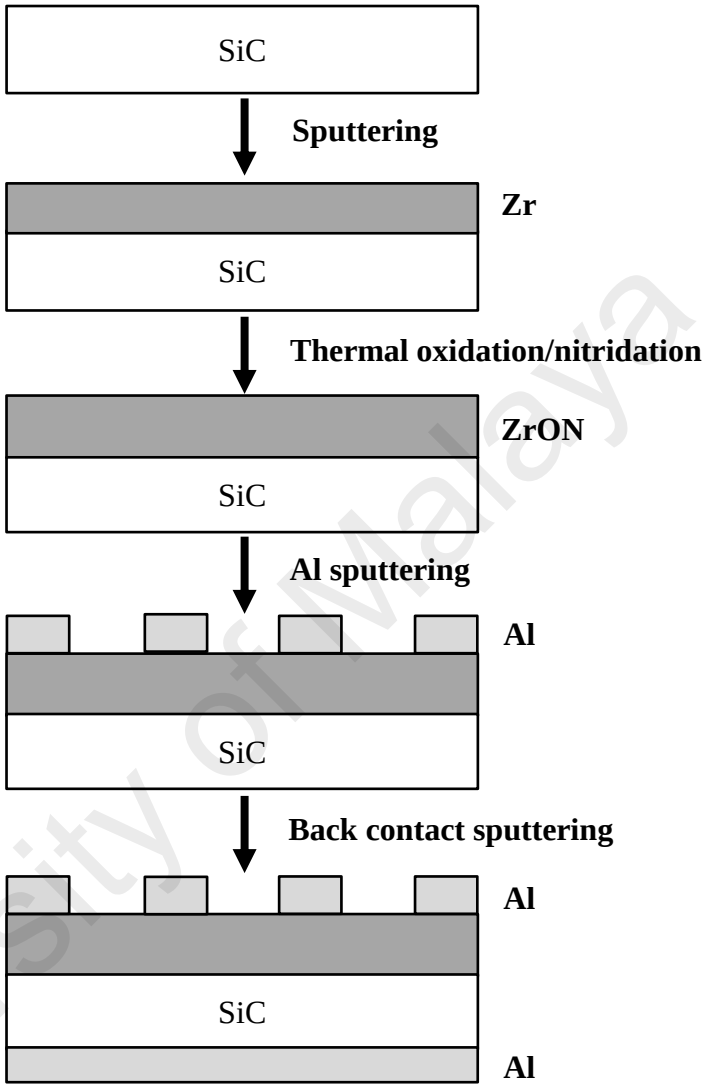

Figure 3.2: Simple illustration of methodology in preparing samples of this research project

3.3.4 Fabricating Al-gate MOS capacitor via sputtering process

For electrical characterization, the oxidized/nitrided Zr thin film on SiC substrate samples were used to fabricate Al-gate MOS capacitors. An Al layer with 100 nm thickness was layered on top and bottom of the sample by deposition technique with

similar steps of Zr sputtering process. The base pressure, working pressure, distance between substrate, RF power, and the target and argon gas flow rate were set to 1.5 x 10^{-3} Pa ,3 x 10^{-3} Pa, 20 cm , 170 W and 25 cm^3/min respectively. Pre-sputtering was done for about 3 minutes, to eliminate the native oxide from the Al target surface. After pre-sputtering completed, Al layer was placed on the top of the film and at the back of the substrate by sputtering process.

3.3.5 I-V measurement

The current-voltage (I-V) measurements were done using BPW-800 8" probe station with a Keithley 4200 semiconductor characterization system (SCS). The frequency is set to 50 Hz and sweep range were set to 0-20 V.

3.4 Characterization of Electrical Properties

The electrical properties of the oxide can be characterized and modeled according to conduction mechanisms by using the SigmaPlot 10.0 software to plot the graphs and analysis of the modeling. The applied voltage and current data obtained from I-V measurement was inserted and processed by using the software.

3.4.1 Characterization of Current Density and Electric Field

To characterize the current density and electric field, the graph of current density(J) against electric field (E) was plotted by multiple scatter plot type. The I-V measurement data obtained was changed to leakage current density against electrical breakdown field (J-E). From the J-E plot, the current density at various fields can be obtained. The E value was determined from equation 3.1.

$$E = (V_g - V_{fb})/t_{ox} \tag{3.1}$$

Where V_{fb} is the flat band voltage, V_g is the gate voltage, and t_{ox} is the thickness of oxide (Goh, Haseeb, & Wong, 2016; Wong & Cheong, 2012). In all characterized MOS

capacitors in higher N_2O concentrations, there are two steps of oxide breakdowns were produced. The first is soft breakdown and the other is hard breakdown (Wong & Cheong, 2011, 2012, 2013).

3.4.2 Space-Charged-Limited Conduction (SCLC) Mechanism-Ohm's Law Analysis

To analyse leakage current density according to SCLC by Ohm's law, the graph of J-V_g is plotted by using the set of data obtained with Ohm's law model fitting based on Equation 2.1. The leakage current density for Ohm's law behavior is analysed at the low applied voltage.

The regression line of the plot is maintained with r^2 between 0.90-0.99 to ensure the model fits the data well. The Ohm's law behavior is observed from the J-V_g plot by obtaining the gradient of the regression line. The gradient of each sample of different oxidation and nitridation temperature was obtained and discussed in section 4.2.

3.4.3 Poole-Frenkel Emission Conduction Mechanism Analysis

To analyse PF emission leakage current density according to PF emission model given by Equation 2.4, the graph of ln (J/E)-$E^{1/2}$ is plotted and fitted with J_{PF} model with r^2 ranges between 0.90-0.98. The leakage current density for PF emission model is analysed at the higher applied voltage before electrical breakdown reached.

The slope of the regression line indicates the dynamic dielectric constant, k_r. For each samples, the values of k_r are obtained and discussed in section 4.3.

CHAPTER 4: RESULTS AND DISCUSSIONS

4.1 Characteristics of Current Density and Electric Field

The relation between density of leakage currents and electric field (J-E) was interpreted to analyse the charge conduction mechanisms of sputtered Zr on SiC that was being thermally oxidized and nitrided simultaneously for 15 minutes at four different temperatures (400˚C-900˚C).The leakage currents of each of the sample were measured. The current density-electric field data were obtained from current-voltage (I-V) measurements that was obtained from computer controlled SPA system. Based on Schroder (2006), the electric field, E value was estimated by Equation 3.1.

The temperature-dependence J-E characteristics for 15-min simultaneously oxidized and nitrided sample are plotted by using the set of data obtained from the system. The data was inserted into SigmaPlot 10.0 and graph of leakage current density against electric field was plotted as shown in Figure 4.1.

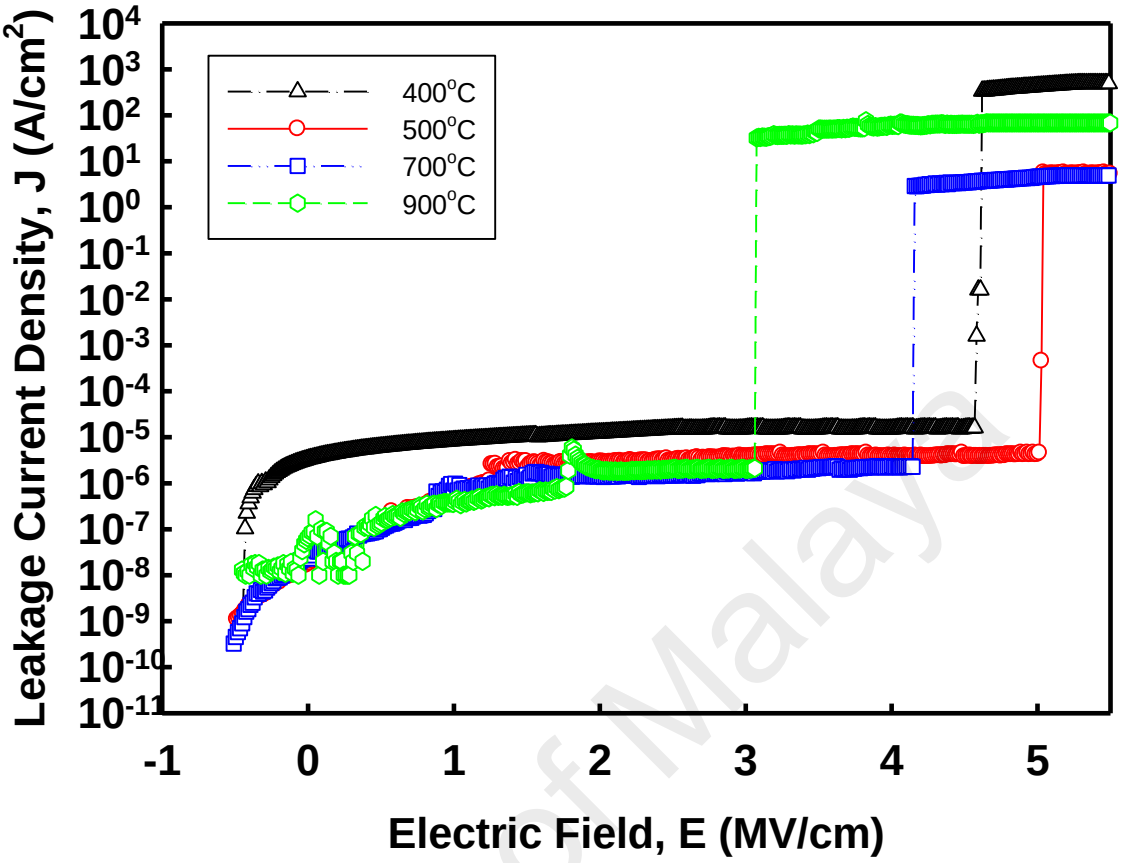

Figure 4.1: J-E Characteristics of samples oxidized and nitrided for 15 minutes duration at various temperatures (400˚C-900˚C)

Based on Figure 4.1 it is observed that the gate oxides experienced dielectric breakdown (E_B) due to instantaneous increment of leakage current density at a specific field. This electric field is where the instantaneous increase occurs is where the permanent oxide breakdown occurs. As the temperature increase, the dielectric breakdown decreased.

The E_B recorded for sample oxidized/nitrided at 400˚C, 500˚C, 700˚C and 900˚C are 4.59 MV/cm, 5.05 MV/cm, 4.16 MV/cm and -0.07 MV/cm. Therefore, it is clearly shown that among four of investigated sample, sample oxidized/nitride at 500˚C has

highest E_B followed by 400˚C sample, 700˚C sample and the lowest is demonstrated by the sample produced at 900˚C.

Through the study of current transport mechanism through oxide, the leakage path causing the electric field breakdown s can be identified. Variation in E_B values can be related to previous study done by Wong and Cheong (2012). The variation can be related to the interfacial layer, thickness of bulk oxynitride, and/or the combined oxides. Based on the structural characterization in the previous work, the cross-sectional EFTEM image of sample oxidized/nitride at 500˚C appears have the smoothest surface compared to the other three samples.

4.2 Space-Charged-Limited Conduction (SCLC) Mechanism-Ohm's Law

Based on the I-V measurement, graph of leakage current density, J against applied voltage, Vg is plotted to evaluate space-charge-limited conduction in the oxide.

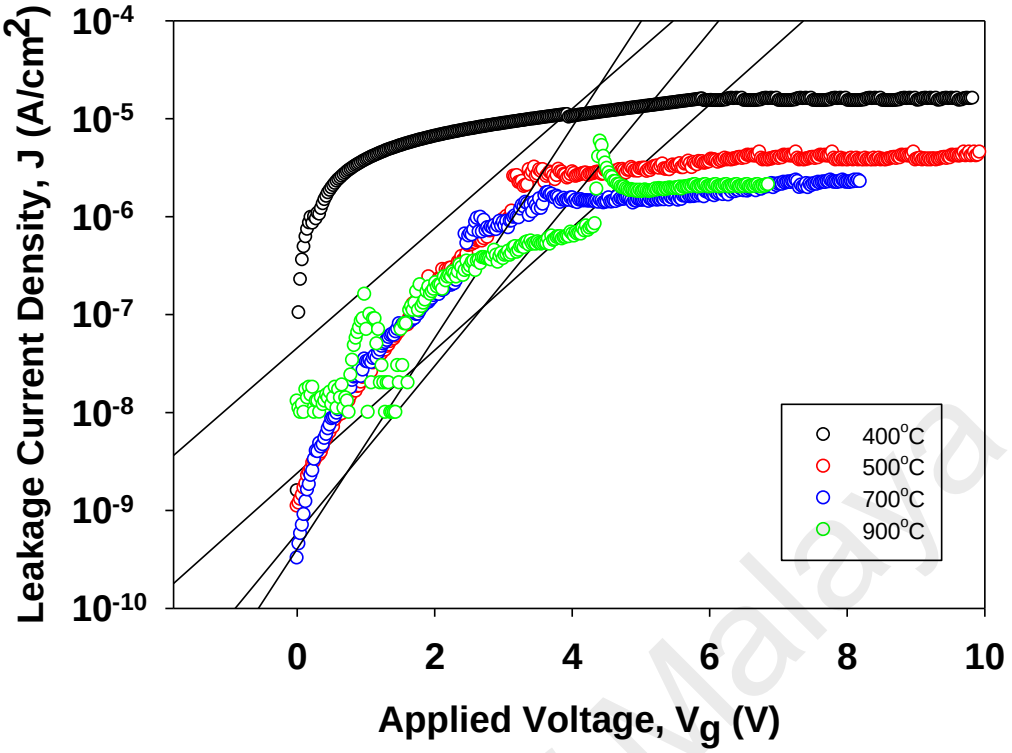

Figure 4.2: J-V_g plot of 15-min oxidation and nitridation at various temperatures (400˚C-900˚C)

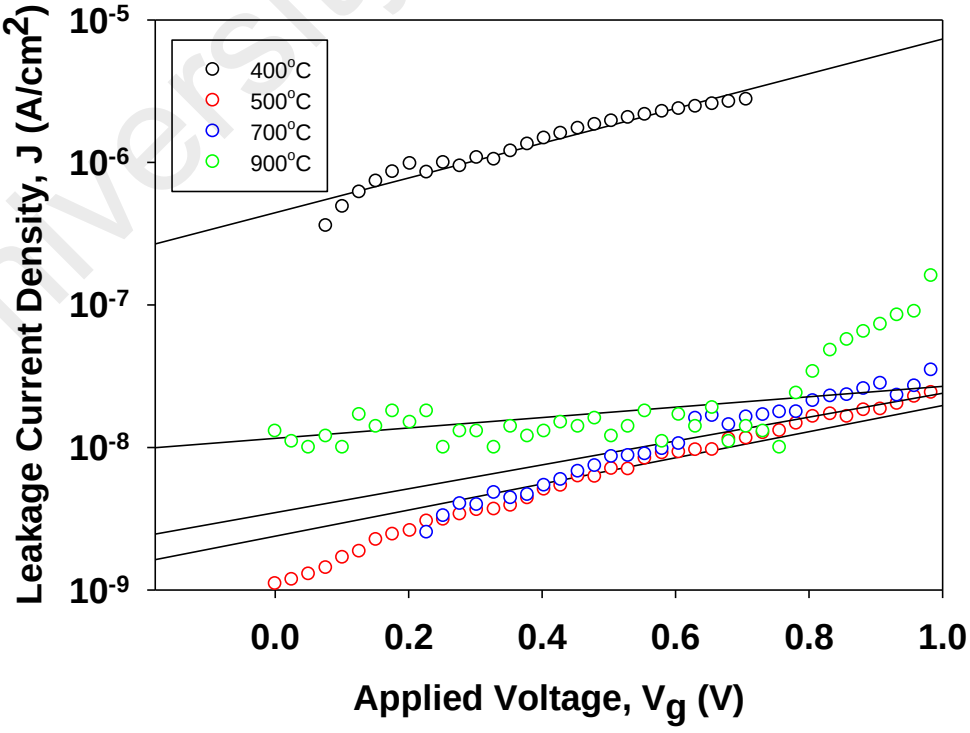

Figure 4.3 : J-V_g with Ohm's law fitted modeling plot of 15-min oxidation and nitridation at various temperatures (400˚C-900˚C)

Figure 4.2 shows the J-V_g plot for overall data of all four samples at various temperatures. Based on the J-V_g plot, we can identify space-charge-limited current due to injection of electrons at an ohmic contact. Figure 4.3 was plot with selected range of data from Figure 4.2 fitted with Ohm's law. Ohm's law stated that the current density is increased when the applied voltage increase (J α Vg). The regression line was plotted in order to determine the gradient of the slope to study the Ohm's Law behaviour at low applied voltage. According to Ohm's Law, the gradient, S of the slope must be equal to 1 for charge conduction to obey Ohm's law.

The gradient of the graph for all four samples oxidized/nitrided at 400°C, 500°C, 700°C and 900°C are obtained from SigmaPlot 10.0. The values of gradients obtained are tabulated as in Table 4.1 and plotted graphically in Figure 4.4.

Table 4.1 : Gradient of J-V_g plot fitted with Ohm's Law as a function of oxidation and nitridation temperature

Oxidation/Nitridation Temperature	Gradient, S
400˚C	1.21
500˚C	0.91
700˚C	0.83
900˚C	0.36

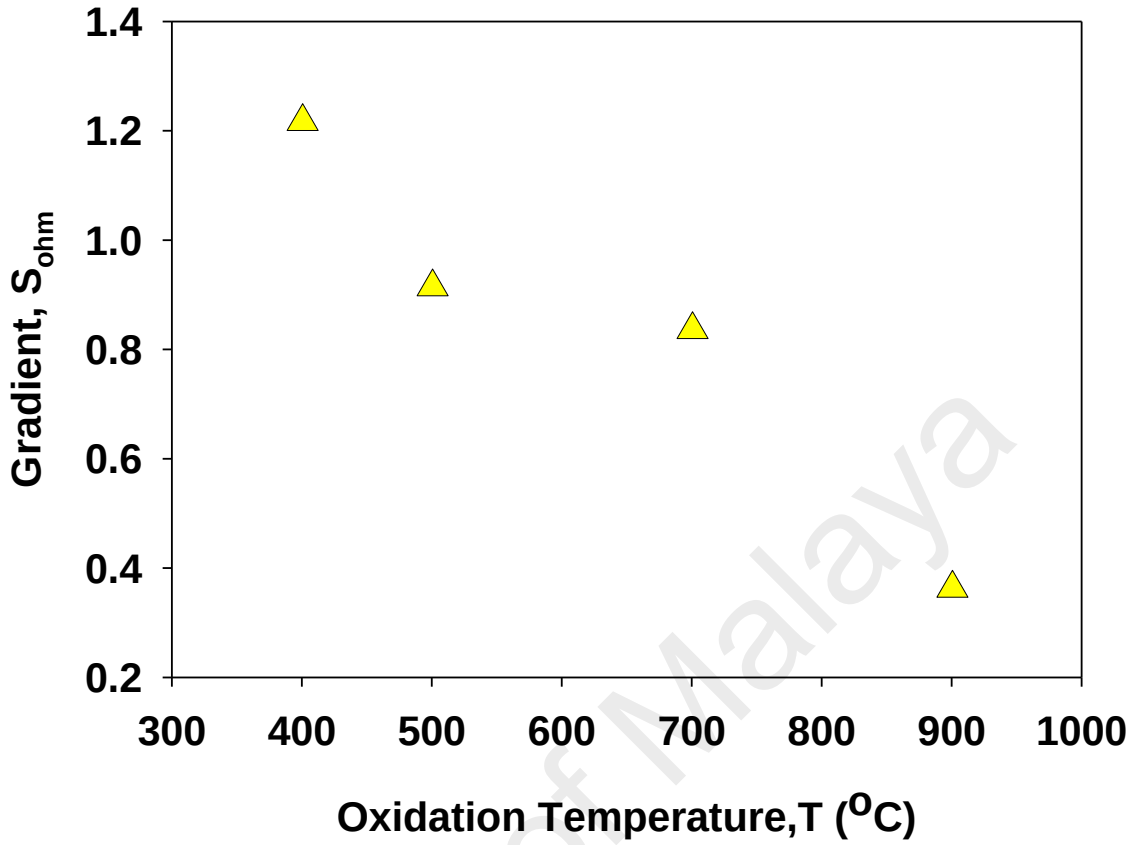

Figure 4.4 : Gradient of J-Vg plot fitted with Ohm's law as a function of oxidation/nitridation temperature

The gradient, S values show that samples oxidized/nitrided at 400˚C, 500˚C, 700˚C and 900˚C has gradient value of 1.21, 0.91, 0.83 and 0.36. The gradients for sample oxidized/nitride at 400˚C, 500˚C and 700˚C are close and comparable to 1, therefore it can be concluded that they obey Ohm's law charge conduction.

While, sample oxidized/nitride at 400˚C which have the gradient value of 0.36 which is very far from 1 show that it does not obey Ohm's law. Based on Ohm's law, it states that

$$V = IR$$

where V is voltage, I is current and R is resistance. In the case of sample oxidized/nitrided at 900˚C, it may be because of high resistance in the oxide. Based on study that was done on ZrON/SiC system, it is observed that as the oxidation and nitridation temperature increased, the IL formed increases from 1.44 to 4.20nm (Wong & Cheong, 2013). This supports the results obtained that increase in oxidation and nitridation temperature increases the resistance caused by increase in IL thickness. Therefore, the increase in IL thickness may be the cause of high resistance in the sample oxidized/nitrided at 900˚C.

4.3 Poole-Frenkel Conduction Mechanism

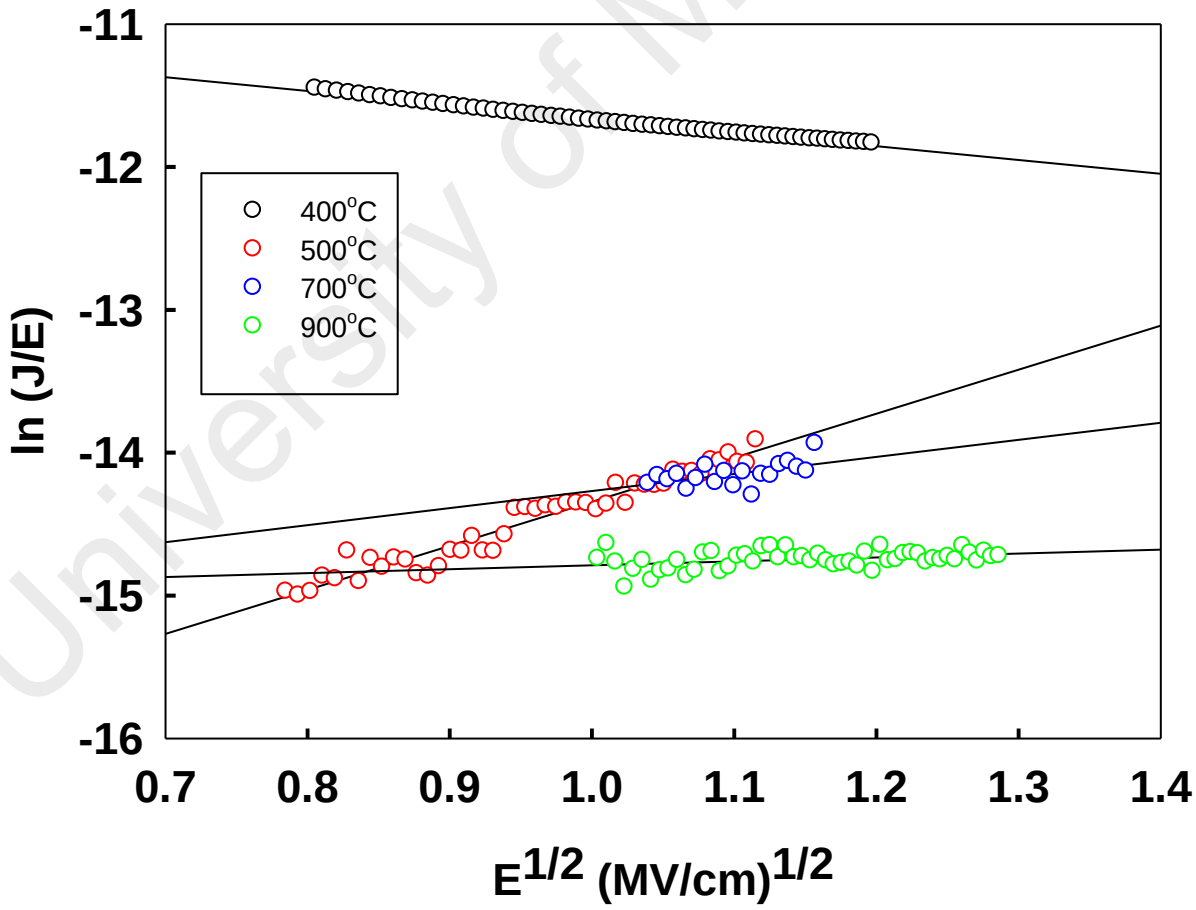

Figure 4.5 : ln (J/E)-$E^{1/2}$ plot of 15-min oxidation and nitridation at various temperatures (400˚C-900˚C)

To analyse the Poole-Frenkel conduction mechanism, current leakage at higher applied voltage is concerned. Figure 4.5 shows the PF plot at four different simultaneous oxidation and nitridation temperatures for 15-min. The slope of graph ln (J/E) against $E^{1/2}$ plot fitted with standard PF emission model is the value of dielectric constant, k_r (Wong & Cheong, 2011b). The values of gradient obtained are tabulated as in Table 4.6. The values of gradients are -0.96, 3.08, 1.20 and 0.27.

Table 4.2: Dynamic dielectric constant from gradient of ln (J/E)- $E^{1/2}$ plot fitted with Poole Frenkel emission as a function of oxidation and nitridation temperature

Oxidation/Nitridation Temperature	Dynamic Dielectric Constant, k_r
400˚C	-0.96
500˚C	3.08
700˚C	1.20
900˚C	0.27

The value of dielectric constant obtained from data analysis is comparable with the standard PF emission model since they were fitted by linear extrapolation with r^2 of 0.90-0.99. This indicates that the data are well-fitted with the standard PF emission model (Equation 2.4). The value of k_r obtained reduces as the oxidation/nitridation temperature increases. This pattern is supported by previous study done on the same dielectric material by Wong & Cheong (2011b) which was the ZrON/Si system.

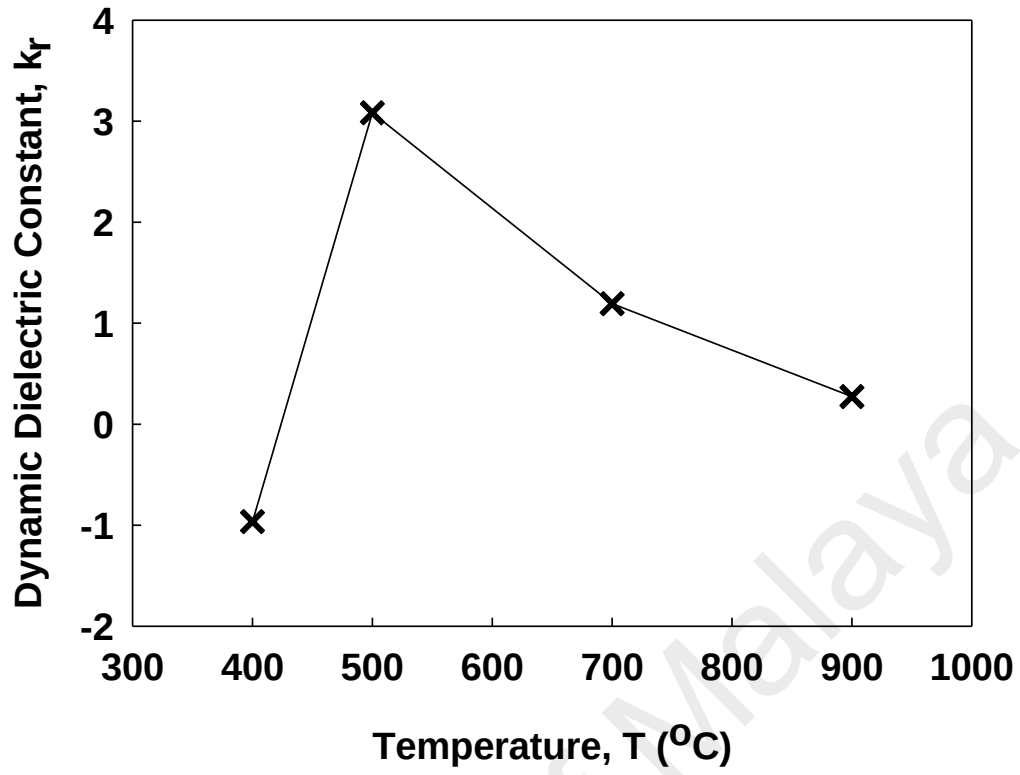

Figure 4.6: Dynamic dielectric constant from PF emission plot as a function of measured oxidation and nitridation temperatures (400˚C-900˚C)

The value of k_r obtained shows that it reduces as the temperature of oxidation and nitridation increases. This is because as the temperature increases, the IL will increase in thickness and thus, reduces the dielectric constant value (Wong & Cheong, 2011b). The value of k_r for sample oxidized/nitride at 400˚C is negative may be because of some thermal excitation of electrons may have occurred which has caused some electrons to be emitted from the trap and it is due to a combination of PF emission and FN tunneling. This can be justified from the J-E plot where the leakage current were still existence during the process of breaking down before reaching FN tunneling.

Based on above analyses, the Ohm's law SCL and PF emission conduction mechanism at various temperatures (400˚C-900˚C) are presented in Table 4.3. The

conduction mechanism due to Ohm's law occurs at low electric field ranges from -0.4 to 0.05 MV/cm. On the other hand, conduction mechanism due to PF emission occurs at higher electric field ranges from 0.6 to 1.6 MV/cm and associated to the permanent oxide breakdown by high leakage current.

Table 4.3 : Summary of charge conduction mechanism and electric field for the ZrOn/SiC system

	Charge conduction mechanism occurring within electric field (MV/cm)	
Oxidation/Nitridation Temperature	**Ohm's law**	**Poole-Frenkel emission**
400˚C	-0.4 – -0.08	0.6 – 1.4
500˚C	-0.4 – -0.05	0.6 – 1.2
700˚C	-0.4 – 0.04	1.0 – 1.3
900˚C	-0.4 – 0.05	1.0 –1.6

CHAPTER 5: CONCLUSION

5.1 Summary

Both space charge limited conduction mechanisms and Poole-Frenkel emission of oxidized/nitrided Zr/SiC in N_2O ambient for different thermal oxidation/nitridation temperatures (400-900˚C) were presented in this study. Based on the Ohm's law fitting, it is found that sample oxidized/nitrided at 500˚C has the closest gradient to 1 for the slope of J-V_g plot. This means that the sample obeys Ohm's law conduction in low electric field.

Based on the electrical chracterization of the oxide evaluated by MOS structure,it is verified that sample oxidized/nitrided at 500˚C portrays the best result in Ohm's law conduction and Poole Frenkel emission because it has the highest E_B of 5.05 MV/cm at 10^{-6} A/cm^2. The high electrical breakdown field shows that oxide have high threshold voltage and can withstand longer before breakdown occur compared to the other samples at 400˚C, 700˚C and 900˚C. The high electrical breakdown field was contributed by the reduction of interface trap density, total interface trap density, effective oxide charge and increment barrier height between conduction band edge of the oxide layer and the semiconductor (Wong & Cheong, 2011b).

In conclusion, according to the charge conduction mechanisms distribution plot for sputtered Zr on SiC oxidized and nitrided at 4 different temperatures (400˚C-900˚C), the leakage current due to Ohm's law space-charge limited conduction occurs at low electric field. While at higher electric field, PF emission occur before the oxide undergoes and FN tunneling until oxide permanently breakdown.

5.2 Recommendations for Future Project

As previously mentioned in Chapter 2, there are two types of conduction mechanism which are electrode-limited conduction mechanism and bulk-limited conduction mechanism. This study only focuses on space-charge-limited conduction by Ohm's Law and Poole-Frenkel emission conduction which are bulk-limited conduction mechanism. In future, electrode limited conduction mechanism such as Schottky emission and Fowler-Nordheim tunneling can be studied and the electrical properties can compared with the bulk-limited conduction mechanism in ZrON/SiC system.

Other than that, other type of semiconductor material can be studied. In this study SiC is chosen as the semiconductor material to be paired with Zr film since the technology is more mature and developed. However, there are variety of wide bandgap semiconductor can be used to replace SiC such as GaN and diamond. These two material exhibit properties that are comparable to SiC in terms of its high bandgap energy and breakdown field. Therefore extensive research can be conducted to further investigate the potential of these material as a promising material as advanced MOS device.

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