LOW-POWER CMOS CROSS-COUPLED DIFFERENTIAL-DRIVE RECTIFIER FOR AMBIENT RADIO FREQUENCY ENERGY HARVESTING SYSTEMS

GABRIEL CHONG SING LEUNG

FACULTY OF ENGINEERING
UNIVERSITY OF MALAYA
KUALA LUMPUR

2020

LOW-POWER CMOS CROSS-COUPLED DIFFERENTIAL-DRIVE RECTIFIER FOR AMBIENT RADIO FREQUENCY ENERGY HARVESTING SYSTEMS

GABRIEL CHONG SING LEUNG

THESIS SUBMITTED IN FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

FACULTY OF ENGINEERING
UNIVERSITY OF MALAYA
KUALA LUMPUR

2020

UNIVERSITY OF MALAYA

ORIGINAL LITERARY WORK DECLARATION

Name of Candidate: **Gabriel Chong Sing Leung**

Name of Degree: **Doctor of Philosophy**

Title of Project Paper/Research Report/Dissertation/Thesis ("this Work"):

Low-Power CMOS Cross-Coupled Differential-Drive Rectifier for Ambient Radio Frequency Energy Harvesting Systems

Field of Study: **Electronics (Engineering & Engineering Trades)**

I do solemnly and sincerely declare that:

(1) I am the sole author/writer of this Work;
(2) This Work is original;
(3) Any use of any work in which copyright exists was done by way of fair dealing and for permitted purposes and any excerpt or extract from, or reference to or reproduction of any copyright work has been disclosed expressly and sufficiently and the title of the Work and its authorship have been acknowledged in this Work;
(4) I do not have any actual knowledge nor do I ought reasonably to know that the making of this work constitutes an infringement of any copyright work;
(5) I hereby assign all and every rights in the copyright to this Work to the University of Malaya ("UM"), who henceforth shall be owner of the copyright in this Work and that any reproduction or use in any form or by any means whatsoever is prohibited without the written consent of UM having been first had and obtained;
(6) I am fully aware that if in the course of making this Work I have infringed any copyright whether intentionally or otherwise, I may be subject to legal action or any other action as may be determined by UM.

Candidate's Signature Date:

Subscribed and solemnly declared before,

Witness's Signature Date:

Name:

Designation:

LOW-POWER CMOS CROSS-COUPLED DIFFERENTIAL-DRIVE RECTIFIER FOR AMBIENT RADIO FREQUENCY ENERGY HARVESTING SYSTEMS

ABSTRACT

Wireless Sensor Node (WSN) for the Internet of Things (IoT) and Internet of Everything (IoE) will require harvesting low-power ambient Radio Frequency (RF) energy to achieve self-power capabilities, alleviating the need of batteries. The research title of "Low-Power CMOS Cross-Coupled Differential-Drive Rectifier for Ambient Radio Frequency Energy Harvesting Systems" relates to the design of integrated circuit (IC) rectifiers for low-power ambient RF energy harvesting (RFEH) in complementary-metal-oxide-semiconductor (CMOS) technology. The adoption of CMOS for the rectifier designs is to achieve small physical form factor, low-cost, and system-on-chip (SoC) integration. The rectifier is the main circuit in an ambient RFEH system to convert the scavenged RF power in alternating current (AC) into usable direct current (DC) for powering WSNs. The Cross-Coupled Differential-Drive (CCDD) rectifier is the selected choice in this thesis due to its high peak power conversion efficiency (PCE) and low sensitivity. However, the dynamic range (DR) efficiency of this topology restricts high-PCE-range performance due to the inherent low-power of ambient RF energy. The rectifier's ability to convert ambient RF power into usable DC level present a bottleneck in achieving high PCE across input RF power range. The intrinsic threshold voltage (V_{th}) of CMOS devices and reverse-leakage are the main causes of performance degradation of the rectifier. In this thesis, a novel mathematical model of a conventional CCDD architecture for ambient RFEH system in CMOS operating in subthreshold region is first proposed. This model fills the gap in the lack a model of a CCDD rectifier for ambient RFEH application. The proposed model was tested and validated through hardware fabricated in a 0.18-μm CMOS process. The model achieved an accuracy of above 90%

from an input RF power level from -20 dBm to 0 dBm with an accuracy of above 80% for an input RF power level up until 3 dBm. Subsequently, a new CCDD architecture based on the conventional CCDD rectifier with enhanced DR performance is proposed. The proposed CCDD architecture adopts a self-body-biasing technique to reduce the intrinsic V_{th} of the device and a gate-biasing technique to reduce the reverse-leakage current to improve the DR performance. Two design iterations of the proposed CCDD architecture were fabricated and characterized in a 0.13-μm CMOS process. The first proposed CCDD iteration (SCC-CCDD) achieved a peak PCE of 83.7% at an input power of -18.4 dBm for $R_{\mathrm{L}} = 100$ kΩ. Alternately, the SCC-CCDD achieved a DR range of 13 dB for a PCE above 40% and a DR of 8 dB for a PCE above 60%. Similarly, the second iteration (ICC-CCDD) achieved a peak PCE of 80.3% at an input power of -17 dBm, a DR of 14.5 dB for a PCE above 40% and a DR of 9 dB for a PCE above 60%. The proposed CCDD rectifier model and architecture contribute towards the development of integrated ambient RFEH system using low-cost CMOS technology. Research on full RFEH system modeling, system integration of the rectifier and investigation of wide technology implementation are potential future works.

Keywords: Ambient RF Energy Harvesting (RFEH), Cross-Coupled Differential-Drive (CCDD) Rectifier, Subthreshold Modelling, Power Conversion Efficiency (PCE), Dynamic Range (DR), CMOS Technology.

PENERUS LITAR CMOS KUASA RENDAH "CROSS-COUPLED DIFFERENTIAL-DRIVE" UNTUK SISTEM PENJANAAN TENAGA DARI AMBIEN FREKUENSI RADIO

ABSTRAK

Nod Sensor Tanpa Wayar (WSN) untuk Internet Perkara (IoT) dan Internet Segala-galanya (IoE) akan memerlukan penuaian tenaga frekuensi radio (RF) yang berkuasa rendah untuk mencapai keupayaan operasi bersendirian tanpa keperluan bateri. Gelaran penyelidikan "Penerus Litar CMOS Kuasa "Cross-Coupled Differential-Drive" Rendah Untuk Sistem Penjanaan Tenaga Dari Ambien Frekuensi Radio" berkaitan reka bentuk penerus litar bersepadu (IC) untuk tenaga rendah RF dicapai dengan teknologi pelengkap-logam-oksida-memonduktor (CMOS). Penggunaan teknologi CMOS adalah untuk mencapai faktor bentuk fizikal miniaturisasi, kos rendah, dan sistem integrasi (SoC). Penerus litar adalah litar utama dalam sistem penuaian tenaga ambien RF (RFEH) yang menukarkan kuasa RF dalam arus selari (AC) ke arus langsung (DC) yang boleh diguna untuk menghidupkan WSN. Penerus litar "Cross-Coupled Differential-Drive (CCDD)" dijadikan pilihan tesis ini kerana topologi ini mampu mencapai kecekapan penukaran kuasa tinggi (PCE) dan kepekaan yang rendah. Walau bagaimanapun, kecekapan julat operasi dinamik (DR) topologi ini mengehadkan prestasi tinggi "PCE-range" adalah disebabkan kuasa tenaga ambien RF yang rendah. Keupayaan penerus litar untuk menukarkan kuasa ambien RF kepada DC dengan mencapai PCE yang tinggi adalah satu cabaran. Voltan ambang intrinsik (V_{th}) dalam transistor CMOS dan arus kebocoran terbalik adalah punca-punca degradasi prestasi penerus litar. Dalam tesis ini, model matematik novel seni bina CCDD konvensional untuk sistem RFEH ambien dalam teknologi CMOS yang beroperasi di julat sub-ambang dicadangkan. Model ini menyumbang kepada model penerus CCDD untuk aplikasi RFEH ambien. Model yang dicadangkan telah diuji dan disahkan melalui perkakasan yang dibuat dalam proses

CMOS 0.18-μm. Model ini mencapai ketepatan lebih daripada 90% paras kuasa RF input dari -20 dBm hingga 0 dBm dan ketepatan lebih daripada 80% untuk tahap RF input sehingga 3 dBm. Seterusnya, seni bina CCDD yang baru berdasarkan penerus litar CCDD konvensional dengan prestasi DR yang dipertingkatkan dicadangkan. Cadangan seni bina CCDD mengamalkan teknik bias diri untuk mengurangkan V_{th} intrinsik peranti dan teknik bias pintu untuk mengurangkan arus kebocoran terbalik meningkatkan prestasi DR. Dua reka bentuk lelaran senibina CCDD yang dicadangkan telah direka dan dicirikan dalam proses CMOS 0.13-μm. Cadangan CCDD pertama (SCC-CCDD) mencapai PCE puncak sebanyak 83.7% pada daya RF input -18.4 dBm untuk R_{L} = 100 kΩ. Disamping itu, SCC-CCDD mencapai julat DR 13 dB untuk PCE lebih daripada 40% dan DR 8 dB untuk PCE lebih daripada 60%. Begitu juga, lelaran kedua (ICC-CCDD) mencapai PCE puncak sebanyak 80.3% pada kuasa RF input -17 dBm, DR 14.5 dB untuk PCE melebihi 40% dan DR 9 dB untuk PCE melebihi 60%. Model penhadkod CCDD dan arkitek yang dicadangkan menyumbang kepada pembangunan sistem RFEH sekitar bersepadu dengan teknologi CMOS kos rendah. Penyelidikan mengenai pemodelan sistem RFEH, penyepaduan sistem penerus dan penyiasatan pelaksanaan teknologi luas adalah kerja masa depan yang berpotensi.

Kata Kunci: Penuaian Tenaga RF Ambien, Penerus Kuasa Rendah Cross-Coupled Differential-Drive (CCDD), Pemodelan Sub-Ambang, Kecekapan Penukaran Kuasa (PCE), Julat Dinamik (DR), Teknologi CMOS.

ACKNOWLEDGEMENTS

I am grateful to God for His Grace and Sovereign Will in which He has directed my life towards the journey of pursuing a PhD. Second, I am grateful to my family for their unending support to embark on my PhD studies. Thank you mom and sister for your patience and kindness in supporting me throughout my entire studies.

I would also like to thank University of Malaya (UM) which supported me in the pursuit of knowledge through my research work at the university. Thank you Assoc. Prof. Dr. Ir. Harikrishnan Ramiah and Dr. Wong Wei Ru for your supervision in guiding me through my academic journey. Thank you to my fellow lab mates at the RF, Analog and Digital Research Group for the knowledge, discussion and support throughout the entire journey.

To the research group at State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, China, I would like to thank Dr. Jun Yin (Kevin), Prof. Pui-In Mak (Elvis) and Prof. Rui P. Martins whom had provided guidance with their expertise in the subject matter and providing critical feedback in publication related works. I would also like to extend my gratitude to Dr. Jagadheswaran Rajendran from Collaborative Microelectronic Design Excellence Center (CEDEC) at Universiti Sains Malaysia (USM) for his co-supervision in measurement of the IC chips.

TABLE OF CONTENTS

Abstract ..... **iii**

Abstrak ..... **v**

Acknowledgements vii

Table of Contents viii

List of Figures xi

List of Tables xiii

List of Symbols and Abbreviations xiv

List of Appendixes xvii

CHAPTER 1: INTRODUCTION **1**

1.1 Background and Motivation 1

1.2 Problem Statement 3

1.3 Objectives of the Study 5

1.4 Research Methodology 6

1.5 Contributions of the Research Work 7

1.6 Thesis Outline 8

CHAPTER 2: LITERATURE REVIEW **9**

2.1 Chapter Overview 9

2.2 RF Energy 9

2.2.1 Background 9

2.2.2 Characteristics of Ambient RF Energy 10

2.2.2.1 Availability 10

2.2.2.2 Frequencies 12

2.2.2.3 Power Density 12

2.3 Review of Integrated Low-Power Rectifiers 14
2.3.1 Power Conversion Efficiency (PCE) Curve 14
2.3.2 Dickson Architecture 15
2.3.2.1 Threshold Voltage (V_{th}) Cancellation or Reduction 16
2.3.2.2 Threshold Voltage (V_{th}) Compensation Scheme 18
2.3.2.3 Bulk-Biasing Scheme 21
2.3.3 Cross-Coupled Differential-Drive(CCDD) Architecture 22
2.3.3.1 Gate-Biasing Scheme 23
2.3.3.2 Body-Biasing Scheme 25
2.3.4 Technology Complementary Technique 26
2.3.5 Reconfigurable Rectifier 27
2.4 Comparison of Integrated Low-Power Rectifiers 29
2.5 Discussion 38
2.6 Summary 40

CHAPTER 3: PROPOSED CCDD RECTIFIER MODEL 41

3.1 Chapter Overview 41
3.2 Prior Works on Modelling Integrated Rectifier 41
3.2.1 Dickson Rectifier 41
3.2.2 CCDD Rectifier 43
3.3 Proposed CCDD Rectifier Model in Subthreshold Operation 44
3.4 Experimental Results 50
3.4.1 CCDD Rectifier Mathematical Model 50
3.4.2 Simulation Results 54
3.4.2.1 I_{s0} Extraction through Simulation 54
3.4.2.2 CCDD Rectifiers 55

3.4.3 Measurement Results 59
3.5 Discussion 62
3.6 Summary 64

CHAPTER 4: PROPOSED CCDD ARCHITECTURE 65
4.1 Chapter Overview 65
4.2 Proposed CCDD Architecture 65
4.2.1 DR Enhancement Concept 65
4.2.2 Proposed CCDD Architecture 67
4.2.3 Working Principle of Proposed CCDD Architecture 68
4.2.4 Multi-Stage Configuration 71
4.3 Experimental Results 75
4.4 Discussion 79
4.5 Summary 82

CHAPTER 5: CONCLUSION 83

References 86
List of Publications and Papers Presented 92
Appendix 96

LIST OF FIGURES

Figure 1.1: WSN as Leaf node in an IoT Framework 1

Figure 1.2: Applications of WSN. 2

Figure 1.3: An RFEH System Block 4

Figure 1.4: Integrated Low-Power Rectifier Architectures 4

Figure 1.5: Methodology of Research. 7

Figure 2.1: Rectifier PCE Curve. 14

Figure 2.2: NMOS-type Rectifier 17

Figure 2.3: Simplified Illustration of a Dickson V_{th} Compensation Scheme 18

Figure 2.4: 2-stage Differential Dickson-type Rectifier 20

Figure 2.5: Floating-Gate Rectifier Scheme 22

Figure 2.6: CCDD Gate-Biasing Scheme 23

Figure 2.7: CCDD Body-Biasing Scheme 26

Figure 2.8: Reconfigurable Rectifier Scheme 27

Figure 3.1: Circuit Analysis Model of Dickson Rectifier. 41

Figure 3.2: Circuit Model for Cross-Coupled Analysis. 44

Figure 3.3: Trasient Simulated Waveforms of M_{p}. 46

Figure 3.4: Program Flowchart. 51

Figure 3.5: 3D Model Plot of V_{Rec} versus R_{L} and $P_{\mathrm{in,rec}}$ 53

Figure 3.6: *I-V* Simulation 55

Figure 3.7: Schematic in EDA tool of the CCDD Rectifiers 56

Figure 3.8: Layout of Rectifiers with Bond Pads in EDA Tool 57

Figure 3.9: Test-Bench Simulation Set-Up 57

Figure 3.10: Input Impedance Simulation of Rectifiers 58

Figure 3.11: Micrograph of Fabricated Rectifiers.....59

Figure 3.12: Schematic of Measurement Set-Up.....59

Figure 3.13: Actual Measurement Set-Up.....60

Figure 3.14: Model Plot and Measurement Results of the CCDD Rectifiers.....61

Figure 4.1: General PCE Curve of CCDD Rectifier.....65

Figure 4.2: CCDD Rectifier Architecture.....67

Figure 4.3: Operational Priciple of Proposed CCDD Architecture.....69

Figure 4.4: *I-V* Curve of Diode-Connected MOS.....70

Figure 4.5: Multi-Stage Configuration of Proposed Rectifier.....71

Figure 4.6: V_{rec} Versus Rectifier Stages.....72

Figure 4.7: Coupling-Capacitor Configuration.....73

Figure 4.8: Micrograph of Fabricated Rectifiers.....75

Figure 4.9: Measurement Set-Up.....76

Figure 4.10: Measured Output Voltage, V_{rec}.....77

Figure 4.11: Comparison of Measured Output Voltage, V_{rec}.....78

Figure 4.12: Comparison of PCE at 900MHz for R_L=100 kΩ.....78

Figure 4.13: Technology roadmap of rectifer designs for ambient RFEH applcation.....82

LIST OF TABLES

Table 2.1: Radio Frequency Spectrum 12

Table 2.2: Measured Power Density of RF Bands 13

Table 2.3: Comparison of Integrated Low-Power Rectifiers 31

Table 2.4: Performance Comparison of Integrated Low-Power Rectifiers 34

Table 2.5: Comparison of Alternative Energy Sources 38

Table 3.1: Numeric Value of Natural Constants and Foundry Specification 50

Table 3.2: Specifications of Fabricated Rectifiers 56

Table 3.3: Comparison with Other CCDD Models 63

Table 4.1: Comparsion of CCDD Architectures 66

Table 4.2: Specifications of Rectifiers 75

Table 4.2: Comparison with Start-of-Art CCDD Architectures 80

LIST OF SYMBOLS AND ABBREVIATIONS

ABBREVIATIONS

AC	:	Alternating Current
ATVC	:	Adaptive Threshold Voltage Compensation
CCDD	:	Cross-Coupled Differential-Drive
ICC-CCDD	:	Individual-Capacitor Coupling CCDD
SCC-CCDD	:	Shared-Capacitor Coupling CCDD
CMOS	:	Complementary Metal Oxide Semiconductor
DAC	:	Digital-to-Analog
DC-DC	:	Direct Current-Direct Current
DR	:	Dynamic Range
DC	:	Direct Current
EDA	:	Electronic Design Automation
EEPROM	:	Electrically Erasable Programmable Read-Only Memory
EH	:	Energy Harvester/Harvesting
EHF	:	Extremely High Frequency
F-N	:	Fowler-Nordheim
FCC	:	Federal Communication Commission
FG	:	Floating Gate
GP	:	General Purpose
HF	:	High Frequency
HVT	:	High-V_{th}
IC	:	Integrated Circuit
IMN	:	Impedance Matching Network
IoE	:	Internet of Everything

IoT	:	Internet of Things
IPD	:	Integrated-Passive-Devices
IVC	:	Internal V_{th} Cancellation
L.E.D	:	Light Emitting Diode
LFDC	:	Low-feeding Direct Current
LVT	:	Low-V_{th}
MIM	:	Metal-Insulated-Metal
MOS	:	Metal-Oxide-Semiconductor
NMOS	:	N-type metal-oxide-semiconductor
OS-CPR	:	Orthogonally Switching-Charge Pump Rectifier
PCE	:	Power Conversion Efficiency
PDK	:	Process Design Kit
PMOS	:	P-type metal-oxide-semiconductor
PMU	:	Power Management Unit
POR	:	Power-on-Reset
PSG	:	Power Signal Generator
RF	:	Radio Frequency
RFIC	:	Radio Frequency Integrated Circuit
RF-DC	:	Radio Frequency-to-Direct Current
RFEH	:	Radio Frequency Energy Harvester/Harvesting
Rx	:	Receiver
S_{BA}	:	Banded Power Density
SAH	:	Sample-and-Hold
SHF	:	Super High Frequency
SOS	:	Silicon-on-Sapphire

TTL	:	Transistor-Transistor-Logic
Tx	:	Transmitter
UHF	:	Ultra-High Frequency
WSN	:	Wireless Sensor Node
WPT	:	Wireless Power Transfer
VHF	:	Very High Frequency
VM	:	Voltage Multiplier
VNA	:	Vector Network Analyzer

LIST OF APPENDIXES

Appendix A: RF Power Density Chart 96

Appendix B: Formulas of Signal Level Conversion 97

Appendix C: Derivation of the Proposed CCDD Model 98

Appendix D: Source Code for Simulation of CCDD Rectifier Model Plot 100

Appendix E: Process Device Specification 103

CHAPTER 1: INTRODUCTION

This chapter introduce this thesis by providing an overview to the background of the research work. The background of the research and problem statement are discussed and identified. Subsequently, the objectives of the research are established, the research methodology is presented and the contributions of the work are highlighted. Finally, the organization of the thesis is concluded the chapter.

1.1 Background and Motivation

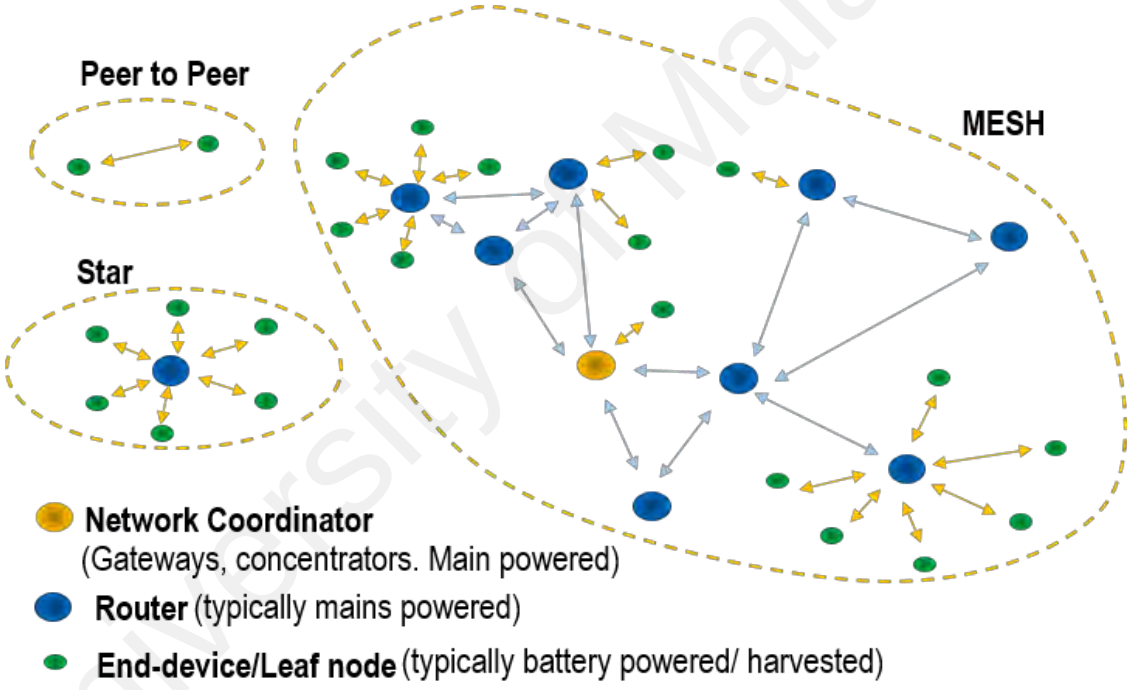

Figure 1.1: WSN as Leaf node in an IoT framework (Alioto, 2017)

The surge of Internet of Things (IoT) and Internet of Everything (IoE) initiatives has spurred a rapid increase in the number of interconnected electronic device (Morgan Stanley Research, 2016). IoT and IoE are communication infrastructures where large number of interconnected electronic devices communicate and interact together through the internet. Wireless sensor node (WSN) will contribute to the highest number count of these interconnected devices for the incoming wave of IoT and IoE initiatives. Figure 1.1

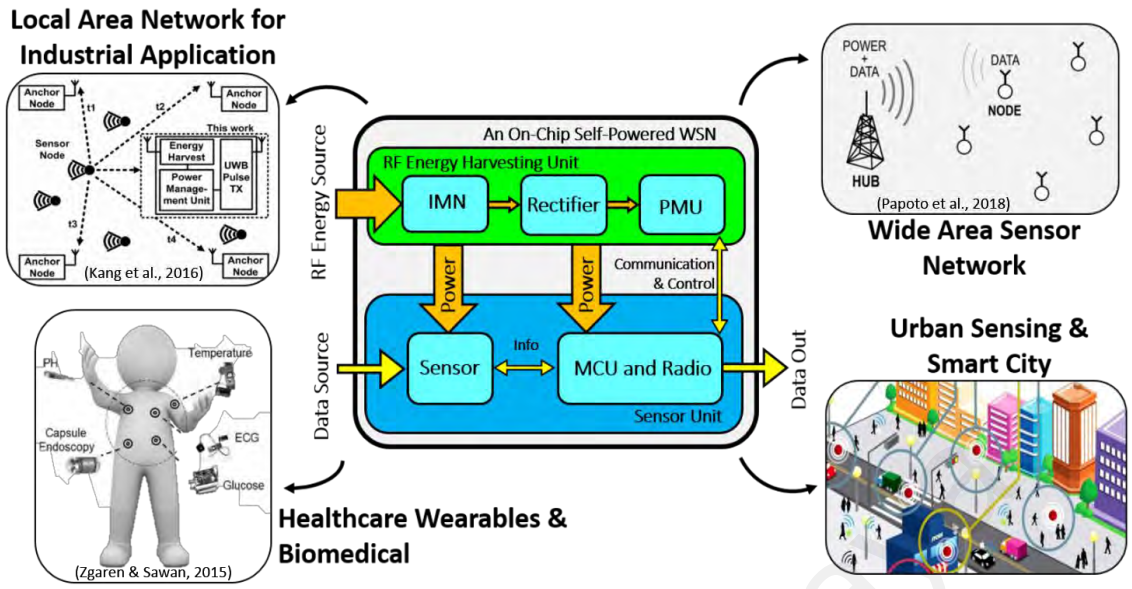

Figure 1.2: Applications of WSN

shows the WSN as leaf nodes in an IoT framework. WSN are sensing devices that acquire data such as temperature, atmosphere, light or images (Zanjireh & Larijani, 2015). The acquired data are wirelessly transmitted to a sensing hub (router) which collects streams of data from multiple WSN to be stored and processed on the internet.

The application of WSN ranges from large scale area network sensing (Papotto et al., 2018), biomedical implants for targeted muscle re-innervation (TMR) (Kim et al., 2015) to electrocardiogram (ECG) monitoring of heart activities (Mansano et al., 2016). Existing WSNs are still widely powered by batteries where the limitations are manifested through their large physical form factor, limitation in energy storage, and maintenance constraints for large number of deployed WSN. Hence, the need for alternative energy source through energy harvesting is required to extend the operational lifespan of WSN without the constraint in the size and the need for maintenance when using batteries as a power source.

Ambient Radio Frequency (RF) energy is a suitable and attractive solution as a power source for WSN (Soyata, Copeland & Heinzelman, 2016). Figure 1.2 depicts the block

diagram of a RF energy harvesting (RFEH) for WSN with some of the applications where it is deployed. The availability, predictability, and ease of scavenging RF energy through an antenna allows for WSN to be deployed in a variety of places including hard to reach area such as beneath the soil in agricultural monitoring or within concrete wall for structural monitoring systems. Coupled with the low-energy requirement of WSN RFEH fits to be as the alternative energy for powering up the sensor.

Complementary metal-oxide-semiconductor (CMOS) is a type of integrated circuit (IC) technology widely used in digital circuits. The small physical form-factor, low-cost, and system-on-a-chip (SoC) solution makes CMOS an attractive technology for research and mass production (Razavi, 2017). However, limitations such as device parasitics, quality factor degradation of on-chip passive components, and a lack of accurate modelling associated with IC technology requires new and improve circuit design techniques and circuit models for effective design of analog and RF circuits. The trajectory of this research is to investigate the characteristics of CMOS technology, develop new IC design insight for RF rectifier, and propose new circuit solutions for ambient RFEH systems.

1.2 Problem Statement

The typical circuit blocks in an RFEH system is shown in Figure 1.3. The system consists of an impedance matching circuit (IMN) to match the impedance of the RF antenna to the entire circuit, a rectifier which converts the harvested RF power in alternating (AC) power to usable direct (DC) power, and a power management unit (PMU) to regulate the converted energy to a suitable level for storage or powering the WSN. The challenge of harvesting RF energy is predominantly due to the low-power density of the energy source for the rectifier to convert the low power. This thesis focuses on the rectifier as it is the core and front-end circuit in the RFEH system.

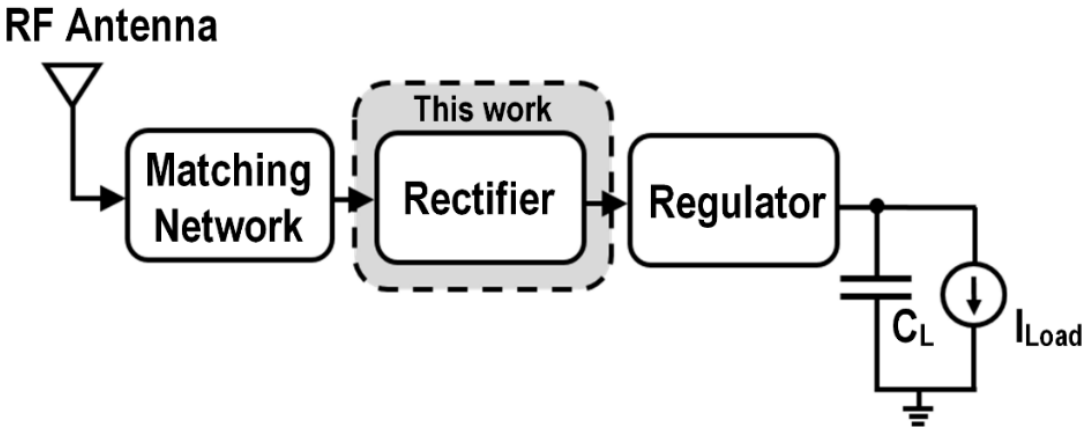

Figure 1.3: An RFEH System Block

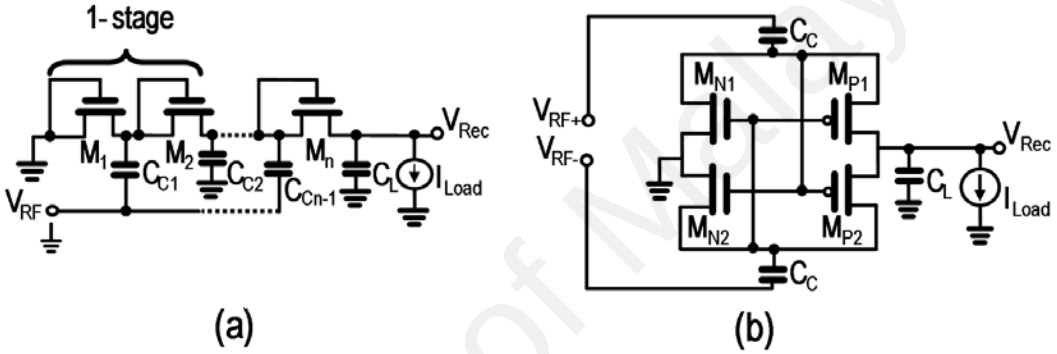

Figure 1.4: Integrated Low-Power Rectifier Architectures: (a) Dickson (Dickson, 1976) (b) Cross-Coupled Differential-Drive (CCDD) (Kotani et al., 2009)

There are two conventional rectifier topologies which are common in low-power RF rectification implemented on IC. The two conventional topologies for AC-to-DC conversion which are the widely implemented on IC are the Dickson and Cross-Coupled Differential-Drive (CCDD) topology shown in Figure 1.4(a) and Figure 1.4(b), respectively. A single rectifier stage is typically cascaded in *N* number of stages to achieve the highest output voltage, V_{rec}. The power conversion efficiency (PCE) and sensitivity are the main performance indicators of an integrated rectifier. PCE is defined in percentage of how efficient the rectifier converts the scavenged AC power into usable DC power. Alternatively, sensitivity is defined as the lowest input power level in decibel-milli-watts (dBm) at which the rectifier is able to convert the power to usable DC level (usually 1V).

This thesis investigates the CCDD architecture as it exhibit higher rectification performance compared to the Dickson counterpart (Kotani et al., 2009). There is a fundamental design gap in the CCDD rectifier where a mathematical model for ambient RFEH application has not been developed. A model is required as a mathematical guide to design the rectifier for the application of ambient RFEH. Existing work by Nariman et al. (2018) has developed a CCDD rectifier model, however, the model does not account for harvesting ambient RF energy. Alternatively, the model proposed by Wei et al. (2011) is too complex, inaccurate, and isn't reliable to be used for designing the rectifier for ambient RFEH.

Despite the high peak PCE performance of the CCDD, this topology still suffers from limitation in its dynamic range (DR) (Almansouri et al., 2018). DR is defined as the range across the harvested input RF power level, $P_{\mathrm{in,rec}}$ in which the rectifier maintains a PCE near its peak value. This limitation is caused by the inherent threshold voltage (V_{th}) of the transistor when rectifying at low $P_{\mathrm{in,rec}}$ and the reverse-leakage current at high $P_{\mathrm{in,rec}}$ which contribute to the DR degradation of the rectifier. A wide DR is essential for ambient RFEH implementation as the $P_{\mathrm{in,rec}}$ level of the harvested RF power is not constant. Besides that, the sensitivity of the rectifier is also crucial as ambient RF energy is typically very low in the actual environment. The inherent forward voltage drop due to the transistor's V_{th} in CMOS contributes to passive power consumption by limiting the forward current, thus degrading the sensitivity of the rectifier.

1.3 Objectives of the study

The aim of the study is to investigate the characteristics of CCDD rectifier for low-power ambient RFEH system implemented on CMOS technology. The objectives are set to contribute to the modelling and performance enhancement through new IC design techniques for the CCDD rectifier in ambient RFEH systems.

Objectives:

1. To investigate the characteristic of ambient RF energy for the development of a low-power rectifier for ambient RFEH in CMOS Technology.
2. To develop a novel mathematical model for the CCDD rectifier in ambient RFEH system.
3. To design and develop a CCDD rectifier for ambient RFEH system with enhanced performance in PCE dynamic range (DR).
4. To analyse and verify the performance of the rectifiers through fabrication, measurement and characterization of the CMOS IC implementation.

1.4 Research Methodology

The research methodology flowchart of this work is shown in Figure 1.5. The methodology is divided into two paths, which are to develop the mathematical model and design an enhanced PCE DR respectively to meet the objectives of the research. The activities of the thesis are executed simultaneously in the completion of this research project to meet the objectives. The first path focuses in developing a new mathematical model of a CCDD rectifier for ambient RFEH application. Investigation into various rectifier and IC modelling techniques are explored. A new model is derived using mathematical concepts applied to the CCDD rectifier on IC implementation. A valid model is developed, simulated and compared with circuit simulation of CCDD rectifier with various specifications designed using an Electronic Design Automation (EDA) tool. The designs are streamed out for fabrication and tested through hardware measurements.

Next, new insights in performance limitations of the CCDD rectifier through the novel model are translated into the development of a new CCDD architecture. The first task is to set initial specification target by comparing with state-of-art CCDD architectures as a benchmark in the development of the new rectifier. Various ideas and concepts for the

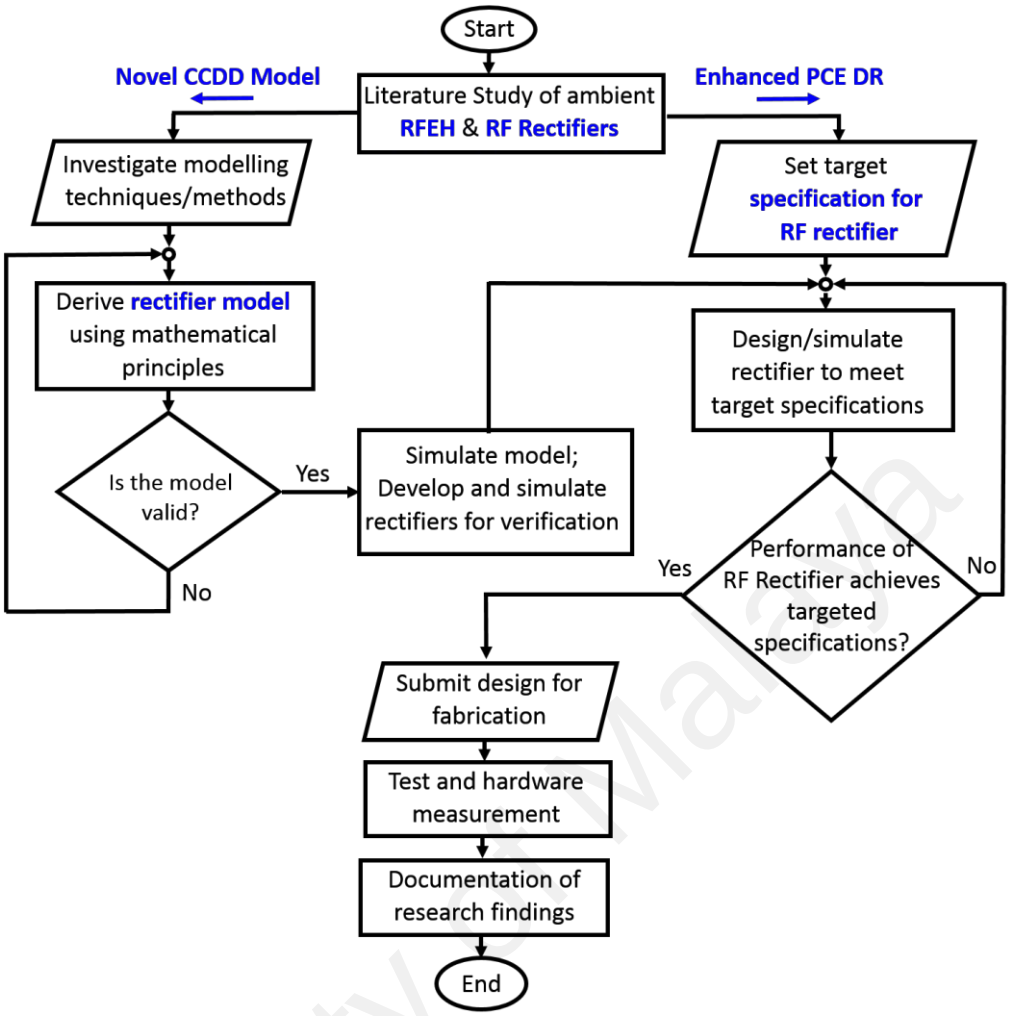

Figure 1.5: Methodology of Research

rectifier are simulated to discover suitable circuit techniques to improve the DR performance. As new innovative circuit techniques are discovered which yields significant improvement in the performance, the circuits are sent for tapeout. Once the tapeout of the rectifiers are fabricated, it is tested and measured to verify its hardware performance. With satisfactory results achieved in both works, the findings are documented and published in journals.

1.5 Contributions of the Research Work

The following highlight the contributions of this work.

1. A novel mathematically model of a CCDD rectifier for ambient RFEH in subthreshold operation with hardware verification.

2. A newly proposed CCDD architecture with enhanced performance of the DR with hardware verification.
3. Analysis and design of two capacitor-coupling configurations, namely, the shared-coupling-capacitors (SCC-CCDD) and individual-coupling-capacitors (ICC-CCDD) are developed.
4. Low-cost solution adopting CMOS technology for all the implemented CCDD rectifiers in this work.
5. System-on-Chip (SoC) solution capabilities of the CCDD rectifiers for system integration for ambient RFEH and WSN systems.

1.6 Thesis Outline

Chapter 1 presents an overview of this thesis through the research background, motivation, problem statements, research objectives and highlighted research contributions. Next, chapter 2 presents a comprehensive literature review of low-power rectifier for the Dickson and CCDD rectifier architecture. A novel mathematical model of the conventional CCDD rectifier in subthreshold operation for ambient RFEH system is proposed in Chapter 3. Furthermore, Chapter 4 proposes a new CCDD architecture with enhanced performance in the PCE DR. Chapter 5 summarizes the work and provide recommendations for future works.

CHAPTER 2: LITERATURE REVIEW

2.1 Chapter Overview

This chapter elaborates the literature review on integrated low-power rectifiers. First, an investigation in the characteristic of RF energy source is studied. A comprehensive literature review of integrated low-power rectifiers focusing on IC implementation is followed. Subsequently, prior works on low-power rectifiers are compared and discussed. The summary concludes the literature review at the end of this chapter.

2.2 RF Energy

2.2.1 Background

RF energies are electromagnetic waves propagated in a free space medium, typically propagated through air (Visser & Vullers, 2013). There are two types of RF energy harvesting (RFEH) system: Near-field and Far-field RFEH systems. These types are typically differentiated based on the frequency or wavelength of the RF energy, the method of the RF energy is transmitted, and the power density of the RF energy to be scavenged. Near-field RFEH system is commonly known as Wireless Power Transfer (WPT) system. The transfer of electrical energy in Near-field RFEH system are intentional where the energy is transmitted between two magnetic-coupled coils or antennas coupled at a very close proximity (Kim et al., 2014). The typical frequency of RF energy is low and within the spectrum of the Industrial, Scientific and Medical (ISM) radio bands of 433 MHz, 16.53 MHz or 6.78 MHz. The applications of Near-field RFEH system are typically towards biomedical implants or near-field RFID tags where the device operates in close proximity to the power transmission hub where the application requires larger amount of energy in the range of milli-watt (mW) for its operation.

Alternatively, Far-field RFEH system harvests residual electromagnetic RF energy which is propagated in the air by radio transmission (Tx) antennas (Visser & Vullers

2013). These propagated RF energies are typically generated by Tx antennas from cellular base stations, Wi-Fi routers or Bluetooth devices. In Far-field RFEH systems, the power density of the harvested RF wave is in the range of micro-watts (μW) and having a frequency much higher to that of Near-field RFEH systems. Scavenging RF energy in Far-field RFEH system is accomplished by the RF energy intercepting a receiver (Rx) antenna which converts the scavenged RF wave into electrical signal through the antenna's conductor wire. The scope of this thesis focuses on Far-field RFEH system with the targeted application for low-power Wireless Sensor Node (WSN). Subsequent denotation of RFEH in this thesis refers specifically to Far-Field RFEH system. Section 2.2.2 investigate the characteristics of ambient RF energy for the development of a low-power rectifier for ambient RFEH in CMOS Technology that corresponds to the first objective of this thesis.

2.2.2 Characteristics of Ambient RF Energy

2.2.2.1 Availability

An RF survey conducted by Piñuela et al. (2013) measures the ambient RF energy level at 270 London Underground station in London, England. It was reported that more that 50% of the stations are suitable for harvesting ambient RF energy. The measurement was conducted in each station between 10 a.m. and 3 p.m. on weekdays from March 5th to April 4th in the year 2012. The measurement was made with an RF analyzer calibrated with an omnidirectional antenna.

Similar RF surveys were conducted to investigate the feasibility of ambient RFEH at various cities such as the city of Covilhã in Portugal (Barroca et al. 2013), downtown Tokyo in Japan (Vyas et al., 2013), the city of Bristol in England (Mimis et al., 2014), city of Shunde in China (Andrenko et al., 2015) and the central region of Paris (Takhedmit, 2016). Despite the low-power density of the measured RF energy in the

reported RF surveys, ambient RF energy is becoming more available in urban environment due to the increase in wireless communication networks installed in cities worldwide. Each RF survey has claimed that harvesting ambient RF energy as a power source for low-power electronic devices such as the WSN will become feasible in the near future as all RF spectrums are becoming crowded.

The theoretical limit of an Rx antenna to convert electromagnetic wave to electrical signal is determined by Friis transmission equation in free space (Friis, 1946) given by:

$$P_{\mathrm{R}} = P_{\mathrm{T}} G_{\mathrm{T}} G_{\mathrm{R}} \frac{\lambda^2}{(4\pi R)^2} \tag{2.1}$$

P_{R} is the power received at the antenna in dBm, P_{T} and G_{T} are the power and antenna gain of the Tx source in dBm, respectively, G_{R} is the gain of the Rx antenna, lambda (λ) is the wavelength of the RF energy, and R is the radius between the Rx and Tx antennas. Subsequently, the generated AC voltage of the input power is given by:

$$V_{\mathrm{ant}} = \sqrt{8 \times R_{\mathrm{ant}} \times P_{\mathrm{R}}} \tag{2.2}$$

where V_{ant} is the peak input AC voltage, P_{R} is the received power and R_{ant} is the radiation resistance of the Rx antenna with a typical value of 50-Ω.

Equation 2.1 shows that the characteristics of the scavenged RF energy by an Rx antenna is determined by λ, R and G_{R} as the values of G_{T} and P_{T} are constant to adhere to the federal communication commission (FCC) regulation for permissible level of propagated RF radiation. Alternatively, equation 2.2 shows that R_{ant} could be altered by designing a custom antenna with higher radiation resistance to increase the peak input AC voltage. However, antenna design is beyond the scope of this research, hence, it will not be considered in the scope of this thesis.

2.2.2.2 Frequencies

The RF spectrum are classified into respective bands in radio communication according to the frequency of the electromagnetic wave (IEEE, 2003). The RF bands are classified by their frequencies, application, and allocation by the communication regulation boards. Table 2.1 summarizes the RF spectrum bands with its corresponding frequency range and applications. The band of interest in this thesis is the ultra-high frequency (UHF). This is due to this frequency band containing the highest power availability in free space due to its crowded spectrum and high intensity of communication activities as more wireless electronic devices operates in this band according to the reported RF surveys, making it practical in actual implementation for RFEH.

Table 2.1: Radio Frequency Spectrum (IEEE, 2003)

Band Name	Abbreviation	Frequency Range	Application
High Frequency	HF	3-30 MHz	Shortwave broadcast, RFID, radio communication
Very High Frequency	VHF	30-300 MHz	FM radio, mobile communication
Ultra-High Frequency	UHF	300-3000 MHz	Broadcasting television, Bluetooth, Mobile phone
Super High Frequency	SHF	3-30 GHz	Microwave devices, communication satellite, wireless LAN
Extremely High Frequency	EHF	30-300 GHz	Millimeter wave, microwave remote sensing

2.2.2.3 Power Density

Table 2.2 tabulates the measured RF power density of the RF survey by Piñuela et al. (2013). Table 2.2 shows the average RF power measured for each frequency band at 270

underground station in London, England where S_{BA} is the banded power density across each frequency band. Among the measured UHF bands, GSM900 (BTx), GSM1800 (MTx) and 3G (BTx) which correspond to the frequency around 900 MHz, 1800 MHz and 2.15 GHz, respectively have the highest power density of RF energy with the potential for harvesting in the real environment.

The measurement tabulated in Table 2.2 are conducted in areas where the Tx antenna source is not known. The input power can only be gauge based on the measurement by the lowest available RF power detected by the RF analyzer used to conduct the survey. Piñuela et al. (2013) has verified the feasibility of harvesting ambient RF energy at these locations by developing an RFEH system prototype implemented with discrete electronic components to harvest ambient RF energy as low as -29 dBm to power up a Light Emitting Diode (L.E.D) to blink every 140 seconds. The reported work by Piñuela et al. (2013) validates that harvesting ambient RF energy in the environment is possible and recommends further research to develop ambient RFEH system.

Table 2.2: Measured Power Density of RF Bands (Piñuela et al., 2013)

Band	Frequency (MHz)	Average S_{BA} (nW/cm^2)	Maximum S_{BA} (nW/cm^2)
DTV	470 ~ 610	0.89	460
GSM900 (MTx)	880 ~ 915	0.45	39
GSM900 (BTx)	925 ~ 960	36	1930
GSM1900 (MTx)	1710 ~ 1785	0.5	20
GSM1800 (MTx)	1805 ~ 1880	84	6390
3G (MTx)	1920 ~ 1980	0.46	66
3G (BTx)	2110 ~ 2170	12	240
Wi-Fi	2400 ~ 2500	0.18	6

2.3 Review of Integrated Low-Power Rectifiers

2.3.1 Power Conversion Efficiency (PCE)

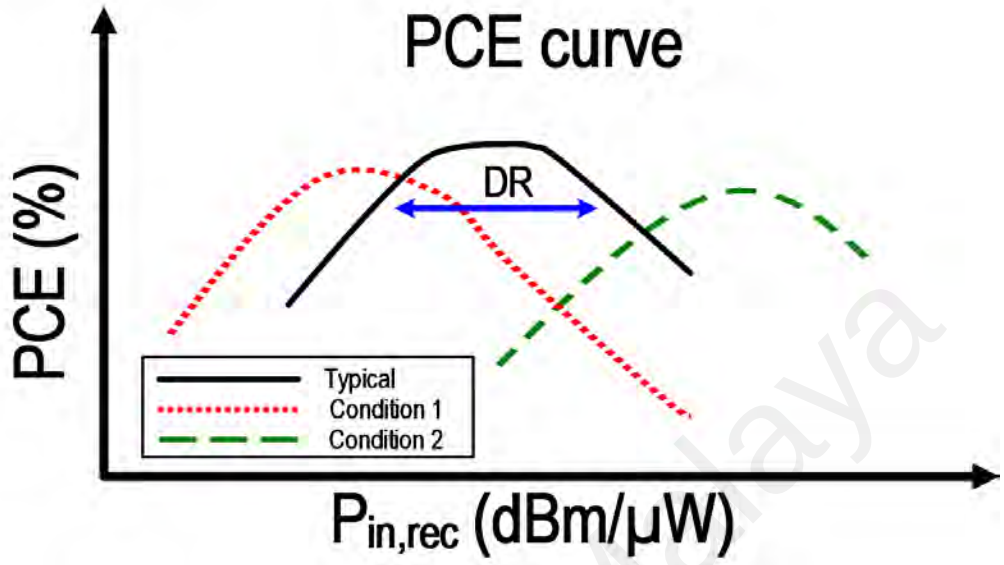

Figure 2.1: Rectifier PCE Curve

The expression to compute the power conversion efficiency (PCE) is given by,

$$\text{PCE} = \frac{\text{Harvested dc Power}}{\text{Input RF Power into Rectifier}} = \frac{P_{\text{DC}}}{P_{\text{RF}}} = \frac{V_{\text{Rec}} I_{\text{Load}}}{\frac{1}{T}\int_0^T v_{\text{in}}(t) i_{\text{in}}(t) dt} \tag{2.3}$$

where P_{DC} is the output DC power and P_{RF} is the instantaneous input AC power of the RF energy. The output power of the rectifier is computed through multiplying the output voltage, V_{Rec} with the output current, I_{Load}. The input AC power is determined by the instantaneous voltage, v_{in} multiplied by the instantaneous current, i_{in} for a single RF cycle at steady-state.

The PCE characteristic of a rectifier can be illustrated through the PCE curve as shown by the PCE plot in Figure 2.1. At low to mid-power range of $P_{\text{in,rec}}$, the PCE rises steadily before it peaks and the curve starts to slope downwards thereafter. There are two conditions which could alter the PCE characteristic of a rectifier to shift. The conditions can be denoted as condition 1 and condition 2 depicted in Figure 2.1 which shifts the PCE

curve to the lower and higher range of the PCE plot, respectively. Condition 1 occurs when the PCE curve shifts to the left in which the rectifier is designed to achieve higher peak sensitivity in its performance. The rectifier design in condition 1 typically consists of a large number of rectifier stages with small output (large resistor value) load. Alternatively, the design of the rectifier which generates a PCE characteristic of condition 2 is to accommodate higher output power requirement of the system for a larger output load (smaller resistor value). This shifts the curve towards the right side in the power range of the PCE curve where sensitivity of the rectifier is compromised. Hence, the PCE curve can be altered based on the rectifier's design for the targeted application.

A new parameter to define the performance of a rectifier has been recently identified by Almansouri et al. (2018) which is the dynamic range (DR) that has been discussed in Chapter 1. DR is defined as the ability of the rectifier to achieve peak PCE across input RF power level, $P_{\mathrm{in,rec}}$. The DR relates closely to the PCE in which the improvement in DR would contribute to the enhancement of the RFEH system across the range of $P_{\mathrm{in,rec}}$. Therefore, the objective of this thesis is to improve the DR of a CCDD rectifier.

2.3.2 Dickson Architecture

The conventional Dickson architecture was first introduced by Dickson (1976) shown in Figure 1.4(a). It is the first reported rectifier implemented on integrated metal-oxide-semiconductor (MOS) technology designed for high voltage generator in memory writing and erasing for Transistor-Transistor Logic (TTL) compatible to non-volatile quad-latch application. With reference to Figure 1.4(a), a single-stage Dickson rectifier consists of two diode-connected transistors, M_1 and M_2. The rectifier can be cascaded for multiple of *N*-stages to boost the rectified voltage with the expenses of PCE. C_{C} are the coupling capacitors and DC block element while C_{L} is the smoothing or output load capacitor to reduce the output ripple voltage.

During the negative half-cycle of the input RF voltage and assuming a steady-state operating condition, coupling capacitor C_{C1} charges to $V_{RF} - V_{th,M1}$ where V_{RF} is the peak AC voltage of the input RF signal and $V_{th,M1}$ is the threshold voltage of M_1. During this cycle, M_1 conducts in forward-bias while M_2 conducts in reverse-bias. Subsequently, during the positive half-cycle of V_{RF}, transistor M_1 turns off while M_2 turns on as it operates in forward-bias. At the same time, capacitor C_{C2} charges to $2V_{RF} - V_{th,M1} - V_{th,M2}$ during the negative half-cycle which doubles the output rectified voltage. This operation generates a rectified output voltage, $V_{Rec,1}$ for a single stage Dickson rectifier and is expressed by:

$$V_{Rec,1} = 2V_{RF} - V_{th,M1} - V_{th,M2} \tag{2.4}$$

It can be observed through equation 2.4 that the threshold voltage (V_{th}) of the transistor significantly influences the output voltage which contributes to the degradation in performance of the rectifier.

2.3.2.1 Threshold Voltage (V_{th}) Cancellation or Reduction

The first intuition to improve the performance of a rectifier would be to eliminate V_{th}. Figure 2.2 shows the Dickson as an NMOS transistors of a Voltage Multiplier (VM) scheme for RFEH proposed by Umeda et al. (2006). The scheme proposed by Umeda et al. (2006) utilized an external battery to reduce the detrimental effect of V_{th} to enhance the performance of the rectifier. An alternate V_{th} cancellation (IVC) scheme proposed by Nakamoto et al. (2007) replaces the external battery with an internal ferroelectric capacitor that replicates the transistor's V_{th}. The ferroelectric capacitors holds a voltage during the charge cycle and discharges the voltage during the release cycle to cancel the transistor's V_{th}.

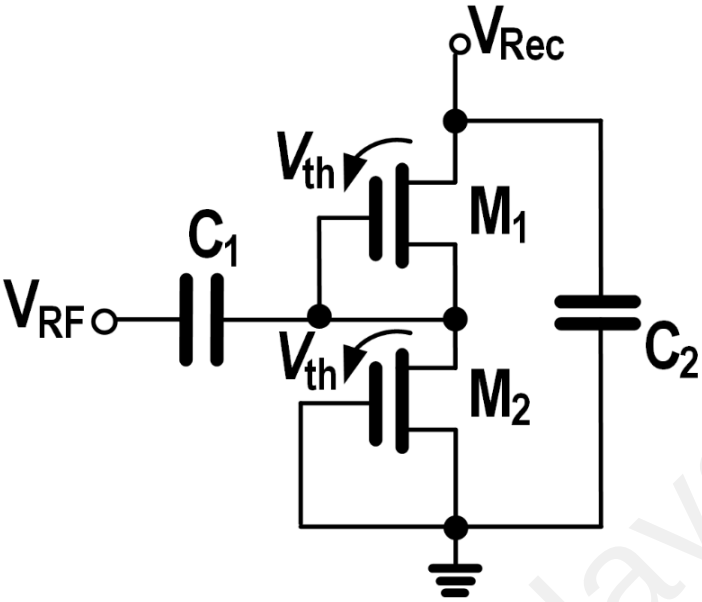

Figure 2.2: NMOS-type Rectifier (Umeda et al., 2006)

Another V_{th} cancellation scheme is the orthogonally switching-charge pump rectifier (OS-CPR) proposed by Mansano et al. (2013). This V_{th} cancellation scheme is implemented using capacitors as energy storage elements with passive resistors to set the optimal gate potential for V_{th} cancellation. However, only simulation results were presented which doubts the practical validation for the proposed scheme in hardware implementation. Similarly, a V_{th} cancellation scheme proposed by Chouhan and Halonen (2015) utilizing the rectified DC output voltage of the rectifier and the input RF voltage cycles along a pumping capacitors to cancel the influence of the V_{th}.

V_{th} cancellation schemes can be effective in reducing the detrimental effect of the transistors' V_{th}. However, V_{th} cancellation schemes introduces reverse-leakage current where this effect is evident during the negative half-cycle operation of the rectifier as the output voltage potential becomes larger than the input rising or falling RF voltage ($V_{\mathrm{rec,N}} > V_{\mathrm{RF}}$) which causes current to flow from the output back to the source. Hence, V_{th} cancellation scheme alone is not sufficient to improve the performance of the rectifier. Ideally, the rectifier should have zero V_{th} during the forward conduction phase to reduce

the V_{th} of the transistors and a large V_{th} during the reverse conduction phase to prevent reverse-leakage current phenomena to occur.

2.3.2.2 Threshold Voltage (V_{th}) Compensation Scheme

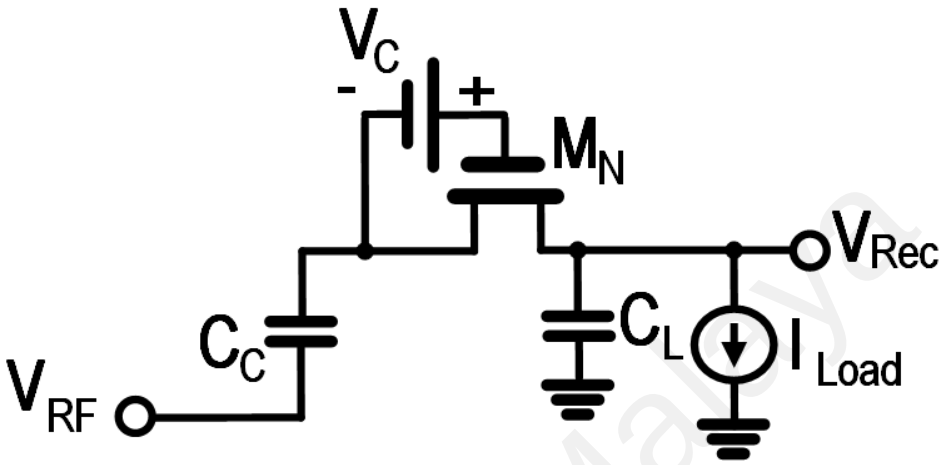

Figure 2.3: Simplified Illustration of a Dickson V_{th} Compensation Scheme

The V_{th} "compensation" schemes is an improved V_{th} cancellation scheme which adopted the key concept of reducing V_{th} at forward conduction phase and increasing V_{th} during the reverse conduction phase. Figure 2.3 illustrates a simplified schematic of a V_{th} compensation scheme where the compensation voltage, V_{C} provides an adaptive voltage to ensure that M_{N} achieved an optimal V_{th} compensation during the operation of the rectifier.

Karthaus and Fischer (2003) first implemented this technique by utilizing a special IC fabrication process through integrating Schottky diodes compatible with CMOS technology. Schottky diodes inherently have very low forward V_{th} and is effective at preventing reverse-leakage current. However, the additional cost of integrating Schottky diodes makes this solution unattractive for IC implementation. Solely utilizing circuit techniques in CMOS process to improve the performances of the rectifier is desirable to maintain the attractiveness in cost and small physical form factor of CMOS technology.

Papotto et al. (2011) proposed a V_{th} compensation scheme in CMOS technology with a multi-stage Dickson rectifier using the concept of "order" compensation. As the rectified DC voltages at the output of each stage differs in a multi-stage rectifier, the optimal V_{C} of each stage could be tapped from respective output voltages in the multi-stage rectifier chain. Equation 2.5 denotes the manner in which V_{C} is able to cancel out the detrimental effect of V_{th}.

$$V_{\mathrm{Rec,1}} = V_{\mathrm{RF}} - V_{\mathrm{th1}} + V_{\mathrm{C}} \tag{2.5}$$

First, the standard working condition of a rectifier with respect to $P_{\mathrm{in,rec}}$ and the loading condition has to be determined. Next, The optimal V_{C} are tapped at the output of the respective rectifier stages according to the required V_{C} for each stage.

Alternatively, Hammed and Moez (2014) proposed a hybrid forward and backward V_{th} compensation scheme which is similar to that of Papotto et al. (2011) with the ability of backward compensation. Instead of determining the optimal V_{C} for each stage, the later stages of the rectifier utilizes $V_{\mathrm{Rec,N+1}}$ from the immediate subsequent stage to tap V_{C}. A follow up work by the same authors improved the scheme with an adaptive V_{th} compensation scheme that provides passively adaptive compensation (Hameed & Moez, 2015). The proposed compensation scheme provides V_{C} to enhance the forward operation and reduce V_{C} during reverse-bias to reduce the reverse-leakage current. Though this V_{th} compensation scheme is effective, this scheme requires an additional auxiliary rectifier chain. Additional power is fed through the auxiliary chain which degrades the PCE of the rectifier as part of the $P_{\mathrm{in,rec}}$ is consumed by the auxiliary chain.

Another V_{th} compensation scheme proposed by Scorcioni et al. (2013) presents a cross-connected technique through a differential Dickson rectifier demonstrated on a 2-stage rectifier shown in Figure 2.4. M_1 and M_4 are the diode-connected transistors of the

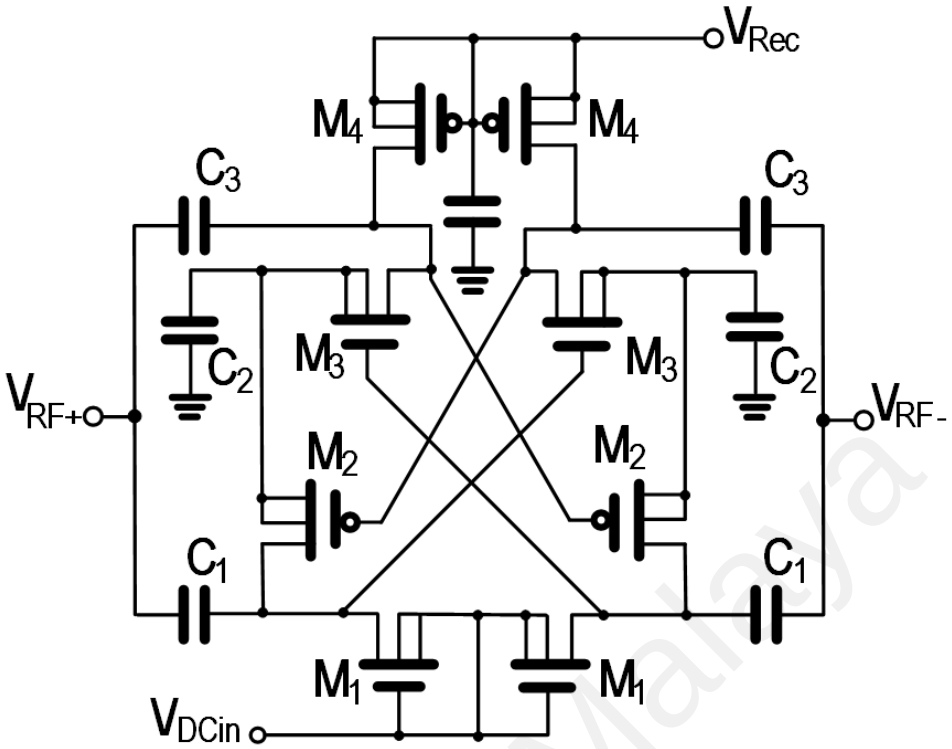

Figure 2.4: 2-stage Differential Dickson-type Rectifier with Cross-Coupled Transistor Scheme (Scorcioni et al., 2013)

rectifier while M_3 and M_4 are the added cross-connected scheme to improve upon the aforementioned V_{th} compensation schemes. The gate of M_2 (M_3) are connected to the source M_3 (M_2) in the opposing branch of the differential pair which allows for a doubling of the gate-source voltage, V_{gs} as compared to conventional diode-connected scheme. Thus, the detrimental effect of V_{th} reduces while impedance mismatch of the rectifier is improved resulting in an enhancement in efficiency and sensitivity.

More complex V_{th} compensation scheme by Xia et al. (2014) proposes a tunable gate-bias rectifier by using MOS switches to control the tuning of the compensation "order" demonstrated with a 12-stage rectifier. A complex digital controller is required to track the input voltage level and tune the "order" of the rectifier by biasing the gates to enhance the performance. Another complex V_{th} compensation scheme is the self-calibrated UHF rectifier proposed by Gharehbaghi et al. (2017) consisting of one main rectifier and two auxiliary rectifiers as offset generator and offset calibrator. The offset generator converts

the RF voltage to a DC source to generate V_{C}. Concurrently, the offset-calibrator compresses V_{C} with a dummy load by regulating the current drawn by the offset generator to achieve a fixed compensation voltage of 0.15V. The value of 0.15V is proposed to be the optimal value for V_{C} across the range of $P_{\mathrm{in,rec}}$ for the implemented rectifier according to preliminary simulation results in the adopted CMOS technology.

Furthermore, an active threshold voltage compensation (ATVC) multiplier was proposed by Luo and Liu (2017) which uses an active circuit to control the level of V_{C}. The ATVC monitors the final output voltage, $V_{\mathrm{Rec,final}}$ at the last stage of the rectifier and generates the optimal V_{C} for each rectifier stage accordingly. The ATVC consists of an oscillator which generates a clock for the timing controller, a clock booster for the sample-and-hold (SAH) circuits, a comparator, a D-flip-flop, and a digital-to-analog converter (DAC) working in synchronous to monitor V_{Rec} and generate the optimal V_{C} for the rectifier. However, the ATVC only commence operation when $V_{\mathrm{Rec,final}}$ exceeds 0.38V to allow the system to turn on, limiting the operation range of this scheme.

2.3.2.3 Bulk-Biasing Scheme

In addition to V_{th} compensation scheme, another approach is through biasing of the transistors bulk to reduce V_{th}. Le et al. (2008) proposed a bulk-biasing technique coupled with a floating-gate rectifier compensation scheme with MOS capacitors utilized to generate V_{C}. Figure 2.5 illustrates the proposed floating-gate rectifier scheme proposed by Le et al. (2008). The MOS capacitors (C_{gs1} and C_{gs2}) are intended as floating-gate transistors connected in series with the rectifier. Charges are externally injected into the floating-gate transistors to reduce V_{th} of M_1 and M_2. The high impedance of the oxide layer allows for trapping charges inside the floating-gate transistors. Thus, the trapped charges in C_{gs1} and C_{gs2} act as a gate-source bias to passively reduce V_{th} of M_1 and M_2

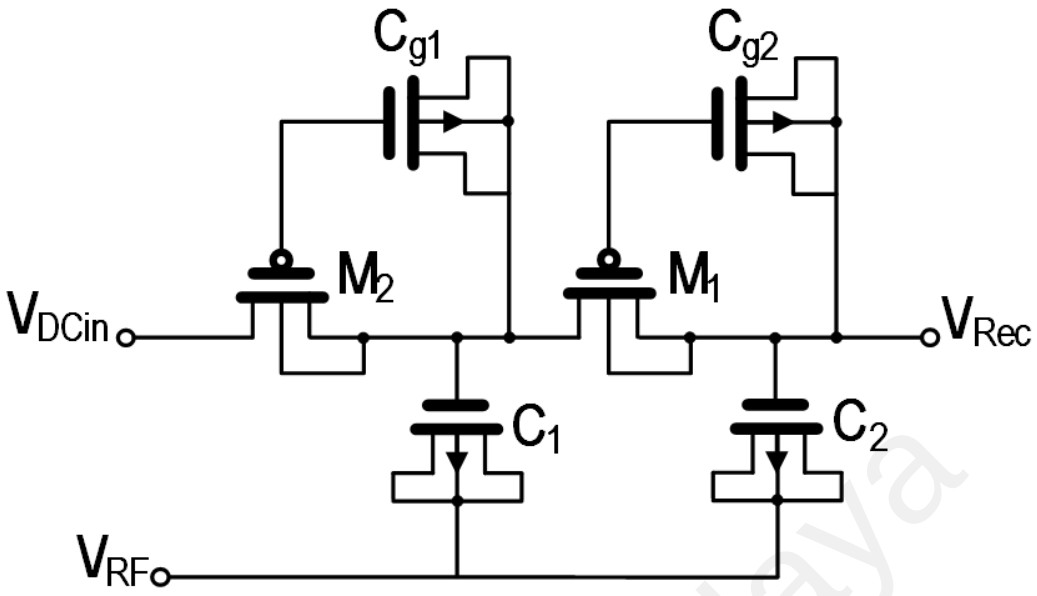

Figure 2.5: Floating-Gate Rectifier Scheme (Le et al., 2008)

while C_1 and C_2 are NMOS implemented as coupling capacitors for size reduction purposes. The bulk terminals of M_1 and M_2 are connected to the bulk terminals of C_{gs1} and C_{gs2} respectively to amplify the reduction effect of V_{th}. Unfortunately, this scheme requires initial programming of the floating-gate transistors making this a complex solution. Besides that, the timing of charge injection to the transistors via Fowler-Nordheim (F-N) adds further complexity to this scheme. It would require precise control of the charge injecting into the transistors when the rectifier is not in operation. The injection of charges could be done with the input sinusoidal RF wave but the process is much slower than F-N tunneling (Le et al., 2008).

2.3.3 Cross-Coupled Differential-Drive (CCDD) Architecture

The counterpart of the Dickson rectifier is the Cross-Coupled Differential-Drive (CCDD) rectifier. The conventional CCDD rectifier was first introduced as a four-cell unit by Mandal and Sarpeshkar (2007) and refined as the Cross-Coupled Differential-Drive scheme by Kotani et al. (2009). The schematic of this rectifier is shown in Figure 1.4(b). Referring to Figure 1.4(b), the structure of a conventional CCDD rectifier consists

of two pairs of one NMOS and one PMOS transistors connected in series with its gate shorted together. C_C are the coupling capacitors at the input RF source and C_L is the smoothing capacitor at the output. The gates of the NMOS and PMOS pair are shorted between the drain or source of the opposing pair in a cross-coupled fashion, hence its name. Similarly, symmetrical connection is evident for the opposite pair where the connecting points are linked to the input terminals for a differential configuration.

Assuming steady-state operation, when the input RF voltage at the V_{RF+} terminal is positive and V_{RF-} is negative, M_{N2} and M_{P1} turn on while M_{N1} and M_{P2} turn off. This creates a loop of the circuit creating a complete path for the current to flow in the rectifier. Similarly, when the terminals of V_{RF+} and V_{RF-} invert, transistors M_{N2} and M_{P1} turn off while M_{N1} and M_{P2} turn on, creating a loop of a complete circuit. The voltage potential at the terminal $V_{Rec,N}$ will remains positive throughout its operation, thus, the input RF voltage is rectified.

2.3.3.1 Gate-Biasing Scheme

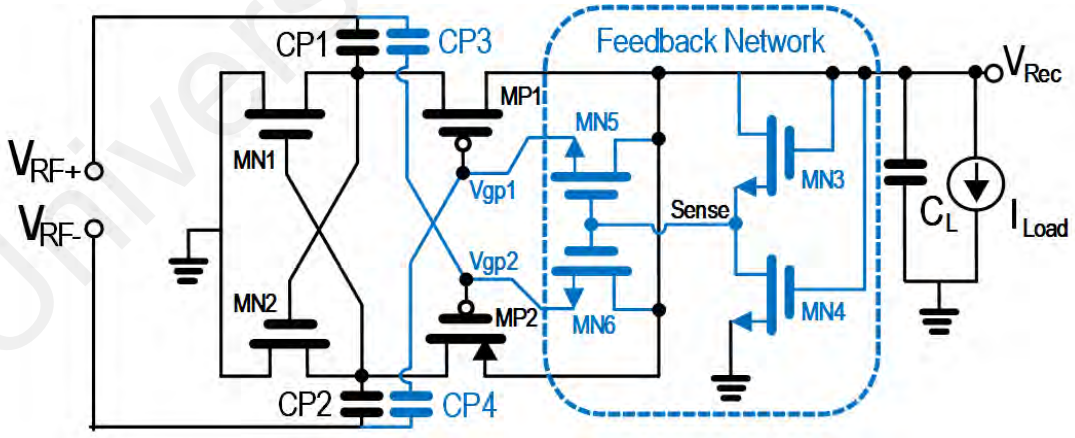

Figure 2.6: CCDD Gate-Biasing Scheme (Ouda et al, 2016)

Recent improvement of this topology focuses on enhancing the sensitivity performance. Improving the sensitivity of the CCDD rectifier typically focuses on reducing the reverse-leakage current. Figure 2.6 illustrates a gate-biasing scheme

proposed by Ouda et al. (2016) that could be applied to the CCDD rectifier to regulate the forward and reverse current conduction in the rectifier to improve the PCE and sensitivity performance.

A gate-biasing scheme by Yoo et al. (2010) employs an adaptive threshold rectifier as a gate-biasing scheme implemented on a CCDD rectifier. As $V_{\mathrm{Rec,N}}$ gradually increases beyond the transistor's V_{th}, a power-on-reset (POR) signal triggers the transistors' gate to be bias by the rectified DC voltage to reduce V_{th} to a virtual value of zero. This reduces the detrimental effect of V_{th} and improves the performance of the rectifier. However, this proposed gate-biasing scheme consists of resistive elements which consumes power and chip area on the IC. A pseudo floating-gate similar to the aforementioned operates by pumping an external floating-gate voltage, V_{FG} generated from an external voltage source for achieving zero V_{th} was proposed by Giannakas et al. (2012). The external voltage source does not provide a fully integration solution which is not suitable for SoC implementation.

Another approach by Nguyen et al. (2014) is through a hybrid piezoelectric and RF energy harvester with a gate-biasing scheme. The RF harvester utilizes the generated DC voltage from the piezoelectric harvester to clamped and bias the gates of the RF rectifier. This provides a DC voltage offset at the gate for the RF rectifier to operate above the subthreshold region. An accompanying power source is required to adopt this scheme where the density of the accompanying power source is required to be larger than the RF power source for this scheme to be effective.

The gate-biasing scheme proposed by Ouda et al. (2016), Ouda et al. (2017) and Almansouri et al. (2018) emphasized on reducing the detrimental effect of reverse-leakage current to improve the sensitivity of the CCDD rectifier. The work by Ouda et al.

(2016) shown in Figure 2.6 implements a self-biased scheme with a feedback network that utilizes the output voltage at high $P_{\mathrm{in,rec}}$ to raise the DC bias of the PMOS in the CCDD rectifier. A potential divider network senses $V_{\mathrm{Rec,N}}$ and limits the reverse-leakage current accordingly by biasing the gate of transistors. The input coupling capacitors, C_{C} are decoupled from the NMOS and PMOS to isolate the bias mechanism of the feedback network. A simple and improved scheme of this solution is by implementing a large passive resistor as the self-bias mechanism between the gate terminal and output terminal of the PMOS transistor to reduce the reverse-leakage current (Ouda et al., 2017). Despite improvement in reducing the reverse-leakage current, the forward conduction current is compromised which limits the performances of the rectifier. To counter this, Almansouri et al. (2018) substituted the large passive resistor with a high-V_{th} diode-connected transistor to increase the forward conduction current and simultaneously reduce the IC chip area. The scheme was also implemented in the NMOS transistors of the CCDD rectifier which was reported to achieve additional performance improvement.

2.3.3.2 Body-Biasing Scheme

Another improvement method reported for the CCDD rectifier is the bulk or body biasing scheme. This technique is implemented by injecting of voltage potential at the bulk of the transistors to reduce V_{th}, resulting in a lower turn-on voltage. Figure 2.7 shows a simple self-body-biasing scheme depicted by the dotted line applied in a conventional CCDD rectifier (Moghaddam et al., 2017).

Reinisch et al. (2011) presents a modified CCDD rectifier to overcome the trade-offs in multi-frequency operation, the range of $P_{\mathrm{in,rec}}$, loading condition, number of stages, output voltage and parasitic consideration using the body-biasing technique. A single-stage CCDD rectifier was used due to higher parasitic being evident in a multi-stage configuration. The rectifier consists of a feedback transistor that provides a static bias

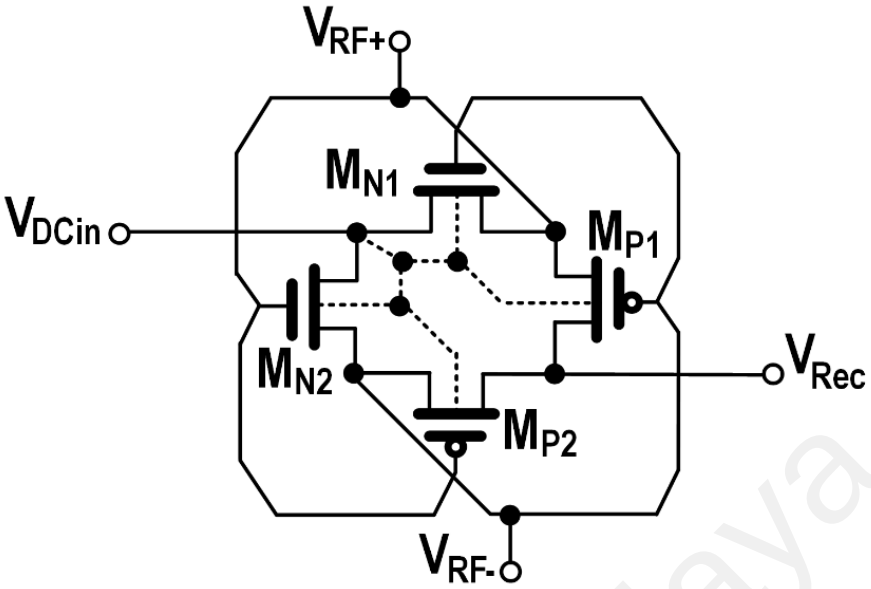

Figure 2.7: CCDD Body-Biasing Scheme (Moghaddam et al., 2017)

voltage, V_{b} which controls the gate and bulk voltages. This reduces the forward voltage drop and achieves wide operating frequency range through reduction in parasitic.

Alternatively, Moghaddam et al. (2017) proposed the low-feeding DC (LFDC) body-biasing scheme shown in Figure 2.7 to improve the forward-current of the rectifier. The body of the NMOS and PMOS are tied to the lower-feeding DC source of the previous stage which creates a self-bias mechanism for the transistor. This scheme enhances the PCE performance with the increase in V_{Rec} at lower RF power levels and becomes a protection circuit at higher levels of $P_{\mathrm{in,rec}}$. Special process of deep N-well transistors is required to perform this method of bulk-biasing.

2.3.4 Technology Complementary Technique

Other improvement schemes reported are through the adoption of technology complementary schemes such as the integration of Schottky diodes in CMOS by Karthaus and Fischer (2003) and the adoption of silicon-on-sapphire (SOS) on CMOS to improve the PCE performance of the rectifier (Theilmann et al., 2012). By superimposing the rectifier with Schottky diodes or SOS with CMOS exploited the benefits of both

technologies to improve the forward conduction and reduce reverse-leakage current in the rectifier. The main drawback in adopting this technique is in the cost of fabrication. Secondly, not all IC fabrication foundry offers unique complementary technology with CMOS in its fabrication service making this technique not a feasible solution to be explored for wide adoption.

2.3.5 Reconfigurable Rectifier

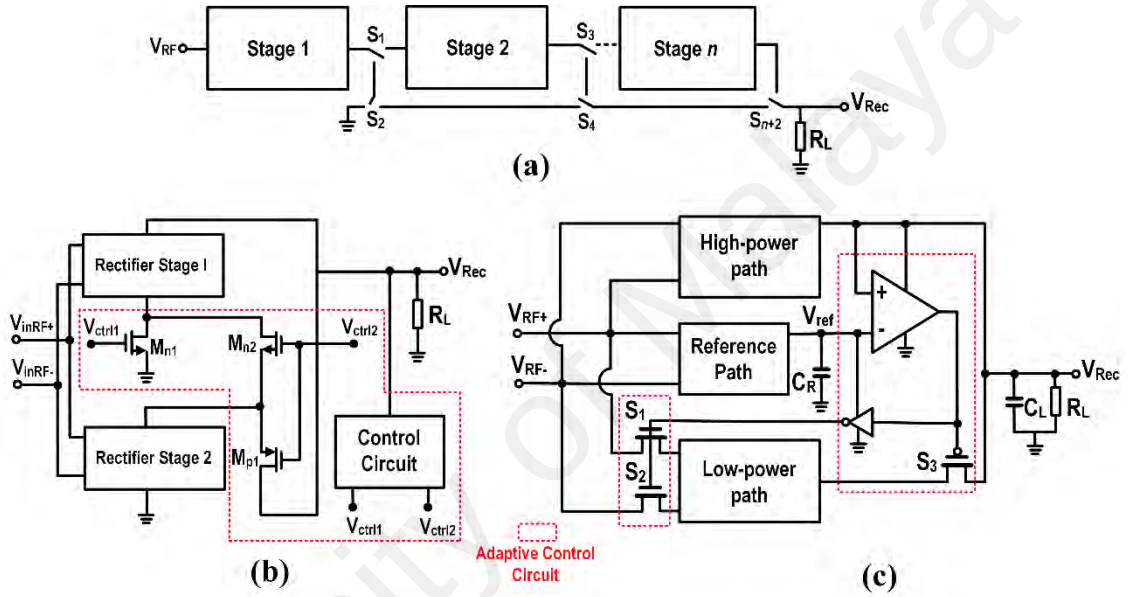

Figure 2.8: Reconfigurable Rectifier Scheme: (a) No. of Stages Reconfiguration (Abouzied et al., 2017) (b) Series-Parallel Reconfiguration (Li & Lee, 2014) (c) Rectifier Path Selection (Lu et al., 2017)

Reconfigurable rectifier is another approach to improve the performance of the rectifier by reconfiguring the number of stages, stage arrangement, or rectifier path. Reconfigurable rectifiers are implemented to overcome the design trade-offs which could not be achieved solely through passive circuit design techniques. Besides that, the type of the transistors of different threshold voltage can affect the start-up, input impedance mismatch and V_{th} drop which influence the performances of the rectifier.

Abouzied et al. (2017) claims there is a need for an RFEH system to adapt to the varying $P_{\mathrm{in,rec}}$ level. This requires for RFEH systems to have a reconfigurable Impedance

Matching Network (IMN) and a reconfigurable rectifier to adapt to the power variation level of $P_{\mathrm{in,rec}}$. Thus, a fully integrated RFEH system adopting a reconfigurable rectifier to adapt to the fluctuating $P_{\mathrm{in,rec}}$ level illustrated in Figure 2.8(a) is proposed (Abouzied et al., 2017). A low-power PMU with minimal DC overhead is adopted to achieve self-startup and a non-overlapping input-output level shifter was adopted to minimize short circuit power loss to regulate the harvested power flow in the system. The implemented RFEH system achieved an overall performance improvement in sensitivity with higher number of rectifier stages at low $P_{\mathrm{in,rec}}$ levels and achieving an average PCE at high $P_{\mathrm{in,rec}}$ levels with the adopted PMU for reconfiguring the rectifier.

Another work by Scorcioni et al. (2013) proposed a reconfigurable rectifier using a simple control logic to configure a two-stage Dickson rectifier in series or parallel. Operating with a smart voltage regulator, this system enhances the sensitivity of the RFEH system by dynamically matching the input impedances of the rectifier and antenna due to variation of the rectifier's input impedance with respect to the level of $P_{\mathrm{in,rec}}$. This method of reconfiguring the rectifier stages to a series or parallel combination improves the sensitivity of the RFEH system by ensuring maximum power transfer is achieved through impedance matching of the rectifier and antenna across $P_{\mathrm{in,rec}}$.

Alternatively, Li and Lee (2014) proposed a similar approach for PCE enhancement by adopting a PMU to configure the arrangement of the rectifier stages. As the rectifier stage arrangement alters the PCE characteristic across $P_{\mathrm{in,rec}}$, the rectifier configures the stage arrangement to be a single-stage rectifier or a two-stage rectifier. The adaptive rectifier utilizes a passive control circuit to switch the configuration of the rectifier to the respective mode in its operation according to the stage arrangement illustrated in Figure 2.8(b). The PMU utilizes a positive feedback mechanism to ensure the modes of the

rectifier are not activated simultaneously for smooth transitioning when the switching between the modes.

Lu et al. (2017) investigated and compared the efficiency of transistor models in a CMOS process design kit (PDK). The transistor models available include low threshold (LVT), standard threshold (SVT) and high threshold (HVT) transistors in a general purpose (GP) and low-power (LP) PDK. The investigation shows that LVT transistors achieves higher efficiency at low $P_{\mathrm{in,rec}}$ level while HVT transistors achieves higher efficiency at high $P_{\mathrm{in,rec}}$ level. Hence, the author proposed a dual-path rectifier as shown in Figure 2.8(c) with each path consisting of dissimilar transistor models. The reference path senses the level of $P_{\mathrm{in,rec}}$ and switches the rectifier paths to achieve optimal efficiency and ensure high PCE of the RFEH system across the harvesting range of $P_{\mathrm{in,rec}}$.

All reconfigurable rectifier scheme reviewed here requires additional power for the control unit. This inevitably reduces the PCE of the RFEH system unless the control unit is able to operate with extremely low power requirements. Besides that, the supply headroom needed to kick-start the control operation reduces its effectiveness for ambient RFEH where the input AC amplitude is low.

2.4 Comparison of Integrated Low-Power Rectifiers

Table 2.3 summarizes the review on low-power rectifiers with its corresponding performances tabulated in Table 2.4. PCE degradation due forward V_{th} drop and reverse-leakage current are evident in low-power rectifiers for RFEH. The reviewed literatures focus extensively to overcome this trade-offs and enhance the rectifier's performances through V_{th} compensation schemes, reverse-leakage current reduction technique, reconfigurable schemes and technology complementary.

Based on the review and performance comparison in Table 2.4, CCDD architecture exhibits higher peak PCE compared to the Dickson counterpart while sensitivity is moderate between both architectures. Besides that, literatures on CCDD reported significantly less number of rectifier stage to achieve similar levels of V_{rec} for low-power rectification. There are more emphasis to design rectifiers within the GSM900 band as this band is highly crowded based on the RF surveys reported in Section 2.2.2.2 and its wide application in RFID technology.

Table 2.3: Comparison of Integrated Low-Power Rectifiers

Author	Project	Problem	Proposed Solution
Dickson (1976)	Integrated High Voltage Generator.	Nonexistence of integrated high voltage generator.	Integrated high voltage generator in NMOS derived from discrete Cockcroft-Walton Multiplier topology.
Karthaus & Fischer (2003)	Fully integrated Passive RFID transponder.	Distance of reading range of transponder.	Design of low-power circuit utilizing CMOS process supporting EEPROM and Schottky.
Umeda et al. (2006)	Rectifier for sensor tag.	Simultaneous *on*-state of transistors for MOS rectifier with threshold below 100 mV.	High sensitivity rectifier with bias voltage using battery.
Mandal & Sarpeshkar (2007)	Rectifier study and design for RFID application.	Impedance of rectifier dominated by linear parasitic component and load.	4-transistor cell with floating-gate employed to maximize the input impedance.
Nakamoto et al. (2007)	Passive RFID CMOS Tag.	High parasitic capacitance due to the switch of transistor that controls V_{th} cancellation.	Internal V_{th} cancellation scheme utilizing ferroelectric RAM.
Le et al. (2008)	Energy harvesting for passively powered sensor tag.	Limited current range of zero-threshold transistors and large physical size of integrated resistors.	MOS floating-gate to create gate-source bias to reduce V_{th} loss of the rectifier.
Kotani et al. (2009)	Cross-Coupled Differential-Drive Rectifier.	Inability to achieve small *on*-resistance and small reverse-leakage at the same time.	A new active V_{th} cancellation scheme rectifier topology.
Yoo et al. (2010)	Self-configurable wearable body sensor controller.	Safety issue and battery lifespan of existing health monitoring system.	Adaptive V_{th} rectifier for body sensor.
Reinisch et al. (2011)	Multi-frequency Passive sensor tag.	Bottleneck in operation range due to load and high parasitic present in a multi-stage rectifier.	Transistor gates of a single-stage rectifier superimposed with AC complementary signal by coupling capacitor.
Papotto et al. (2011)	Threshold compensated RFEH for RF powered-sensor network.	Sensitivity of rectifier dictated by V_{th} and multi-path fading based on Friis equation.	"Order" compensation scheme to provide bias offset compensation voltage to the rectifier.

Table 2.3, continued

Author	Project	Problem	Proposed Solution
Theilmann et al. (2012)	Technology complementary solution for rectifier.	Complementary benefits and drawbacks of rectifier in SOS and CMOS.	Utilizing separate integration technology into one rectifier design.
Giannakas et al. (2012)	Energy harvesting technique.	Trade-off between low V_{th} and reverse blockage.	Pseudo floating-gate (FG) to reduce V_{th}.
Scorcioni, et al. (2013)	RF energy scavenger.	Unpredictable variation of power and sensitivity.	Differential rectifier with cross-coupled scheme to reduce detrimental effect of V_{th}.
Mansano et al. (2013)	Rectifier for energy harvesting.	Detrimental effect of V_{th}.	Orthogonally Switching Charge Pump Rectifier (OS-CPR) for optimal dc gate potential biasing.
Nguyen et al. (2014)	Hybrid energy harvester.	Deterioration of efficiency toward lower V_{th}.	Biasing of RF rectifier by clamped piezoelectric signal.
Xia et al. (2014)	Multi-node Wireless Body area Network	Detrimental effect of V_{th} and parasitic capacitance.	Tunable rectifier with tracking loop system.
Hameed & Moez (2014)	Compensation scheme for RF energy harvester.	Reducing of efficiency due to increased number of stage and increase compensation increases reverse-leakages.	Hybrid Forward and Backward Compensation scheme.
Stoopman et al. (2014)	Co-design of antenna with rectifier.	Reverse-leakage at higher rectification of output voltage.	Final rectifier stage replace with a complementary diode-connected rectifier.
Li & Lee (2014)	Adaptive power harvester.	Peak PCE only available at different rectifier arrangement.	Passive control circuit to switch between rectifier arrangements.
Chouhan & Halonen (2015)	Threshold compensation scheme.	Peak efficiency attain at a particular trigger voltage and saturation of output voltage with increase in input voltage.	Threshold compensation scheme utilizing DC output voltage and input RF voltage to cancel influence of V_{th}.

Table 2.3, continued

Author	Project	Problem	Proposed Solution
Hameed & Moez (2015)	Adaptive threshold rectifier.	Losses due to reverse-leakage that increases overall power loss.	Passive adaptive compensation scheme using minimal circuit to increase V_{th} at forward voltage and decrease V_{th} at reverse voltage.
Ouda et al. (2016)	RF-DC power converter.	Reverse current caused by bi-directionality of MOS transistor.	Adaptive self-biasing feedback network.
Gharehbaghi et al. (2017)	Self-calibrating technique for threshold compensation.	Peak efficiency only at one particular input power level.	Two auxiliary rectifiers for offset generator and offset calibrator for threshold compensation.
Luo & Liu (2017)	Threshold compensated rectifier.	Large forward voltage and threshold cancellation increases reverse-leakage current.	Adaptive V_{th} compensated multiplier.
Moghaddam et al. (2017)	Rectifier for far-field RF energy harvesting.	Forward voltage drop and reverse-leakage current.	Low feeding DC-biasing rectifier scheme.
Ouda et al. (2017)	Self-biased rectifier to enhance efficiency dynamic range.	Poor sensitivity of the Dickson topology and high reverse-leakage when rectifying high input RF power.	Self-biasing mechanism to control current conduction by raising effective turn-on voltage at high input RF power.
Lu et al. (2017)	Dual-path rectifier.	Varied in performance of transistor model in a given semiconductor process.	Adaptive control to select between two distinct rectifier paths with different transistor model used.
Abouzied et al. (2017)	Fully integrated RF energy harvester.	Variable nature of input RF power and the effect of load on start-up.	Reconfigurable rectifier stages based on the input power level and output load.
Almansouri et al. (2018)	RF-DC power converter.	Reverse current that affects efficiency across input power range.	Single-sided and double-sided rectifier scheme.
Mohamed et al. (2018)	RF-to-DC rectifier.	Power dissipation of the threshold voltage.	Gate-biasing of PMOS switch with an external clamper circuit.

Table 2.4: Performance Comparison of Integrated Low-Power Rectifier

Author	Year	Technology (nm)	Frequency (MHz)	Topology, Stages	Peak PCE (% @ dBm for load)	Sensitivity (dBm @V_{Rec} for load)	Max tested load
Dickson	1976	NMOS	100	Dickson, 3-4 stage	n.a.	n.a.	3.2 MΩ
Karthaus & Fischer	2003	500 + Schottky	868 2,400	Dickson, n.a.	18% @ 12.5 μW for 1.5 μA 5% @ 45 μW for 1.5 μA	9.8 μW @ 1.5V for 0.95 μA	1.58 MΩ
Umeda et al	2006	300	950	Dickson, 6-stage	11% @ -6 dBm for 0.4 μA	-14 dBm @ 1.5V for 0.4 μA	3.75 MΩ
Nakamoto et al.	2007	350	953	Dickson, 1-stage mirror stacked	36.6% @ -6 dBm for 80 μW	n.a.	112.5 kΩ
Mandal & Sarpeshkar	2007	500/180	900/950	CCDD, 3-stage	23.5% @ n.a. for 2 μW	n.a.	500 kΩ
Le et al.	2008	250	906	Dickson, 16/36-stage	60% @ -8 dBm† for ∞	-22.6 dBm @ 1V for 0.3 μA	0.33 MΩ
Kotani et al.	2009	180	953	CCDD, 1/3-stage	82.6% @ -24.5 dBm for 100 kΩ	-25 dBm @ 0. 25V for 50 kΩ	10 kΩ
Yoo et al.	2010	180	400	CCDD, 4-stage	54.2% @ -2 dBm for 12 μW	n.a.	2.7 MΩ
Reinisch et al.	2011	130	900	CCDD, 1-stage	7.5% @ -10.1 dBm for 250 kΩ	-12.5 dBm @ 1V for 2.1 μW	98 kΩ

*simulation †estimated from graph #IMN+Rectifier+PMU

Table 2.4, continued

Author	Year	Technology (nm)	Frequency (MHz)	Topology, Stages	Peak PCE (% @ dBm for load)	Sensitivity (dBm @ V_{Rec} for load)	Max tested load
Papotto et al.	2011	90	915	Dickson, 17-stage	11% @ -15 dBm* for 0.5 MΩ	-22.44 dBm @ 1V for ∞	0.5 MΩ
Theilmann et al.	2012	250 + Silicon-On-Sapphire	100/915	CCDD, Complementary Bridge, 3-stage	44% @ -26.4 dBm for 1 μW	-26.4 dBm @ 1V for 1 MΩ	30 kΩ
Giannakas et al.	2012	90	2,450	Dickson, 20-stage	5.46% @ 1.29meter (from energy source) for 1 MΩ	125 mV @ 1.2V for 1 MΩ	500 kΩ
*Mansano et al.	2013	180/90	13.56, 433, 915	Dickson, 4-to-8-stage	11.9% @ -18.2 dBm for 1 MΩ	-20 dBm @ 1V for 1 MΩ	0.1 MΩ
#Scorcioni et al.	2013	130	868	Modified Dickson, 2-stage	60% @ - 7.5 dBm† for ∞	-21 dBm @ 2V for ∞	n.a.
Nguyen et al.	2014	90	13.56	CCDD, 6-stages	44%† @ -11 dBm for 68 kΩ	300 mV_{pp} @ 1V for 330 kΩ	68 kΩ
Xia et al.	2014	65	904.5	Dickson, 12-stage	5.2% @ -14 dBm for 0.5 MΩ	-20dBm @ 0.9V for 5 MΩ	0.5 MΩ
Hameed & Moez	2014	130	915	Dickson, 8/12-stage	21.6% @ -14.8 dBm for 5 MΩ	-24dBm @ 1V for 5 MΩ	1 MΩ
Stoopman et al.	2014	90	868	CCDD, 5-stage	40% @ -17 dBm for 0.33 MΩ.	-27 dBm @ 1V for ∞	0.33 MΩ
Li & Lee	2014	180	2,400	CCDD, 3-stage	47% @ 8.9 dBm for 2 kΩ	n.a.	2 kΩ

*simulation †estimated from graph #IMN+Rectifier+PMU

Table 2.4, continued

Author	Year	Technology (nm)	Frequency (MHz)	Topology, Stages	Peak PCE (% @ dBm for load)	Sensitivity (dBm @ V_{Rec} for load)	Max tested load
Chouhan & Halonen	2015	180	433	Dickson, n.a	30% @ -5 dBm for 10 kΩ	-14 dBm† @ 0.3V for 1 MΩ	10 kΩ
Hameed & Moez	2015	130	915	Dickson, 24/2-stage	32% @-15 dBm for 1 MΩ	-20.5 dBm @ 3.2V for 1 MΩ	500 kΩ
Ouda et al.	2016	180	1,000	CCDD, 1-stage	65% @ **-18 dBm for 100 kΩ	-18 dBm @ 1V for 100 kΩ	100 kΩ
Gharehbaghi et al.	2017	180	433	Dickson, 5-stage	34% @ -7 dBm for 50 kΩ	-19 dBm @ 1V for ∞	50 kΩ
Luo & Liu	2017	180	402	Dickson, 3-stage	31.9% @ -1 dBm for 30 kΩ	-12 dBm @ 1.38V for 1 MΩ	30 kΩ
Ouda et al.	2017	180	433	CCDD, 1-stage	65.3% @ -15 dBm for 50 kΩ	30 μW @ 1V for 50 kΩ	50 kΩ
Moghaddam et al.	2017	130	953	CCDD, 3-stage	73.9% @ 4.34 dBm for 2 kΩ	-7 dBm† @ 1V for 50 kΩ	2 kΩ
#Lu et al.	2017	65	900	CCDD, 5-stages	36.5% @ -10 dBm for 147 kΩ	-17 dBm @ 1V for ∞	147 kΩ

*simulation †estimated from graph #IMN+Rectifier+PMU

Table 2.4, continued

Author	Year	Technology (nm)	Frequency (MHz)	Topology, Stages	Peak PCE (% @ dBm for load)	Sensitivity (dBm @ V_{rec} for load)	Max tested load
[#]Abouzied et al.	2017	180	900	Dickson, 1-2-4-8	25% @ 0 dBm for 1 MΩ	-17 @ 1V for 1 MΩ	2 kΩ
Almansouri et al.	2018	180	433	CCDD, 1-stage	86% @ 11.5 μW[†] for 100 kΩ	-19.2 dBm @ 1V for 100 kΩ	50 kΩ
			900		66% @ 12.5 μW[†] for 100 kΩ	-18.2 dBm @ 1V for 100 kΩ	
Mohamed et al.	2018	180	402	CCDD, 1-stage	86% @ -15 dBm[†] for 50 kΩ	-16.5 dBm @ 0.52V for 10 kΩ	10 kΩ
			953		70% @ -15 dBm[†] for 50 kΩ	-16.8 dBm @ 0.38V for 10 kΩ	

*simulation [†]estimated from graph [#]IMN+Rectifier+PMU

2.5 Discussion

The RF surveys in section 2.2 showed that the power density of RF spectrums are projected to grow in urban and sub-urban areas as wireless communication technology are becoming widely adopted in everyday life. Thus, the increasing power density of the RF spectrums will produce more residual of RF energy available in the environment for harvesting. Hence, this justifies RF energy as the choice of investigating as an alternative power source for WSN devices. Table 2.5 depicts the benefits of ambient RF energy in comparison to other alternative energy source. The controllability, predictability and small physical size are the primary considerations for investigating in this thesis. Despite its main drawback in its low power density, the energy density is sufficient for low-power WSN applications.

Table 2.5: Comparison of Alternative Energy Sources (Kim et al., 2014)

Energy	Power Density	Available Time	Transducer	Average Total Harvester Size
Ambient Radio Frequency	0.0002 ~ 1 μW/cm^2	Continuous	Antenna	2~3g
Vibration	200 μW/cm^3	Actively Dependent	Piezoelectric	2~10g
Thermal	60 μW/cm^2	Continuous	Thermoelectric Generator (TEG)	10~20g
Light	100 mW/cm^2	Day time ~ 4-8 hours	Solar	5~10g

The various prior-art rectifiers reviewed have drawn circuit design concepts of the rectifiers from well-established application such as RFID systems. This research is built upon the development of the rectifier for RFEH systems towards WSN application. V_{Rec} is typically increased by adding more rectifier stages. However, the trade-off between the PCE and number of stages is evident due to the forward V_{th}. An optimal number of rectifier stages is required to achieve a balance in PCE performance. Besides that, the

effect of reverse-leakage current at high $P_{\mathrm{in,rec}}$ level degrades the PCE performance. Alternatively, the PCE DR performance has only been recently reported a new performance indicator for rectifiers in RFEH system.

The Dickson rectifier requires large number of stages to achieve a reasonable V_{Rec} and has poor PCE performance due to the degradation effect of V_{th} in a multi-stage configuration. Highly complex V_{C} compensation schemes are required to enhance the performance of the rectifier to overcome the forward V_{th} drop and reverse-leakage current. The conventional CCDD on the other hand requires less number of stages to achieve a comparable V_{rec} which alleviates the concern for achieving a high PCE. However, the poor DR exhibit in the CCDD shows potential in conducting research to improve the rectifier for ambient RFEH systems. Besides that, the limitation of the DR which is significant in this topology shows potential for improvement towards the application of ambient RFEH system.

Hence, the CCDD rectifier is chosen for the study in this research. As the importance in the PCE DR is of an emerging concern for RFEH, improving the DR sets one of the objectives of this research. Enhancing the DR of the CCDD rectifier will ensure an overall improvement in PCE performance of the RFEH system. Developing new circuit technique to achieve high PCE across a wide $P_{\mathrm{in,rec}}$ range would improve the DR of the rectifier while retaining the sensitivity performance of the rectifier.

Various reported rectifier concepts has drew circuit design insights from well-established applications such RFID where this research in this thesis is built. Trade-offs between high PCE, sensitivity and number of stages are evident in low-power rectifier. New circuit technique with optimal number of rectifier stages is required to overcome the trade-offs which are caused by the detrimental effect of V_{th} and reverse-leakage current

across a wide input RF power range. Thus, DR as the new performance indicator is considered in this work as an investigation criteria in the development of a new rectifier for ambient RFEH towards WSN application.

2.6 Summary

An investigation of RF energy and a comprehensive literature review on low-power IC rectifiers have been presented. First, the review covers an overview of the characteristics of ambient RF energy. Subsequently, a review of various circuit techniques to improve the performance of low-power IC rectifier is followed. The PCE and sensitivity are the main performance indicators of the rectifier. The PCE DR is an emerging importance for RFEH systems. Justification has been made in the choice of RF frequency and the CCDD rectifier chosen for this research work. A review on ambient RFEH system which includes the review on integrated low-power rectifiers in this chapter has been published in a volume of Springer: Analog Integrated Circuits and Signal Processing.

CHAPTER 3: A NOVEL CCDD RECTIFIER MODEL

3.1 Chapter Overview

This chapter presents a novel Cross-Coupled Differential-Drive (CCDD) rectifier model in subthreshold operation for ambient RFEH achieving an accuracy of 90%. The novel CCDD model is targeted toward the design of ultra-low-power Internet of Things (IoT) devices such as medical implants (Ouda et al., 2013) and biomedical wearables (Yoo et al., 2010). The chapter begins with a review of prior works in modelling integrated rectifiers. Next, the novel model of the CCDD rectifier is presented with an in-depth analysis through step-by-step derivation of its development. Finally, experimental results are presented and discussed with comparison of the model with prior-art CCDD rectifier models. A summary concludes the findings at the end of this chapter.

3.2 Prior Works on Modelling Integrated Rectifier

3.2.1 Dickson Rectifier

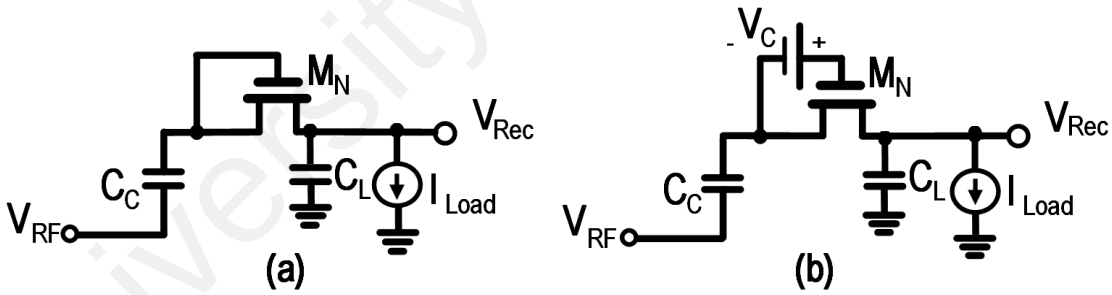

Figure 3.1: Circuit Analysis Model of Dickson Rectifier for RF Energy Harvesting: (a) Standard Circuit Model (Yi et al., 2007) (b) Circuit Model with Compensation Voltage, V_C (Gahrehbagh et al., 2017)

Mathematical modelling provides an in-depth understanding in the operation of a circuit, identifies the contributing factors in its operation, defines the theoretical operation limit, and provides insight for effective design methodology of the circuit. There have been various proposed mathematical models of integrated monolithic rectifier for the Dickson rectifier. Yi et al. (2007) first developed a model of the Dickson rectifier for

RFEH in complementary metal-oxide-semiconductor (CMOS) with design methodologies for highest V_{rec} and highest peak PCE. Subsequently, Gahrehbaghi et al. (2017) improved on the model proposed by Yi et al. (2007) with additional consideration of the compensation voltage, V_{C}. Alternatively, Razavi Haeri et al. (2017) complements the work by Yi et al. (2007) by developing a similar model of the Dickson rectifier targeted towards ambient RFEH with inclusion of V_{C}. Figure 3.1 shows the schematic for circuit analysis of the Dickson rectifier for RFEH.

Other reported works improve upon existing models of the Dickson rectifier for RFEH through approximating the transistors as diode-connected metal-oxide-semiconductor (MOS) to reduce the complexity of the mathematical derivation while maintaining high accuracy (Ashry et al., 2008). Besides that, Barnett et al. (2009) proposed a Dickson model which considers the non-ideality of the transistors and Gharehbaghi et al. (2016) proposed a Dickson model which considers the body-effect and channel-length modulation. Models of the Dickson rectifier in Schottky Diode technology (Curty et al., 2005) and electrically erasable programmable read-only memory (EEPROM) compatible in CMOS technology (Bergeret et al. 2007) are available. In addition, models to achieve faster evaluation time has also been investigated (Roover and Steyaert, 2010).

The charge conservation principle is identified to be widely used in modelling the rectifier on monolithic integrated circuits (ICs). This technique is able to derive and deduce the equation to an integral as presented by Yi et al. (2007). However, a note of caution is that it produces a Riccatti equation at certain operation mode of the rectifier which could not be solved analytically if a particular solution is unknown (Bronshtein et al., 2004). Hence, Yi et al. (2007) employed a Taylor series expansion of the $\cos \omega t$ function to approximate the function around the peak of the integral. This is to achieve simplicity where the use of power series expansion may result in a complicated model

without producing valuable design insight in the developed model. The charge conversation principle by characterization of the transistors as diode-connected was proved to be simple by Ashry et al. (2008) and Rabén et al. (2012). Another modelling technique adopted by Gharehbaghi et al. (2017) approximated the steady-state voltage and current simulation waveform of the rectifier with a triangle geometry to formulate a function for developing the model. By using the conventional triangle geometric equation, a model was developed based on the waveform. However, over simplifying the expression has the potential to decrease the accuracy of the model.

The modified Bessel function is another solution for modelling the rectifier but was proven to be not an easy task due to its mathematical complexity (De Vita and Iannaccone, 2005). Abouzied and Sánchez-Sinencio (2015) managed to utilize the modified Bessel function to obtain the drain current and output voltage respectively in their models. In addition, Razavi Haeri et al. (2017) was able to model the rectifier in subthreshold operation and developed a unique model for low-power ambient RFEH application with this modelling solution. The Bessel function proposed by Razavi Haeri et al. (2017) was shown to be very effective and simple to be developed without compromising the accuracy of the model.

3.2.2 CCDD Rectifier

There are limited models available in regards to the CCDD rectifier. Recent CCDD rectifier model available for RFEH was published by Nariman et al. (2017) where the model is only applicable towards near-field RFEH or WPT systems where the density of input RF power, $P_{\mathrm{in,rec}}$ is large. The proposed model has intentionally neglected the subthreshold operation region claiming that this region is insignificant in the scope of its target application. Another CCDD rectifier model by Wei et al. (2011) proposed a CCDD model for RFEH through analyzing the current conduction of the circuit at different mode

of operation. However, the model is too complex to yield an accurate output value. Even though the model considered the subthreshold region in the analysis, the time interval for the forward and reverse operation has to be extracted which requires prior simulation results of the circuit. This contends the development of a model for the CCDD rectifier pronouncing the impracticality of the proposed model. Wei et al. (2011) and Nariman et al. (2017) have adopted the charge conservation principle to develop the models. However, Nariman et al. (2017) has neglected the integral for subthreshold operation mode and the model by Wei et al. (2011) lack simplicity and accuracy to aid the effective design of a rectifier for ambient RFEH.

To fill this gap, a novel and accurate model of the CCDD rectifier has been developed. The next section presents the mathematical solution to develop the novel CCDD rectifier model for ambient RFEH. The novel mathematical CCDD model in this work is simple in its derivation while achieving high accuracy compared to prior-art CCDD models.

3.3 Proposed CCDD Rectifier Model in Subthreshold Operation

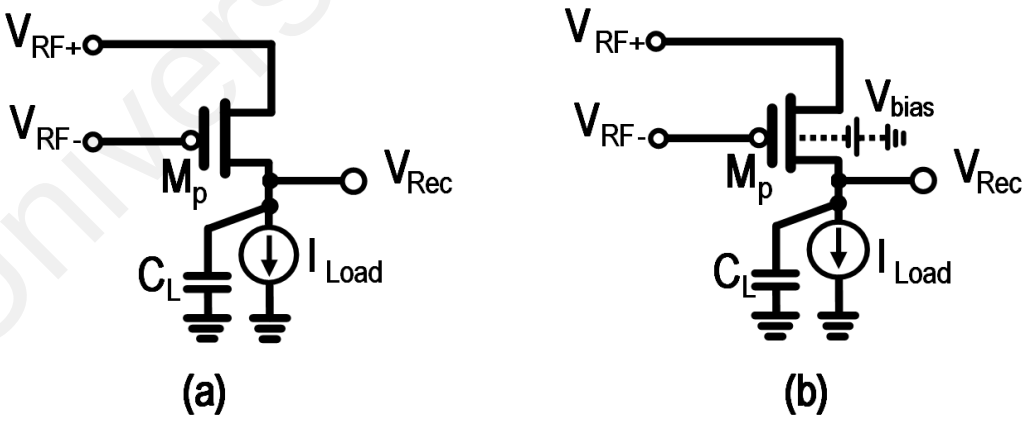

Figure 3.2: Circuit Model for Cross-Coupled Analysis: (a) Forward Conduction Mode (b) Reverse Conduction Mode

The charge conservation principle is first employed to obtain the core integrals for the CCDD rectifier's operation modes. The Bessel Function as a second mathematical solution is applied to solve the equation in which the new CCDD model is developed.

The Bessel Function is utilized without adding significant complexity to deduce the model of the CCDD rectifier for ambient RFEH.

The CCDD rectifier is first analyzed through DC analysis to derive the model of the rectifier. The model is developed by evaluating the PMOS transistor, M_{P} at the output terminal of a single-stage CCDD rectifier. Figure 3.2 shows the circuit analysis through the schematic of the PMOS transistor with its terminal labelled according to the voltages $V_{\mathrm{RF+}}$ and $V_{\mathrm{RF-}}$ at the input terminals of the rectifier. M_{P} is the PMOS transistor of a CCDD rectifier where the source(drain) terminal is shorted to the output load. C_{L} is the smoothing capacitor and the output load current is represented by I_{Load}.

As ambient RF energy is low, the rectifier will operate primarily in the subthreshold region in which the source-to-gate voltage satisfies the conduction $V_{\mathrm{sg}} < |V_{\mathrm{th}}|$. Equation 3.1 represents the subthreshold conduction equation of the transistor in CMOS technology.

$$I_{\mathrm{D,sub}} = I_{\mathrm{s0}} e^{\frac{V_{\mathrm{sg}}}{nV_{\mathrm{T}}}} \left[1 - e^{\frac{(-V_{\mathrm{sd}})}{V_{\mathrm{T}}}}\right](1 + \lambda_{\mathrm{sub}} V_{\mathrm{sd}}) \tag{3.1}$$

V_{sg} and V_{sd} are the source-gate and source-drain voltages, respectively. V_{T} is the thermal voltage, n is the slope factor and $(1 + \lambda_{\mathrm{sub}} V_{\mathrm{sd}})$ is the channel-length modulation. I_{s0} is the process dependent variable and it is defined in equation 3.2.

$$I_{\mathrm{s0}} = \mu C_{\mathrm{d}} {V_{\mathrm{T}}}^2 (W/L)\, e^{\,(-V_{\mathrm{th}} - V_{\mathrm{off}})/nV_{\mathrm{T}}} \tag{3.2}$$

μ is the channel mobility of the charge carrier and C_{d} is the capacitance of the depletion region beneath the gate cross sectional area in which C_{d} is expressed as $C_{\mathrm{d}} = \sqrt{e_{\mathrm{si}} q N_{\mathrm{ch}} / 2\Phi_{\mathrm{B}}}$ where e_{si} is the dielectric constant of silicon in Farad per meter square (F/m^2), q is the electron charge in coulombs, N_{ch} is the substrate doping density in cm^{-3},

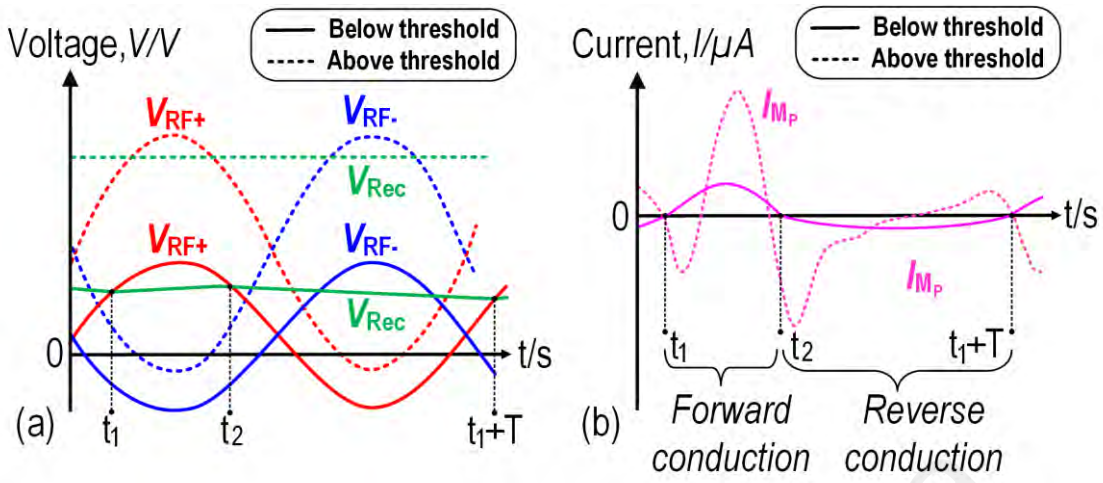

Figure 3.3: Transient Simulated Waveform of M_P: (a) Voltage (b) Current

and Φ_B is the built-in potential of the junction in volts. V_{off} is the subthreshold region offset voltage and V_{T} is the thermal voltage given by kT/q where k is Boltzmann's constant and T is the temperature in Kelvin. The terms μ, e_{si}, and q are natural constants while N_{sub} and Φ_{B} are process dependent according to the adopted foundry specification.

A periodic voltage and current at each terminal of transistor M_{p} in Figure 3.2 is illustrated in Figure 3.3(a) and 3.3(b) for subthreshold operation and mixed operation. By observing the waveforms for subthreshold operation in Figure 3.3, two distinct intervals can be observed. The current waveform of M_{p} for the mixed operation mode in Figure 3.3(b) can be seen to be more complex which will not be analyzed in this work as the analysis has already been conducted by Wei et al. (2011). Mixed mode operation is not part of the scope of the proposed model as this work focuses on ambient RFEH in which the transistors operate primarily in subthreshold region to satisfy the condition of $V_{\text{RF}\pm} < V_{\text{th}}$.

In reference to Figure 3.3(a), the first subthreshold conduction interval from t_1 to t_2 is the forward conduction where the current flow towards the load as depicted in Figure 3.3(b). Forward conduction occurs around the positive peak of $V_{\text{RF+}}$ as the voltage

potential of V_{Rec} is larger than V_{Rec} while the voltage potential $V_{\mathrm{RF-}}$ is negative, turning on M_{P}. Hence, current flows from $V_{\mathrm{RF+}}$ to V_{Rec} as depicted in Figure 3.3(b). The circuit analysis of this interval is shown in Figure 3.2(a). The second interval from t_2 to t_{1+T} is the reverse conduction where the current flows from the load back to the input RF source shown by the circuit analysis in Figure 3.2(b). This interval occurs when the potential of V_{Rec} is higher than the input $V_{\mathrm{RF}\pm}$ creating a reverse potential for the current to flow back to the source as the potential at $V_{\mathrm{RF+}}$ become more negative in respect to V_{Rec}.

To develop a new CCDD model, first the charge conservation principle is applied based on the operation mode of the rectifier in Figure 3.3. The accumulated charge at steady-state for a complete cycle of V_{RF} accounting both the forward and reverse current conduction is taken into consideration. In reference to Figure 3.2, the term $V_{\mathrm{RF+}}$ will be represented as $V_{\mathrm{a}} \cos \omega t$ where V_{a} is the peak value of the input RF voltage. Similarly, terminal $V_{\mathrm{RF-}}$ is the inverse of $V_{\mathrm{RF+}}$ which will be taken as $-V_{\mathrm{a}}\cos\omega t$.

By referring to the PMOS terminals in Figure 3.2(a) for forward conduction with the source terminal represented as $\mathrm{V_{RF+}}$, gate terminal as $V_{\mathrm{RF-}}$ and V_{Rec} as the drain terminal while assuming steady-state operation of the rectifier for a time t_1 to t_2, substituting the terms into equation 3.1 for forward conduction yields the accumulated charge for forward conduction mode as obtained in equation 3.3.

$$Q_{\mathrm{sub,fw}} = \int_{t_1}^{t_2} I_{\mathrm{sub,fw}}\, dt = \int_{t_1}^{t_2} I_{\mathrm{s0}} e^{\frac{V_{\mathrm{a}} \cos \omega t - (-V_{\mathrm{a}} \cos \omega t)}{nV_{\mathrm{T}}}} \left[1 - e^{\frac{-(V_{\mathrm{a}} \cos \omega t - V_{\mathrm{Rec}})}{V_{\mathrm{T}}}}\right] dt \qquad (3.3)$$

Alternatively, the drain and the source terminal are inversed for reverse conduction where $V_{\mathrm{RF+}}$ is now the drain terminal and V_{Rec} is the source terminal. Substituting the terms into equation 3.1 for a time interval from t_2 to $t_1 + T$ yields the expression for reverse conduction given by equation 3.4.

$$Q_{\text{sub,rv}} = \int_{t_2}^{t_1+T} I_{\text{sub,rv}}\, dt = \int_{t_2}^{t_1+T} I_{\text{s0}} e^{\frac{V_{\text{Rec}}+V_{\text{a}}\cos\omega t}{nV_{\text{T}}}} \left[1 - e^{\frac{-(V_{\text{Rec}}-V_{\text{a}}\cos\omega t)}{V_{\text{T}}}}\right] dt \tag{3.4}$$

In both equations for forward and reverse conduction intervals, the term $(1 + \lambda_{\text{sub}} V_{\text{sd}})$ is omitted as channel-length modulation of the transistor is less present during subthreshold operation. In addition, the slope factor, *n* is commonly approximated to 1 to simplify the expression (Razavi Haeri et al., 2017). Since there are two PMOS in the circuit, the expression accounts for the charges flowing through both PMOS transistors for a full cycle at steady-state which are substituted to equation 3.5.

$$Q_{\text{load}} = 2\left(Q_{\text{sub,fw}} - Q_{\text{sub,rv}}\right) \tag{3.5}$$

Taking the accumulated charge through both PMOS of equation 3.3 and 3.4 into equation 3.5 and simplifying the expression yields equation 3.6.

$$\begin{aligned}
\int_{t_1}^{t_1+T} I_{\text{load}} dt \; &= 2\int_{t_1}^{t_2} I_{\text{sub,fw}} dt - 2\int_{t_2}^{t_1+T} I_{\text{sub,rv}} dt \\
&= 2\int_{t_1}^{t_2} I_{\text{s0}} e^{\frac{V_{\text{a}}\cos\omega t-(-V_{\text{a}}\cos\omega t)}{nV_{\text{T}}}} \left(1 - e^{-\frac{-(V_{\text{a}}\cos\omega t-V_{\text{Rec}})}{V_{\text{T}}}}\right) dt \\
&\quad -2\int_{t_2}^{t_1+T} I_{\text{s0}} e^{\frac{V_{\text{Rec}}+V_{\text{a}}\cos\omega t}{nV_{\text{T}}}} \left[1 - e^{\frac{-(V_{\text{Rec}}-V_{\text{a}}\cos\omega t)}{V_{\text{T}}}}\right] dt \\
&= 2I_{\text{s0}} \int_{t_1}^{t_1+T} e^{\frac{V_{\text{a}}\cos\omega t}{V_{\text{T}}}} \left(e^{\frac{V_{\text{a}}\cos\omega t}{V_{\text{T}}}} - e^{\frac{V_{\text{Rec}}}{V_{\text{T}}}}\right) dt
\end{aligned} \tag{3.6}$$

It is observed that equation 3.6 constitutes a full period in its integral where the result can be independent of the time intervals t_1 and t_2. The full detailed derivation is attached in Appendix C. Solving equation 3.6 by calculating the integrals for $[0, T]$ in steady-state operation of the rectifier and isolating V_{Rec}, the novel CCDD model in subthreshold operation for ambient RFEH is developed and expressed in equation 3.7.

$$V_{\mathrm{Rec}} = V_{\mathrm{T}} \ln \left[\frac{I_{s0} I_0 \left(\frac{2V_{\mathrm{a}}}{V_{\mathrm{T}}} \right) - I_{\mathrm{load}}}{I_{s0} I_0 \left(\frac{V_{\mathrm{a}}}{V_{\mathrm{T}}} \right)} \right] \tag{3.7}$$

The term $I_0(x)$ in equation 3.7 is a zero-order modified Bessel function of the first kind which is denoted by:

$$I_0(x) = \frac{1}{\pi} \int_0^{\pi} e^{x \cdot \cos\theta} d\theta \tag{3.8}$$

The zero-order modified Bessel Function is adopted to account for the time-constant of the expression in equation 3.8 for the charge flow across a given cycle of the input RF voltage. The function is adopted because the solution in equation 3.7 could not be deduced using standard algebraic method to obtain the derived model from a single input RF cycle. To represent I_{load} as a resitive load in equation 3.7, an additional iteration to obtain V_{Rec} for $I_{\mathrm{load}} = 0$ is deduced to an actual I_{load} value for a given R_{L} using the standard ohm's law equation of $I_{\mathrm{load}} = V_{\mathrm{Rec}}/R_{\mathrm{L}}$ and substituting back the actual I_{load} to equation 3.7.

Next, to determine the total rectified output ($V_{\mathrm{Rec,total}}$) for a multi-stage CCDD rectifier, equation 3.8 is multiplied by *N*-stages. Hence, the expression of the model in a multi-stage CCDD rectifier for ambient RFEH is given by:

$$V_{\mathrm{Rec,total}} = N(V_{\mathrm{Rec}}) \tag{3.9}$$

The next section analyzes and tests the model by the conduction of experiments through theoretical calculation, simulation of the model and circuit implementation to validate the proposed CCDD rectifier model.

3.4 Experimental Results

3.4.1 CCDD Rectifier Mathematical Model

The novel CCDD rectifier model in equation 3.7 shows that in subthreshold operation, the variables V_{a} and I_{load} are the external determining factors of V_{Rec}. Internal variables include I_{s0} which is the process dependent variable and the design width (W). Alternatively, V_{T} is also a contributing factor that depends on the environmental temperature which the rectifier is operating.

Table 3.1: Numeric Value of Natural Constants and Process Specifications

Parameter	Value
Natural Constants	
Permittivity of free space, e_0	8.85×10^{-14} F/cm
permittivity of silicon	11.7
Relative permittivity of silicon, e_{si}	$11.7e_0$
Electron charge, q	1.60217×10^{-19} C
Mobility of holes in silicon, μ	450 $\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$
Boltzmann Constant, k	$1.3806 \times 10^{-19}\mathrm{m}^2\ \mathrm{kg}/(\mathrm{s}^2 K)$
Room temperature, T	300 ºK (27˚C)
Process Foundry	
Substrate doping, N_{sub}	10^{20} cm^{-3}
Bulk-Junction Potential, ϕ_{B}	1 V
Adopted Technology, L	0.18-μm

To test this new CCDD rectifier model, first a theoretical calculation is executed using the model using a programming tool (Python 3.6, 3.2 bits). The value of the variables has to be substituted into the novel CCDD model. Table 3.1 tabulates the parameters consisting of natural constants and the adopted foundry specifications with their corresponding values. The parameters of the foundry specification are obtained from the adopted CMOS technology. Figure 3.4 illustrate the flowchart of the program for calculating the rectified output voltage, $V_{\mathrm{Rec,total}}$ with the source code attached in Appendix D.

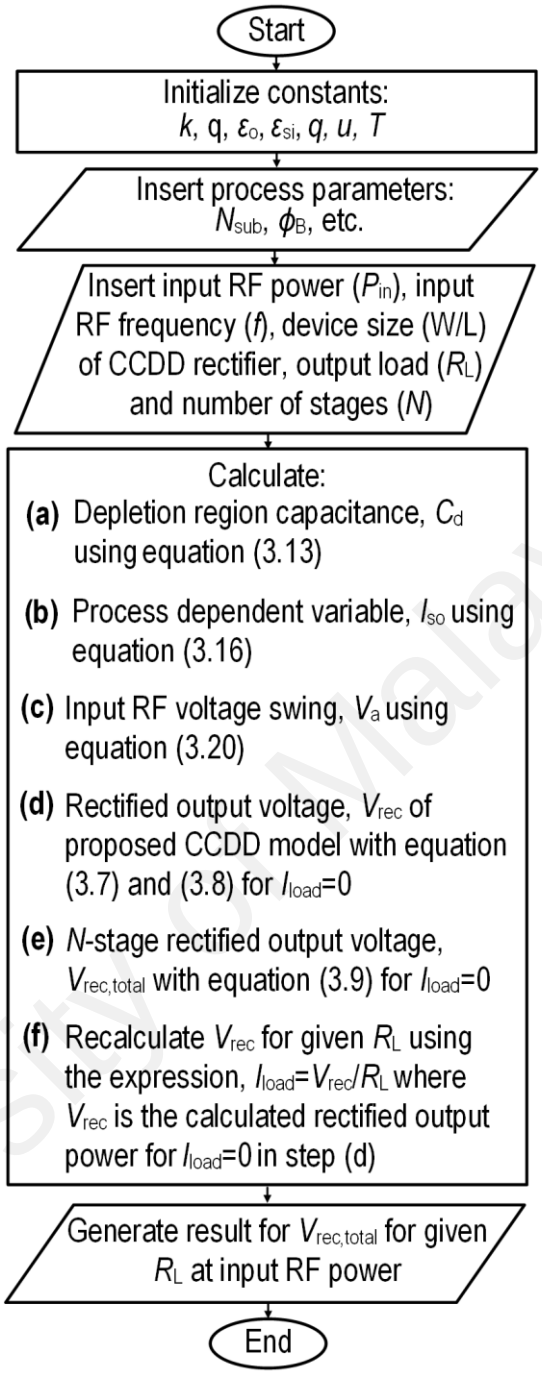

Figure 3.4: Program Flow Chart

The variables of I_{s0} are determined based on the selected technology process and V_T is assumed to be at room temperature (300 Kelvin). The plot of the model through theoretical calculation will be compared to the simulated and measured results.

Equation 3.10 is used to calculate V_T at room temperature which gives a value of 26 mV. The calculation is as follow:

$$V_T = kT/q \tag{3.10}$$

$$V_{\mathrm{T}} = (1.3806 \times 10^{-19})(300)/(1.60217 \times 10^{-19}) \tag{3.11}$$

$$V_{\mathrm{T}} = \underline{\mathbf{26}}\ \mathbf{mV} \tag{3.12}$$

Next, I_{s0} is calculated based on the process specification. The capacitance of the depletion region, C_{d} is first calculated with equation 3.13.

$$C_{\mathrm{d}} = \sqrt{e_{\mathrm{si}} q N_{\mathrm{ch}}/2\Phi_{\mathrm{B}}} \tag{3.13}$$

$$C_{\mathrm{d}} = \sqrt{(11.7)(8.85 \times 10^{-14})(1.60217 \times 10^{-19})(10^{20})/2(1)} \tag{3.14}$$

$$C_{\mathrm{d}} = \underline{\mathbf{0.0288 \times 10^{-4}}}\ \mathbf{F/cm^2} \tag{3.15}$$

With C_{d} calculated to be equal to $\underline{0.0288 \times 10^{-4}}$ F/cm^2, I_{s0} can be obtained through equation 3.16 based on adopted technology with $L = 0.18$-μm and $W = 1$-μm.

$$I_{\mathrm{s0}} = \mu C_{\mathrm{d}} {V_{\mathrm{T}}}^2 (W/L) \tag{3.16}$$

$$I_{\mathrm{s0}} = (450)(0.0288 \times 10^{-4})(0.026)^2\,(1 \times 10^{-6})/(0.18 \times 10^{-6}) \tag{3.17}$$

$$I_{S0} = \underline{\mathbf{4.8672}}\ \boldsymbol{\mu}\mathbf{A} \tag{3.18}$$

To have a standard process-dependent parameter to be used for the model, I_{S0} is defined with a parameter independent of the design width which gives a parameter of I_{S0} per unit width, (I_{S0}/W) with the unit in micro-ampere per micro-meter (μA/μm).

$$(I_{S0}/W) = \underline{\mathbf{4.8672}}\ \mu\mathrm{A}/\mu\mathrm{m} \tag{3.19}$$

The peak RF input amplitude, V_{a} could be obtained with equation 3.20 assuming a power-match case.

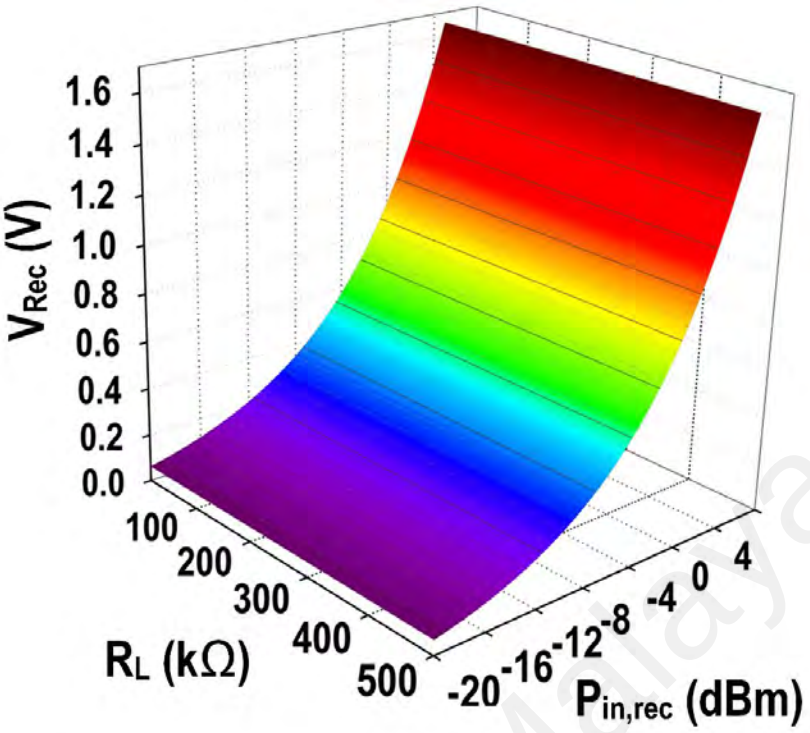

Figure 3.5: 3D Model plot of $V_{\mathrm{Rec,total}}$ versus R_{L} and $P_{\mathrm{in,rec}}$ [$Technology(L) = 0.18\ \mu m, N = 3, W = 50\ \mu m, f = 900\ MHz, V_T = 26mV, (I_{s0}/W) = 4.7686\ \mu A/\mu m$]

$$V_{\mathrm{a}} = \sqrt{8 \times P_{\mathrm{av}} \times R_{\mathrm{s}}} \quad \frac{R_{\mathrm{rec}}}{R_{\mathrm{rec}} + R_{\mathrm{s}}} \tag{3.20}$$

Equation 3.20 as described by Curty et al. (2005) takes a power-match case where the harvested power P_{av} is equal to the power entering the rectifier achieving a condition of $P_{\mathrm{av}} = P_{\mathrm{in,rec}}$ for an ideal impedance matching in an RFEH system. The input source impedance, R_{s} is the radiation resistance of the harvesting antenna with a typical value of 50-Ω and R_{rec} is the real input impedance component of the rectifier which is dependent on its design and process.

The newly developed model in equation 3.8 and equation 3.9 is tested through the programming tool to analyze the features of the novel CCDD model. The width of the transistor is taken to be 1-μm and the load is swept from zero to 500 kΩ. The number of rectifier stages is set to 3-stages and the range of $P_{\mathrm{in,rec}}$ is swept from -20 dBm to 3

dBm. Figure 3.5 shows a 3D plot of the tabulated results of the proposed CCDD model for a power-match case with $R_{\mathrm{rec}} = R_{\mathrm{s}} = 50\text{-}\Omega$. The results of the generated V_{Rec} for each tested load across $P_{\mathrm{in,rec}}$ range are tabulated and the tabulated data are plotted in Figure 3.5 which shows the relation of $V_{\mathrm{Rec,total}}$ with respect to $P_{\mathrm{in,rec}}$ and R_{L}.

The 3D plot of the proposed CDD rectifier model of a 3-stage rectifier in Figure 3.5 shows sufficient output voltage, $V_{\mathrm{Rec,total}}$ for low-power application across R_{L}. Besides that, R_{L} is observed to have very minimal but not negligible effect on $V_{\mathrm{Rec,total}}$ in subthreshold operation. While the PCE of the rectifier is known to be effected by V_{th}, however it is not of concern in subthreshold operation as V_{th} is not expressed in equation 3.7. As V_{a} does not exceed the transistor's V_{th}, PCE degradation due to leakage current will be more prominent in subthreshold operation. Hence, it can be concluded that common understanding regarding the PCE degradation of a rectifier due to the forward V_{th} drop is not evident in subthreshold operation for the CCDD rectifier.

3.4.2 Simulation Results

3.4.2.1 I_{s0} Extraction through Simulation

I_{s0}/W is extracted through circuit simulation to verify the theoretical value in equation 3.19. A distinct current, $I_{\mathrm{on}} = I_{\mathrm{s0}} = [(I_{\mathrm{s0}}/W) \cdot W\,]$ is first established as the drain current in strong inversion for $V_{\mathrm{sg}} = V_{\mathrm{th}}$ of the transistor (Kang & Leblebici, 2005). $e^{(-V_{\mathrm{th}} - V_{\mathrm{off}})}$ in the definition of I_{s0} in equation 3.2 is omitted during the extraction of I_{s0}. I_{on} can now be extracted through the *I-V* curve of transistor with the testbench set-up shown in Figure 3.6. Obtaining the value of the drain current, I_{D} when $V_{\mathrm{g}} = V_{\mathrm{th}}$ of the transistor yields I_{on}. Figure 3.6(b) shows the simulated *I-V* curve of the transistor in the adopted process to extract the value of I_{s0} through simulation.

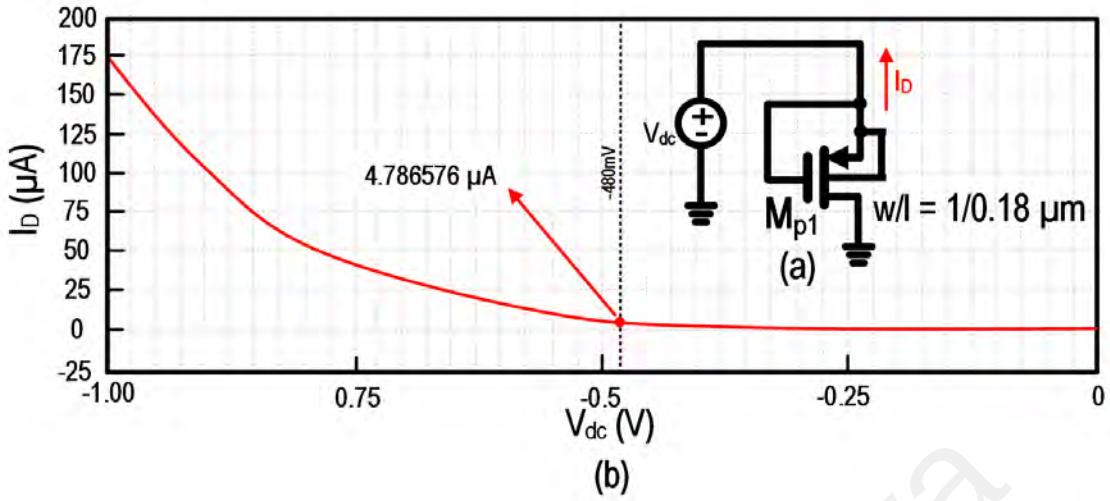

Figure 3.6: *I-V* Simulation. (a) Testbench Set-Up (b) *I-V* Curve of Transistor

Using the steps given to obtain I_{s0} of the adopted process, the simulated value of I_{s0} is $\underline{4.7872}$ μA. Hence, I_{s0}/W of the transistor can be extracted to be 4.7686 μA/μm corresponding to the transistor width of 1 μm through simulation. The extracted value is close ($\pm 2\%$) to the obtained theoretical value of $I_{s0} = \underline{4.7872}$ μA.

3.4.2.2 CCDD Rectifiers

Three distinct CCDD rectifiers with dissimilar width and number of stages are designed and optimized through an EDA software tool. Figure 3.7 shows the schematic of the three CCDD rectifier in the EDA circuit simulation tool. The rectifiers are designed for a targeted R_L of 200 kΩ which is a midpoint for the R_L test range from 10 kΩ to 500 kΩ. The specification of each rectifier is tabulated in Table 3.2. The technology foundry process adopted is a CMOS 0.18-μm platform for verification purposes. The model can be applied for other advanced CMOS technology as recently demonstrated by (Xu, Flandre & Blo, 2019). The V_{th} of the PMOS in the adopted CMOS process is ~|-480 mV|. The circuits are first simulated with a differential signal source at the input of the rectifier. 3-, 4- and 7-stages are selected for the rectifier to generate $V_{Rec,total}$ within 1V across the $P_{in,rec}$ range for R_L of 10 kΩ, to 500 kΩ. Next, the W of the transistors is optimized to achieve for best performance by which highest $V_{Rec,total}$ is obtainable.

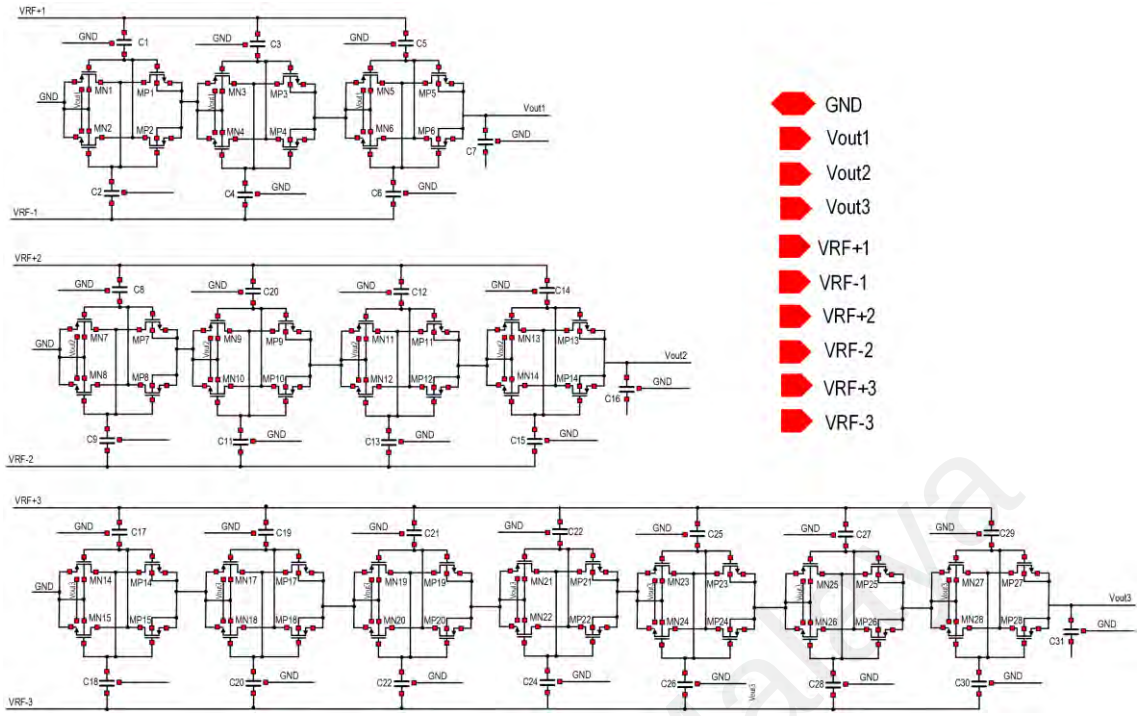

Figure 3.7: Schematic in EDA tool of the CCDD Rectifiers

Table 3.2: **Specifications of Fabricated Rectifiers**

Parameter	Value		
No. of stages	3	4	7
W/L	50/0.18 μm	60/0.18 μm	30/0.18 μm
$\mathbf{C_C}$	20 pF	20 pF	20 pF
$\mathbf{C_L}$	20 pF	20 pF	20 pF

Finally, the size of C_C and C_L are determined to provide sufficient charge storing and DC smoothing at the output.

Figure 3.8 shows the post layout design of the rectifiers with a GSGSG input RF configuration. The input traces of the rectifiers have to be fully symmetrical to obtain minimal mismatch of the differential input RF power signal entering the circuit. In addition, the input traces are to be as short as possible and placed close to the input pads to reduce parasitic effect which deteriorate the performance of the rectifier. As the output traces are carrying DC power, the output length of the traces to connect with the output

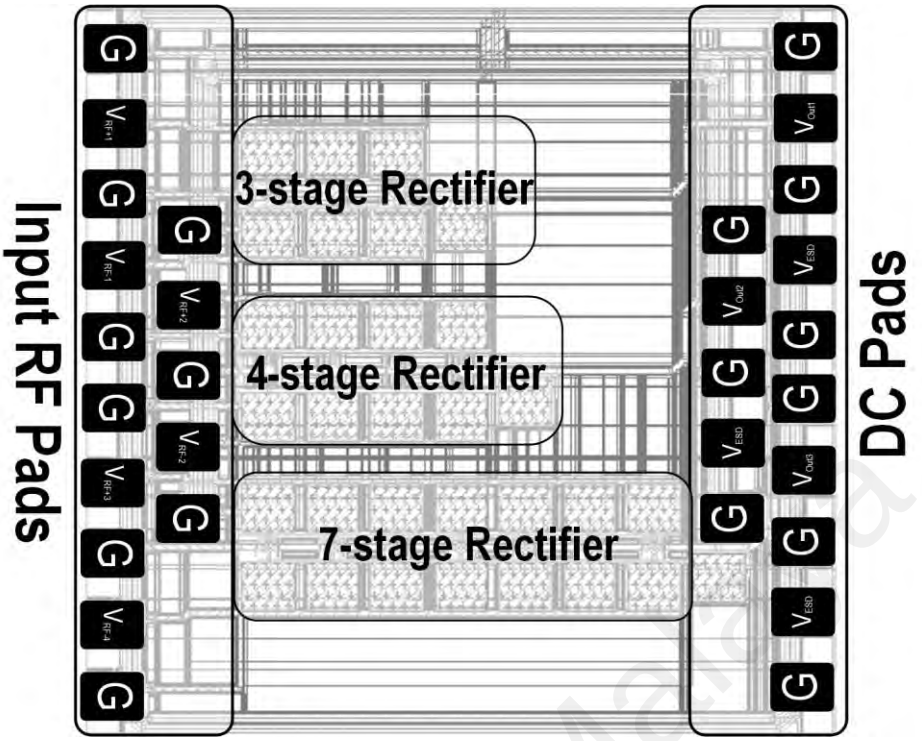

Figure 3.8: Layout of Rectifiers with Bond Pads in EDA Tool

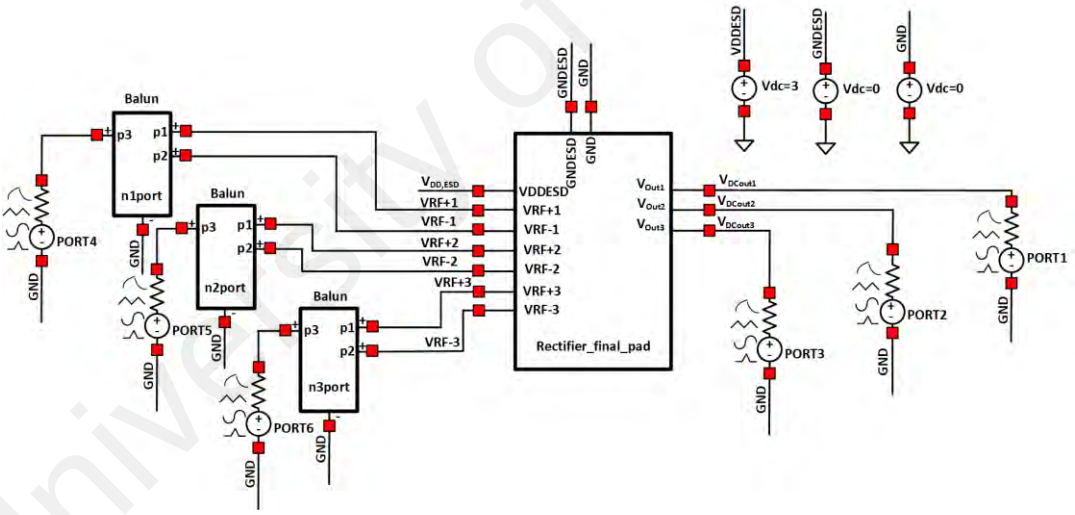

Figure 3.9: Test-Bench Simulation Set-Up

pad would not be affected much by the parasitic components, but produces a DC voltage drop which is negligible.

Figure 3.9 shows the simulation test-bench for the rectifiers. The external balun for generating the differential signal is uploaded to the test-bench to provide an accurate simulation output result to the hardware measurement. The balun emulates the actual measurement set-up that would be conducted for the rectifiers. The simulation results of

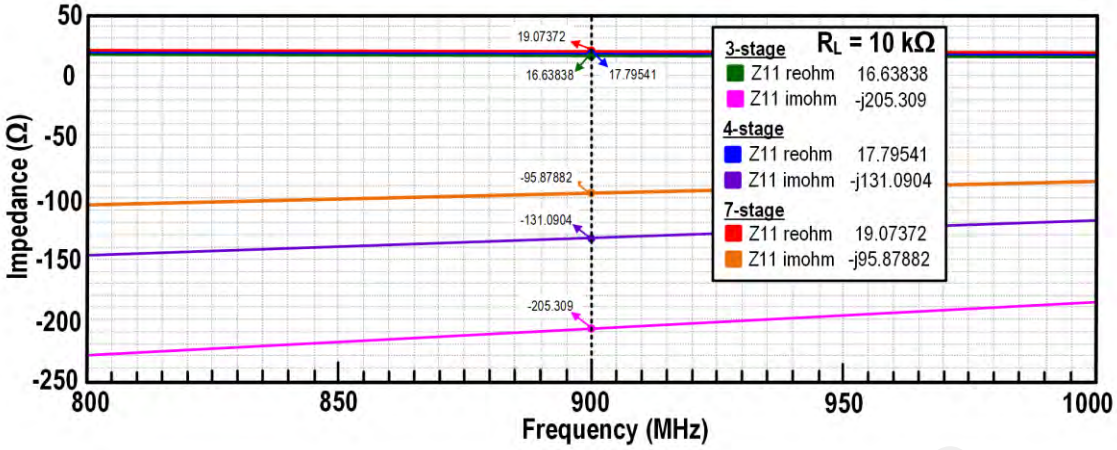

Figure 3.10: Input Impedance Simulation of Rectifiers

the rectifiers' input impedance for $R_{\mathrm{L}} = 10\ \mathrm{k\Omega}$ of each rectifier are shown in Figure 3.10. To account for the power loss and reflection losses of the rectifier, equation 3.21 is adopted to calculate $P_{\mathrm{in,rec}}$ accurately as no matching network is adopted.

$$P_{\mathrm{in,rec}}(\mathrm{dBm}) = P_{\mathrm{sg}}(\mathrm{dBm}) - P_{\mathrm{losses}}(\mathrm{dB}) - 10\log\left|S_{11,\mathrm{rec}}\right|^2 \qquad (3.21)$$

P_{sg} is the power for the signal generator, P_{losses} is the power losses associated with the balun and $S_{11,\mathrm{rec}}$ is the reflection coefficient of the rectifier.

To accurately calculate V_{a} to plot the model, equation 3.22 is adopted where $P_{\mathrm{in,rec}}$ represents the rectifier's input RF power and R_{rec} is the real component of the rectifier's input impedance.

$$V_{\mathrm{a}} = \sqrt{2 \times P_{\mathrm{in,rec}} \times R_{\mathrm{rec}}} \qquad (3.22)$$

The simulated impedance of the rectifiers for $R_{\mathrm{L}} = 10\ \mathrm{k\Omega}$ are $16.64 - j205.31\ \Omega$, $17.8 - j131.09\ \Omega$ and $19.07 - j95.88\ \Omega$ at a frequency of 900 MHz for the 3-, 4- and 7-stage rectifier, respectively. The simulated output results of the rectifiers are plotted along with the model and the measurement results in Figure 3.14. The values of $P_{\mathrm{in,rec}}$ are taken from the power entering the rectifier using equation 3.21 in the test bench where

the losses of the balun in the test-bench and the rectifier's reflection coefficient are subtracted.

3.4.3 Measurement Results

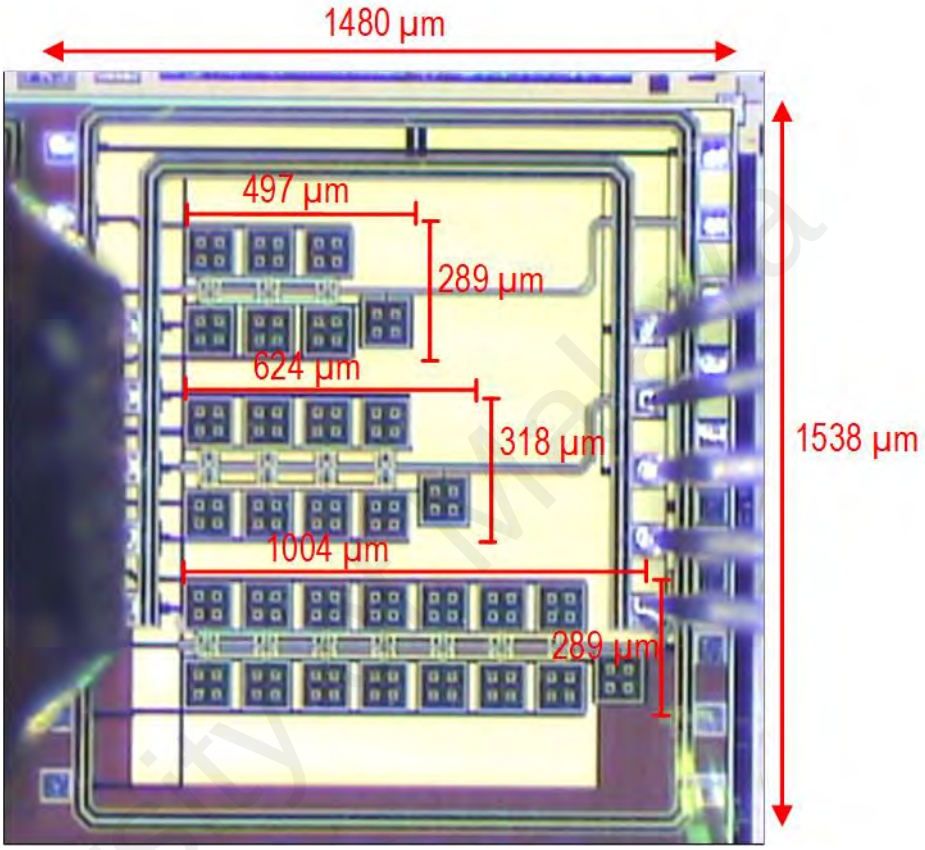

Figure 3.11: Micrograph of Fabricated Rectifiers

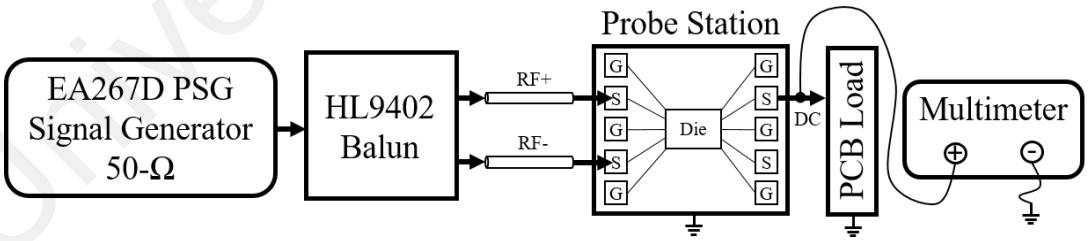

Figure 3.12: Schematic of Measurement Set-Up

Figure 3.11 shows the photomicrograph of the fabricated chip. Figure 3.12 shows the testbench of the measurement set-up to measure the rectifiers. A power signal generator (PSG) and an external broadband balun were used in the measurement. The broadband balun is adopted to generate the differential RF signal and to ensure true differential signal

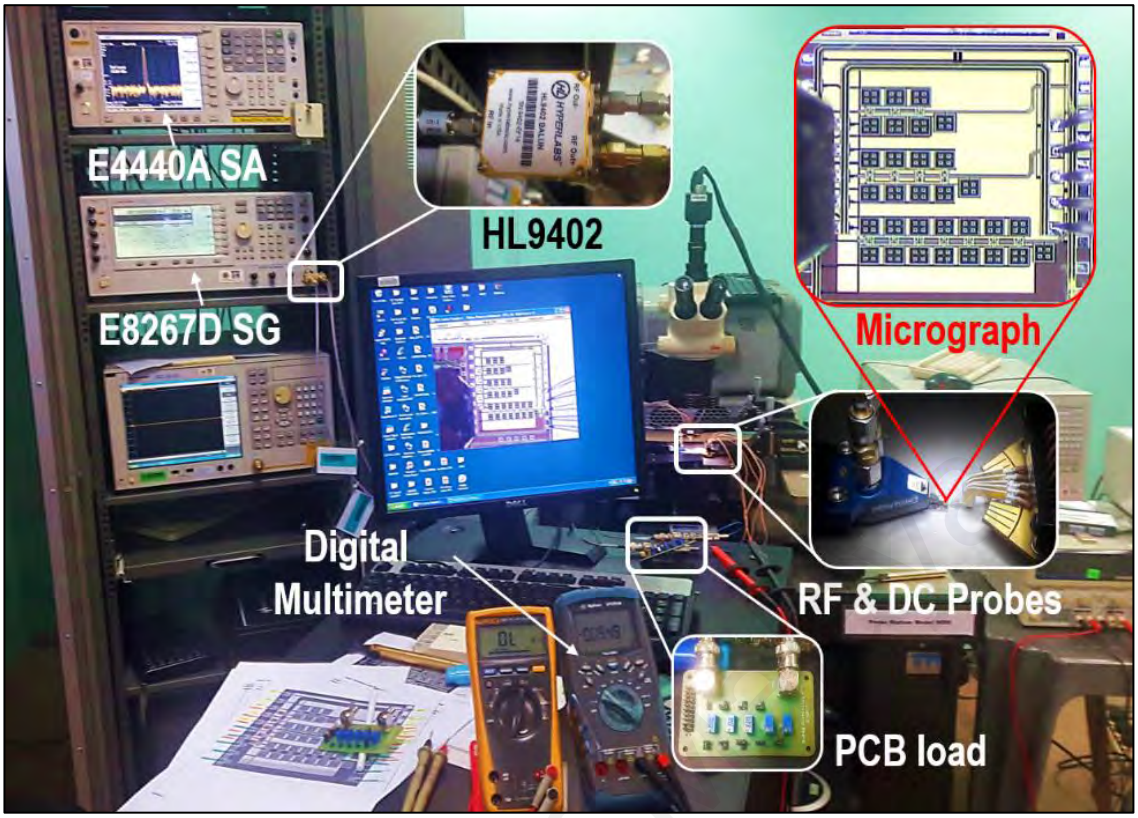

Figure 3.13: Actual Measurement Set-Up

is generated at the probe tips at the input of the rectifier. At a frequency of 900 MHz, the losses of the balun and cables are measured to be -3 dB and -0.7 dB, respectively. As the measurement set-up is similar to the simulation test-bench in Figure 3.9, equation 3.21 is adopted during the measurement of the rectifier to determine $P_{\text{in,rec}}$ and in tabulating the measurement results.

Figure 3.13 shows the actual measurement set-up for testing the rectifiers where the chip is mounted on the probe station. On-wafer probing technique was adopted in characterizing the circuit to increase the accuracy of the model in the experiment. A vector signal analyzer (VNA) was adopted to measure the balun and cable losses. The inputs of the rectifiers are connected to a PSG with an impedance of 50-Ω. The output load termination of the rectifiers is a tunable PCB resistor where a digital multimeter was used to measure the rectifiers' DC output voltage. Each rectifier is tested with the off-chip PCB load resistor with a value of 10 kΩ, 30 kΩ, 100 kΩ, 500 kΩ, and open-load to provide a

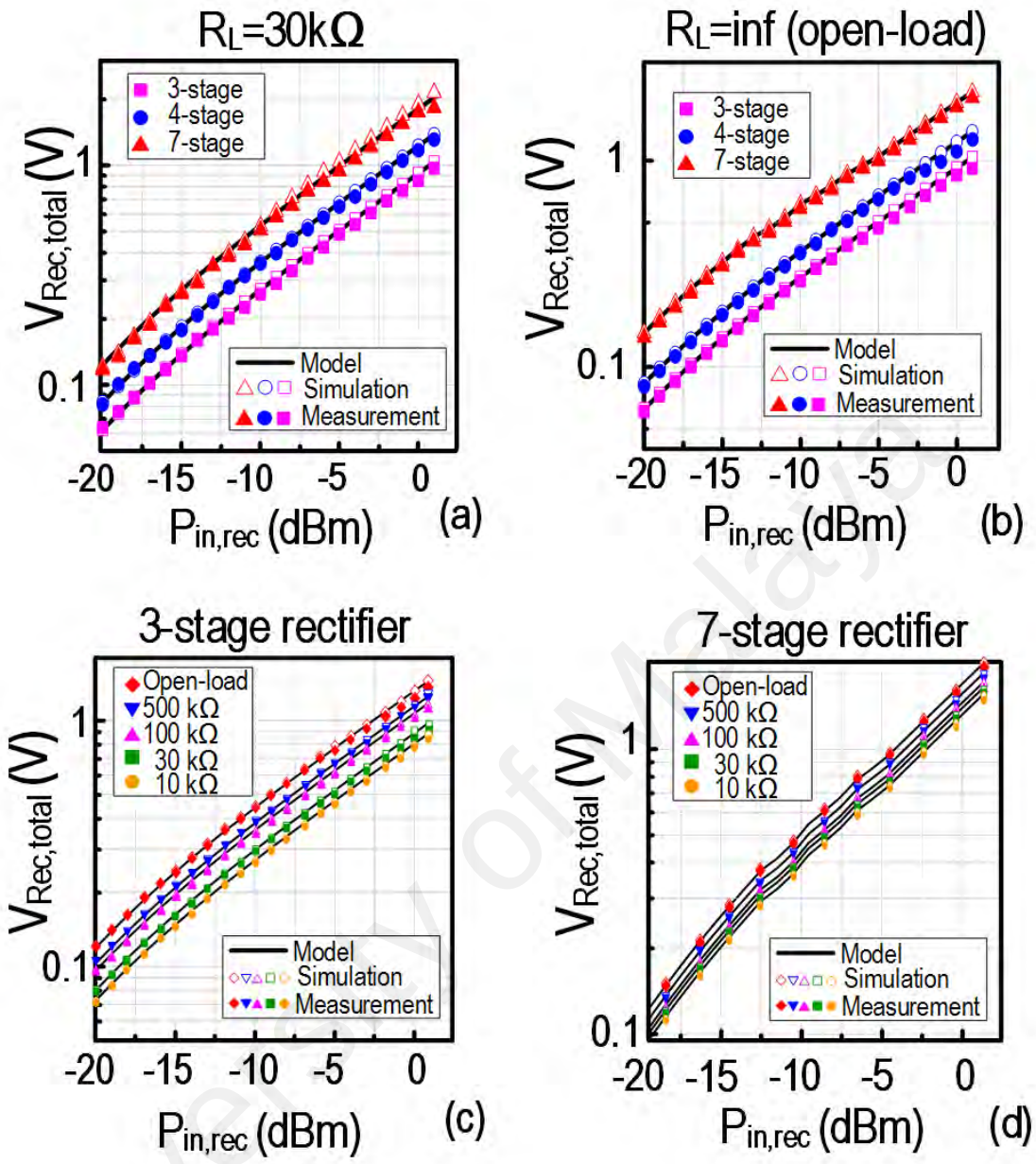

Figure 3.14: Model Plot and Measurement Results of the CCDD Rectifiers: (a) Output Voltage at 30 kΩ (b) Output Voltage for Open-Load (c) Output Voltage of 3-Stage (d) Output Voltage of 7-Stage

wide range of loading condition. The input RF power level of the PSG signal is swept from -20 dBm up to 3 dBm and the values of V_a in the simulation and measurement to plot the model are obtained through equation 3.23 (Razavi Haeri et al., 2017).

$$P_{\text{in,rec}} = V_a/2R_{\text{Rec}} \tag{3.23}$$

Figure 3.14 presents the final experimental results of the rectifiers. Figure 3.14(a) and Figure 3.14(b) present the results for R_L = 30 kΩ and open-load condition for each rectifier (3-, 4- and 7-stage), respectively. Alternatively, Figure 3.14(c) and Figure 3.14(d) plot the results for 3-stage and 7-stage rectifier configuration for all the tested loads (R_L =10, 30, 100, 500 kΩ and open load), respectively. Each figure plots the model, simulation and measured results for a visual comparison of its accuracy. The accuracy of the model is defined by equation 3.24 to measure the accuracy of the model to the measurement results.

$$accuracy(\%) = 100\% - error(\%)$$
$$= 100\% - \left(\left|\frac{|measured - model}{model}\right| \times 100\%\right) \quad (3.24)$$

The experiment results of each rectifier for all tested R_L achieve an accuracy of above 90% up to a level of 0 dBm and 80% up to an input of 3 dBm between the theoretical model and measurement output.

3.5 Discussion

As predicted by the novel CCDD rectifier model, the results show that higher number of stages raises $V_{\mathrm{Rec,total}}$. It is consistent in the measurement results that R_L has minimal but not negligible effect of $V_{\mathrm{Rec,total}}$ in subthreshold operation. Second, the effect of the forward drop is more prominent when the V_{RF} level is above the transistors' V_{th} as the term for V_{th} is absent in the expression of equation 3.7. However, as the input power approaches 3 dBm, the peak input RF voltage approaches the transistors' V_{th} causing the model to breakdown as the operation moves from subthreshold to mixed threshold operation. This effect can be seen in Figure 3.14 that the accuracy of the model starts to

Table 3.3: Comparison with Other CCDD Models

Author	This work	(Wei et al., 2011)	(Nariman et al., 2017)
Technology	0.18-μm	0.18-μm	0.04-μm
Topology	CCDD	CCDD	CCDD
Frequency (MHz)	900	900	60,000
V_{th} compensation	Static	Dynamic	Static
No. of stages	**3, 4 and 7**	1*, 2 and 3*	1 and 2
Input RF voltage	31.6mV – 316mV	n.a.	251mV – 794mV
Peak DC Voltage	2V @ 2 dBm	3.6V* @ 3 dBm	1.4V @ 8 dBm
Peak PCE	42.3%†	43%	32.8%
Model Peak Error	**9%**	11%	42%
Tested Load, R_L	**10/30/100/500-kΩ**	75 kΩ* & 160 kΩ	200 Ω to 2 kΩ
RF Harvesting Level	**Subthreshold operation**	Mix threshold operation	Above threshold operation

*Simulation Only †P_{in} = - 6 dBm for R_L = 10 kΩ, 7-stage rectifier

degrades when $P_{\text{in,rec}}$ increases beyond -5 dBm where V_{th} will have an effect towards $V_{\text{Rec,total}}$.

This work has filled the gap in the lack of a CCDD rectifier model in subthreshold operation for ambient RFEH. Besides that, the proposed model achieved the lowest peak error of 9% with the widest output load test range from 10 kΩ to 500 kΩ compared to prior works which only achieved a peak error of 11% as shown in Table 3.3. The use of Bessel function in the proposed CCDD rectifier model shows superiority by considering an interval which constituted a full period for a time interval 0 to T at steady-state in the application range of the rectifier. Compared to the model by Wei et al. (2011), the newly proposed CCDD model in this work does not require the exact time interval of the forward and reverse current conduction to be extracted which increases its accuracy. The significant of achieving lower peak error reduces the number of iteration of chip

fabrication needed during the testing phase, thus reducing the cost of production of developing a self-powered WSN in which the CCDD rectifier is a key circuit in the system.

An element that could cause the deviation in achieving lower error of the model is the second-order effects which was omitted for simplification of the model. Even with those simplifications made, the proposed CCDD rectifier model achieves a very high accuracy for the targeted application. Table 3.3 summarizes and compares this work with prior-art CCDD models. The proposed model in this chapter fills the gap in the lack of a CCDD rectifier model which has been tested on wide R_{L} range and rectifier stages compared to prior works.

3.6 Summary

A novel CCDD rectifier model in subthreshold operation for ambient RFEH has been presented. The novel mathematical model was developed using the subthreshold current conduction equation for a MOS transistor by applying the charge conservation principle to derive V_{Rec} which corresponds to the input RF level (V_{a}), number of stages (N) and output load (R_{L}). The results for the simulation and measurement exhibit high accuracy when compared to the theoretical calculations. The new CCDD rectifier model fills the gap in the lack of model available of the CCDD rectifier for ambient RFEH systems. The work in this chapter has been published in a volume of the IEEE Transactions on Circuits and Systems-II: Express Briefs.

CHAPTER 4: CCDD RECTIFIER WITH ENHANCED DYNAMIC RANGE

4.1 Chapter Overview

Though the conventional Cross-Coupled Differential-Drive (CCDD) rectifier as studied in Chapter 3 can effectively harvest ambient RF energy, its power conversion efficiency (PCE) is restricted due to the present of reverse-leakage current during the reverse conduction phase of the circuit's operation. Hence, this chapter presents a new CCDD architecture with enhanced PCE and dynamic range (DR) performance for ambient RFEH systems. The proposed CCDD architecture is first introduced and the working principle of the new architecture with the adopted multi-stage configuration are analyzed thereafter. Experimental results through hardware measurement are conducted and discussed. The summary concludes the findings at the end of the chapter.

4.2 Proposed CCDD Rectifier

4.2.1 DR Enhancement Concept

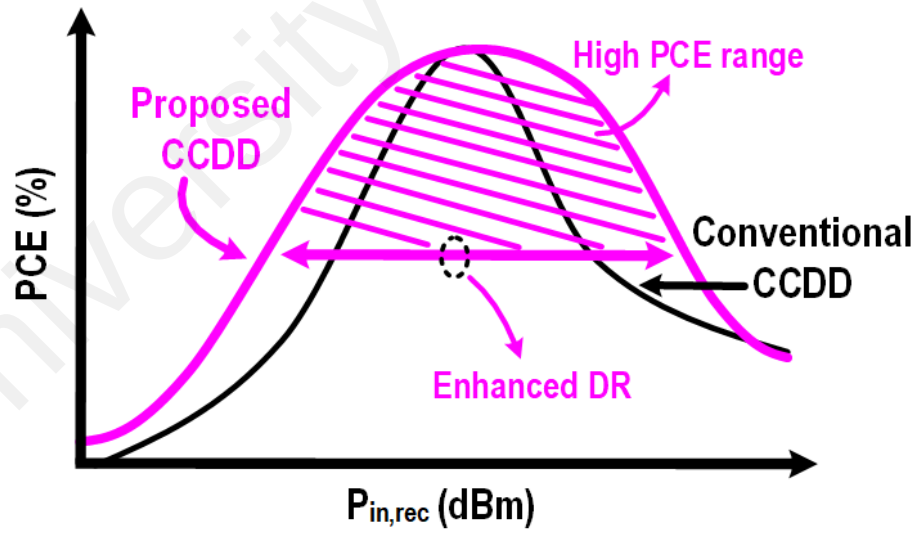

Figure 4.1: General PCE Curve of CCDD Rectifier

The proposed CCDD architecture in this work is designed to achieve an extension of 2.5 dB in its PCE DR as illustrated in Figure 4.1. To achieve an extended DR in its performance, the proposed CCDD architecture adopts a self-body-biasing technique and a gate-biasing scheme which are discussed in this chapter. Table 4.1 tabulates the

Table 4.1: Comparison of CCDD Architectures

CCDD Architecture	Conventional	Gate-biasing	Body-biasing	Proposed
Low $P_{\text{in,rec}}$	High turn-on voltage Low-leakage current	High turn-on voltage Low-leakage current	Low turn-on voltage High-leakage current	Low turn-on voltage Low-leakage current
High $P_{\text{in,rec}}$	High turn-on voltage High-leakage current	High turn-on voltage Low-leakage current	Low turn-on voltage High-leakage current	Low turn-on voltage Low-leakage current

comparison of CCDD architectures which highlights the benefit and limitation of various CCDD architectures with respect to the input RF power, $P_{\text{in,rec}}$ levels. It can be seen when $P_{\text{in,rec}}$ is low, reverse-leakage current is not evident in all CCDD architectures with the exception of the body-biasing scheme. Besides that, the conventional and gate-biasing CCDD architecture exhibit high turn-on voltage across $P_{\text{in,rec}}$ which degrades the PCE at low $P_{\text{in,rec}}$ and limits the sensitivity of the rectifier. High leakage current is also evident in the conventional and body-biasing architecture at high $P_{\text{in,rec}}$ levels due to the lower turn-on voltage which degrades the PCE. The trade-off is evident between achieving low leakage-current and low turn-on voltage across a wide $P_{\text{in,rec}}$ range. By overcoming this trade-off across $P_{\text{in,rec}}$ by ensuring a low turn-on voltage when $P_{\text{in,rec}}$ is low while achieve low leakage current at high $P_{\text{in,rec}}$ levels the DR range at which the rectifier achieve high PCE can be extended.

The proposed CCDD architecture in this work aim to achieve reduction in reverse-leakage current and low turn-on voltage across a wide $P_{\text{in,rec}}$ range to achieve an enhanced DR performance. The proposed CCDD architecture is able to achieve both the benefits of low turn-on voltage and reduced reverse-leakage current across a wide $P_{\text{in,rec}}$

range. Having the benefit of low reverse-leakage current and low turn-on voltage across $P_{\text{in,rec}}$, the DR performance of the rectifier is significantly improved.

4.2.2 Proposed CCDD Architecture

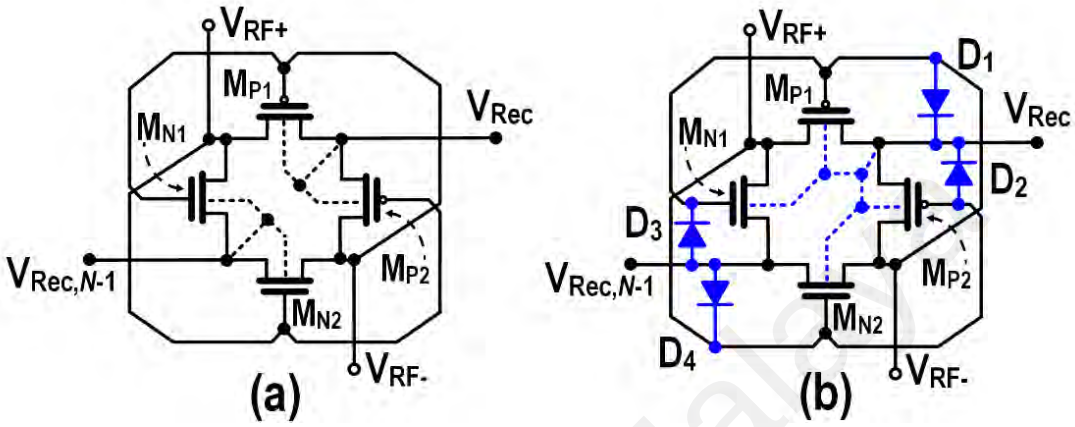

Figure 4.2: CCDD Rectifier Architecture: (a) Conventional (b) Proposed

Figure 4.2(b) presents the schematic of the proposed CCDD architecture. Transistors M_{P1}, M_{P2}, M_{N1} and M_{N2} are transistors in a conventional CCDD architecture. The novelty of this circuit is in the fusion of a self-bulk-biasing and gate-biasing scheme to overcome the trade-off of achieving low turn-on voltage and low reverse-leakage current. The bulk of all the transistors (NMOS and PMOS) are shorted to the highest potential at V_{Rec} of the rectifier and $V_{\text{Rec},N-1}$ is the rectified output voltage of the prior rectifier stage in a multi-stage configuration.

The first feature of the proposed architecture is the gate-biasing scheme implemented through diode-connected MOS transistors (D_{1-4}) at the gate to source (drain) of M_{P1}, M_{P2}, M_{N1} and M_{N2}. The gate-biased technique is implemented to reduce the reverse-leakage current during the negative bias and to produce large forward current through the diode-connected MOS during forward conduction. This technique creates a large threshold voltage when the level of the input RF voltage, $V_{\text{RF}\pm}$ swings below the rectified

output voltage, V_{Rec} which restrict current from flowing back to the source due to the higher DC potential of V_{Rec} with respect to $V_{\mathrm{RF}\pm}$.

The second feature of the proposed CCDD rectifier is the dynamic bulk-biasing technique for reducing the transistors' V_{th} to create a low turn-on voltage. This technique reduces the voltage drop across the transistors and provide more current to flow to the load during the turn-on state which simultaneously increases the sensitivity. A constant negative potential is applied to the bulk of the PMOS to reduce the threshold of the PMOS transistors. However, there is no negative DC potential passively generated by this structure which prevents the turn-on voltage of the PMOS to be reduced. Hence, this method of bulk-biasing only reduces the turn-on voltage of the NMOS which through experiment, proven to be sufficient in improving the performance of the rectifier. A detailed working principle of the proposed CCDD architecture is discussed in the next subsection.

4.2.3 Working Principle of Proposed CCDD Architecture

Figure 4.3 illustrates the working principle of the proposed CCDD architecture. The operation of the rectifier at low $P_{\mathrm{in,rec}}$ is illustrated in Figure 4.3(a) and 4.3(b) for the positive ($V_{\mathrm{RF+}} > V_{\mathrm{RF-}}$) and negative phase($V_{\mathrm{RF+}} < V_{\mathrm{RF-}}$) of the RF input voltage cycle, respectively. All diodes are off when $P_{\mathrm{in,rec}}$ is low as the diodes exhibit a large potential due to its V_{th}, emulating as an open-circuit. Therefore, the diodes have minimal effect when $P_{\mathrm{in,rec}}$ is low. Alternatively, the rectified voltage, V_{Rec} biases the bulk of the NMOS to reduce the turn-on voltage. With a lower turn-on, the NMOS allows the transistor to be effective in forming the channel in the depletion region for more current to flow. At high $P_{\mathrm{in,rec}}$, the diodes would turn-on by operating with respect to phase of the input RF voltage, $V_{\mathrm{RF}\pm}$ as shown in Figure 4.3(c) and Figure 4.3(d). The voltage potential of V_{Rec}

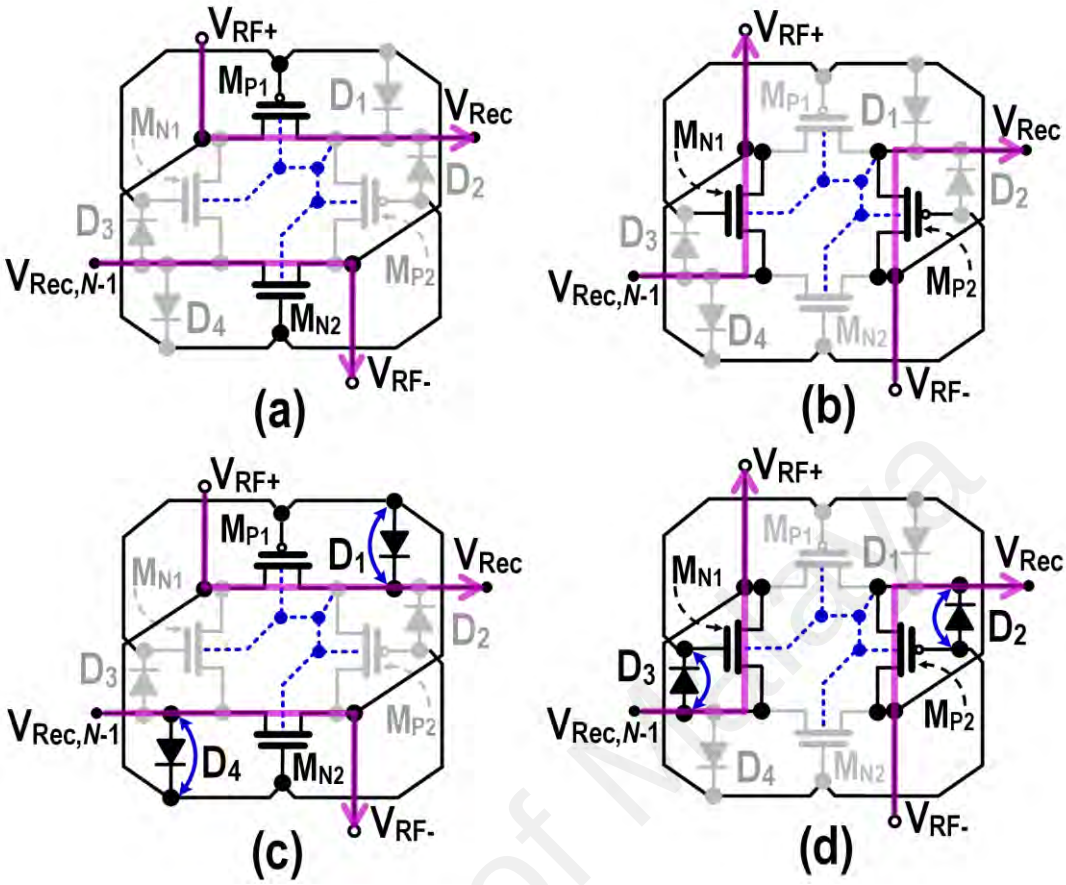

Figure 4.3: Operational Principle of the Proposed CCDD Architecture: (a) Low-power, Positive-cycle (b) Low-power, Negative-cycle (c) High-power, Positive-cycle (d) High-power, Negative-cycle

at the PMOS and $V_{\mathrm{Rec,N-1}}$ at the NMOS creates a large DC voltage at the terminal of the diodes as $V_{\mathrm{RF\pm}}$ swing for the diodes to operate.

To comprehend the working principle of D_{1-4} at high $P_{\mathrm{in,rec}}$, the adopted diode-connected MOS is analyzed through the diode's *I-V* curve in Figure 4.4. $D_{1,2}$ are the diode-connected MOS between the gate and drain terminals of the PMOS transistors. When $V_{\mathrm{RF\pm}} > V_{\mathrm{Rec}}$, $D_{1,2}$ are in forward bias as shown in Figure 4.3(c) and Figure 4.3(d). The potential of $D_{1,2}$ between the gate and drain terminals of the PMOS is $V_{\mathrm{D}} = V_{\mathrm{gd}} = V_{\mathrm{RF\pm}} - V_{\mathrm{Rec}}$ as shown in Figure 4.4. This increases the forward current from $V_{\mathrm{RF\pm}}$ to V_{Rec} through $D_{1,2}$ which increases the total output charge, thus improving the sensitivity and PCE performance of the rectifier. Alternatively, as $V_{\mathrm{RF\pm}} < V_{\mathrm{Rec}}$ which occurs during

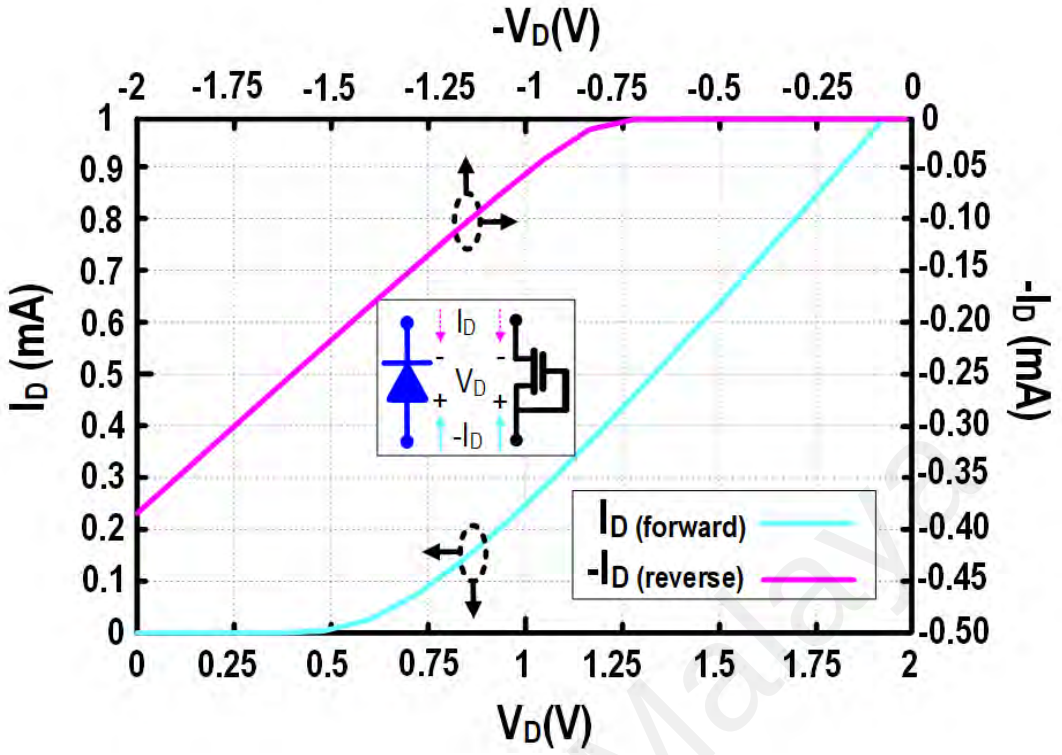

Figure 4.4: *I-V* Curve of Diode-Connected MOS

the rising and falling phase of $V_{\mathrm{RF}\pm}$, $D_{1,2}$ are reverse bias where $V_{\mathrm{D}} = V_{\mathrm{gd}}$ becomes more negative. $D_{1,2}$ would emulate a large resistor which suppresses the reverse-leakage current through $M_{\mathrm{P}1,2}$. As potential of V_{D} exceeds the negative conduction voltage of the diodes around $V_{\mathrm{D}} = -0.75\mathrm{V}$ as shown in Figure 4.4, slight leakage-current through $D_{1,2}$ is bound to occur. However, the amount of current conduction through $D_{1,2}$ is significantly lower when the potential of V_{D} is positive. The ratio of the forward to reverse current through $D_{1,2}$ would be large which uphold the PCE performance of the rectifier.

Alternatively, the terminals of $D_{3,4}$ at the NMOS transistors are inversed where the anode and cathode junctions of the diodes are shorted between the source and gate, respectively. At high $P_{\mathrm{in,rec}}$ and $V_{\mathrm{Rec},N-1} > V_{\mathrm{RF}\pm}$, $D_{3,4}$ are in forward bias where the potential of the diodes is given as $V_{\mathrm{D}} = V_{\mathrm{sg}} = V_{\mathrm{Rec},N-1} - V_{\mathrm{RF}\pm}$. This condition occurs during the rising and falling phase of $V_{\mathrm{RF}\pm}$. Additional forward current path from $V_{\mathrm{Rec},N-1}$ to $V_{\mathrm{RF}\pm}$ is created through $D_{3,4}$ during this operational phase. This additional

path improves the forward current conduction, improving the PCE. Alternately, when $V_{\mathrm{Rec},N-1} < V_{\mathrm{RF}\pm}$, $D_{3,4}$ are in forward bias. $D_{3,4}$ would emulate a large resistor to suppress the reverse-leakage current flowing from $V_{\mathrm{RF}\pm}$ to $V_{\mathrm{Rec},N-1}$ through $M_{\mathrm{N1,2}}$. The concept of the bulk-biasing to decrease the turn-on voltage of the NMOS devices remains the same for high $P_{\mathrm{in,rec}}$.

4.2.4 Multi-Stage Configuration

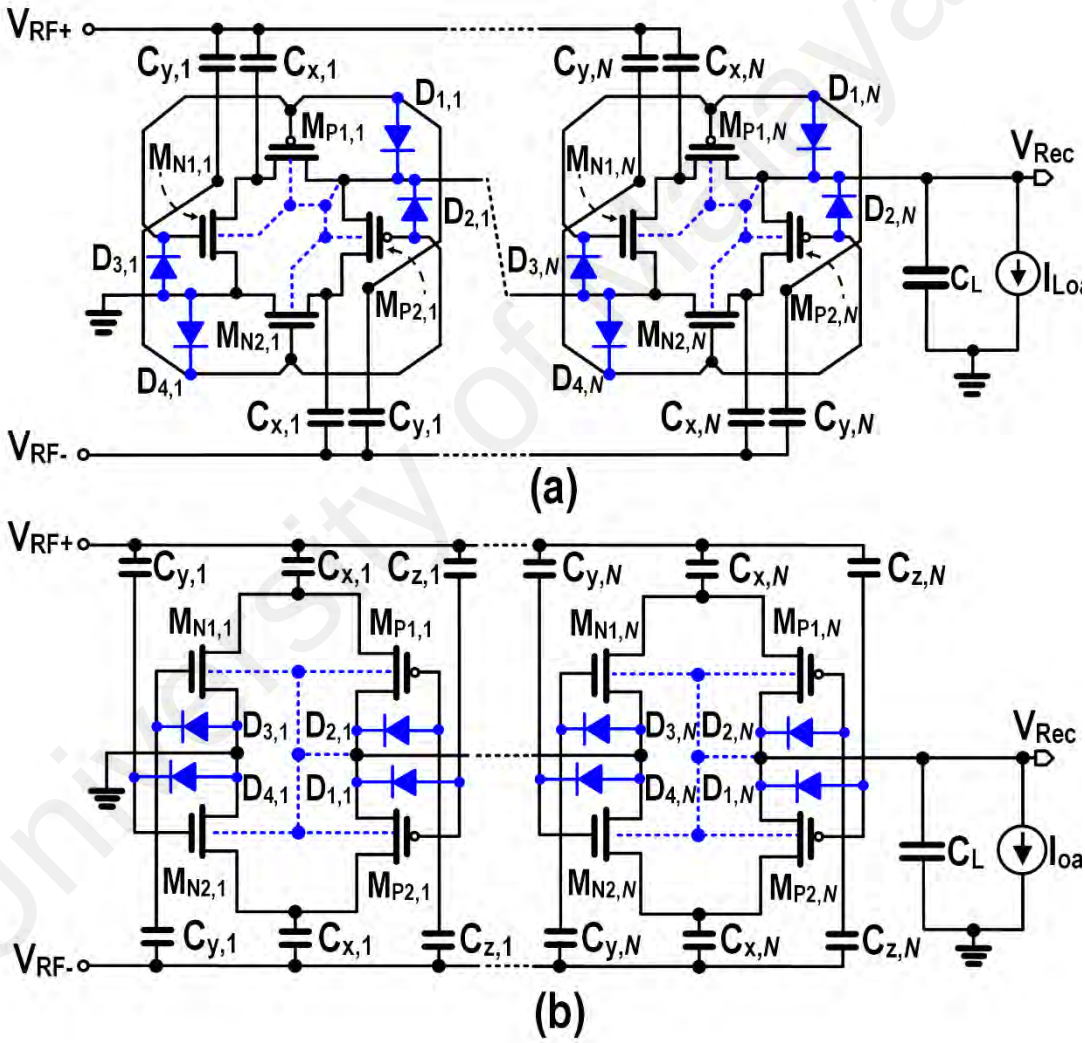

Figure 4.5: Multi-stage Configuration of Proposed Rectifier: (a) Shared-capacitor coupling (SCC) (b) Individual-capacitor coupling (ICC)

A single rectifier cell is typically cascaded to create a multi-stage rectifier with N number of stages as shown in Figure 4.5 to achieve a higher V_{Rec} at the output when

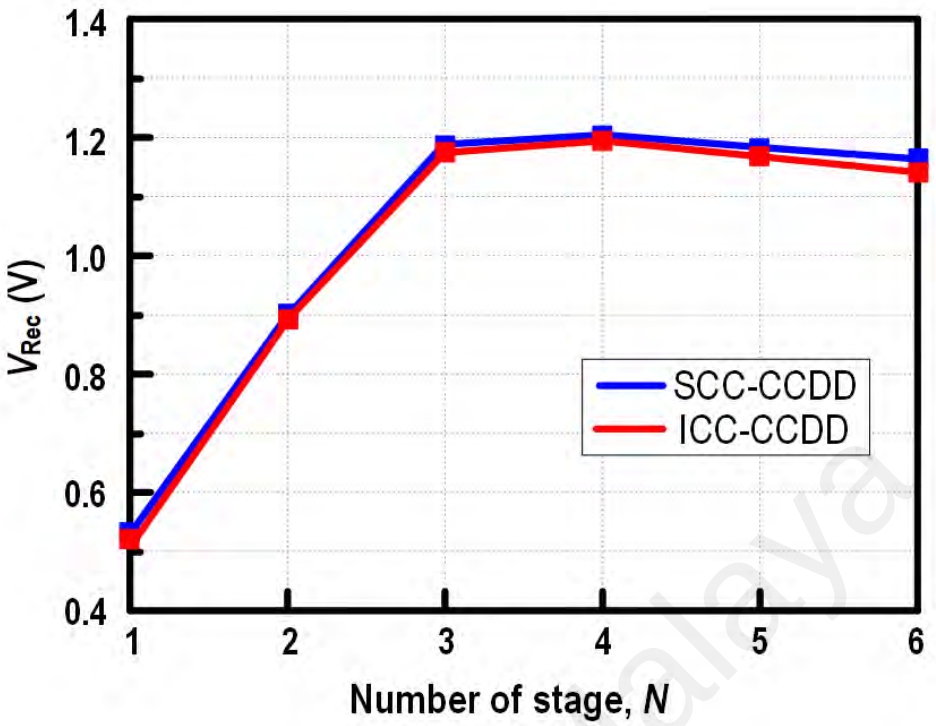

Figure 4.6: V_{Rec} versus Rectifier Stages for R_{L} = 100 kΩ and $P_{\mathrm{in,rec}}$= -18 dBm

implemented in an RFEH system. It is well understood that IC rectifiers cascaded for higher number of stages would increase V_{Rec}. However, there are two reasons which refute this claim. First, a theoretical limit denoted by equation 4.1 precludes the value of V_{Rec} due to its proportionality to $P_{\mathrm{in,rec}}$ assuming a fixed value of PCE and R_{L}.

$$V_{\mathrm{Rec}} = \sqrt{PCE \cdot P_{\mathrm{in,rec}} \cdot R_{\mathrm{L}}} \tag{4.1}$$

It would be redundant to further increase the number of stages as V_{Rec} would saturate. The second reason is the inherent V_{th} drop and reverse-leakage current of the rectifier would detriment the PCE by degrading V_{Rec} as the number of stages increases. Figure 4.6 shows the plot of V_{Rec} with respect to the number of stages for a fixed $P_{\mathrm{in,rec}}$ and R_{L}.

Achieving the highest V_{Rec} as possible while yielding the highest PCE is desirable without increasing the detrimental effect of the forward V_{th} drop and reverse-leakage current in the rectifier. Hence, through iterative simulation of the proposed rectifier, a 3-

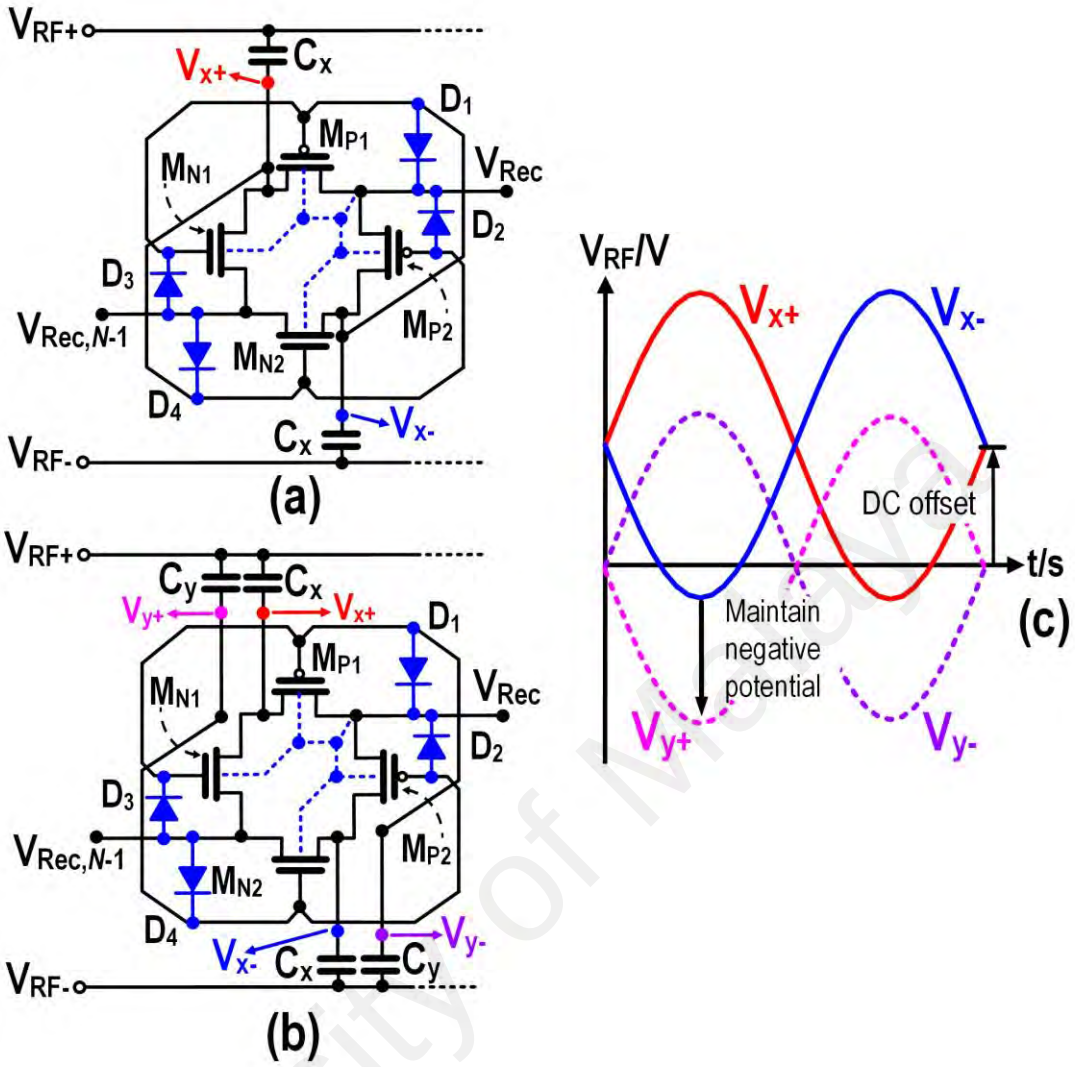

Figure 4.7: Coupling-Capacitor Configuration: (a) Single Coupling-Capacitor (b) Split Coupling-Capacitor (c) Terminal Voltage Waveform

stage configuration has been identified to be the optimal number of stages to achieve a high value of V_{Rec} for a load of $R_{\mathrm{L}} = 100$ kΩ where increasing the rectifier stages further would not cause significant rise in the value of V_{Rec}. Increasing beyond 3-stages is redundant and could be detrimental to the PCE of the rectifier for larger number of stages.

The proposed CCDD rectifier is implemented with two coupling-capacitor configurations as shown in Figure 4.5. The concept of both coupling-capacitor configurations shares a similarity in its purpose to isolate the pumping capacitor from the

gate-biasing capacitors. Figure 4.7 explains further the concept of the capacitor coupling techniques.

The configuration of the conventional CCDD rectifier shown in Figure 4.7(a) consists of only a single coupling capacitor, C_{x} for each RF input terminal. A single coupling capacitor is sufficient as a DC block to isolate $V_{\mathrm{RF}\pm}$ from the rectifier cell. However, as C_{x} simultaneously functions as a pumping capacitor, C_{x} would accumulate charges which creates a DC offset voltage illustrated through the waveform in Figure 4.7(c). This is undesirable as the DC offset reduces the negative voltage of $V_{\mathrm{RF}\pm}$ to effectively bias the PMOS transistors in the rectifier.

To overcome the drawback of a single coupling capacitor, capacitor C_{x} is decoupled from the gate of the transistors with an additional capacitor, C_{y} isolates the gate and drain (source) terminal of the input RF terminal the rectifier cell. This configuration isolates the gate biasing of the transistor through C_{y} and removes the DC offset effect due to the pumping capacitor, C_{x}, as shown in Figure 4.7(b). Therefore, the DC offset of C_{x} will not affect the biasing of the transistors to uphold the negative potential for biasing the PMOS transistors shown in the terminal waveform in Figure 4.7(c). This allows C_{y} to focus solely on biasing the gate of the transistors without being affected by the DC offset.

Two methods of the capacitor coupling are implemented in this work. The first capacitor coupling configuration is the shared-capacitor coupling (SCC-CCDD) where C_{y} is shared between the gates of the corresponding NMOS and PMOS transistors shown in Figure 4.5(a). The next configuration is the individual-capacitor coupling (ICC-CCDD) where C_{y} is further split to enhance the isolation of the gates of each transistor in the rectifier. The ICC-CCDD is able to reduce the input impedance $Z_{\mathrm{in,rec}} = R_{\mathrm{in,rec}} - j/\omega C_{\mathrm{in,rec}}$ of the rectifier due to the additional capacitors connected in parallel. Lower

input impedance is desirable to improve the peak value of $V_{RF\pm}$ for driving the gates of the rectifier. This configuration also provides supports when designing the impedance matching network (IMN) as the CCDD rectifier typically exhibits a large value for $Z_{in,rec}$.

4.3 Experimental Results

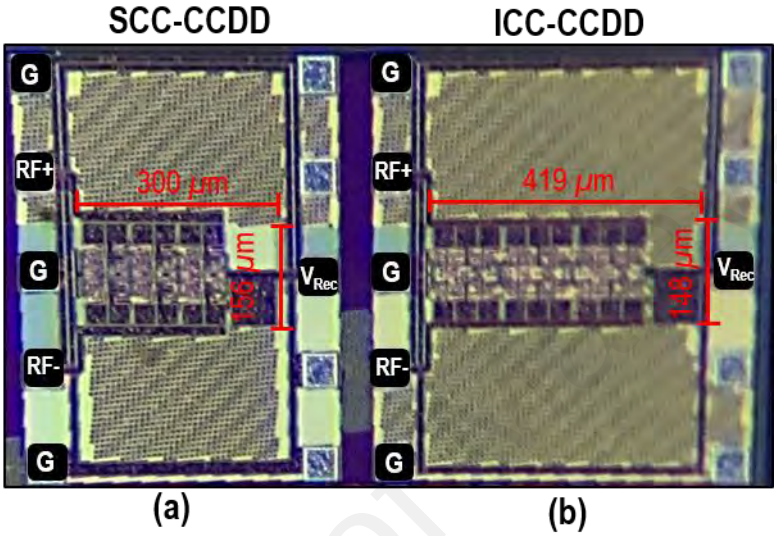

Figure 4.8: **Chip Micrograph (a) SCC-CCDD (b) ICC-CCDD**

Table 4.2: Specifications of Rectifiers

Device	SCC & ICC
$M_{P1,2}$	12 μm/0.13 μm
$N_{M1,2}$	4 μm/0.13 μm
D_{1-4}	1 μm/0.13 μm
$C_{C\ (x,y,z)}$	1.012 pF
C_L	5.012 pF

The rectifiers were fabricated on CMOS 0.13-μm technology where the photo photomicrograph of the rectifiers along with its specifications are shown in Figure 4.8. The specifications of the rectifiers are listed in Table 4.2. The CMOS 0.13-μm technology was adopted due to the limited analog voltage range the transistors could handle in advanced IC technologies as the transistor size decreases (Daly et al., 2018). Without the restriction of limited analog voltage range allows the rectifiers to operate at a wide

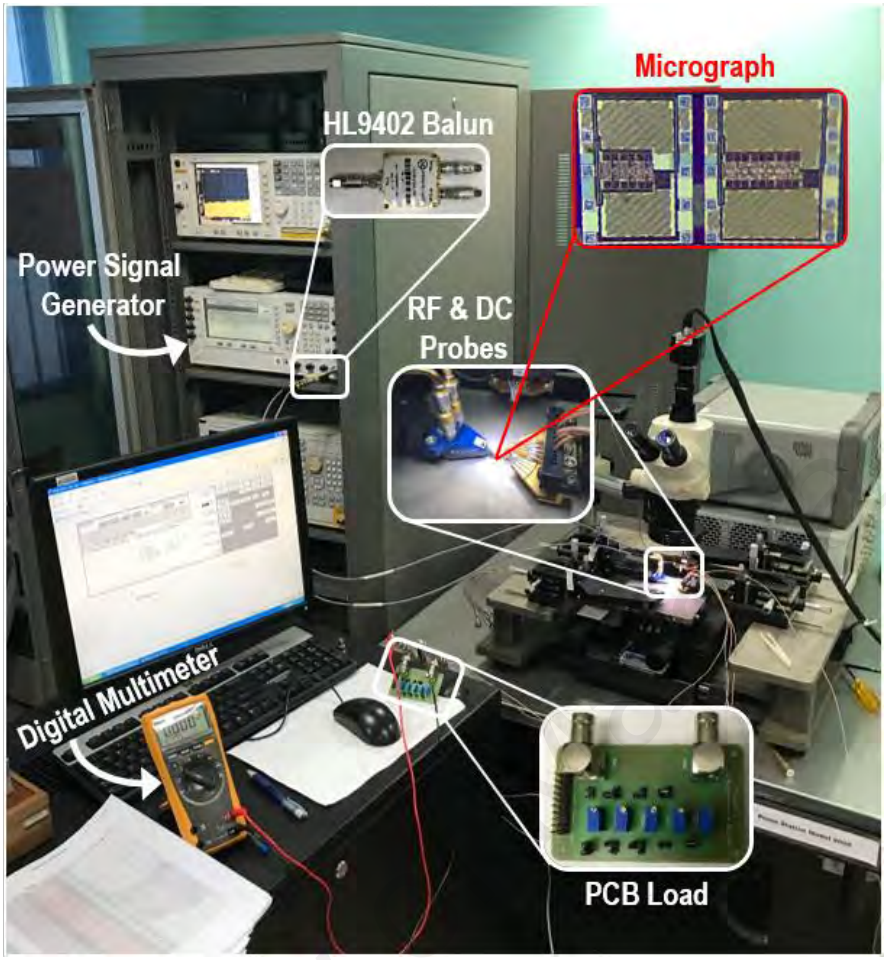

Figure 4.9: **Measurement Set-Up**

$P_{\text{in,rec}}$ range. Alternatively, the measurement set-up adopted to test the rectifiers is shown in Figure 4.9. The experimental equipment, set-up and procedure for the simulation and measurement of the rectifiers are identical as in section 3.4.2 and section 3.4.3 respectively of this thesis. The power signal generator is swept from -30 to 10 dBm with 5 samples of the chip tested to measure V_{Rec}. The measured V_{Rec} of the SCC-CCDD and ICC-CCDD are plotted in Figure 4.10(a) and Figure 4.10(b), respectively.

The average measured results of the 5 samples are plotted along with the conventional and state-of-the-art CCDD architectures in Figure 4.11. The measurement results show that V_{Rec} is enhanced across a wide $P_{\text{in,rec}}$ range for the same $R_{\text{L}} = 100$ kΩ. It can be seen that the efficiency at high $P_{\text{in,rec}}$ is enhanced from state-of-the-art CCDD architectures. Besides that, the sensitivity to achieve 1V for $R_{\text{L}} = 100$ kΩ in SCC-CCDD

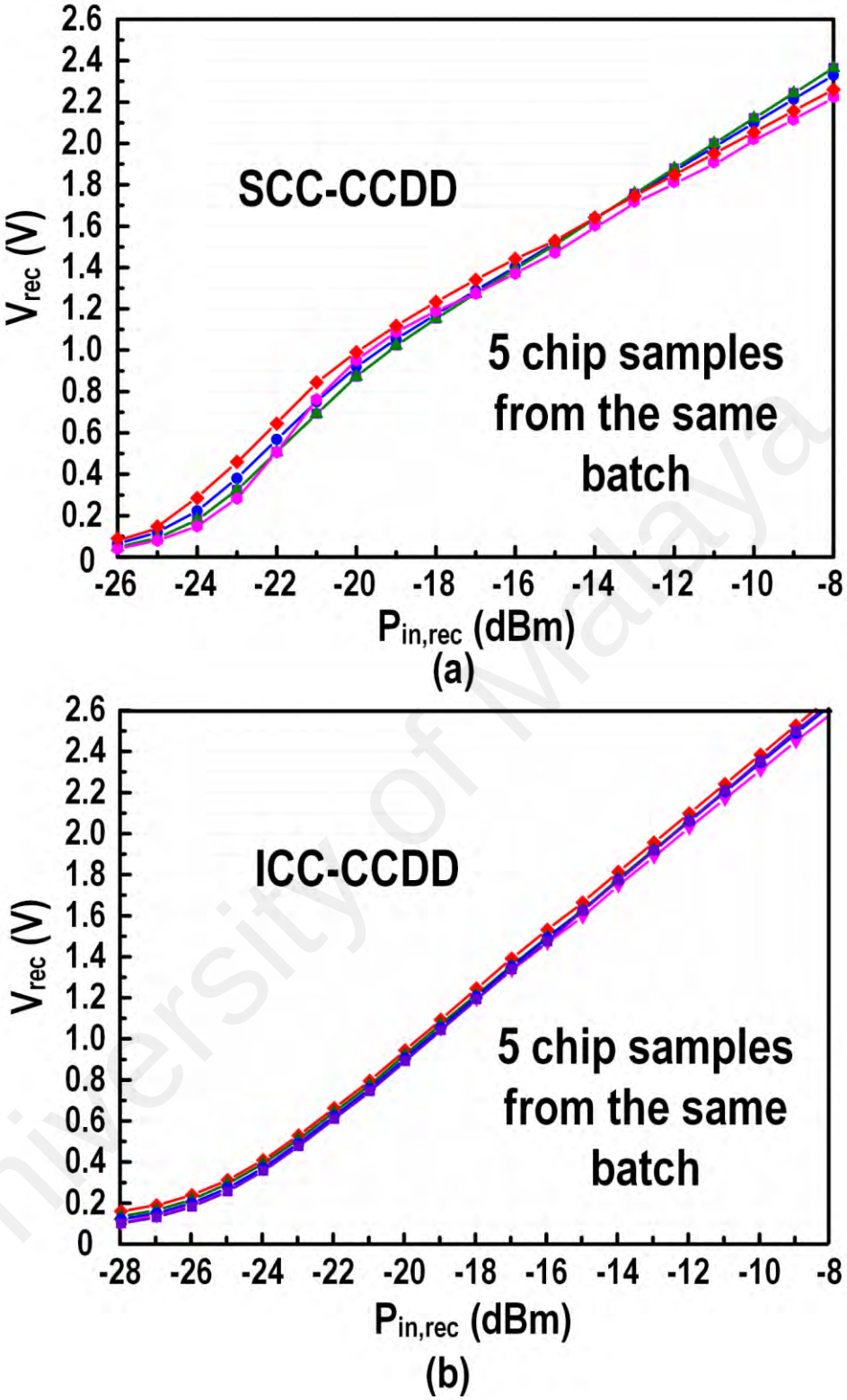

Figure 4.10: **Measured Output Voltage, V_{rec} at 900 MHz for $R_{\mathrm{L}} = 100$ kΩ**

and ICC-CCDD configurations are the highest as compared to other works. For a clear visualization, V_{Rec} for a PCE of 100%, 80%, 60%, 40%, 20% and 10% with $R_{\mathrm{L}} = 100$ kΩ are annotated in Figure 4.11 to show the theoretical limit of V_{Rec}.

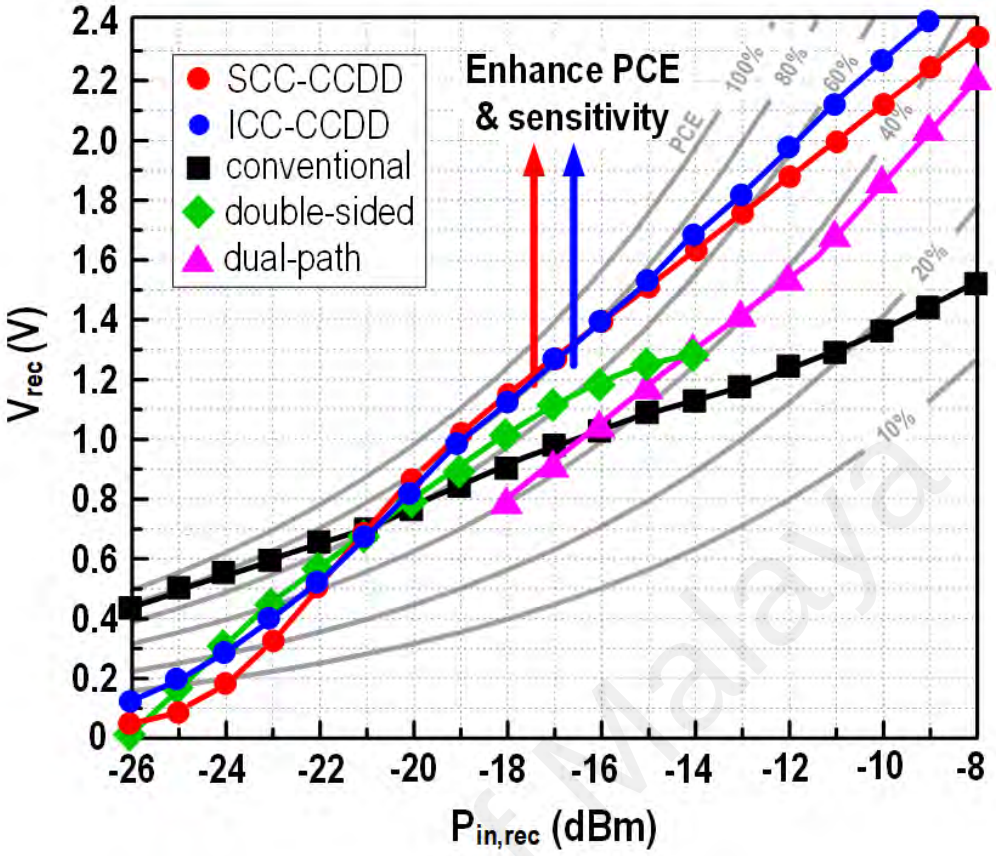

Figure 4.11: **Comparison of V_{rec} at 900 MHz for $R_L = 100$ kΩ**

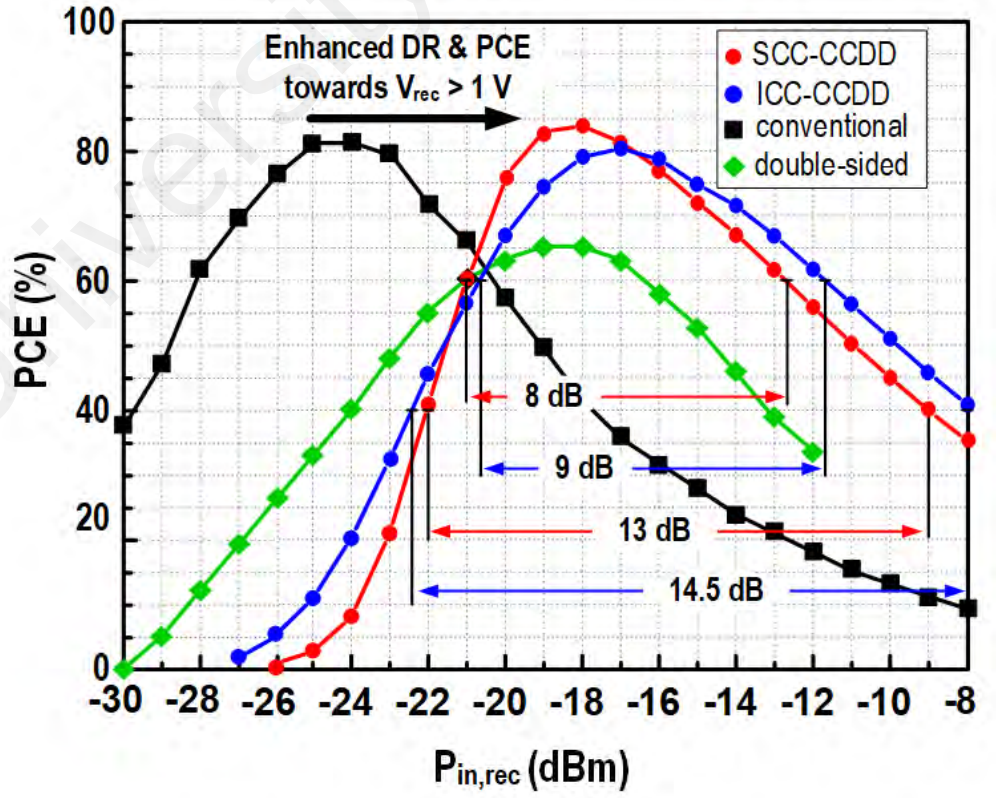

Figure 4.12: **Comparison of PCE at 900 MHz for R_L=100 kΩ**

Alternatively, Figure 4.12 shows the PCE plot of the rectifiers in which the DR could be obtained. The proposed rectifiers achieved a comparable peak PCE performance when compared to the conventional CCDD architecture for the same R_{L}. Also, the SCC-CCDD achieves a wide input PCE range of 13 dB for $P_{\mathrm{in,rec}}$ of -22 to -9 dBm (PCE $>$ 40%). Besides that, the ICC-CCDD achieves a wider DR range of 14.5 dB from -22.5 to -8 dBm with a slight reduction in the peak PCE compared to the SCC-CCDD. In addition, the proposed rectifiers are able to shift the PCE curve towards the range where V_{Rec} approaches 1V to achieve peak PCE within a sufficient headroom to be supplied to R_{L}. Table 4.3 summarizes the performances of the proposed CCDD architecture and provides a comparison with state-of-the-art CCDD architecture.

4.4 Discussion

The experiment results show that the proposed CCDD architectures are able to efficiently convert the input AC power from an ambient RF source into usable DC power across a wide $P_{\mathrm{in,rec}}$. Besides that, the rectified power of the SCC-CCDD and ICC-CCDD for a V_{Rec} between 0.5 V to 2.25 V corresponds to a usable power of 2.5 μW to 50.63 μW and 2.03 μW to 63.5 μW, respectively. This rectified power range is adequate to supply a DC-DC converter in an RFEH system for charging a storage capacitor or powering up a WSN transceiver.

Though the conventional CCDD might have a comparable PCE, the sensitivity and the DR range performances were lacking. The sensitivity was enhanced from -13 dBm of the conventional CCDD rectifier to <-18.7 dBm in the proposed CCDD architecture for $R_{\mathrm{L}} = 100$ kΩ. In addition, the DR range for the proposed CCDD architectures has been shifted towards a higher $P_{\mathrm{in,rec}}$ range where V_{Rec} is ~1 V. Having high PCE where V_{Rec} is ~1 V is much significant as the efficiency in this range contributes to higher overall system efficiency at a usable $P_{\mathrm{in,rec}}$ range. Having a high PCE for V_{Rec}<0.7V can be redundant

Table 4.3: Comparison with State-of-Art CCDD Architectures

Author		Proposed†		Almansouri et al. (2018)†	Moghaddam et al. (2017)	Ouda et al. (2016)†	Lu et al. (2017)†	Kotani et al. (2009)†
Technology (nm)		**130**		180	130	180	65	180
Frequency (MHz)		**900**		900	953	1,000	900	953
CCDD Architecture		**SCC**	**ICC**	double-sided	Low-feeding DC (LFDC)	self-bias	dual-path	conventional
No. of stages		**3**		1	3	1	5	3
Dynamic Range (dB)	**>PCE 60%**	**8** (*-21 to -13 dBm*)	**9** (*-20.6 to -11.6 dBm*)	4.2 (*-21 to -16.8 dBm*)	5 (*3.5 to 8.5 dBm*)	6 (*-23 to -17 dBm*)	n.a.	8 (*-28.5 to -20.5 dBm*)
	>PCE 40%	**13** (*-22 to -9 dBm*)	**14.5** (*-22.5 to -8 dBm*)	10.5 (*-24 to -13.5 dBm*)	8 (*2 to 10 dBm*)	11 (*-24 to -13 dBm*)	n.a.	12 (*-29.8 to -17.8 dBm*)
Peak PCE		**83.7%** @ -18.4 dBm	**80.3%** @ -17 dBm	66 % @ -18.5 dBm	69.5 % @ 5.26 dBm, R_L = 2 kΩ	65 % @ -21 dBm	45.5 % @ -15 dBm	82.6% @ -24.6 dBm
Peak Sensitivity @ 1V (dBm)		**-19.2**	**-18.7**	-18.2	-6.5 R_L = 50 kΩ	-18	-16.5	-13

†Results with R_L =100 kΩ

as it is challenging for DC-DC converters to boost V_{Rec} up to a usable output DC voltage to supply a load.

Alternatively, the double-sided CCDD architecture by Almansouri et al. (2018) in Table 4.3 is observed to achieve a comparable performance in terms of sensitivity compared to the proposed CCDD architecture. However, the PCE and DR of double-sided CCDD architecture are compromised due to the reduction in forward current. The PCE results in Figure 4.12 shows that the proposed CCDD architecture has an improved PCE compared to the double-sided CCDD architecture by Almansouri et al. (2018).

When comparing between the SCC-CCDD and ICC-CCDD configurations, it is observed that the ICC-CCDD achieves slightly higher (3.4%) peak PCE while the ICC-CCDD achieves a wider extended DR. As the rectifier is non-linear predominantly at low $P_{\mathrm{in,rec}}$, the $Z_{\mathrm{in,rec}}$ is dominated by the parasitic capacitance. Hence, $Z_{\mathrm{in,rec}}$ would increase due to the parasitic capacitance and causes the peak value of $V_{\mathrm{RF}\pm}$ to simultaneously increase. The higher peak value of $V_{\mathrm{RF}\pm}$ is able to increase the gate voltage of the rectifier which increases the forward current conduction. As a result, the PCE is enhanced at low $P_{\mathrm{in,rec}}$ as shown in Figure 4.12. Besides that, the 1 dB extended DR observed in the ICC-CCDD is due to the lower $Z_{\mathrm{in,rec}}$ value which improves the input $V_{\mathrm{RF}\pm}$ swing at low $P_{\mathrm{in,rec}}$. The peak PCE of the ICC-CCDD does not degrade significantly as the value is still above 80% which is higher than the other CCDD architectures listed in Table 4.3. Overall, the proposed CCDD architecture in this work has achieved significant improvement in its PCE and sensitivity performance where the focus on improving the DR has contributed to the performance improvement of the CCDD rectifier. Figure 4.13 shows the trend line for peak PCE performance across time in the development of rectifiers for ambient RF energy harvesting application.

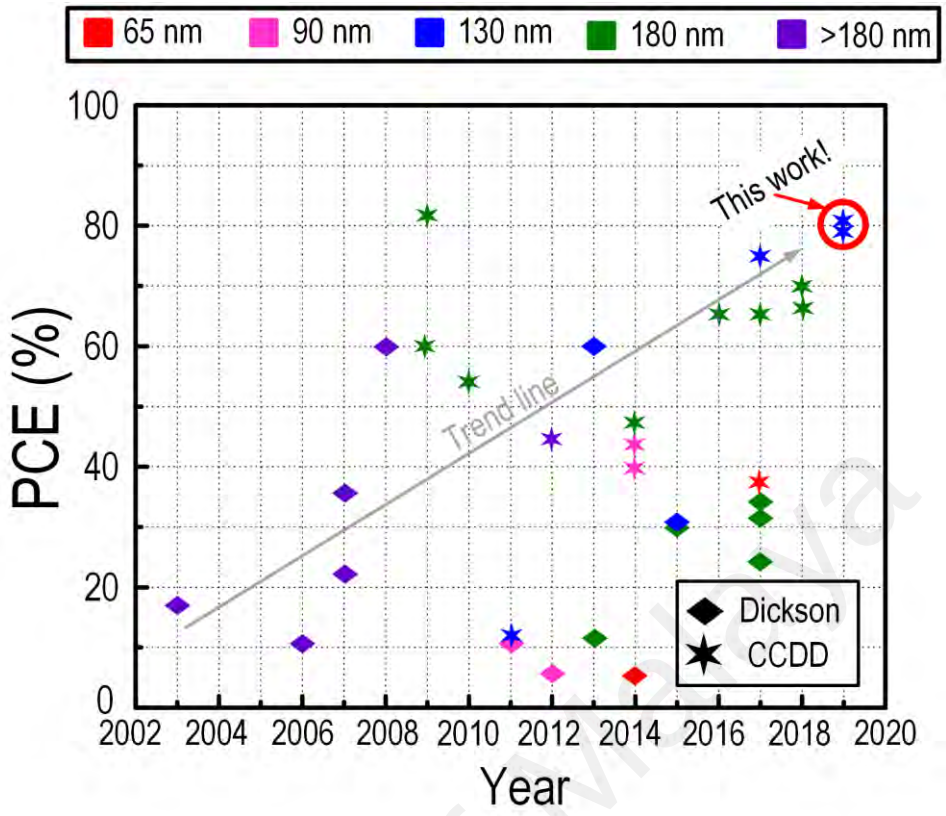

Figure 4.13: Technology roadmap of rectifier designs for ambient RFEH application

4.5 Summary

This chapter has proposed a new CCDD architecture with enhanced performance. The new self-bulk-biasing and gate-biasing schemes have been implemented to elevate the PCE and sensitivity performances of the rectifier to achieve an enhanced DR performance. An analysis of the proposed CCDD architecture was made to identify the contributing factors in which enhances the performances of the rectifier. Two input coupling capacitor configurations of the proposed CCDD rectifier were explored where the experimental results achieve substantially improvement in PCE, DR and sensitivity compared to the conventional and state-of-art CCDD architectures. The findings in this chapter has been published in a separate volume of the IEEE Transactions on Circuits and Systems-II: Express Briefs.

CHAPTER 5: CONCLUSION

In this research on integrated rectifier design in CMOS technology for ambient RFEH, two major contributions corresponding to the objectives has been achieved. The first major contribution of this thesis is a novel CCDD rectifier model in subthreshold operation for ambient RFEH presented in Chapter 3. The model was derived through the charge conservation principle using the CMOS subthreshold equation and the Bessel Function. The model achieved an accuracy above 90% up to a $P_{\mathrm{in,rec}}$ of 0 dBm and an accuracy above 80% for $P_{\mathrm{in,rec}}$ up until 3 dBm with a peak error of 9%. The model provides a quick and accurate method to design a conventional CCDD rectifier for ambient RFEH systems. Furthermore, the model addressed the gap by where no prior CCDD rectifier model for ambient RFEH were available.

Although the conventional CCDD rectifier is able to operate in subthreshold region to harvest ambient RF energy as presented in chapter 3, the $P_{\mathrm{in,rec}}$ range at which the rectifier achieve high PCE is limited due to the reverse-leakage current at high $P_{\mathrm{in,rec}}$ and the turn-on voltage at low $P_{\mathrm{in,rec}}$ respectively which limits the rectifier's dynamic range (DR). Hence, a second major contribution of this thesis is a proposed CCDD architecture with enhanced DR performance is presented in Chapter 4. The proposed CCDD architecture achieved a wide DR of 14.5 dB for PCE above 40% with a peak PCE of 83.7% and a sensitivity of -19.2 dBm at 1V. The outcome of the proposed CCDD architecture achieved substantial performance improvement in terms of the DR compared to the conventional CCDD rectifier by Kotani et al. (2009) while achieving better sensitivity than the state-of-art double-sided CCDD architecture by Almansouri et al. (2018).

The findings of this thesis also resulted in the contribution towards low-cost CMOS technology implementation and system-on-chip (SoC) solution of the developed rectifiers. The use of CMOS technology in the design of the rectifiers allows for low-cost solution, small physical form factor of the IC chip and the ability for SoC implementation of the RFEH system in a Wireless Sensor Node (WSN). Through the findings of this thesis, RFEH systems will be able to be realized in self-powered WSN for the Internet of Things (IoT) application which alleviates the need of using batteries in near future.

The first recommendation for future research is to adopt a system perspective to incorporate the rectifier into a full RFEH system to include the IMN and PMU in the scope of the research work. A fully integrated ambient RFEH system will allow for real environment prototype testing of the system to validate the performance of the RFEH system for practical implementation in a WSN.

Next future recommendation relates to the scope of mathematical modeling the CCDD rectifier. Other circuit blocks in an RFEH system could alter the natural condition of the rectifier. For example, it has been shown that voltage boosting network through co-antenna design strategy (Li et al., 2013) or impedance matching network (IMN) boosting scheme (Soltani & Yuan, 2010) could significantly boost the input voltage, $V_{\mathrm{RF}\pm}$ at low $P_{\mathrm{in,rec}}$ to improve the sensitivity of the RFEH system. Therefore, the next future recommendation work is to develop a complete RFEH model which considers the other circuit blocks in an RFEH system such as the IMN network. This recommendation relates closely to the first recommendation to develop a fully integrated RFEH system. A complete model for an ambient RFEH system allows for new insight and design methodology to be established in effective design of a complete RFEH system. Further reduction of the peak error in the CCDD model by incorporating the second-order effects into the model without adding complexity can

be research. Also, the potential of a software tool for designing ambient RFEH systems can be developed as this research area matures.

A final suggestion for further research work is to conduct a comparison study of the proposed CCDD rectifier model and CCDD architecture with other IC technology process. The literature review in chapter 2 suggests that complementary integrated technologies with CMOS is becoming widespread as the availability and cost of these processes would become competitive with CMOS in the near future (Theilmann et al., 2012). Though CMOS technology is highly desirable due to its low-cost, small physical form factor and SoC integration, integrated circuit (IC) design techniques applied to other technologies such as sub-micron CMOS technologies in 28/40/65-nm, special infused integrated process with CMOS technology such as the Schottky diode (Karthaus & Fischer, 2003), Silicon-on-Sapphire (Theilmann et al., 2012) or System-in-Package (Yi et al., 2017) can be explored. The comparison study would be able to produce a cost-to-performance analysis of contending IC technologies available in the market to identify which technology would be well suited for the development of ambient RFEH systems. This will provide economic insight and perspective to the development of ambient RFEH system for commercialization where the cost factors are included in the consideration.

REFERENCES

Abouzied, M. A., Ravichandran, K., and Sánchez-Sinencio, E. (2017). A Fully Integrated Reconfigurable Self-Startup RF Energy-Harvesting System With Storage Capability. *IEEE Journal of Solid-State Circuits*, 52(3), 704-719.

Alioto, M. (2017). *Enabling the Internet of Things from Integrated Circuits to Integrated Systems.* Cham: Springer.

Almansouri, A. S. M., Ouda, H., and Salama, K. N. (2018). A CMOS RF-to-DC Power Converter With 86% Efficiency and -19.2-dBm Sensitivity. *IEEE Transactions on Microwave Theory and Techniques*, 66(6), 2409 - 2415.

Andrenko, A. S., Lin, X., and Zeng, M. (2015). Outdoor RF spectral survey: A roadmap for ambient RF energy harvesting. *TENCON 2015 - 2015 IEEE Region 10 Conference*, Macao, 1-4.

Ashry, A., Sharaf, K., and Ibrahim, M. (2008). A Simple and Accurate Model for RFID Rectifier. *IEEE Systems Journal*, 2(4), 520-524.

Barroca, N., Saraiva, H. M., Gouveia, P. T., Tavares, J., Borges, L. M., Velez, F. J., Loss, C., Salvado, R., Pinho, P., Goncalves, R., Carvalho, N. B., Chavez-Santiago, R., and Balasingham, I. (2013). Antennas and circuits for ambient RF energy harvesting in wireless body area networks. *2013 IEEE 24th Annual International Symposium on Personal, Indoor, and Mobile Radio Communications (PIMRC)*, London, 532-537.

Barnett, R. E., Lui, J., and Lazar, S. (2009). A RF to DC Voltage Conversion Model for Multi-Stage Rectifiers in UHF RFID Transponders. *IEEE Journal of Solid-State Circuits*, 44(2), 354-370.

Bergeret, E., Gaubert, J., Pannier, P., and Gaultier, J. M. (2007). Modeling and Design of CMOS UHF Voltage Multiplier for RFID in an EEPROM Compatible Process. *IEEE Transactions on Circuits and Systems II: Express Briefs,* 54(10), 833-837.

Bronshtein, I. N., Semendyayev, K. A., Musilo, G., and Muehlig, H. (2004). *Handbook of Mathematics.* 4th edition. Berlin, Germany: Springer-Verlag.

Chouhan, S. S., and Halonen, K. (2015). Threshold voltage compensation scheme for RF-to-DC converter used in RFID applications. *Electronics Letters*, 51(12), 892-894.

Curty, J. P., Joehl, N., Krummenacher, F., Dehollain, C., and Declercq, M. J. (2005). A model for μ-power rectifier analysis and design. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 52(12), 2771-2779.

Daly, D. C., Fujino, L. C., and Smith, K. C. (2018). Through the Looking Glass - The 2018 Edition: Trends in Solid-State Circuits from the 65th ISSCC. *IEEE Solid-State Circuits Magazine*, 10(1), 30-46.

De Vita, G., and Iannaccone, G. (2005). Design criteria for the RF section of UHF and microwave passive RFID transponders. *IEEE Transactions on Microwave Theory and Techniques*, 53(9), 2978-2990.

Dickson, J. F. (1976). On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique. *IEEE Journal of Solid-State Circuits*, 11(3), 374-378.

Friis, H. T. (1946). A Note on a Simple Transmission Formula. *Proceedings of the IRE*, 34(5), 254-256.

Gharehbaghi, K., Zorlu, Ö., Koçer, F., and Külah, H. (2017). Threshold Compensated UHF Rectifier With Local Self-Calibrator, *IEEE Microwave and Wireless Components Letters*, 27(6), 575-577.

Giannakas, G., Plessas, F., and Stamoulis, G. (2012). Pseudo-FG technique for efficient energy harvesting. *Electronics Letters*, 48(9), 522-523.

Hameed, Z., and Moez, K. (2015). A 3.2 V –15 dBm Adaptive Threshold-Voltage Compensated RF Energy Harvester in 130 nm CMOS. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 62(4), 948-956.

Hameed, Z., and Moez, K. (2014). Hybrid Forward and Backward Threshold-Compensated RF-DC Power Converter for RF Energy Harvesting. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 4(3), 335-343.

IEEE. (2003). *IEEE Standard Letter Designations for Radar-Frequency Bands*. 221-2002 at:https://www.ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=1160089&isnumber=26011 [Accessed 2nd May 2018].

Kang, S.Y., and Leblebici, Y. (2005) *CMOS Digital Integrated Circuits Analysis and Design*. 3th Edition. New York: McGraw-Hill.

Kang, J., Rao, S. Chiang P. and Natarajan, A. (2016). Design and Optimization of Area-Constrained Wirelessly Powered CMOS UWB SoC for Localization Applications. *IEEE Transactions on Microwave Theory and Techniques*, 64(4), 1042-1054.

Karthaus, U., and Fischer, M. (2003). Fully integrated passive UHF RFID transponder IC with 16.7-μW minimum RF input power. *IEEE Journal of Solid-State Circuits*, 38(10), 1602-1608.

Kim, S., Vyas, R., Bito, J., Niotaki, K., Collado, A., Georgiadis, A., and Tentzeris, M. M. (2014). Ambient RF Energy-Harvesting Technologies for Self-Sustainable Standalone Wireless Sensor Platforms. *Proceedings of the IEEE*, 102 (11), 1649-1666.

Kim, Y., Bhamra, H. S., Joseph, J., and Irazoqui, P. P. (2015). An Ultra-Low-Power RF Energy-Harvesting Transceiver for Multiple-Node Sensor Application, *IEEE Transactions on Circuits and Systems II: Express Briefs*, 62(11), 1028-1032.

Kotani, K., Sasaki, A., and Ito, T. (2009). High-Efficiency Differential-Drive CMOS Rectifier for UHF RFIDs. *IEEE Journal of Solid-State Circuits*, 44(11), 3011-3018.

Le, T., Mayaram, K., and Fiez, T. (2008). Efficient Far-Field Radio Frequency Energy Harvesting for Passively Powered Sensor Networks. *IEEE Journal of Solid-State Circuits*, 43(5), 1287-1302.

Li, B., Shao, X., Shahshahan, N., Goldsman, N., Salter, T., and Metze, G. M. (2013). An Antenna Co-Design Dual Band RF Energy Harvester. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 60(12), 3256-3266.

Li, C., Yu, M., and Lin, H. (2017). A Compact 0.9-/2.6-GHz Dual-Band RF Energy Harvester Using SiP Technique. *IEEE Microwave and Wireless Components Letters*, 27(7), 666-668.

Lu, Y., Dai, H., Huang, M., Law, M. K., Sin, S. W., U., S. P., and Martins, R. P. (2017). A Wide Input Range Dual-Path CMOS Rectifier for RF Energy Harvesting. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 64(2), 166-170.

Luo, Y. S., and Liu, S. I. (2017). A Voltage Multiplier With Adaptive Threshold Voltage Compensation. *IEEE Journal of Solid-State Circuits*, 52(8), 2208-2214.

Mandal, S., and Sarpeshkar, R. (2007). Low-Power CMOS Rectifier Design for RFID Applications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 54(6), 1177-1188.

Mansano, A., Bagga, S., and Serdijn, W. (2013). A High Efficiency Orthogonally Switching Passive Charge Pump Rectifier for Energy Harvesters. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 60(7), 1959-1966.

Mansano, A. Li, L. Y., Bagga, S., and Serdijn, W. A. (2016). An Autonomous Wireless Sensor Node With Asynchronous ECG Monitoring in 0.18µm CMOS, *IEEE Transactions on Biomedical Circuits and Systems*, 10(3), 602-611.

Mohamed, M.M., Fahmy, G.A., Abdel-Rahman, A.B., Allam, A., Barakat, A., Abo-Zahhad, M., Jia, H., and Pokharel, R.K., (2018). High-Efficiency CMOS RF-to-DC Rectifier Based on Dynamic Threshold Reduction Technique for Wireless Charging Applications. *IEEE Access*, 6, 46826-46832.

Morgan Stanley Research, (2016). *Mighty Micro-Engines of the Internet of Things*. Morgan Stanley. Available at: https://www.morganstanley.com/ideas/microcontrollers-semiconductors-internet-of-things [Accessed 5th December 2017].

Mimis, K., Gibbins, D., Dumanli, S., and Watkins, G. T. (2015). Ambient RF energy harvesting trial in domestic settings. *IET Microwaves, Antennas & Propagation*, 9(5), 454-462.

Moghaddam, A. K., Chuah, J. H., Ramiah, H., Ahmadian, J., Mak, P. I., and Martins, R. P. (2017). A 73.9%-Efficiency CMOS Rectifier Using a Lower DC Feeding (LDCF) Self-Body-Biasing Technique for Far-Field RF Energy-Harvesting Systems. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 64(4), 992-1002.

Nakamoto, H., Yamazaki, D., Yamamoto, T., Kurata, H., Yamada, S., Mukaida, K., Ninomiya, T., Ohkawa,, T., Masui, S., and Gotoh, K. (2007). A Passive UHF RF Identification CMOS Tag IC Using Ferroelectric RAM in 0.35-µm Technology. *IEEE Journal of Solid-State Circuits,* 42(1), 101-110.

Nariman, M., Shirinfar, F., Pamarti, S., Rofougaran, A., and De Flaviis, F. (2017). High-Efficiency Millimeter-Wave Energy-Harvesting Systems With Milliwatt-Level Output Power. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 64(6), 605-609.

Nguyen, T. T., Feng, T., Häfliger, P., and Chakrabartty, S. (2014). Hybrid CMOS Rectifier Based on Synergistic RF-Piezoelectric Energy Scavenging. *IEEE Transactions on Circuits and Systems I: Regular Papers,* 61(12), 3330-3338.

Ouda, M. H., Arsalan, M., Marnat, L. Shamim, A. and Salama, K. N. (2013). 5.2-GHz RF power harvester in 0.18-µm CMOS for implantable intraocular pressure monitoring. *IEEE Transactions on Microwave Theory and Techniques,* 61(5), 2177–2184.

Ouda, M. H., Khalil, W., and Salama, K. N. (2016). Wide-Range Adaptive RF-to-DC Power Converter for UHF RFIDs. *IEEE Microwave and Wireless Components Letters*, 26(8), 634-636.

Ouda, M. H., Khalil, W., and Salama, K. N. (2017). Self-Biased Differential Rectifier With Enhanced Dynamic Range for Wireless Powering. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 64(5), 515-519.

Papotto, G., Carrara, F., and Palmisano, G. (2011). A 90-nm CMOS Threshold-Compensated RF Energy Harvester. *IEEE Journal of Solid-State Circuits*, 46(9), 1985-1997.

Papotto, G., Greco, N., Finocchiaro, A., Guerra, R., Leotta, S., and Palmisano, G. (2018). An RF-Powered Transceiver Exploiting Sample and Hold Operation on the Received Carrier, *IEEE Transactions on Microwave Theory and Techniques*, 66(1), 396-409.

Piñuela, M., Mitcheson , P. D., and Lucyszyn, S. (2013). Ambient RF Energy Harvesting in Urban and Semi-Urban Environments. *IEEE Transactions on Microwave Theory and Techniques*, 61(7), 2715-2726.

Razavi, B. (2017). *Design of Analog CMOS Integrated Circuits.* 2nd Edition. New York: McGraw Hill Education.

Razavi Haeri, A. A., Karkani, M. G., Sharifkhani, M., Kamarei, M., and Fotowat-Ahmad, A. (2017). Analysis and Design of Power Harvesting Circuits for Ultra-Low

Power Applications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 64(2), 471-479.

Reinisch, H., Wiessflecker, M., Gruber, S., Klamminger, M., Pribyl, W., and Holweg, G. (2011). A Multifrequency Passive Sensing Tag With On-Chip Temperature Sensor and Off-Chip Sensor Interface Using EPC HF and UHF RFID Technology. *IEEE Journal of Solid-State Circuits*, 46(12), 3075-3088.

Roover, C. D., and Steyaert, M. S. J. (2010) Energy Supply and ULP Detection Circuits for an RFID Localization System in 130 nm CMOS. *IEEE Journal of Solid-State Circuits*, 45(7), 1273-1285.

Scorcioni, S., Larcher, L., and Bertacchini, A. (2013). A Reconfigurable Differential CMOS RF Energy Scavenger With 60% Peak Efficiency and -21 dBm Sensitivity, *IEEE Microwave and Wireless Components Letters*, 23(3), 155-157.

Soltani N., and Yuan, F. (2010). A High-Gain Power-Matching Technique for Efficient Radio-Frequency Power Harvest of Passive Wireless Microsystems. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 57(10), 2685-2695.

Soyata, T., Copeland, L., and Heinzelman, W. (2016). RF Energy Harvesting for Embedded Systems: A Survey of Tradeoffs and Methodology. *IEEE Circuits and Systems Magazine*, 16(1), 22-57.

Stoopman, M., Keyrouz, S., Visser, H. J., Philips, K., and W. A. Serdijn (2014). Co-Design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters, *IEEE Journal of Solid-State Circuits*, 49(3), 622-634.

Takhedmit, H. (2016). Ambient RF power harvesting: Application to remote supply of a batteryless temperature sensor. *2016 IEEE International Smart Cities Conference (ISC2)*, Trento, 1-4.

Theilmann, P. T., Presti, C. D., Kelly, D. J., and Asbeck, P. M. (2012). A μW Complementary Bridge Rectifier With Near Zero Turn-on Voltage in SOS CMOS for Wireless Power Supplies. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 59(9), 2111-2124.

Umeda, T., Yoshida, H., Sekine, S., Fujita, Y., Suzuki, T., and Otaka, S. (2006). A 950-MHz rectifier circuit for sensor network tags with 10-m distance. *IEEE Journal of Solid-State Circuits*, 41(1), 35-41.

Visser, H. J., and Vullers, R. J. M. (2013). RF Energy Harvesting and Transport for Wireless Sensor Network Applications: Principles and Requirements. *Proceedings of the IEEE*, 101(6), 1410-1423.

Vyas, R. J., Cook, B. B., Kawahara, Y., and Tentzeris, M. M. (2013). E-WEHP: A Batteryless Embedded Sensor-Platform Wirelessly Powered From Ambient Digital-TV Signals. *IEEE Transactions on Microwave Theory and Techniques*, 61(6), 2491-2505.

Wei, P., Che, W., Bi, Z., Wei, C., Na, Y., Qiang, L., and Hao, M. (2011). High-Efficiency Differential RF Front-End for a Gen2 RFID Tag. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 58(4), 189-194.

Xia, L., Cheng, J., Glover, N. E., and Chiang, P. (2014). 0.56 V, –20 dBm RF-Powered, Multi-Node Wireless Body Area Network System-on-a-Chip With Harvesting-Efficiency Tracking Loop, *IEEE Journal of Solid-State Circuits*, 49(6), 1345-1355.

Xu, P., Flandre, D., and Bol, D. (2019). Analysis, Modeling, and Design of a 2.45-GHz RF Energy Harvester for SWIPT IoT Smart Sensors. *IEEE Journal of Solid-State Circuits*, 55(10), 2717-2729.

Yi, J., Ki, W. H., and Tsui, C. Y. (2007). Analysis and Design Strategy of UHF Micro-Power CMOS Rectifiers for Micro-Sensor and RFID Applications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 54(1), 153-166.

Yoo, J., Yan, L., Lee, S., Kim, Y., and Yoo, H. J. (2010). A 5.2 mW Self-Configured Wearable Body Sensor Network Controller and a 12μW Wirelessly Powered Sensor for a Continuous Health Monitoring System. *IEEE Journal of Solid-State Circuits*, 45(1), 178-188.

Zanjireh, M. M., and Larijani, H. (2015). A Survey on Centralised and Distributed Clustering Routing Algorithms for WSNs. *2015 IEEE 81st Vehicular Technology Conference (VTC Spring)*, Glasgow, 1-6.

Zgaren, M. and Sawan, M. (2015). A Low-Power Dual-Injection-Locked RF Receiver With FSK-to-OOK Conversion for Biomedical Implants. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 62(11), 2748-2758.

LIST OF PUBLICATIONS AND PAPERS PRESENTED

Chong, G., Ramiah, H., Yin, J., Rajendran, J., Wong, W.R., Mak, P.-I., and Martins, R. P. (2018). Ambient RF Energy Harvesting System: A Review on Integrated Circuit Design. *Analog Integrated Circuits and Signal Processing*, 97 (3), 515-531. [ISI, Q4]

Chong, G., Ramiah, H., Yin, J., Rajendran, J., Wong, W.R., Mak, P.-I., and Martins, R. P. (2019). CMOS Cross-Coupled Differential-Drive Rectifier in Subthreshold Operation for Ambient RF Energy Harvesting – Model and Analysis. *IEEE Transactions on Circuits and Systems II: Express Brief*, 66(12), 1942-1946. [ISI, Q2]

Chong, G., Ramiah, H., Yin, J., Rajendran, J., Mak, P.-I., and Martins, R. P., A Wide-PCE-Dynamic-Range CMOS Cross-Coupled Differential-Drive for Ambient RF Energy Harvesting. *IEEE Transactions on Circuits and Systems II: Express Brief.* [ISI, Q2]