OPTIMIZED TRANSCONDUCTANCE DESIGNS TO ENHANCE THE LINEARITY PERFORMANCE OF RF FRONT-END RECEIVER CIRCUITS IN 130 NM CMOS TECHNOLOGY

NANDINI A/P VITEE

FACULTY OF ENGINEERING
UNIVERSITY OF MALAYA
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OPTIMIZED TRANSCONDUCTANCE DESIGNS TO ENHANCE THE LINEARITY PERFORMANCE OF RF FRONT-END RECEIVER CIRCUITS IN 130 NM CMOS TECHNOLOGY

ABSTRACT

Highly linear front-end circuits are greatly desired for wireless receivers to improve the dynamic range. However, intermodulation distortions caused by the non-linear transconductor current limits the linearity of the front-end receiver circuit in CMOS technologies. In addition to the inherent nonlinear effect, the downscaling of CMOS further exacerbates the linearity of the circuit due to lower voltage headroom and high-field mobility. Thus, it is essential to develop effective circuit techniques that can aid linearity enhancement without jeopardizing other preferred performances such as low noise, high conversion gain, and low-power consumption. In this thesis, two different high linear transconductors are presented which are designed and fabricated in 130 nm CMOS technology. The first circuit is a low-voltage high linearity differential-folded mixer with multiple-feedback techniques for performance enhancement. The capacitor cross-coupled (CCC) common-gate transconductance stage is implemented to improve the noise figure (NF) at low power by boosting the effective transconductance while enhancing the linearity via suppressing the 2^{nd}-order harmonic distortion. However, the created loop gain of the CCC can raise the 3^{rd}-order intermodulation (IM3) distortion, penalizing the input referred 3^{rd}-order intercept point (IIP3) performance. Therefore, a positive and a 2^{nd} capacitive feedback are implemented into the CCC common-gate transconductor, not only to suppress the IM3 distortion current, but also to add design flexibility to the input transistors. Furthermore, the positive feedback also improves the input impedance matching, conversion gain and NF through a flexible design criterion. The proposed mixer operating at 900 MHz dissipates 4 mW at 1.0 V. The measured NF is 8.5 dB, the conversion gain is 18.4 dB and the IIP3 is +12.5 dBm. The second circuit

is a high conversion gain and high linearity inductively source degenerated balun-low noise amplifier (LNA)-mixer with integrated transformer-based gate inductor and 2nd-order intermodulation (IM2) injection technique. In this work, two linearization techniques are proposed to improve the IIP3 of the balun-LNA-mixer. The intrinsic IM3 product of the inductively source degenerated (ISD) transconductor from the 2nd-order derivative transconductance component (g_m'') is reduced by tailoring towards optimum biasing point at moderate-inversion region. While, the generated IM3 current by the 1st-order derivative transconductance (g_m') due to the interaction with the feedback component in the ISD transconductor is attenuated by 2nd harmonic injection via the bulk of the ISD transconductor. Further, a transformer-based gate inductor and a transformer-based balun are applied to improve the input impedance matching and produce a balanced differential input signal. Measured results show a high IIP3 of +16 dBm and a conversion gain of 22 dB at 2.4 GHz. The double sideband (DSB) NF_{DSB} is 7.2 dB and the power consumption is 3.15 mW at 1.2 V.

Keywords: CMOS, high linearity, IM3 cancellation, front-end receiver.

REKA BENTUK TRANSKONDUKTAN YANG DILAKSANAKAN UNTUK MENINGKATKAN PRESTASI KELELURUSAN LITAR PENERIMA RF BAHAGIAN HADAPAN DALAM 130 NM CMOS TEKNOLOGI

ABSTRAK

Litar bahagian-hadapan yang sangat lelurus amat dikehendaki untuk penerima wayarles untuk meningkatkan julat dinamik. Walau bagaimanapun, herotan saling modulatan yang disebabkan oleh arus transkonduktor yang tak lelurus mengehadkan kelelurusan litar penerima bahagian-hadapan dalam teknologi CMOS. Selain kesan tak lelurus terwujud, penyingkatan CMOS menambah buruk lelurus litar disebabkan oleh ruang atas voltan yang lebih rendah dan kebolehgerakan medan yang tinggi. Oleh itu, adalah penting untuk membangunkan teknik litar yang berkesan yang boleh membantu peningkatan lelurus tanpa menjejaskan prestasi keinginan lain seperti hingar yang rendah, peningkatan gandaan penukaran yang tinggi dan penggunaan kuasa rendah. Dalam tesis ini, dua transkonduktor lelurus tinggi yang berbeza telah dibentangkan dan mereka semua direkabentuk dan terbikin dalam 130 nm CMOS teknologi. Litar pertama ialah pencampur-penukar berlipat-pembeza yang bervoltan rendah kelelurusan tinggi dengan teknik berbilang-suap balik untuk peningkatan prestasi. Peringkat transkonduktansi get sepunya yang dipasang oleh kapasitor gandingan-silang (CCC) dilaksanakan untuk perbaiki angka hingar (NF) pada kuasa rendah dengan menggalakan transkonduktansi yang berkesan sambil meningkatkan kelelurusan dengan menindas herotan harmonik tertib ke-2. Walau bagaimanapun, gandaan gelung CCC yang dihasilkan dapat meningkatkan herotan saling modulatan ke-3 (IM3), menghukum prestasi pintasan titik masukan tertib ke-3 (IIP3). Oleh itu, suap balik positif dan kapasitif ke-2 dilaksanakan ke dalam transkonduktor get sepunya CCC, bukan sahaja untuk menindas arus herotan IM3, tetapi juga untuk menambahkan fleksibiliti rekabentuk kepada transistor masukan. Selain itu, suap balik positif juga meningkatkan padanan galangan masukan, gandaan penukaran

dan NF melalui kriteria rekabentuk yang fleksibel. Pencampur-penukar yang dicadangkan beroperasi pada 900 MHz dengan melesap 4 mW pada 1.0 V. NF diukur adalah 8.5 dB, gandaan penukaran adalah 18.4 dB dan IIP3 ialah +12.5 dBm. Litar kedua adalah balun-penguat hingar rendah (LNA)- pencampur-penukar yang berdasarkan sumber induktif merosot dengan bersapadu transformer sebagai get induktor dan teknik suntikan herotan saling modulatan ke-2 (IM2) dalam mencipta penukaran gandaan yang tinggi dan kelelurusan tinggi. Dalam kerja-kerja ini, dua teknik pelelurusan dicadangkan untuk meningkatkan IIP3 dari balun-LNA-pencampur-penukar. Produk IM3 intrinsik dari transkonduktor sumber induktif merosot (ISD) dari komponen transkonduktan derivatif ke-2 (g''_m) dikurangkan dengan melaras ke arah titik pincangan optimum di kawasan penyongsang sederhana. Sementara itu, arus IM3 yang dijana oleh transkonduktansi derivatif tertib pertama (g'_m) melalui interaksi dengan komponen suap balik dalam transkonduktor ISD dilemahkan oleh suntikan harmonik ke-2 pada pukal transkonduktor ISD. Selanjutnya, induktor get berasaskan transformer dan balun digunakan untuk meningkatkan padanan galangan masukan dan menghasilkan isyarat input perbezaan yang seimbang. Keputusan yang diukur menunjukkan IIP3 tinggi pada +16 dBm dan keuntungan penukaran 22 dB pada 2.4 GHz. Jalur sisi kembar (DSB) NF_{DSB} adalah 7.2 dB dan penggunaan kuasa adalah 3.15 mW pada 1.2 V.

Keywords: CMOS, kelelurusan tinggi, pembatalan IM3, penerima bahagian-hadapan.

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A	:	Amplitude
AC	:	Alternating current
a_n	:	Coefficient constant
ACP	:	Air coplanar
CAD	:	Computer aided design
CCC	:	Capacitor cross-coupled
C_{fb}	:	Feedback capacitance
CG	:	Common-gate
C_{gs}	:	Gate-source parasitic capacitance
C_L	:	Load capacitance
CMOS	:	Complementary metal-oxide semiconductor
C_p	:	Parasitic capacitance
CS	:	Common source
dB	:	Decibel
dBm	:	Decibel-milliwatts
DC	:	Direct current
DCCC	:	Dual capacitor cross-coupled
DCQ	:	Direct current quadrant
DRC	:	Design rule check
DSB	:	Double sideband
DUT	:	Device under test
EM	:	Electromagnetic
F	:	Noise factor
FET	:	Field-effect transistor

F_{IF}	:	IF amplifier's noise factor
F_{LNA}	:	LNA's noise factor
F_{MIX}	:	Mixer's noise factor
FOM	:	Figure-of-merit
F_{tot}	:	Total noise factor
G_c	:	Conversion gain
g_{dsn}	:	1st-order coefficient of drain-conductance of transistor n
GHz	:	Gigahertz
G_L	:	Loop gain
G_{LNA}	:	LNA's power gain
G_m	:	Effective transconductance
g_{mbn}		Bulk-transconductance of transistor n
g'_{mbn}	:	1st-order coefficient of the bulk-transconductance of transistor n
g''_{mbn}		2nd-order coefficient of the bulk-transconductance of transistor n
G_{MIX}	:	Mixer's power conversion gain
g_{mn}	:	Fundamental transconductance of transistor n
g'_{mn}	:	1st-order transconductance coefficient of transistor n
g''_{mn}	:	2nd-order transconductance coefficient of transistor n
I_{dsn}	:	Drain-source current of transistor n
IF	:	Intermediate frequency
IIP3	:	Input referred 3rd-order intercept point
$IIP3_{CL}$	:	Closed loop input referred 3rd-order intercept point
$IIP3_{IF}$	:	IF amplifier's input referred 3rd-order intercept point
$IIP3_{LNA}$	:	LNA's input referred 3rd-order intercept point
$IIP3_{MIX}$	:	Mixer's input referred 3rd-order intercept point

$IIP3_{OL}$	:	Open loop input referred 3rd-order intercept point
$IIP3_{tot}$	:	Total input referred 3rd-order intercept point
IM2	:	2nd-order intermodulation
IM3	:	3rd-order intermodulation
IMD	:	Intermodulation distortion
ISD	:	Inductively source degenerated
ISS	:	Impedance standard substrate
KCL	:	Kirchhoff's current law
k_n	:	Coupling coefficient of transformer n
LC	:	Inductor-capacitor
LMV	:	LNA-mixer-VCO
L_n	:	Length of transistor n
LNA	:	Low-noise amplifier
LO	:	Local oscillator
LVS	:	Layout versus schematic
MHz	:	Megahertz
NF	:	Noise figure
n_k	:	Turn ratio of transformer k
NMOS	:	n-channel metal-oxide semiconductor
OFDM	:	Orthogonal frequency division multiplexing
P1dB	:	1-dB compression point
P_{DC}	:	DC power dissipation
PMOS	:	p-channel metal-oxide semiconductor
PVT	:	Process, voltage and temperature
Q	:	Quality factor
RF	:	Radio frequency

R_L	:	Load resistance
R_s	:	Termination source resistance
R_{sw}	:	Switching stage resistance
S_{11}	:	Input reflection coefficient
VCO	:	Voltage control oscillator
V_{DD}	:	Supply voltage
v_{ds}	:	Drain-source voltage
v_{gs}	:	Gate-source voltage
v_{IF}	:	IF voltage signal
v_{LO}	:	LO voltage signal
VNA	:	Vector network analyser
v_{RF}	:	RF voltage signal
W_n	:	Width of transistor n
Y_{gsn}	:	Gate–source parasitic admittance of transistor n
Y_{dsn}	:	Drain–source parasitic admittance of transistor n
Z_{in}	:	Input impedance
α	:	Ratio between the device transconductance and the zero-bias drain conductance
γ	:	Coefficient of gate noise
ω_{IF}	:	IF angular frequency
ω_{LO}	:	LO angular frequency
ω_{RF}	:	RF angular frequency
ω_T	:	Ratio between fundamental transconductance and parasitic capacitance

LIST OF APPENDICES

CHAPTER 1: INTRODUCTION

1.1 Background and Motivations

In recent years, the momentum of wireless communication keeps increasing and the future generation breakthrough are under active research and development worldwide. However, the growth in wireless communication sector and the increase in the number of wireless connected devices cause the radio spectrum to be congested with interferers. Additionally, the modern wireless communication protocols, for example, IEEE 802.11 b/g/ah standard is in favour to incorporate orthogonal frequency division multiplexing (OFDM) modulation scheme due to its high spectral efficiency, high data rate and excellent immunity to multi-path fading. To meet these demands for current and future wireless communication system, as well to reduce large interferers from creating unwanted intermodulation distortion (IMD) and corrupting the carrier signal, the linearity becomes a critical requirement in a RF receiver.

In a receiver chain (referring Figure 1.1), the linearity of the cascaded system is defined by the last stage as its IIP3 is scaled down by the total gain of the previous stage (RF stage) according to the linearity cascade theory (Razavi, 2012). Nevertheless, higher linearity at the IF stage could be easily guaranteed by using high gain amplifiers with feedback loops (automatic gain control). For the RF stage, a similar technique is not applicable due to the limited bandwidth and stability issues. The most practical technique is in the use of high quality (Q) factor, preselection filters (duplexers in transceivers) after the antenna. In practice, however, it is very difficult to implement the filter with high Q factor (Tohidian, Madadi, & Staszewski, 2014). In the absence of high Q factor filter, the unwanted signals cross-modulates into wanted frequencies and reduces the gain of the desired signal due to the presence of a number of nonlinear transistors in the RF front-end subcircuits as illustrated in Figure 1.2. As a result, the effective signal to noise ratio

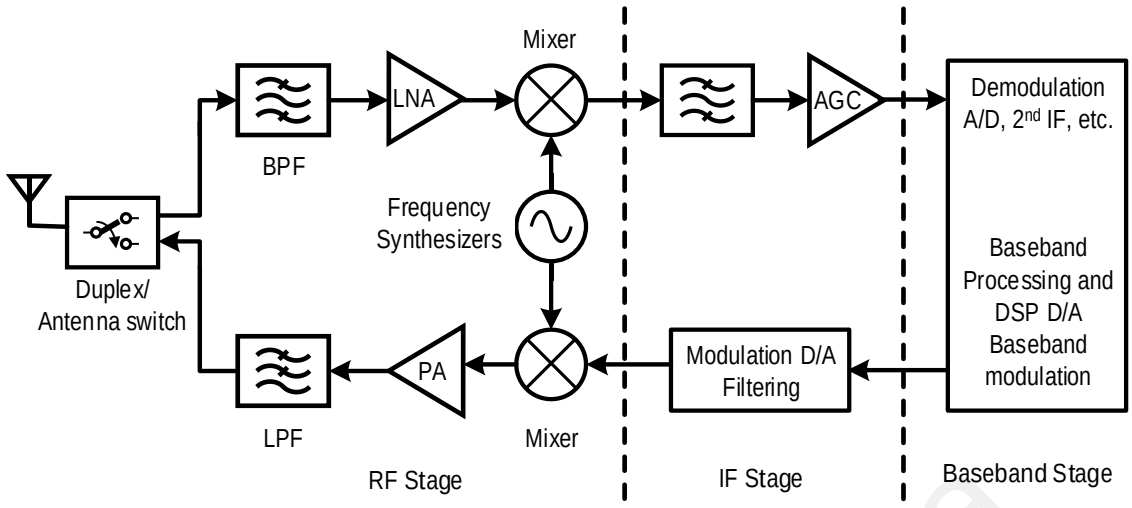


Figure 1.1: Simplified block diagram of the typical transceiver.

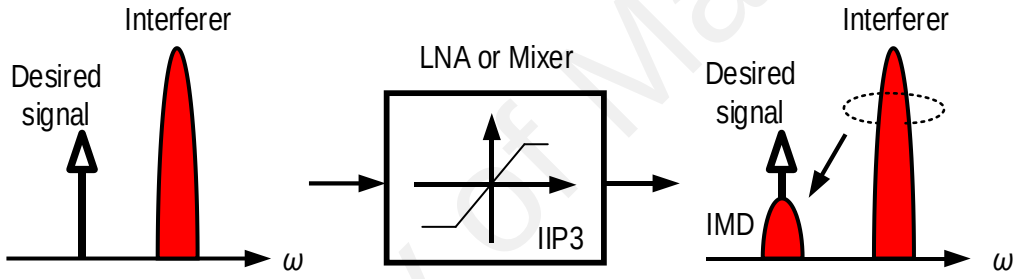


Figure 1.2: Corruption of a signal due to cross-modulation.

(SNR) of the received signals is reduced. As the last module of the RF front-end (RF stage), mixer plays a crucial role in defining the linearity of the entire RF receiver.

Mixer is generally classified into active and passive types. The active mixer is usually based upon the conventional Gilbert-cell architecture, whereas the passive mixer is based upon a FET (Field-effect transistor) or diode ring. Active mixer typically yields low conversion loss or even gains, provides a good degree of balance, but often at the penalty of a modest linearity. The transconductor (transconductance stage) of a mixer is the main block in defining the linearity of the architecture. Therefore, the investigation of linearization techniques for the transconductor in active mixer is a topic of continuous interest. Moreover, a high linear active mixer which preserves the simplicity of the design

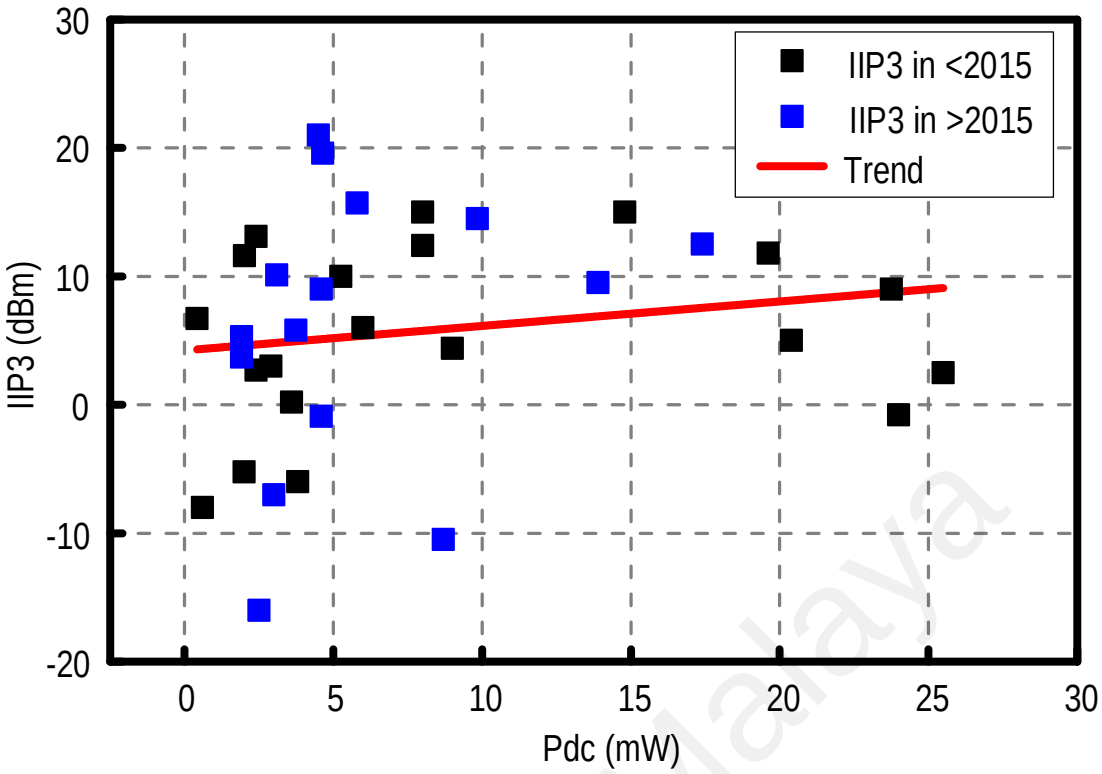


Figure 1.3: Comparison of mixers: IIP3 versus DC power consumption.

and other performance parameter such as conversion gain, noise figure and power consumption is desirable to satisfy the requirements of the current and next generation of wireless communication systems.

The trade-off between linearity and DC power consumption has to be considered for battery operating systems such as the handsets and the wearable health-monitoring devices. In order to establish the relationship between linearity and DC power consumption, consider the results of the IIP3 comparison of 35 different CMOS mixers circuits published recently (Table A.1 & A.2, in an Appendix A), also depicted in Figure 1.3. The rectangular shaped makers represent the IIP3 value corresponding to its DC power consumption from Table 1.0, whereas the solid line represents a linear trend based on the calculated dataset. As predicted, high linearity is achieved at the cost of increased power consumption (+0.19 dBm/mW) as the intermodulation distortion closely related to its power consumption. However, it may not necessarily yield the best noise figure and

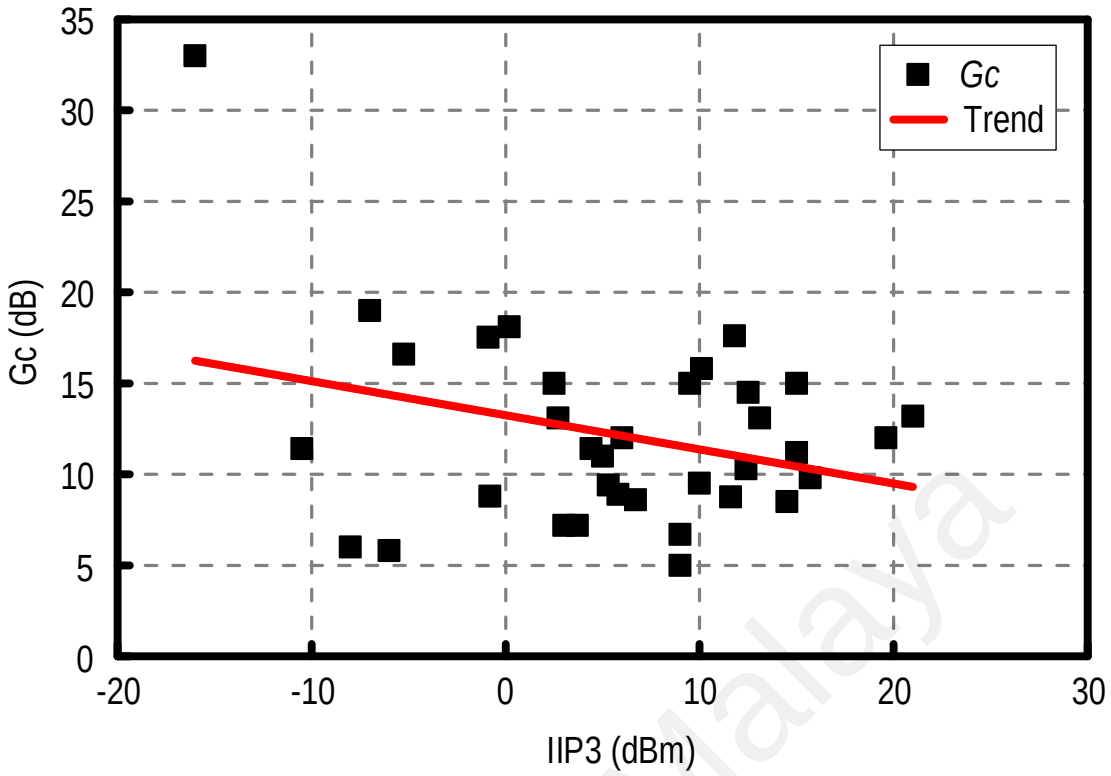


Figure 1.4: Comparison of mixers: G_c versus IIP3.

conversion gain performances. As depicted from Table 1.0, most of the high linearity performances were obtained at the penalty of low conversion gain. This characteristic is illustrated in Figure 1.4, where the IIP3 of the mixers are strongly dependent on the conversion gain as the slope of a trend line is approximately -0.19 dB/dBm with an average conversion gain of 12.2 dB. Hence, there is a need to enhance the linearity at the desired operating frequency, while maintaining the conversion gain and also other important parameters of the RF receiver circuits such as noise figure, stability and input matching with minimal current overhead by adopting some innovative linearization techniques.

In addition, for the merged low noise amplifier (LNA) and mixer, the selected input transconductor matching network must exhibit excellent input matching over the desired frequency while adding minimum noise into the input RF signal path to ensure good performance. This requirement becomes more stringent as the intermodulation distortion

Table 1.1: IEEE 802.11 common WLAN standards breakdown.

Standard	Frequency band	Bandwidth	Modulation Scheme	Channel Architecture	Maximum Data Rate	Range	Max Transmit Power
802.11	2.4 GHz	20 MHz	BPSK to 256-QAM	DSSS, FHSS	2 Mbps	20 m	100 mW
b	2.4 GHz	20 MHz	BPSK to 256-QAM	CCK, DSSS	11 Mbps	35 m	100 mW
a	5 GHz	22 MHz	BPSK to 256-QAM	OFDM	54 Mbps	35 m	100 mW
g	2.4 GHz	23 MHz	BPSK to 256-QAM	DSSS, OFDM	54 Mbps	70 m	100 mW
n	2.4 GHz, 5GHz	24 MHz and 40 MHz	BPSK to 256-QAM	OFDM	600 Mbps	70 m	100 mW
ac	5 GHz	20, 40, 80, 80+80=160 MHz	BPSK to 256-QAM	OFDM	6.93 Gbps	35 m	160 mW
ad	60 GHz	2.16 GHz	BPSK to 256-QAM	SC, OFDM	6.76 Gbps	10 m	10 mW
af	54-790 MHz	6, 7 and 8 MHz	BPSK to 256-QAM	SC, OFDM	26.7 Mbps	> 1km?	100 mW
ah	900 MHz	1, 2, 4, 8, and 16 MHz	BPSK to 256-QAM	SC, OFDM	40 Mbps	1 km	100 mW

(IMD) performance of an active RF circuit is closely related to its dc power consumption. Hence, the implementation of the LNA and mixer as a single solution, remains a challenging task and often requires innovative techniques to overcome this design challenge without jeopardizing other preferred performances.

On the other hand, the fast-evolving wireless communication industry has benefited from the advances of the CMOS technology, which is low cost, high integration and low power consumption. As the featured minimum size scales down, CMOS stands out with great advantage in providing portable and affordable multi-functional wireless devices. Nevertheless, when the supply voltage of a circuit is reduced, the power of the incident RF signals to the circuit has to be lowered to keep the IMD tones at sufficiently low levels, thus it limits the maximum possible input signal swing and gain. At the same time, mobility reduction due to the increase in vertical electrical fields and limited voltage headroom exacerbate the linearity of the circuit. While the imperative to reduce the dc

supply voltage of RF circuits in wireless communication system continues unabated, the linearity requirements of the system remains largely intact.

1.2 Wireless Standards and Applications

IEEE 802.11 Wireless Local Area Network (WLAN) has greater attention in wireless technologies due to its easy deployment and low-cost. This initial standard prescribes an operating frequency of 2.4 GHz operating with data rates of 1 or 2 Mbps. The increasing market of wireless communication network brought the need of developing a new standard in order to comply ubiquitous wireless access. Therefore, new features have been introduced to this standard as amendments, and these amendments describe various operating characteristics such as maximum data rate and frequency band of operation, how data is encoded for transmission (modulation scheme), and the characteristics of the transmitter and receiver. These are among the most common IEEE 802.11 amendments as seen in Table 1.1 (Microwave & RF).

The IEEE 802.11b/g operates in the 2.4 GHz band, where IEEE 802.11b uses the direct sequence, spread spectrum signaling (DSSS) with a maximum data rate of 11 Mbps, while IEEE 802.11g occupies the same frequency spectrum with a data rate of 54 Mbps with orthogonal frequency division multiplexing (OFDM) modulation methods. However, both 802.11b/g devices suffer interferences from other products operating in this congested 2.4 GHz band.

IEEE 802.11ah is another emerging standard that defines a narrow-band OFDM physical layer (PHY), i.e., 1/2/4/8/16 MHz, operating in the license-exempt bands below 1 GHz (typically 900 MHz band) to provide an extended range to WLAN network. As a result, it suitable for several potential applications, such as Internet of Things (IoT), smart grid, healthcare, smart appliances and wearables.

Hence, this proposed work is mainly targeted to meet the direct conversion receiver front-end for the IEEE 802.11b/g/ah applications.

1.3 Objectives

In the receiver chain, the nonlinearity of the transconductor limits the achievable receiver front-end performance for the current and future wireless communication systems. Accordingly, there is a need for a low-power high linearity active CMOS transconductor for RF wireless communication applications. In summary the main objectives of this project is to:

- Propose an innovative method to enhance linearity performance of the transconductance stage through IM3 cancellation.
- Achieve comparable noise and conversion-gain performances without the penalty of an increase in power consumption and achieve a high figure-of-merit (FOM) in the front-end solution.
- Present a detailed linearity analysis of the proposed front-end architecture using much accurate Volterra series to validate the performance.
- Design high performance front-end solution for the selected 900 MHz and 2.4 GHz wireless communication applications in 130 nm CMOS technology.

1.4 Contributions of This work

This thesis predominantly focuses on the challenges faced when designing front-end receiver for current and future wireless applications. The main context emphasis the techniques of enhancing the linearity of the active transconductor while implementing a demanding functionality in CMOS technology. Subsequently, after a comparative study on the different architectures used in the reported recent works, two distinguished high

linear narrow band transconductors is presented in this work to meet the stringent requirement of the arising wireless communications.

First, a novel highly linear differential folded-mixer using a multiple-feedback transconductor is presented. The common-gate (CG) LNA with dual cross-coupled capacitive (DCC) feedback which was reported in (Han et al., 2015) is utilized into the proposed transconductance stage of the active mixer with additional positive feedback loop to enhance the linearity and also to improve the input impedance matching, the noise figure (NF) and the conversion gain (G_c) performances with a flexible design criterion. The architecture acquires 8.5 dB of double sideband (DSB) NF_{DSB}, 18.4 dB of conversion gain and 12.5 dBm of IIP3 at 900 MHz input frequency with 4mW of power consumption.

In addition, the conventional architecture of front-end receiver generally integrates discrete, independent LNA, mixer and voltage control oscillator (VCO) coupled together with inter-stage matching network, balun or filters. These interleaving circuits lead to additional power consumption and unwanted parasitic components due to an increased complexity of the system. In the recent work of fully integrated RF receivers, some

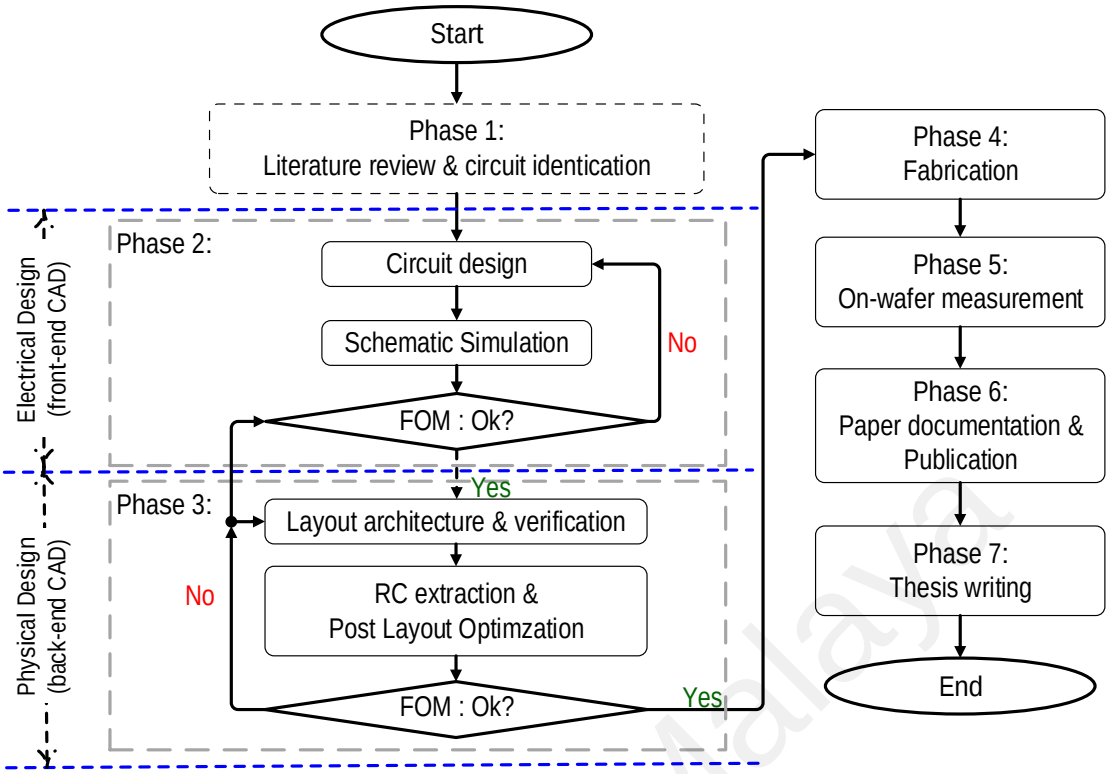


Figure 1.5: Research and design flow.

attempts have been made to merge blocks in order to minimize area, cost and power consumption: merged LNA-mixer (Chong et al., 2014), and oscillator-mixer (Burasa et al., 2016). Therefore, a new combined balun-LNA-mixer based on inductively source degenerated (ISD) transconductor is also presented in this thesis, where a special attention is given in improving the linearity of the circuit, while achieving a low power consumption, high conversion gain and better input impedance matching at the operating frequency. The proposed architecture operating at 2.4 GHz achieves a high IIP3 of +16 dBm and a high G_c of 22 dB. The NF_{DSB} is 7.2 dB with a low power consumption of 3.15 mW at 1.2 V.

Both of the designs have been fabricated and measured on a standard 130 nm CMOS technology process and their performances have been evaluated using rigorous simulation and characterization results. Besides, this thesis also reports a detailed theoretical analysis

of input impedance matching, conversion gain, and noise figure, as well IIP3 of the proposed transconductor by adopting complex Volterra-series.

1.5 Research Methodology

The research work and the circuit design flow are summarized in Figure 1.5, which involves seven major phases. This general methodology flow can be applied for both of the proposed circuits.

Phase 1 involves literature review on the particular topics of the RF front-end receiver circuits and wireless communication system's specification in order to identify promising theories and methods, concurrently, grouping the key techniques and circuit theories to identify the performance gaps by conducting a review of the published sources, such as books, articles, conference proceedings and journals. The selection of the CMOS platform should be finalized at this stage.

Phase 2 identifies proper circuit topology. The design of the circuits are carried out based on realistic components models which includes the losses and parasitic effects instead of ideal component models by using CAD (Computer Aided Design) tools, such Cadence Spectre-RF Simulator. The passive inductors or transformers are simulated to obtain an accurate inductance, quality factor and coupling factor by using SONNET high frequency electromagnetic (EM) software. All the modules and blocks are verified via Cadence Spectre-RF Simulator in order to acquire the desired results. The circuit optimization are repeated until performance specifications are met. Basically, the process involves an iterative optimization by varying devices size, transistors biasing voltages and supply voltages. FOM is set to be the benchmark due to the following reason:

In theory, mixer is indirectly dependent on DC power dissipation, however recent work verified that certain mixer circuits can exhibit high IIP3 performance abstaining the

penalty of the increase in power by adopting proper linearization technique as depicted in Figure 1.3 with blue dots. However, in order to include the rest of the design constraints such as the conversion gain, input impedance matching, and noise figure, more current is needed by the transconductance stage which inevitably translates into high power consumption of the overall mixer/LNA+mixer solution. Therefore, all the related RF parameters must be taken into consideration in verifying and evaluating the performance of the dedicated RF circuit. Obviously, figure-of-merit (FOM) will be an ideal choice in satisfying stringent specification of wireless communication systems. The benchmark should follow the FOM1 (Vidojkovic et al., 2005),

$$FOM1 = 10\log\left(\frac{10^{(G_C(dB)/20)} \times 10^{(IIP3(dBm)-10)/20}}{10^{(NF(dB)/10)} \times P_{DC}(mW)}\right). \quad (1.1)$$

According Equation 1.1, a high performance RF circuit is characterized by minimum noise figure, high conversion gain, high IIP3, and low DC power dissipation. For advance CMOS technology, it is difficult in maintaining high conversion gain with high linearity due to the swing limitation in reduced supply headroom. Therefore, recent published work on mixers includes supply voltage in the denominator of the FOM2 as (Asghari & Yavari, 2016):

$$FOM2 = 10\log\left(\frac{10^{G_C(dB)/20} \times 10^{(IIP3(dB)-10)/20}}{10^{NF(dB)/10} \times P_{DC}(mW) \times V_{DD}(V)}\right). \quad (1.2)$$

A high FOM value, indirectly indicates a balanced trade-offs made within the parameters.

Phase 3 defines circuit layout by using Cadence Virtuoso XL. Layout Design Rule Check (DRC) and Layout Versus Schematic (LVS) tests are executed through by using Mentor Graphic Calibre. Post-layout simulation on the circuit is performed incorporating parasitic extraction, resulted from the elements layout. The performances are verified in

post layout extractor, where redesign and optimization of the circuit (from phase 2) and layout are undertaken until the design specifications are met.

Phase 4 prepares the GDS file of the final layout for tape-out process.

Phase 5 develops the testbench setup for on-wafer measurement on the fabricated chips. The obtained results are tabulated and compared with the simulated outputs.

Phase 6 is in the compilation of the results into journals/conference proceedings.

Phase 7 concludes the entire project findings in thesis.

1.6 Thesis Outline

This thesis is organized into five chapters including the introduction. The introduction elaborates on the motivation for the linearity improvement in wireless receiver front-ends. Based on the context of the project, a list of objective are presented in order to clearly define the scope of this work. The following chapters of this thesis are organized as follows:

Chapter 2 introduces the basic configuration of LNA and mixer circuits. The key performance metric in defining the linearity of the circuits such as 1-dB compression point and input referred 3rd-order intercept are included in this chapter. Several state-of-art linearity enhancement techniques are also presented to provide the understanding of distortion cancellation using Taylor series as well as to address the limitation of those techniques.

Chapter 3 describes and analyses in detail the proposed differential-folded mixer with CG transconductor using multiple-feedback to realise high IIP3 and low noise. This chapter also summarizes the simulated and the measured results, as well compares the

output to the recent published state-of-the-art mixer topologies, followed by the conclusions.

Chapter 4 presents the proposed inductively source degenerated balun-LNA-mixer with integrated transformer-based gate inductor and IM2 injection technique circuit for the front-end receiver. By using linearity enhancement techniques such as 2^{nd}-order intermodulation (IM2) injection and optimum biasing, the IIP3 of the overall circuit is effectively improved. The simulation and measurement results are discussed at the end of the chapter.

Chapter 5 summarizes the major contributions of this thesis and discusses the possibilities of the future work in an extension that can be realized to further improve the proposed architectures.

CHAPTER 2: LITERATURE REVIEW

This chapter provides background information on the basic LNA and mixer circuits. Before proceeding to an in-depth analysis on the linearity techniques, a brief review of transcondcutor nonlinear behaviors together with the corresponding metrics is presented. Finally, a literature review on linearization techniques with the benefits and disadvantages are elaborated. Some of the techniques presented in this chapter are used in the presented front-end receiver (mixer and LNA+mixer) in the following chapters. As this thesis focuses in down-converting mixers, the mixers mentioned herein refer to these down-converters unless specified otherwise.

2.1 Introduction

The wireless signal propagating in open space is susceptible to electronic noise, interference, and attenuation; therefore, in order to accurately retrieve the original information, a high performance receiver is needed. LNA and mixer are important circuits at the receiver front-end to fulfil the requirements and specifications of the wireless applications.

According to IIP3 cascade theory in Equation (2.1), IIP3 of the last stage (IF amplifier in Figure 2.1) will determine the entire linearity of the cascaded front-end receiver as it is scaled down by the total gain of the preceding blocks. However, this concept only valid if that linearity of LNA and mixer are not limiting factor.

$$\frac{1}{IIP3_{tot}} \approx \frac{1}{IIP3_{LNA}} + \frac{G_{LNA}}{IIP3_{MIX}} + \frac{G_{LNA}G_{MIX}}{IIP3_{IF}} \tag{2.1}$$

As an example consider the simplified model of the cascaded RF heterodyne front-end in Figure 2.1 with an IF amplifier power gain, G_{IF} of 15 dB and $IIP3_{IF}$ of 30 dBm, whereas IIP3 of LNA, $IIP3_{LNA}$ and power conversion-gain of mixer, G_{MIX} is equal to 10 dBm and 5 dB, respectively. Assume each block is matched to input termination and interstage

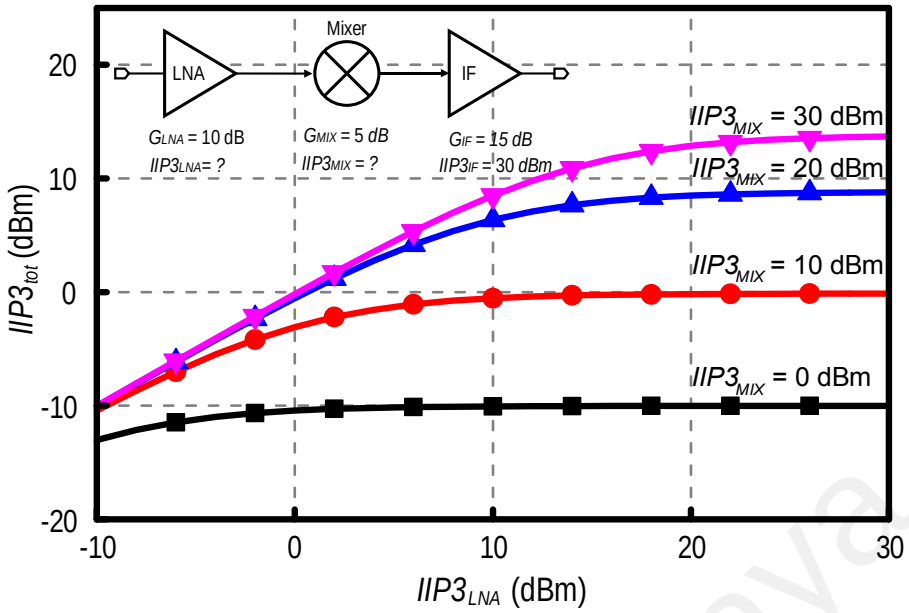


Figure 2.1: Total IIP3 of the cascade receiver circuit versus IIP3 of LNA at different mixer's IIP3.

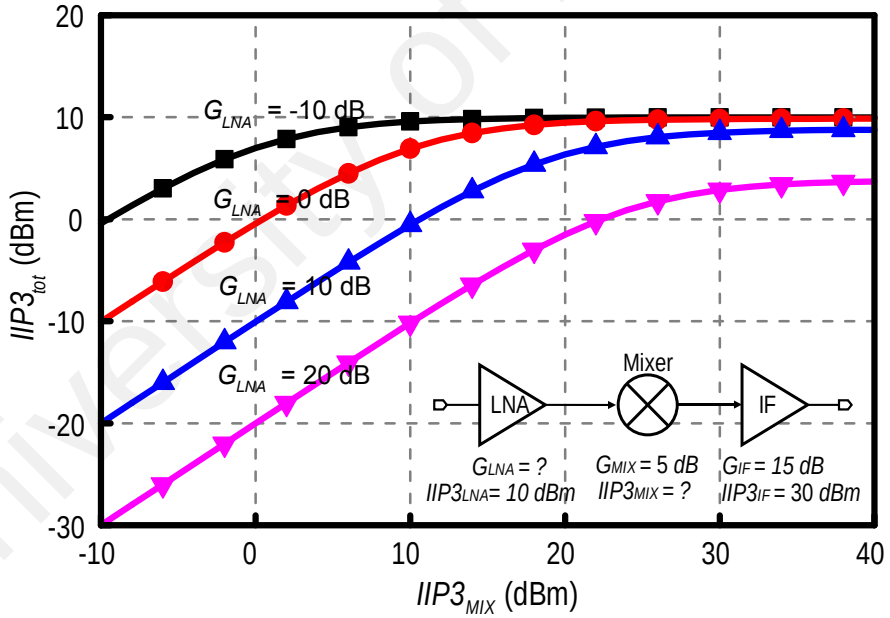


Figure 2.2: Total IIP3 of the cascade receiver circuit versus IIP3 of mixer at different LNA's gain.

filters are neglected. Figure 2.1 shows the results of the calculated total IIP3 of cascade system, $IIP3_{tot}$ as function of the mixer linearity for the different IIP3 of LNA. It is observed that the $IIP3_{tot}$ is strongly dependent on both the intercept point levels of LNA

and mixer. When the gain of the LNA block is higher the $IIP3_{tot}$ degrades and linearity requirement of the mixer becomes stringent as illustrated in Figure 2.2. Due to high gain of the forefront LNA, both the desired signals and interferers are amplified by the LNA before they pass through the mixer. Many interferers are too close to the wanted signals and those interferers can be much stronger than the desired signal.

Early RF receiver front-end architectures usually consists of separate integrating blocks and a compromise in the performance of the individual block occurs during system integration. Later, more advanced receiver front-end architectures were introduced with higher efficiency and lower power consumption by integrating different functions in same block with a mixture of voltage and current mode operation; e.g. the Blixer (Blaakmeer et al., 2008), stacked LNA-mixer-VCO, (LMV) (Selvakumar et al., 2015) and merged mixer (Guo et al., 2014), Therefore, in order to realize LNA and mixer into a single block, its transconductance stage must achieve high gain, low noise figure, high linearity, and good input matching at the operating frequency. When an active mixer is used, a single transistor based transconductance stage is sufficient to provide reasonable performance.

2.2 Low-Noise Amplifier (LNA)

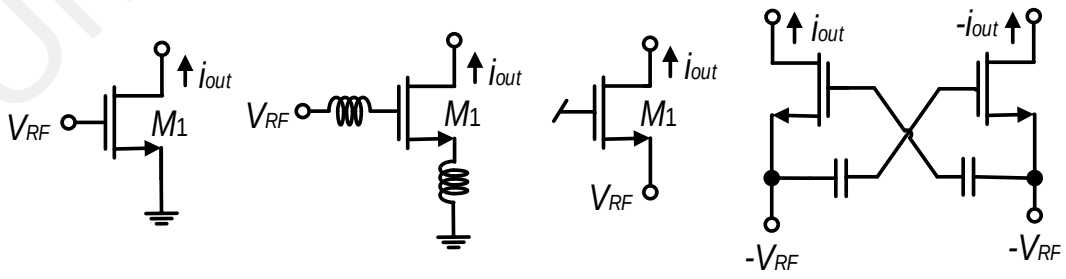
The low noise amplifier is the first block in most RF front-end receivers after the antenna. As a first stage, it amplifies the received incoming weak signal while introducing minimum amount noise to the signal. Generally, the overall noise factor of the receiver front-end is defined by the LNA block respective to the Friis' equation given as

$$F_{tot} \approx F_{LNA} + \frac{F_{MIX} - 1}{G_{LNA}} + \frac{(F_{MIX} - 1)(F_{IF} - 1)}{G_{LNA} G_{MIX}} \tag{2.2}$$

where F_{LNA} and G_{LNA} are noise factor and gain of the LNA, respectively. As described in Equation (2.2), F_{LNA} contributes the dominant noise factor in the receiver and the noise factor of the subsequent stage degrades by the LNA gain. Hence, a LNA with high gain

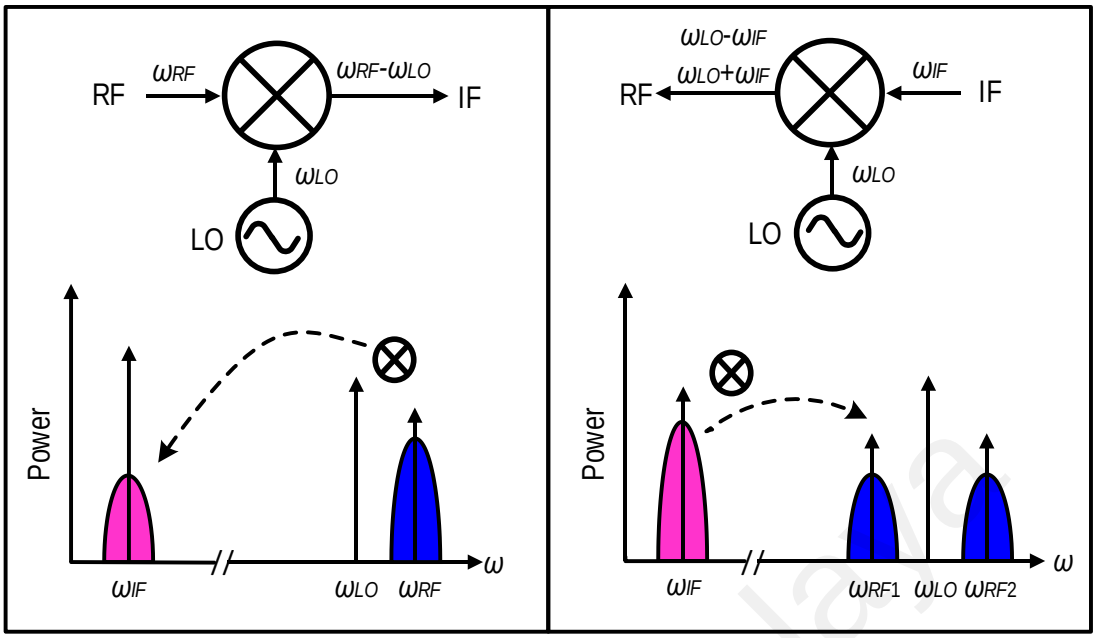
and low noise figure are highly desirable to enhance the cumulative performance of the receiver.

When the LNA is used as a transconductance in active mixer (stacked structure), it has three main roles: 1) It has to transform RF voltage signal to an RF current signal while introducing minimum noise to the circuit, 2) it should provide good input impedance matching to maximize power transfer of the received RF signal, and 3) it should observe sufficient gain and good linearity to maintain performances the of the entire receiver circuit. Common-gate and common-source (CS) amplifiers are the most commonly adopted transconductance LNA in wireless applications. Figure 2.3(a) shows CS transconductor, where it has sufficient transconductance, but does not provides input impedance matching. Thus, CS transconductor with inductive source generation as shown in Figure 2.3(b) is often used to provide a narrowband input matching and its effective transconductance is equal to $G_m(=\omega_T L_s)$. For instance, the ISD common-gate LNA is not very effective for high linearity due to the 2nd-order interaction issue which is caused by the feedback path between the output current, i_{out} and the gate-source voltage V_{RF}. Figure 2.3(c) shows the single-ended CG transconductance LNA where it has a wideband input impedance matching characteristic ($Z_{in}=1/g_m$) at the cost of high transistor g_m (≈20mS)



(a) (b) (c) (d)

Figure 2.3: LNA topologies. (a) Common-source. (b) Common-source with ISD. (c) Common-source. (d) CCC differential common-gate.



(a) (b)

Figure 2.4: (a) Down-conversion and (b) up-conversion mixing process

requirement. As a solution to the CG LNA setbacks, Figure 2.3(d) shows the capacitor cross-couple differential common-gate LNA where it boosts the transistor g_m (≈10 mS) at reduced bias current and minimize the 2nd-order harmonic feedback effect on the IIP3.

2.3 Mixer

A nonlinear three terminals device that performs frequency conversion in the transceiver is called mixer. A down-conversion mixer convert the high RF to low IF in the receiver (for demodulation process), an up-conversion mixer converts the low intermediate frequency (IF) to high RF frequency in the transmitter (for modulation process) by providing a local oscillator (LO) input signal as shown in Figure 2.4. A straight forward mathematical identity can be utilized to show the mixing operation of the down-conversion mixer. Ideally, the mixer can be treated as a multiplier, assuming the RF input signal is $v_{RF}(t) = V_{RF} \cos(\omega_{RF}t)$ and the LO signal is $v_{LO}(t) = V_{LO} \cos(\omega_{LO}t)$, then the output IF signal can be described as

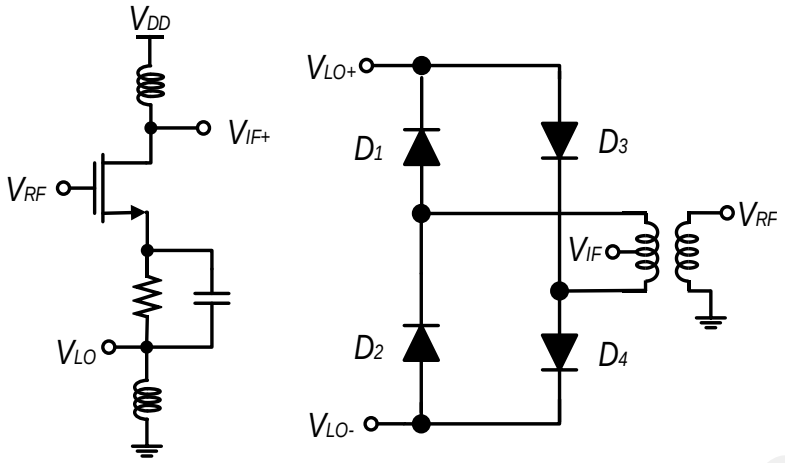
$$
\begin{aligned}
v_{IF}(t) &= v_{RF}(t) \times v_{LO}(t) \\
&= \frac{V_{RF}V_{LO}}{2}\left[\cos\left(\omega_{RF}+\omega_{LO}\right)t + \cos\left(\omega_{RF}-\omega_{LO}\right)t\right]
\end{aligned} \tag{2.3}
$$

From the above equation, it can be observed that the output signals are produced at the sum and difference frequencies of RF and LO signals. For down-conversion mixer, the difference output signal (ω_{RF}-ω_{LO}) is desired and the sum output signal (ω_{RF}+ω_{LO}) is filtered out at the output stage. Alternately, if the mixer is being used for up-conversion mixer, the IF and LO signals become inputs and the RF as an output signal with a frequency of (ω_{IF}±ω_{LO}). To perform this frequency translation, potential nonlinear devices are needed includes diodes, transistors and superconducting junctions for sub-millimeter waves.

2.4 Active and Passive Mixers

Mixer can be classified into two main types, knowns as active mixer and passive mixer as shown in Figure 2.5(a) and 2.5(b), respectively. The active mixer includes the transistor-level structure where the RF signal is fed into the gate of the transistor M_1 to convert the RF input voltage signal into a current. Subsequently, the same transistor M_1 commutate the current to the IF output at each LO period. The passive mixer is the most common and simplest solution. During the positive LO cycle, the left two diodes (D_1 and D_2) are turned on, and positive RF will allow the IF current to flow out of the transformer. During negative LO cycle, the right two diodes (D_3 and D_4) are turned on, and negative RF will allow the IF current o flow out of the transformer. Both the active and passive mixers are compared in Table 2.1 to appreciate their respective performance.

The passive mixer does not provide conversion gain and consume any power. As a result, the passive mixer has been widely chosen when the linearity and power budget is the main requirement of the circuit. Despite the unique advantages of passive mixers, such as high linearity, wider bandwidth operation and zero current dissipation resulting



(a) (b)

Figure 2.5: A typical (a) MOS active mixer and (b) diode passive mixer

Table 2.1: Comparison between active and passive mixers in Figure 2.2 (Li, 2009)

Performances	**Active mixer**	**Passive mixer**
Current drain	~-2 to 5	~0
LO Injection (dBm)	~-10 to 0	~-5 to 10
Conversion Gain (dB)	~5 to 10	~-5 to -3
Noise Figure (dB)	~10 to 15	~3 to 5
IIP3 (dBm)	~-8 at G_c=8dB	~-5 to -2 at G_c=-4 to -4.5 dB
Bandwidth	Narrower	Wider
Part count	~13	~6
Reliability	Lower	Higher
Cost	Lower	Higher

in lower flicker noise, the receiver still needs current to integrate additional filters in rejecting the unwanted harmonics at the output IF port. In addition to that, a large LO signal amplitude is required to periodically switch on and off the passive transistors and as a result, the LO drive circuits consume a large amount of power to attain a large LO signal swing. The passive mixer also has significant signal power loss and its NF is nearly equals to its power loss as can be observed from Table 2.1.

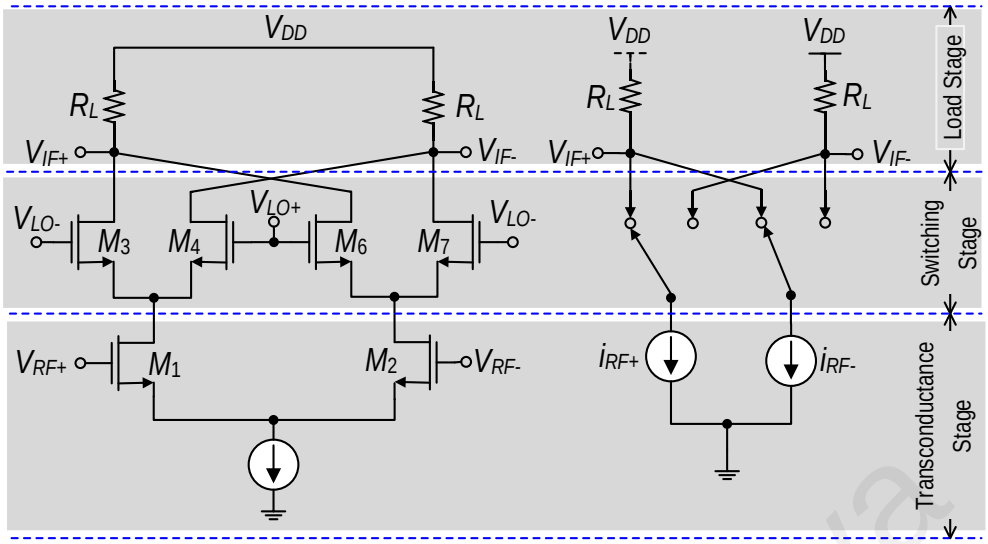


Figure 2.6: Gilbert cell mixer circuit with working principle.

On the other hand, the active mixer provides conversion gain at the cost of static power consumption, a higher noise figure, and lower operating bandwidth. The total noise contributions might be higher than passive mixer, but the noise can be suppressed further by higher gain. Conversion gain is important in wireless receiver because it relaxes the gain requirements from the preceding LNA block and suppresses noise contributions from the subsequent IF stages. The required LO injection level is also much lower than that in a passive mixer and result in reducing the total power consumption of the receiver. However, it has poor linearity due to the nonlinearity characteristic of the transconductor.

Gilbert cell active mixers are the most well-known and popular types of double-balanced active mixer, which contains three main stages as shown in Figure 2.6. The first stage is the transconductance stage which consists of transistor M_1-M_2 as a transconductor, where the incoming RF input voltage is converted into current (V-I). In the switching stage, transistors M_3-M_6 are biased in subthreshold region to operate as switches, so that ideally it can be fed a square waveform at a large LO signal swing. The amplified current from the transconductance stage is alternately redirected into one of the two load R_L branches to execute the multiplication process with the square-wave LO

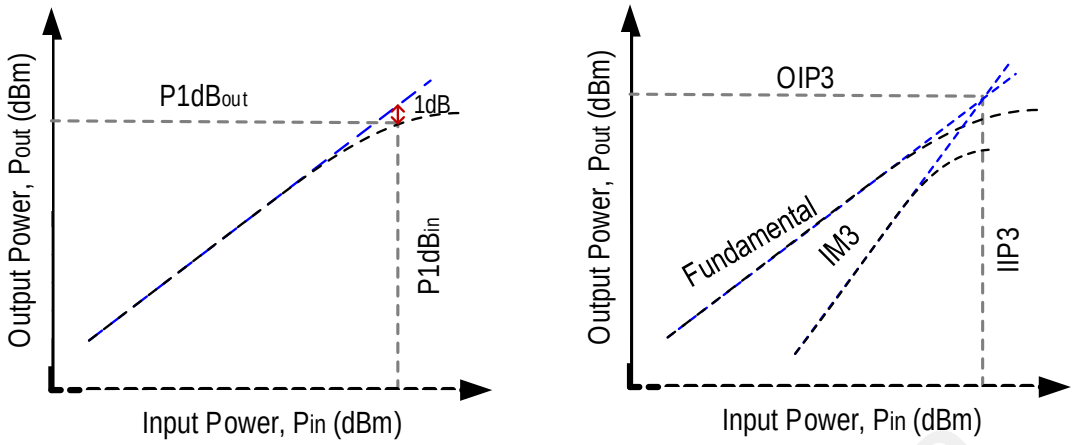


Figure 2.7: (a) 1-dB compression point. (b) 3rd order intercept point.

signals. In this mixer, its IIP3 is proportional to the square root of the bias current flowing in the input transconductance stage. When the bias current is increased to improve the linearity of the transconductance stage, the voltage headroom of the switching stage is reduced due to bias current sharing behavior in a stacked structure. As a result, the linearity improvement of the mixer is not achievable. This problem can be solved using linearization technique along with current bleeding or folded architecture. Ultimately, the current bleeding or folded architecture allows lower current flow in the switching stage, thus resulting in a smaller LO power requirement due to the soft switching and high conversion gain due to the large load resistance and high input transconductance. Meanwhile the nonlinearity contribution from the input transconductance stage can be improved by several linearization techniques.

2.5 Nonlinearity Analysis

Before initiating an analysis of how to design a high linear transcondcutor, the nonlinear relationship between input and output of the transconductor must be identify and understand well. For the sake of simplicity, assuming the system is memoryless (no

capacitor and/or inductor or operate at low frequency) and thus, the input-output signal is specified by third-order nonlinearity function as:

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \ldots \tag{2.4}$$

where a_n is a coefficient constant, $x(t)$ and $y(t)$ represent the input and output signals, respectively. Assuming that the input signal is a simple sinusoidal signal with a single tone which can be expressed as

$$x(t) = A\cos(\omega_{RF} t) \tag{2.5}$$

Substituting this expression into Equation (2.4), yields

$$\begin{aligned} y(t) &= a_1 A\cos(\omega_{RF} t) + a_2 A^2 \cos^2(\omega_{RF} t) + a_3 A^3 \cos^3(\omega_{RF} t) + \ldots \\ &= \frac{1}{2} a_2 A^2 + \underbrace{\left(a_1 A + \frac{3}{4} a_3 A^3 \right)}_{\text{fundamental}} \cos(\omega_{RF} t) + \underbrace{\left(\frac{1}{2} a_2 A^2 \right)}_{\text{2nd order signal}} \cos(2\omega_{RF} t) \\ &\quad + \underbrace{\left(\frac{1}{4} a_3 A^3 \right)}_{\text{3rd order signal}} \cos(3\omega_{RF} t) + \ldots \end{aligned} \tag{2.6}$$

In most cases, the coefficient a_3 is negative, and hence, as the input signal is increased, the contribution of the second term in fundamental signal is dominant. Therefore, a gain compression occurs in the system by the large amplitudes of the desired input signal. In RF circuits, this effect is quantified by the 1-dB compression point (P1dB). Figure 2.7 (a) shows the plot of the 1-dB compression point. Above the P1dB, the desired output signal amplitude gets distorted. In other words, the P1dB is simply a measure of the dynamic range of the circuit where the maximum RF input signal that can be processed by the receiver.

Due to the nonlinear behavior of the transistor, there are more than one tone signal or/and interferers present at the input which produces undesired intermodulation products at the output. Mainly, the third-order intermodulation products (IM3) are the most critical

components because they appear in vicinity of the desired output signal. A convenient way to analyze the third-order intermodulation products is to apply two input signals of RF_1 and RF_2 with a small frequency.

$$x(t) = \underbrace{A_1 \cos(\omega_{RF1} t)}_{RF_1} + \underbrace{A_2 \cos(\omega_{RF2} t)}_{RF_2} \tag{2.7}$$

Assuming the RF_1 is the wanted input signal, while the RF_2 is considered as an interferer. By substituting the Equation (2.7) into (2.4), yields the following expression

$$\begin{aligned} y(\mathrm{t}) &= a_1 A_1 \cos(\omega_{RF1} t) + a_1 A_2 \cos(\omega_{RF2} t) + a_2 \left[A_1 \cos(\omega_{RF1}\,\mathrm{t}) + A_2 \cos(\omega_{RF2} t) \right]^2 \\ &\quad + a_3 [A_1 \cos(\omega_{RF1} t) + A_2 \cos(\omega_{RF2} t)]^3 + \ldots \\ &= \frac{1}{2} a_2 (A_1^2 + A_2^2) + \left(a_1 A_1 + \frac{3}{4} a_3 A_1^3 + \frac{3}{2} a_3 A_1 A_2^2 \right) \cos(\omega_{RF1} t) \\ &\quad + \left(a_1 A_2 + \frac{3}{4} a_3 A_2^3 + \frac{3}{2} a_3 A_1^2 A_2 \right) \cos(\omega_{RF2} t) + \left(\frac{1}{2} a_2 A_1^2 \right) \cos(2\omega_{RF1} t) \\ &\quad + \left(\frac{1}{2} a_2 A_2^2 \right) \cos(2\omega_{RF2} t) + a_1 A_1 A_2 \cos(\omega_{RF1} \pm \omega_{RF2}) t \\ &\quad + \left(\frac{1}{4} a_3 A_1^3 \right) \cos(3\omega_{RF1} t) + \left(\frac{1}{4} a_3 A_2^3 \right) \cos(3\omega_{RF2} t) \\ &\quad + \frac{3}{4} a_3 A_1^2 A_2 \cos(2\omega_{RF1} \pm \omega_{RF2}) t + \frac{3}{4} a_3 A_1 A_2^2 \cos(2\omega_{RF2} \pm \omega_{RF1}) t \end{aligned} \tag{2.8}$$

If the two input signals have equal amplitude, $A_1 = A_2 = A$, then the third-order intermodulation products become

$$2\omega_{RF1} \pm \omega_{RF2} : \frac{3}{4} a_3 A^3 \left[\cos(2\omega_{RF1} + \omega_{RF2}) t + \cos(2\omega_{RF1} - \omega_{RF2}) t \right] \tag{2.9}$$

$$2\omega_{RF2} \pm \omega_{RF1} : \frac{3}{4} a_3 A^3 \left[\cos(2\omega_{RF2} + \omega_{RF1}) t + \cos(2\omega_{RF2} - \omega_{RF1}) t \right] \tag{2.10}$$

These RF signals will mix with LO consequently to form third-order intermodulation products at $[(2\omega_{RF1} \pm \omega_{RF2}) \pm \omega_{LO}]$ and $[(2\omega_{RF2} \pm \omega_{RF1}) \pm \omega_{LO}]$ as well as other undesirable intermodulation products and harmonics. Note that in the case of a down-conversion mixer, only the signal at the (ω_{RF1} - ω_{LO}) is desired. The two IM3 products at [(2ω_{RF1} -

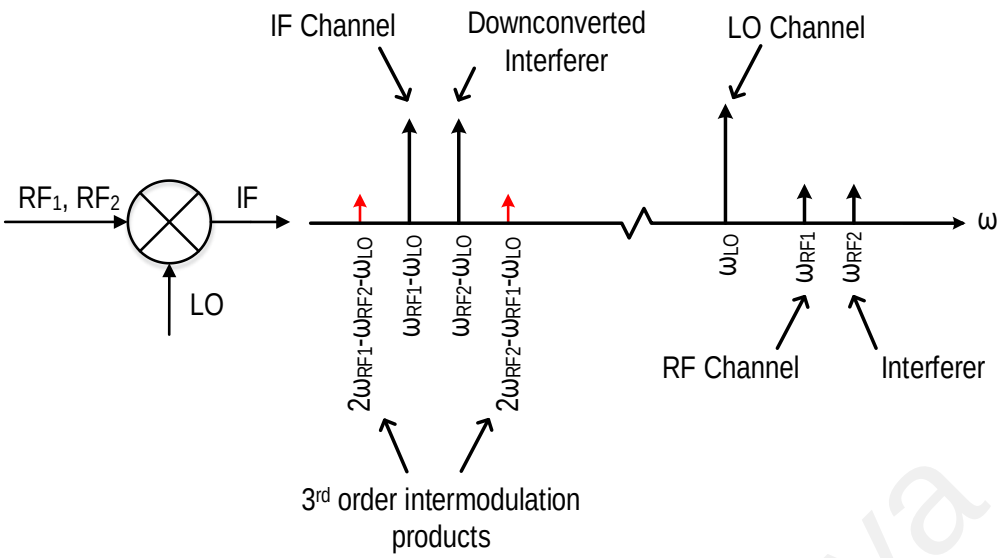


Figure 2.8: Third-order intermodulation products excited at the output of the mixer by two RF signals at frequencies ω_{RF1} and ω_{RF2}.

ω_{RF2}) - ω_{LO}] and [(2ω_{RF2} - ω_{RF1}) - ω_{LO}] are adjacent to the desired IF signal as shown in Figure 2.8. As a result, the components face difficulty in being filtered out and cause severe interference. If they fall in the band of the desired output, the desired output signal may be corrupted.

Note that the magnitude of IM3 increases in proportion to A^3, thus it increases much faster that the fundamental output signals. The parameter of 3rd-order intercept point (IP3) is usually used to quantify the level of 3rd order intermodulation where the linear extrapolation of the fundamental equals the linear extrapolation of the IM3 response, as illustrated in Figure 2.7(b). The value of the IP3 depends on the circuit's linearity. The more linear the circuit, the higher the IP3 because of the superior suppression of the third-order intermodulation product.

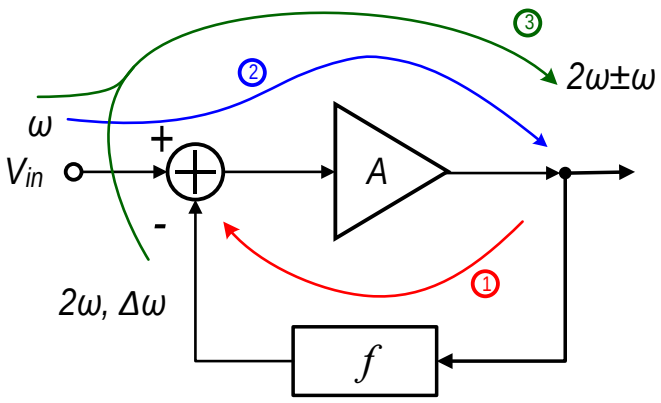


Figure 2.9: A nonlinear amplifier with negative feedback.

2.6 Linearization Techniques

Linearization techniques are highly desirable for the front-end receiver. The implemented linearization techniques should be simple with limited power budget, at the same time should preserve other RF performances. Many traditional linearization techniques are already available in the market, such as resistive source degeneration and floating-gate input attenuation topologies, but these techniques are not feasible for the high in demand wireless applications, as they reduce the gain/conversion gain and deteriorate NF or input impedance matching. Hence, linearization for the RF circuit is more challenging, and often needs innovative techniques. This section discusses few linearization techniques to increase the linearity of the transconductor in terms of their advantages and limitations.

2.6.1 Feedback

Based on feedback theory, a closed-loop negative feedback system can be adopted to linearize the active device in a feedforward path with a loop gain, G_L and the IIP3 of this feedback system, $IIP3_{CL}$ can be approximately related with IIP3 of the open loop, $IIP3_{OL}$ circuit as (Rossi et al., 2005)

$$IIP3_{CL} \approx IIP3_{OL} \times (1+G_L)^3 \tag{2.11}$$

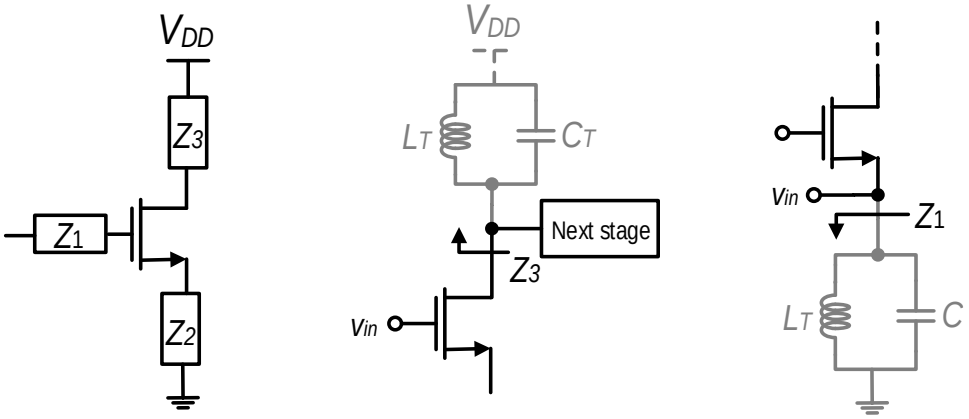
where $IIP3_{OL}$ is IIP*3* of the open-loop circuit with the absence of the negative feedback loop. As can be seen in Equation (2.11), the feedback topology can increase IIP3 by boosting G_L, however, it is limited by the gain, noise and power consumption of the RF circuit. Besides, the above equation is only valid when the 2nd-order nonlinear coefficient of main transistor, g'_m is zero which never the case in a typical feedback circuit.

Referring to the negative feedback block diagram of Figure 2.9, the IIP2 and IIP3 for a closed loop system with nonlinear amplifier and linear feedback, f can be expressed as (Sansen, 1999)

$$AIP2_{CL} = \sqrt{\frac{g_m}{g'_m}(1+G_L)^2} \tag{2.12}$$

$$AIP3_{CL} = \sqrt{\frac{4}{3}\frac{g_m}{g''_m}\frac{(1+G_L)^3}{\left(1-\frac{2g'^2_m}{g_m g''_m}\frac{G_L}{1+G_L}\right)}} \tag{2.13}$$

where g_m, g'_m and g''_m are the linear, 2nd- and 3rd-order nonlinear coefficients of the transistor, respectively. As seen in Equations (2.12) and (2.13), AIP2 is improved by a factor of $(1+G_L)^2$; whereas an increase in IIP3 is proportional to $(1+G_L)^3$ but only when g'_m is zero. The finite g'_m contributes to the IM3 distortion and degrades IIP3, this phenomenon known as 2nd-order interaction. This distortion generating process is illustrated in Figure 2.9; (1) the nonlinear of the transistor/amplifier contains 2nd-order nonlinear component at the output, (2) subsequently this intrinsic 2nd-order nonlinear is fed back to the input of the amplifier, and, (3) mixed with the fundamental input signal and intermodulated into IM3. This phenomenon is common in an ISD transconductor topology (Lee, 2004) and also due to the feedback path between input and output by the source degenerated inductance.



(a) (b) (c)

Figure 2.10: (a) Harmonic termination technique in CS amplifier with termination impedances. (b) CS with LC resonating RF current source (Kim et al.,2004). (c) CG with RF current source (Kim, 2009).

2.6.2 Harmonic Termination

Harmonic termination is the most simplest technique, where it integrates a termination network to the circuit to reduce the contribution of 2nd-order distortion ($\Delta\omega$, 2ω) to the 3rd-order distortion or to cancel the intrinsic 3rd-order distortion by tuning the amplitude and phase of the generated 2nd-order interaction terms (due to feedback) at certain frequencies. This can be explained well by capturing memory effects of the frequency-dependent network such as inductively source-degenerated (ISD) common-source (CS) transconductor using Volterra series analysis.

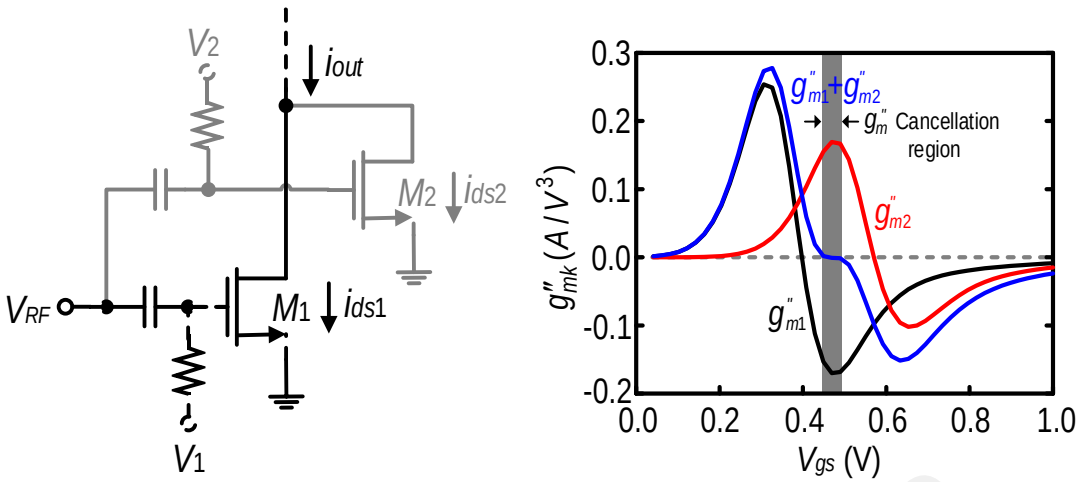
The detailed derivation for two tone IIP3 based on Volterra series for ISD transconductor will be discussed in Chapter 4, thus, only the expression of $\varepsilon(\pm\omega_1 \mp \omega_2, \pm 2\omega_1)$ in Equation (4.6) is adopted here to describe the working principle of the harmonic termination technique.

$$\varepsilon(\pm\omega_1 \mp \omega_2, \pm 2\omega_1) = \underbrace{g_m''}_{\text{intrinsic\_3rd\_order}} \underbrace{-\frac{2}{3}(g_m')^2 \cdot \left(\frac{2}{g_m + g(\pm\omega_1 \mp \omega_2)} + \frac{1}{g_m + g(\pm 2\omega_1)} \right)}_{\text{2nd-order\_interaction}} \quad (2.14)$$

where $g(\pm\omega_1 \mp \omega_2)$ and $g(\pm 2\omega_1)$ are conductance functions that is defined by the circuit loop gain and termination impedances at the 2nd-order frequencies, i.e., $\pm\omega_1 \mp \omega_2$ and $\pm 2\omega_1$. Equation (2.14) shows that the total 3rd-order distortion depends on both intrinsic 3rd-order nonlinearity in the drain current, g_m'' and 2nd-order interaction component. For a stable amplifier, the 2nd term in Equation (2.14) has a positive real part; and its amplitude and phase depends on the input and output impedance networks. Thus, if g_m'' is a positive value, the 2nd term can be optimized to cancel the g_m'' by adjusting the termination impedance at 2nd-order frequency. It means the MOS transistor must be operate in a weak or moderate region inversion region to cancel the 3rd-order distortions.

For the circuit using a MOS in strong inversion, the harmonic termination technique can be used to decrease the contribution of 2nd-order interaction to the overall 3rd-order nonlinearity instead of cancelling the g_m'' component. Typically, the termination impedance tuning is performed by the resonant *LC* tanks as shown in Figure 2.10(b) and (c). However, the required inductance value is very large with high *Q* factor, resulting in a practical off-chip inductors being used. The low *Q* factors of on-chip inductors limit the linearity improvement and add in noise, as well effect the input matching. As an alternative, a cascode topology can be used to reduce Z_3 to $1/g_m$ and capacitor cross-coupling in the cascode transistor to further reduce Z_3 to $1/2g_m$ (Fan et al., 2008) in Figure 2.10(a). However, the linearity improvement is not as good as the harmonic termination technique as it benefits from less area consumption and wide operating frequency range.

In CMOS transconductor, in-order to achieve a substantial linearity improvement without affecting the gain and noise, harmonic termination technique is not sufficient as both the intrinsic 3rd-order coefficient and 2nd-order interaction components must be reduced simultaneously.



(a) (b)

Figure 2.11: (a) Derivative superposition technique and (b) its linearization concept.

2.6.3 Feedforward and Derivative Superposition (DS)

A feedforward technique consists of a main nonlinear amplifier and an auxiliary path at the input, whereas the output signal is a difference of the corresponding output signals from each of the main and auxiliary paths (Yongwang & Harjani, 2002). The auxiliary path includes a replica amplifier and signal-scaling factors (b and $1/b^n$) to cancel the IM3 distortion in main path. In practice, due to the auxiliary path is an exact replica of the main amplifier, the total power consumption, and noise are increased.

The derivative superposition technique ((Kim et al, 2004; Kim, 2009) is one of the modifications of feedforward method, where the opposite sign of 3rd derivative of an auxiliary transistor M_2, g''_{m2} is used to cancel the 3rd derivative of main input transistor M_1, g''_{m1}. The simplified schematic of the DS technique is shown in Figure 2.11. The drain current of the transistors M_1 and M_2 can be expressed using a Taylor series as

$$i_{ds1} \approx g_{m1}v_{RF} + g'_{m1}v_{RF}^2 + g''_{m1}v_{RF}^3 + \ldots \quad (2.15)$$

and

$$i_{ds2} \approx g_{m2}v_{RF} + g'_{m2}v_{RF}^2 + g''_{m2}v_{RF}^3 + \ldots \quad (2.16)$$

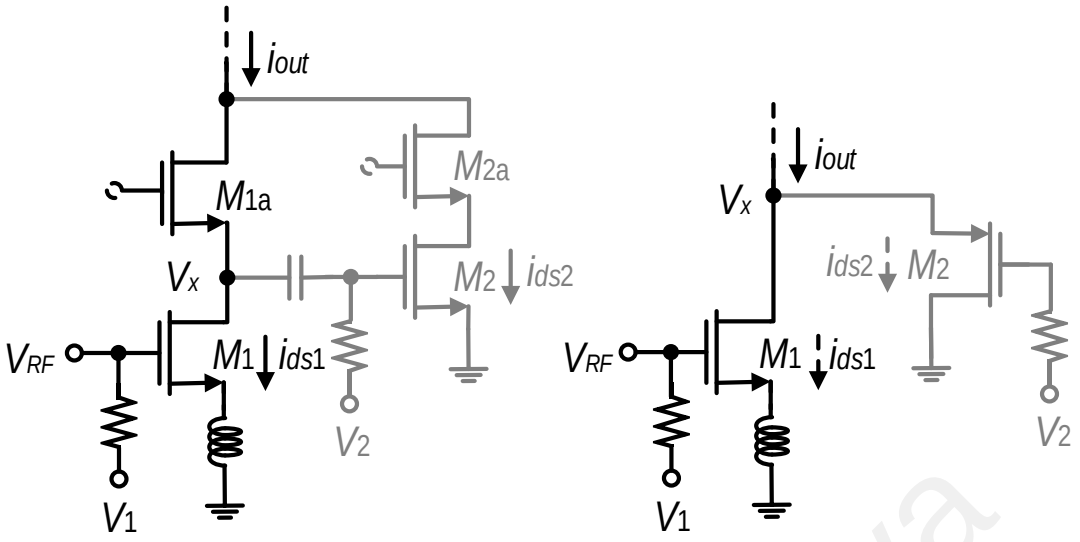
respectively. The output current, i_{out} is the sum of currents i_{ds1} and i_{ds2}, thus

$$\begin{aligned} i_{out} &= i_{ds1} + i_{ds2} \\ &= (g_{m1} + g_{m2})v_{RF} + (g'_{m1} + g'_{m2})v_{RF}^2 + (g''_{m1} + g''_{m2})v_{RF}^3 \end{aligned} \tag{2.17}$$

As can be seen from Figure 2.11(b), the value of g''_m is changing across the gate-source voltage, V_{gs} as the transistor changes from weak, moderate, and strong inversion regions. Generally, the transistor M_1 operates in strong region with a positive value of g''_{m1} to provide high gain and low noise results; transistor M_2 works in weak inversion region with a negative value of g''_{m2} and an equal value to that of transistor M_1 to create net zero ($g''_{m1} + g''_{m2}$) according Equation (2.17), resulting in a high IIP3. The main advantage of this technique over feedforward method is in the minimum power consumption as transistor M_2 operates in weak inversion region and no scaling factor is needed in creating out of phase IM3 products. However, since the gate of transistor M_2 directly connected together with the gate node of the input transistor M_1, gate noise of the transistor M_1 are affected due to the gate noise induced by transistor M_2, resulting in the noise and input impedance matching to be degraded.

2.6.4 Post Distortion (PD)

The post distortion (PD) technique (Kim et al, 2006; Kim & Kim 2006; Zhang et al., 2009) is a similar concept with the previously described PS method with that an auxiliary transistor's nonlinearity is being used to cancel out the nonlinearity of the main path, but it differs in the auxiliary transistor's connection and operating region. Figures 2.12(a) and (b) show PD implementation circuits, where the auxiliary transistor M_2 is connected to the output of the main transistor M_1 instead of directly connecting to the input. In this way, all the transistors can operate in saturation region and it minimizes the impact on input impedance matching.



(a) (b)

Figure 2.12: (a) Post distortion technique based on (a) NMOS auxiliary transistor (Kim et al., 2006) and (b) PMOS auxiliary transistor (Kim & Kim 2006)

Similar to the DS method, the drain currents of M_1 and M_2 can be modeled using Taylor series as

$$i_{ds1} \approx g_{m1}v_{RF} + g'_{m1}v_{RF}^2 + g''_{m1}v_{RF}^3 + ... \tag{2.18}$$

and

$$i_{ds2} \approx g_{m2}v_x + g'_{m2}v_x^2 + g''_{m2}v_x^3 + ... \tag{2.19}$$

respectively. The voltage node v_x is related with the input voltage as

$$v_x = -b_1 v_{RF} - b_2 v_{RF}^2 - b_3 v_{RF}^3 \tag{2.20}$$

where b_n is the nth-order frequency-dependent parameter with positive value and can be extracted from simulation. At the output node, the sum of the current i_{ds1} and i_{ds2}, yields

$$\begin{aligned} i_{out} &= i_{ds1} + i_{ds2} \\ &= \underbrace{(g_{m1} - b_1 g_{m2})}_{Fundamental} v_{RF} + \underbrace{(g'_{m1} - b_1^2 g'_{m2} - b_2 g_{m2})}_{2^{nd}-order\ nonlinear} v_{RF}^2 \\ &\quad - \underbrace{(g''_{m1} - b_1^3 g''_{m2} - b_3 g_{m2} - 2b_1 b_2 g'_{m2})}_{3^{rd}-order\ nonlinear} v_{RF}^3 \end{aligned} \tag{2.21}$$

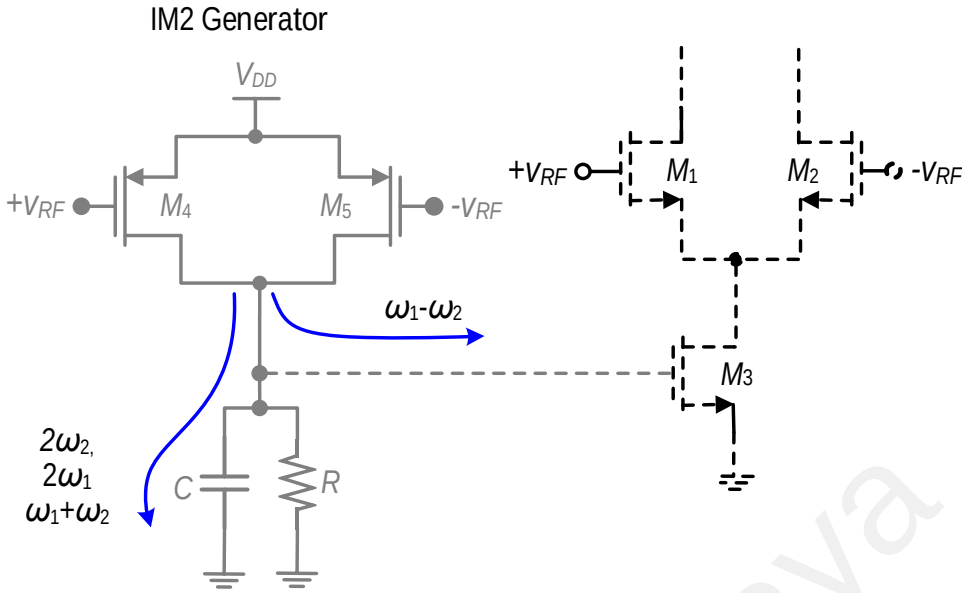


Figure 2.13: Circuit implementation of IM2 injection technique (Lou & Luong, 2007; Mollaalipour & Miar-Naimi, 2013).

Based on Equation (2.21), both the 2nd- and 3rd-order distortions can be partially cancelled out by biasing both the main and auxiliary transistors to operate at saturation region with positive g_m''. The drawback is that the transistor M_2 affects both the gain (referring 1st term in 2.21) and linearity of the circuit, limiting the maximum achievable IIP3. On the other hand the power consumption is also increased as the auxiliary transistor are biased in saturation region for robust distortion cancellation.

2.6.5 IM2 Injection

Another approach to improve the circuit linearity is an IM2 injection technique (Lou & Luong, 2007; Mollaalipour & Miar-Naimi, 2013), shown in Figure 2.13. A simple squaring circuit composed of M_4, M_5 and load (R and C) is used to generate a low-frequency IM2 current at (ω_1-ω_2). This IM2 current is transformed to a voltage by resistor R which is subsequently injected into the transistor M_3. The injected low-frequency IM2 is multiplied by the fundamental signal that results in a new IM3 components to cancel

the IM3 signals arising from intrinsic 3rd-order distortion. The IM3 will be cancelled fully if the following condition is satisfied:

$$-\frac{2g_{m1}g''_{m1}}{4g'_{m1}}+\frac{3}{2}g'_{m1}=-2g_{m3}g'_{m4}R \tag{2.22}$$

It is observed that the injected IM2 signal must be in phase with the envelope of the RF input signal to avoid gain degradation. Noise from the IM2 injection technique can be neglected as the injected noise from the squaring circuit appears as a common-mode noise. The main drawback of this technique is that it only works in narrowband with small two-tone spacing.

2.7 Summarize

This chapter presented a comprehensive description of a LNA and down-conversion mixers. The active and passive mixers were also explained in Section 2.4. In CMOS technology, it is often the case, where various parameters are in trade-off against each other by using different architectures and techniques. Each architectures and techniques inherits their own advantage at the cost of adversely effecting other performance parameter. Prior to the introduction of the proposed front-end circuit architecture, this chapter focuses on understanding the trade-offs encountered in various linearity techniques. It would facilitate the process of innovating a proper architecture and technique to a wireless application.

CHAPTER 3: DIFFERENTIAL-FOLDED MIXER WITH COMMON-GATE TRANSCONDUCTOR USING MULTIPLE-FEEDBACK

In this chapter, Section 3.1 describes the existing technique in improving linearity of active mixer for wideband- and narrow-bands application. In section 3.2, both the positive and negative feedback circuits in common-gate topology are analysed. Section 3.2 presents and analyses in detail the proposed mixer. Section 3.3 summarizes the simulated and the measured results comparing them to the state-of-the-art mixer topologies, followed by the conclusions in Section 3.4.

3.1 Introduction

To provide better performances with low power consumption, the active mixers currently integrating several LNA transconductor topology into the transconductance stage of the mixer as the transconductance stage will define the linearity when the switching stage is assumed to be ideal. In (Ho & Saavedra, 2010), a noise-cancelling approach from (Bruccoleri, Klumperink, & Nauta, 2004) was adopted to achieve broadband input impedance matching and low NF simultaneously. The circuits in (Bae et al., 2013) and (Guo, Wang, & Yang, 2014) adopts a resistive-feedback noise-cancelling transconductor to enable wideband operation with low NF and high linearity.

Recently, several narrowband high-linearity active-mixer topologies based on IM2 injection (Lou, 2008) have been reported (Asghari & Yavari, 2014, 2016; Mollaalipour & Miar-Naimi, 2016), achieving an IIP3 beyond +9 dBm and consuming between 4 to 5.8 mW of power. However, this IM2 injection adopts an extra squaring circuit, which causes phase shift in the generated IM2 signals and deteriorates the IIP3. Moreover, these works have been only verified through simulations extraction, without impedance-matching at the input-output terminals.

The CG transconductor is the most popular and simplest circuit in achieving wideband input impedance matching by using the transconductance of the input CG transistor to provide the real impedance to be $1/g_m$ (g_m≈20 mS) to match the 50 Ω input impedance. Also, it offers a good linearity, stability and reverse isolation due to the absence of the Miller effect due to C_{gd}. However, the gain and noise performance of the CG transconductor was limited by the transconductance value to satisfy the input matching condition. The introduction of a feedback loop around the differential CG transductors adds a degree of freedom to the design. A positive feedback technique (Liscidini et al., 2006) and dual negative feedback technique (Han et al. 2015) are used separately for transconductor linearization. In this work, both these techniques are used concurrently to create an effective linearization transconductor topology while adding more flexibility in design without compromising interdependent performance metrics. The proposed differential transconductor stage is merged into folded-type mixer, which helps in validating the concept successfully. It also includes a *LC*-folded configuration at the output of the transconductance stage to maintain a high drain-to-source voltage in the input transistors, while attenuating the low frequency IM2 signal to improve the linearity of the mixer.

In next section, the principle and trade-offs of the different positive- and negative-feedbacks topologies are presented first, followed by the description of the proposed circuit topology of the transconductor in folded mixer circuit.

3.2 Literature Review

In (Zhuo et al., 2005), the negative feedback scheme with the cross-coupled capacitors, C_{fb1} as shown in Figure 3.1(a) is used to boost the effective transconductance to become $g_{m1}(1+A_{CF})$ with input impedance matching of $1/g_{m1}(1+A_{CF})$, where $A_{CF}=(C_{fb1}-C_{gs1})/(C_{fb1}+C_{gs1})$. For $C_{fb1}>>C_{gs1}$, the A_{CF} is approximated to be unity. Thus, the g_m value

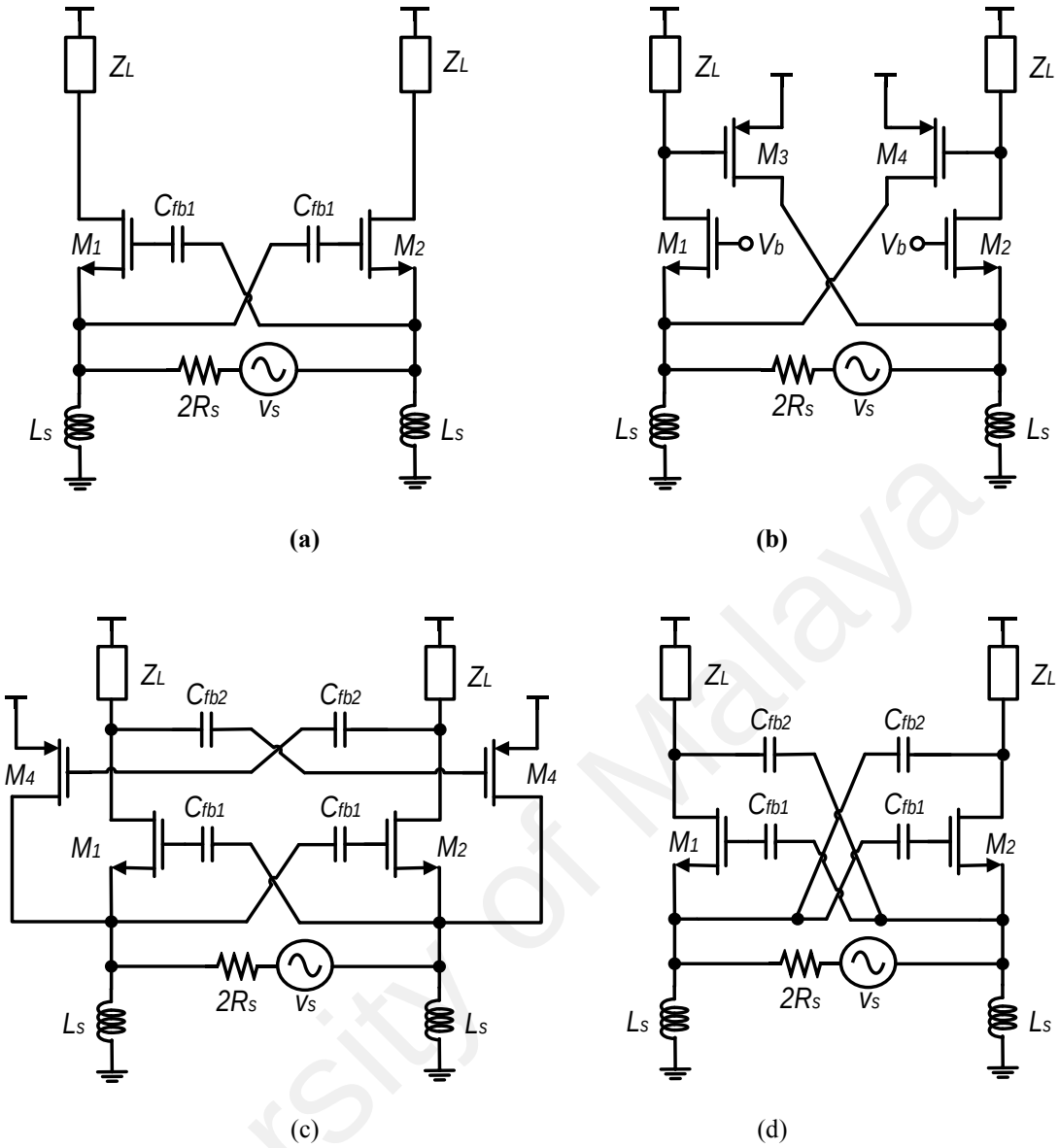


Figure 3.1: Differential CG amplifier with (a) CCC negative feedback (Zhuo, 2005), (b) positive feedback (PF) (Liscidini, 2006), (c) positive-negative feedback (PF-NF) (Woo, 2012), and (d) DCCC negative feedbacks (Han, 2015)

is halved (~10 mS) compared to the CG topology at the input matching condition, which mean the power consumption and size of transistor are also effectively reduced. As a result, the channel noise contribution from input transistor $M_{1,2}$ to noise figure is reduced at the same factor $(1+A_{CF})$ with concomitant decrease in power consumption. At the same time, it also inherently helps in reducing the second-order distortion in RF path. However, the linearity of CCC CG amplifier is still restricted by the input matching constraint.

A positive feedback (Liscidini et al., 2006) is proposed as shown in Figure 3.1(b) to eliminate correlation between the input impedance and transconductance of the CG LNA. The positive feedback path in CG LNA increases the input impedance to $1/g_m(1\text{-}A_{PF})$. A_{PF} $=g_{m3,4}Z_L$ is the positive feedback gain, where it can be varied from 0 to 1 for stable operation. In this way, $g_{m1,2}$ can be higher than 20 mS by increasing the A_{PF}. However, this type of CG topology improves gain and NF at the penalty of high-power dissipation. Therefore, by combining CCC negative feedback into the positive-feedback CG amplifier as shown in Figure 3.1(c), both the gain and noise enhancement can be achieved by using half of the g_m value compared to the positive feedback topology while maintaining the input matching (Woo et al., 20120).

Figure 3.1(d) shows the DCCC amplifier where it uses an additional capacitive feedback loops to the main CCC transconductor by connecting the drain node of each transistor to the other source in order to increase the loop gain for the IIP3 improvement with the reduced second-order signal in CCC topology (Han et al., 2015). The total loop gain of dual feedback including the source resistance R_s effect can be expressed as

$$G_L = g_{m1}(1+A_{CF})Z_T(\omega)\left(1+\frac{j\omega C_{fb2}Z_L}{1+j\omega C_{fb2}Z_L}\right) \tag{3.1}$$

From (3.2) it appears that the first CCC structure inherently improves the linearity by boosting the loop gain by two. The second capacitive-feedback further improves the linearity with a loop gain of $[j\omega C_{fb2}Z_L/(1+j\omega C_{fb2}Z_L)]$. However, since second feedback reported in (Han et al., 2015) needs direct voltage-to-current feedback loop between drain and source nodes in common-gate transistor, thus it creates correlation between input impedance and gain of the input transistor to the feedback capacitance, C_{fb2} and load, Z_L resulting a limitation in the linearity optimization of the circuit. Moreover, that passive capacitive-feedback requires a large loop gain to linearize the non-linearities of main circuit compared to the active feedback (Amirabadi et al., 2011). Therefore, large load

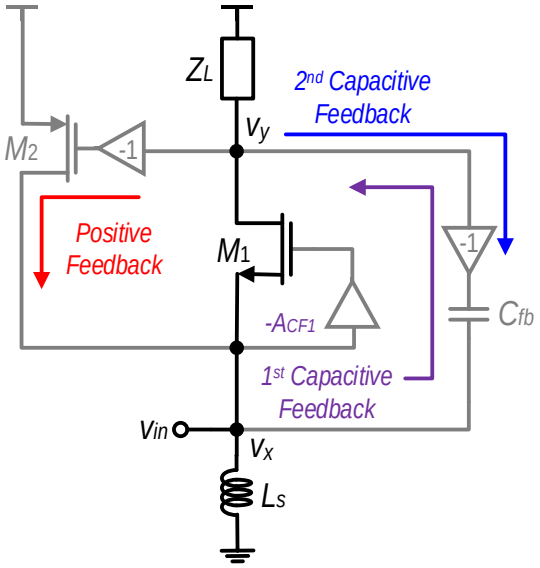


Figure 3.2: Schematic diagram of the proposed multiple-feedback transconductor

impedances are used as off-chip components while varying C_{fb2} value to provide the required loop gain with minimum tradeoff gain and input matching. But these bulky inductor loads are not viable to apply as an on-chip integration due to its low Q factor and large area consumption. Besides, it will add noise and degrade the linearity of the circuit.

In this work, another positive feedback loop for the DCCC transconductor is proposed to create an effective linearization, while creating additional design flexibility without compromising the interdependent performance metrics. Figure 3.2 illustrates the single-ended model of our transconductance stage. Due to the nature of the CCC configuration, the first capacitive feedback structure improves the NF and reduces the 2nd-order harmonic of the transconductor with low power consumption. The proposed positive feedback in conjunction with the 2nd capacitive feedback cancels the IM3 distortion while adding a new degree of freedom in the selection of the operating region of the input transistors while retaining the noise and G_c performances of the transconductance stage. Furthermore, the positive feedback scheme introduced into the DCCC CG transconductor also improves the input impedance matching, the NF and the G_c performances with a

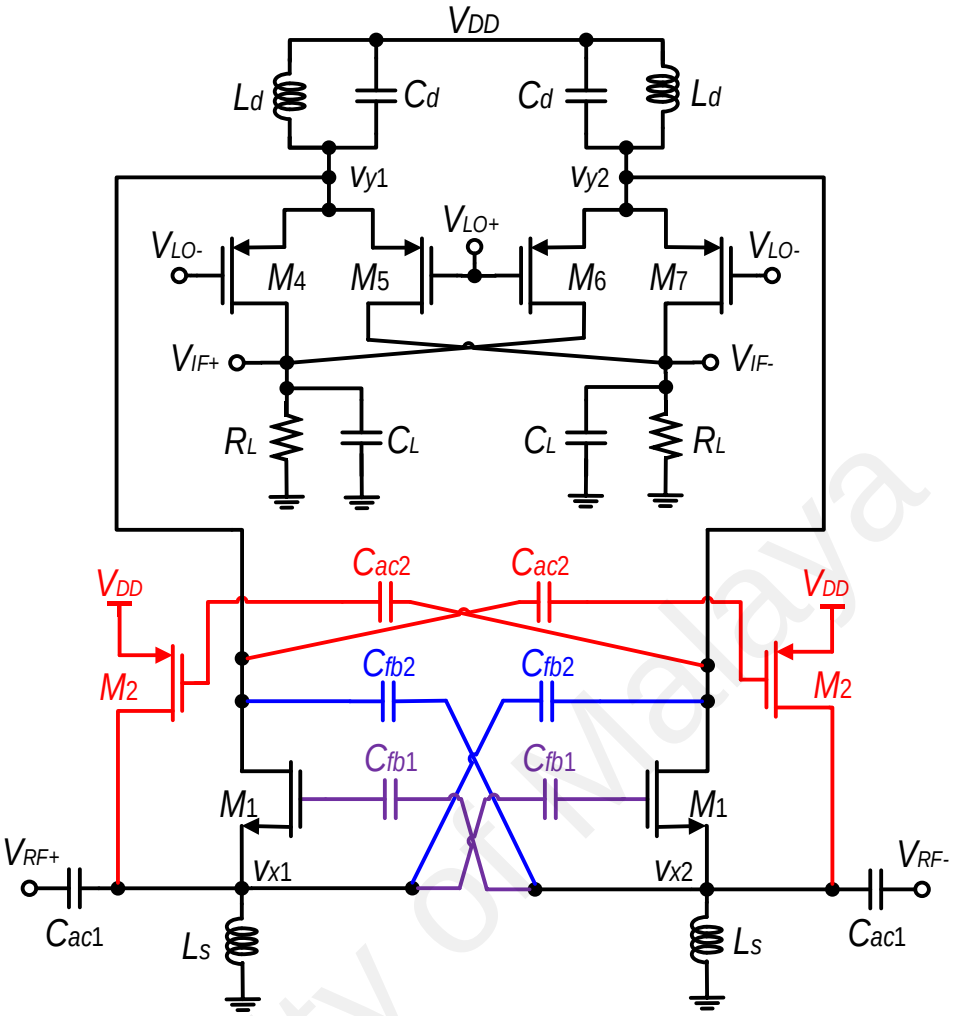


Figure 3.3: Schematic of the proposed multiple-feedback differential-folded mixer (bias circuit not shown)

flexible design criterion. The proposed differential transconductor stage is merged into a folded-mixer successfully validating the concept. A *LC*-folded configuration also is adopted at the output of the transconductance stage to maintain a high drain-to-source voltage in the input transistors, while attenuating the low frequency IM2 signal to improve the linearity of the mixer.

3.3 Proposed Mixer Based on Multiple-Feedback Transconductor

Figure 3.3 shows the full schematic of the proposed mixer which implements the multiple feedback concept. The transistors M_1-M_2 are the main transistors, whereas

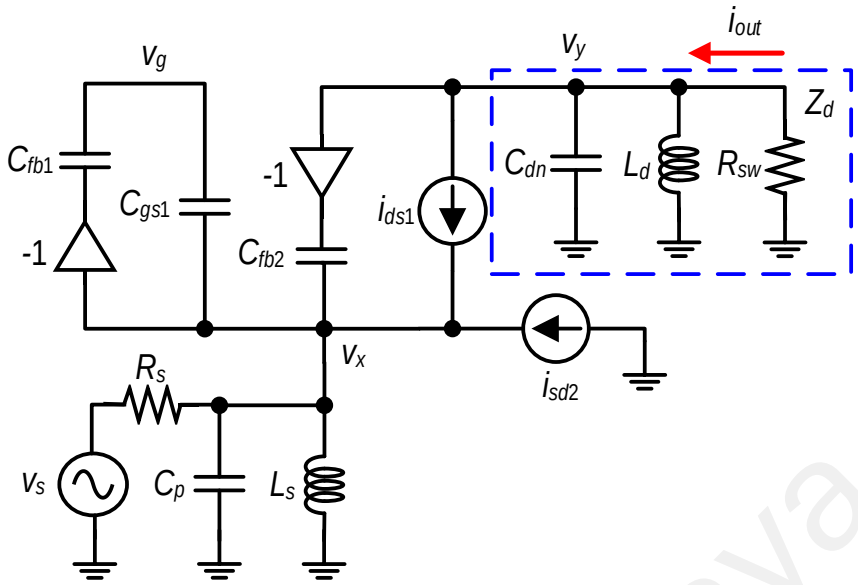


Figure 3.4: Small-signal equivalent half circuit of the proposed transconductance stage

transistors M_4-M_7 form the pMOS-based LO switching quad, and also construct a current-steering structure raising the design flexibility. The source of M_1 at one branch is cross-connected with the gate of M_1 at another branch through the capacitor C_{fb1}. The boosted CG transconductor effectively reduces the 2nd-order distortion in the signal path due to the nature of the cross-coupling scheme, while doubling the transconductance g_{m1}. The cross-coupled capacitor C_{fb2} creates another passive feedback path other than the one created by C_{fb1}. The third feedback utilizes transistor M_2 which creates a current feedback to enhance the gain, the NF and the input impedance matching with an aid in the freedom of selection of the g_{m1}. With the positive and 2nd capacitive feedback, the linearity is able to improve with the 3rd-order intermodulation signal suppression.

3.3.1 Input matching and effective transconductance

Figure 3.4 shows the equivalent half-circuit small-signal model of the proposed transconductance stage for the quantitative analysis. C_p is the total parasitic capacitance associated at the input pad, and at the source and the drain of M_1, and M_2. C_{dn} models the

capacitive load defining the parallel combination of the dynamic and parasitic capacitors at the output node. The impedance Z_d is defined by $R_{sw}||j\omega L_d||(1/j\omega C_{dn})$, where R_{sw} is the output resistance of the switching transistors. $v_{x1,2}$ and $v_{y1,2}$ are the source and gate voltages of M_1, respectively. By setting $g_{m1}(1+A_{CF1})>>j\omega C_{fb2}$, the input impedance becomes,

$$Z_{in}(j\omega)=\frac{1}{g_{m1}\left(1+A_{CF1}\right)\left(1+\dfrac{(j\omega C_{fb2}-g_{m2})Z_d}{1+j\omega C_{fb2}Z_d}\right)}\left\|\frac{1}{j\omega C_x}\right\| j\omega L_s \tag{3.2}$$

where $C_x=C_p+C_{fb2}$ and $A_{CF1}=(C_{fb1}-C_{gs1})/(C_{fb1}+C_{gs1})$. C_{gs1} is the gate-source capacitance of M_1. For $C_{fb1}>>C_{gs1}$, $A_{CF1}\approx 1$. In practice, the value of L_s is selected to resonate with the capacitance C_x at the operating frequency, thus, the first term in (3.2) plays a key role in the input impedance matching. Complementing the condition for input-impedance matching yields,

$$g_{m1}=\frac{1}{2R_s(1-g_{m2}R_{sw})} \tag{3.3}$$

$$L_d=\frac{1}{\omega_o^2\left[C_{dn}+C_{fb2}+(C_{fb2}/g_{m2}R_{sw})\right]} \tag{3.4}$$

where R_s is the terminating source resistance. When $g_{m2}=0$, g_{m1} is constrained by the matching condition, and the inductance L_d is significantly dependent on the capacitances C_{fb2} and C_{dn}. With the additional term $g_{m2}R_{sw}$ due to the positive feedback, the input impedance can be varied, which also offers a degree of freedom in the selection of the values of C_{fb2} and L_d to set the reactance of the input impedance to zero. Comparatively, the required load inductance L_d is reduced to the value of the load inductance in the DCCC circuit. Thus, this allows the integration of L_d on-chip which reduces the silicon area.

It appears that the input impedance matching condition imposes two boundaries on the feedback loops as follows: 1) $(j\omega C_{fb2}\text{-}g_{m2})(1/j\omega C_{fb2} \| Z_d)<1$ $|(j\omega C_{fb2}\text{-}g_{m2})(Z_d \| 1/j\omega C_{fb2})|<1$ which appears due to the input stability condition from (3.2); and 2) $g_{m2}R_{sw}<1$ which is due to the finite input transconductance from (3.3).

At matching condition, the effective transconductance G_m ($=i_{out}/v_s$) of the proposed multiple-feedback transconductor will be,

$$|G_m(\omega_o)| \approx \frac{g_{m1}}{\sqrt{1+\beta^2}} = \frac{1}{2R_s(1-g_{m2}R_{sw})} \cdot \frac{1}{\sqrt{1+\beta^2}} \tag{3.5}$$

where β denotes the ratio of $\omega_o C_{fb2}$ to g_{m2}, with β and g_{m1} directly related to the G_m of the transconductance stage. Thus, G_m is limited in the conventional DCCC architecture due the restricted g_{m1} in achieving input impedance matching, as well as the selection of C_{fb2} in providing a high loop gain for good linearity. In the presence of positive feedback, g_{m1} can be increased to a higher value than that of the DCCC topology to reach a high G_m regardless of the input impedance matching.

The overall conversion gain, G_c is,

$$G_c(\omega_o) \approx \frac{2}{\pi} g_{m1} R_L \left(1/\sqrt{1+\beta^2}\right) \tag{3.6}$$

at the frequency of interest.

3.3.2 Stability

The multiple feedback in the CCC transconductor imposes a circuit stability analysis. This is often evaluated by a return ratio (*RR*) approach defined as the difference ratio of the output currents transconductor with and without the feedback (Liscidini et al., 2008). Assuming $2g_{m1} >> j\omega C_{fb2}$, the *RR* for the proposed transconductor will be,

$$RR = \frac{2g_{m1}R_s}{1+2g_{m1}R_s}\left(j\omega C_{fb2} - g_{m2}\right)\left(Z_d \| \frac{1}{j\omega C_{fb2}}\right). \quad (3.7)$$

The 2nd capacitive feedback and active feedbacks can work as a single negative or positive, depending on the selection of the feedback gain loop. This design is tuned to have a positive feedback by setting the resultant ($j\omega C_{fb2}$-g_{m2})[(1/$j\omega C_{fb2}$)||Z_d] lower than 0. The stability condition of 0<RR<-1 can be guaranteed with a proper choice of the *LC* tank while meeting the input matched condition (3.2).

3.3.3 Noise Analysis

Under the input matching condition, the noise factor (*F*) of a single transconductance stage derived at ω_o is,

$$F = 1 + \frac{\gamma}{\alpha}\frac{1 - g_{m2}R_{sw}}{1 + A_{CF1}} + \frac{\gamma}{\alpha}g_{m2}R_s \quad (3.8)$$

where α is the ratio of the device transconductance to zero-bias the drain-to-source conductance and γ is the coefficient of the gate noise. The second term represents the channel-noise contribution of M_1, reduced through A_{CF1} and the positive feedback. The third term shows noise induced by M_2 and it is decreased by using a small g_{m2}. Then, evidently, the NF of the proposed transconductor is smaller than that of a typical DCCC transconductor.

3.3.4 Linearity

The transconductance stage will dominate the linearity in a down-conversion mixer if the switching stage is ideal. The simplified equivalent circuit of Figure 3.4 is used to calculate the IIP3 of the proposed transconductance stage. The C_{gs1} value is approximated to a value much smaller than C_{fb1} in order that the 2nd-order signal at v_{x1} has the same

magnitude and phase of the 2nd-order signal at the gate node of M_1 at another branch (Figure 4.2). Similarly, for the 2nd-order signal at the v_{x2} and v_{g1} nodes, the 2nd-order nonlinear transconductance of M_1 will be zero, $g'_{m1}v^2_{gs1} \cong 0$ (Han, Jung, & Kim, 2015). Hence, the nonlinear drain current of M_1 and M_2 can be modeled by the 3rd-order Taylor series expansion as,

$$i_{ds1} \approx -g_{m1}(1+A_{CF1})v_x - g''_{m1}(1+A_{CF1})^3 v_x^3 + ... \tag{3.9}$$

$$i_{ds2} = -g_{m2}v_y - g'_{m2}v_y^2 - g''_{m2}v_y^3 + ... \tag{3.10}$$

where v_{gs} and v_{ds} are gate-source and drain-source voltages, respectively. From (3.9), the fundamental signal is amplified by the factor of $(1+A_{CF1})$ due to the g_m-boosting feature of the CCC topology, and the 2nd-order nonlinearity is reduced to zero, so that the 2nd-order harmonic feedback effect to the IIP3 can be eliminated. Yet, the 3rd-order transconductance increases by a factor of $(1+A_{CF1})^3$ when compared with the conventional CG transconductor despite the reduction in the 2nd-order distortion. The 3rd-order nonlinear signal defines the IM3 distortion at low signal levels, and, thus, determines the IIP3 of the overall circuit. Therefore, it is outmost essential to minimize the 3rd-order nonlinearity in the output current signal to raise the IIP3 significantly. The relaxed 2nd-order nonlinear contribution to IIP3 in CCC topology will ease the cancellation process of 3rd-order distortions.

To cancel the 3rd-order distortion of the CCC transconductor implies the utilization of additional positive and 2nd capacitive feedbacks in the CCC topology. With these additional feedbacks in the CCC transconductor, another IM3 component will appear at the drain current in addition with the generated IM3 distortion signal. By a proper selection of the biasing, aspect ratio and capacitance C_{fb2} of the transistor M_2, an equal in magnitude and opposite in phase IM3 component appears with that in the main path at

the output current of the transconductor, resulting in the total IM3 component to be smaller. In order to perform the nonlinear cancellation, the 3rd-order coefficient, g_m'' of the transistors M_1 and M_2 must be opposite in phase to each other. With the inclusion of the 2nd capacitive feedback, the operating region of the transistors M_1 and M_2 can be interchanged without degrading the other performances such as G_c, NF, and at the expense of minimal additional power. This will be explained in details in the following description.

To theoretically verify the cancellation mechanism of the proposed technique, the equivalent small-signal circuit of the proposed transconductor as shown in Figure 3.4 is analyzed using Volterra series. For weakly nonlinear operation, the output current of the transconductance stage can be presented as a function of the input voltage v_s by using Volterra series as

$$i_{out} = G_1(\omega) \circ v_s + G_2(\omega_1, \omega_2) \circ v_s^2 + G_3(\omega_1, \omega_2, \omega_3) \circ v_s^3 \tag{3.11}$$

where "$\circ$" represents the Volterra kernel operator, ω's denotes the dependent frequencies, G_1, G_2, and G_3 model the 1st-, 2nd- and 3rd-order transconductance of the proposed transconductor, respectively.

With a lengthy derivation, reported in Appendix B, an expression for the Volterra kernels G_n that describe the nonlinearity of the proposed transconductor is obtained as,

$$G_1(\omega) = -\frac{Z_d(\omega)}{R_s R_{sw}} \cdot \frac{g_{m1}\left(1 + A_{CF_1}(\omega)\right) - Y_{fb2}(\omega)}{V(\omega)} \tag{3.12}$$

$$G_2(\pm\omega_1, \mp\omega_2) = \frac{Z_d(\pm\omega_1 \mp \omega_2)}{R_{sw} V(\pm\omega_1 \mp \omega_2)} \times \left\{ \begin{array}{l} \left[g_{m1}\left(1 + A_{CF_1}(\pm\omega_1 \mp \omega_2)\right) - Y_{fb2}(\pm\omega_1 \mp \omega_2) \right] \\ \cdot g'_{m2} B_1(\pm\omega_1) B_1(\mp\omega_2) \end{array} \right\} \tag{3.13}$$

$$G_3(\pm\omega_1,\pm\omega_1,\mp\omega_2)$$

$$= -\frac{Z_d(\pm 2\omega_1 \mp \omega_2)}{R_{sw}V(\pm 2\omega_1 \mp \omega_2)} \times \left\{ \begin{array}{l} \left[\frac{1}{Z_T(\pm 2\omega_1 \mp \omega_2)} + Y_{fb2}(\pm 2\omega_1 \mp \omega_2)\right] \\ \cdot\left[g''_{m1}\left(1 + A_{CF_1}(\pm 2\omega_1 \mp \omega_2)\right)^3 A_1^2(\pm\omega_1)A_1(\mp\omega_2)\right] \\ +\left[g_{m1}\left(1 + A_{CF_1}(\pm 2\omega_1 \mp \omega_2)\right) - Y_{fb2}(\pm 2\omega_1 \mp \omega_2)\right] \\ \cdot\left[g''_{m2}B_1^2(\pm\omega_1)B_1(\mp\omega_2) + 2g'_{m2}\overline{B_1(\pm\omega_1)B_2(\pm\omega_1,\mp\omega_2)}\right] \end{array} \right\} \quad (3.14)$$

where $Z_T=R_s\|j\omega L_s\|(1/j\omega C_x)$. In (3.14), the 1st product term represents the nonlinearity of M_1, where the 3rd-order nonlinear coefficient g''_{m1} increases by $(1+A_{CF1})^3$ in the presence of the CCC topology. While M_2 causes the additional 2nd and 3rd product terms. On the other hand, the 2nd-order interaction term in (3.14) will be,

$$\begin{aligned} \overline{B_1(\pm\omega_1)B_2(\pm\omega_1,\mp\omega_2)} &= \frac{1}{3}\left[2B_1(\pm\omega_1)B_2(\pm\omega_1,\mp\omega_2) + B_1(\pm\omega_2)B_2(\pm\omega_1,\mp\omega_1)\right] \\ &= \frac{1}{3}B_1^2(\pm\omega_1)B_1(\pm\omega_2)\times\left[2N(\pm\omega_1\mp\omega_2) + N(\pm 2\omega_1)\right] \end{aligned} \quad (3.15)$$

where

$$N(\omega) = Z_d(w)\cdot\frac{g_{m1}\left(1 + A_{CF1}(\omega)\right) - Y_{fb2}(\omega)}{V(\omega)}. \quad (3.16)$$

The term $(2g_{m1}\text{-}Y_{fb2})$ in the numerator of $N(\omega)$ represents the feedback that C_{fb2} introduces between the input and output of the transconductor circuit. With an additional RF current source, composed by the parallel inductor L_d and capacitor C_{dn}, it is possible to minimize the low frequency 2nd-order distortion by decreasing the value of Z_d at the $\Delta\omega$ frequencies. Besides, the 2nd-order nonlinear distortion still appears in the differential structure although with a negligible amount. Hence, $G_3(\pm\omega_1,\pm\omega_1,\mp\omega_2)$ in (3.14) can be approximated at the 3rd-order distortion frequency as,

$$G_3(\pm\omega_1 \pm \omega_1, \mp\omega_2)$$

$$= \frac{Z_d(\pm 2\omega_1 \mp \omega_2)}{R_{sw} V(\pm 2\omega_1 \mp \omega_2)} \times \left\{ \begin{array}{l} \left[\left[\frac{1}{Z_T(\pm 2\omega_1 \mp \omega_2)} + Y_{fb2}(\pm 2\omega_1 \mp \omega_2) \right] \right. \\ \times \left(1 + A_{CF_1}(\pm 2\omega_1 \mp \omega_2)\right)^3 g''_{m1} A_1^2(\pm\omega_1) A_1(\mp\omega_2) \\ + \left[g_{m1} \left(1 + A_{CF_1}(\pm 2\omega_1 \mp \omega_2)\right) - Y_{fb2}(\pm 2\omega_1 \mp \omega_2) \right] \\ \left. \times g''_{m2} B_1^2(\pm\omega_1) B_1(\mp\omega_2) \right\}. \end{array} \right. \quad (3.17)$$

In general, IIP3 can be described from (3.13) and (3.18) as,

$$IIP3(\pm\omega_1, \pm\omega_1, \mp\omega_2) = \frac{1}{6}\frac{1}{R_s}\left|\frac{G_1(\omega_1)}{G_3(\pm\omega_1, \pm\omega_1, \mp\omega_2)}\right|. \quad (3.18)$$

$G_1(\omega_1)$ is typically fixed by the design parameters, therefore the high IIP3 is achieved by reducing $G_3(\pm\omega_1, \pm\omega_1, \mp\omega_2)$. Referring to (4.17), if the 2nd-order distortion is completely eliminated, the IIP3 can be improved by minimizing the composite g''_m. As shown in

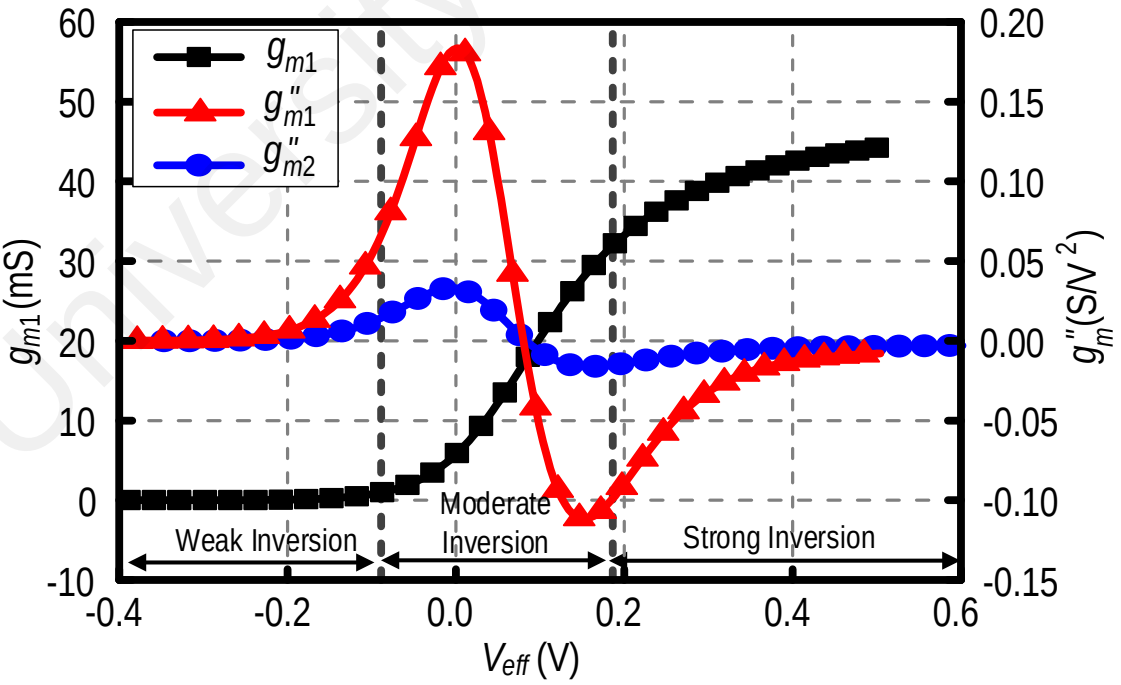


Figure 3.5: Simulated g''_m of NMOS and PMOS transistors as a function of the gate overdrive voltage V_{eff}. $(W/L)_{1\text{-}2}$ = 60/0.13 μm and $V_{ds1,2}$ = 1.0 V

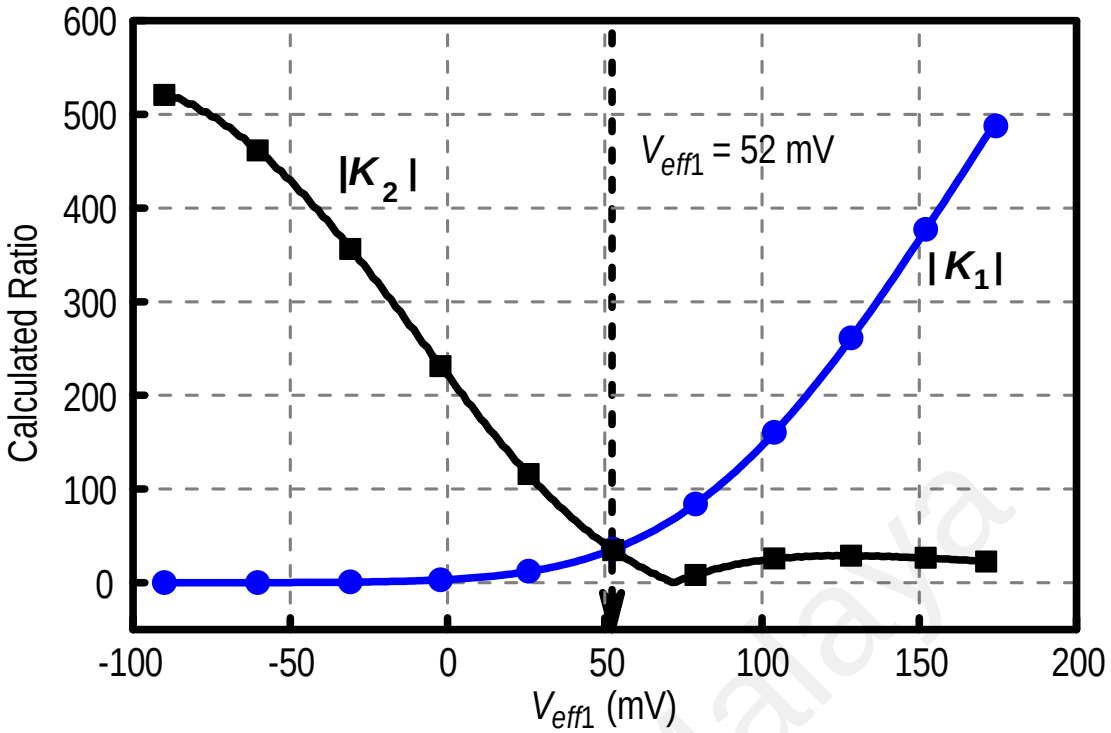
Figure 3.5, the sign of g''_m changes from positive to negative as the operating region changes from the weak inversion to the strong inversion, with the changing spot $V_{eff1,2}$ =80 mV as the reference point. In (3.18), can deduct from basic circuit theory that both A_1 and B_1 have the same signal. Therefore, by setting the coefficient transconductances of transistors M_1 and M_2, $g''_{m1,2}$ with opposite signal while varying the capacitor C_{fb2}, the IM3 distortion components can be reduced substantially.

To simplify the equation, A_{CF1} is attribute as an unity gain value. Thus, the equation (3.18) implies that the IM3 distortion can be cancelled if the following condition holds,

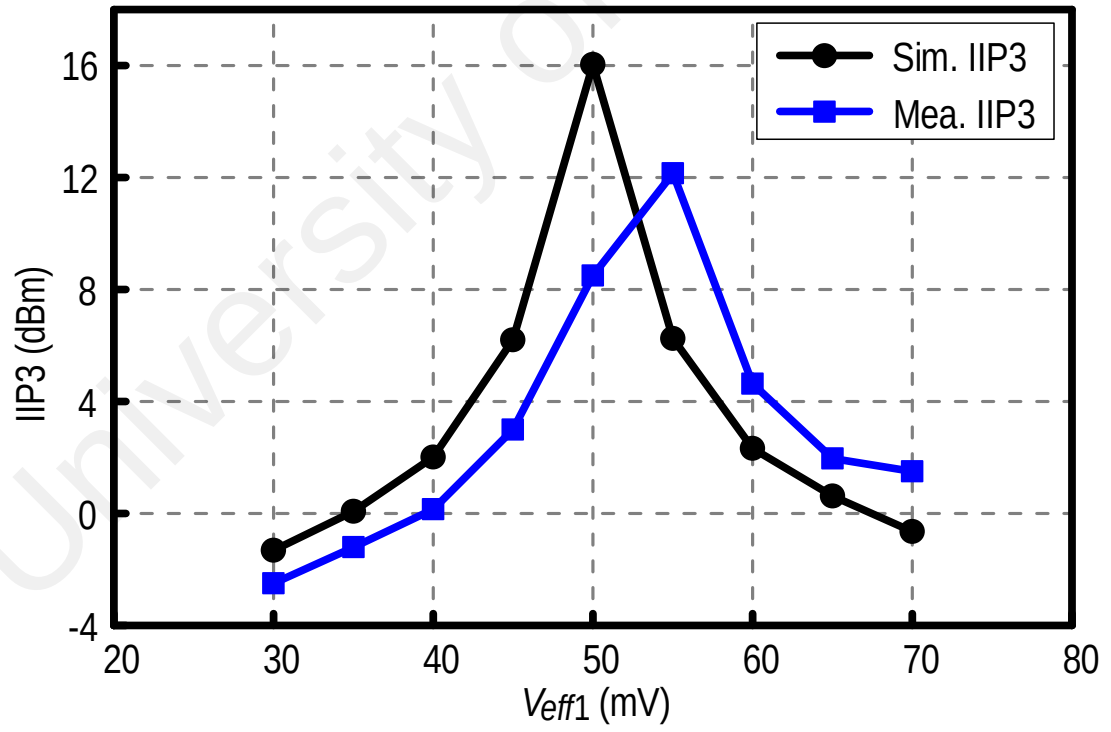
$$\frac{B_1^2(\pm\omega_1)B_1(\mp\omega_2)}{A_1^2(\pm\omega_1)A_1(\mp\omega_2)} = 8\frac{g''_{m1}}{g''_{m2}}\frac{\left(1/Z_T(\pm 2\omega_1 \mp \omega_2)\right)+Y_{fb2}(\pm 2\omega_1 \mp \omega_2)}{2g_{m1}-Y_{fb2}(\pm 2\omega_1 \mp \omega_2)}. \qquad (3.19)$$

The ratio between the drain and source voltages of the input CG needs to match with the ratio of the component in the right-hand side of Equation (3.19). As an initial step, both capacitors C_{fb2} and gate biasing of M_2 are fixed according to the input impedance matching and stability conditions leading to a negative value of g''_{m2}. Thus, the gate voltage of M_1 varies until the optimum gate overdrive voltage of M_1 is obtained. Figure 3.6(a) illustrates the plot used to find the optimum V_{eff1}, where the left and right terms in (3.19) are represented as K_1 and K_2, respectively. The maximum IM3 distortion cancellation should be obtained when the magnitude of $K_1 = K_2$. To validate this, the IIP3 simulation and measurement across V_{eff1} is performed as shown in Figure 3.6(b). The proposed mixer achieves an optimum IIP3 at the V_{eff1} of 50 and 55 mV, respectively, which is reasonably close to the theoretical value of 52 mV predicted by Figure 3.6(a).

An extensive set of simulations were carried out to determine how the IIP3 of the circuit varies at different operating regions of M_1 and M_2. Figure 3.7(a) and 3.7(b) illustrate the 3-D plot of the simulated IIP3 across the gate overdrive voltages of M_1 and M_2. The capacitor C_{fb2} is selected accordingly to provide the required magnitude in (3.20)

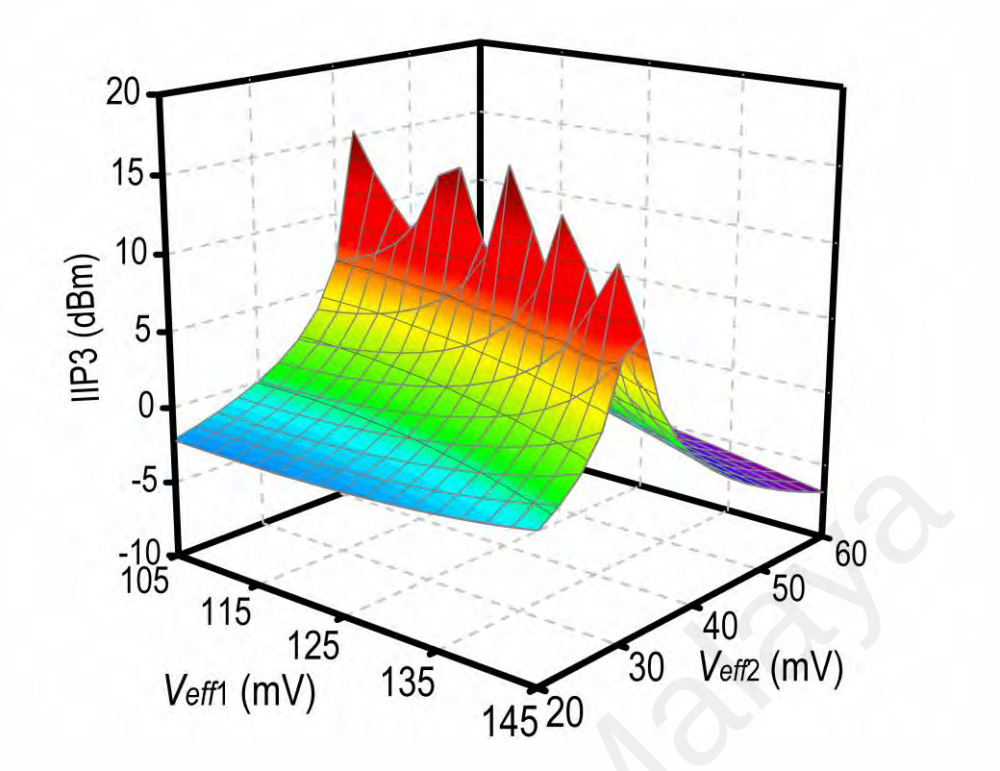


(a)

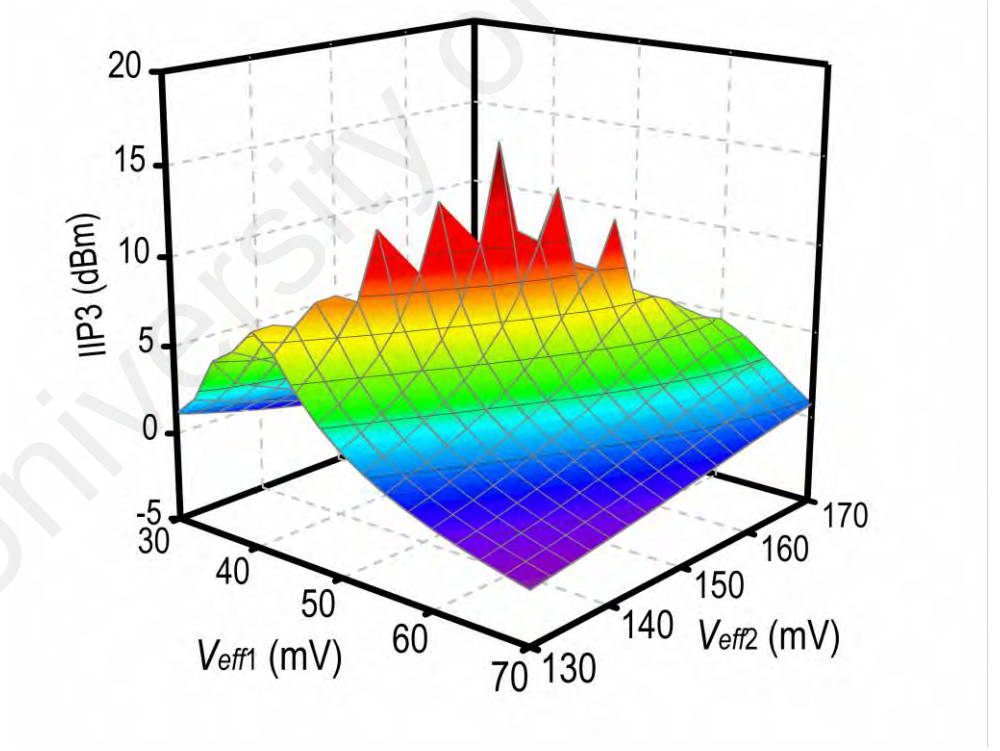


(b)

Figure 3.6: (a) Calculated ratio based on Eq. (25); (b) Simulated and measured IIP3 of the proposed mixer with W_1/L_1 = 125/0.13 μm, W_2/L_2 = 35/0.13 μm, C_{fb2} = 280 fF and V_{eff2}=150 mV



(a)



(b)

Figure 3.7: Simulated IIIP3 of the proposed mixer when setting (a) V_{eff1}>80 mV and V_{eff2}<80 mV with W_1/L_1 =60/0.13 μm, W_2/L_2 = 55/0.13 μm, C_{fb2} = 390 fF (Case 1) and (b) V_{eff1}<80 mV and V_{eff2}>80 mV with W_1/L_1 = 125/0.13 μm, W_2/L_2 = 35/0.13 μm, C_{fb2} = 280 fF (Case 2)

Table 3.1: Circuit Parameters of the Proposed Mixer

Parameter	$(W/L)_{4\text{-}7}$ (μm)	L_s (nH)	L_{d2} (nH)	Q_s	Q_d	C_d (fF)	C_{fb1} (pF)	R_L (Ω)	C_L (pF)
Value	75/0.13	10	17	8.2	9.8	185	8.5	550	1

Table 3.2: Mixer in Different Bias Regions

	V_{eff1} (mV)	V_{eff2} (mV)	g_{m1} (mS)	g_{m2} (mS)	C_{fb2} (fF)	W_1/W_2 (μm/μm)
Case 1	130	40	28	3.25	390	60/55
Case 2	50	150	28	4.9	280	125/35
	I_T (mA)	V_{DD} (V)	IIP3 (dBm)	G_c (dB)	NF (dB)	P1dB (dB)
Case 1	4.4	1.0	15.0	18.1	8.2	-15.6
Case 2	4.0	1.0	16.0	18.4	8.3	-15.8

to attenuate the 3rd-order kernel of the transconductance stage output current. The size of the transistors is also optimized to provide the necessary g_m. In both designs, the capacitance C_{fb1}, inductance L_s, RF choke (L_d and C_d), load (R_L and C_L) and switching transistors are set to be same, and their parameter values are listed in Table 3.1.

As shown in Figure 3.7, the high peaks of IIP3 are acquired for certain optimum bias point at which the complete distortion cancellation happens. For example, in case 1 for large V_{eff1} and low V_{eff2}, the high peak IIP3 value is achieved around V_{eff1}=130 mV and V_{eff2}=40 mV with C_{fb2}=390 fF as illustrated in Figure 3.7(a). In case 2, when M_2 is biased with a large V_{eff2} while reducing V_{eff1}, the optimal IIP3 is obtained at V_{eff1}=50 mV and V_{eff2}=150 mV with C_{fb2} =280 fF, as shown in Figure 4.6(b). Table 3.2 summarizes the device sizes and other performances at these selected points. For case 1, there is a tiny drop in G_c (~0.3 dB) due to β increment according to Equation (3.6). Besides, the NF is

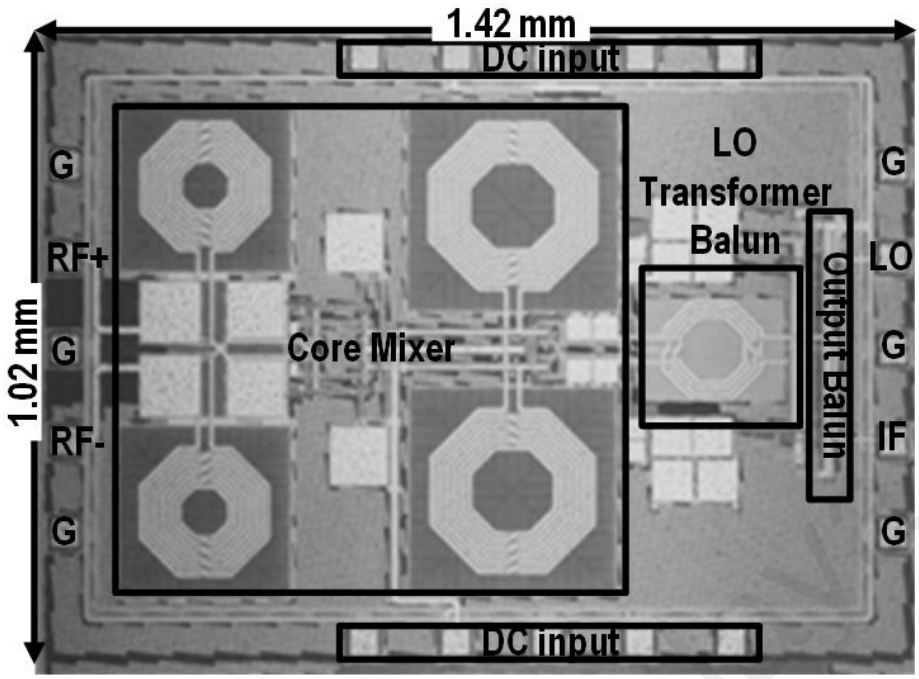


Figure 3.8: Die microphotograph.

almost identical in both cases as g_{m2} is in a tradeoff with noise. Further, the achieved IIP3 is basically the same while maintaining G_c, NF and P1dB performances. These characteristics implies that the design of the proposed transconductor allows the selection of the operating region in the input transistors through the choice of capacitance, C_{fb2} and the gate biasing of transistor, $M_{1,2}$.

Furthermore, the positive feedback in the DCCC transconductor provides higher linearity through the IM3 cancellation, which exhibits more flexibility in the simultaneous optimization of the input impedance matching, the conversion gain, and the NF instead of conquering the total gain through the conventional method in the DCCC circuit.

When the transistor operates in a moderate inversion region, the required fundamental transconductance value is obtained through the increase of its device size which in turn increases the parasitic capacitance effect, however with the inductors located at the source and drain of the transistor M_1, this effect can be nullified. However, the existence of the narrow band *LC* tank and the 2nd capacitive feedback will limit the operating bandwidth. Therefore, this technique is suitable for narrow band applications.

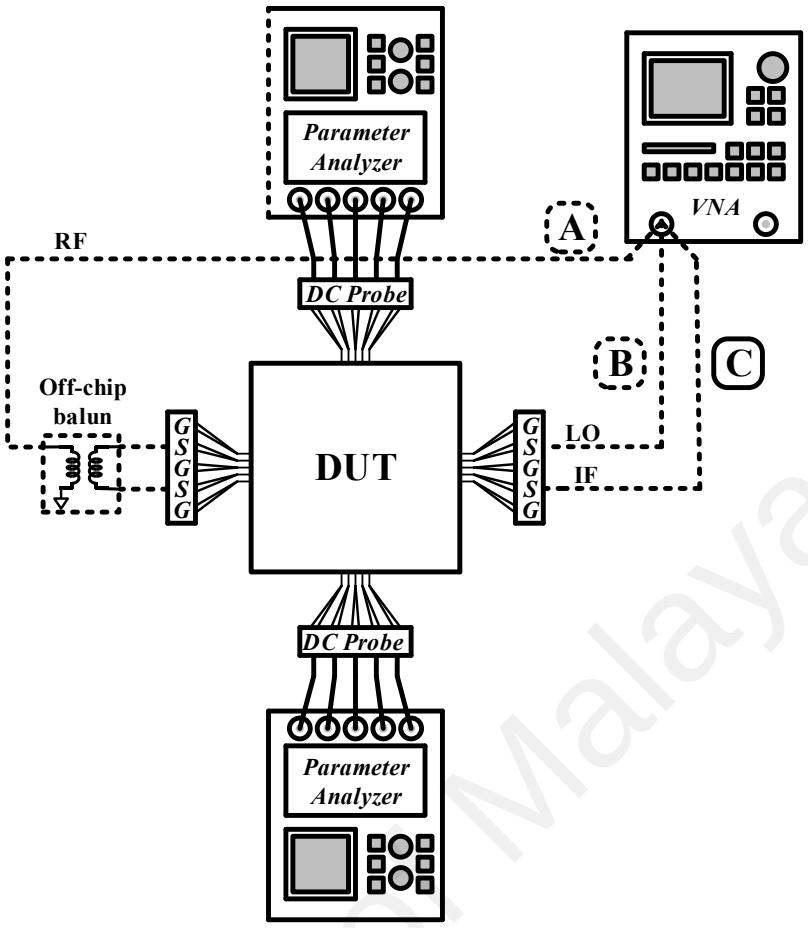


Figure 3.9: Test setup for input reflection coefficient measurement.

3.4 Simulation and Measurement Results

To characterize the performance on-chip wafer probing is utilized. The Cascade Microtech's RF probes based on Air Coplanar (ACP) family in GSGSG pattern are used to provide the RF, LO input signals and to receive the IF output signal. While, Cascade Microtech's DC probe based on DC Quadrant (DCQ) power probe series are used to provide the VDD and ground. The Short-Load-Thru calibration was conducted using the impedance standard substrate (ISS) to avoid the systematic errors. Different measurement configurations were performed to obtain various parameter readings of the proposed circuits. The measurement setup diagram and the obtained measurement and simulation results will be discussed as belows:

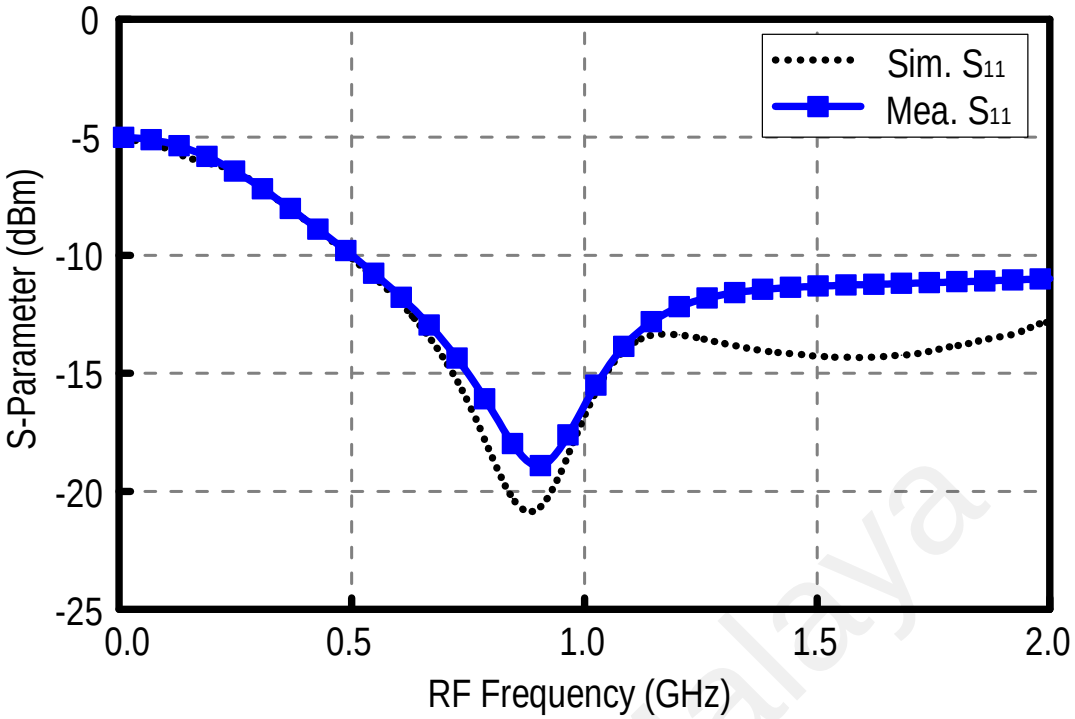


Figure 3.10: Measured and simulated S_{11}.

Figure 3.8 shows the die micrograph which occupies a die area of 1.42 x 1.02 mm^2 including the pads. An on-chip stacked 1:1 transformer-based balun also is used at the LO input to provide a differential LO input signal with 0 dBm of input power, whereas an on-chip active buffer is used at the IF output to realize the 50 Ω output impedance matching for measurement purposes. The measurement uses an external RF balun to convert the single-ended RF signal into a differential output. The measured power consumption excluding the IF buffer is 4 mW at a supply voltage of 1 V.

Figure 3.9 shows input reflection coefficient measurement setup by using Vector Network Analyzer (VNA). Before performing the measurement, the VNA was calibrated well together with the probe station, cables and off-chip RF input balun. Figure 3.10 shows the measured and simulated RF input reflection coefficient (S_{11}) of the proposed down-conversion mixer. The measured S_{11} for the RF input port is less than -15 dB at 900 MHz. This result indicates that the proposed differential input common-gate transistors has achieved a sufficient input matching to the 50 Ω termination at the desired operating

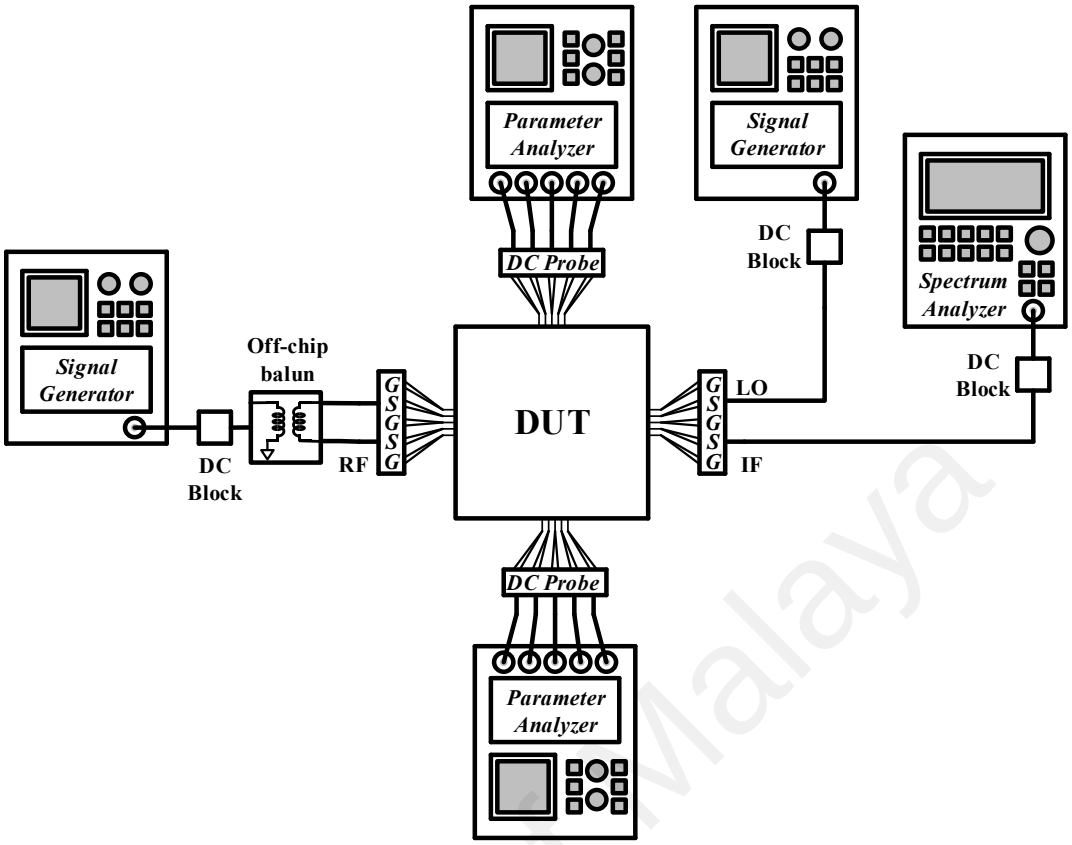


Figure 3.11: Test setup for conversion gain and IIP2 measurements.

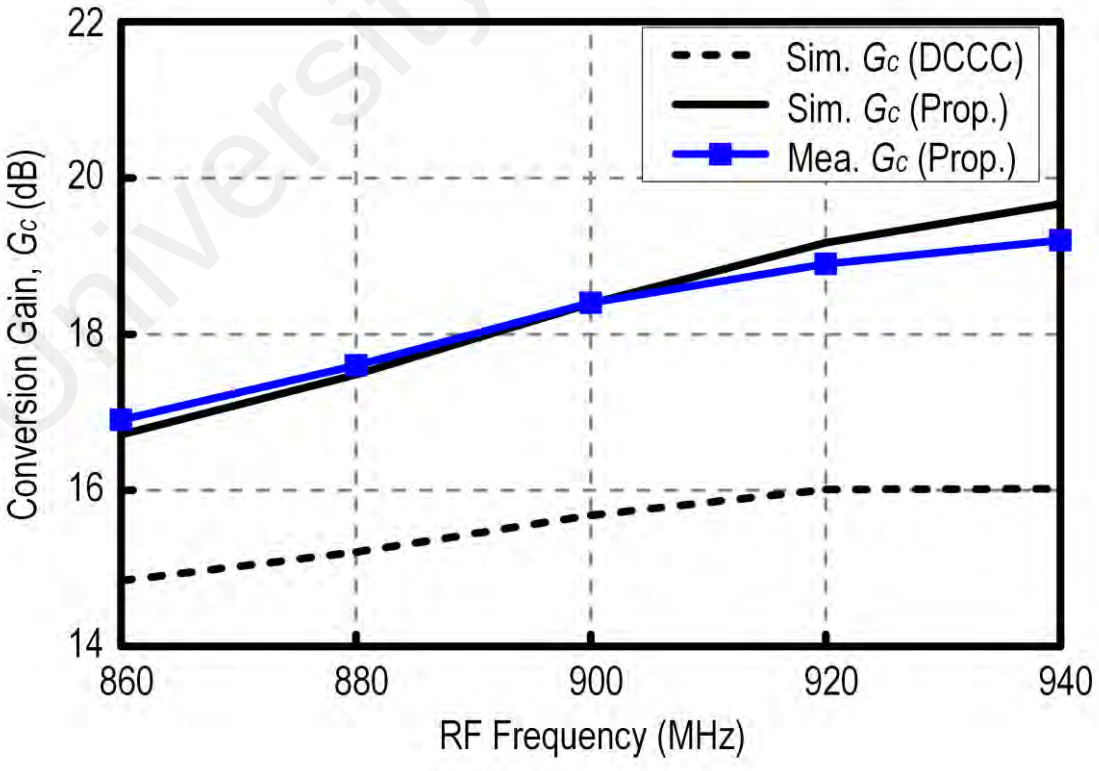


Figure 3.12: Measured and simulated conversion gain versus RF frequency.

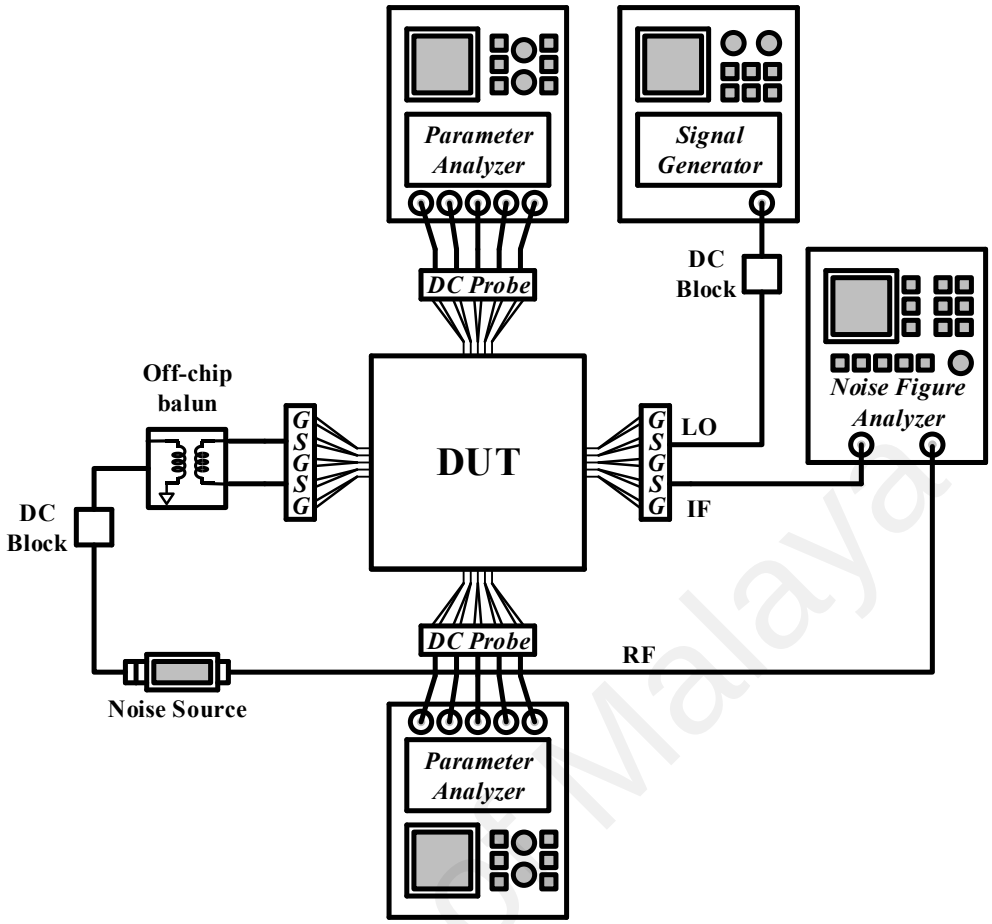


Figure 3.13: Test setup for noise figure measurement.

frequency in order to transfer a maximum signal into the DUT (device under test) circuit.

The existing reported DCCC architecture and the proposed circuits are designed and simulated to compare their performances, with the same transistor sizes and load impedances for a fair comparison. In DCCC, the capacitor C_{fb2} and the bias voltage of the input CG transistors are optimised to operate at 900 MHz. To perform conversion gain measurement, the following test setup was adopted as shown in Figure 3.11, where the RF and LO input signals were varied simultaneously with a fixed 50 MHz frequency different. Based on spectrum reading in spectrum analyser, the conversion gain is calculated. Figure 3.12 exhibits the measured and simulated conversion gain across the RF frequency of the proposed mixer and the conventional DCCC transconductance based

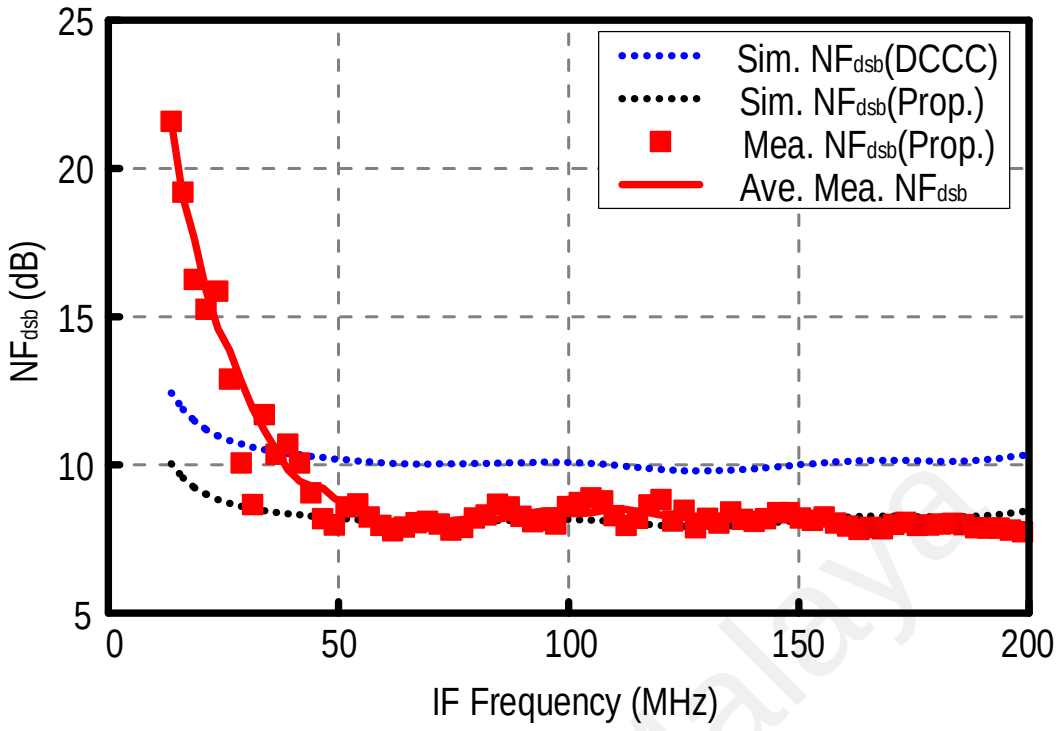


Figure 3.14: Measured and simulated DSB NF versus IF frequency.

mixer. The conversion gain is equal to 18.4 dB at 900 MHz of RF frequency, which has been improved by ~3dB with respect to the conventional DCCC mixer.

The noise figure measurement is conducted by using an Agilent Noise Figure Analyser (N8975A) with a noise source N4002A. An accurate calibration is done by connecting the noise source to the noise figure analyser through the "Thru" connection, thus later the noise contribution from cable and off-chip component such, balun and DC block can be de-embedded in NF reading. The Y-factor method has been used to characterise the noise of the prosed mixer. The noise figure test setup is shown in Figure 3.13. Figure 3.14 illustrates the measured and simulated NF_{DSB}. The simulated NF performance is better in the proposed mixer with a 2 dB improvement, indicating a measured NF_{DSB} of ~8.5 dB. The noise discrepancy between the measurement and simulation results at low frequency is mainly due to the starting operating frequency (10 MHz) of the noise analyser which is in the vicinity of the operating IF frequency (50 MHz).

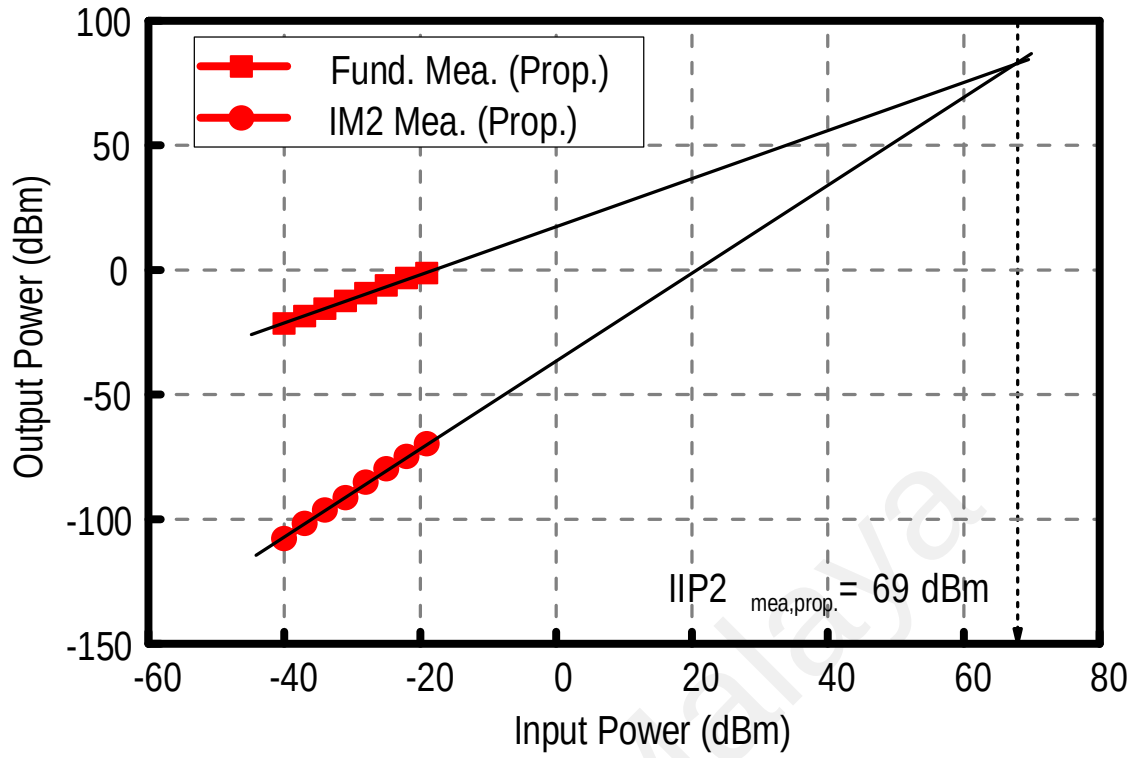


Figure 3.15: Measured IIP2 of the proposed mixer.

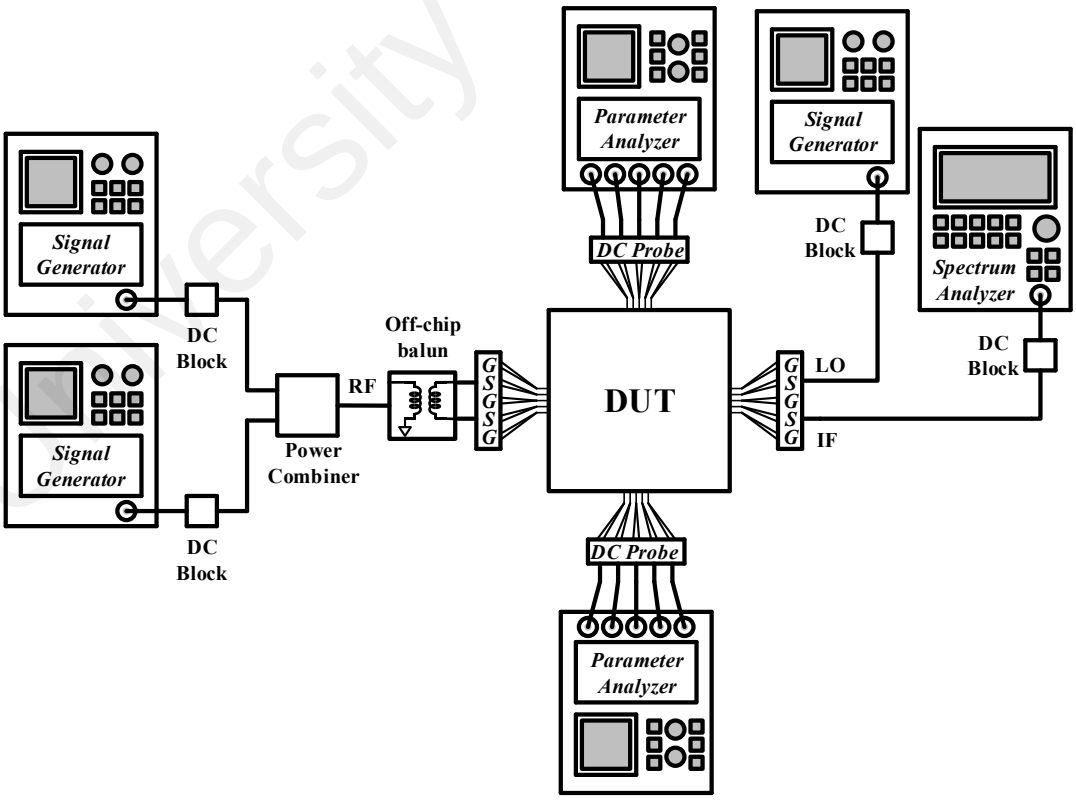


Figure 3.16: Test setup for IIP3 measurement.

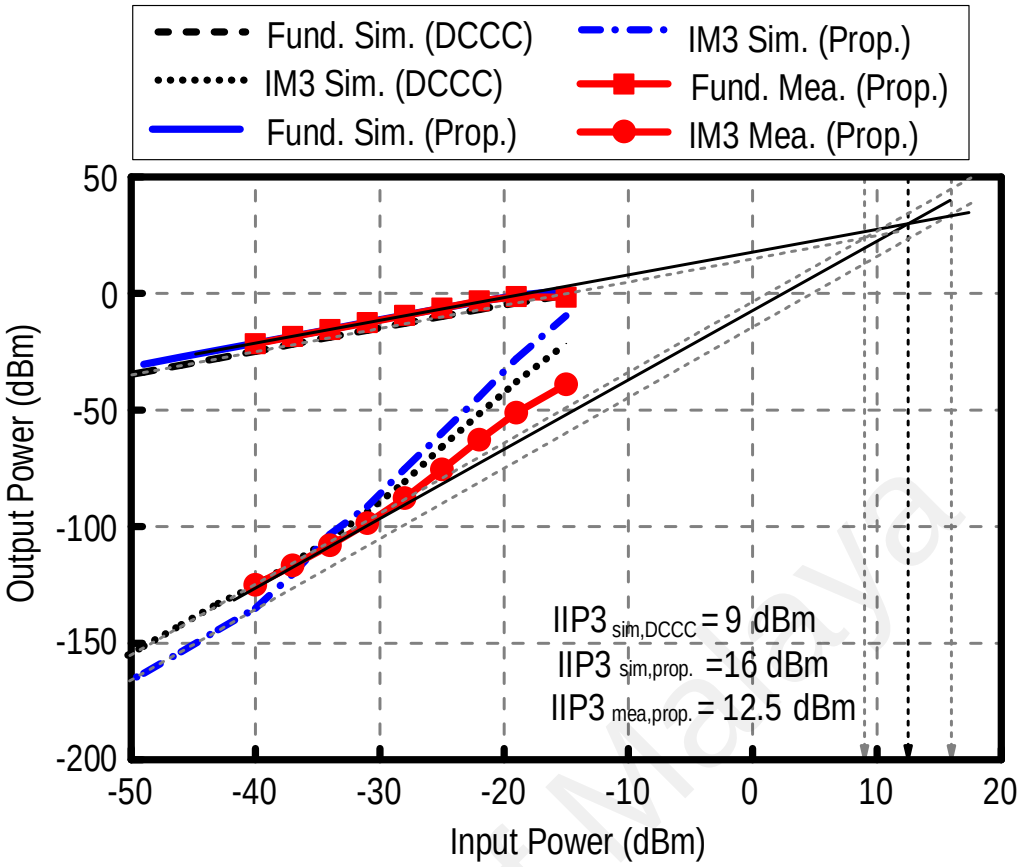


Figure 3.17: Measured and simulated IIP3 results.

The measured input-referred 2nd-order intercept point (IIP2) of the propose mixer result is shown in Figure 3.15, where it obtains 69 dBm of IIP2. For this IIP2 reading, the same setup that used for conversion gain measurement is used. The mixers IIP3 were obtained with a two-tone test, with the same amplitude and a frequency spacing of 1 MHz (900 and 901 MHz) RF signals. Figure 3.16 shows the test setup for IIP3 measurement, where power combiner is used to combine these both RF signals prior entering the DUT. Figure 3.17 shows the measured and simulated IIP3 of the mixers. The measured IIP3 is +12.5 dBm. This value also indicates that the proposed mixer has -18.0 dBm measured 1-dB input compression point (P1dB). As expected, the proposed architecture shows better performances than the DCCC based mixer. The discrepancy of the simulated and measure IIP3 point could be effected due to variation of the design parameters, also due to the constructive and destructive interference of several non-linearities.

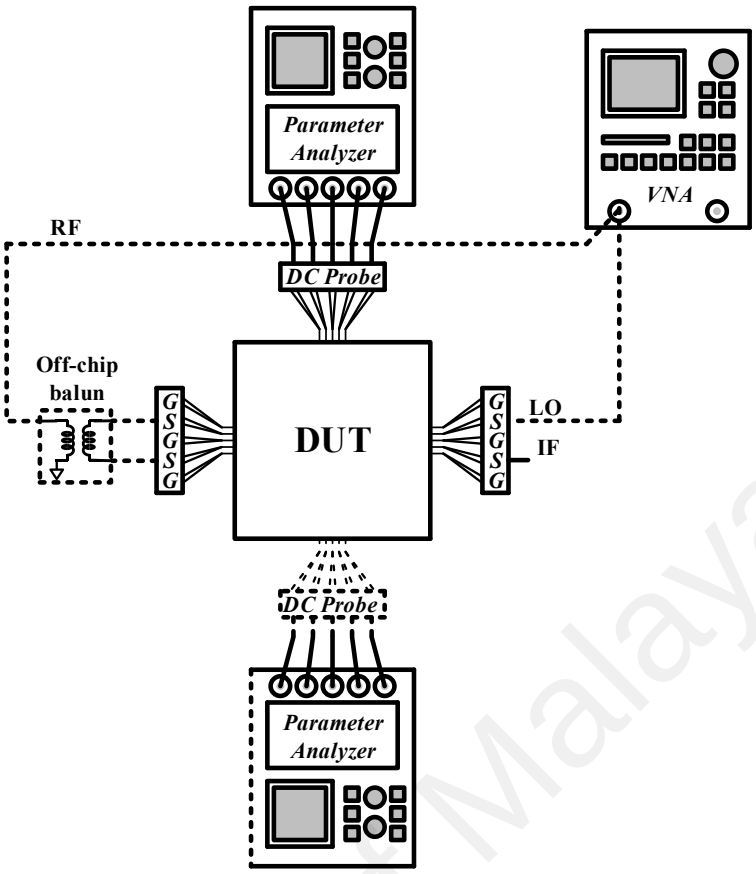


Figure 3.18: Test setup for isolation measurement.

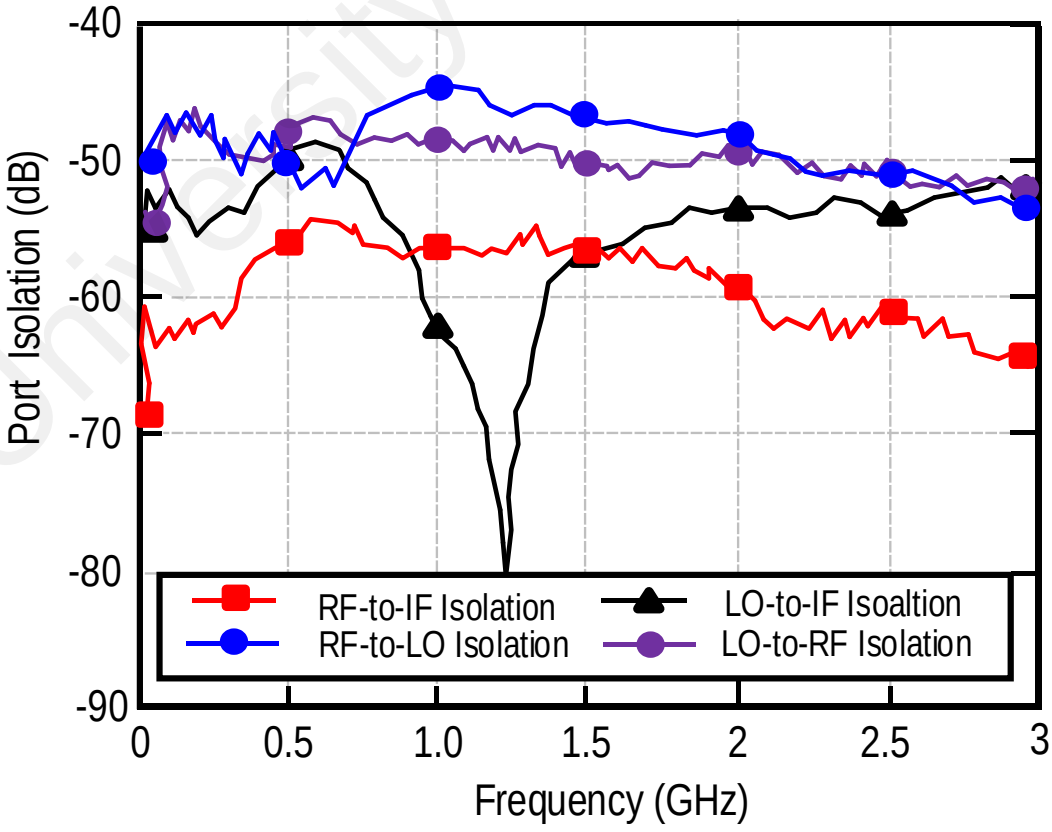


Figure 3.19: Measured port-to-port isolation

Table 3.3: Corner and Temperature Variations of the Proposed Circuit (Simulated)

Parameters	*IIP3* (dBm)	*P1dB* (dB)	G_c (dB)	*NF* (dB)	*Power* (mW)
FF@-40°C	13.5	-19.5	20.5	7.6	4.7
FF@85°C	14.5	-14.7	14.5	9.7	4.3
TT@27°C	16.0	-15.8	18.4	8.3	4.0
SS@85°C	15.2	-12.5	12.0	9.5	3.2
SS@-40°C	13.8	-16.1	21.3	7.1	3.5

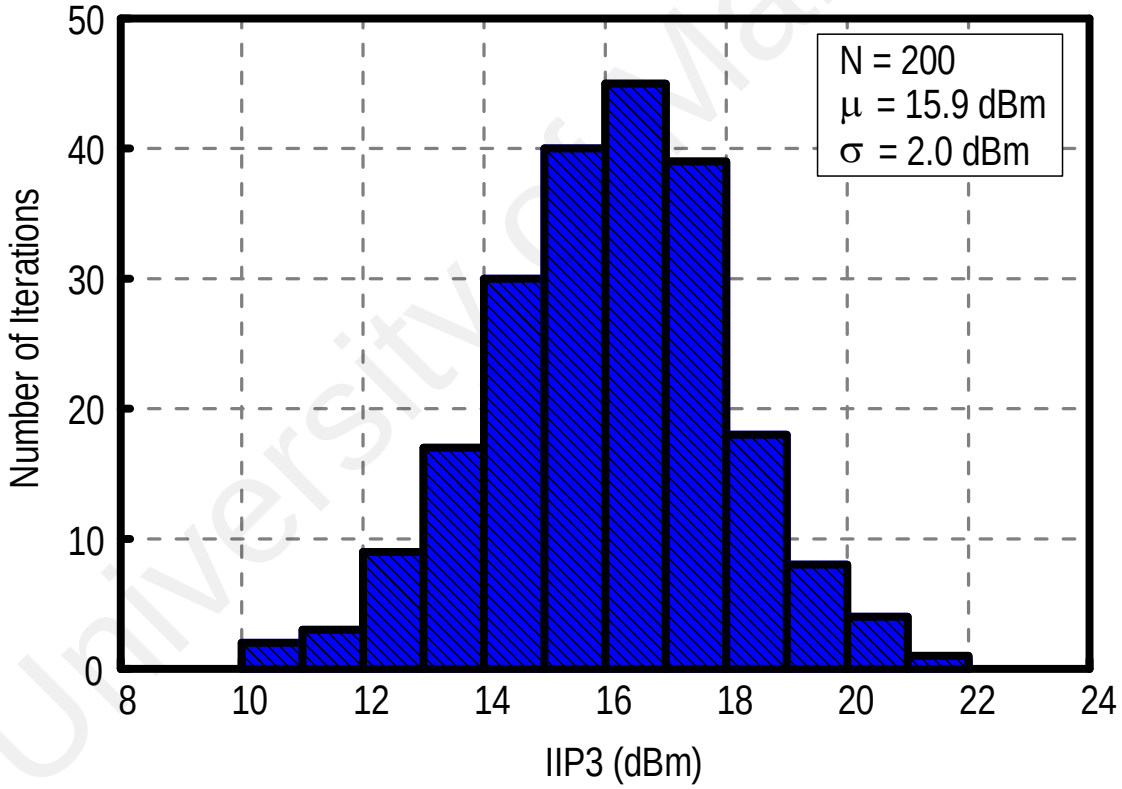


Figure 3.20: IIP3 Monte Carlo simulation results of the proposed mixers.

The port-to-port isolation measurement is conducted by connecting the respective input and output ports to VNA. For example, the RF-to-LO and LO-to-RF isolations measurement results are obtained by connecting the respective RF and LO ports to VNA

as illustrated in Figure 3.18. Similarly, the RF-to-IF and LO-to-IF simulation is performed by connecting the VNA to RF and IF ports, and to LO and IF ports, respectively. Figure 3.19 shows the measured port-to-port isolation between input and output of the proposed mixer. The isolation is >45 dB between the LO, RF, and IF ports.

Table 3.3 summarizes the simulation results in different process corner cases and temperature variations of the proposed circuit. Optimization of the overdrive voltages of M_1 and M_2 lead to a commendable performance even in worse case conditions (FF@85°C and SS@-40°C). In addition, Figure 3.20 plots the Monte-Carlo simulation for IIP3 with process and mismatch variations.

Table 3.4 summarizes the measured results of the proposed mixer in comparison with the state-of-art recently reported in CMOS. The designed prototype mixer reaches the highest FOM which indicates the effectiveness of the proposed linearization technique without compromising other performances, like the conversion gain, the NF and the power consumption.

3.5 Conclusion

A novel multiple-feedback active mixer topology has been introduced with concurrent improvement of the linearity, NF and conversion gain. The reduction of the 2nd-order harmonics in the CCC topology, along with the doubling of the effective transconductance, allows this mixer to obtain low noise and low power. The additional third feedback composed by the positive feedback scheme contributes to the relaxation of the constraints inherent to the conventional DCCC CG transconductor. Prototyped in 0.13-μm CMOS, the mixer measures an IIP3 of +12.5 dBm in a two-tone test, together with a NF of 8.5 dB and a conversion gain of 18.4 dB at an IF = 50 MHz. The mixer consumes 4 mW at 1 V.

Table 3.4: Performance summary and benchmark

Reference	Process (µm)	RF (GHz)	G_c (dB)	NF (dB)	P1dB (dBm)	IIP3 (dBm)	V_{DD} (V)	P_{DC} (mW)	FOM1	FOM2
(Asghari & Yavari 2016)*	0.09	2.4	9.8#	15	-	+15.7	1.2	5.8	-14.9	-15.7
{Mollaalipour &Miar-Naimi, 2016)*	0.18	2.4	6.7	17	-	+9	1.6	4.6	-208	-210.0
[{Asghari & Yavari, 2014)*	0.09	2.4	22.1	13.2	-	+17.1	1.0	4	-4.6	-4.6
(Mollaalipour 2013)*	0.18	2.1	15	14	-	+15	1.8	8	-13.0	-15.6
Kim & Yun, 2014)	0.13	2.1	16.6	14.4	-14.0†	-5.24	1.0	2	-16.7	-16.7
(Bhatt et al., 2014)*	0.18	2.4	5	27**	-	+9	1.8	23.76	-38.8	-41.4
(He & Saavedra 2013)	0.13	0.3-1.2	8.8	4.8**	-8.8	-0.8	0.9	24	-19.6	-19.1
(Liu et al., 2016)	0.18	0.1-2.5	8.9	9.6	-4	+5.8	1.8	3.74	-13.0	-15.6
(Cheng et al., 2013)	0.16	0.9	17.6	10.1**	-18.0†	11.8	1.8	19.62	-13.3	-15.9
(Liao et al., 2018)	0.13	0.3-3.0	15.8	8.6**	-	10.1	1.2	3.1	-5.6	-6.4
This work	**0.13**	**0.9**	**18.4**	**8.5****	**-18.0**	**+12.5**	**1.0**	**4.0**	-4.0	-4.0

* Simulated results ** DSB noise † Graphically estimated # Voltage conversion gain

CHAPTER 4: INDUCTIVELY SOURCE DEGENERATED BALUN-LNA-MIXER WITH INTEGRATED TRANSFORMER-BASED GATE INDUCTOR AND IM2 INJECTION TECHNIQUE

This chapter is organized as follows. Section 4.1 provides brief introduction on ISD transconductor and describes some existing works. In Section 4.2, investigates the ISD transconductor in depth using Volterra series analysis. Section 4.3 presents the proposed linearity enhancement techniques that effectively improve the IIP3 of the ISD transconductor. The measurement results are presented in Section 4.4. Finally, Section 4.5 concludes this chapter.

4.1 Introduction

An ISD transconductor, as shown in Figure 4.1(a), is commonly used in both LNA and mixer design (Nguyen et al., 2004). However, the linearity performance is unsatisfactory as the intrinsic second-order distortion current at the transistor's source is mixed with the fundamental input signal by the feedback mechanism through the degeneration source inductor, thereby generating IM3 distortion.

In fact, there are more than one feedback path existing in an ISD transconductor (i.e., gate-drain feedback through gate-drain capacitance and gate-input feedback through input impedance matching network) as depicted in Figure 3.1(b). The overall linearity can be improved by terminating the second-order nonlinearity in the feedback loop to suppress the generated IM3 component. Harmonic termination (Kim, 2009; Kim, 2004) was proposed in realizing it, where the integrated *LC* network creates a low impedance path to the supply/ground for the second-order frequencies ($\Delta\omega$, 2ω). Despite the suppression in second-order distortion interaction, the required passive *LC* components are bulky which incur noise and restrict improvements in linearity, due to the limited Q factor of the on-chip inductors.

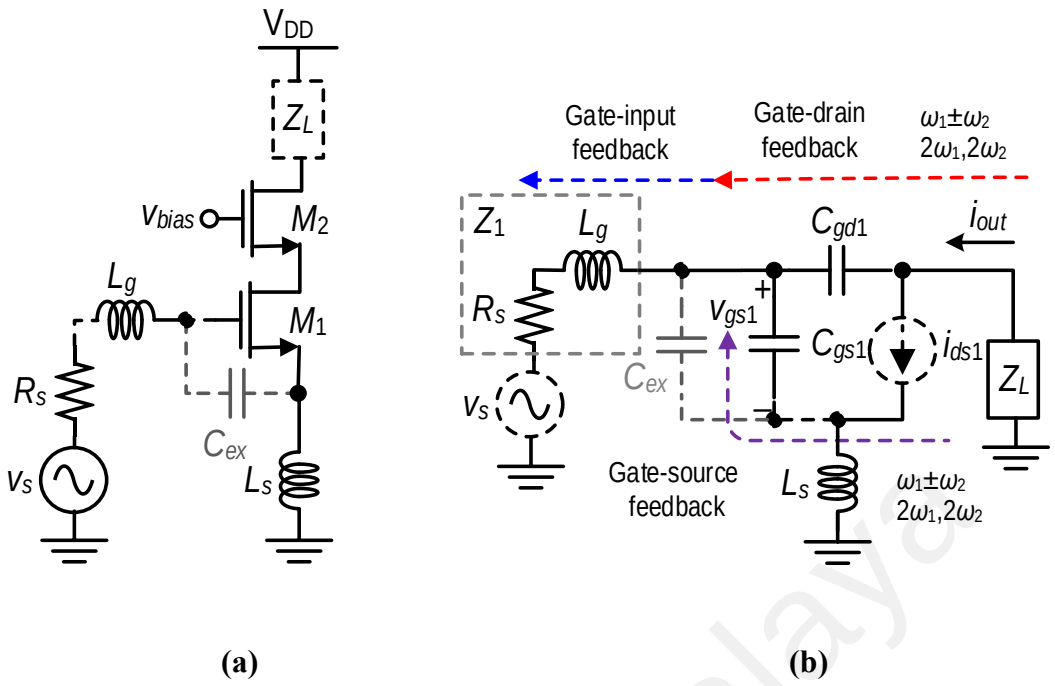


Figure 4.1: (a) Schematic and (b) small-signal equivalent circuit of the ISD common-source transconductor with feedback path

Another technique is the modified derivative superposition (Aparin et al., 2005) that uses two transistors operating in different regions to relax the source-gate feedback effect. This involves a main transistor, M_{main} operating in the saturation region and an auxiliary transistor, M_{aux} operating in subthreshold region to create a second-order derivative transconductance, $g''_{m,aux}$ to cancel the resultant vectors, g'_m and g''_m of M_{main}. When M_{aux} is biased in subthreshold region, additional noise is induced and the input impedance matching is degraded as both transistor gates are shorted together at the input. Similarly, in the pre-distortion technique (Jafarnejad et al., 2017), nonlinearity improvement is achieved at the input of the common gate transistor with an auxiliary transistor operating in the weak inversion region. Post-distortion technique has been implemented in (Kim, 2006; Zhang et al., 2009; Ye et al., 2014) where the auxiliary transistor is connected at the drain of the main transistor instead of directly connecting to the gate. However, this technique improves the nonlinearity with the penalty of gain reduction.

An IM2 injection technique has been proposed in recent years attenuating the total IM3 current by injecting a phase inverted IM2 signal into the differential transconductor and producing an interaction term in the IM3 current. (Asghari & Yavari, 2016; Lou & Luong, 2008; Mollaalipour & Miar-Naimi, 2013, Yu, 2015) adopted a squaring circuit to generate the IM2 signal. In (Mollaalipour & Miar-Naimi, 2013), the IM2 signal is injected at the gate of the mixer's input transistor; thus, the second-order component potentially leaks through the gate-input feedback to the former block such as the LNA, resulting in performance degradation for the entire receiver. This problem can be mitigated by injecting the IM2 signal into bulk of the input transistor (Asghari & Yavari, 2016) or tail transistor of the differential amplifier (Yu et al., 2015) with commendable output IIP3 improvement. In (Yu et al., 2015), the conventional capacitor in IM2 circuit was replaced with a large varactor to increase the two-tone spacing at the cost of increase in active chip area consumption. But, the discussion in both work is limited to the linearity improvement of the circuit only. On the other hand, the cascaded LNA and mixer configuration in (Lou & Luong, 2008) achieves an IIP3 of +10.6 dBm at the penalty of higher power consumption. In contrary to the cascaded architecture, the merging of the LNA and mixer through the current reuse structure is preferred to reduce total power consumption (Guo, 2014).

In this work, IM2 injection and optimum bias voltage technique are introduced into the ISD transconductance based LNA-mixer to improve the linearity and to maintain the G_c at low power consumption. Also, a passive balun and transformer-based gate inductor are adopted at the input of the transconductor to aid input impedance matching and to create high fundamental rejection signal for the IM2 injection circuit via its balanced feature. This architecture also achieves a solution to the gate-input feedback through the transformer-based input impedance matching network.

4.2 Literature Review

The simplified equivalent circuit of the conventional ISD transconductor is shown in Figure 4.1(b) and is used to calculate the IIP3. The output current of the input transistor, M_1 can be expressed as a harmonic function of the input voltage v_s using the following Volterra-series expression:

$$i_{out} = G_1(\omega) \circ v_s + G_2(\omega_1, \omega_2) \circ v_s^2 + G_3(\omega_1, \omega_2, \omega_3) \circ v_s^3 \tag{4.1}$$

where ° is the Volterra series operator. The $G_1(\omega)$, $G_2(\omega_1, \omega_2)$ and $G_3(\omega_1, \omega_2, \omega_3)$ are models representing the first-, second-, and third-order transconductance of M_1, respectively. Similar to the expansion presented in (Kim, Aparin, & Larson, 2011) with the inclusion of linear conductance, g_{ds1} while neglecting distortion contribution from the cascode transistor M_2, the IIP3 expression of the ISD common-source stage by using Volterra series can be expressed as follows:

$$IIP3(\pm\omega_1, \pm\omega_1, \pm\omega_2) = \frac{1}{6R_s}\left|\frac{G_1(\omega_1)}{G_3(\pm\omega_1, \pm\omega_1, \mp\omega_2)}\right|. \tag{4.2}$$

The first- and third-order Volterra kernels are given by (4.3) and (4.4), respectively, given as

$$G_1(\omega) = T_1(\omega) \times \left\{ \frac{g_{m1}\left(1 - Y_{gd1}(\omega)Z_s(\omega)\right) - g_{ds1}c(\omega)Z_s(\omega) - b(\omega)Y_{gd1}(\omega)}{g_{ds1}\left(Z_s(\omega) + Z_L(\omega)\right) + a(\omega)} \right\} \tag{4.3}$$

$$\begin{aligned} G_3(\pm\omega_1, \pm\omega_1, \mp\omega_2) &= T_1^2(\pm\omega_1) \cdot T_1(\mp\omega_2) \\ &\times \left\{ \frac{1}{g_{m1} + g(\pm 2\omega_1 \mp \omega_2)} \cdot \frac{\alpha(\pm 2\omega_1 \mp \omega_2)}{Z_x(\pm 2\omega_1 \mp \omega_2)} \cdot \varepsilon(\pm\omega_1 \mp \omega_2, \pm 2\omega_1) \right\} \end{aligned} \tag{4.4}$$

in which,

$$T_1(\omega) = \frac{1}{g_{m1} + g(\omega)} \times \frac{g_{ds1}\left(Z_s(\omega) + Z_L(\omega)\right) + a(\omega)}{Z_x(\omega)} \tag{4.5}$$

$$\varepsilon(\pm\omega_1 \mp \omega_2, \pm 2\omega_1) = g''_{m1} - \frac{2}{3}(g'_{m1})^2 \cdot \left(\frac{2}{g_{m1} + g(\pm\omega_1 \mp \omega_2)} + \frac{1}{g_{m1} + g(\pm 2\omega_1)} \right) \quad (4.6)$$

$$g(\omega) = \frac{1}{Z_x(\omega)} \times \left\{ g_{ds1}\left(Z_x(\omega) + Z_y(\omega)\right) + Y_{gs1}(\omega)Z_x(\omega) + a(\omega) + c(\omega)Z_1(\omega) \right\} \quad (4.7)$$

$$\alpha(\omega) = b(\omega) + c(\omega)Z_1(\omega) \quad (4.8)$$

$$Z_x(\omega) = Z_s(\omega) + Y_{gd1}(\omega)Z_T(\omega) \quad (4.9)$$

$$Z_y(\omega) = Z_L(\omega) + Y_{gs1}(\omega)Z_T(\omega) \quad (4.10)$$

$$Z_T(\omega) = Z_1(\omega)Z_L(\omega) + Z_1(\omega)Z_s(\omega) + Z_L(\omega)Z_s(\omega). \quad (4.11)$$

a=$(1+Y_{gd1}Z_L)$, b=$(1+Y_{gs1}Z_s)$ and c=$(Y_{gs1}+Y_{gd1})$. Y_{gs1} and Y_{gd1} are the parasitic admittances at the gate-source and gate-drain of M_1, respectively. Z_s is the source node impedance of M_1 which is denoted as $j\omega L_s$. $T_1(j\omega)$ is the linear transfer function of gate-source voltage, v_{gs1} over v_s. $\varepsilon(\pm\omega_1 \mp \omega_2, \pm 2\omega_1)$ shows the effect of the output current nonlinearities on IM3 distortion. The second term in (4.6), describes the second-order nonlinearity of the input transistor, g'_{m1} contributing IMD3 due to multiple harmonic feedback interaction triggered in the circuit mainly by degenerated source inductor and gate-drain capacitances. This causes a degradation in IIP3 even at the optimum gate biasing point, where the third-order nonlinear coefficient g''_{m1} of input transistor is zero. As can be inferred from Figure 4.2, when g''_{m1} is minimized to 0 at V_{gs}=0.49 V, g'_{m1} shows a peak value, thus the second term in (4.6) dominates the nonlinearity of the circuit at this bias point. Figure 4.3 explains this phenomenon, where the analytical IIP3 plot shows a high peak without the g'_{m1} component.

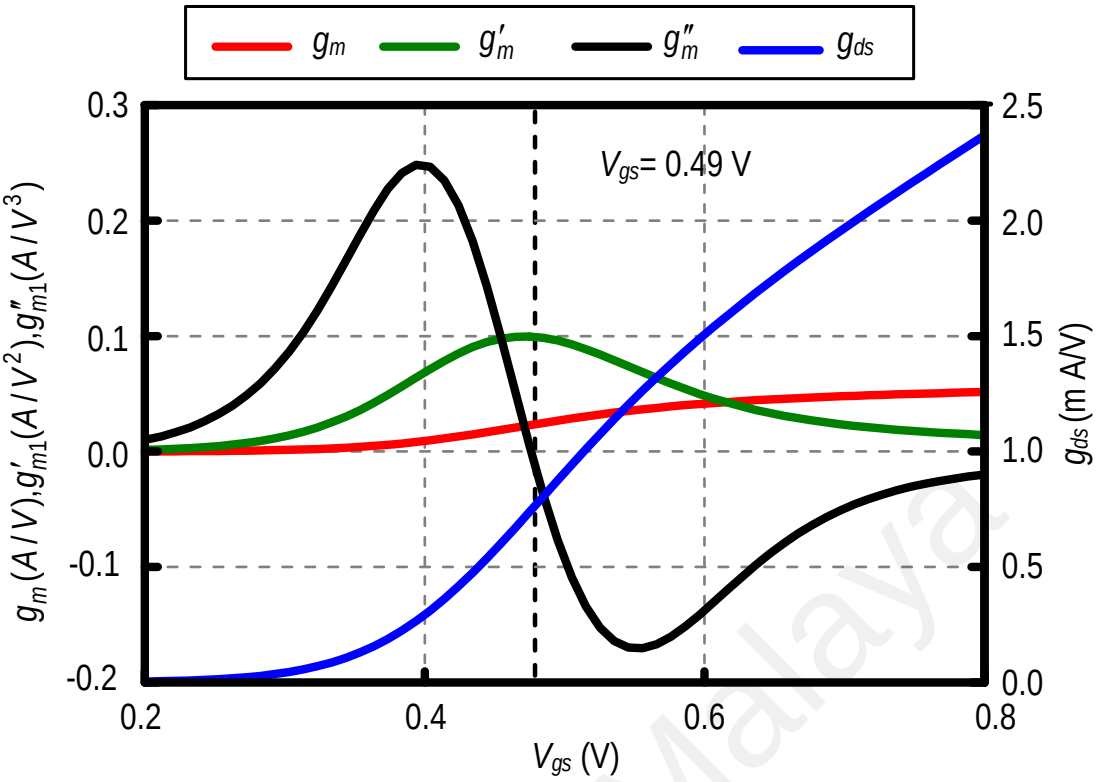


Figure 4.2: g_m, g_{ds}, g'_m and g''_m common-source 80/0.13-µm NMOS transistor. Threshold voltage is about 0.40 V for this device.

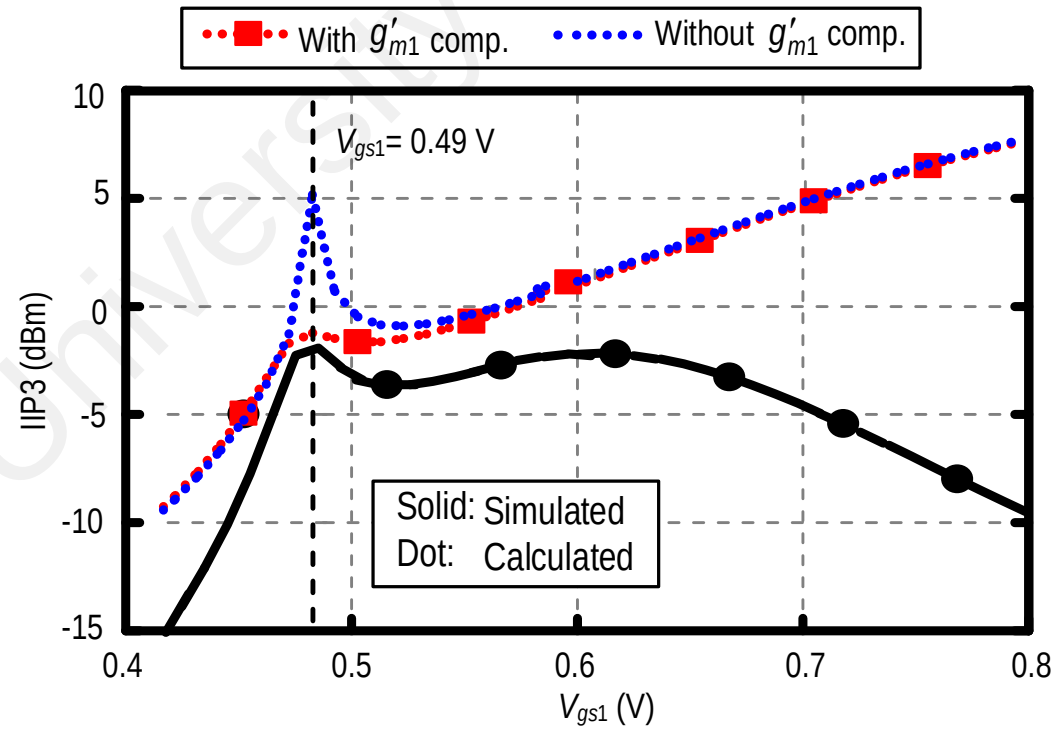


Figure 4.3: Simulated and calculated of IIP3 for different values of V_{gs1}

However, the possibility in improving linearity of the ISD transconductor without degrading the NF performance is established if a small-device of input transistor is selected at a relatively high overdrive voltage V_{gsT} ($\approx V_{gs}$-V_{th}). As discussed in (Baki, Tsang, & El-Gamal, 2006), the capacitor C_{ex} integrated in reducing the input transistor size in minimizing the feedback effect caused by C_{gd} and C_{ds}, also reducing the transconductance distortions due to large V_{gsT}. This is illustrated in Figure 4.3, where the analytical IIP3 plot of the ISD transconductor improves when V_{gsT} increases at the cost of increased power consumption. However, note that the simulated IIP3 plot of the cascoded ISD transconductor is limited and degraded drastically when V_{gsT} (>200 mV). This is because, when, the input cascoded ISD transistor biased in strong inversion region, the drain-voltage plays a significant role due to higher gain of the transconductor compared to the one biased in moderate inversion region. Despite the reduction in transconductance distortion as V_{gsT} is increased, the transistor M_1 tends to be pushed into linear region of operation at high V_{gsT} at low supply voltage resulting in a high output conductance nonlinearity (g'_{ds1} , g''_{ds1}) and cross-modulation nonlinearity, hence (4.4) becomes invalid. Besides that, the distortion contribution from the cascoded transistor M_2 becomes dominant, as the output resistance of M_1 is low in advanced CMOS process (Cheng, 2012).

In this work, to effectively enhance the linearity of the ISD transconductor at low power consumption, the input transistor is biased at moderate inversion region by setting g''_{m1} to zero, while, the third-order nonlinearity distortion current which arises by the feedback effect is suppressed by injecting an opposite sign of second-order intermodulation current into the bulk of the input transistor. In addition, the second-order injection technique is plausible because it does not degrade the gain and contribute noise as it works in common-mode frequencies and consumes negligible amount of current.

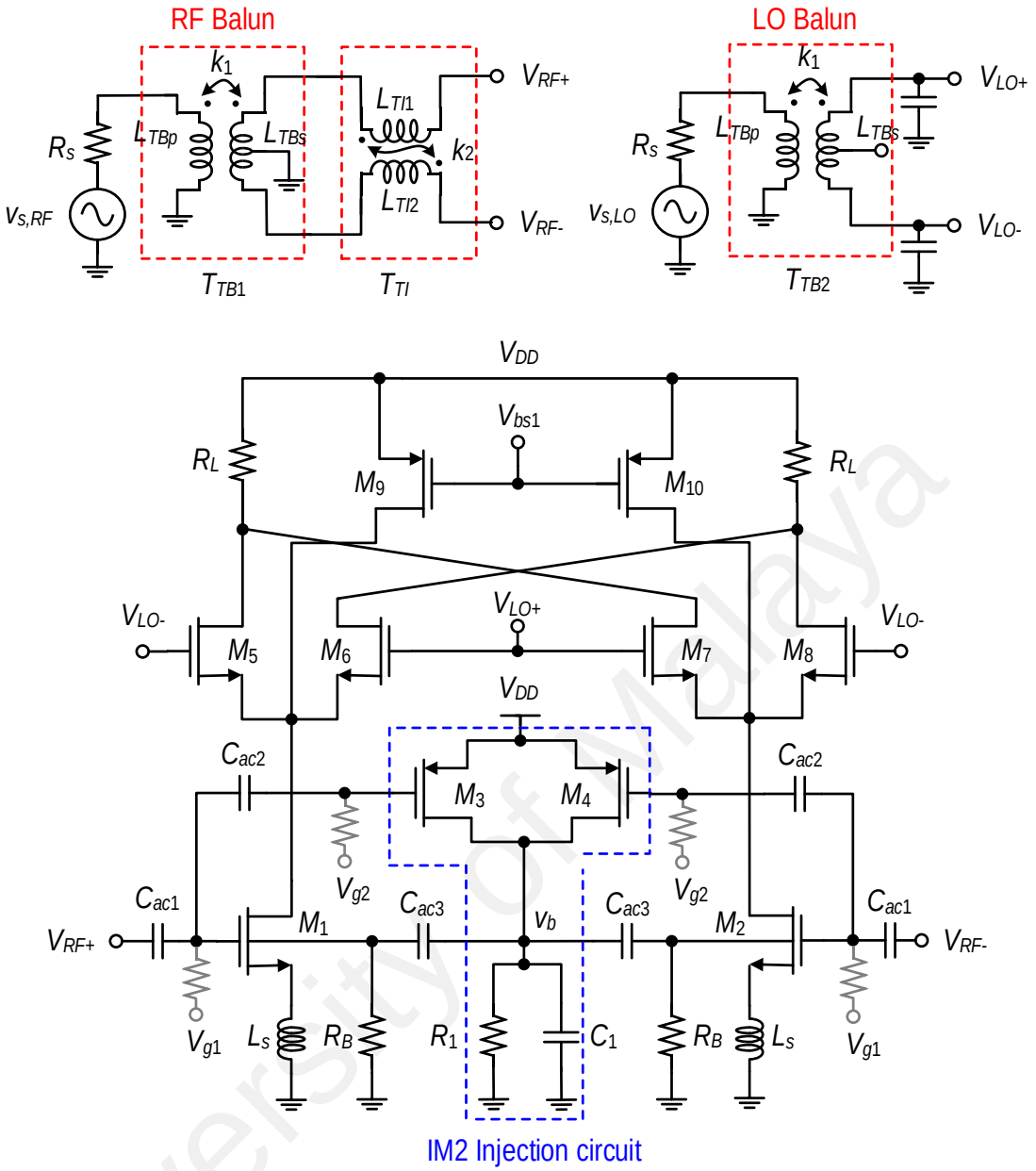
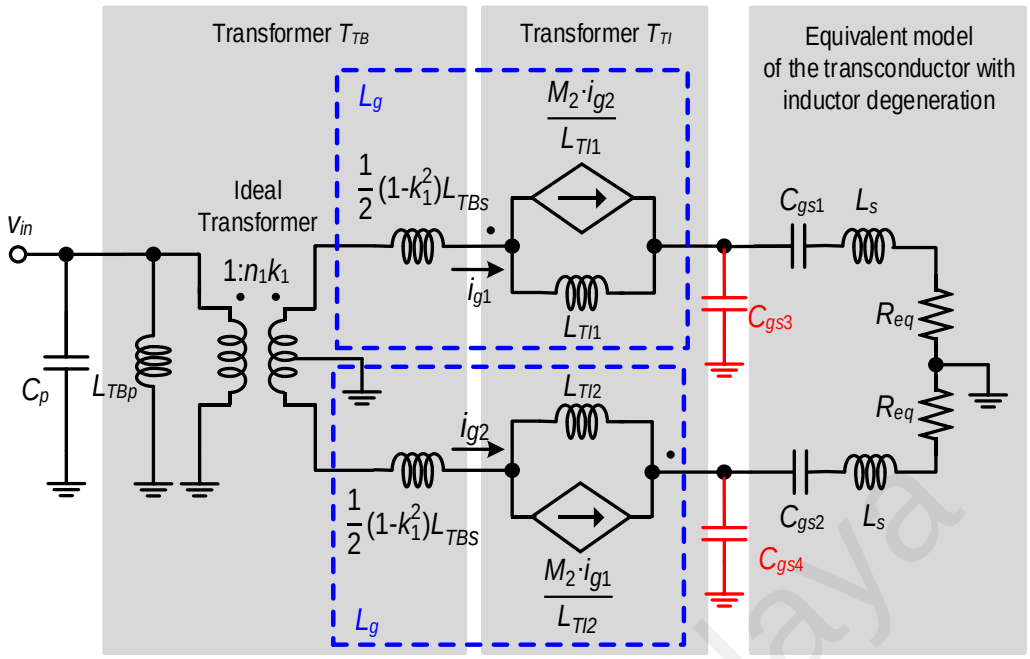


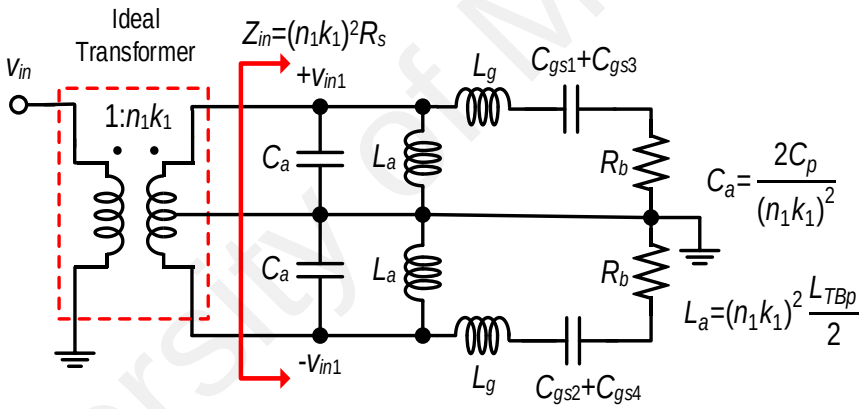
Figure 4.4: Circuit schematic of the proposed modified ISD balun-LNA-mixer including an on-chip transformer-based balun and a transformer-based inductor at the input transconductance stage without the output IF buffer and biasing circuits. The three transformers impedance ratio from the primary to the secondary winding is unity

4.3 Proposed ISD Based Balun-LNA-Mixer

Figure 4.4 shows the proposed balun-LNA-mixer, where the transistor M_1-M_2 acts as the ISD transconductor with a source inductor L_s while the transistor M_5-M_8 forms the switching pair for the differential double-balanced mixer. An IM2 injection circuit which consists of $M_{3,4}$, R_1 and C_1, are introduced into the ISD transconductor to improve the



(a)



(b)

Figure 4.5: Schematic showing the proposed differential ISD transconductor with (a) transformer equivalent model of transformer-based balun T_{TB1} and transformer-based gate inductor T_{TI} while including input parasitic capacitance. (b) The more compact equivalent circuit model of input network for calculating the input impedance by series of parallel-series conversion

linearity by injecting the second-order intermodulation at the bulk of $M_{1,2}$ through the ac-coupling capacitor C_{ac3}. Resistor R_B bias the bulk terminal of $M_{1,2}$ with zero potential as it is shorted to ground. The current-bleeding transistor $M_{9\text{-}10}$ enhances the CG of the LNA-mixer by splitting the current flow into the load, R_L. A simple 1:1 transformer-based balun $T_{TB1,2}$ in an unbalance-to-balanced configuration with a center-tap is used at the input of

RF and LO ports for input impedance matching and single-ended to differential conversion. Additionally, the transformer T_{TI} is added between T_{TB1} and transistor $M_{1,2}$ to provide the necessary series gate inductance for the input impedance matching and high common-mode rejection for the IM2 circuit with reduced physical area consumption compared to the conventional practice in integrating an individual gate inductor.

Subsections 4.3.1, 4.3.2 and 4.3.3 present a detailed analysis of the input impedance matching, conversion gain and noise on the proposed ISD topology by considering the transformer losses due to magnetic flux leakage. Those subsections, the bulk effect of the input transistor is neglected as the output of the squaring circuit contains only even-order components and the fundamental signal is cancelled at V_b. In contrary, the linearity computation in Subsection 4.3.4 incorporates this bulk effect to obtain a comprehensive analysis into the nonlinearity of the proposed transconductor.

4.3.1 Input Impedance Matching

Input differential transconductance stage, consists of two transformers T_{TB1} and T_{TI} where the transformer models are adopted from (Vallese et al., 2009) and (Long, 2000), respectively. The parasitic resistance of T_{TB1} and T_{TI} are neglected to simplify the analysis. L_{TBp} and L_{TBs} are the primary and secondary inductance of T_{TB1} respectively and $n_1 = \sqrt{L_{TBs}/L_{TBp}}$ represents the turn ratio. L_{TI1} and L_{TI2} are the primary and secondary winding inductance of T_{TI}, respectively with a mutual inductance, M_2. The parameter k_1 represents the coupling coefficient of T_{TB1}. The capacitance C_p represents both the parasitic capacitance of the primary side of T_{TB1} and the bondpads. The parasitic gate-source capacitance, $C_{gs3,4}$ of the squaring device is accounted in as it is directly connected to the input transistor.

T_{TI} is a 1:1 transformer, hence, it could be related as $L_{TI1} = L_{TI2}$ and i_{g1}=-i_{g2}. In differential mode, the effective inductance of the primary and secondary coils $i_{g1} = -i_{g2}$ of T_{TI} can be

represented as $L_{eff} = L_{TI}(1+k_2)$, where $k_2 = M_2/\sqrt{L_{TI1}L_{TI2}}$ is the coupling coefficient of T_{TI}. The input network is simplified further as shown in Figure 4.5(b) by transferring the primary impedance of T_{TB1} referred to the secondary of an ideal transformer. The variable L_g is used to represent the total series inductance of $0.5(1-k_1^2)L_{TBs}+L_{eff}$. At resonant frequency, the parallel capacitor $C_{gs3,4}$ in Figure 4.5(a) is transformed into series representation by applying a parallel-to-series impedance transformation (Sivonen, Kangasmaa, & Parssinen, 2003). Then, the resulting real impedance of the ISD amplifier is reduced to $R_b \approx \eta^2 R_{eq}$, where $\eta = C_{gs1}/(C_{gs1}+C_{gs3})$ and $R_{eq} = \omega_T L_s + R_g$. R_g is gate resistance of the input transistor M_1. Interestingly, the circuit transformation forms a parallel-to-series input network.

At resonant frequencies,

$$\omega_{o1} L_a = \frac{1}{\omega_{o1} C_a} \tag{4.12}$$

$$\omega_{o2} L_g = \frac{1}{\omega_{o2} C_t} \tag{4.13}$$

where ω_{o1} and ω_{o2} are parallel and series LC resonant frequencies and $C_t = C_{gs1} + C_{gs3}$. The ideal input impedance matching condition is achieved by selecting proper inductor and capacitor values to ensure the parallel and series LC networks resonate at the same frequency ($\omega_{o1} = \omega_{o2} = \omega_o$); i.e., $L_a C_a = L_g C_t$, and the real impedance of $Z_{in} \approx n_1^2 k_1^2 R_s$. Subsequently, the real input differential impedance looking into the secondary winding becomes,

$$\begin{aligned} Z_{in}(\omega_o) &= n_1^2 k_1^2 R_s \\ &= 2\eta^2 R_{eq} = 2\eta^2(\omega_T L_s + R_g) \end{aligned} \tag{4.14}$$

where $\omega_T = g_{m1}/C_{gs1}$. If the parasitic resistance is neglected, the real part of Z_{in} is reduced by the term η in comparison to the typical power-constrained ISD amplifier for a given

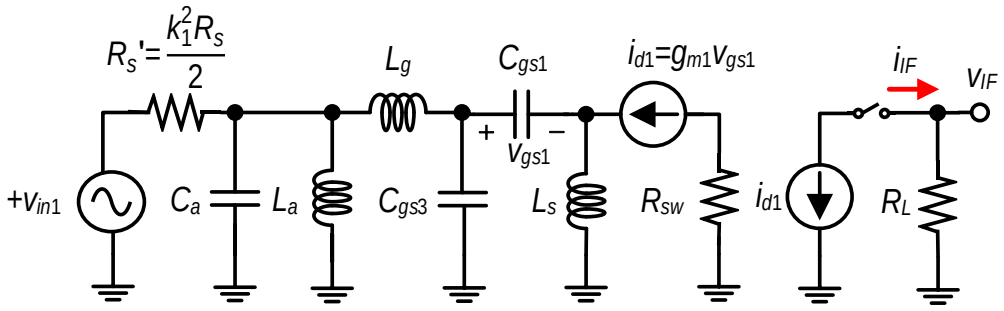


Figure 4.6: Half-circuit small signal representation of proposed balun-LNA-mixer

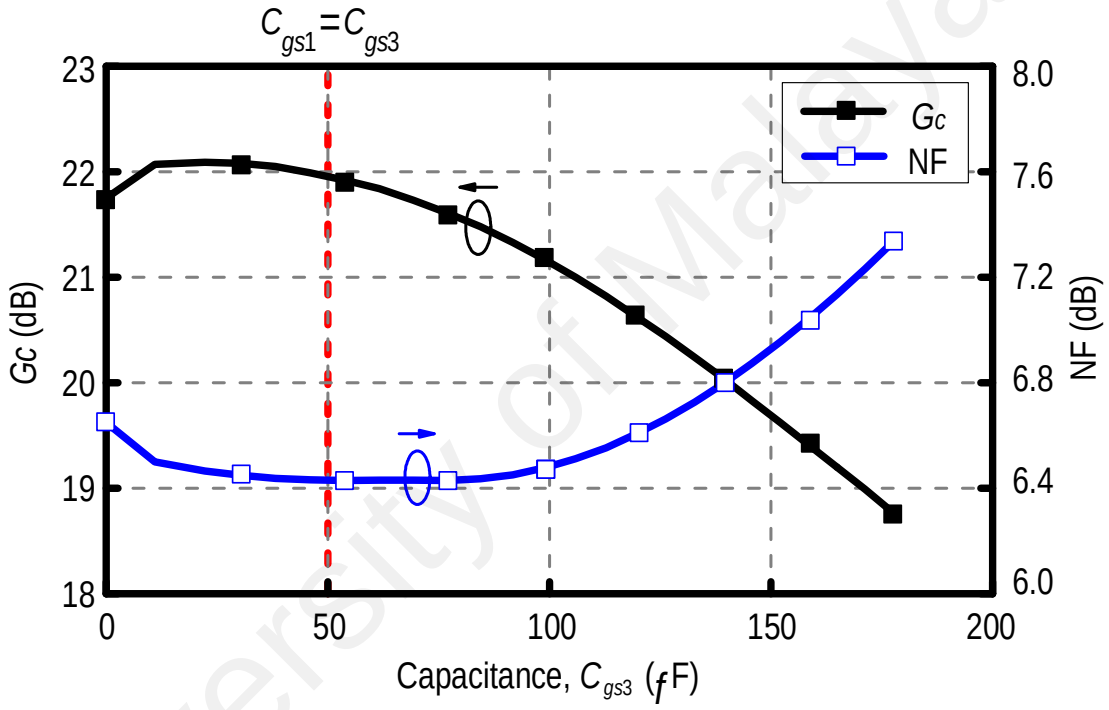


Figure 4.7: Simulated G_c and NF of the proposed balun-LNA-mixer with different transistor size of $M_{3,4}$, to demonstrate its effects when $C_{gs1} \approx 50$ fF

value of L_s, g_{m1}, and transistor size. This means that the ratio of T_{TB1} is limited by C_{gs3}. An additional inductance is adopted via the transformer based gate inductor, as the inductance T_{TB1} is insufficient to resonate at 2.4 GHz.

In reference to (4.13), a smaller gate inductance L_g is required for series resonance at a given input device size and operating frequency due to C_{gs3}. Also, the transformer coupling effect increases the effective inductance of each side of T_{TI} by a factor of (1 +

k_2) in a differential input network. This suggests that the physical area can be reduced further while retaining the desired inductance for input impedance matching. As a result, the parasitic capacitance which is dependent on the length and size of the winding metal trace is reduced, consequently improving the circuit performance as compared to the individual inductors. Similarly, higher quality factor and self-resonant frequency can be achieved compared to individual inductors (Long, 2000).

Note that the parallel-to-series transformation of $C_{gs3,4}$ in Figure 4.5(b) is only valid at the resonant frequency. Since both the parallel and series tank resonates at the same frequency of ω_o, the equivalent circuit transformation is valid.

4.3.2 Conversion Gain and Balanced Input Signal Analysis

Figure 4.6 shows the half circuit small-signal model of the transconductance stage where R_{sw} represents the resistance at the switching transistor's source. At input impedance matching condition, neglecting the parasitic resistance and adopting $(\omega_T/\omega_o)>>1$, the voltage G_c of the LNA-mixer, A_v can be expressed as,

$$A_v = \frac{2}{\pi}\frac{R_L}{\omega_o L_s}\cdot\left|\frac{1}{1-\omega_o{}^2 C_{gs3}L_g + j\omega_o C_{gs3}R_s'}\right|. \tag{4.15}$$

G_c of the LNA-mixer at the resonant frequency is relatively independent of the transconductance $g_{m1,2}$. Thus, the G_c performance of the proposed circuit is relaxed by the optimum biasing point technique.

The injected IM2 would cause gain degradation through the interaction with the fundamental signal in the main path; however, the generated IM3 is at the same order of the intrinsic IM3 at the main path (Lou, 2008). Thus, the G_c is effectively unchanged by the proposed linearization techniques. Alternately, the parasitic capacitance from the transistor $M_{3,4}$ would not deteriorate the G_c performance of the circuit. For a 1:1

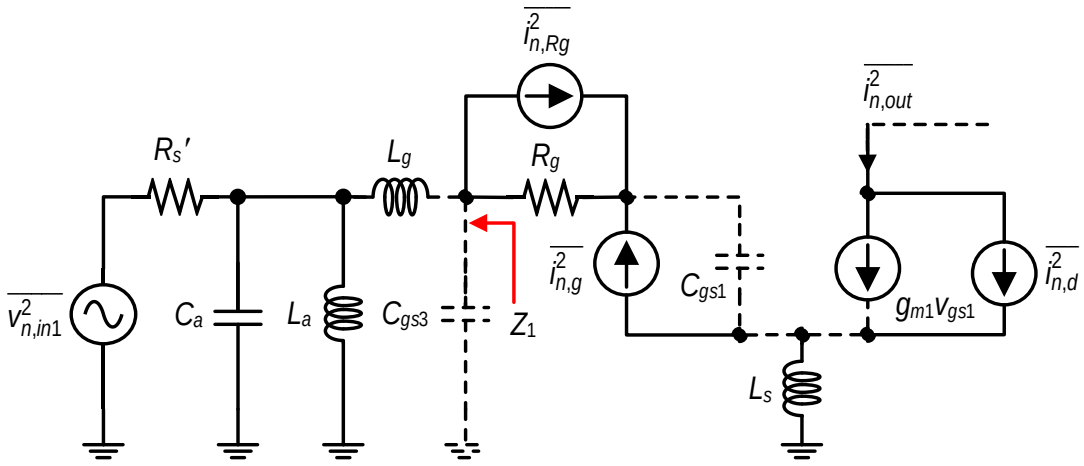


Figure 4.8: Noise equivalent half-circuit of the input transconductance stage

impedance transformer, C_{gs3} is designed to be equal or smaller than C_{gs1} for the purpose of input impedance-matching in (4.14), thus conserving the G_c of the LNA-mixer, evidently observed in Figure 4.7. In conclusion, a lower impedance transformation and an optimum device dimension of $M_{3,4}$ are required to maintain the G_c.

Some gain and phase imbalances of an on-chip or off-chip transformer-balun are unavoidable due to its imperfection and asymmetric parasitic capacitance interaction with the internal circuit elements. The integration of inductor-based transformer between the output differential terminals of the balun creates a mutual inductance between the differential terminals so that a well-balanced input signal is generated and to ensure that the squaring circuit has high common-mode rejection (Oh, Kim, & Kim, 2017). This high common-mode rejection allows the NF of the main transconductance stage to be well isolated from the noise generated from the squaring circuit.

4.3.3 Noise Figure Analysis

Figure 4.8 depicts the half circuit of the transconductance stage with the transformer input network to compute the NF. The noise contribution from IM2 injection circuit is neglected as the injected signal only contains common-mode components, and the

capacitance $C_{gs3,4}$ is included as it is directly connected to the gate of the input transistor $M_{1,2}$. The parallel LC network, i.e. $(1/sC_a)//sL_a$ is an open circuit at the desired operating frequency for maximum power transfer, and hence, it contributes minimum noise to the circuitry.

When C_{gs3}=0, the noise factor (F) of the single transconductance stage at ω_o is given as (Belostotski, 2006}

$$F = 1 + \frac{R_g}{R_{eq}} + \frac{\delta\alpha}{5}\frac{1}{g_{m1}R_{eq}} + \frac{\gamma}{\alpha}g_{m1}R_{eq}\left(\frac{\omega_T}{\omega_o}\right)^2 \cdot \left(1 + \frac{\delta\alpha^2}{5\gamma} - 2\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \quad (4.16)$$

where α is the ratio of device transconductance to zero-bias drain-to-source conductance, δ is the coefficient of drain noise, γ is the coefficient of gate noise, and c is a correlation coefficient of the gate-induced noise current and the drain noise current. In the presence of C_{gs3}, the noise factor in (4.16) can be rewritten by simply substituting the resistance R_{eq} with $R_s/2\eta^2$ (Sivonen, Kangasmaa, & Parssinen, 2003) and assuming k_1 is equal to 1, i.e.,

$$F = 1 + 2\frac{R_g\eta^2}{R_s} + \frac{\delta\alpha}{5}\frac{2\eta^2}{g_{m1}R_s} + \frac{\gamma}{\alpha}\frac{g_{m1}R_s}{2\eta^2}\left(\frac{\omega_o}{\omega_T}\right)^2 \cdot \left(1 + \frac{\delta\alpha^2}{5\gamma} - 2\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right). \quad (4.17)$$

As shown in Figure 4.7, the NF increases when the device size of M_3 is increased, where the last term in (4.17) becomes dominant as the factor η is inversely proportional. This term can be reduced by increasing ω_T through either increasing the aspect ratio or the gate biasing of the input transistor $M_{1,2}$. Unfortunately, a large aspect ratio leads to a large C_{gs1}, alternately an increase in the gate biasing effects the sweet spot induced linearity. However, the drop in the fourth term is partially relaxed by a lower turn ratio of the transformer T_{TB}, which is reflected by the factor of 1/2. Furthermore, in this design,

C_{gs3} is approximated to be equal to the parasitic capacitance C_{gs1}, thus, the 2nd and 3rd terms can be reduced by half compared to the conventional notation described in (4.16).

4.3.4 Linearity Analysis

As discussed earlier, the linearity performance of the ISD transconductance stage is limited by two mechanisms; the intrinsic third-order nonlinearity term, g''_{m1} in the main path and second-order nonlinear component, g'_{m1} interaction in a feedback. If the second-order nonlinear signal IM2 is injected into the bulk terminal of the input transistors, additional IM3 components will appear at the output of the ISD transconductor. This additional IM3 terms originating from g'_{mb1} and g'_{m3} by the interaction created between the bulk and source terminals, with an opposite sign and same magnitude, cancels the indirectly generated IM3 signal in the main path due to the second-order interaction.

The IM2 injection signal is externally generated based on a simple squaring circuit M_3 and M_4 as shown in Figure 4.9. Z_1 is the source impedance looking into the left side of gate terminal M_1. To understand the proposed linearization technique in ISD transconductor, a two-tone input signal with equal amplitude is injected for the linearity verification. As both the drain of M_3 and M_4 are shorted, the fundamental and odd-order distortion components are cancelled with only even-order components present at node v_b. The injected IM2 voltage is mixed with the fundamental input signal to generate new third-order intermodulation, IM3 term at $2\omega_1$-ω_2 which cancels out the generated IM3 distortion component due to the gate-source and gate-drain feedbacks.

As the signal is applied at the bulk terminal of the transistor $M_{1,2}$, the body effect is taken into consideration while the nonlinear output conductance and cross-modulation terms among the nonlinearity components are neglected. Additionally, the back bias of M_3 and M_4 are ignored as both the bulk terminals are tied to the source. Thus, the small-signal drain current of the transistors can be expressed by a Taylor series expansion as:

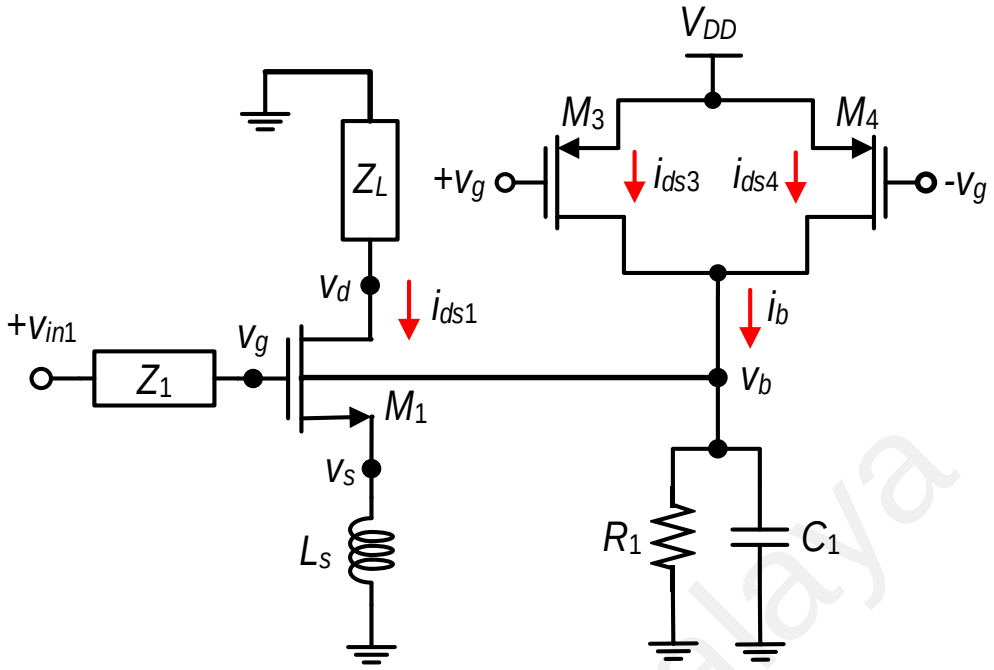


Figure 4.9: Thevenin's equivalent half-circuit of a combined inductively-degenerated common-source transconductance stage and IM2 injection

$$\begin{aligned} & i_{ds1}(v_{gs1}, v_{ds1}, v_{bs1}) \\ & = g_{m1}v_{gs1} + g_{ds1}v_{ds1} + g_{mb1}v_{bs1} + g'_{m1}{v_{gs1}}^2 - g'_{mb1}{v_{bs1}}^2 + g''_{m1}{v_{gs1}}^3 + g''_{mb1}{v_{bs1}}^3 + \ldots \\ & = g_{m1}(v_g - v_s) + g_{ds1}(v_d - v_s) + g_{mb1}(v_b - v_s) + g'_{m1}(v_g - v_s)^2 \\ & -g'_{mb1}(v_b - v_s)^2 + g''_{m1}(v_g - v_s)^3 + g''_{mb1}(v_b - v_s)^3 \end{aligned} \tag{4.18}$$

$$i_{ds3}(v_{sg3}) = g_{m3}v_{sg3} + g'_{m3}{v_{sg3}}^2 + g''_{m3}{v_{sg3}}^3 = -g_{m3}v_g + g'_{m3}{v_g}^2 - g''_{m3}{v_g}^3 \tag{4.19}$$

$$i_{ds4}(v_{sg4}) = g_{m4}v_{sg4} + g'_{m4}{v_{sg4}}^2 + g''_{m4}{v_{sg4}}^3 = g_{m4}v_g + g'_{m4}{v_g}^2 + g''_{m4}{v_g}^3 \tag{4.20}$$

where v_{gsn} and v_{bsn} are the voltages applied to the gate-to-source and bulk-source of nth transistor, respectively. g_{mb1} is the first-order coefficient of the bulk-transconductance of the transistor M_1. g'_{mbn} and g''_{mbn} denotes the first- and second-order derivative of bulk-transconductance, respectively.

The ultimate goal is to derive the relationship between the input voltage and output current by using Volterra series expansion in the frequency domain so that the third-order nonlinearity coefficient can be identified. Hence, the gate, source, and bulk voltages of M_1 can be modeled by the following truncated Volterra series with respect to the input voltage, v_{in1} as:

$$v_g = A_1(\omega) \circ v_{in1} + A_2(\omega_1, \omega_2) \circ {v_{in1}}^2 + A_3(\omega_1, \omega_2, \omega_3) \circ v_{in1}^3 \tag{4.21}$$

$$v_s = B_1(\omega) \circ v_{in1} + B_2(\omega_1, \omega_2) \circ {v_{in1}}^2 + B_3(\omega_1, \omega_2, \omega_3) \circ v_{in1}^3 \tag{4.22}$$

$$v_d = C_1(\omega) \circ v_{in1} + C_2(\omega_1, \omega_2) \circ {v_{in1}}^2 + C_3(\omega_1, \omega_2, \omega_3) \circ v_{in1}^3 \tag{4.23}$$

$$v_b = D_2(\omega_1, \omega_2) \circ v_{in1}^3 \tag{4.24}$$

Similarly, A_n's, B_n's, C_n's and D_n's models the n-th order nonlinear responses. Firstly, Kirchhoff's current law (KCL) equations can be developed at each node to derive the A_n, B_n, C_n and D_n kernels as follows:

$$\frac{v_{in1} - v_g}{Z_1(\omega)} = Y_{gs1}(\omega)(v_g - v_s) + Y_{gd1}(\omega)(v_g - v_d) \tag{4.25}$$

$$i_{ds1} + Y_{gs1}(\omega)\left(v_g - v_s\right) = \frac{1}{Z_s(\omega)} v_s \tag{4.26}$$

$$Y_{gd1}(\omega)\left(v_g - v_d\right) = i_{ds1} + \frac{v_d}{Z_L(\omega)} \tag{4.27}$$

$$i_b = i_{ds3} + i_{ds4} = Y_b(\pm\omega_1 \pm \omega_2) v_b \tag{4.28}$$

where $Y_b = 1/R_1 + j\omega C_1$ is the output drain admittance of transistor $M_{3,4}$. Here, Z_L represents impedance at the drain node of transistor $M_{1,2}$, which includes R_{sw} and the

parasitic capacitance at this drain node. Taking M_3 and M_4 to be identical and substituting (4.19) and (4.20) into (4.28), the output voltage of the squaring circuit can be found as,

$$v_b = 2\frac{1}{Y_b(\pm\omega_1 \mp \omega_2)} g'_{m3} v_g^2. \tag{4.29}$$

From (4.24) and (4.29), the second-order Volterra kernel of $D_2(\omega_1,\omega_2)$ can be derived as,

$$D_2(\pm\omega_1, \mp\omega_2) = \frac{2g'_{m3}}{Y_b(\pm\omega_1 \mp \omega_2)} A_1(\omega_1) A_1(\omega_2). \tag{4.30}$$

In reference to Figure 4.9, a nodal equation at the drain node of transistor M_1 can be obtained as,

$$i_{ds1} = i_{out} = -v_d / Z_L(\omega). \tag{4.31}$$

Hence, the nth-order Volterra operator $G_{n,p}$ that describes the output current nonlinearity of the proposed transconductor are given as,

$$G_{n,p} = -C_n \Big/ Z_L\left(\sum\nolimits_{i=1}^{\{2,3\}} \omega_i\right). \tag{4.32}$$

Therefore, $C_n(\omega_1, \omega_2, \ldots, \omega_n)$ has to be derived to obtain $G_{n,p}$ of the Volterra operators. (4.25)-(4.27) are solved recursively to obtain kernels in (4.21)-(4.23). The detailed derivation of the Volterra kernels is given in the Appendix C. By using Volterra kernels $A_n(\omega_1, \omega_2, \ldots, \omega_n)$, $B_n(\omega_1, \omega_2, \ldots, \omega_n)$ and $C_n(\omega_1, \omega_2, \ldots, \omega_n)$, the $G_{n,p}(\omega_1, \omega_2, \ldots, \omega_n)$ of the Volterra operators are

$$G_{1,p}(\omega) = -\frac{1}{Z_x(\omega)} \cdot \frac{1}{g_{m1} + g_p(\omega)} \times \begin{Bmatrix} g_{m1}\left(Y_{gd1}(\omega) Z_s(\omega) - 1\right) \\ + g_{mb1} c(\omega) Z_s(\omega) + b(\omega) Y_{gd1}(\omega) \end{Bmatrix} \tag{4.33}$$

$$G_{2,p}(\pm\omega_1,\mp\omega_2)$$
$$=\frac{\alpha(\pm\omega_1\mp\omega_2)}{Z_x(\pm\omega_1\mp\omega_2)}\times\begin{Bmatrix} g'_{m1}\left(A_1(\pm\omega_1)A_1(\mp\omega_2)-A_1(\pm\omega_1)B_1(\mp\omega_2)-B_1(\pm\omega_1)A_1(\mp\omega_2)\right)\\ +(g'_{m1}-g'_{mb1})B_1(\pm\omega_1)B_1(\mp\omega_2)+g_{mb1}D_2(\pm\omega_1,\mp\omega_2)\end{Bmatrix} \quad (4.34)$$

$$G_{3,p}(\pm\omega_1,\pm\omega_1,\mp\omega_2)$$
$$=\frac{\alpha(\pm2\omega_1\mp\omega_2)}{Z_x(\pm2\omega_1\mp\omega_2)}\times\begin{Bmatrix} g''_{m1}\begin{bmatrix} A_1^2(\pm\omega_1)A_1(\mp\omega_2)-B_1^2(\pm\omega_1)B_1(\mp\omega_2)\\ -3\left(2A_1^2(\pm\omega_1)B_1(\mp\omega_2)+A_1(\pm\omega_1)A_1(\mp\omega_2)B_1(\pm\omega_1)\right)\\ +3\left(2B_1^2(\pm\omega_1)A_1(\mp\omega_2)+B_1(\pm\omega_1)B_1(\mp\omega_2)A_1(\pm\omega_1)\right)\end{bmatrix}\\ +\frac{2}{3}g'_{m1}\begin{bmatrix} 2A_1(\pm\omega_1)A_2(\pm\omega_1,\mp\omega_2)+A_1(\mp\omega_2)A_2(\pm\omega_1,\pm\omega_1)\\ -2A_1(\pm\omega_1)B_2(\pm\omega_1,\mp\omega_2)-A_1(\mp\omega_2)B_2(\pm\omega_1,\pm\omega_1)\\ -2B_1(\pm\omega_1)A_2(\pm\omega_1,\mp\omega_2)-B_1(\mp\omega_2)A_2(\pm\omega_1,\pm\omega_1)\\ +2B_1(\pm\omega_1)B_2(\pm\omega_1,\mp\omega_2)+B_1(\mp\omega_2)B_2(\pm\omega_1,\pm\omega_1)\end{bmatrix}\\ -\frac{2}{3}g'_{mb1}\begin{bmatrix} 2B_1(\pm\omega_1)B_2(\pm\omega_1,\mp\omega_2)+B_1(\mp\omega_2)B_2(\pm\omega_1,\pm\omega_1)\\ -2B_1(\pm\omega_1)D_2(\pm\omega_1,\mp\omega_2)-B_1(\mp\omega_2)D_2(\pm\omega_1,\pm\omega_1)\end{bmatrix}\\ -g''_{mb1}B_1^2(\pm\omega_1)B_1(\mp\omega_2)\end{Bmatrix}. \quad (4.35)$$

Hence, by substituting (4.33) and (4.35) into (4.2), it is observed that IIP3 of the transconductor can be improved substantially by reducing the magnitude of the third-order harmonic Volterra operator $G_{3,p}(\pm\omega_1,\pm\omega_1,\mp\omega_2)$. Clearly, (4.35) shows that the linearity performance of the transconductor is limited by the first term in the numerator bracket; that is the direct distortion from the composite g''_{m1} and the second term is the feedback interact distortion component by the first- and second-order products with the intrinsic second-order nonlinear term g'_{m1} of the input transistors. The third term is an additional bulk interaction distortion which is formed by the proposed IM2 injection technique. The third-order bulk-transconductance nonlinearity distortion, g''_{mb1} in (4.35) is negligible as it contributes relatively low effect compared to the other distortion components.

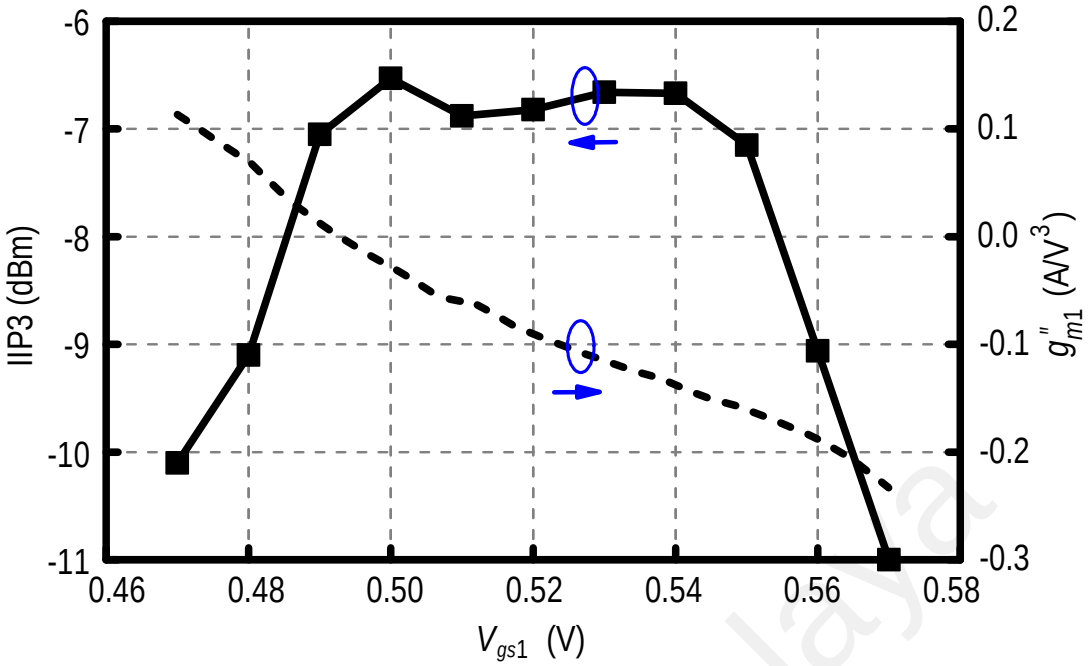
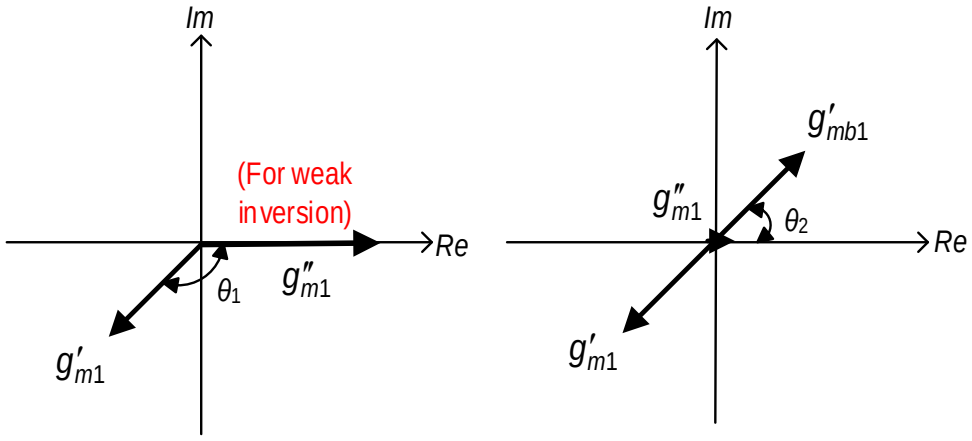


Figure 4.10: Simulated IIP3 and g''_{m1} of the input transistor $M_{1,2}$ without integrating IM2 circuit relating to its gate-source voltage V_{gs1}

By solving the third-order $G_{3,p}(\pm\omega_1,\pm\omega_1,\mp\omega_2)$ kernel using mathematic tools such as Mathematica or Maple, the close-form expressions can be obtained, where this mathematical relation is inscrutable as it is lengthy. Thus, the characteristic of this circuit is best described graphically by the vector diagram obtained through this expressions using the mathematical tool.

In this work, the intrinsic third-order nonlinearity is eliminated by nullifying the composite g''_{m1}, which is achieved by setting the gate bias of input transistors at g''_{m1} equal to zero. Figure 4.10 shows the IIP3 behaviour of the ISD transconductor for an aspect ratio of 60µm/0.13µm with stacked switching and IF stages. However, the IIP3 does not exhibit significant improvement at the sweet spot of V_{gs1} = 0.49 V due to the second-order nonlinearity of the input transistor, g'_{m1} which contributes IMD3 as explained in Section II. Therefore, an IM2 injection technique is also implemented to



(a) **(b)**

Figure 4.11: Vector diagram for the components of $G_3(\pm\omega_1,\pm\omega_1,\mp\omega_2)$ for (a) conventional ISD transconductor, and (b) proposed ISD transconductor

suppress the third-order nonlinearity distortion current which arise due to the feedback effect.

The generated g'_{m1} nonlinear distortion is mainly caused by the gate-drain capacitance and degenerated inductance. Hence, the angle of θ_1 in Figure 4.11(a) is relaxed from the parametric variation of R_1 and C_1. By adjusting R_1 and C_1 defined through the term g'_{mb1}, a collinear relationship is established with the vector of the second-order distortion produced by g'_{m1} with a fixed value of the input device size and L_s. As shown in Figure 4.11(b), the imaginary and real part of g'_{mb1} contribution is adjusted such that it is out-of-phase with the second-order contribution of g'_{m1}.

Initially, the aspect ratio of $M_{3,4}$ is set to achieve an accurate input impedance matching by setting its gate capacitance equal to that of $M_{1,2}$. Thus, the DC bias of $M_{3,4}$, R_1 and C_1 are chosen appropriately to give the desired IM2 amplitude and phase, while setting the gate bias of M_1 (V_{gs1} = 0.49 V) to the sweet spot point. To validate the Volterra analysis, an extensive set of simulation is done using Cadence SpectreRF simulator. The graph in

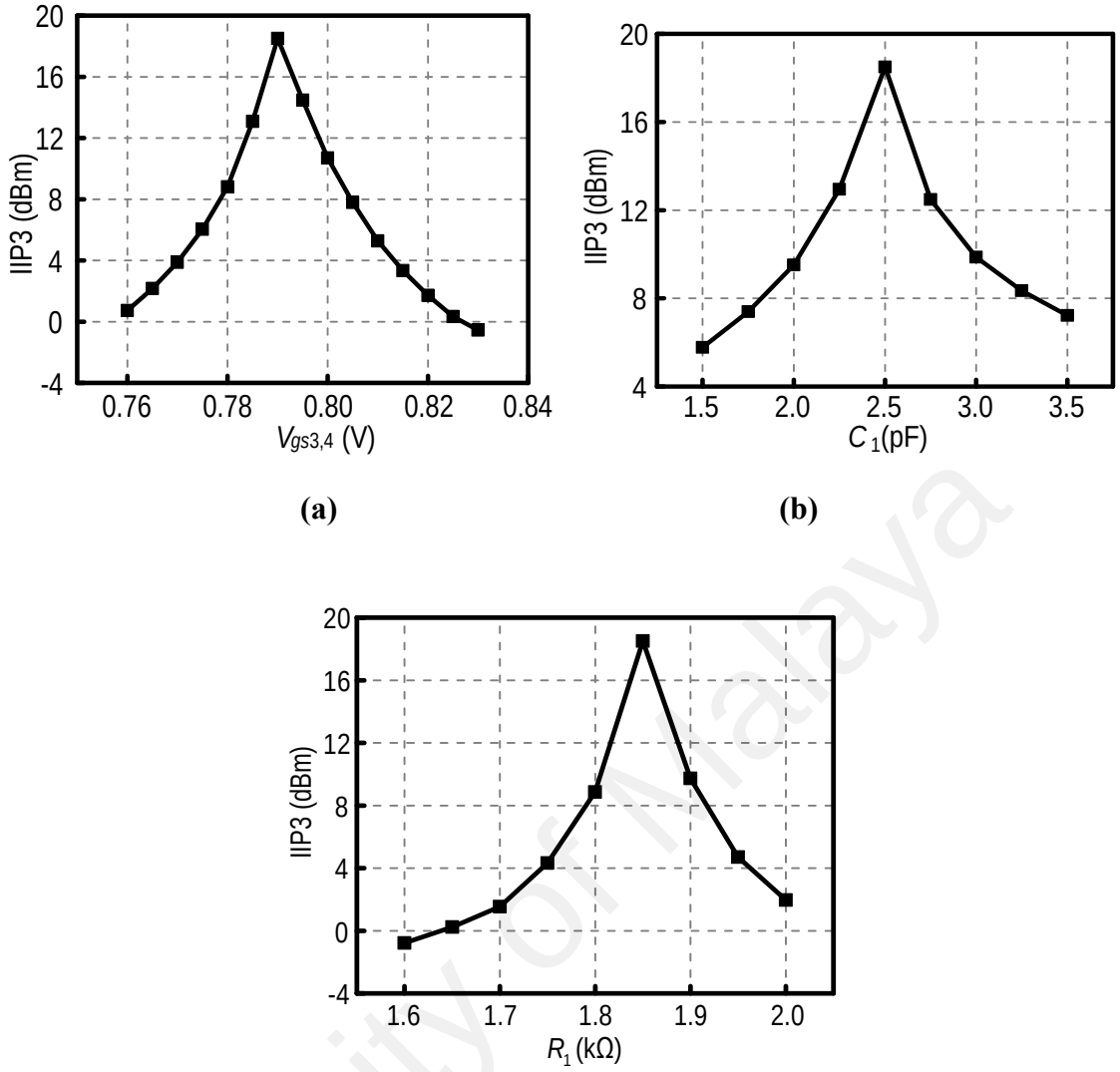


Figure 4.12: Simulated plots of (a) IIP3 versus $V_{gs3,4}$ at constant C_1 = 2.5 pF, R_1 = 1.85 kΩ, (b) IIP3 versus capacitor C_1 at constant $V_{gs3,4}$ = 0.79 V, R_1 = 1.85 kΩ, and (c) IIP3 versus resistor R_1 at constant $V_{gs3,4}$ = 0.79 V, C_1 = 2.5 pF

Figure 4.12 shows that the maximum IIP3 appears at a gate bias voltage, $V_{gs3,4}$ of 0.79 V with capacitance C_1 = 2.5 pF and resistance, R_1 = 1.85 kΩ. However, this technique is frequency dependent and the phase shift of IM2 injection would limit the linearity improvement. Therefore, it is more suitable for a narrow-band circuit with small two-tone spacing.

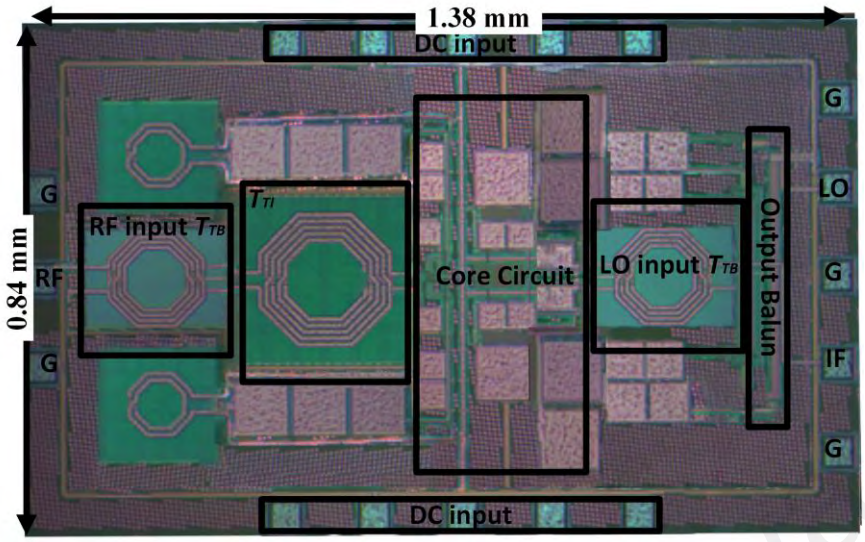


Figure 4.13: Microphotograph of proposed LNA-mixer

Table 4.1: Circuit parameters of the proposed balun-LNA-mixer.

Parameter	T_{TB}+T_{TI}+IM2 Injection Circuit	Parameter	T_{TB}+T_{TI}+IM2 Injection Circuit
$(W/L)_{1,2}$ (μm/μm)	60/0.13	R_L (Ω)	500
$(W/L)_{3,4}$ (μm/μm)	60/0.13	L_s (nH)	0.7
$(W/L)_{5\text{-}8}$ (μm/μm)	40/0.13	R_1 (Ω)	1850
$(W/L)_{9,10}$ (μm/μm)	70/0.13	C_1 (pF)	2.5
k_1	0.78	C_L (pF)	1.5
k_2	0.76	L_{TBp}/L_{TBs} (nH)	3.26/3.28
Q_{TBp}/Q_{TBs}	11.0/9.8	L_{TI1}/L_{TI2} (nH)	4.22/4.22
Q_{TI}	10.3	P_{DC} (mW)	1.2V@3.15 mW

The gate-input feedback effect can also be eliminated due to the differential nature of the transformer balun, which cancels out the even-order distortion current at the gate of the transistor $M_{1,2}$ by transforming it back to the input in antiphase.

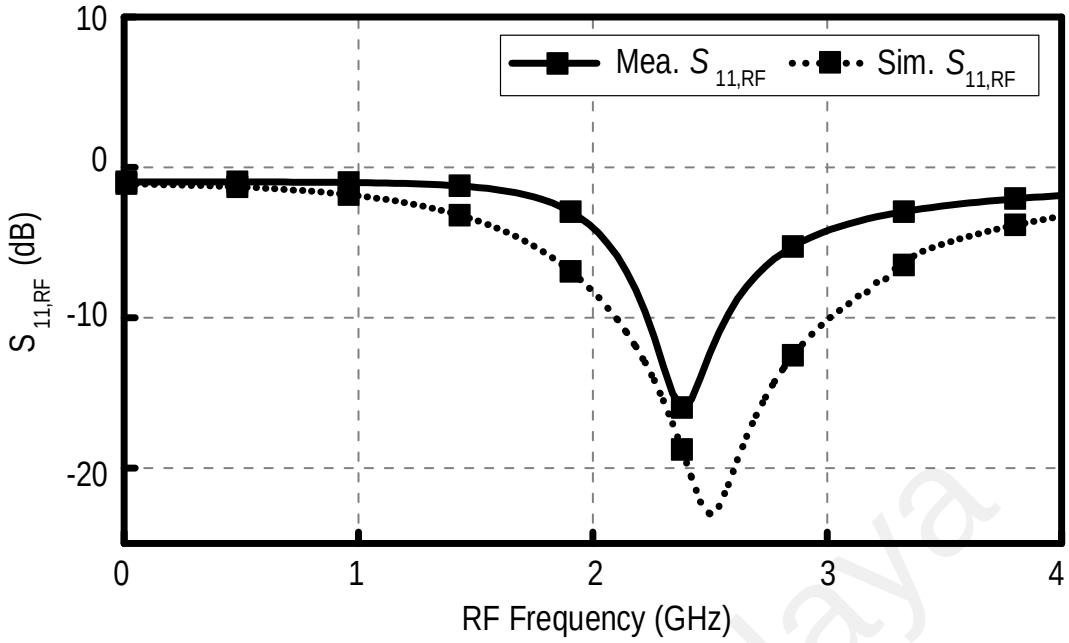
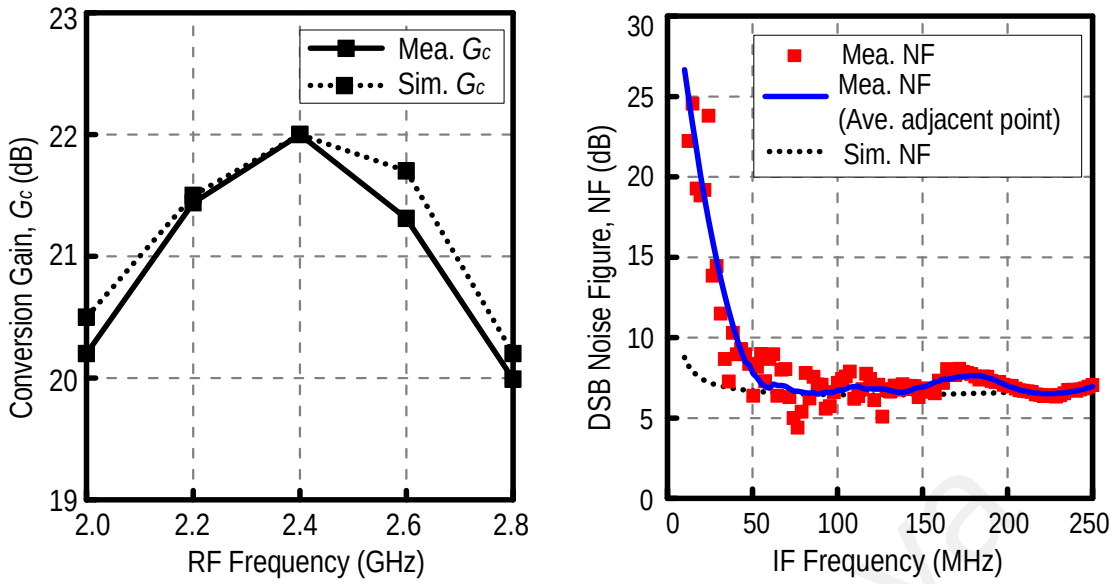


Figure 4.14: Measured and simulated of input return loss (S_{11}) of the RF port

4.4 Simulation and Measurement Results

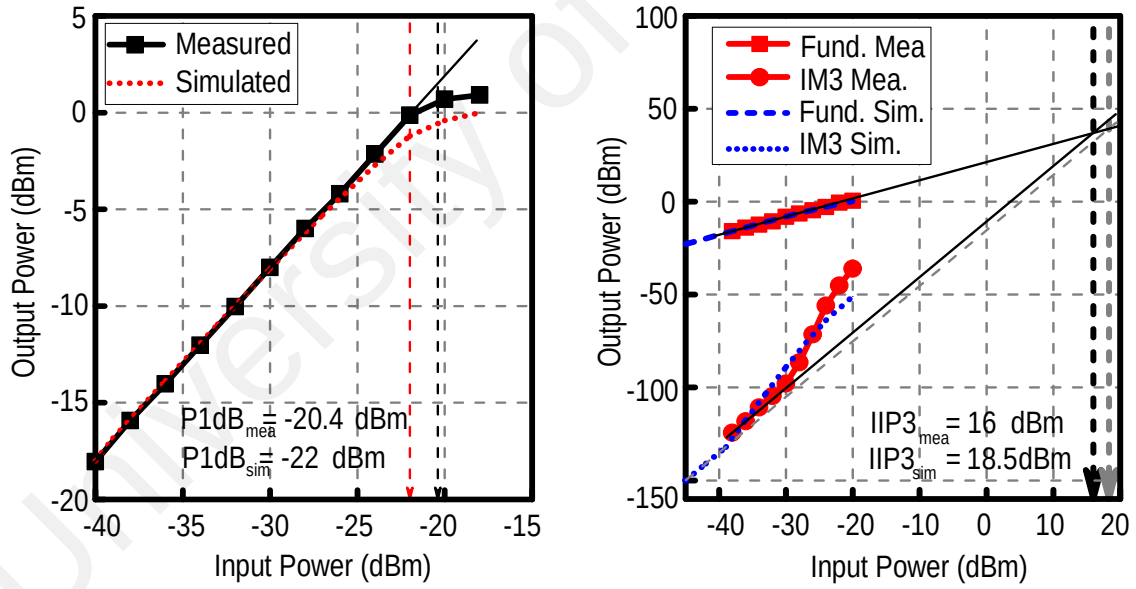
Based on the extensive analysis, a highly linear balun-LNA-mixer is implemented with 130nm CMOS technology by Global Foundries. The microphotograph of the proposed architecture is shown in Figure 4.13, with a total area of 1.16 mm^2, which includes the pad and the output active balun. The chip is measured through on-chip wafer probing and similar measurement setups as explained in Section 3.4 were used to characterize the performance. In this characterization, an active balun (not shown for conciseness) is integrated at the output of the LNA-mixer to convert the differential IF signals into a single-ended output with a 50 Ω matching. The input port is single-ended and matched to the 50 Ω characteristic impedance of the system and enabled the integration of single-ended front-end antenna to the balun-LNA-mixer circuit. The design parameters of the proposed balun-LNA-mixer are summarized in Table 4.1.

The core balun-LNA-mixer and the squaring circuit consumes 3.15 mW of power at 1.2 V. Figure 4.14 shows the input reflection coefficient at the RF port, which is <-10 dB at the desired frequency. The measurement and a comparative simulation of G_c versus



(a) **(b)**

Figure 4.15: Measured and simulated (a) conversion gain versus RF frequency, and (b) DSB noise figure versus IF frequency



(a) **(b)**

Figure 4.16:. Measured and simulated (a) P1dB and (b) two-tone IIP3 results

RF frequency is performed for a fixed IF of 100 MHz at a LO power of 0 dBm. As presented in Figure 3.15(a), the simulated and measured power G_c is 22 dB. Figure 4.15(b) illustrates the simulated and measured NF_{DSB} as a function of IF frequency. The

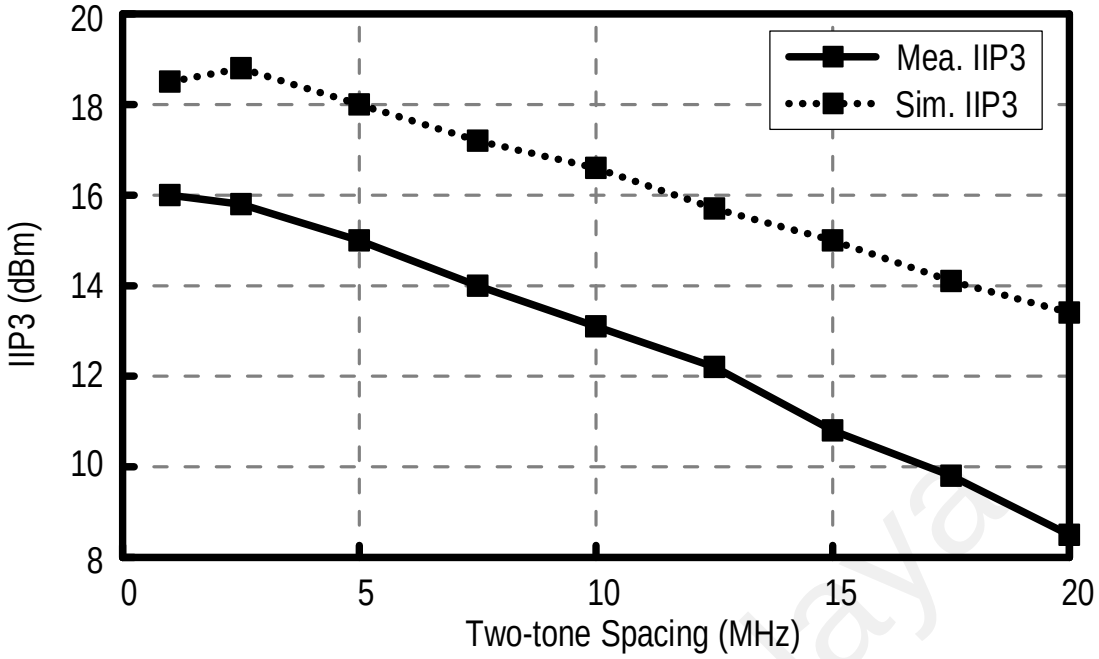


Figure 4.17: Measured and simulated IIP3 versus two-tone spacing.

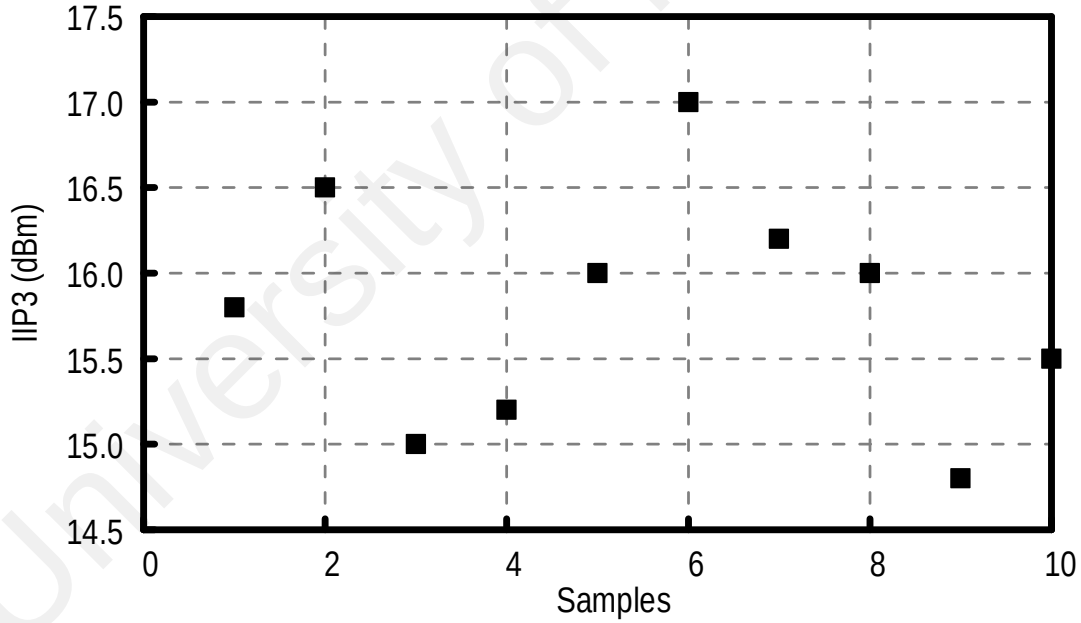
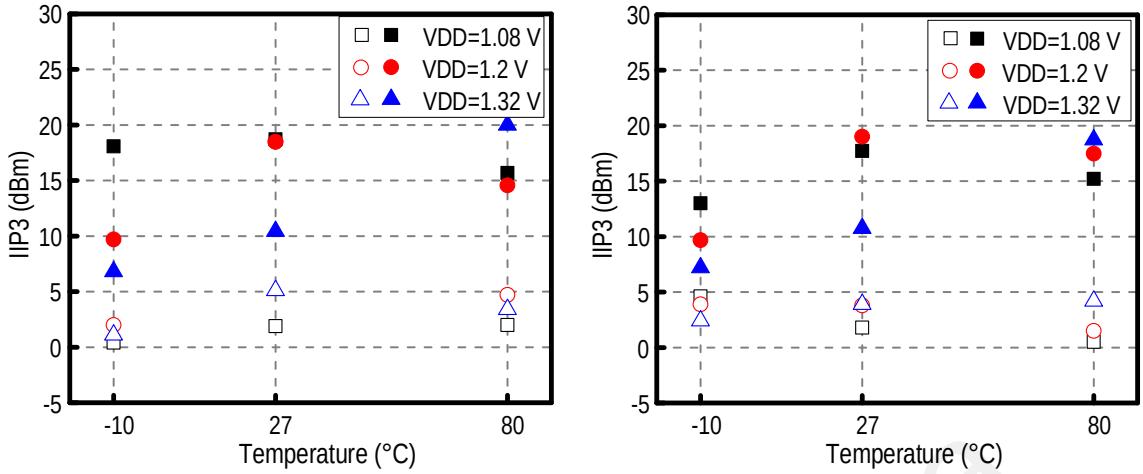


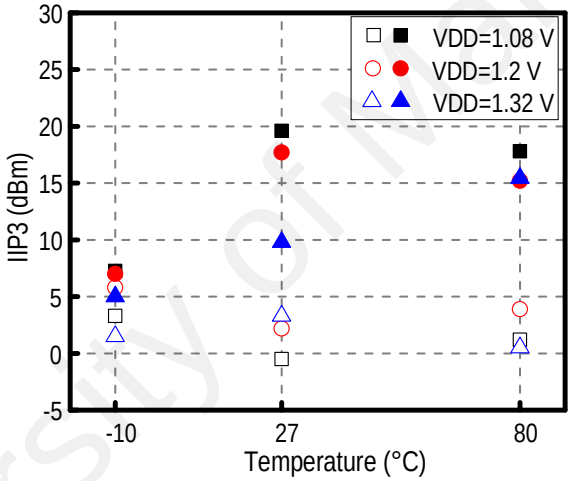
Figure 4.18: Measured IIP3 over ten samples.

NF is 7.2 dB at the output IF frequency of 100 MHz.

Figure 4.16(a) shows that the measured and simulated P1dB of -22 dBm and -20.4 dBm, respectively at the input RF frequency of 2.4 GHz. A two tone RF signal at 2.4 GHz and 2.401 GHz with 1 MHz frequency offset is applied to extract the IIP3 performance.



(a) **(b)**



(c)

Figure 4.19: Simulated IIP3 with PVT variations: (a) typical corner, (b) slow-slow corner, and (c) fast-fast corner. The open symbol represents uncalibrated IIP3 and solid symbol represents calibrated IIP3.

Figure 4.16(b) depicts the output power against input power for both fundamental and third-order intermodulation components, resulting in an IIP3 of +16 dBm. As the IM3 suppression is dependent on the two-tone spacing ω_2-ω_1, IIP3 results would vary under different two-tone spacing frequency as depicted in Figure 4.17. An increase in frequency space causes a decrease in IIP3 performance.

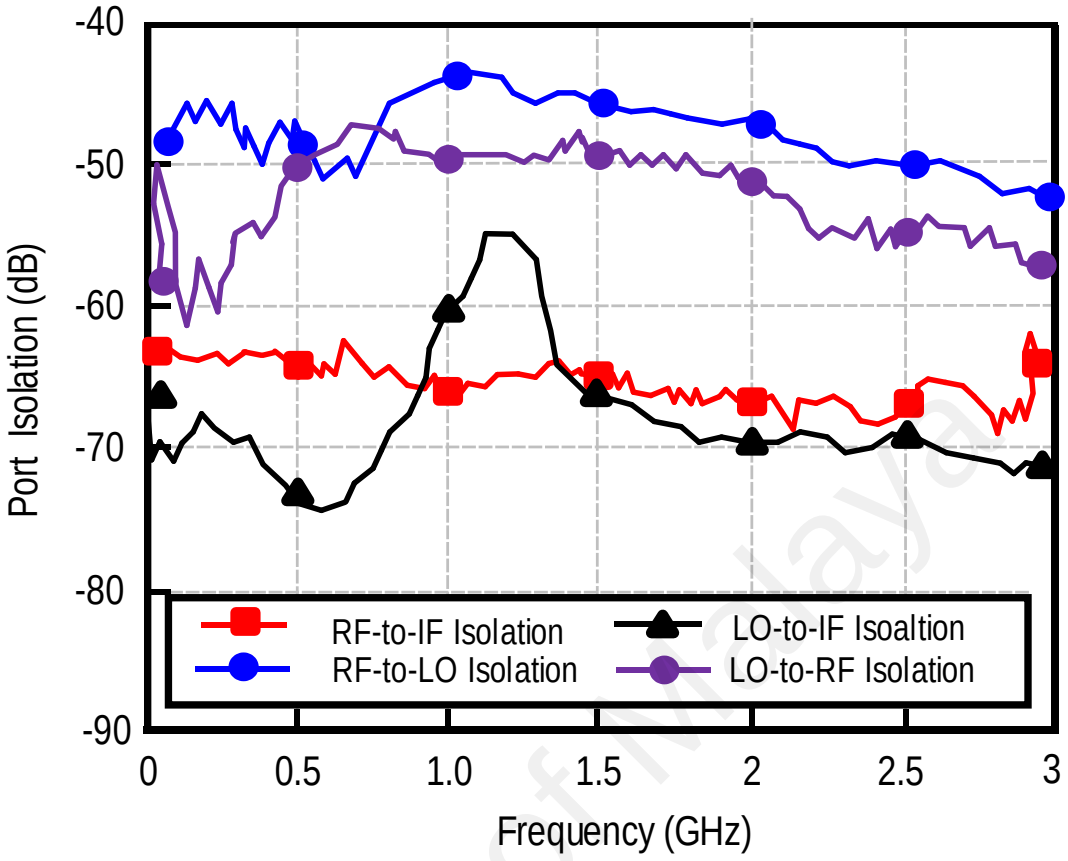


Figure 4.20: Measured port-to-port isolation.

Figure 4.18 shows the measured IIP3 for a sample of 10 chips at the operating frequency of 2.4 GHz, where the gate bias voltage of $M_{1,2}$ and $M_{3,4}$ are adjusted externally to maintain the desired IIP3 performance.

In addition, Figure 4.19 displays the simulated performance of the uncalibrated and calibrated IIP3 for various PVT (process, voltage, temperature) condition at 2.4 GHz. As expected, the optimum gate biasing technique is sensitive to the PVT variation. After applying the external gate-bias voltage calibration for both transistors $M_{1,2}$ and $M_{3,4}$, can be deduced that all the obtained IIP3 is significantly improved. Figure 4.20 representing port-to-port isolation of the proposed front-end receiver architecture.

Table 4.2 summarizes the performance of the proposed highly linear balun-LNA-mixer. The comparison with prior reported works proximating at the same operating frequency

in CMOS technology is tabulated adopting the FOMs in equations (1.1) and (1.2). The presented architecture strikes a good balance between G_c, NF, linearity, and power consumption. Therefore, it achieves a superior FOM with only 0.36 mW of additional power consumption from the squaring circuit.

4.5 Conclusions

This thesis presents a novel solution to improve the linearity of the conventional ISD transconductance stage by implementing both the optimum biasing and the IM2 injection techniques. The optimum biasing technique was employed in the input transistors to set the second-order derivative transconductance to zero. The use of the IM2 injection technique at the bulk of the input transistors suppresses the second-order feedback components. The measurement result in 0.13 μm CMOS process at 2.4 GHz shows that the differential balun-LNA-mixer only dissipates 3.15 mW of power from 1.2 V power supply with an NF of 7.2 dB, a G_c of 22 dB, an IIP3 of +16 dBm, and a P1dB of -20.4 dBm with no off-chip components required. Comparing with the state- of-the-art architecture, this work presents a high linearity, high G_c and low power consumption solution.

Table 4.2: Performance summary and comparison.

Reference	Process (μm)	RF (GHz)	G_c (dB)	NF (dB)	P1dB (dBm)	IIP3 (dBm)	V_{DD} (V)	P_{DC} (mW)	FOM1	FOM2	Topology	Circuit
(Asghari & Yavari, 2016)**	0.09	2.4	9.8	15.0	N/A	+15.7	1.2	5.8	-14.9	-15.7	Fully-differential	Mixer
(Mollaalipour & Miar-Naimi 2016)**	0.18	2.4	6.7	17.0	N/A	+9.0	1.6	4.6	-20.8	-22.8	Fully-differential	Mixer
(Asghari & Yavari, 2014)**	0.09	2.4	22.1	13.2	N/A	+17.1	1.0	4.0	-4.6	-4.6	Fully-differential	Mixer
(Bhatt et al., 2014)**	0.18	2.4	5.0	27.0*	N/A	+9.0	1.8	23.76	-38.7	-41.3	Fully-differential	Mixer
(Chong et al., 2014)**	0.13	2.4	22.3	7.2	-22.3	-10.8	0.5	0.91	-6.0	-3.0	Fully-differential	LNA+Mixer
(Silva et al., 2019)	0.13	2.4	42	7.2	N/A	-17	1.2	1.7	-2.0	-2.8	Single-ended RF input	RX
(Syu et al., 2013)	0.18	2.4	31	3	N/A	-10	1.8	9	-7.0	-9.6	Single-ended RF input	Subharmonic front-end RX
This work	**0.13**	**2.4**	**22.0**	**7.2***	**-20.4**	**+16.0**	**1.2**	**3.15**	1.8	**1.03**	**Single-ended RF input**	**Balun+LNA+Mixer**

*DSB noise **Simulated results †Estimated from graph

CHAPTER 5: CONCLUSION AND FUTURE WORK

5.1 Conclusion

In this thesis, two different conventional transconductors have been investigated, which are the CCC common-gate and ISD common-source topologies and subsequently implemented high linear circuit techniques to increase the linearity of the RF front-end receiver circuits without sacrificing other performance metric for wireless applications in 130 nm CMOS technology. These circuits are mainly designed to meet the future and current wireless communication standard of 802.11b/g& ah at 2.4 GHz and 900 MHz, respectively.

The first design is the optimized CCC common-gate topology. The reduction of the second-order harmonics in the CCC common-gate topology, along with second capacitive feedback leads the transconductor to be highly linear. The additional third feedback which composes by the positive feedback scheme helps in relaxing the constraint reliance in the conventional DCCC common-gate transconductor, while improving conversion gain, noise, and linearity, simultaneously. The proposed multiple feedback transcondcutor has been realized into a transconductance stage of the differential folded- mixer at 900 MHz wireless application using 130 nm CMOS technology. The IIP3 reaches up to +12.5 dBm in a two-tone test; while a noise figure of 8.5 dB and conversion gain of 18.6 dB at IF frequency of 50 MHz is achieved. The proposed mixer consumes 3.15 mW from a 1.0 V supply.

The second design targets on the ISD common-source topology. Biasing the transistor at the highest possible overdrive voltage and using smaller input transistor size are conventional solutions in ISD common-source amplifier to reduce the IM3 distortion. The price that is paid for this performance enhancement is in the power consumption and it's not an effective solution for advanced CMOS technology due to the low supply voltage

and decrease in output resistance which leads contribution of the nonlinear output conductance and cross-term among v_{gs}, v_{ds} and v_{bs}. In line to the objectives that is highlighted earlier, this work provides a high performance balun-LNA-mixer circuit in CMOS 130 nm technology for 2.4 GHz wireless communication applications, with special attention being paid in achieving high transconductance stage linearity. Two innovative techniques to improve IM3 distortion in conventional ISD transconductance stage is proposed while considering its effect on other performances. First, an optimum biasing technique was employed for the input transistors to set the second-order derivative transconductance to zero. Second, an IM2 injection technique at the bulk of input transistors was utilized for the second-order feedback term suppression. This IM2 injection circuit with lower impedance-transformation transformer at the input transconductance stage leads to higher IIP3 value and better input-impedance matching, while retaining the conversion gain and NF. The transformer-based gate inductor at the input transistor ensures smaller active area and produces balanced differential input signal. The mathematical expressions for the input-impedance matching, conversion gain, NF and linearity, provide a guideline for designing a differential ISD LNA-mixer with high linearity at low power consumption. Measurement result shows that at 2.4 GHz, the differential LNA-mixer dissipates 3.15 mW from 1.2 V power supply and obtains a 7.2 dB noise figure, 22 dB conversion gain and 16 dBm third-order input-intercept point with a 1-dB compression point at -20.4 dBm. In addition, no off-chip components are required.

The benchmarking with other state-of-art work shows that both the proposed front-end circuit have a high conversion gain and low power consumption yet meeting the stringent linearity requirement of the future wireless demands, corresponding to a high FOMs. The nonlinear cancellation mechanism is also investigated and validated using the complex Volterra series analysis.

5.2 Future Works

Several improvements can be applied to each circuit to further enhance its performance further. For the mixer in Chapter 3, the large die area due to the four on-chip inductors should be eliminated by using off-chip inductors as adopted in (Han et al., 2015).

The off-chip calibration proposed is based on manual hand trimming, compensating the variation of IIP3 respective to the process corner. By assigning the transconductance stage itself to detect its output distortion and an integration of a feedback mechanism to adjust its individual bias voltages is much favored. This built-in self-test capability involves on-chip distortion sensing and associated mixed-mode signal processing. These techniques have been demonstrated in a work on spectral sensing of on-chip supply noise (Alon & Horowitz, 2008). Application of these techniques into the proposed LNA-mixer would be more viable and realistic for on-chip calibration.

Besides, the RF front-end receiver presented in this thesis is only part of the entire receiver system. To complete the receiver chain, an on-chip voltage-controlled oscillator (VCO) to generate the LO signal, variable gain amplifier (VGA) with automatic gain control, and the ADC blocks should also be integrated.

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