DESIGN AND FABRICATION OF LOW POWER DIFFERENTIAL LOW NOISE AMPLIFIER FOR WLAN APPLICATION IN DEEP SUB-MICRON STANDARD CMOS TECHNOLOGY

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THESIS SUBMITTED IN FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

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ABSTRACT

This thesis presents the design and implementation of low power differential low noise amplifier for wireless local area network application. The operating frequency was designed at 2.4 GHz with a supply headroom of 1.2 V and implemented on Silterra's 0.13µm RF CMOS process. A detailed methodology that leads to a power efficient design of the circuit is presented. Then, a comprehensive circuit analysis and design methodology of the differential cascode topology, that is the differential Power-Constrained Simultaneous Noise and Input Matching low noise amplifier. A theoretical noise figure optimization using fixed power and physics-based characteristics were used as a design optimization guide. Simultaneous noise and input matching under constrained power was achieved with an extra gate source capacitor while gain enhancement was obtained by employing a capacitive feedback at the cascode transistor. Scattering parameter measurement of differential four-port networks low noise amplifier requires a four-port vector network analyzer. Thus, a measurement technique that enables very accurate measurement for S-parameter of differential low noise amplifier by means of a standard two-port vector network analyzer is presented. This technique involves by terminating two ports at one time while another two ports are measured. Apart from that, a general noise figure de-embedding technique also presented in this thesis. De-embedding noise figure measurement of a differential low-noise amplifier based on the analysis of two gain definitions. The effects of impedance match on noise figure are investigated. The result shows a noise figure of 0.57 dB obtained with the de-embedding technique and 1.2 dB without the de-embedding technique. Noise figure was measured under three different source impedances namely short, open and load.

The end-design of the optimized differential low noise amplifier produces a power gain of 17.12dB with a dc power consumption of 7.2mW. A linearity of -10.5 dBm

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achieved. The LNA has been experimentally verified for its functionality and results a validated peak the performance at 2.4 GHz of operating frequency.

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ABSTRAK

Tesis ini membentangkan reka bentuk dan pelaksanaan penguat bunyi hingar rendah bagi aplikasi rangkaian kawasan tanpa wayar. Kekerapan operasi ialah 2.4 GHz dengan voltan bekalan 1.2 V dan dilaksanakan pada proses CMOS CM 0.13μm Silterra. Kaedah terperinci yang membawa kepada reka bentuk litar kuasa litar dibentangkan. Ini diikuti oleh analisis litar yang komprehensif, metodologi reka bentuk dan perbandingan prestasi topologi cascode yang berbeza, iaitu Kebarangkalian Serentak Kuasa dan Input yang sepadan dengan penguat bunyi yang rendah. Pengoptimuman angka bunyi bising teori menggunakan ciri tetap dan ciri berasaskan fizik telah digunakan sebagai panduan pengoptimuman reka bentuk. Kebetulan serentak dan pencocokan input di bawah kuasa yang dikekang telah dicapai dengan kapasitor tambahan pintu gerbang sementara mendapat peningkatan diperolehi dengan menggunakan maklum balas kapasitif pada transistor cascode.

Pengukuran parameter pengukuran perbezaan empat-port rangkaian penguat bunyi rendah memerlukan penganalisis rangkaian vektor empat-port. Oleh itu, teknik pengukuran yang membolehkan pengukuran yang sangat tepat untuk parameter S-parameter penguat bunyi kebisingan rendah dengan cara penganalisis rangkaian vektor dua-port piawai dibentangkan. Teknik ini melibatkan dengan menamatkan dua port pada satu masa manakala dua pelabuhan lain diukur. Selain daripada itu, teknik bunyi de-embedding umum juga dibentangkan dalam tesis ini. Mengurangkan pengukuran angka hingar bagi penguat kebisingan rendah berdasarkan analisis dua definisi keuntungan. Kesan padanan impedans pada angka bunyi disiasat. Hasilnya menunjukkan angka kebisingan 0.57 dB yang diperoleh dengan teknik de-embedding dan 1.2 dB tanpa teknik de-embedding. Angka kebisingan diukur di bawah tiga impedans sumber yang berbeza iaitu pendek, terbuka dan beban.

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Reka bentuk akhir pengubah bunyi bising rendah yang dioptimumkan menghasilkan keuntungan kuasa 17.12dB dengan penggunaan kuasa 7.2 mWatt. Linearity biasanya diukur dari segi titik memintas input ketiga, IIP3 dan LNA mempunyai IIP3 dari -10.5 dBm. LNA telah disahkan eksperimen untuk fungsinya dan keputusan mengesahkan puncak prestasi pada 2.4 GHz.

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LIST OF SYMBOLS AND ABBREVIATIONS

Ω	Ohm
γ	Noise parameter
α	Noise parameter
χ	Noise parameter that includes both correlated and uncorrelated portions of the transistor's gate noise
μ_n	Mobility of electron
μ_p	Mobility of hole
δ	Coefficient of gate noise
κ	Noise parameter of the correlated portion of the transistor's gate noise
ε_o	Permittivity of free space, $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m
λ	Wavelength of the frequency of operation
ξ	Noise parameter of the uncorrelated portion of the transistor's gate noise
ω_o	The resonant frequency
ω_T	Transition angular frequency
A_v	Voltage gain
A_{vo}	Open-circuit voltage gain
CG	Common Gate
CS	Common Source
MAC	Media Access Control
RF	Radiofrequency
S_{11}	Input reverse isolation
S_{22}	Output reverse isolation

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S_{12}	Isolation
S_{21}	Gain
NF	Noise Figure
K_f	Stability Factor
LNA	Low Noise Amplifier
LO	Local Oscillator
SNR	Signal to Noise ratio
PCSNIM	Power-Constrained Simultaneously Noise Input Matching
SNIM	Simultaneously Noise Input Matching
T_{ox}	Oxide Thickness
WLAN	Wireless Local Area Network

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CHAPTER 1: INTRODUCTION

1.1 Background

Wireless communication technologies have great influence on many society activities, including in the case daily cellphone, wireless local area network (WLAN), Bluetooth, etc. Along with the increase in the competition in wireless market, the existing gadget with the basic function cannot fulfill the requirements of modern wireless communication system (Yan, Chen, Yang, Zhang, & Lin, 2017). The performance requirements such as low cost, high efficiency and reliability becomes increasingly important (Koutsoyannopoulos & Papananos, 2000). Low noise amplifier (LNA) is the first block of any receiver system for wireless communication. It is used in the receiver frontend of communication systems to amplify very weak signals captured by an antenna while adding as little noise and distortion as possible. Noise figure (NF) of LNAs is a key parameter since it determines the overall noise performance of receivers due to this fact, the LNA is considered as one of the most important stage to be considered (Yan et al., 2017) .

1.2 Motivation

Wireless communication systems are rapidly developing in the last few decades. Due to the fast-growing demands in the wireless consumer electronic devices, there is a huge demand for low power, portable, battery-operated electronic devices such as mobile phones, tablet and laptop computers. The rapid development in the wireless technology introduces new design issues and challenges such a low power, low cost and small chip area. This provides the motivation for further research towards achieving higher on chip integration and lower power consumption (Hayati, Cheraghaliei, & Zarghami, 2017) .

LNA is considered as one of the most important stage to be designed. It is one of the most critical blocks in radio frequency (RF) transceiver. Thus, it is very important for

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the LNA to be performing well in order to provide the following stages with good signals to process. Current market trend that require for low power device portrays challenges to LNA design in containing sufficient voltage gain, low noise figure, high linearity, smaller area and low power consumption at the same time (Tu et al., 2005) .

1.3 Problem Statement

The low-noise amplifier (LNA) is a electronic amplifier used to amplify low sensitivity signals. LNA is an important block, which is located at the front-end of a RF receiver circuit network. While the noise of the LNA itself is injected directly into the received signal, the noise of all the succeeding stages of the block is reduced by the gain of the LNA (Shankar & Dhas, 2014) . Therefore, it is essential for an LNA to optimize the desired signal power while adding as little noise as possible to the circuit. Wireless applications are almost by definition battery powered devices. Power consumption is therefore a major concern for the LNA. The focus of a design is to identify an LNA architecture which gives low power consumption without degrading other parameter's performance (Jusung et al., 2010).

Even though single-end input stage consumes less power and the active chip area consumption is minimum, differential topology is preferred for the following important issues (Zokaei, Amirabadi, & Ghasemzadeh, 2015). Firstly, since the noise figure is a critical factor for the low noise amplifier, the better noise performance of the differential stage is more popular due to the ability of rejecting the common-mode noise. Theoretically, the two sides of the circuit are identically matched and therefore the common-mode noise of each side can be viewed as the same. Secondly, not only limiting towards the noise but also for the linearity performance, the differential mode amplifier exhibits better performance (Das, Srivastava, Ananthapadmanabhan, Ahmad, & Baghini, 2016). Due to the inherent circuit architecture, which is symmetrical, the nature ability of

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cancelling the even-order distortions increases the linearity of the amplifier. Finally, in view of the integrated receiver, the differential LNA can relate to the subsequent circuits directly if the receiver topology is the image-rejection architecture. The balun can be integrated in front of the total front-end to keep the circuit integration.

In integrated analogue electronics and especially in RF applications, a fully differential approach is usually preferred, due to its well-known properties of immunity to common-mode disturbances, rejection to parasitic couplings and increased dynamic range (Ganesan, Sanchez-Sinencio, & Silva-Martinez, 2006). Although the differential operation must be preserved in the chip, there are cases where the input signal is single-ended such as RF image filters and IF filters in a RF receiver. In addition, there are circuits that require differential signals to perform their function. In these situations, a stage which is able to convert single-ended to differential signals is needed. Several highly integrated direct-conversion CMOS front-ends achieve high performance, but at the cost of requiring a fully differential LNA that needs two RF input pins and an external RF single-ended to differential conversion (Feng, Takemura, Kawaguchi, & Kinget, 2009). This typically requires special front-end filters or an additional off-chip balun, which can incur extra loss and can degrade the system noise figure.

An important issue that should be taken into consideration is the linearity of the low noise amplifier. Linearity is important to get minimize the output distortion output. Nevertheless, there is always a tradeoff between gain and linearity. Based on (Mazhab Jafari & Yavari, 2015), a differential LNA is better to be implemented in a mixed-mode design where a single-ended LNA is prone to be affected by substrate noise and other interferers on chip of the receiving block. LNA linearization techniques should keep gain, noise figure and input matching while consuming minimum power and die area. Hence, it is a big design challenge and the most of linearization techniques for baseband circuits

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isn't applicable for LNA and requires innovative methods (Jafarnejad, Jannesari, & Sobhi, 2017).

1.4 Aim and Objectives

The aim of this thesis is to study different architectures of LNA designs for front-end receiver WLAN application and design LNA that can be used in the frequency range of 1 to 4GHz. The following research objectives are included in the design in line to the problem statement reviewed are:

- Study on possible techniques of narrowband LNA design and optimization for low power design for differential signal.
- Design a differential Low Noise Amplifier (LNA) with optimize noise figure and gain performances following the specifications set by IEEE 802.11g WLAN standard adopting 2.4GHz operating frequency with band range 1- 4 GHz.
- Develop and introduce a modified measurement method to characterize networks incorporating differential signal schemes and adopting de-embedding technique for efficient noise measurement.

The following are the contributions from the accomplishments of this project:

a. An improved differential LNA design with Power Constraint Simultaneous Noise Input Matching (PCSNIM) using Power Constraint Noise Optimization (PCNO) technique was designed.
b. A systematic methodology on designing the PCSNIM LNA was offered. The methodology starts from the requirement of the standard specifications, then by derivations for the gain, noise and S-parameters of the design, the calculations for the components and lastly the on-wafer chip measurement.

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c. An on-wafer measurement method for differential LNA by using conventional two port network and adopting a de-embedded technique for noise reduction was presented.

1.5 Thesis Outline

This thesis is structured as follows:

Chapter 2 - Literature review section explains the background on the wireless standard of the LNA's in this research. Prior to designing the LNA, specifications of the standard and CMOS LNA design topologies are specified in this chapter. Specifications requirement of the wireless standard becomes the reference for the LNA's performance. In this research work, the LNA is intended for the Wireless Local Area Network application and the receiver is the direct conversion type. This is due to to the high integration level that it is capable of. High level of integration in a transceiver architecture is very crucial especially in wireless systems. This section also presents numerous LNA topologies, performance metrices and techniques in designing LNAs. LNA with its design objectives and functions were also explained also in this section together with the different amplifier topologies available. Finally, the gain, S-parameters, linearity and noise figure definitions and descriptions are given in this section for the LNA performance metrics.

Chapter 3 – Project Design Methodology. This chapter highlights the methodology in designing LNA that engaged in this study. It starts with a explanation on the power constrained noise figure optimization method to provide the LNA transistor's width that can lead to the best noise performance. The methodologies in designing the SNIM, PCSNIM and new PCSNIM with differential inductor LNAs are systematically explained in this chapter. In this research work, the LNA were simulated, fabricated and measured.

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Chapter 4 - Results and discussion section discusses highlights the findings obtained from this work. Simulations for the pre and post-layout design were done and comparisons between the both were present. The differences also explained in this chapter. Simulated performances of the LNAs are compared with the specifications imposed by the WLAN standard. Measurement test setup of the single and differential input LNA are explained. Then, the measurement results on the several experiments performed on the PCSNIM LNA discussed in this chapter.

Chapter 5 – Conclusion and future work. In this section, the work presented in this thesis is concluded and reaffirmed. Finally, the direction of future research is discussed which contains future work that can be achieved to further improvement the design circuit.

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CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

Low noise amplifier (LNA) is the backbone of wireless communication receivers as it is the first stage in the receiver path. Its main purpose is to amplify the input signal level, while at the same time minimizing the addition of the noise figure (NF) of the whole receiver system. LNA provides enough gain to the input signal to enable the signal to tolerate the noise of the subsequent stages yet maintaining very minimum noise to the signal (Shaeffer & Lee, 1996). If the LNA has low gain, the signal will be more susceptible to higher noise contributions from the stages following the LNA. The two tasks of providing high gain and low noise are not always easily achieved simultaneously, the main reason due to noise and input impedance matching and the input impedance matching are not obtained as for the same source impedance.

In a direct conversion receiver (DCR), the LNA provides most of the gain before the signal is down converted to baseband. Hence, the LNA is required to provide high gain without degrading its linearity. In DCR, the gain of the LNA is limited by the stringent linearity requirements. Although high gain is good to amplify the weak signals, it will be disastrous if the signals are strong. High gain under strong input signal condition is undesirable because of saturation or distortion (Receiver, Zolfaghari, & Razavi, 2003).

Common-source configuration is the most commonly used topology in the design of an LNA as it provides low noise figure. A modification to this configuration is the cascode, which is also a very popular topology as it gives good stability and reverse isolation. Good reverse isolation is important for an LNA in a DCR as the local oscillator (LO), which typically is at the same frequency as the signal of interest, is in the mixer stage which is directly connected to the output of the LNA. A good reverse isolation LNA can mitigate the possibility of LO leakage.

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2.2 CMOS LNA Design

LNA is the most crucial portion of a receiver front end. Numerous circuits with different topologies and architecture have been proposed for LNA, for various applications. Several methods have been proposed for LNA design and optimizations. In this section an overview of existing LNA circuits and design and optimization methods will be discussed.

The incoming wireless signal from the antenna is fed to the input of LNA, which is normally low in sensitivity in the region of -100dBm to -70dBm. The LNA needs to amplify the weak signal so that the following mixer can process it. Thus, the LNA needs to have a defined power gain. The noise generated by LNA is directly added in the signal in the amplifying procedure and reduces the signal to noise ratio (SNR) of the signal. In contrast, the noise contribution from the following stages of the receiver is attenuated by LNA gain. To satisfy the system noise requirement, the noise contribution from the LNA should not be large. Finally, due to the nonlinear performance of the LNA, the out-of-band signal can generate in-band interference, which will reduce the overall system linearity performance and dynamic region. Different metrics and topologies of the LNA are discussed in the following sections. LNA circuits in Complementary Metal Oxide Semiconductor (CMOS) technology are designed as Common Gate (CG) or Common Source (CS) configuration. Cascode stage that is widely used in CMOS RF LNAs, can be considered as current–reuse configuration of a CS stage, followed by a CG stage. For each application, some of LNA characteristics are more important than the others.

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2.3 WLAN Standard

Wireless local area network (WLAN) refer to a wireless network that can transmit data at high speeds. Designing LNA to be applied in WLAN application must follows the IEEE 802.11 standards. IEEE 802.11 is a set of media access control (MAC) and physical layer (PHY) specifications for WLAN. IEEE 802.11b, g, n is single band. They provide only the 2.4GHz band. IEEE 802.11g associations the best of both 802.11a and 802.11b bandwidth up to 54 Mbps, and it uses the 2.4 GHz frequency for greater range. The main differences between the 2.4 GHz and 5GHz wireless frequencies are range and bandwidth. 5GHz perform faster data rates with shorter distance. While the 2.4GHz wireless frequency gives coverage for larger distances but may provide at slower speeds. Table 2.1 illustrates the characteristic of IEEE 802.11 WLAN standard. Designing LNA will be based on this standard in order to set the design target and requirement.

Table 2.1: General characteristic of IEEE 802.11 WLAN Standard

Standard	Maximum Data Rate (Mbps)	Operating Frequency Band
802.11b	11	2.4 GHz
802.11g	54	2.4 GHz
802.11a	54	5 GHz
802.11n	600 (Theoretical Max)	2.4 GHz & 5 GHz

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Table 2.2 depicts the available IEEE 802.11 WLAN systems variant standard and bands. This specification is useful as a design guideline the frequency range for LNA design.

Table 2.2: IEEE 802.11 WLAN systems variant and bands

IEEE 802.11 variant	Frequency bands used
802.11ac	Below 6GHz
802.11ad	Up to 60 GHz
802.11af	TV white space (below 1 GHz)
802.11ah	700 MHz, 860MHz, 902 MHz, etc. ISM bands dependent upon country and allocations

2.4 LNA Topologies

Having discussed the WLAN standard for LNA application, this section will discuss the LNA topology. Common source (CS) and common gate (CG) are two commonly used topologies in CMOS LNA circuits. CS LNA has good noise performance and high gain (Nguyen et al., 2004). Inductive source degenerated architecture is the most common configuration of a CS. Inductor that placed in the source of CS topology affects the gain and noise performance of LNA. While the CG topology can gives to low power consumption and robust against parasitic but the disadvantage is that it has poor noise performance (Andreani, Sjoland, & Sjoland, 2001). Some methods, such as capacitive cross coupling, has been offered to improve the CG stage noise performance (Belmas, Hameau, & Fournier, 2012; Jafarnejad, Jannesari, Nabavi, & Sahafi, 2016) . Wideband input matching is possible for CG configuration and hence this configuration is extensively used in broadband LNA circuits (Keehr & Hajimiri, 2012; Lo & Kiang, 2011). However, CS configuration may be used in wideband applications adapting

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feedback circuits. Inductive source degenerated CS configuration is conventionally used in narrowband LNA circuits (Prameela & Elizabeth, 2016).

2.4.1 Common Gate Topology

Figure 2.1 illustrates the common gate (CG) topology. CG topology circuit has an input impedance of $1/g_m$. A suitable selection of the transistor size and bias current are needed in order to deliver the required 50 Ω. Although the poor gain response makes the CG topology less common for narrowband applications. It is often implemented in the wideband design applications since its input impedance over a wide band is about $1/G_m$, which is approximately close to 50 Ω. G_m is the effective transconductance, equal to g_m for simple CG stage. The noise factor, F is given by $F \geq 1 + \gamma / \alpha$ for the low frequency (Lee, Samavati, & Rategh, 2002). So, for long-channel devices, as $\gamma = 2 / 3$ and $\alpha = 1$. However, for short-channel devices, the NF will surge to 4.8 dB if γ / α is assumed to be 2. α will be less than 1(for short-channel devices) and γ is always taken as 2 to 3 times its value for long-channel (for short-channel devices).So that, usually γ is in the range of 1 to 2 for short channel devices (Shaeffer & Lee, 1996). The NF of CG stage is slightly high, but it is independent of ω and remains nearly constant irrespective of bandwidth.

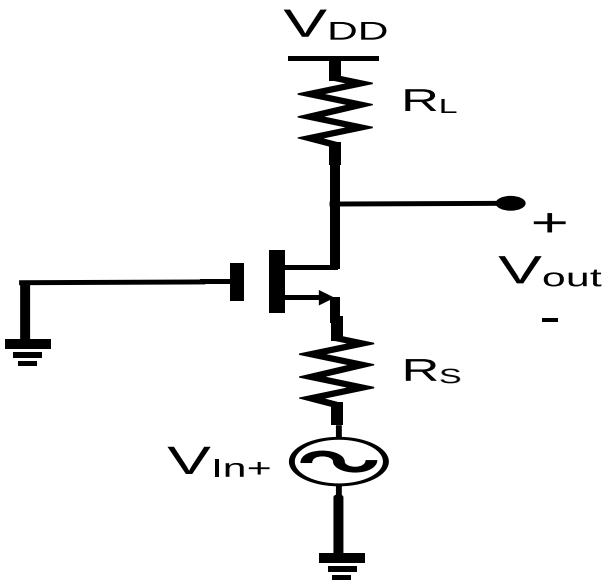

Figure 2.1: Common Gate Topology

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2.4.2 Common source topology

The common source (CS) topology is demonstrated in Figure 2.2. CS topology popular for narrow-band applications. This is due to its pre-amplification by the input matching series resonant network and superior noise performance. Since no physical resistor for matching and due to the 50 Ω, R_1 at the input, the CS amplifier topology circuit delivers practical 50 Ω termination (Shaeffer & Lee, 1997). The input parasitic is absorbed by resonate network, which is very thoughtful in inductively degenerated common source topology. The input impedance of the circuit is $Z_{in} = Z_1 // R_1$. The input impedance of the amplifier, Z_{in} is almost 50 Ω due to $R_1 = R_S = 50$ Ω and this will lead $Z_1 = 1 / sC_{gs}$ is much bigger than 50 Ω for frequencies up to a few GHz. Z_1 is the input impedance to the transistor. R_S is the source resistance and R_L is the load resistance. C_{gs} is the transistor's gate-source capacitance. The existence of R_1 will decrease the signal by a factor of 2 ahead of the transistor. The cause is understandable by viewing at the circuit topology given in Figure 2.2 and presented in equation below:

$$V_{gs} = \frac{(R_1 // -Z_1)}{(R_1 // +R_S)} V_{in} \qquad \textbf{(2.1)}$$

R_1 and Z_1, the V_{gs}, will be approximately half of the V_{in} ($R_1 // Z_1 \approx R_1 = 50$ Ω). Therefore, this category of topology tends to deliver very high NF contribute also from R_1 that increases the thermal noise. The noise factor of this circuit is $F \geq 2 + (4\gamma / \alpha)(1 / g_{mR})$ where $R = R_S = R_1$, γ is the noise parameter and $\alpha = g_m / g_{d0}$. g_m is the transistor's transconductance and g_{d0} is the transistor's drain-source conductance at 0 V_{DS} (Lee et al., 2002). The term noise factor, F is for operating in low frequency applications (not including the gate noise).

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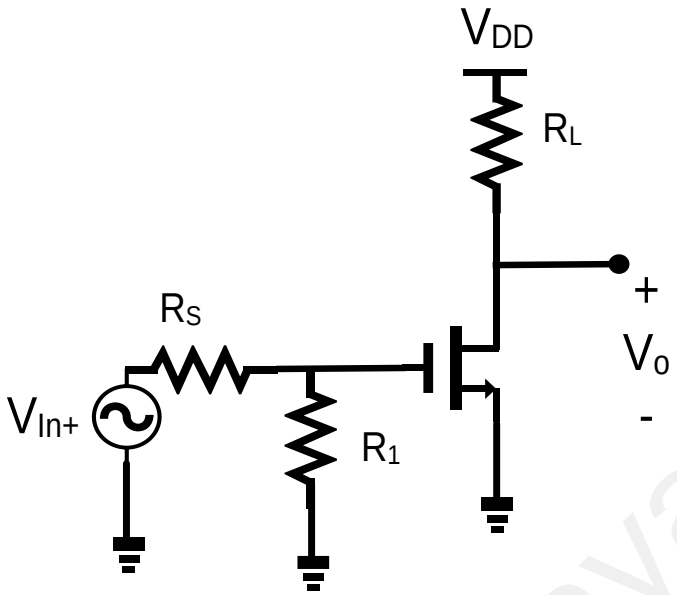

Figure 2.2: Common source topology

2.4.3 Shunt series Topology

The shunt series amplifier topology illustrated in Figure 2.3 . This topology can give real input impedance for broadband application. It has good NF performance by not decreasing the input signal with noisy attenuator before amplifying it. Due to the presence the of the resistive feedback, Rf, this shunt-series generates thermal noise. Even though it faced less problems than the CS with shunt input resistor. This topology does not have an impedance equals to the maximum source impedance of the noise, Z_{opt}, at any frequency. $F > F_{min}$ where F_{min} is the minimum noise factor. This makes this topology not a good selection to be consider in this work since NF is the crucial criteria in the design. Nevertheless, the broadband ability of this circuit reimburses for the drawback in the noise performance. Consequently, this circuit topology is usually found in many LNA circuit applications.

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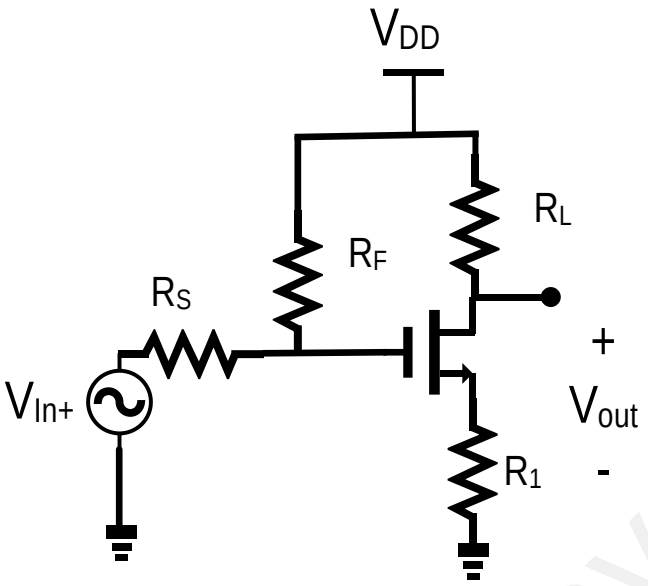

Figure 2.3: Shunt Series Amplifier Topology

The presence of impedances (resistors) in all the topologies studied above, result to noisy resistance in the network signal circuitry and lead to poor NF performance because these LNA circuits suffer NF degradation. Thus, make it not a good selection to start with for LNA design in this work. However, there is one alternative topology circuit that offers resistive input impedance without having to use resistors. This circuit topology is demonstrated in Figure 2.4 and is known as CS with inductively degeneration topology.

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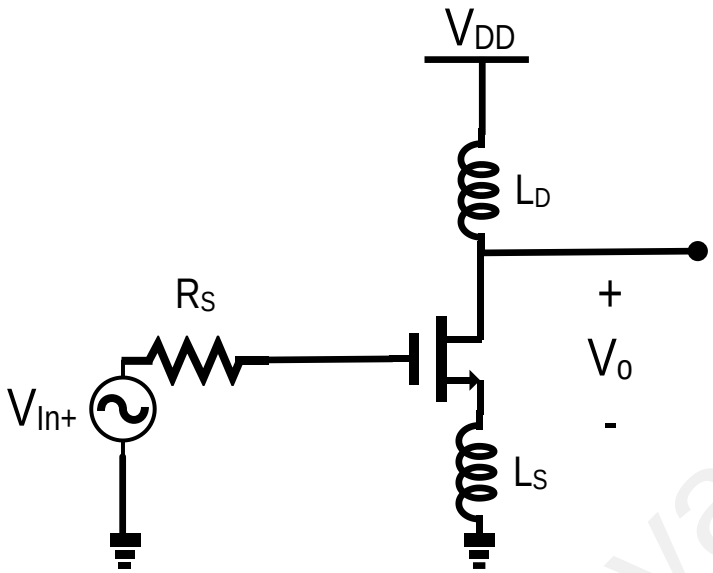

Figure 2.4: Common Source with Inductive Degeneration Topology

2.4.4 Inductively degenerated common source

The CS with inductively degenerated topology is to help the input matching. The small-signal model in Figure 2.5 is used as a guide in order to determine the input impedance of the circuit. The subsequent derivations can illustrate how the input can be simply matched to the source resistance.

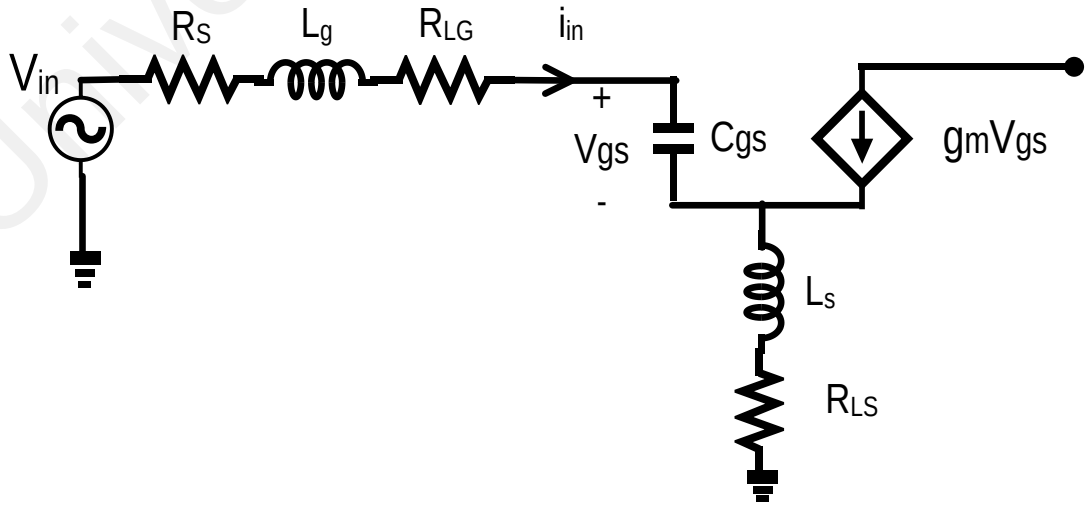

Figure 2.5: Small signal model representation for CS with inductively degenerated

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$$V_{in} = i_{in}\left(\frac{1}{SC_{gs}} + sL_s + R_{Lg}\right) + (i_{in} + g_m V_{gs})(sL_s + R_{LS}) \quad \textbf{(2.2)}$$

$$V_{gs} = \frac{i_{in}}{sC_{gs}} \quad \textbf{(2.3)}$$

$$V_{in} = i_{in}\left(\frac{1}{SC_{gs}} + sL_s + R_{Lg}\right) + \left(i_{in} + g_m \frac{i_{in}}{sC_{gs}}\right)(sL_s + R_{LS}) \quad \textbf{(2.4)}$$

$$Z_{in} = s(L_s + L_g) + \left(R_{Lg} + R_{Ls} + \frac{g_m L_s}{C_{gs}}\right) + \frac{1}{sC_{gs}}(1 + g_m R_{Ls}) \quad \textbf{(2.5)}$$

Z_{in} is an RLC series circuit with a resistive term which is straightly proportionate to the value of the inductance. Where at resonance, the real term in Z_{in} contains L_s. Consequently, in this input matching the utilization of degenerated inductor is needed. This make the presence of L_s helps in providing a right input impedance to eliminate the RF filter in the preceding the of the LNA, in which in the typical condition, need to match to 50 Ω impedance. While L_g will resonate with C_{gs} and it guarantees that the frequency of the input signal is adjusted to the frequency of the operating application. Hence during resonance, the source resistance and others parameter can be determined as the expression derived below:

$$R_s = R_{in} = R_{Lg} + R_{Ls} + \frac{g_m L_s}{C_{gs}} \approx R_{Lg} + R_{Ls} + \omega_T L_s = 50 \quad \textbf{(2.6)}$$

$$s(L_g + L_s) + \frac{1}{sC_{gs}}(1 + g_m R_{Ls}) = 0 \quad \textbf{(2.7)}$$

$$j\omega_o(L_g + L_s) = \frac{j}{\omega_o C_{gs}}(1 + g_m R_{Ls}) \quad \textbf{(2.8)}$$

$$L_g = \frac{1}{\omega_o^2 C_{gs}}(1 + g_m R_{Ls}) - L_s \quad \textbf{(2.9)}$$

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Comparing with the common source topology alone, inductively degenerated CS LNA has always been the candidate to give the best noise performance because of the absence of resistors. Though, it has a problem of being sensitive to gate induced current noise (Y. Koolivand A. Zahabi and P. J. Maralani, 2005). The Q factor of the input circuit would not be too big due to the noise is proportional to the Q-factor of the input circuit of the cascode LNA.

Cascode LNA as shown in Figure 2.6, can offer high gain, lower noise, efficient power consumption and good reverse isolation (Razavi, 2001). The noise sources of the upper, M_2 transistor of cascode transistor is degenerated by the lower, M_1 transistor output impedance. Therefore, it has superior noise performance in the lower frequency band. However, this outstanding noise and gain performance of cascode transistors stage degrades in very high frequencies band. This is because the effect of substrate parasitic admittance located at the drain-source common node that rises as frequency increases. As a result of lower impedance in the source of M_2, the drain noise presents in the output node. Additionally, cascode LNA topology aid to boost output impedance and thus enhance input and output isolation. This will reduce the interaction between the output stage and the input stage. With this condition, the sizing of the input transistor, input and load can be optimized separately. Owing to this separation, the reverse isolation can also be improved and ultimately the consequence the later stage can be better reduced (Fouad, Sharaf, El-Diwany, & El-Hennaway, 2002). Also, the stability of the LNA is enhanced and in better performance as the cascode structure lessens feedback signal from output to input. The circuit will be susceptible to oscillation if it is designed but without the cascode devices (Razavi, 2001).

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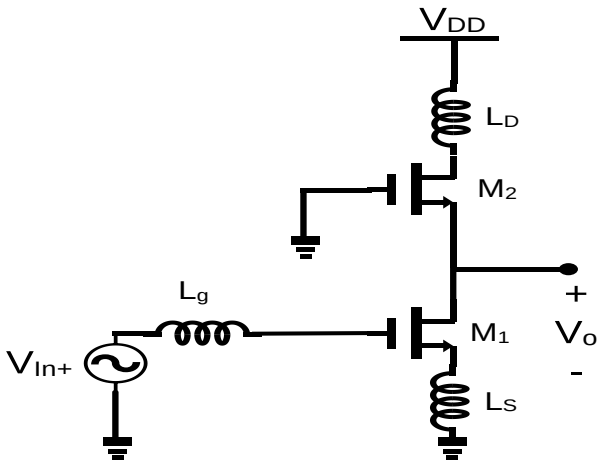

Figure 2.6: Cascode LNA topology

2.4.5 Single-stage CS inductively degenerated with open drain

There are several advantages of the open drain circuit, as L_d will allow point capacitance at the drain of M_2 to resonate with it. This will tune the output to the resonating frequency and thus leads to additional band-pass filtering. This also will provide more flexibility to tune the output to the wanted frequency and extra filtering, C_d is contained within in the circuit. An additional advantage of this circuit is that L_d will let only a slightly small voltage across it because of the resistance in series. Henceforth, a complete justification that this type of connection is very beneficial to implement for low power design.

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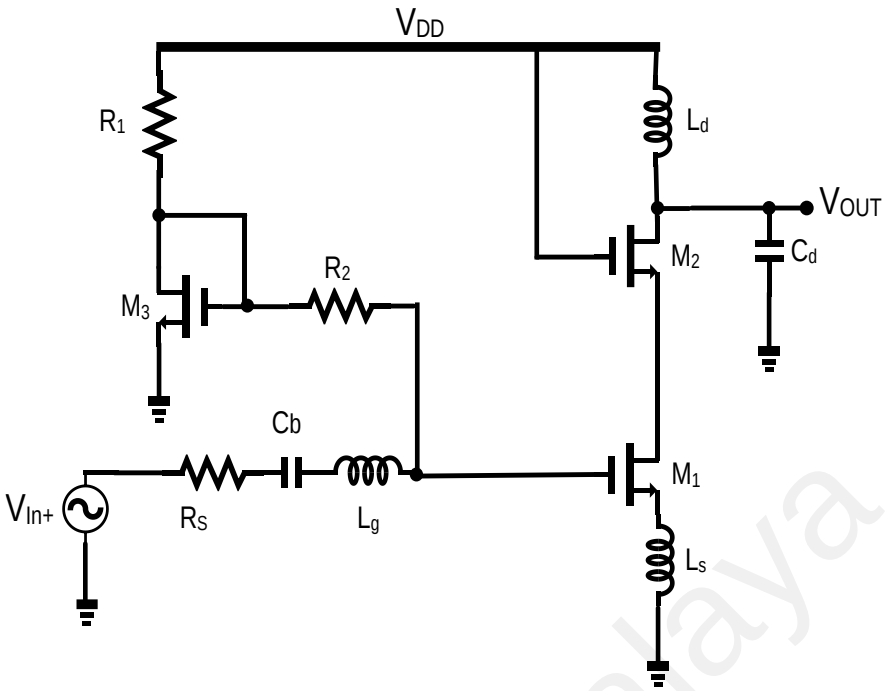

Figure 2.7: Single-stage inductively-degenerated CS with open drain LNA (Shaeffer & Lee, 1996)**.**

Figure 2.7 is single ended open drain with inductively degenerated CS LNA. M_3 and M_1 are in the current mirror connection for biasing the LNA circuit. The ratio of M_3 and M_1 controls flowing of current over the cascode node. The right selection of M_1's width will determine the V_{gs} of M_1. R_2 function to separate the signal path from the current mirror. By using this, the input signal will be ac feed to the LNA input. The value of R_2 is not critical as long as it is much bigger than the Z_{in} of the LNA. The L_s in this circuit has the contributions as such before. This degeneration inductor influences the gain of LNA and also allow more flexibility in input matching to 50 Ω.

The representation of small-signal model of the inductively degenerated CS open drain cascode LNA is shown in Figure 2.8. In this model, the drain resistance, r_o, and the body transconductance, g_{mb}, of both transistors are neglected. R_{Ld} and R_{Lg} (not shown in this figure) are the series resistance of the L_d and L_g, respectively.

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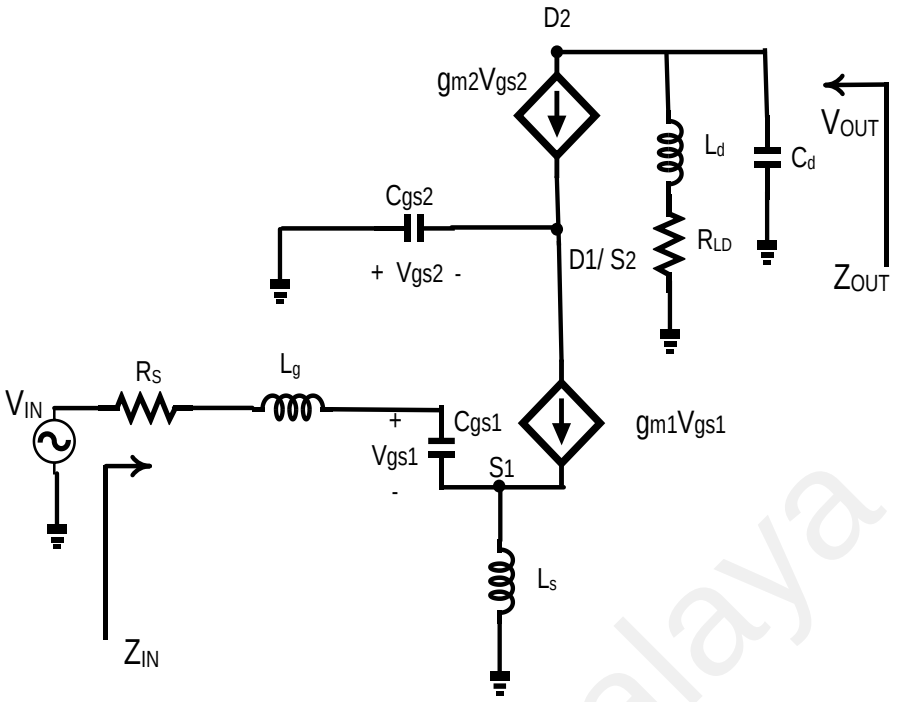

Figure 2.8: Representation of small-signal model of the inductively-degenerated CS open-drain cascode LNA.

At the output, the load impedance, Z_{L1}, is the combination of the load inductor, L_d, with a series resistance, R_d, in parallel with the drain capacitance, C_d given as equation in **(2.10)** below:

$$Z_{L1} = (sL_d + R_{Ld}) \,//\, \frac{1}{sC_d}$$

$$= \frac{(sL_d + R_{Ld})\frac{1}{sC_d}}{sL_d + R_{Ld} + \frac{1}{sC_d}}$$

$$Z_{L1} = \frac{sL_d + R_{Ld}}{S^2 L_d C_d + sC_d R_{Ld} + 1} \qquad \textbf{(2.10)}$$

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$$V_{out} = -g_{m2}V_{gs2}Z_{L1} \tag{2.11}$$

$$V_{in} = i_{in}R_s + i_{in}sL_g + i_{in}R_{Lg} + V_{gs1} + \left(g_{m1}V_{gs1} + i_{in}\right)sL$$

$$V_{in} = i_{in}\ (R_s + sL_g + R_{Lg}) + V_{gs1} + \left(g_{m1}V_{gs1} + i_{in}\right)sL \tag{2.12}$$

$$= V_{gs1}sC_{gs1}\left(R_s + sL_g + R_{Lg}\right) + V_{gs1} + \left(g_{m1}V_{gs1} + V_{gs1}sC_{gs1}\right)sL_s$$

$$= V_{gs1}\left[sC_{gs1}\left(R_s + sL_g + R_{Lg}\right) + 1 + (g_{m1} + sC_{gs1})sL_s\right]$$

$$V_{gs1} = \frac{V_{in}}{sC_{gs1}\left(R_s + sL_g + R_{Lg}\right) + 1 + (g_{m1} + sC_{gs1})sL_s}$$

$$V_{gs1} = \frac{V_{in}}{s^2C_{gs1}\left(L_g + L_s\right) + s\left(C_{gs1}R_s + C_{gs1}R_{Lg} + g_{m1}L_s\right) + 1} \tag{2.13}$$

Neglecting the current that may flow through Cgs2, gm1vgs1 = gm2vgs2. From equations **(2.11)** and **(2.13)**:

$$V_{out} = \frac{-g_{m1}V_{in}Z_{L1}(S)}{S^2C_{gs1}\left(L_g + L_s\right) + S\left[C_{gs1}\left(R_s + R_{Lg}\right) + g_{m1}L_s\right)\right] + 1} \tag{2.14}$$

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$$A_{vo} = \frac{V_{out}}{V_{in}} = \frac{-g_{m1}Z_{L1}(s)}{s^2C_{gs1}(L_g + L_s) + s[C_{gs1}(R_s + R_{Lg}) + g_{m1}L_s] + 1} \quad \textbf{(2.15)}$$

$$A_{vo} = \frac{-g_{m1}\omega_o^2 Z_{L1}(s)}{s^2C_{gs1}\omega_o^2(L_g + L_s) + s\omega_o^2[C_{gs1}(R_s + R_{Lg}) + g_{m1}L_s] + \omega_o^2}$$

$$A_{vo} = \frac{-g_{m1}\omega_o^2}{s^2C_{gs1}\omega_o^2(L_g + L_s) + s\omega_o^2[C_{gs1}(R_s + R_{Lg}) + g_{m1}L_s] + \omega_o^2} \quad \textbf{(2.16)}$$

$$\cdot\frac{sL_d + R_{Ld}}{s^2L_dC_d + sC_dR_{Ld} + 1}$$

As can be seen from Equation **(2.16)**, the voltage gain can be increased if the summation of Lg and L_s is minimized. With the smaller L_g, R_{Lg} will also be reduced (if R_{Lg} is important when compared to R_S) which will also lead to the rise in gain.

2.4.6 Differential LNA

For differential LNA, the most commonly used topology is as shown Figure 2.9, which is using the common source degenerative topology with the addition of L_g and C_b for DC blocking, and a cascode transistor at the drain of the transistor. For the sake of simplicity, the biasing circuit of differential LNA is not shown. A differential LNA can be used to suppress the common-mode distortion induced through the substrate and coupled to the RF input in a mixed mode chip. However, differential amplifier is not an optimal solution

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in terms of power consumption. Another drawback is the requirement of a balun if the input of the LNA is not of the differential nature. In practice, the loss of the balun needs to be added to the NF of the whole receiver system. Differing from single-ended LNA, differential LNA provides better linearity as it can help to cancel off the even order distortion and reject common mode noise as well. An important issue that should be taken into consideration is the linearity of the low noise amplifier. Linearity is important to get less distortion output. Nevertheless, there is always a tradeoff between gain and linearity. Another factor that should be considered is both input and output ports have to be matched to 50 Ohm for maximum power transfer. This also indicates that the S_{11} and S_{22}, the reverse isolation for input port and output port respectively, must be small enough, which is at less –10 dB. Other than these specifications, low power consumption for receiver architecture is also another important issue that needs to be tackled. The gain for differential low noise amplifier should be high enough to feed to the following stage. As the value implies the noise figure of the LNA is important parameter that needs to be fulfilled, the noise figure and noise factor should be smaller than certain power level. A good low noise amplifier should consist of acceptable gain and noise figure, thus, can produce an output signal which consists of low inherent noise signal level.

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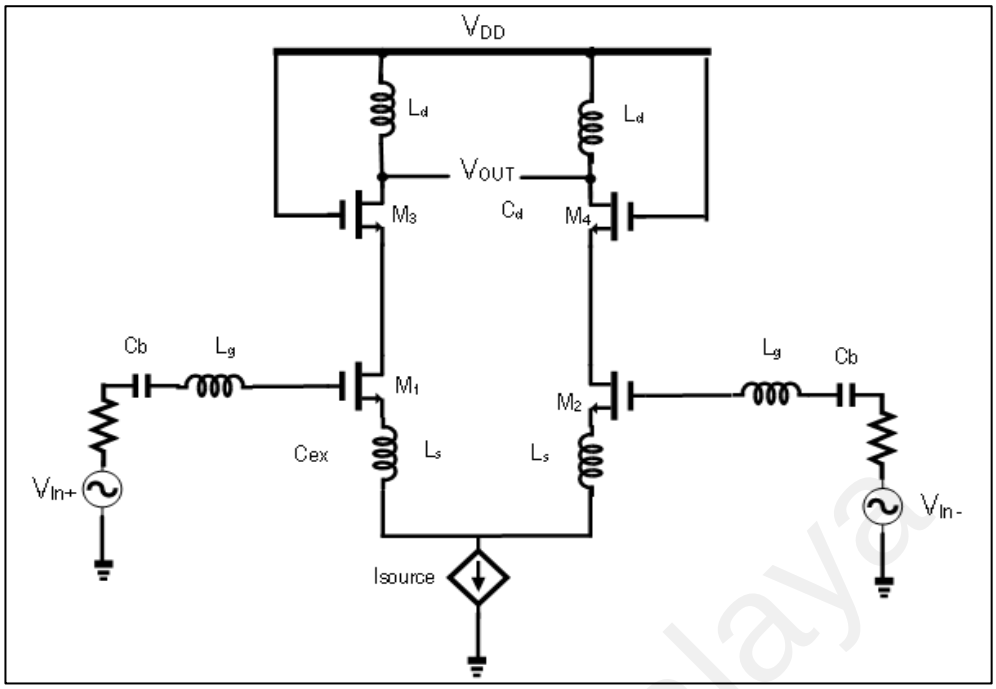

Figure 2.9: Common Source Inductive Degeneration Cascode Differential LNA

The LNA with differential topology has many advantages as follows. The circuit is able to reject common-mode disturbances. Hence, filtering of noise is not so critical as in single-ended circuits. This capability is essential in mixed-signal application, where both supply and substrate voltages are very noisy. In differential circuits, spurious tones, which leak to the supply lines, become common-mode signals as the biasing is shared. To maximize common mode rejection ratio (CMRR), layout should be as symmetrical as possible. The architecture is unaffected by parasitic ground inductance and can avoid problems caused by substrate coupling. The circuit can reject on-chip interference better and hence the noise and linearity performances of the circuit are better due to it.

An example of common-mode noise rejection of a differential amplifier which occurs with noise supply voltage is shown in Figure 2.10. Referring to Figure 2.10 (a), if the V_{DD} varies by ΔV, then the V_{out} will also vary by the same amount. This indicates that the output signal is susceptible to the noise that exists at V_{DD} (Enz & Cheng, 2000).

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In Figure 2.10 (b), if the same noise and ΔV occurs on the V_{DD}, V_{out1} and V_{out2} will also observe the same magnitude but opposite in phases amount of variation with a differential output, $V_{out} = V_{out1} - V_{out2}$. This means that the noise effect will be cancelled at the differential sensing. Hence, this circuit is more robust to supply noise.

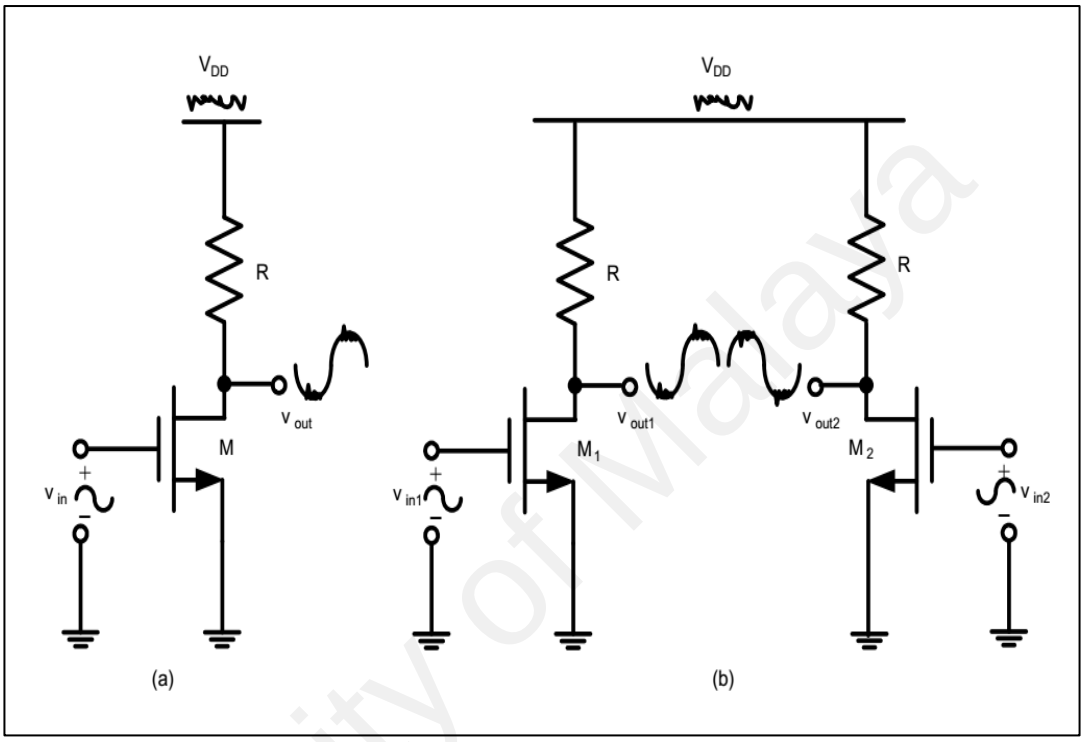

Figure 2.10: Circuit representation of the noise from supply effect (a) single-ended circuit (b) differential double-ended circuit (Razavi, 2001)

Besides the advantages of differential LNA, however there are problems regarding to the differential topologies such as:

1. The current dissipates by the differential circuit is twice than the current required by a single-ended. Thus, power consumption by the balanced structure is twice than the single-ended.
2. The differential circuit consumes twice chip area needed by single-ended counterpart due to the two identical circuits. This is a challenge if on-chip

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inductors are vital. If the inductively degenerated cascode is constructed in differential structure, six inductors are required instead of three inductors. This is a bottleneck as inductors are bulky components and they control the overall area and size of the chip.

3. A differential LNA requires a balun at its output or input port if this port is connected to a single-ended circuit. The loss of the balun needs to be corporate to the NF of the whole receiver system.

2.5 CMOS LNA Characteristics

As the first active block in the receiver chain, the performance of an LNA dictates the overall performance of receivers. Noise performance and power gain are the most important characteristics of an LNA. Beside these characteristics, the main parameters affecting the selection of a proper circuit for an LNA are DC power consumption, bandwidth, stability, linearity, supply voltage and chip area.

In this chapter, a review on CMOS LNA characteristics are presented. This key performance parameters for RF CMOS communication circuit design are discussed. Following that are an introduction to LNAs and trade-offs in LNA design.

2.5.1 Noise and Power Gain Matching

Minimum attainable noise figure of an LNA can be gained by using optimum noise input matching. While power gain provides the maximum available power gain, both of maximum available gain and NF_{min} are not at the same time possible due to performance and design tradeoffs. However, in CMOS technology these two situations are very near together and this is an significant benefit of CMOS circuits that can improve inherit crucial noise performance of CMOS LNA technologies (N M Noh & Zulkifli, 2007).

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Simultaneous noise and power matching become possible in CMOS technology. In order fot the maximum power gain matching to occur, this need the resistive term of the input impedance of LNA. This resistance term is transformed to the real part of the source impedance. Several classic techniques to give the essential resistive term in the input impedance of an LNA has been explained previously.

The resistive term is portion of the input impedance to the source of the CG transistor in the case of CG stage while for a CS or cascode stage the input impedance is capacitive in very low frequencies. Hence a resistive part is important and need to be added to the input impedance. One of the techniques is by using a resistive feedback this can be possible for the required term. Another way is to place a parallel resistance in the gate or a degenerating inductance in the source of common source CS transistor. However, parallel resistance in the gate rises the noise figure of LNA and make it not favored in a design. The feedback resistor between drain and gate, forms a self-bias mechanism for transistors, as well contributes in the real part of the input impedance to relax the matching circuit. Degenerating inductance in the source of CS stage produces a resistive term in the input impedance of MOS transistor. This technique is widely used in CS and cascode LNA circuits (Norlaili Mohd. Noh & Zulkifli, 2007). For narrowband LNA designs, CS and cascode stage are the suitable selections. Source degenerated cascode of common source stage displays a good narrowband input matching, good noise performance and high stability (Nguyen et al., 2004) . As been reviewed previously, CG stage offers wideband matching. Some special matching techniques have been developed for ultra-wideband UWB applications (Rastegar, Saryazdi, & Hakimi, 2013). Direct matching of antenna to LNA in a receiver front end has been taken care of in recent years (Chen et al., 2013; Nguyen et al., 2004) . Using this technique, simultaneous optimum noise and power matching of LNA becomes possible.

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As the name implies, the LNA's performance is primarily measured by its NF. The importance of having an LNA with good noise performance is indicated by the Friis's formula for a Rx with the an LNA being the first stage (Korakkottil Kunhi Mohd, Zulkifli, & Sidek, 2010):

$$F_{receiver} = F_{LNA} + \frac{(F_{rest} - 1)}{G_{LNA}} \quad \textbf{(2.17)}$$

where $F_{receiver}$ is the overall NF of the Rx and F overall noise factor of the stages subsequent to the LNA, G_{LNA}, F_{rest} and G_{LNA} formula, it is seen that F_{LNA} is the NF of the LNA. F_{LNA} rest is the power gain of the magnitudes are expressed as ratios, not in decibels. From this formula on the receiver is evidently dominated by F_{LNA} of the LNA. This means that an LNA with a high-power gain is welcomed as it will lead to the overall noise contributed by the rest of the circuits in the Rx to be quite insignificant. The next observation is that the NF of the LNA must be low as it is the dominating contributor to the overall NF of the Rx.

The input signal to the LNA is usually not consistent in magnitude. Besides amplifying the small signals, the LNA should also be able to amplify large signals without distortion. Hence, good linearity is required from the LNA. Besides this, the LNA's linearity performance is crucial in ensuring that undesired signals such as the second- and third- order inter-modulation products will not be able to have significant influence on the amplification of the desired signal.

Input and output matching are very important to the LNA. Good matching ensures optimum power transfer, optimum gain and optimum noise performance. As the LNA is normally found in receivers for wireless application, power consumption is an important factor to indicate the LNA's ability to operate in low power.

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2.5.2 Noise Figure of the LNA

The quality of the signal can be evaluated by signal-to-noise ratio (SNR), which is defined as the ratio of a signal power to the noise power corrupting the signal.

$$\mathrm{SNR} = \frac{\mathrm{P_{signal}}}{\mathrm{P_{noise}}} \tag{2.18}$$

Where $\mathrm{P_{signal}}$ and $\mathrm{P_{noise}}$ indicates signal power and noise power in watt respectively. Meanwhile, noise factor is a merit used to indicates how much the signal to noise ratio, SNR, deteriorates as signal pass through a specific circuit or systems, and its expression is as given as (Shaeffer & Lee, 1996),

$$\mathrm{F} = \frac{\mathrm{SNR_{in}}}{\mathrm{SNR_{out}}} \tag{2.19}$$

Noise figure is an alternative expression of noise factor, and basically, it just the logarithm of noise factor, or shown as given below.

$$\mathrm{NF} = 10\ \log_{10} F = 10 \log_{10} \left(\frac{\mathrm{SNR_{in}}}{\mathrm{SNR_{out}}}\right) \tag{2.20}$$

Hence, for ideal case, the LNA design should has noise figure approximate to unity. In other words, lower the noise figure, the better performance of that LNA. Being the first stage of receiver architecture, basically, LNA plays an utmost important role as the signal from antenna will straight away feed into LNA, and ideally, we want to get rid of those "inevitable" noise produced during modulation and transmission. Besides noise figure, there are some other specifications that need to be taken into consideration during

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LNA design, like voltage gain, current consumed, linearity, matching etc. On top of these constraints, the die's size area is also being taken into consideration while designing LNA.

Hence, while designing, the bulky components, such as inductor and capacitor, are usually treated as off-chip components rather than integrated as on-chip elements. This implies that, for matching circuit, the serial or parallel inductors and capacitors, is inevitably constructed externally (off chip component).

During the amplification, RF LNA also adds noise in the signal which further corrupts the signal. The noise performance of the RF LNA is evaluated through the noise factor (F) or noise figure (NF). The noise factor describes the degradation of the incoming signal SNR due to the LNA. It is defined as:

$$F = \frac{SNR_i}{SNR_o} = \frac{\frac{S_{in}}{N_i}}{\frac{S_{out}}{N_{out}}} = \frac{S_{in}N_i}{(S_{out}G)N_{out}} = \frac{N_{out}}{GN_i} \quad \textbf{(2.21)}$$

where SNRi and SNR_o are the signal-to-noise (SNR) at the input and the output respectively. N_{out} is the noise power at the output.

2.5.3 Scattering Parameters

Scattering parameters are widely used in RF and microwave circuits to represent the scattering or reflection functions of the traveling wave when the n-port network is inserted into a transmission line. They are helpful for component modelling and circuit design. There are also other representations using impedance (Z) and or admittance (Y) parameters. At the low frequency, the Z parameters can be easily obtained using the open-circuit approach. The Y parameters can be easily obtained using the short-circuit approach. At the high frequency, it is difficult to provide adequate shorts or opens, and the active circuits may resonate when terminated in short or open circuits. S-parameter, in the contrary, measures the traveling wave, which does not need nor allow the short or

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open connections. Since a line terminated in its characteristic impedance generates no reflections, S-parameter can measure the device, which has some distance from the instrument and is connected using a low-loss transmission line.

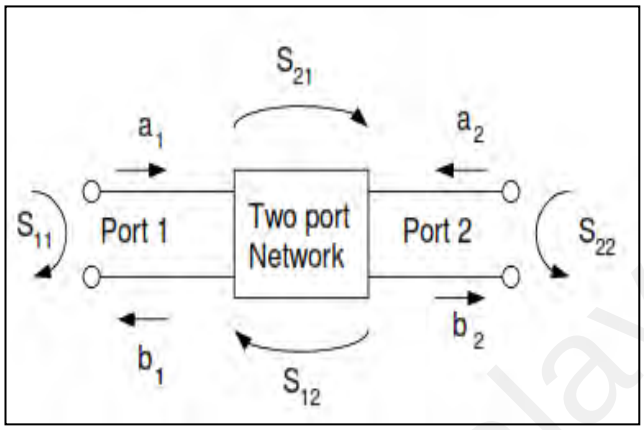

Figure 2.11: Two port network and its S-parameter

A typical two port network in Figure 2.11 is used to explain the definition of the S parameters, where a_1 and a_2 represent the incident waves and b_1 and b_2 represent the reflected waves (Vaz & Caggiano, n.d.).

S-parameters are given by:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad \textbf{(2.22)}$$

$$b_1 = a_1 S_{11} + a_2 S_{12} \quad \textbf{(2.23)}$$

$$b_2 = a_1 S_{21} + a_2 S_{22} \quad \textbf{(2.24)}$$

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where;

$$S_{11} = \frac{b_1}{a_1}|_{a_{2=0}} = \text{input reflection coefficient with matched output port}$$

$$S_{21} = \frac{b_2}{a_1}|_{a_{2=0}} = \text{forward transmission gain with matched output port}$$

$$S_{22} = \frac{b_2}{a_2}|_{a_{1=0}} = \text{output reflection coefficient with matched input port}$$

$$S_{12} = \frac{b_1}{a_2}|_{a_{1=0}} = \text{reverse transmission gain with matched input port}$$

$a_1 = 0$ means that the incident wave is zero, i.e. there is no source of energy at the port 1. At that times, port one is loaded with resistance of $Z_L = Z_o$. $a_2=0$ means that there are no incident waves from port 2. At that time, port two is loaded with a resistance of $Z_L = Z_o$. S_{11} and S_{22} represent the reflection coefficients from port 1 to port 2 and from port 2 to port 1. The ideal values of S_{11} and S_{22} are –10 dB is generally considered sufficiently good as this value indicates that the reflected wave is ≈30% from the incident wave and hence that the port 1 and port 2 are perfectly isolated. The more negative value than this will show a better matching performance as it indicates that smaller percentage of the incident signal is being reflected. The S_{21} typically represents the transmission gain or forward voltage gain, which needs to be designed according to the system requirement.

2.5.4 Stability

Stability is also one of the important parameter characteristics in designing LNAs. The stability of an LNA circuit is defined by Stern stability factor given in below:

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{11}||S_{22}|} \quad \textbf{(2.25)}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad \textbf{(2.26)}$$

In this work, LNA circuit is unconditionally stable if K > 1.

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2.5.5 Input and output impedance matching

Input and output matching are one of the crucial parameters in RF LNA circuits and it demonstrates important part in its performance. Good matching guarantees optimum and efficient power transfer and optimum noise performance. Input and output impedance matching is given by the input and output return loss and is defined as in expression **(2.27)** and **(2.28)**.

$$20\ log|\Gamma_{in}| = 20\log|S_{11}| \quad \textbf{(2.27)}$$

$$20\ log|\Gamma_{out}| = 20\log|S_{22}| \quad \textbf{(2.28)}$$

where Γ_{in} and Γ_{out} are the reflection coefficient at the input and out respectively.

2.5.6 Linearity

There is another important issue that must take into serious consideration, which is the linearity of LNAs. It plays significance consideration along with other criteria such as gain, noise and impedance matching. Active RF LNAs device can be classified as nonlinear in their operation. It can create unwanted spurious signal when large input signal is driven. Nonlinearities in LNA can lead to intermodulation distortion, desensitization and blocking and cross modulation. Blocking is a phenomenon where the inter-modulation products caused by the strong interferer overcome the desired weak signal. Cross modulation, on the other hand, resulted from non-linearity that transfers the modulation of one signal to the carrier of another. RF research trend nowadays is to eliminate the external front-end module (FEM) that is expensive (Lie, 2010) . Thus a highly linear RF receiver system is required. What is more critical is that the LNA must be able to receive a weak signal properly even in the incidence of a strong intrusive signal (Tarighat & Yargholi, 2016). The input frequency is known as fundamental while the higher order are known as harmonics. There are two performance criteria to evaluate the

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linearity of LNA circuit which are the 1-dB compression point and input third-order intercept point (IIP_3)

Basically, linearity means the "dependency" of output towards input signal as depicted in Figure 2.12. However, it is difficult get such a linear output. As what usually obtained is distorted little bit from the ideal linear output. Figure 2.12 shows the graph of output signal (V_{OUT}) vs input signal (V_{IN}) in order to illustrate the linearity and non-linearity in a RF system.

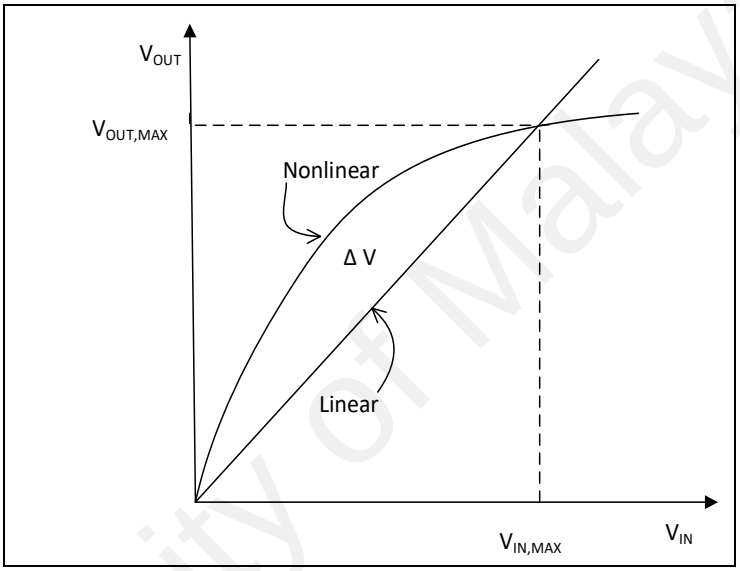

Figure 2.12: Graph of V_{OUT} vs V_{IN} to illustrate linearity and non-linearity in a system

The effect of non-linearity is quite big, as shown in Figure 2.13 . Notice that, the amplitude of signal I_N' and I_N'' is the same indeed, however, when they are driven using different voltage to the input of a non-linear amplifier, the output is no longer the same. Distortion occurs. This kind of distortion will affect the linearity of the circuit. This effect may conclude that the output of a non-linear amplifier would differ even though the amplitude of the input signal is the same. Hence, linearity is important to produce a good output. Hence, in order to represent the non-linearity effect, it can be express using Taylor Expansion series, which is shown as below [9],

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$$y(t) = A_1\, x(t) + A_2 x_2(t) + A_3 x_3(t) + A_4\, x_4\,(t) \ldots \qquad \textbf{(2.29)}$$

For a non-linear system, the component A_2, A_3 and so on is significant, and no longer negligible. With the existence of Taylor Expansion Series, we can roughly estimate the linearity of a system by the interception of component A_1 and A_3, which is the main idea of the 3rd intermodulation point, of IIP_3. IIP_3 is a standard in measuring linearity of a system, usually measured in dBm. It indicates how good a receiver performs in the incidence of strong interferers. The more positive of the IIP_3 value, the better linearity performance of the systems. Figure 2.14 illustrates the IIP_3 of a system.

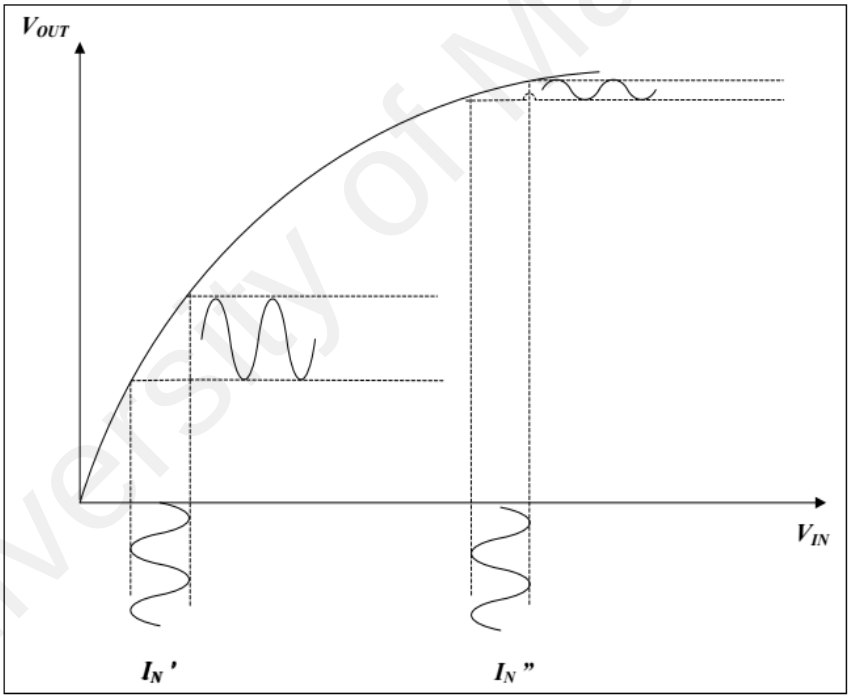

Figure 2.13: Variation of small signal gain in non-linear amplification

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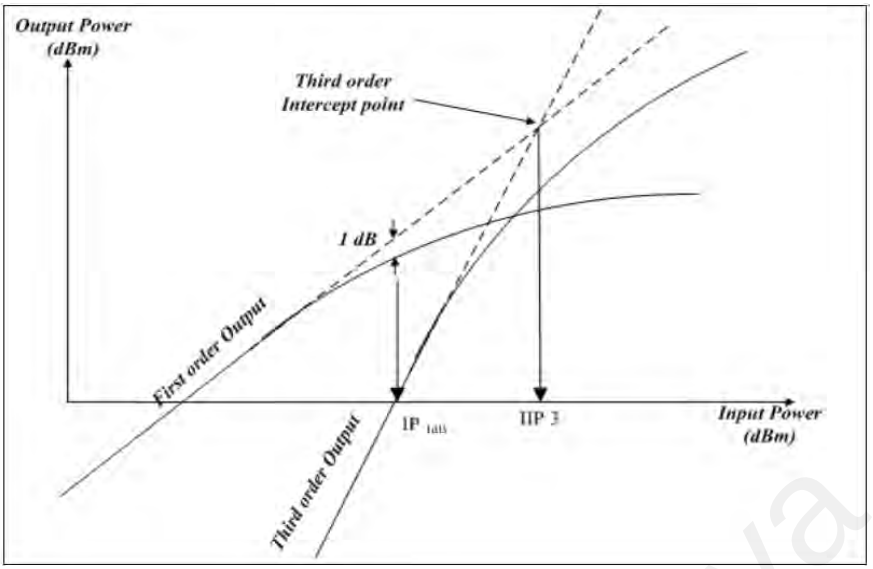

Figure 2.14: Input third order intercept point, IIP_3

The performance measure for this nonlinearity is usually expressed by the third-order input intercept point (IIP3). The basic methodology to improve linearity is by adding a cascode transistor. The cascading transistor will give improvement to linearity performance, meanwhile the main transistor contributes to noise performance (Abdulaziz, Ahmad, Tormanen, & Sjoland, 2017). Figure 2.15 illustrates an example IIP_3 performance of an LNA at 21 dBm.

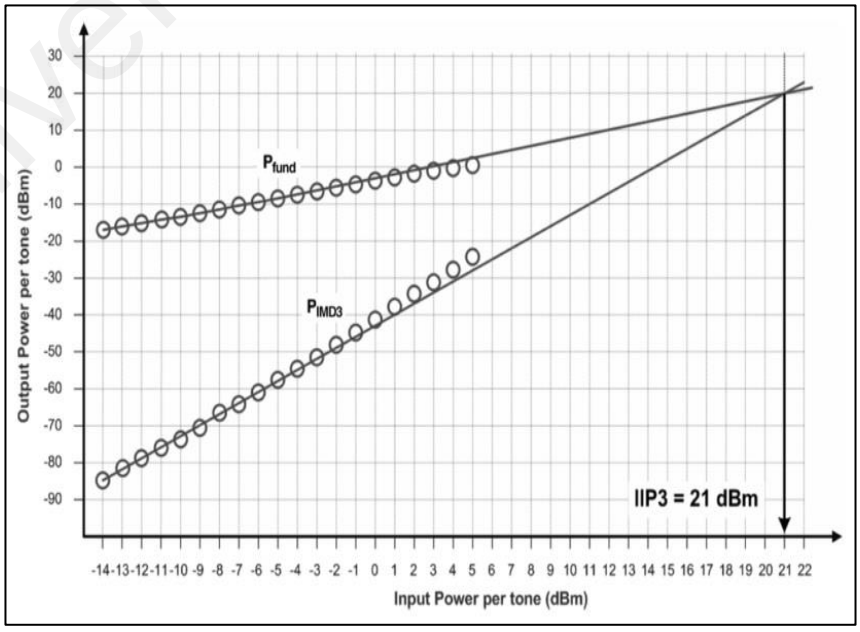

Figure 2.15: Illustration of IIP_3 performance of LNA (Ganesan et al., 2006)

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The intersection of line of the fundamental first order output and 3rd order intermodulation product is called the third-order intercept point, with horizontal component called input IP3 (IIP3) and vertical output IP3 (OIP3).

2.5.7 1-dB Compression point

1-dB compression point is the measure of gain compression. As shown in Figure 2.16, it is defined as the input signal level for which the gain of the amplifier drops by 1-dB. This mechanism can be described by example an LNA is driven by a sufficient high input signal, then the gain of the amplifier starts to drop at a certain level of input. 1-dB compression point is the measure of the maximum input range of the circuit. In typical RF front-end LNA, 1-dB compression point is around -20dBm to -10 dBm (Ganesan et al., 2006).

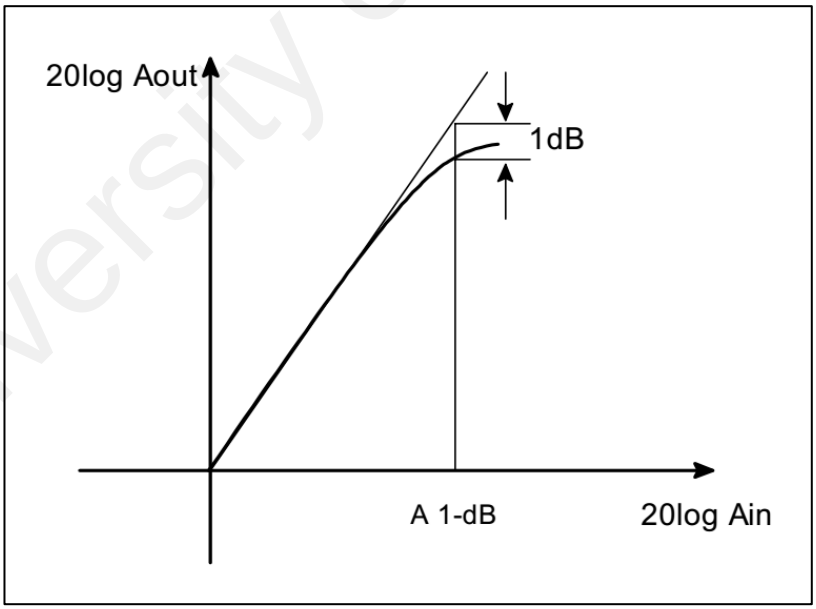

Figure 2.16: Graph representation of 1-dB compression point

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2.6 Conclusion

Several CMOS LNA design topologies and techniques have been reviewed and discussed in this chapter. There several CMOS LNAs techniques that have been proposed previously that proven to cater certain requirement and application. Having discussed in the above, a fully differential approach is usually preferred in RF application. This is due to its eminent properties of immunity to common-mode disturbances, increased in dynamic range and also rejection to parasitic couplings. There are RF circuits that need differential signals to achieve their function such as mixer. In these conditions, an integrating component to be able to convert single-ended to differential signals is needed. A differential LNA is better to be implemented in a mixed-mode design where a single-ended LNA is prone to be affected by substrate noise and other interferers on chip of the receiver.

Generally, there are six basic LNAs topologies and architectures that were reviewed in this chapter. This includes the common gate amplifier, common source with shunt-input resistor, shunt-series topology, inductively degenerated CS, cascode and differential topology. Out of the six, the inductively degenerated CS amplifier is considered to be the topology capable of offering the best noise performance due to the nonappearance of resistors in the topology. After determined the best topology for noise performance, improvement and optimization on the performance of the LNA in terms of the other parameters was taken care of.

On the justification of accurate input matching provided by differential low-noise amplifier inductively degenerated cascode attracts considerable interest by design world. Also, the design solution proposes good linearity, efficient chip area and low power.

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As a summary, the LNA's performance is being evaluated by the following performance matrices:

- Noise Figure (NF).
- Voltage Gain (A_V) or Power Gain (S_{21})
- Input 1-dB Compression Point (P1 dB and IIP3 1dB) and Input-Referred Third-Order Intercept). The values of these metrics are indicators of the circuit's linearity.
- Input and output matching which are measured by the values of the input and output reflection coefficient, S_{11} and S_{22} respectively
- Power consumption.
- Reverse isolation which is indicated by the scattering parameter S_{12}

From the performance metrics stated, it is obvious that amongst the important parameters to measure the performance of an LNA are the s-parameters as these parameters indicate the gain, matching and the capabilities of the LNA. NF is a crucial parameter in the receiver system to have lowest SNR at the lowest signal sensitivity.

Prior to the LNAs issues and techniques discussed here, the important issues highlighted in this thesis hence becomes the background of the project. Several techniques of the recent published of differential CMOS LNA that been reviewed and discussed are presented in Table 2.3.

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Table 2.3: Performance comparison of differential LNA technique performance based on previous research works

Tech. (nm)	Topology	Technique	Freq (GHz)	S_{21} (dB)	S_{11} (dB)	IIP3 (dBm)	NF (dB)	Power (mW)	Power Supp. (V)	Chip Area (mm^2)	References
65	*Fully differential	Active feedback, Common gate noise cancellation method	0.8 - 5	13.7–13.9	-10	+11.9	3–3.28	16.5	-	0.515 × 0.220	(Zokaei & Amirabadi, 2018)
130	*Fully differential	Active Post Distortion	3.5 - 5	14	-15	4	3.9	21	1	0.557 x 0.567	(Zokaei et al., 2015)
65	+Fully differential	Operational transconductance (OTA)	0.67 - 0.95	-	-	10	-	12.6	1.2	-	(Abdulaziz et al., 2017)
65	+Single to Differential	Inductorless, active balun	0.3 – 3.5	15	<-10	>0	< 3.5	21	1.2	-	(Blaakmeer, Klumperink, Leenaerts, & Nauta, 2008)

+ = Measured, * = Post layout, a= 1-dB compression point, b = voltage gain

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Table 2.4 Continued: Performance comparison of differential LNA technique performance based on previous research works

Tech. (nm)	Topology	Technique	Freq (GHz)	S_{21} (dB)	S_{11} (dB)	IIP3 (dBm)	NF (dB)	Power (mW)	Power Supp. (V)	Chip Area (mm^2)	References
180	+Single to Differential	Center tap differential inductor	1.575	24.6	-	-	3.2	9.36	1.8	1.3 x 0.9	(Duan et al., 2012)
180	+Single-ended	Resistive feedback, MDS	5 -10	22-10.3	<-8.5	-13 to 7	2 – 5.6	5.3	1.8	660 x 748	(Tarighat & Yargholi, 2016)
130	+Fully differential	Inductively degenerated CS cascode	3 – 5	9.5	<-10	-6[a]	3.5	16.5	1.5	-	(Bevilacqua, Sandner, Gerosa, & Neviani, 2006)
130	*Fully differential	Common gate, built-in linearizer	3.1 - 10.6	10.24	-	6.80	0.9-4.1	17.2	-	-	(Rastegar & Ryu, 2015)
65	+Fully differential	LNA + Filter	3.5 - 4	28[b]	<-6		3.4	2.1	-	-	(Chen et al., 2013)

+ = Measured, * = Post layout, a= 1-dB compression point, b = voltage gain

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Table 2.5 Continued: Performance comparison of differential LNA technique performance based on previous research works

Tech. (nm)	Topology	Technique	Freq (GHz)	S_{21} (dB)	S_{11} (dB)	IIP3 (dBm)	NF (dB)	Power (mW)	Power Supp. (V)	Chip Area (mm^2)	References
180	+Single ended	Common gate & Common source	3.1 - 10.3	9.6–2.71	<-9	-3	2.5- 3.9	13.4	-	-	(Lo & Kiang, 2011)
90	+Single to differential	Noise cancelling + transformer	2.5 – 4	19	<-10	-8	4-5.4	8	-	0.7 x 1.1	(Bruccoleri, Klumperink, Nauta, & Member, 2004)
130	+Single to differential	Inductorless balun	0.1 - 2	7.6	<-10	0.5	4.15	3	-	0.075	(Kim & Silva-Martinez, 2012)
180	*Single to differential	Active balun + Noise cancelling	0.15 – 0.6	-	-11.7	-	3.9	-	1.8	-	(Ling, Lin, Yang, & Huang, 2011)
180	+Single to differential	3 Inverter based gain	0 - 1.4	16	<-10	<-13.3	3	12.8	1.8	-	(Liu, Chen, Hsia, Yin, & Lu, 2014)

+ = Measured, * = Post layout, a= 1-dB compression point, b = voltage gain

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Table 2.6 Continued: Performance comparison of differential LNA technique performance based on previous research works

Tech. (nm)	Topology	Technique	Freq (GHz)	S_{21} (dB)	S_{11} (dB)	IIP3 (dBm)	NF (dB)	Power (mW)	Power Supp. (V)	Chip Area (mm^2)	References
180	Fully Differential	Active balun + cascode CS	5	23	-	-8	3.6	8	1.8	-	(Azevedo et al., 2006)
350	[+]Differential	Inductively degenerated cascode	2.2	8.4	-	-2.55	1.92	16.2	1.8	-	(Fan, Zhang, Member, & Sánchez-sinencio, 2008)
350	[+]Differential	Inductively degenerated	0.9	17.5	-	-6	2	21.6	2.7	-	(Gatta, Sacchi, Svelto, Vilmercati, & Castello, 2001)
180	*Single ended,	current reused	5.4	12.55	-	-23.84	0.42	2.87	1.2	-	(Shankar & Dhas, 2014)
180	*Single ended	noise cancelling, current reused	3.1 - 10.6	>10	-11	-4.6	2.9	15.2	1.8	-	(Shim, Yang, & Jeong, 2013)

[+] = Measured, * = Post layout, a= 1-dB compression point, b = voltage gain

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CHAPTER 3: PROJECT DESIGN METHODOLOGY

3.1 Introduction

This chapter elaborates the design methodology in this work. The power budget is the used constrain for integrated circuit implementation, thus a design approach oriented towards lower power needs to be implemented. Design of the LNA has been implemented using BSIM4 model libraries of 0.13 μm CMOS process technology from Silterra (M) Sdn Bhd. This work was implemented using Cadence SpectreRF for circuit simulation and Cadence Virtuoso for layout implementation. This research is being conducted to improve various LNA parameters such as gain, S parameters, noise figure (NF), IIP_3, power and chip area. The development of this work starts by selection of the LNA configuration. Then, the general work can be divided mainly into two section. The first part is designing single-ended LNA based on the selected configuration. Several design techniques were employed such as power constraint noise optimization (PCNO). The optimization of the single ended LNA was further developed using power constrained simultaneous noise and input matching (PCSNIM) in order to reduce the noise and lower the power consumption of the design is performed to ensure the performance achieved specification requirement set by WLAN standard. The second part of the research work is to design differential LNA based on the optimized single ended LNA PCSNIM configuration implemented in the first part. This differential LNA was double ended in nature thus there a need balun circuitry to assist the valuation of the circuit. The differential LNA PCSNIM was fabricated by Silterra. Then, the testing and measurement is done on the wafer itself. On-wafer s-parameter characterization of this four-port differential LNA was measured using two-port vector network analyzer. This measurement technique is one of the contributions in this research work and will further explain in the later section.

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Next, the noise figure of the fabricated differential LNA chip was measured using de-embedding technique that was developed in this research to reduce the interference of noise into the system.

The overview of the overall methodology implemented in this research is highlighted in Figure 3.1

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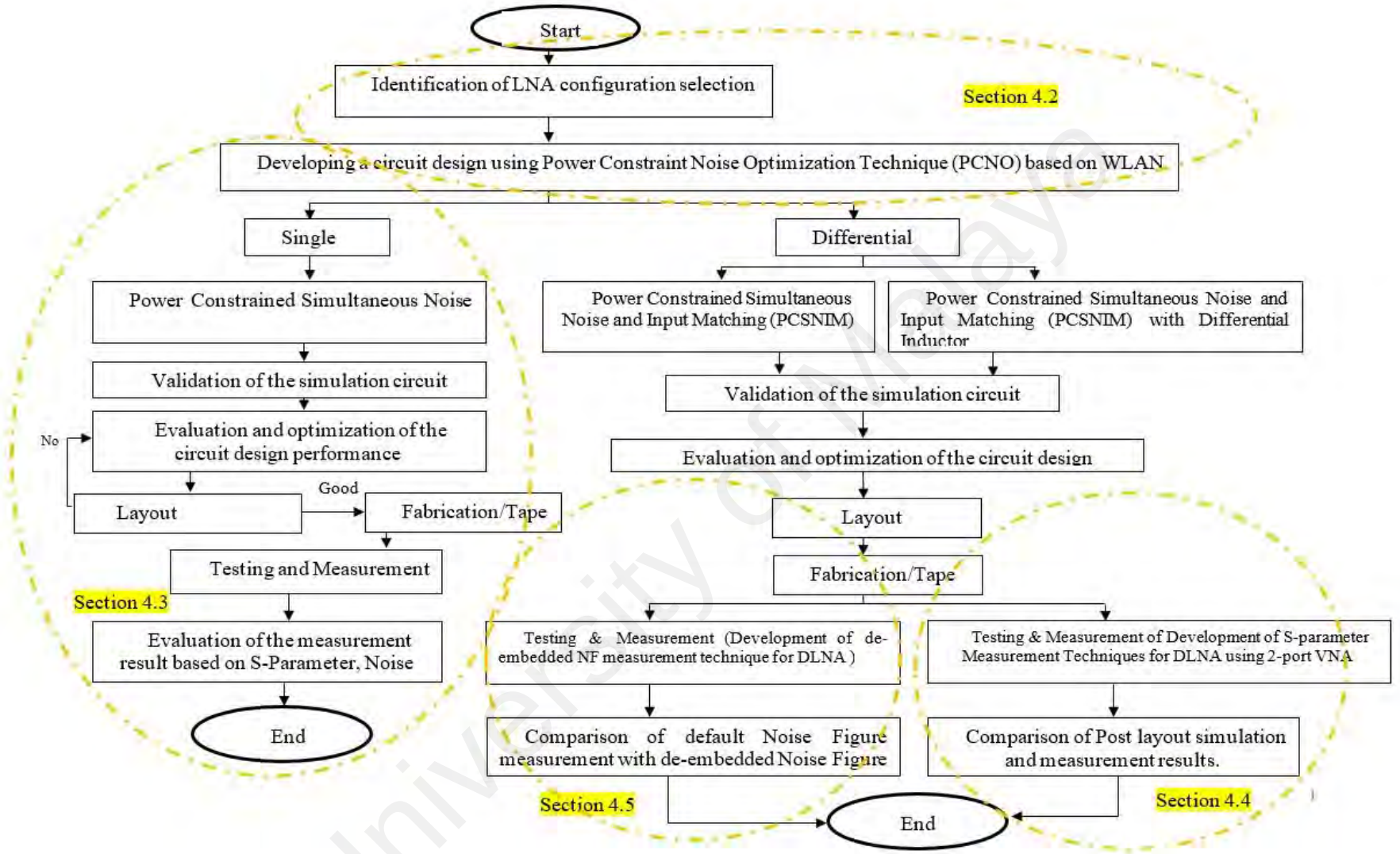

Figure 3.1: Schematic diagram of project flow chart used in this research

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3.2 LNA Design

The power budget is the common constrain for integrated circuit implementations, thus a design approach oriented towards lower power need to be adopted. The former chapter already explained the performance metrics of LNA and several topologies that could be implemented in designing LNA. The LNA design that is described here would be an inductively degenerated cascode topology. This topology is preferred as it is the basic topology in the commonly found LNA architecture available recently. The inductively-degenerated cascode structure is also known as simultaneously noise input matching (SNIM) topology (Nguyen et al., 2004) is shown in Figure 3.2.

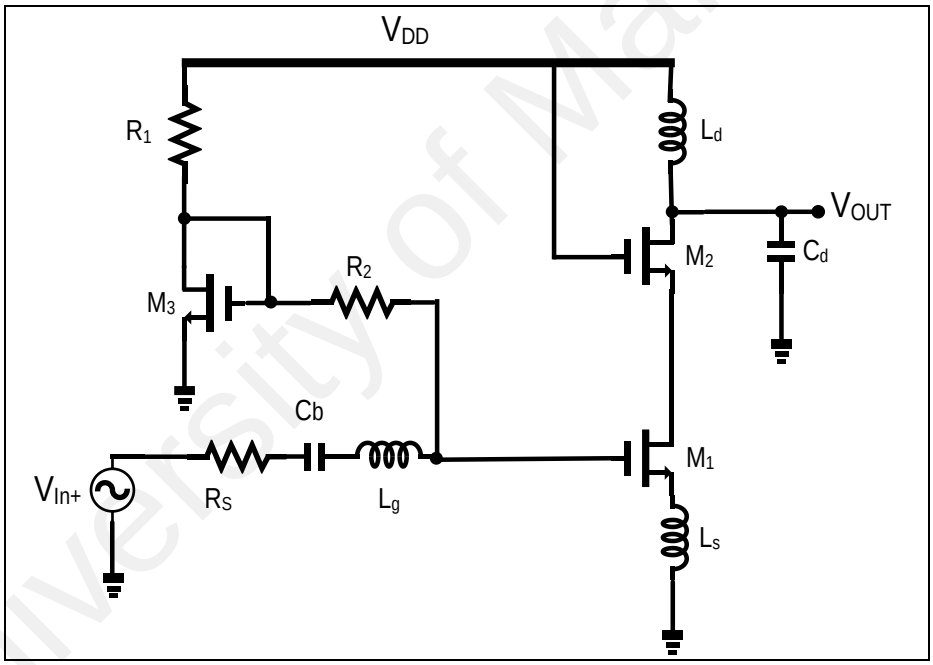

Figure 3.2: Inductively degenerated cascode LNA topology

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3.3 LNA Design Flowchart

Table 3.3 shows the flowchart of the design methodology for the inductively degenerated cascode LNA.

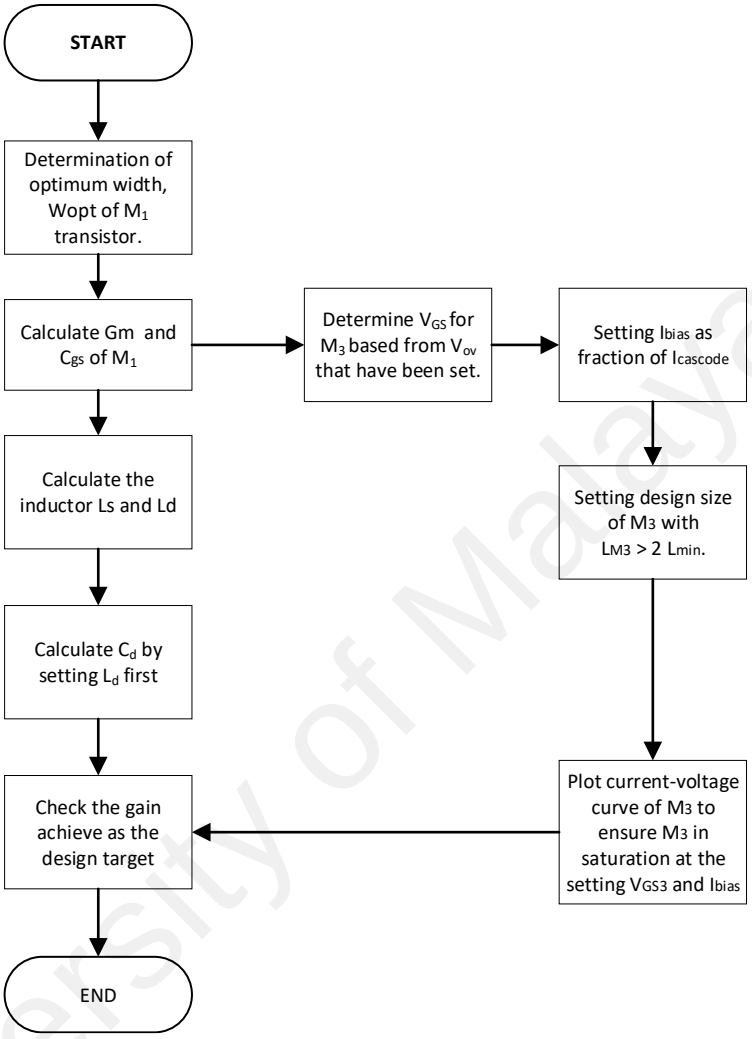

Figure 3.3: Flowchart of the LNA design methodology

3.4 Determination of transistor size

The width of the main transistor can be determined by the expression below:

$$W_{opt} = \frac{3}{2\omega_o L C_{ox} Q_{s,opt} R_s} \quad \textbf{(3.1)}$$

where L is length of the transistor, R_S is the 50 Ω resistor, and Oxide capacitance, C_{ox} can be represented by the expression below:

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$$C_{ox} = \frac{\varepsilon . \varepsilon_r}{t_{ox}} \quad \textbf{(3.2)}$$

where ε indicates permittivity of free space, ε_r *is* the relative permittivity or dielectric constant, and t_{OX} indicates the gate thickness oxide. Meanwhile,

$$\omega = 2\pi f \quad \textbf{(3.3)}$$

$$W_{MT} \approx \frac{1}{3\omega L C_{ox} R_s} \quad \textbf{(3.4)}$$

3.5 Design Specification

The LNA is to be designed with the following proposed specification summarized in Table 3.1. Generally, the 0.13µm CMOS LNA is to be designed such as to comply with the wireless local area network (WLAN) specifications whereby the LNA needs to provide a high gain with low noise figure at low power, with its center operating frequency at 2.4 GHz.

Table 3.1: LNA Design Specification for WLAN Standard (IEEE802.11)

Parameter	Target specification
CMOS Process technology	0.13µm
Frequency band	2.4 GHz
Power supply	≤ 1.2 V
Gain, S_{21}	> 15 dB
Input matching50 ohm (S_{11})	< - 12 dB
Noise Figure	< 2.5 dB
IIP3	-12dBm
Power dissipation	< 8mW
Stability Factor	Should be unconditionally stable

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3.6 LNA Configuration Selection

3.6.1 Single Ended Cascode LNA

This LNA is constructed using an inductively degenerated cascode topology. The cascode topology is adopted as it provides high gain and good input-output isolation, which improve circuit design stability and also simplify input matching. The simplified schematic of the proposed CMOS LNA for noise optimization and gain enhancement is illustrated in Figure 1(a) and the simplified small-signal equivalent circuit is shown in Figure 1 (b) where V_{RF} and R_S model the antenna. LNA is to be designed for WLAN application.

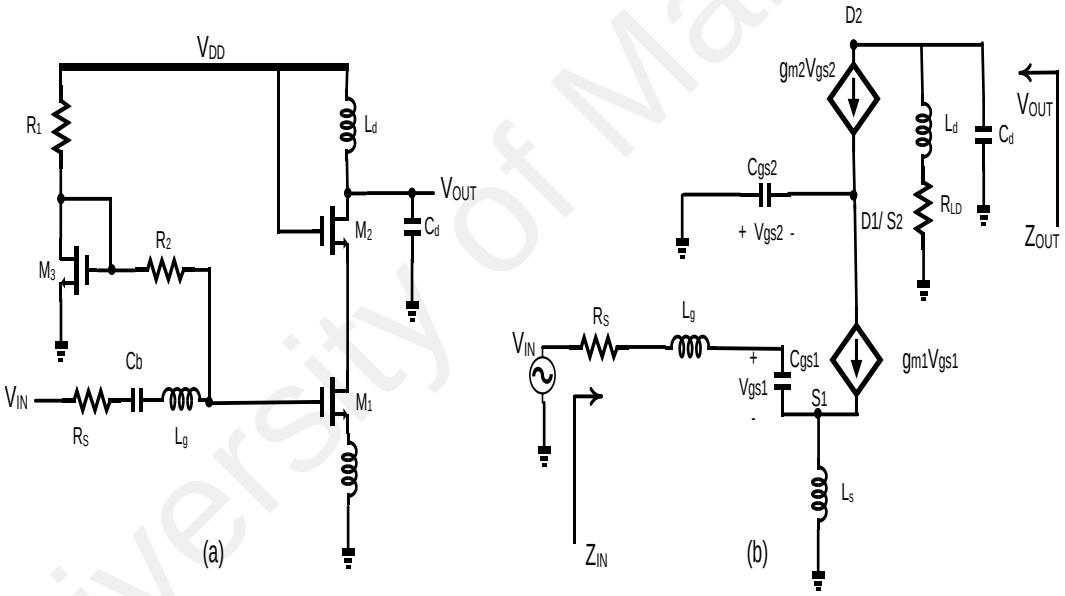

Figure 3.4: Simplified configuration of (a) the proposed single ended LNA and (b) the small-signal equivalent circuit

3.6.2 Power-Constrained Noise Optimization (PCNO) Technique

The power dissipated (P_D) as a function of gate overdrive (V_{ov}) expression was derived by using drain current for short channel equation. The equation was further arranged to indicate P_D as a function of input quality factor (Q_{in}) of the LNA (Belostotski, Haslett, Leonid, & James, 2006; Norlaili Mohd. Noh & Zulkifli, 2007). The two

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relationships were transformed into curves which resulting the NF as a function of Q_{in}. The Noise Figure prediction versus quality factor, Q_{in} for several power dissipations where the contours of constant P_D relating to the noise figure, NF and the quality factor Q_{in} are shown in Figure 3.5. The derivation of the expressions for the optimum transistor width, optimum Q_{in} and the LNA noise factor has been elaborately discussed in (Jafarnejad et al., 2017) and is further adopted into the present work. Given a specified restriction on power consumption, this method should yield the optimum device that minimizes noise. The expressions are as presented in equations (3.5) till (3.9) (Low, Amplifier, Shaeffer, Member, & Lee, 1997),

$$P_D = V_{DD}V_{sat}\frac{3}{2\omega_o Q_s R_s}E_{sat}\left[\frac{\rho^2}{1+\rho}\right] \tag{3.5}$$

$$Q_{L,opt,PD} = |c|\sqrt{\frac{5\gamma}{\delta}}\left[1+\sqrt{1+\frac{3}{|c|^2}\left(1+\frac{\delta}{5\gamma}\right)}\right] \tag{3.6}$$

$$W_{M1,opt,PD} = \left[\frac{2}{3}\omega_0 L C_{ox} R_s Q_{L,opt,PD}\right]^{-1} \tag{3.7}$$

$$F = 1+\frac{R_1}{R_2}+\frac{R_g}{R_s}+\frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_0}{\omega_T}\right) \tag{3.8}$$

$$\boldsymbol{\chi = 1+2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}}+\frac{\delta\alpha^2}{5\gamma}(1+Q_L{}^2)} \tag{3.9}$$

Where $Q_{L,opt,PD}$ is the optimum input network quality factor, $W_{M1,opt,PD}$ is the optimum width of the M_1 transistor, F is the noise factor, c is the correlation coefficient, where it is ≈ 0.395j exact for long-channel devices, γ is the bias-dependent factor, which

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is much greater than 2/3 for short-channel devices, δ is the coefficient of gate noise, ωo is the resonant frequency, L is the effective length of the device, C_{ox} is the oxide capacitance, Rs is the source resistance, which equals to 50 Ω, R_l and R_g are the losses due to inductor resistances and gate resistances respectively.

As only the positive value is considered, $Q_{in,\ PDmin} = 3.92 \approx 4.00$. Hence, it is clearly seen that the Q_{in} at the minimum P_D does not depend on the frequency, transistor size, process or noise factor due to canceling the effect. This is the optimum Q_{in} for each NF as P_D is at its minimum. From (3.6) , the optimum Q_{in} of the 0.13μm CMOS transistor for a power dissipation of 1mW is 3.9 and hence a corresponding minimum noise figure of 2.05 dB is extrapolated from Figure 3.5. Note that the predicted noise figure neglects any contribution of parasitic losses, particularly due to on-chip spiral inductors, to the noise factor which will eventually influence the noise figure of the LNA. Accordingly, the amplifier will possess a noise figure which is greater than 2.05 dB due to the losses of the input network, the noise contributions of the cascoding device, M_2 and the noise contributions of the output buffer.

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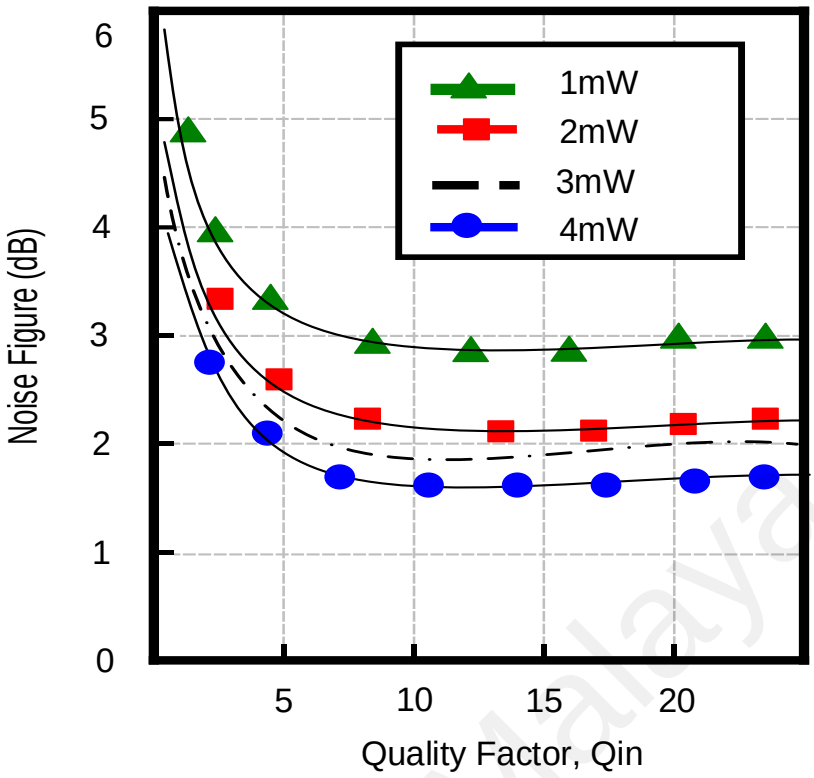

Figure 3.5: Theoretical prediction of the noise figure for several power dissipations. L=0.13 µm, R_S=50Ω, ω_o = 15.08 Grps, V_{DD} = 1.2 V, γ = 2, δ = 4, |c| = 0.395. An optimum Q_{in} of 3.9 is obtained.

The size of transistor determines the optimum input noise match or , specifically sets the Q_{in}. The width of transistor, W is optimized in the simulation under a fixed biasing current and its value is determined by using the method call power-constraint noise optimization (Shaeffer & Lee, 1997). An approach to this optimization method is to assume a fixed power consumption. This method is implemented to estimate the amount of noise figure degradation which must be tolerated in exchanged for reduced power consumption. Note that the predicted noise figure neglects any contribution of parasitic losses, particularly due to on-chip spiral inductors, to the noise factor which will eventually influence the noise figure of the LNA.

The gate-to-source bias V_{gs} was determined by referring to the physics-based transconductance-to-current ratio (g_m/I_D) characteristics. The performance of the devices in the circuit are directly related to the g_m/I_D characteristics whereby it offers a clear sign of the transistor operating region and a straight forward assessment of the transistor's bias

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point in order to obtain good trade-off between gain (g_m) and power (g_m/I_D). Figure 3.6 illustrates simulations based on the BSIM3v3 sub circuit model for the Silterra's (Malaysia) 0.13 μm RFCMOS process. The sub circuit consists of a DC MOS transistor core with BSIM3vs3 model and parasitic elements to predict both DC and RF characteristics. Figure 3.6 (a) exhibits the drain current, I_D of a 0.13 μm CMOS transistor model as a function of its gate voltage, V_{gs}. Figure 3.6(b) and Figure 3.6 (c) depicts the graphical representation of the transconductance and the transconductance efficiency of the 0.13 μm CMOS model respectively.

The threshold voltage, Vth of the transistor is around 0.288 V. Figure 3.6 (a) shows that at V_{gs} greater than 0.45 V, the I_D-V_{gs} curve becomes more linear compared to a quadratic curve that had formed immediately after passing the threshold voltage. This suggests that the circuit will attain better linearity when working the transistor at strong-to-moderate boundary inversion region gate bias voltage. In order to relate device performance to power consumption, the transconductance efficiency (gm/I_D) curve is presented. The gm/I_D ratio is a measure of the efficiency to translate current, which indirectly leads to power, into transconductance. The greater the gm/I_D value is, the greater the transconductance obtained at a constant current value. Therefore, the gm/I_D is expressed as a measure of the transconductance generation efficiency. It is evident from Figure 3.6(c) that the transconductance efficiency decreases towards strong inversion. To exploit the high characteristic of gm/I_D, it is imminent to work the transistor in the subthreshold region. The benefit gained from this optimization is that the power dissipation will be smaller, but the loss will be on lower linearity (IIP_3) and ω_T.

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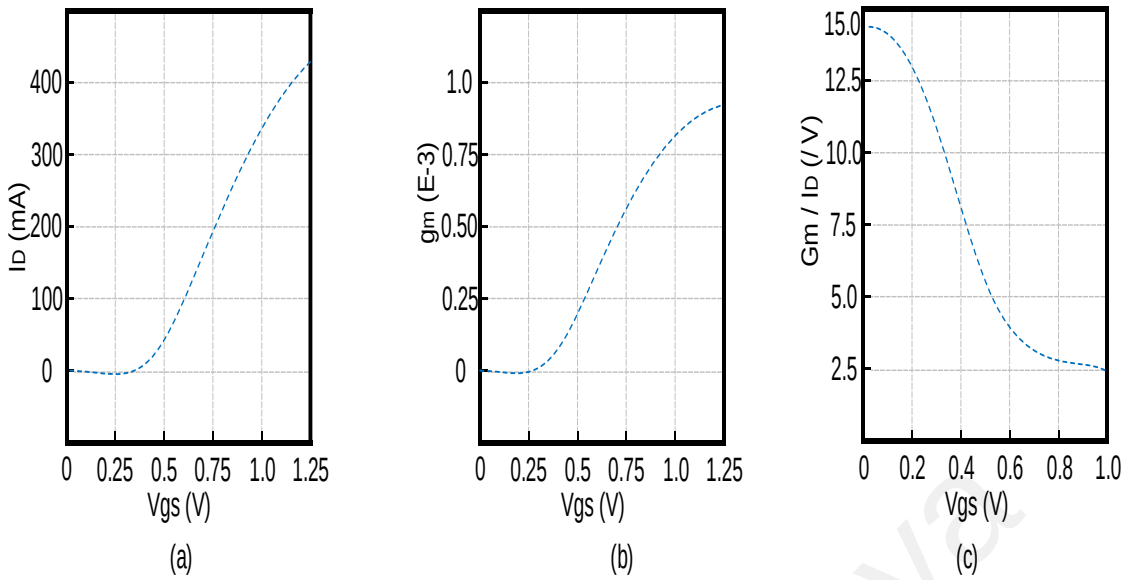

Figure 3.6: Graphical Representation of (a) Drain Current (I_D) (b) Transconductance (gm) (c) Transconductance Efficiency (gm/ I_D) versus the gate bias voltage, V_{gs} for the 0.13µm CMOS model.

The current density, I_{den} is given by $I_D/(W/L)$ where I_D is the drain current while W and L are the width and length of the transistor device, respectively. Typically, L is chosen to be the minimum length of the technology, and hence I_{den} can be expressed as I_D /W as given in expression (3.9)(Shim & Jeong, 2017).

$$I_D = I_{den}W \tag{3.10}$$

$$P_D = I_D V_{dd} \tag{3.11}$$

The gate inductor, Lg and the source degeneration inductor L_S are designed by finding the estimate of the input impedance Zin given by (3.12) (Norlaili Mohd. Noh & Zulkifli, 2007) using the small signal model in Figure 2.6(b). Body effect and the channel-length modulation are assumed to be small for this estimation.

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$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \omega_t L_s \quad \textbf{(3.12)}$$

The input impedance is that of a series RLC network, with a resistive term directly proportional to the inductance value. L_S is determined by equating the real part of the input impedance to R_S, as in (3.12)(Yan et al., 2017):

$$Re\{Z_{in}\} = \omega_T L_s = R_s = 50\Omega \quad \textbf{(3.13)}$$

Where ω_T is the transition frequency. Once L_S is found, L_g is obtained by setting the imaginary part of Z_{in} to zero as in **(3.14)**, yielding**(3.16)**:

$$Im\{Z_m\} = \frac{1}{\omega_0 C_{gs}} + \omega_0(L_s + L_g) = 0 \quad \textbf{(3.14)}$$

$$L_g = \frac{1}{{\omega_0}^2 C_{gs}} - L_s \quad \textbf{(3.15)}$$

The components of the tank circuit, C_T and L_T are calculated as given below:

$$\omega_0 = \frac{1}{\sqrt{L_T C_T}} \quad \textbf{(3.16)}$$

3.6.3 Differential PCSNIM

Power-Constrained Simultaneous Noise and Input Matching (PCSNIM) technique is further adopted onto the proposed design to further reduce the noise and enhance the gain. An additional capacitor C_{ex} is introduced into the LNA design and is located between the gate and the source of the common source transistor, M_1. The difference between the SNIM and PCSNIM is the additional C_{ex} in parallel with C_{gs}. In this technique, even if the transistor is small in size and resulting in small Cgs, noise and input matching can still be achieved by manipulating the value of C_{ex}. Figure 3.7 illustrates the modified differential PCSNIM with gain enhancement circuit.

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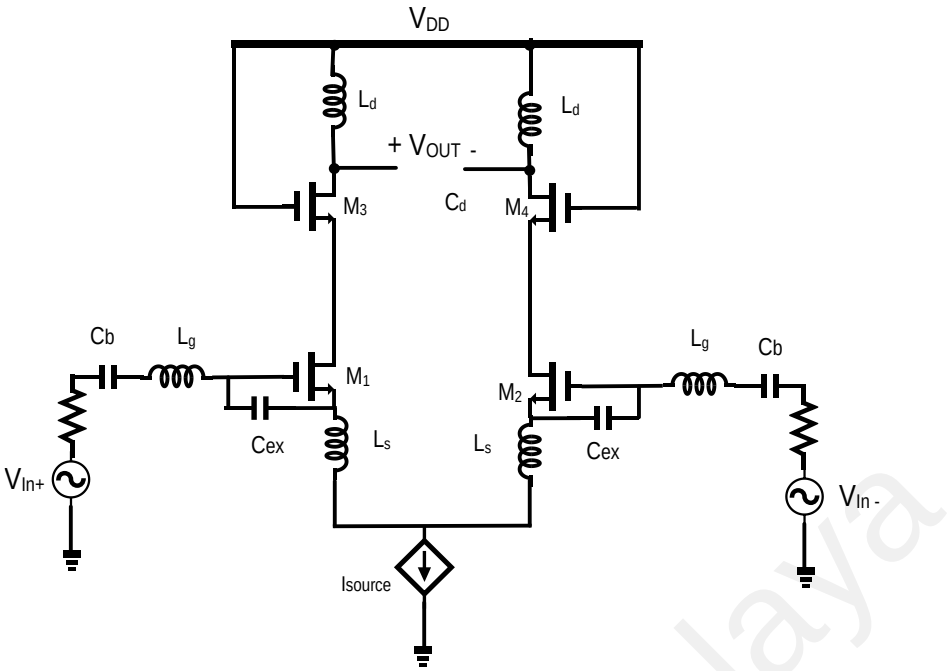

Figure 3.7: Modified differential PCSNIM with gain enhancement

The value of C_{ex} is chosen by considering the compromise between the size of L_S and the available power gain. A small value of C_{ex} has been chosen for a large value may lead to gain reduction due to the degradation of the effective cutoff frequency of the transistor (Nguyen et al., 2004). The conditions that allow simultaneous noise and input matching are as below (Norlaili Mohd Noh, Hashim, Tan, & Tan, 2010):

$$Re[Z_s] = \frac{\alpha\sqrt{\frac{\delta}{5\gamma(1-|c|^2)}}}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\frac{C_{tot}}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} \quad \textbf{(3.17)}$$

$$Im[Z_s] = \frac{j\left(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\frac{C_{tot}}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} \quad \textbf{(3.18)}$$

$$Re[Z_s] = \frac{g_m L_s}{C_{tot}} \quad \textbf{(3.19)}$$

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$$-Im[Z_s] = sL_s + \frac{1}{sC_{tot}} \tag{3.20}$$

Here, $\alpha = g_m / g_{do}$ where g_m is the device transconductance and gdo is the zero-bias drain conductance, δ is the coefficient of gate noise , γ is the coefficient of the channel thermal noise, c is the correlation coefficient of the gate noise and drain noise and $C_{tot} = C_{gs} + C_{ex}$. The design parameters that satisfy **(3.17)** to **(3.19)** are V_{gs}, W (or C_{gs}), L_S and C_{ex}. These expressions can be solved for an arbitrary value of Z_S, by fixing the value of one of the design parameters which can either be the power dissipation or the gate bias voltage, V_{gs}. Hence, this LNA design optimization technique allows simultaneous noise and input matching design at any level of power dissipation.

The gain of the LNA is given in the equation (3.21) below; (Nguyen et al., 2004)

$$A_v = G_m Z_L \tag{3.21}$$

where the expression for the overall stage transconductance G_m is given in the equation below;

$$G_m = g_{m1} Q_m = \frac{\omega_T}{\omega_0 R_s\left(1 + \omega_T \frac{L_S}{R_S}\right)} = \frac{\omega_T}{2\omega_0 C_{gs}} \tag{3.22}$$

Equations **(3.23**) till **(3.25**) present the noise parameters of a circuit implementing the PCSNIM technique.

$$R_n = \frac{\gamma}{\alpha}\frac{1}{g_m} \tag{3.23}$$

$$Z_{opt} = \frac{\alpha\sqrt{\frac{\delta}{5\gamma(1-|c|^2}} + j\left(\frac{C_{tot}}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\frac{C_{tot}}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} - sL_s \tag{3.24}$$

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$$F_{min=\ 1+\frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)}} \quad \textbf{(3.25)}$$

This justifies the notion introduced in equations above, revealing that the noise figure and the noise resistance, R_N are not greatly affected by the addition of C_{ex}. This differential LNA design adopts PCSNIM technique with inductively degenerated cascode topology. The design is focused in improving the linearity performance of the single ended LNA. By using this differential LNA topology, a new modified measurement approach will be introduced in measuring the fabricated chip. This is by using 2 ports conventional network analyzer where 2 ports will be terminated with 50Ω at a time. Data from this approach will be validated by using 4 ports network analyzer in order to confirm the method presented.

For a differential LNA, the circuit adopt cascode inductively degenerated topology which is the most preferred used topology. For simplicity, the biasing circuit of differential LNA is not shown in Figure 3.8.

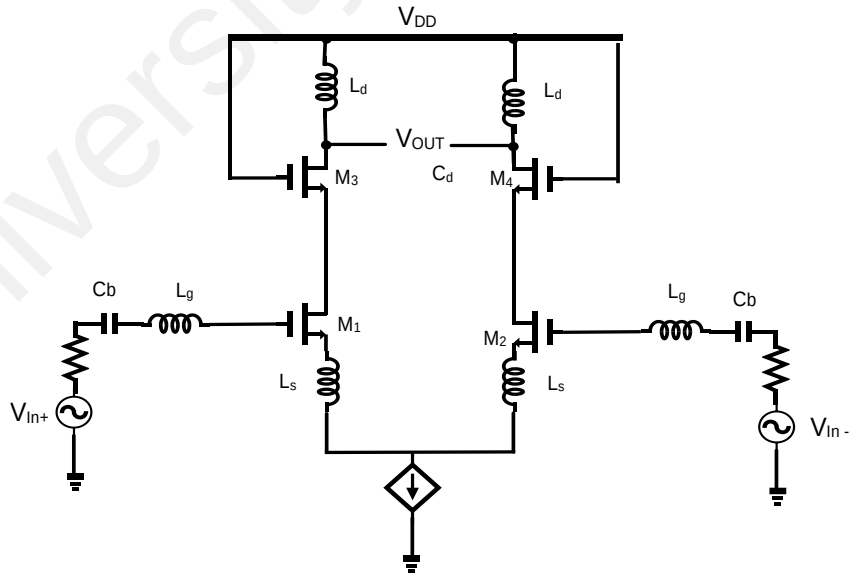

Figure 3.8: Inductively degenerated differential LNA

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3.6.3.1 S-parameter of four-port Differential LNA

Differential PCSNIM LNA designed in this work are double-ended thus it is four-port network device. The definitions of S-parameters have been expressed in terms of the input and output power waves of any electrical network. Differential LNA circuit can be characterized based on its response to differential and common mode signal. This include whichever mode of transformation. S-parameters is the most appropriate technique to characterize the nature of RF signal. Figure 3.9 shows an LNA device under test (DUT) which has been constructed as a basic four-port network and has been established in (Ka Mun, Vaz, & Caggiano, 2005).Equation **(3.26**) is the standard S-parameter illustration of this circuit network.

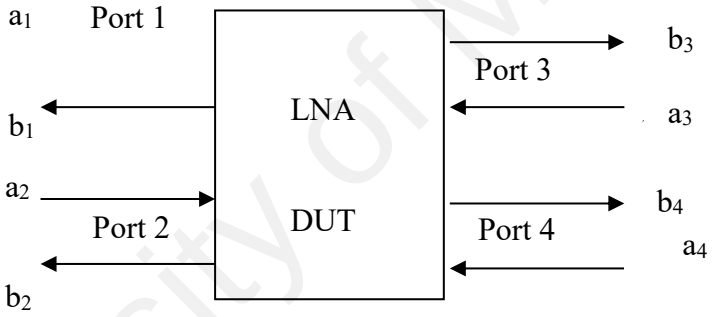

Figure 3.9: Structure of a four-port network

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \quad \textbf{(3.26)}$$

The relationship between two port network and four port network has been analyzed in (Belostotski & Haslett, 2008) .The 4 x 4 differential S-matrix is briefly summarized as stated in Figure 3.10. This is done by manipulating the definitions of differential voltages and currents into equation of power waves. S_{DD11} refers to the differential-mode return loss at differential port 1, S_{DD12} the differential insertion loss from differential port 2 to

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differential port 1, S_{DD21} the differential insertion loss from port 1 to port 2 and S_{DD22} the differential return loss at port 2. Another 12 S-parameters are described as DC referring to the differential to common-mode conversion, CD referring to the common-mode to differential-mode conversion and CC referring to the pure common-mode parameters. Figure 3.10 shows another technique of characterizing differential LNA networks with two-port VNA by utilizing a method of measuring the s-parameters of two ports at one time while the other two ports are terminated with 50 Ω.

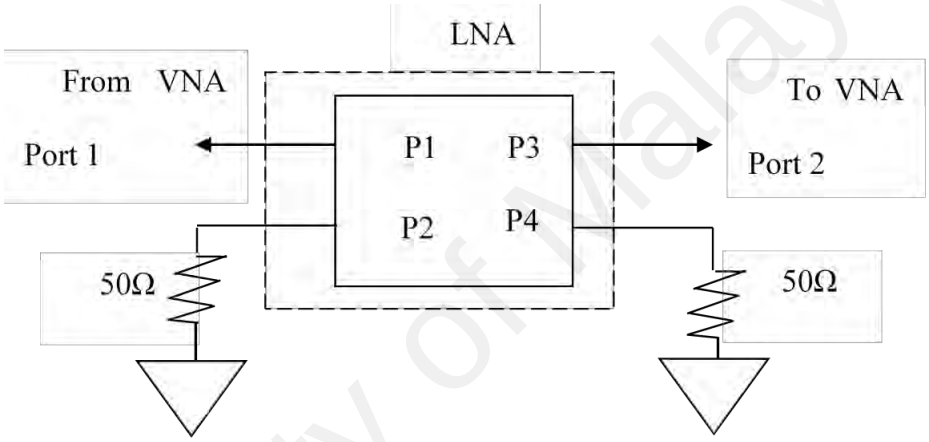

Figure 3.10: Differential LNA terminated with single-ended 50 Ω at each port

$$\begin{bmatrix} S_{DD11} & S_{DD12} & S_{DC11} & S_{DC12} \\ S_{DD21} & S_{DD22} & S_{DC21} & S_{DC22} \\ S_{CD11} & S_{CD12} & S_{CC11} & S_{CC12} \\ S_{CD21} & S_{CD22} & S_{CC21} & S_{CC22} \end{bmatrix} = \quad \textbf{(3.27)}$$

$$\frac{1}{2}\begin{bmatrix} (S_{11}-S_{12}-S_{21}+S_{22}) & (S_{13}-S_{14}-S_{23}+S_{24}) & (S_{11}+S_{12}-S_{21}-S_{22}) & (S_{113}+S_{14}-S_{21}-S_{24}) \\ (S_{31}-S_{32}-S_{41}+S_{42}) & (S_{11}-S_{34}-S_{43}+S_{44}) & (S_{33}+S_{32}-S_{41}-S_{42}) & (S_{33}+S_{34}-S_{43}-S_{44}) \\ (S_{11}-S_{12}+S_{21}-S_{22}) & (S_{13}-S_{14}+S_{23}-S_{24}) & (S_{11}+S_{12}+S_{21}+S_{22}) & (S_{13}+S_{14}+S_{23}+S_{24}) \\ (S_{31}-S_{32}+S_{41}-S_{42}) & (S_{33}-S_{34}+S_{43}-S_{44}) & (S_{31}+S_{32}+S_{41}+S_{42}) & (S_{33}+S_{34}+S_{43}+S_{44}) \end{bmatrix}$$

By using standard four-port VNA as in Figure 3.9 and two-port VNA as in Figure 3.10, measurement of the S-parameter is carried out. Both measurements were analyzed and compared. Four-port S-parameters data can be taken directly from the measurement.

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However, by using two-port VNA to measure differential LNA, six different measurement set ups are essential in order to calculate the relation between mixed-mode. In each set up, two ports of the LNA DUT are connected to any port of VNA, while the other remaining two ports are terminated to 50 Ω loads. Table 3.2 shows one of the six set up that needs to be done. For example, it shows S-parameters measurement of P_1 (port 1) and P_3 (port 3). With this set up, the S-parameters of P_1P_2, P_1P_3, P_1P_4, $_{P3P2}$ and P_3P_4 can be measured respectively. This measurement will take 24 s-parameters data in which the s-parameters data of S_{11}, S_{22}, S_{33} and S_{44} are tabulated and measured three times.

Table 3.2: Two-Port Set Up for S-Parameter Measurement

Port	Port 1	Port 2	Port 3	Port 4
(P_1P_3)	Input signal	Terminated with 50Ω	Input signal	Terminated with 50Ω
(P_2P_3)	Terminated with 50Ω	Input signal	Input signal	Terminated with 50Ω
(P_2P_4)	Terminated with 50Ω	Input signal	Terminated with 50Ω	Input signal
(P_1P_4)	Input signal	Terminated with 50Ω	Terminated with 50Ω	Input signal
(P_3P_4)	Terminated with 50Ω	Terminated with 50Ω	Input signal	Input signal
(P_1P_2)	Input signal	Input signal	Terminated with 50Ω	Terminated with 50Ω

3.6.4 Differential Cascode LNA using differential inductor

Another design that been consider in this research work shown in Figure 3.11. It is differential LNA that been implemented is using center-tap inductor or differential inductor. This is to study the effect of inductor performance to differential LNA circuit as compare to the previous design. Another significant advantage of this propose design shown below is that it enables less number of inductors used in a differential design. With normal inductors, the differential designs require 6 inductors for L_g, L_s and L_d on each side of the differential. With center-tap inductors, L_d and L_s from both sides of the differential are sharing the same inductor, respectively. Hence, only 4 inductors are used

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in this differential design thus it will lower chip area as we know that passive inductor consume larger chip area. This mark the contribution and improvement to the differential circuit design. The inductor implement in the layout design is generated based on Silterra's inductor model that can be tune to the selected required frequency (refer Appendix)

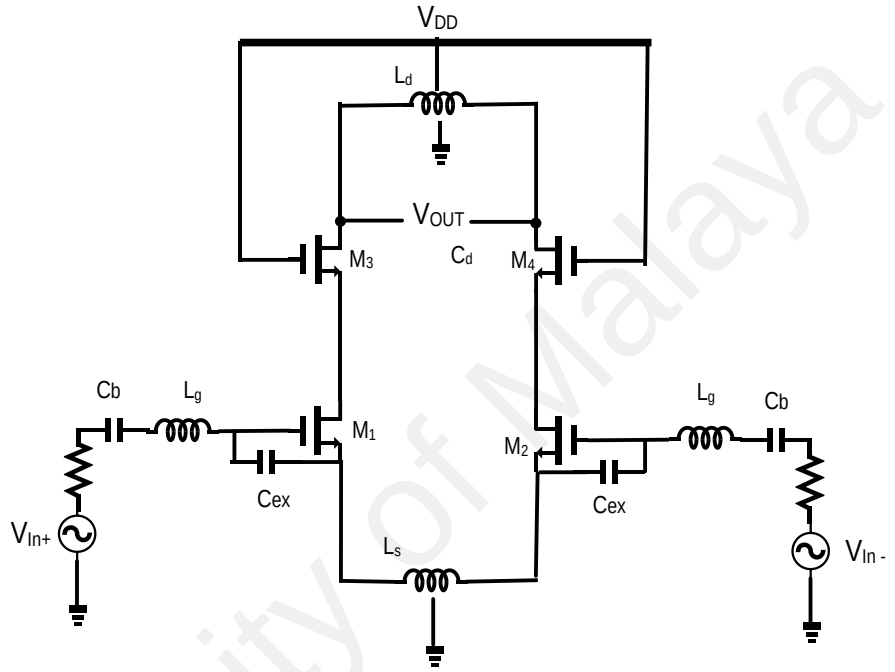

Figure 3.11: Schematic diagram of Differential Cascode using differential inductor

3.7 Post Layout Simulation Method

The importance of the pre-layout simulations is not to be denied. It gives the first confirmation on whether the circuit designed is functioning as required. However, this type of simulation does not include the effects of the parasitic, that by no means, absent in integrated circuits. As an example, the schematic editor does not have the information on the capacitance, resistance and routing of the wires. Especially in CMOS technology, the high conductivity of the silicon and substrate will reduce the quality factor of passive components and increase the substrate coupling of the circuit components which

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consequently will result in worse noise and performance degradation. Worse still, for deep sub-micron processes, the physical interconnects do not behave as ideal wires. They, in fact, resemble networks of capacitors and resistors. The parasitic that are represented by these resistors and capacitors will be affecting the noise performance as well as the frequency response of the circuit, including the gain and matching. In fact, the measured bandwidth of an amplifier may not reflect the value that the circuit was designed for if the parasitic at the critical nodes of the design were not minimalized through careful layout (Y. Koolivand A. Zahabi and P. J. Maralani, 2005).

The post-layout simulations conducted in this work were for the following purposes:

(i) To determine the effects on the LNA performance if extreme conditions were imposed on the passives and devices. This is to predict if the fabricated LNA is still able to perform according to the WLAN requirement if these conditions were to occur.

(ii) To determine the influences of the transistors' condition on the S-parameters.

(iii) To determine the effects of matching on the LNA's performance.

In this work, analysis was performed on the results of the post-layout simulations. Analysis were performed to understand the effects of the parasitic on the design. The post-layout simulations conducted in this work were performed by Calibre, which is a robust parasitic extraction tool that is widely used by the semiconductor industry in verifying their designs. Calibre will determine the parasitic to be included onto the designed layout and consequently, the extracted information of the layout with parasitic will be used to perform analog simulations.

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3.8 S-parameter Measurement Method

This section presents a technique that enables very accurate measurement for S-parameter of differential low noise amplifier by means of a standard two-port vector network analyzer (VNA). This technique involves by terminating two ports at one time while another two ports are measured. Accurate characterization of a two-port device requires a four-port vector network analyzer, which might be not easily available. Thus, it is a common practice to terminate the two of the four ports to be used which the conventional/standard two port VNA. Even though the above approach is applicable, but the reliability and conformity of the test method is still limited and uncertain. For verification, the measurement using four-port VNA have been conducted to test the devices S-parameters are accurately similar with the two-port network. The fabricated on-wafer differential LNA structure was tested and measured with normal two-port VNA and four-port VNA. By using this technique, any multi-port circuit network can be measured.

The pad diagram, such as shown in Figure 3.12, is required when characterizing the chip. The pads are all labeled in accordance to the layout of the LNA.

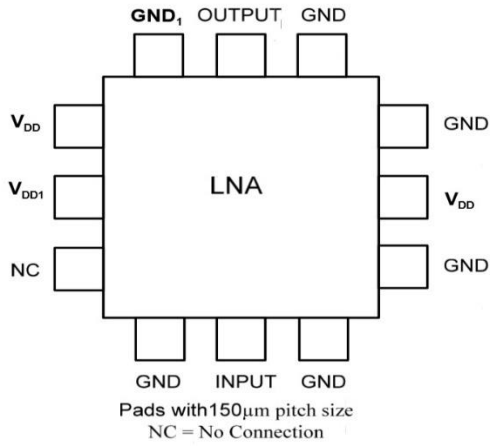

Figure 3.12: The general representation of bond pad diagram of the LNA die

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Figure 3.13 shows the layout of single-ended LNA together with the bond pad. This layout is implement using three Silterra's octagonal inductor.

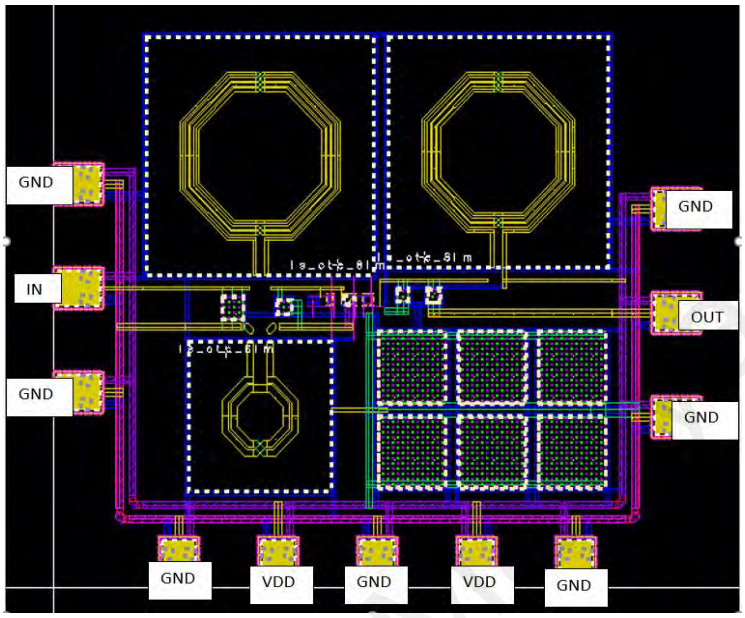

Figure 3.13: Layout representation of single-ended LNA with the bond pad

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3.9 DC measurement test set-up

The aim of this test is to find out the biasing of the LNA circuit. The measured current flowing through the cascode must be close to the one desired and used in the calculations. Only then, the circuit will be able to provide the expected performances. The set-up for the DC measurement is shown in Figure 3.14. Table 3.3 presents the expected reading during DC measurement test set-up.

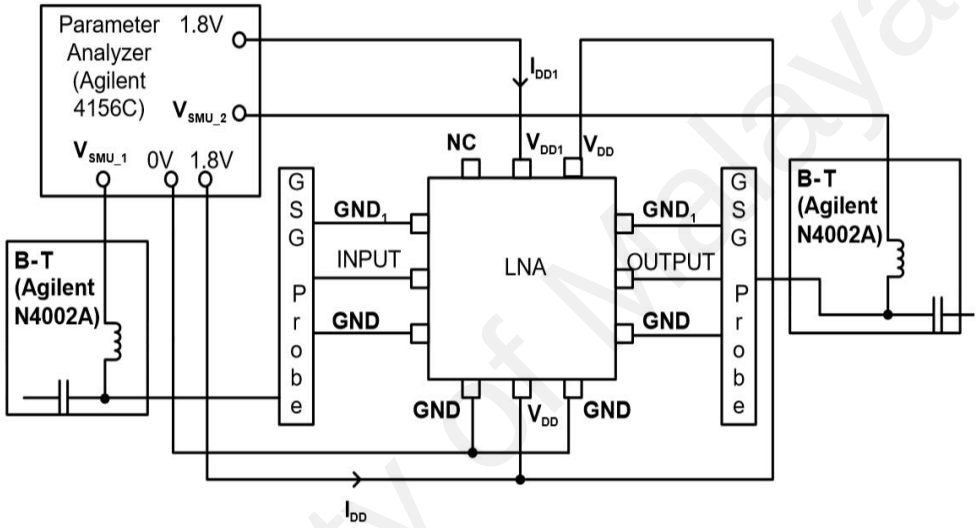

Figure 3.14: DC measurement test set-up

Table 3.3: Expected reading DC measurement test set-up

Voltage and current to be measured	Expected reading
V_{DD} (V)	1.2
I_{DD} (µA)	100-150
I_{DD1} (mA)	2-4
$V_{smu\ 1}$ (V)	0.5-0.55
$V_{smu\ 2}$ (V)	1.2

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3.10 S-Parameter Measurement test set-up

Figure 3.15 shows S-parameter measurement test set up for LNA. This set up was referred from Semiconductor MAXIM Application note. Some modification in the set up was performed to in order to suit the available equipment in the lab.

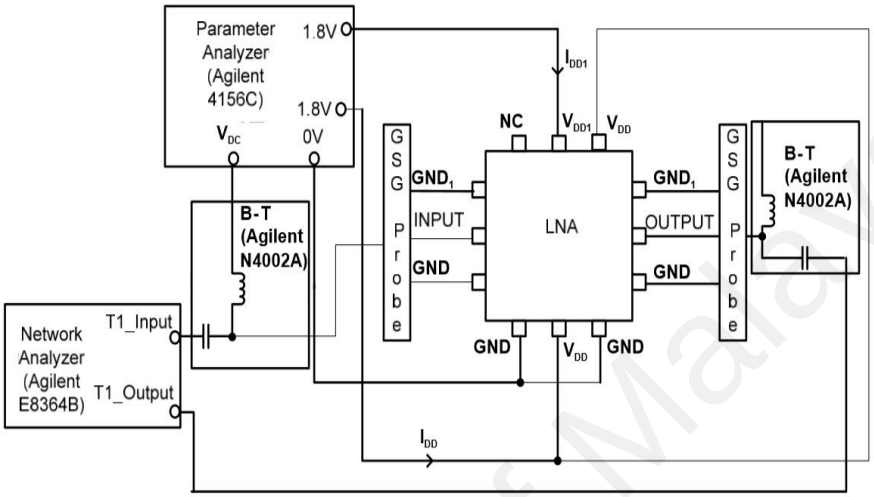

Figure 3.15: S-parameters measurement test set-up

Since the LNA is design differentially which require 2 input simultaneously at the same time, the measurement of the differential LNA cannot be done using a normal conventional method using 2 ports network analyser.

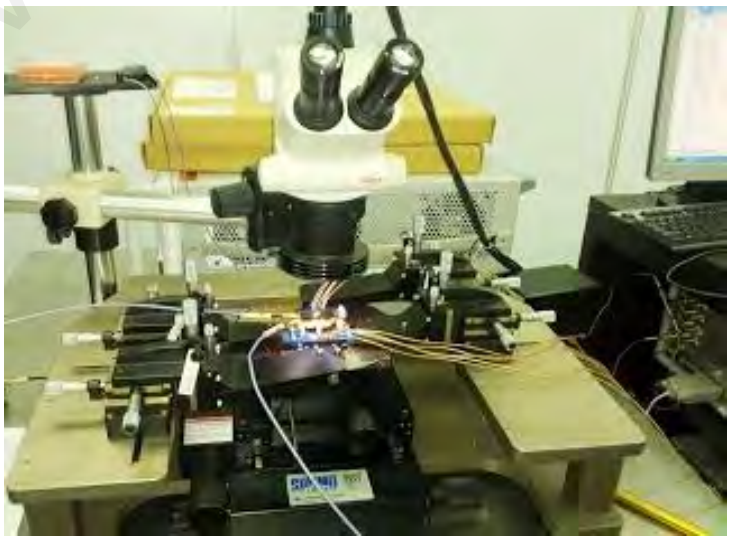

Figure 3.16: On wafer measurement

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Figure 3.17: Probe station using two-port network analyser

3.10.1 S-parameter measurement set-up for four-port network

Figure 3.18 illustrates the S-parameter measurement set up of four-port differential LNA using a two-port network analyzer.

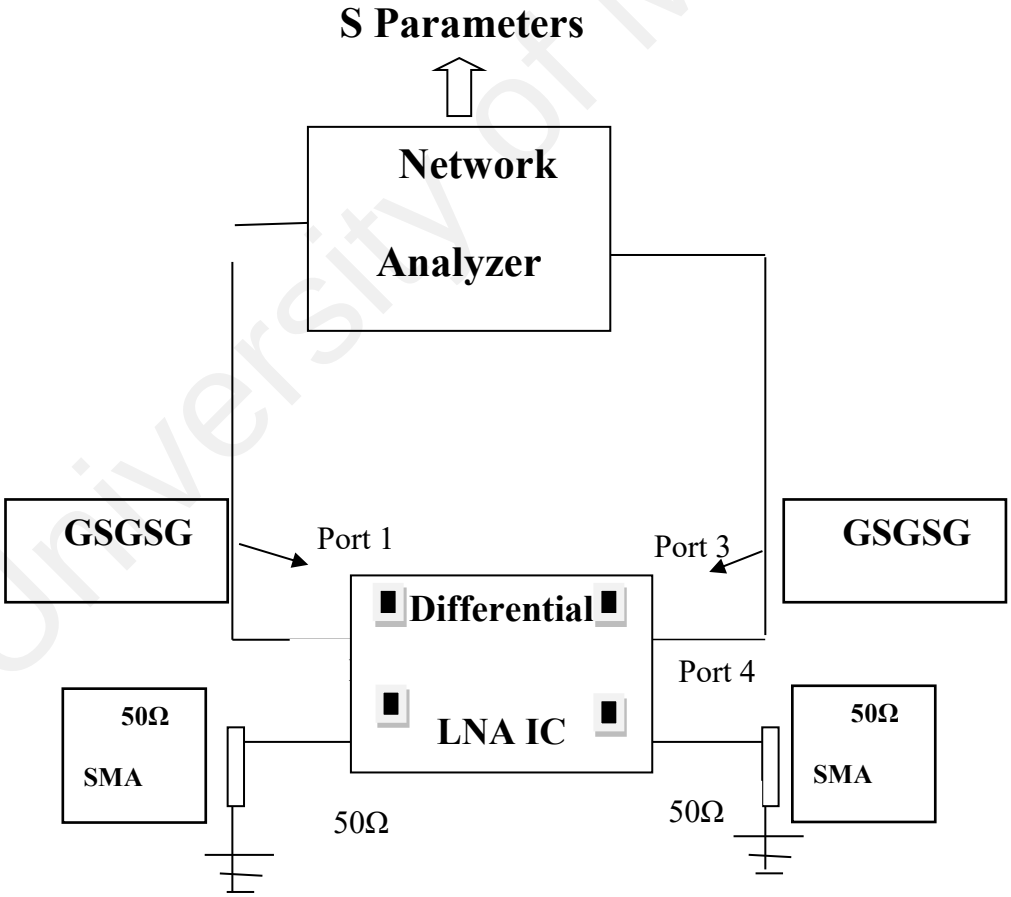

Figure 3.18: Test equipment setup for 4-port S-parameter measurement using two-port network analyzer

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The measurement procedures method starts by terminate the input port (eg: port 2) and output port (e.g: port 4) using auxiliary load 50 ohm. Next the sixteen combination of two-port measurements is taken (eg: S_{31}, S_{41}, S_{32} and S_{42}). Refer for the Table below that adapt from Table 3.2: Two-Port Set Up for S-Parameter Measurement to know which port that need to be terminated during the measurement. This measurement took 24 s-parameters data in which S_{11}, S_{22}, S_{33} and S_{44} are taken three times as in equation **(3.27)**.

$$\begin{matrix} S_{DD11} & S_{DD12} & S_{DC11} & S_{DC12} \\ S_{DD21} & S_{DD22} & S_{DC21} & S_{DC22} \\ S_{CD11} & S_{CD12} & S_{CC11} & S_{CC12} \\ S_{CD21} & S_{CD22} & S_{CC21} & S_{CC22} \end{matrix} = \begin{matrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{matrix} \quad \textbf{(3.28)}$$

3.11 Set-up for noise measurement

Noise figure of the LNA is measured by using the setup such as shown in Figure 3.19. Modifications to the set-up was performed to incorporate the existing equipment available in the lab. The wafer has to be placed on a probe table as the cable. The basic set-up for the noise measurement was obtained from Dallas Semiconductor MAXIM Application Note 3571 (Dallas Semiconductor, 2005) and Ganesan (2006, 2007).

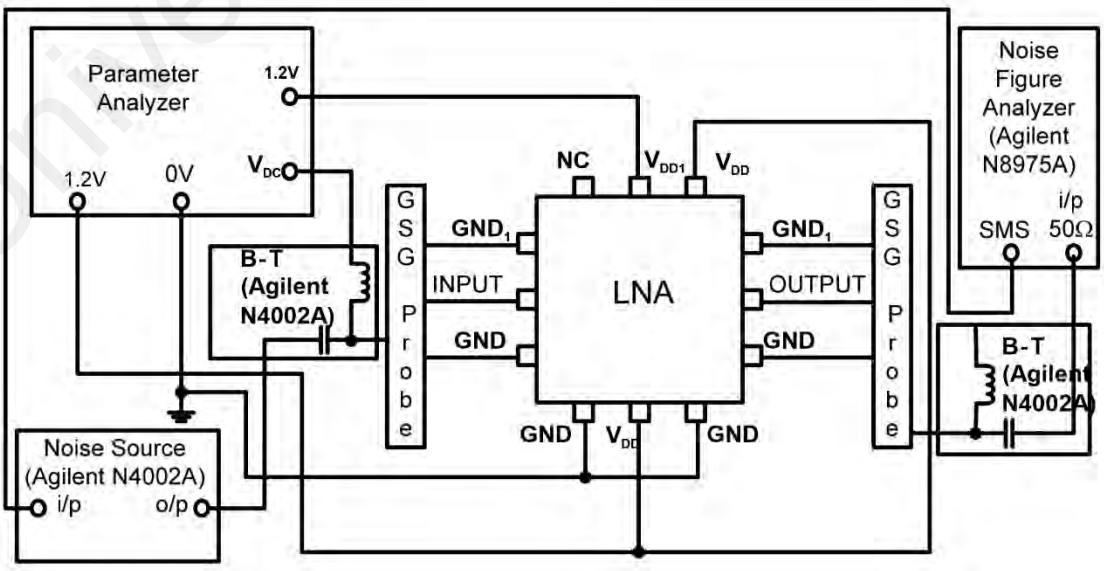

Figure 3.19: Test-setup for the measurement of noise

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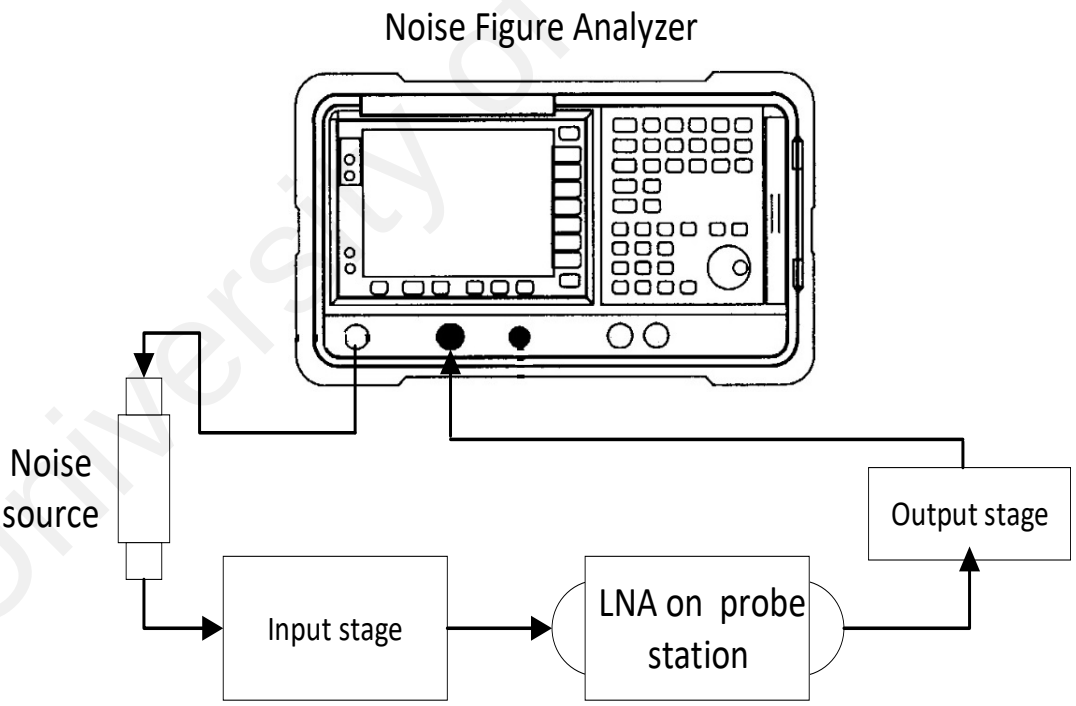
3.12 Noise figure de-embedding technique measurement

A basic two-port true differential mode concept with correlation is presented. The equation **(2.29)** is modified by introducing true differential mode concept to suit the generalized cascade two-port Friis equation **(3.33)** (Rastegar et al., 2013). And it leads a straightforward and simple approach to measure differential NF. This testing procedure can be performed repeatedly with high accuracy, and the results are compared with other methods. The NF de-embedding measurement technique was done as shown in Figure 3.20.

$$NF = 10\, log_{10}\left(\frac{SNR_{IN}}{SNR_{OUT}}\right) \quad \textbf{(3.29)}$$



(a)

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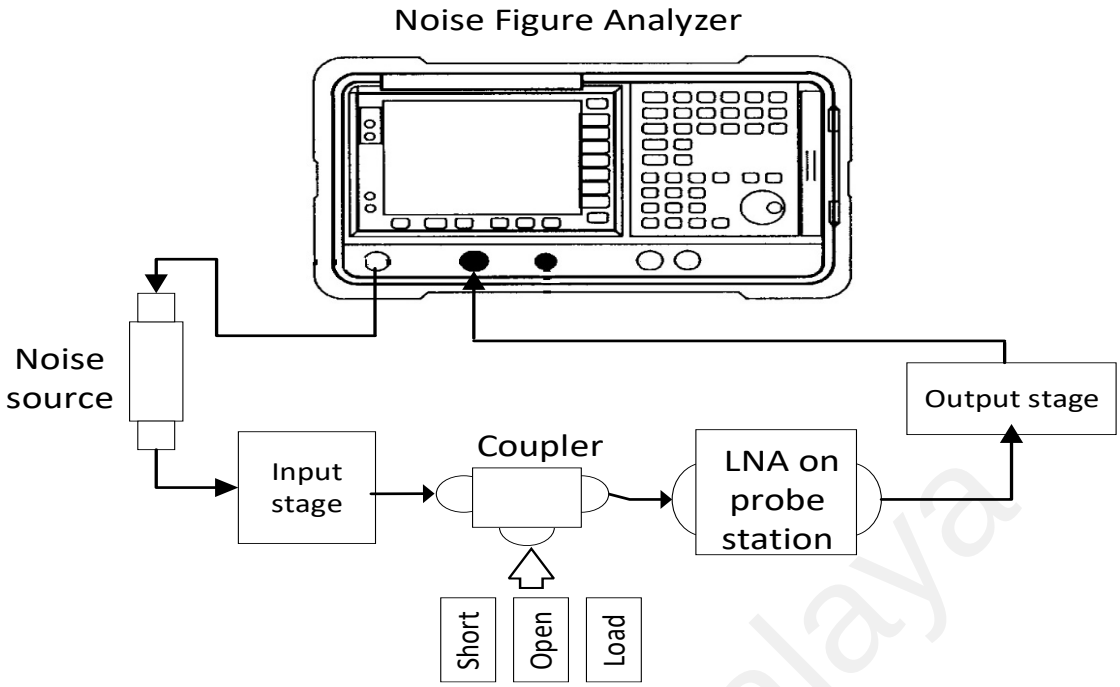
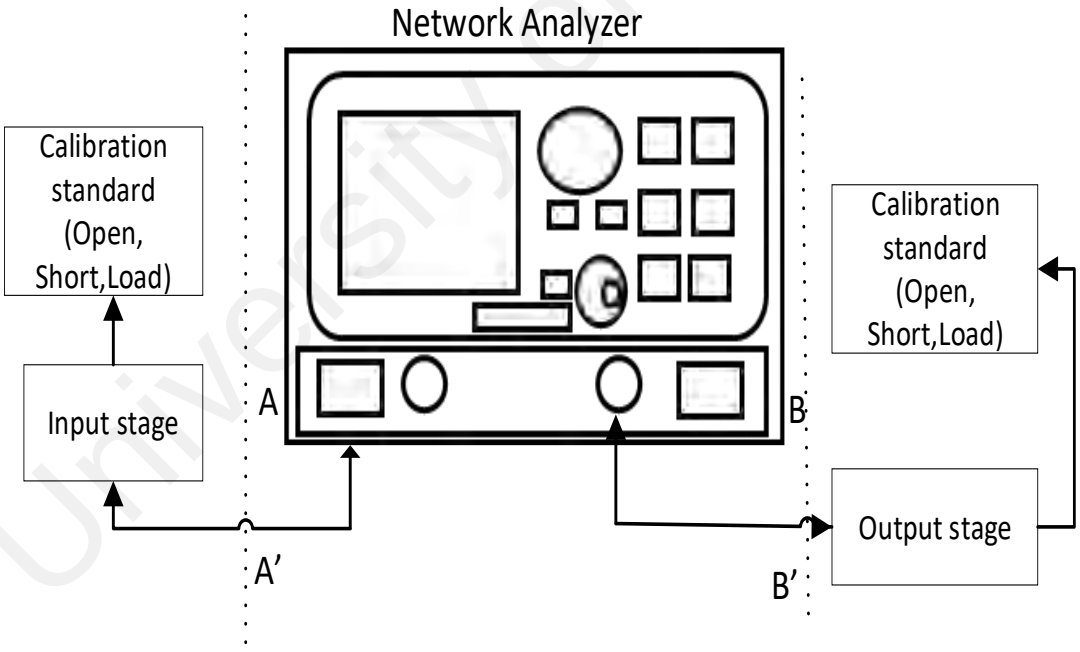


(b)



(C)

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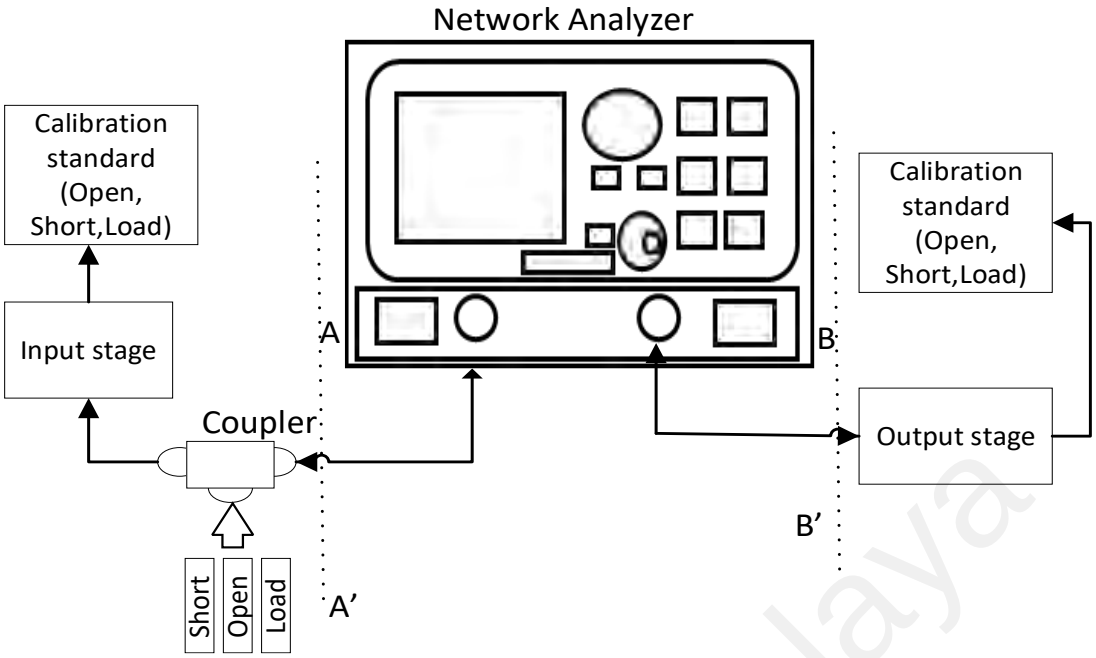

(d)

Figure 3.20: Measurement set-up for noise figure analysis (Korakkottil Kunhi Mohd, Zulkifli, & Sidek, 2010) **; (a) On-wafer noise figure measurement set-up, (b) Noise set-up with different input reflection coefficient, (c) S-parameter measurement set-up, (d)Network set-up with different input reflection coefficient**

Figure 3.21 shows the flowchart of the on-wafer NF measurement de-embedding procedures.

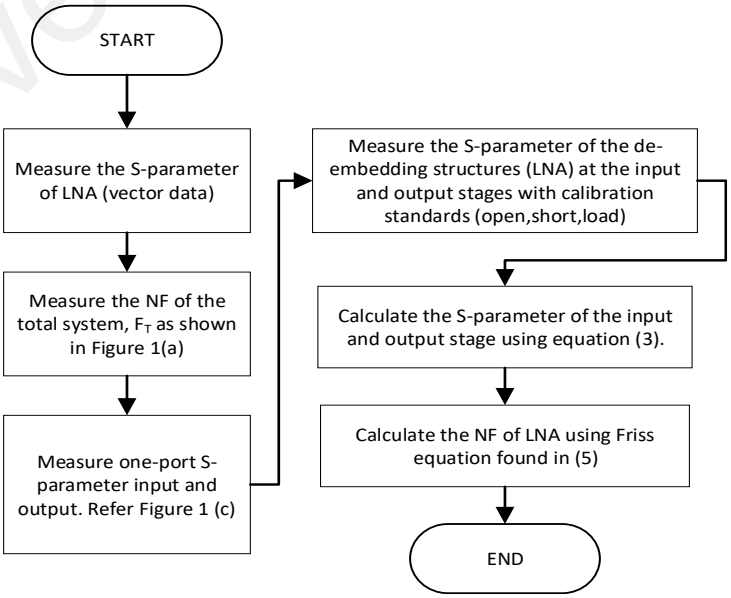

Figure 3.21: Flowchart of the de-embedding NF on-wafer measurement

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For the LNA circuit, the procedures start with the measurement of S-parameter. Then, the NF of the total system (F_T) is measured for both input and output stages. This is shown in Figure 3.20. Next step is to measure a one-port S-parameter for both input and output stages as illustrated in Figure 3.20(c). The network analyser needs to be calibrated using mechanical calibration kit at position (A-A') and (B-B') planes by referring to the figure set-up. The s-parameter of the differential LNA at the input stage and output stages represented by $S_{11}^{OPEN}, S_{11}^{SHORT}, S_{11}^{LOAD}, S_{22}^{OPEN}, S_{22}^{SHORT}$ and S_{22}^{LOAD} which is referring to the calibration standards (open, short, load). By using the following expression below, the calculation of the S-parameter can be achieved for both input and output stages (Korakkottil Kunhi Mohd et al., 2010). $S_{11}^{LOAD}, S_{11}^{OPEN}$ and S_{11}^{SHORT} represent the input stage of the S-parameters during the probe is connected to the load, open and short calibration standard. The same method follows for the S-parameters at the output stage. Determination of the NF of the LNA can be determined using the Friss equation in **(3.31)**.

$$S_{11}^{IN} = S_{11}^{LOAD} \tag{3.30}$$

$$S_{22}^{IN} = \frac{S_{11}^{LOAD} + S_{11}^{SHORT} + 2S_{11}^{IN}}{S_{11}^{OPEN} - S_{11}^{SHORT}} \tag{3.31}$$

$$S_{12}^{IN} = S_{21}^{IN} = \sqrt{(S_{11}^{OPEN} - S_{IN}^{IN})(1 - S_{22}^{IN})} \tag{3.32}$$

$$F_T = F_{IN} + \frac{F_{LNA} - 1}{G_{IN}} + \frac{F_{OUT} - 1}{G_{IN} G_{LNA}} \tag{3.33}$$

F_{IN} is the noise factor of the input stage and G_{IN} is the available gain of the input stage. Whereas F_{out} is the noise factor at output stage, F_T is the total network noise factor. F_{LNA} and G_{LNA} are the noise factor and gain of the differential LNA respectively. Rearranging

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from equation (3.31), the noise factor of the LNA, F_{LNA} can be determined using the following expressions:

$$F_{LNA} = G_{IN}F_T - \frac{1 - G_{OUT}}{G_{OUT}G_{LNA}} \quad \textbf{(3.34)}$$

G_{IN}, G_{OUT} and G_{LNA} were calculated from (Jianjun et al., 2003):

$$G_{IN} = \frac{|S_{21}^{IN}|^2}{1 - |S_{22}^{IN}|^2} \quad \textbf{(3.35)}$$

and

$$G_{OUT} = \frac{|S_{21}^{OUT}|^2}{1 - |S_{22}^{OUT}|^2} \quad \textbf{(3.36)}$$

where

$$G_{LNA} = \frac{|S_{21}^{LNA}|^2\,(1 - |S_{22}^{IN}|^2)}{|1 - S_{11}^{LNA}\,S_{22}^{IN}|^2(1 - |S_{22}|^2)} \quad \textbf{(3.37)}$$

and

$$S_{22} = S_{22}^{LNA} + \frac{S_{12}^{LNA}\,S_{21}^{LNA}\,|S_{22}^{IN}|}{1 - S_{11}^{LNA}\,|S_{22}^{IN}|} \quad \textbf{(3.38)}$$

G_{LNA} used in the equation (3.35) is the available gain. The noise figure is recalculated using G_{LNA} as the insertion gain for the analysis of the gain uncertainty. The influence of the measurement data under mismatch situations measurement can be studied by measuring NF under three different impedances as illustrated in Figure Figure 3.20(b) and Figure 3.20(d).

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3.13 Conclusion

In this chapter, a methodology to design and characterize LNA for WLAN / IEEE 802.11b/g standard was presented. The operating frequency is in the range 1-4GHz with center frequency at 2.4GHz. The work start by selection of the LNA topology. Inductively degenerated cascode common source topology has been chosen as the initial design topology. This topology also known as SNIM (simultaneously noise input matching). Then, designing single-ended LNA based on the selected configuration. Several design techniques was employed such as power constraint noise optimization (PCNO). The evaluation and optimization of the single ended LNA is performed to ensure the performance achieved specification requirement set by WLAN standard. The second part of the research work is to design differential LNA based on the optimized single-ended LNA configuration implemented in the first part. This differential LNA was further developed using power constrained simultaneous noise and input matching (PCSNIM) in order to reduce the noise and lower the power consumption of the design. The differential LNA PCSNIM was further evaluate and optimized by comparing with another topology design. The noise figure of the fabricated differential LNA chip was measured using de-embedding technique that was developed in this research to reduce the interference of noise into the system. On-wafer s-parameter characterization of this four-port differential LNA was measured using two-port vector network analyzer. This measurement technique is one of the contributions in this research work and will further explain in the later section.

On-wafer de-embedding measurement technique for differential LNA with the analysis of two gain definition was also presented. The detailed procedure and set up of the de-embedding technique were proposed utilizing the scattering parameter.

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CHAPTER 4: RESULT AND DISCUSSION

4.1 Introduction

This chapter presents the findings obtained from this work. The result and discussion will be divided into four parts. The first part will highlight the schematic circuit design (pre) simulation, post-layout simulation and measurement result of single ended PCSNIM LNA based on PCNO technique where PCSNIM were employed in this design. The second part is focused on the pre, post-simulation and measurement on differential PCSNIM LNA design. The analysis will emphasize on the measurement technique of the S-parameter and noise figure and de-embedding technique effects on noise figure measurement. Meanwhile, the third part will present the performance of the differential PCSNIM LNA that using differential inductor. Lastly, the comparison between the this work and published works are shown focusing on the s-parameter, noise figure and IIP_3 of the LNA. This work was implemented using Cadence SpectreRF with the model libraries from Silterra's 1-poly 6-metal 0.13 μm CMOS process. All CMOS process enables a high level of circuit integration. The features from the SpectreRF used were the Composer for schematic editing, Analog Design Environment (ADE) as the simulator and finally the Virtuoso for layout editing.

Pre-layout and post-layout simulations and measurements were performed on the single ended LNA as shown in Figure 4.1 and the PCSNIM LNA as in Figure 4.3. The PCSNIM differential LNA in Figure 4.4, and the modified PCSNIM with output buffer LNA in Figure 4.5 performances were determined from post-layout simulations. The LNAs performances are compared with the specifications set by the W-LAN standard to determine whether the LNAs in this work conform to the design specifications. The LNAs components and parameters were given in Table 3.1: LNA Design Specification for WLAN Standard (IEEE802.11).

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4.2 Pre and Post Simulation Performance of Single Ended PCSNIM LNA

Pre-layout simulations in this work were performed to investigate on the following issues:

- The current versus voltage (I-V) characteristics of the 290 µm / 0.13 µm. This is important as the amount of voltage to ON the transistor and the amount of current that flows at this voltage needs to be determined.
- The size of the transistor to be placed in the current mirror in order to bias the transistors in the cascode of the LNA.
- The functionality and the performance of the LNA in terms of the S-parameters, noise and linearity. As generally known, the fluctuations in integrated capacitors, resistors and transconductance are about 10% to 20% from their designed values due to the process variations. These variations are, hence, very important to be considered when designing integrated circuits. Not only the performance of the circuit influenced by the process, it is also affected by the voltage and temperature variations.

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4.2.1 S-Parameter and Noise Figure

Simulations were performed on the schematic such as shown in Figure 4.1. The component value and the device size were calculated following the methodology described in Chapter 3. The S-parameter plots, noise and IIP3 performances are shown in Figure 4.1 to Figure 4.8 respectively. As can be seen from Figure 4.1, the circuit's input and output were matched to the 50Ω required at the operating frequency of 2.4 GHz.

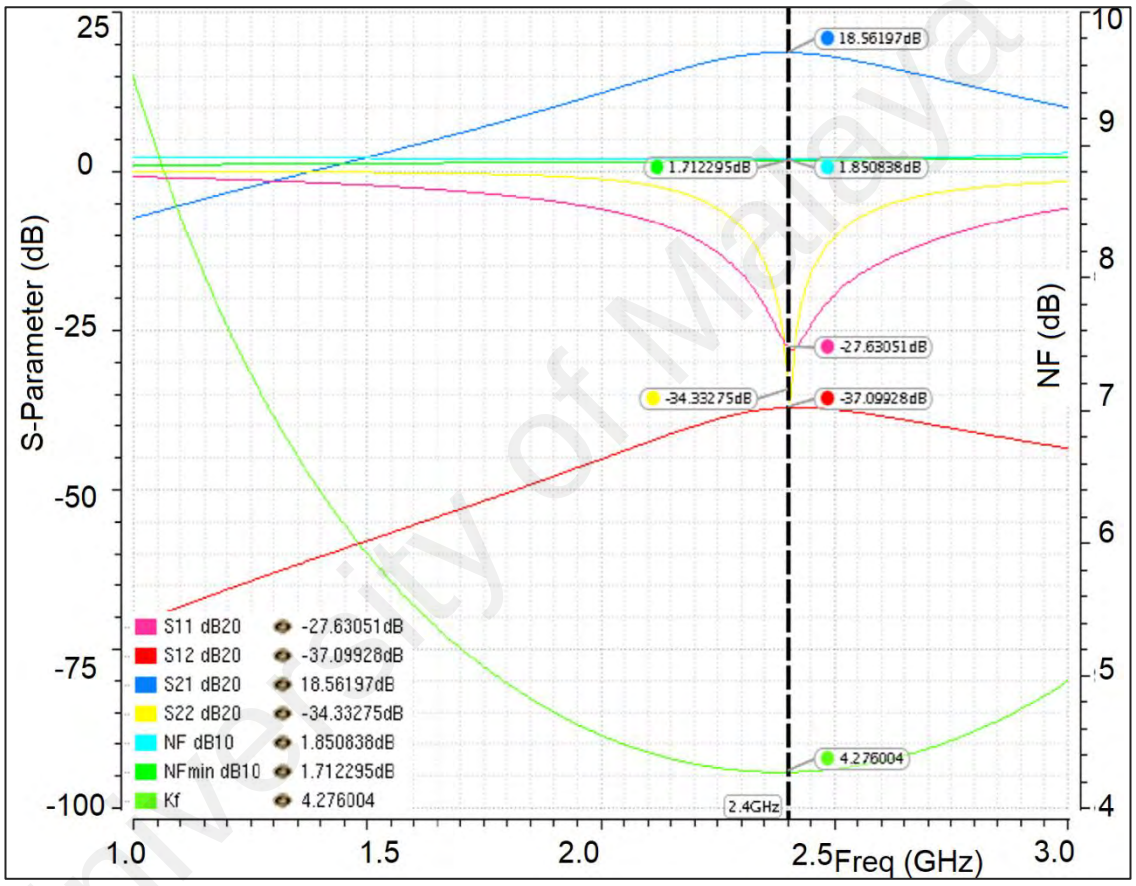

Figure 4.1: Graph of simulated NF and s-parameter for pre-layout performance of single-ended LNA at 2.4GHz

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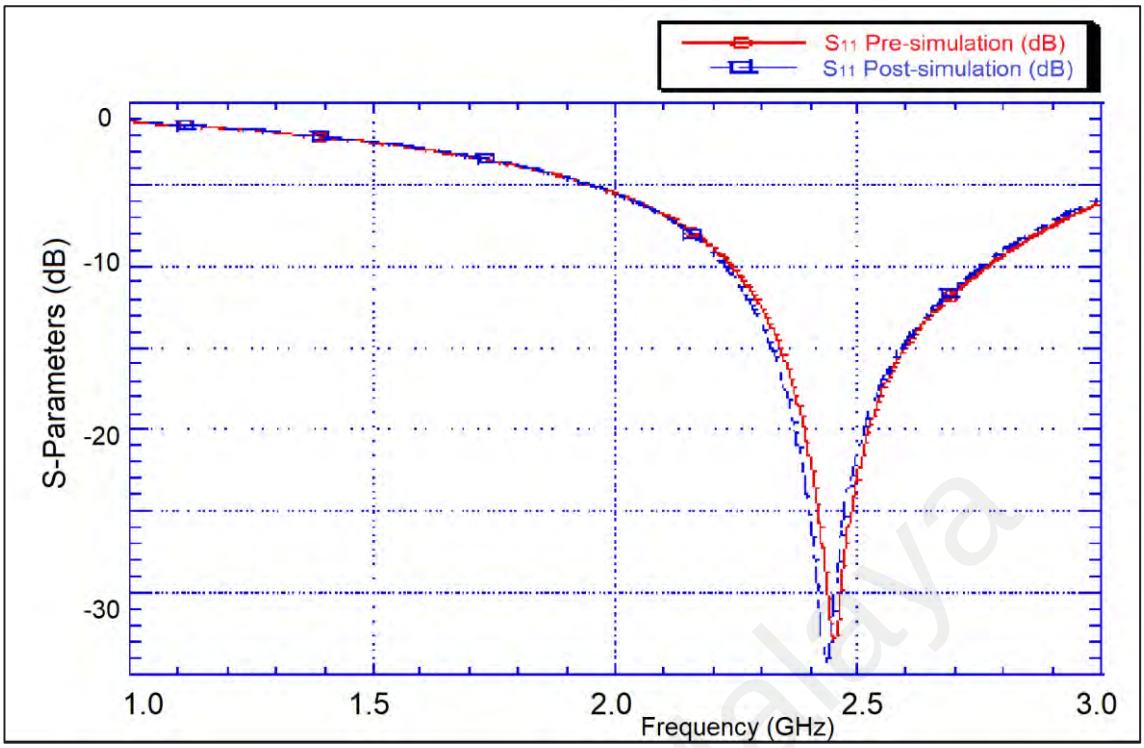

Figure 4.2: Graph of simulated S11 for pre and post layout performance of single-ended LNA at 2.4GHz

Figure 4.1 and Figure 4.2 show the pre and post layout S-parameter simulation of single ended PCSNIM LNA respectively. In pre-simulation S_{11} obtained -32.77 dB while -30.7 dB in post layout simulation. It can be seen that most of the S parameter curve for post layout simulation is shifted to higher frequency. This is due to the parasitic of the component lower down the frequency response of the circuit. The pre-layout simulations normally have better performances compared to their post-layout counterparts. If the condition of the components in the LNA are the same, the post-layout simulation results are typically worse than the results from the pre-layout simulations. This is because the post-layout simulation includes the parasitic effects of the substrate. As an example, the NF from the pre-layout simulation (Table 4.1) of the PCSNIM LNA is 4.1% (i.e. (2.67-2.56)x100%/2.67) better than the NF obtained from the distributed post-layout simulation when the circuit was maintained under same condition and the frequency was at 2.4 GHz.

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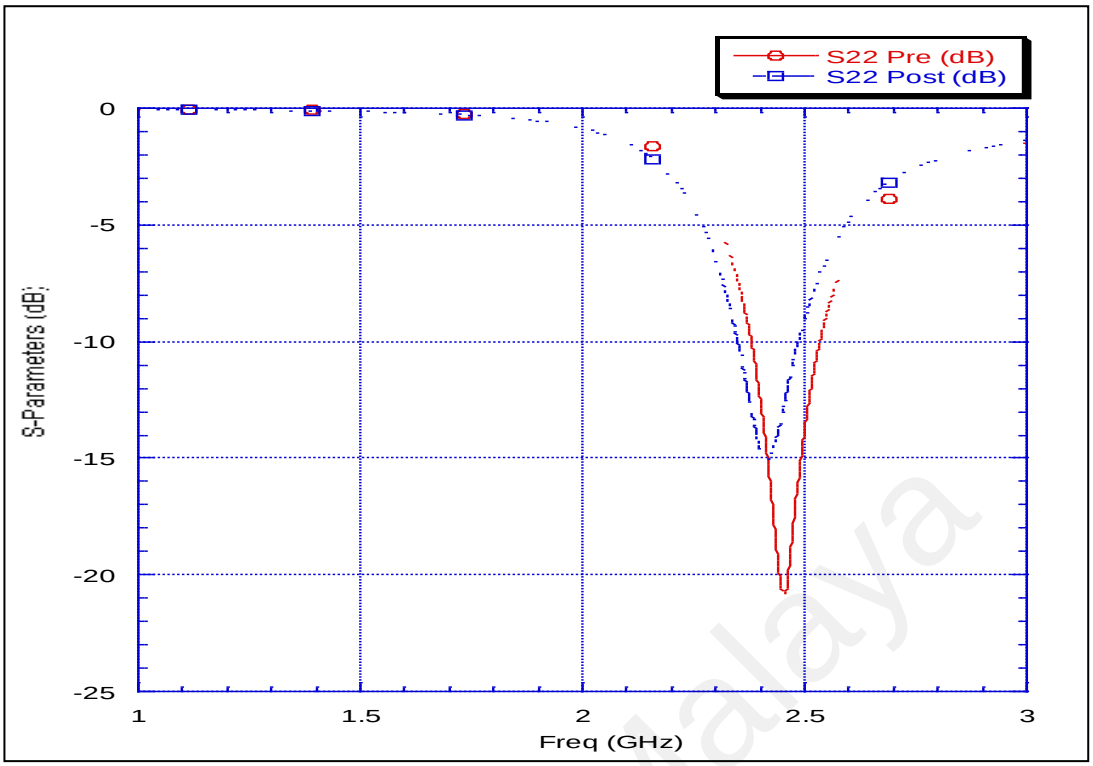

Figure 4.3: Graph of simulated S_{22} for pre and post layout performance of single-ended LNA at 2.4GHz

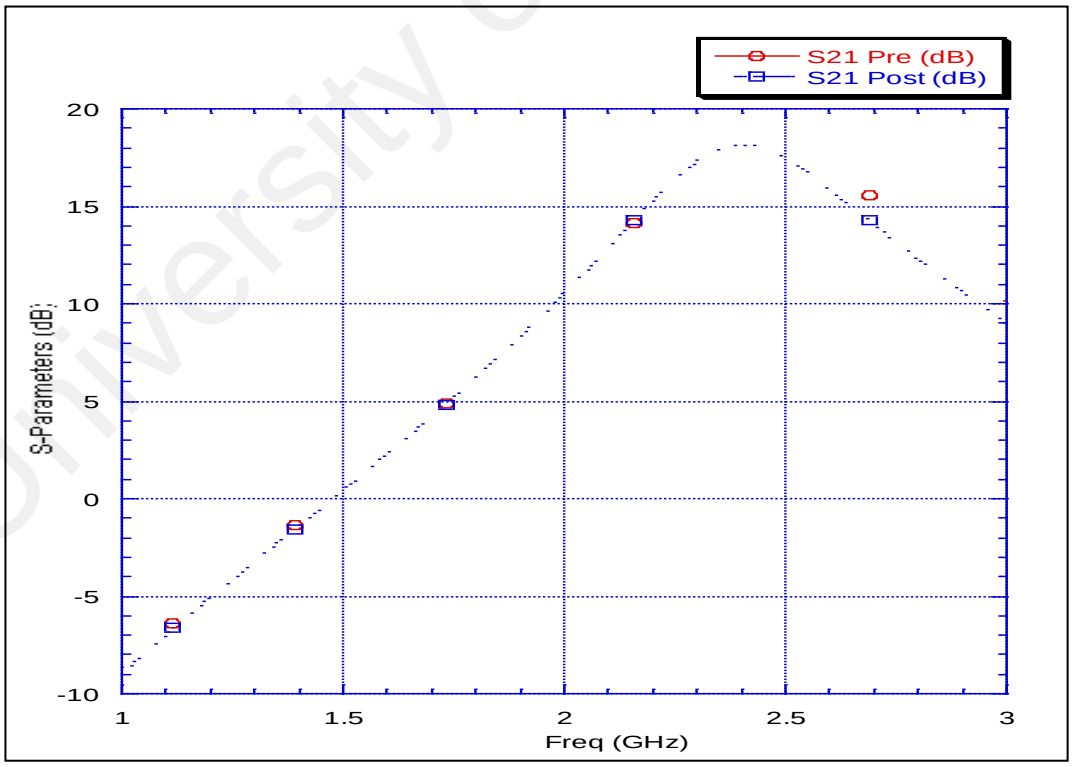

Figure 4.4: Graph of simulated S_{21} for pre and post layout performance of single-ended LNA at 2.4GHz

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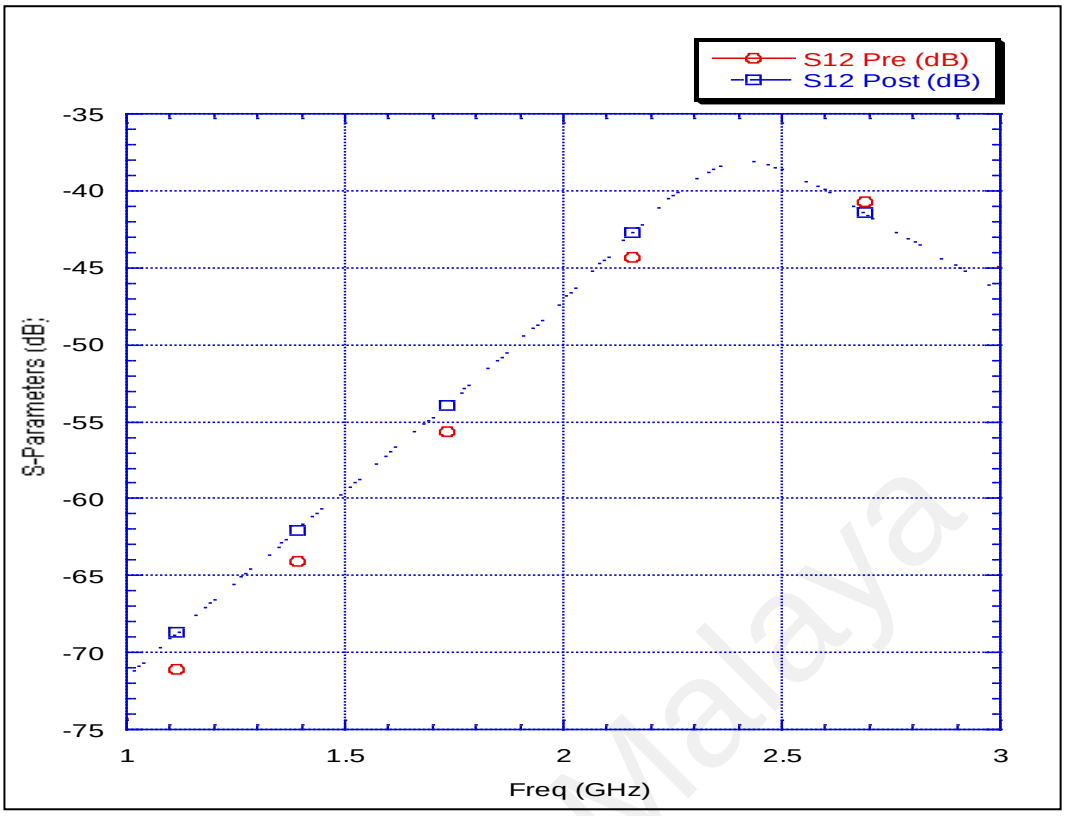

Figure 4.5: Graph of simulated S_{12} for pre and post layout performance of single-ended LNA at 2.4GHz

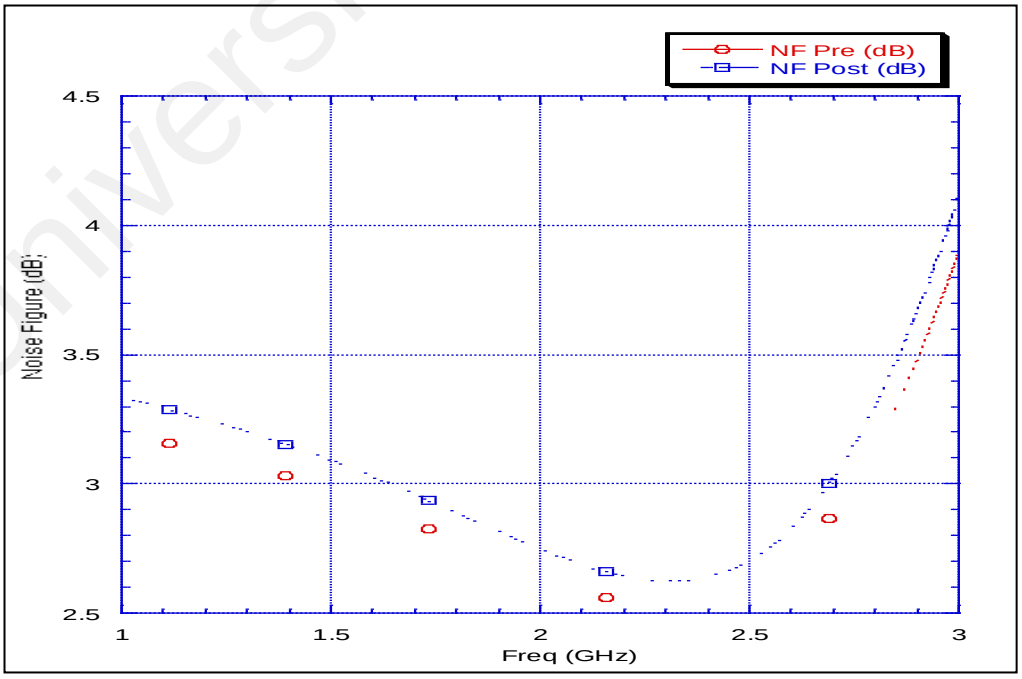

Figure 4.6: Graph of simulated NF for pre and post layout performance of single-ended LNA at 2.4GHz

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4.2.2 Stability Factor, K_f

In order to ensure a better stability, the reverse isolation is the important parameter in achieving it. The inductively degenerated PCSNIM LNA have the stability factor, Kf >1 at the frequency of 2.4 GHz as can be seen from Figure 4.7 the value is 3.3.

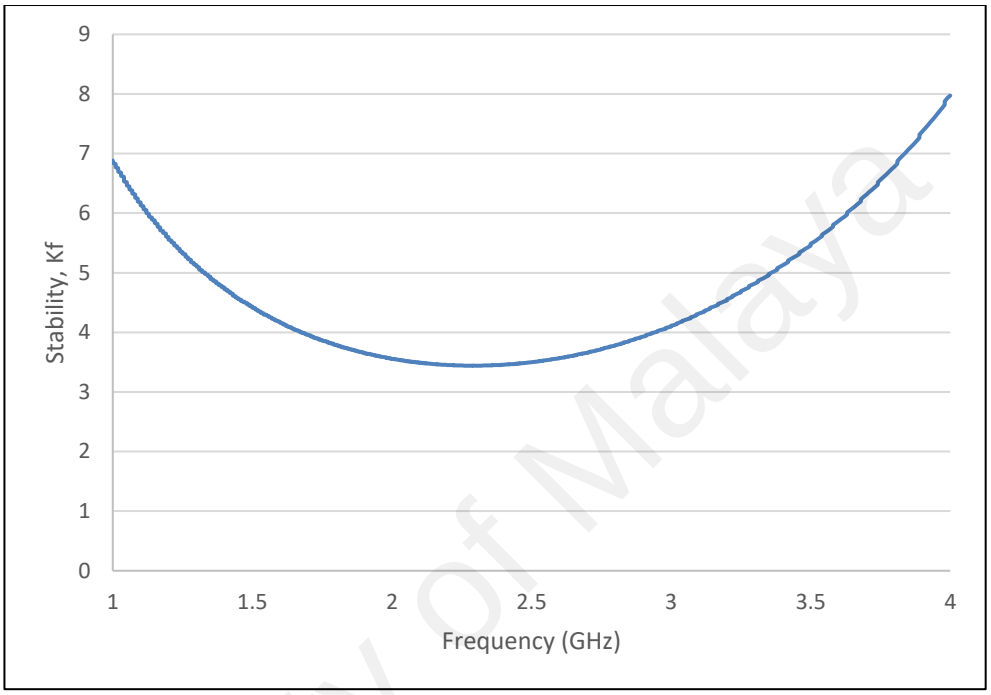

Figure 4.7: Stability factor of single-ended LNA

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4.2.3 IIP3

The most typical measures of linearity are the third-order intercept points, IIP3. Figure 4.8 shows the IIP3 performance for single ended PCSNIM LNA for pre and post layout simulation. For linearity, the IIP3 interception point for pre and post simulation are at –12.86 dBm and 11.97dBm, which can be considered high linear LNA (where the input extrapolation point is chosen at -25 dBm).

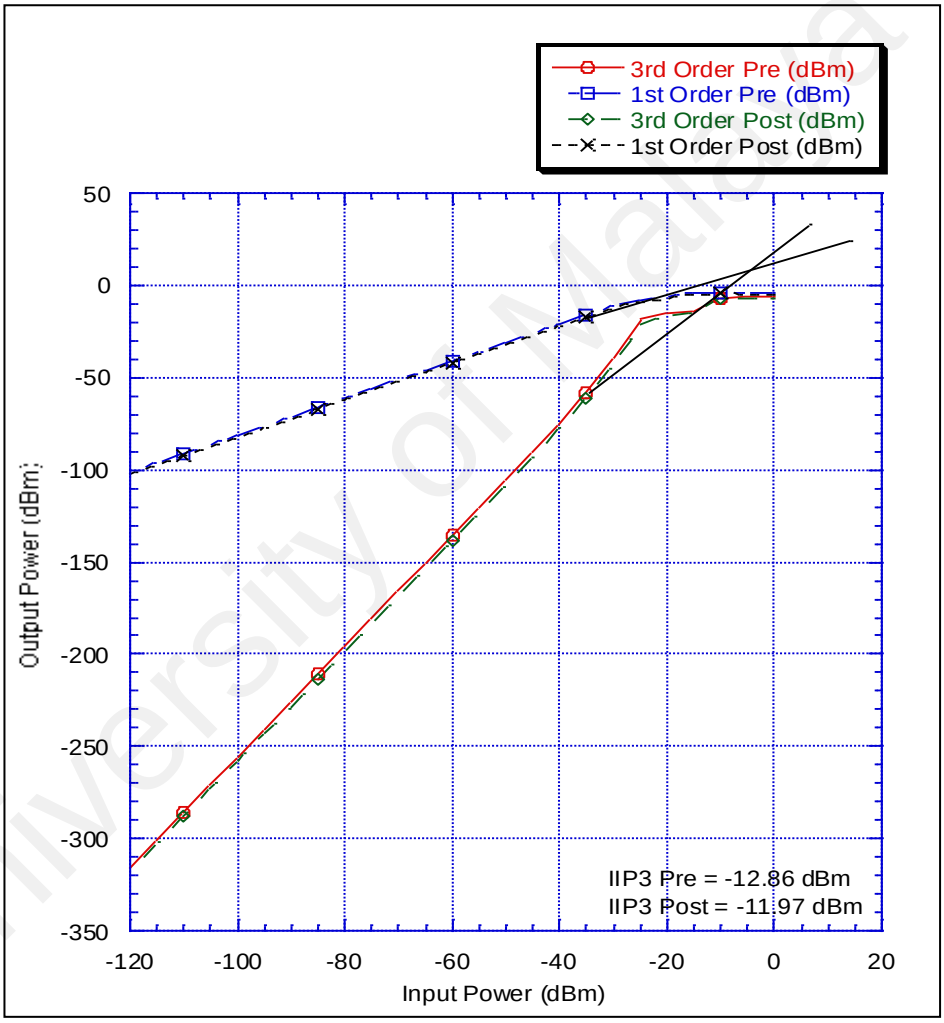

Figure 4.8: Graph of simulated IIP3 for pre and post layout performance of single-ended LNA at 2.4GHz

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4.3 Measurement Result Performance Single Ended LNA

4.3.1 S-Parameter

Figure 4.9 below is the s-parameter on-wafer measurement of single ended inductively degenerated cascode PCSNIM LNA. It can be seen from the curve that all the s-parameters is shifted to the right or at higher frequency a bit. Thus, the peak frequency is at 2.5 GHz. The measurement reading is taken at frequency 2.4 GHz. The input reverse isolation, S_{11} is 15.6 dB while out reverse coefficient S_{22} is -10.57 dB. While at peak frequency at 2.5GHz, S_{11} manage to achieve lowest value of -30 dB which is nearly the same as simulated in the post layout in Figure 4.9: S-Parameter curve of on-wafer measurement performance of single-ended LNA at 2.4GHz.

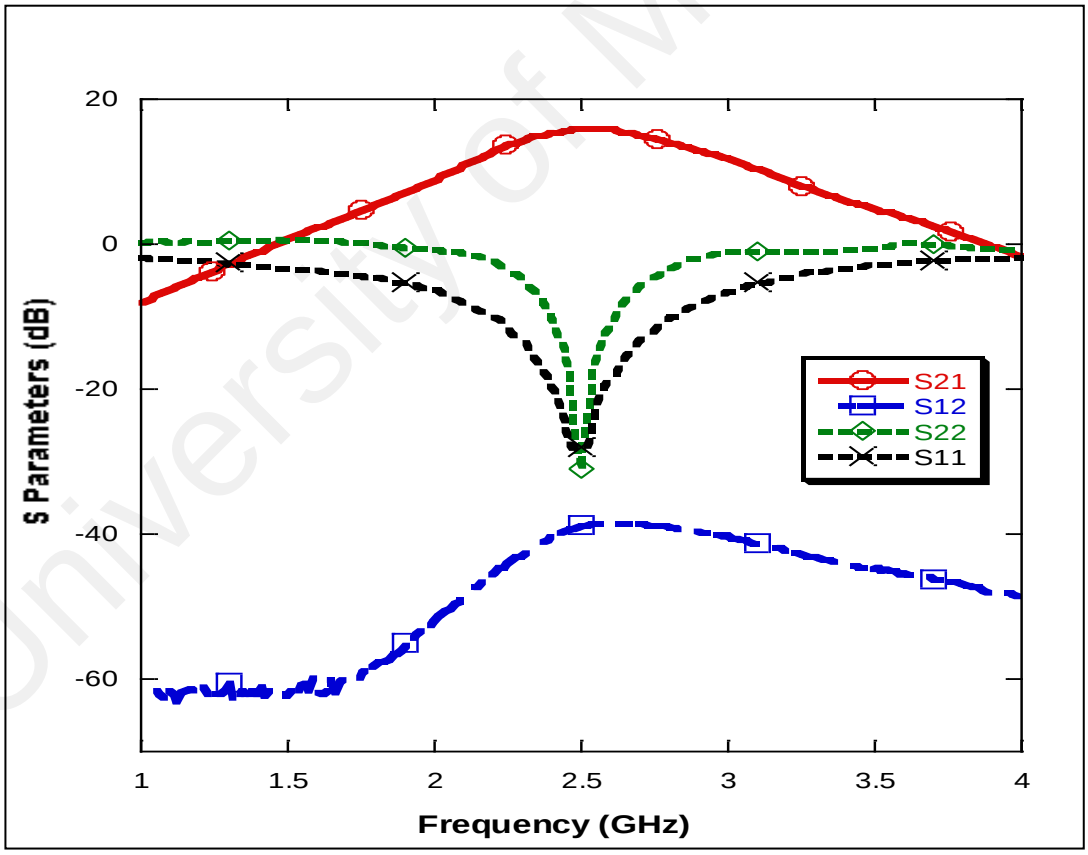

Figure 4.9: S-Parameter curve of on-wafer measurement performance of single-ended LNA at 2.4GHz

The same goes to S_{22} that achieved -32 dB. This is show that design single ended LNA have good input and output matching proof by the performance of S_{11} and S_{22}. As for the

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gain, S_{21} is 15.6 dB at 2.4 GHz while 18 dB at 2.5 GHz. This shows that, a small effect in frequency transition can lead to variation in the LNA gain. As in this case, a reduction of 2.4 dB gain due to the curve shifting to the frequency. This contribution due to the effects of the coupling between metals and the parasitic in the interconnects too. Even though careful design have been taken care of start from the beginning and also parasitic that are available at each node of the circuit are also included in the post-layout simulation, but still there is slight difference in the actual measurement reading. The performance of the fabricated LNA slighly reduce by comparing to post-layout simulation as in Figure 4.2. Having said that, the designed single ended LNA achieved to satisfy requirement in Table 3.1: LNA Design Specification for WLAN Standard (IEEE802.11). The total power consumed is 4.34 mW.

4.3.2 Noise figure

Noise figure on-wafer measurement result of the single-ended LNA was tabulated in the graph shown in Figure 4.10. The single-ended LNA manage to achieve NF of 2.1 dB (using de-embedded) while 3.9 dB (without de-embedded) at 2.4 GHz. By using de-embedding measurement method for NF can obtain lower NF after eliminating unwanted noise from cable, surrounding and etc. This is significant improvement of 1.8 dB in NF by considering proper gain definition as discussed in section 3.11 earlier. Thus, this is proven the de-embedding method implement in this work manage to measure the actual noise contribution of the LNA itself.

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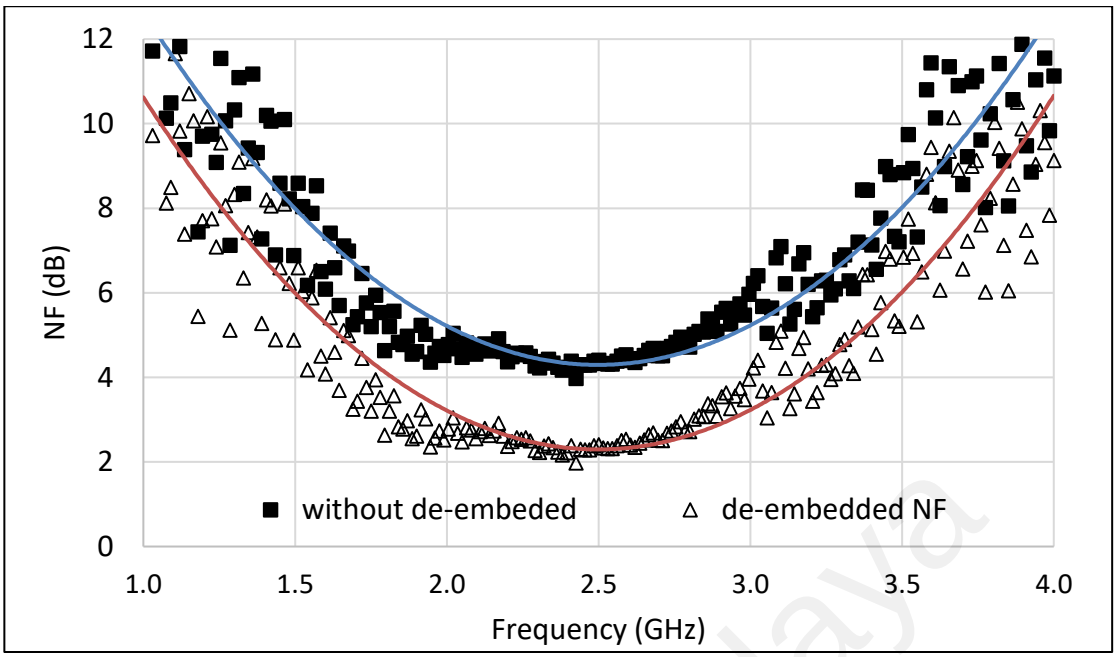

Figure 4.10: Noise figure plot obtained from on-wafer measurement using de-embedding technique for single ended LNA.

Table 4.1 shows post-layout and measurement data obtained for single ended LNA. The performance of the fabricated LNA slighly reduce by comparing to post-layout simulation. This can be due to the variation in the fabrication process that cause the measured performance shift around 100MHz to the right. However, the LNA still manage to attain the WLAN standard requirement.

Table 4.1: Measurement data for single ended LNA.

Data	I_{tot} (mA)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	S_{12} (dB)	NF (dB)	IIP_3
Pre-layout	3.82	18.91	-32.77	-20.8	-38.2	2.56	-12.86
Post- layout	3.76	17.96	-30.70	-12.92	-38.21	2.67	-11.97
Measurement	3.62	15.60	-20	-10.57	-37.39	2.1	-11

Having the performance mentioned, the PCSNIM cascode topology single-ended LNA is suitable to achieve low noise figure. Thus, a differential PCSNIM LNA was designed based on the optimized single-ended topology. The following section is the simulation result of the PCSNIM differential LNA.

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4.4 Pre and Post Simulation Performance Differential Cascode PCSNIM LNA

4.4.1 S-Parameter and Noise Figure

Figure 4.11 and Figure 4.12 shows the pre and post layout simulation performance of differential inductively degenerated cascode PCSNIM. It is designed for operating frequency at 2.4 GHz. The S parameter curve for post layout simulation is shifted to higher frequency, thus making the peak frequency not at 2.4GHz. Even though the post-layout simulation includes the parasitic effects of the substrate. These parasitic considerations closely resemble the actual conditions that may occur physically in the LNA. However, the performance of the differential LNA still stratify the design target and with S_{11} obtained -19dB while the S_{21} is19.6 dB at 2.4GHz. While NF manage to achieve 1.7 dB with NF_{min} is 1.5 dB. This gain and NF value is considered excellent performance for LNA designed for WLAN application with still room of improvement. With proper design beginning from the start, this good result is attainable. When designing an integrated circuit, one must aware and always consider all implications of the physical layout that might be affecting the circuit's performance.

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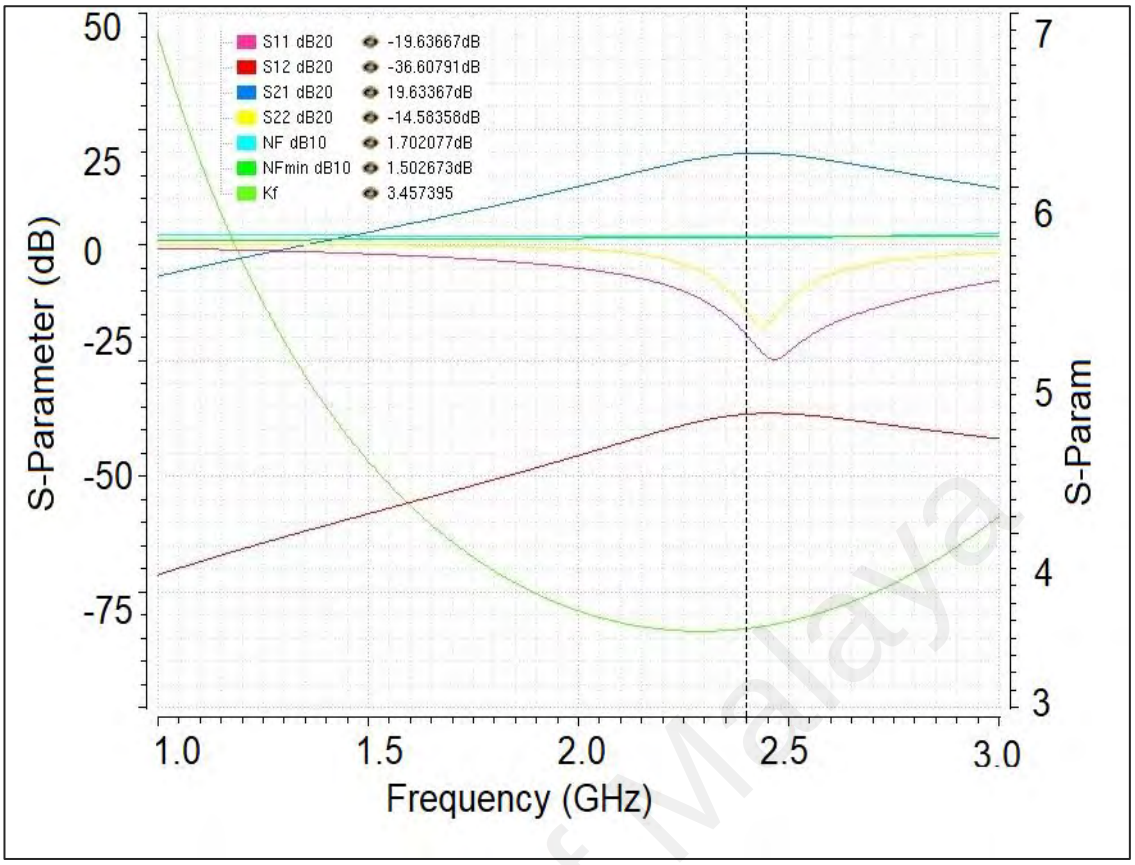

Figure 4.11: Graph of simulated s-parameter and NF for pre-layout performance of differential cascode PCSNIM LNA at 2.4GHz

The pre-layout simulations normally have better performances compared to their post-layout counterparts. If the condition of the components in the LNA are the same, the post-layout simulation results are typically worse than the results from the pre-layout simulations.

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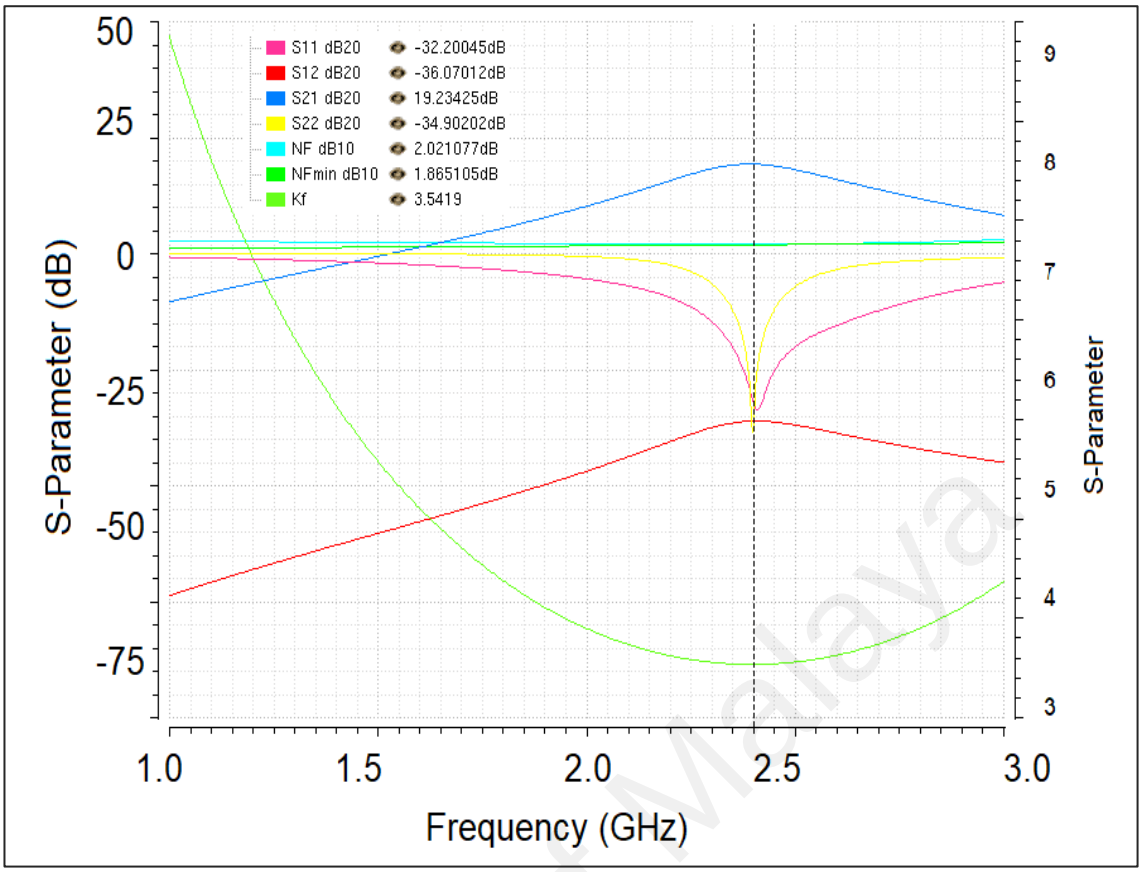

Figure 4.12: Graph of simulated s-parameter for post-layout performance of differential cascode PCSNIM LNA at 2.4GHz

Table 4.2 depicts the summary of the simulation data for differential PCSNIM LNA performed as in Figure 4.11 and Figure 4.12 taken at 2.4 GHz.

Table 4.2: Differential PCSNIM LNA: Pre and Post layout simulation data

Data	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	S_{12} (dB)	NF (dB)	IIP3
Pre-layout	19.6	-19.6	-14.5	-36.6	1.7	-19.74
Post- layout	19.2	-32.2	-34.9	-36	2	-19.8

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4.4.2 IIP3

The pre and post layout simulation result are presented in this section for P1 dB and IIP3 in Figure 4.13, Figure 4.14 , Figure 4.15 and Figure 4.16 respectively. IIP3 is -8.22 dBm (pre) and -7.75 dBm (post). An improvement in the linearity performance by 0.47 dBm which is around 6% of improvement compared to pre-layout simulation.

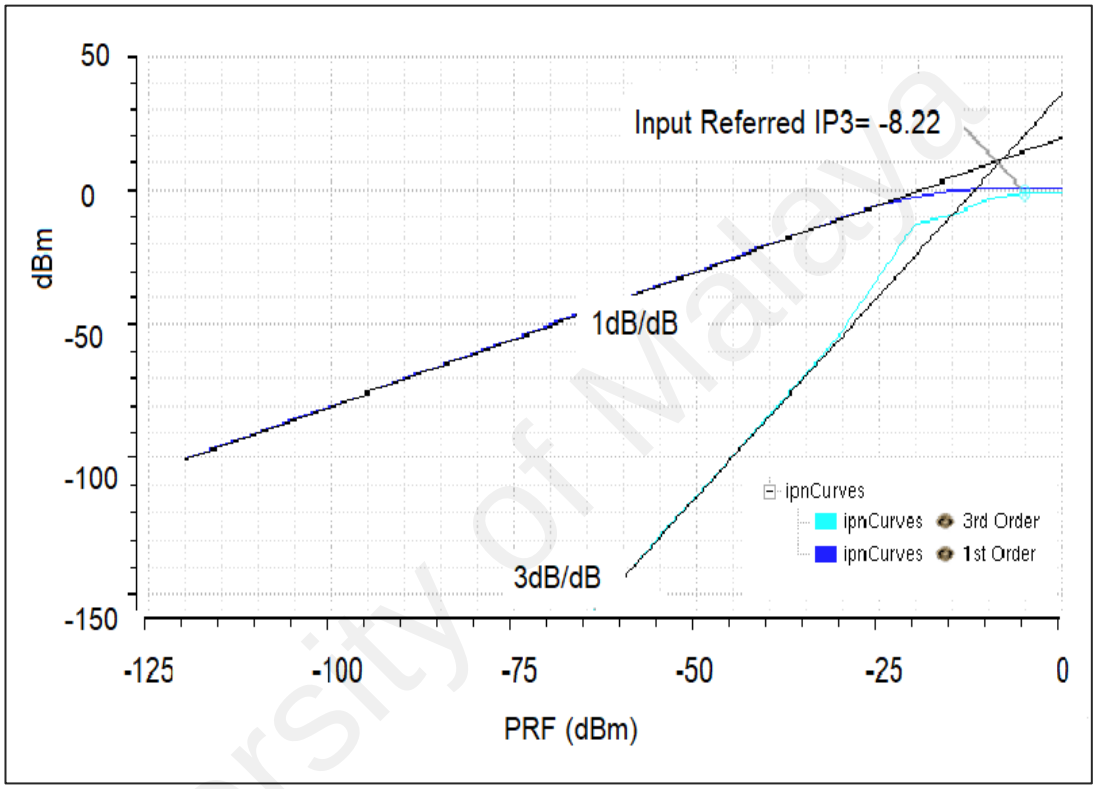

Figure 4.13: Graph of simulated IIP3 for pre-layout performance of differential cascode PCSNIM LNA at 2.4GHz

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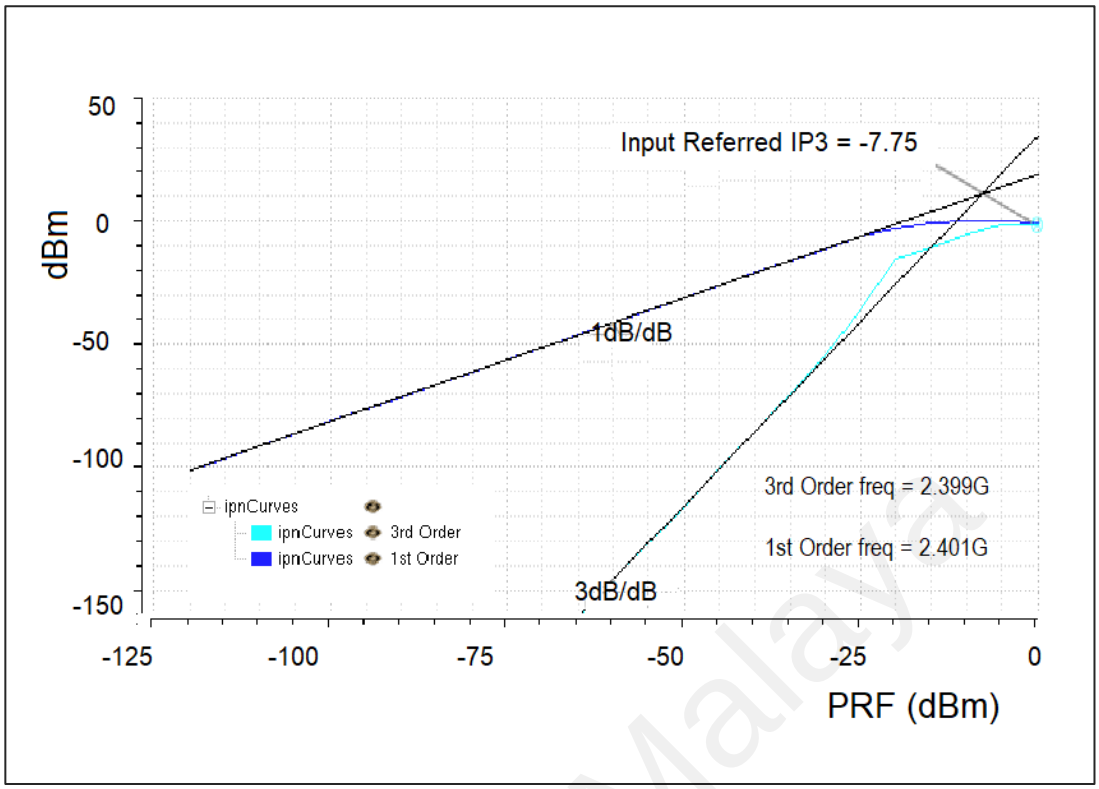

Figure 4.14: Graph of simulated IIP3 for post-layout performance of differential cascode PCSNIM LNA at 2.4GHz

The P1dB points (IP1dB and OP1dB) was determined from simulation and shown here in respectively. As can be observed from the respected graph, the difference between OP1dB and IP1dB is 19.79 dBm (pre) while 19.6 dB(post) respectively. These values correspond to the gain of the LNA which is $S21_{pre}$ is 19.6 dB and $S21_{post}$ 19.2. This is due to the intercept point and the IP1dB and OP1dB are corresponding to a point on the linear slope as shown in the graph. The simulated design of the differential LNA manage to achieve the design target. The pre and post layout simulation reading also just got slightly small difference between them.

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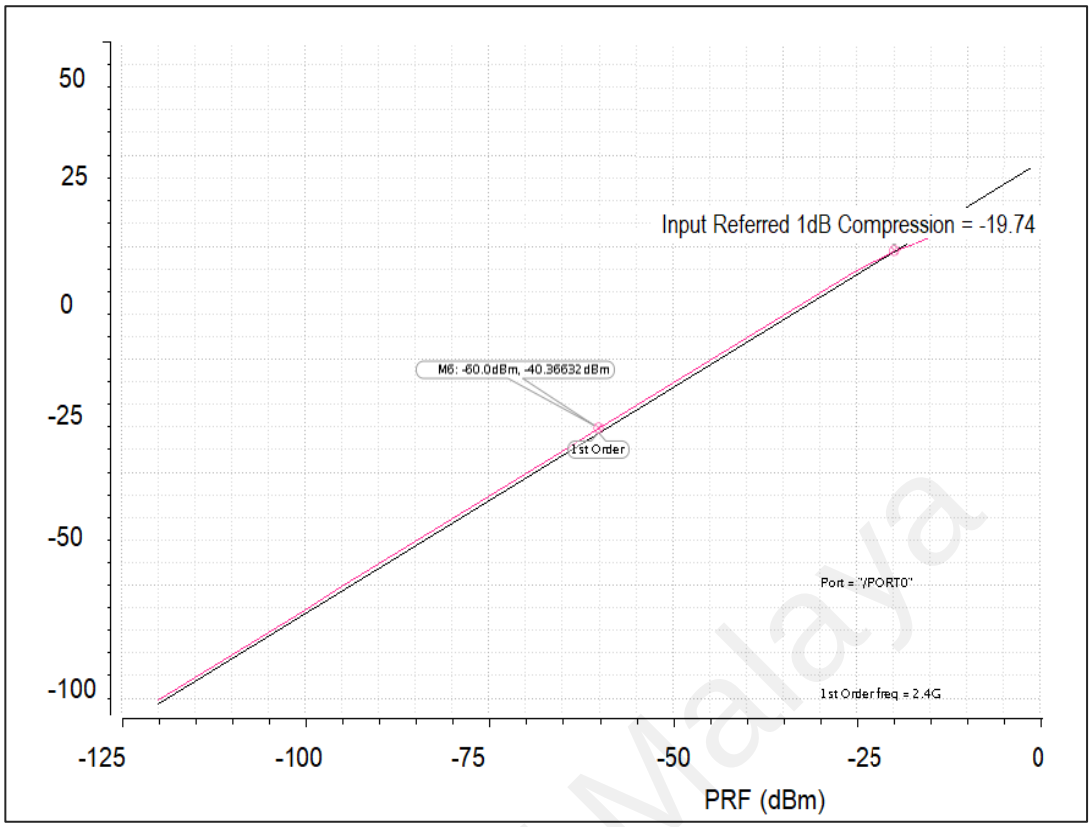

Figure 4.15: Graph of simulated P1dB pre-layout performance of differential cascode PCSNIM LNA at 2.4GHz

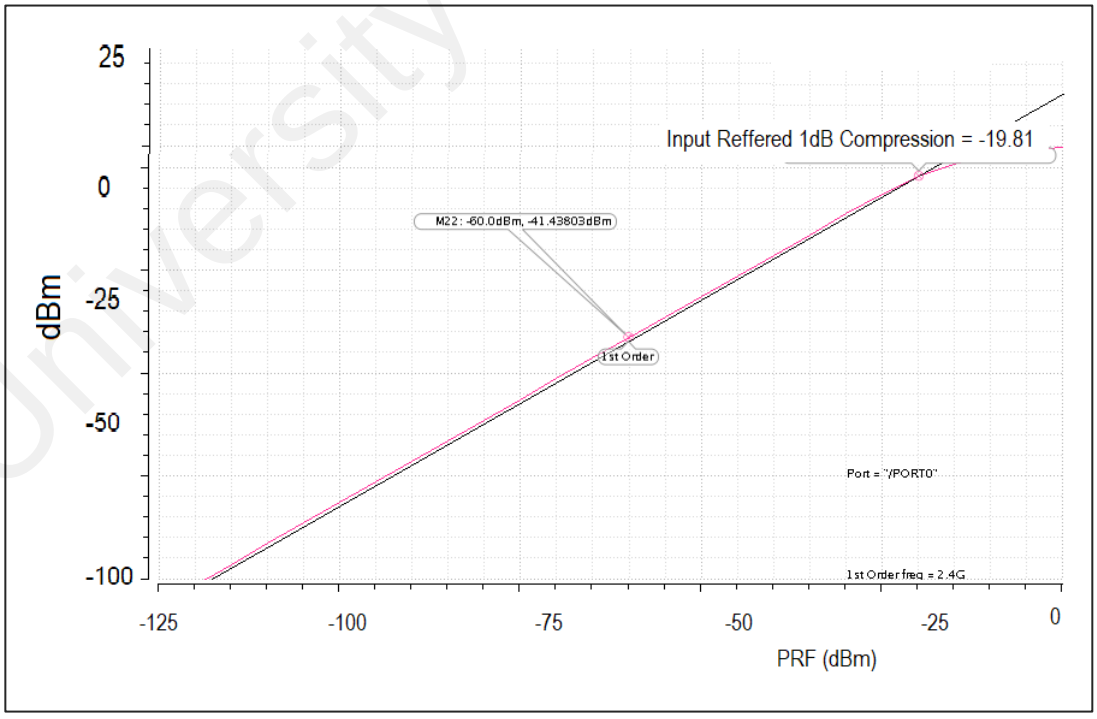

Figure 4.16: Graph of simulated P1dB for post-layout performance of differential cascode PCSNIM LNA at 2.4GHz

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4.5 Measurement Performance Differential LNA data

4.5.1 S-Parameter and Noise Figure

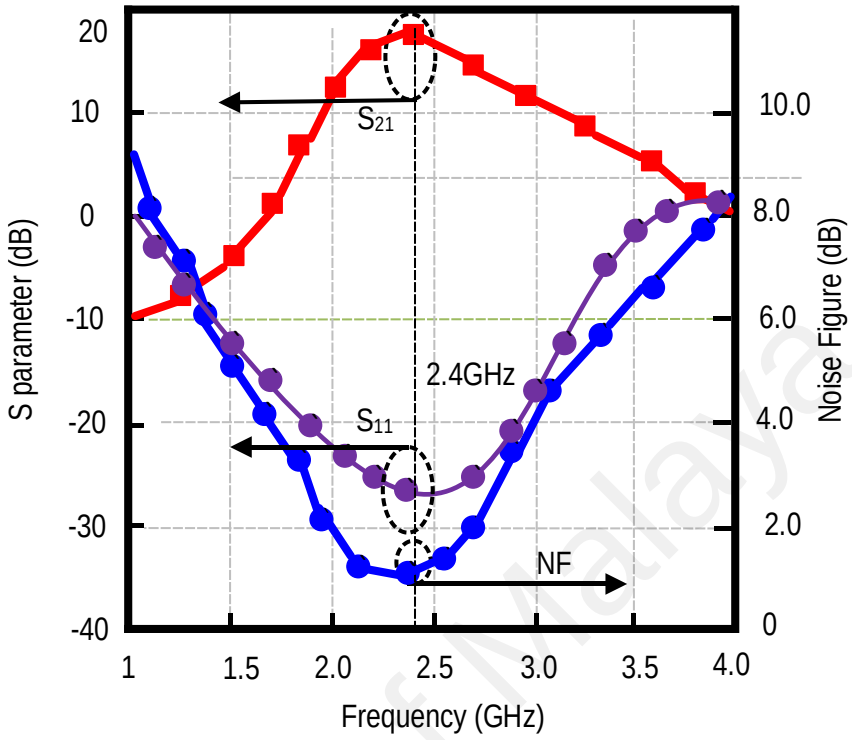

Figure 4.17: S-Parameters and Noise Figure on-wafer measurement performance of differential LNA Cascode PCSNIM

Figure 4.17 illustrates the on-wafer measurement result of the S-Parameter and NF. At frequency 2.4 GHz, NF manage to achieve 1.8 dB while in post simulation as in Figure 4.12, NF is 2.02 dB. There is a 0.22 dB of reduction in NF measurement compared to simulation. The degraded measured NF is by a small amount contributed by the difference in the S_{21} gain in which is 19.2dB in post layout simulation while reduced to 17.12 dB in the measurement. As for the input reflection coefficient, S_{11} is -32.2 dB in post-layout simulation but reduced to -27 dB for the measurement which is 5.2 dB increment. However, this reading considers good as it meets design target specify by WLAN standard. There a few factors that might contribute to the difference, one of them is due to the parasitic occurring in the design.

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4.5.2 S-parameter measurement validation

A common problem handled in the areas of signal integrity is the incapability to effectively depict networks with differential signalling schemes. The main challenge is lacking instrument capable of simultaneously stimulating dual input ports with signals synchronized with each other. Thus, accurately defining the power waves incoming and leaving the network, such as a four-port Vector Network Analyzer (VNA) with dual synthesized frequency sweepers. This work proposes a low-cost method of characterizing differential networks with existing two-port VNAs by using a technique of measuring the Scattering Parameters (s-parameters) of two ports at a time while the other two are appropriately terminated, in this work with standard 50Ω terminations.

As been discussed and explained in section 3.10, differential LNA designed in work make used of ideal balun in the pre and post simulation. Figure 4.18 illustrates the comparison of S-parameters of the designed differential LNA that measured using four-port and two-port VNA. The results demonstrated good agreement for both measurements using two-port and four-port VNA. The curve fitting between both measurement for all S-parameter results. Nonetheless, there is a marginal difference using two-port VNA due to the limitation but mostly the peak performance occurs at the center operating frequency which is at 2.4 GHz. The gain of the differential LNA which are S_{31} and S_{41} manage to achieve 17.28 dB and 17.29 dB respectively. S_{11} and S_{22} is the reverse isolation of the differential LNA. The reverse isolation parameter S_{11} taken using two-port is better compared to the other one. S_{11} reading at center frequency of 2.4GHz is -27.5 dB. This shows that the input impedance matching for this differential LNA is good. There is slightly frequency shift at S_{22} parameters which cause the both reading not properly overlapped. This might be due to the GSGSG probe not properly touch the wafer during measurement and some parasitic that present during the measurement. However, this does

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not affect the overall reading and performance of the LNA since the requirement specify by the WLAN is still fulfill.

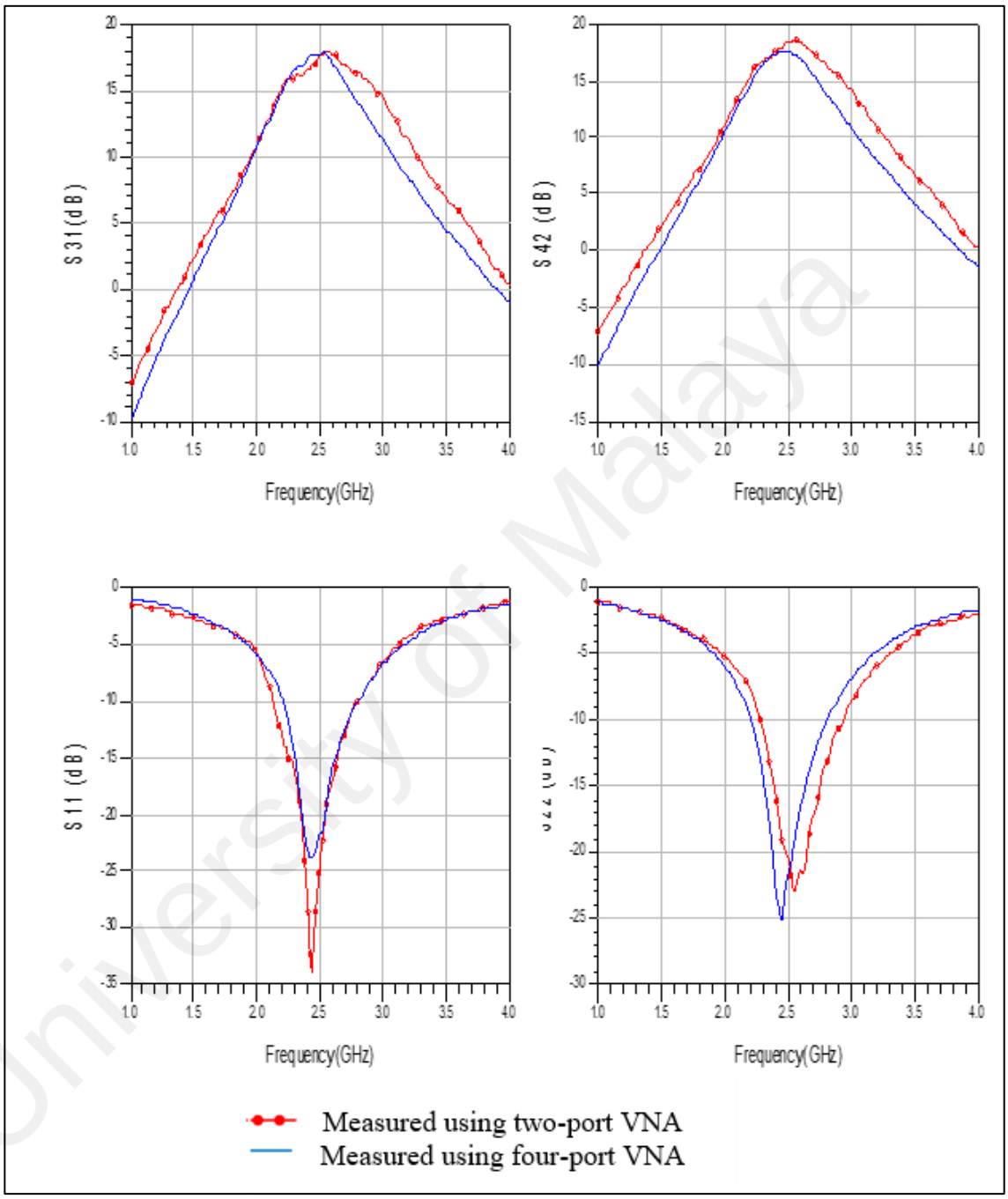

Figure 4.18: Comparison of the measured S-parameters for differential LNA

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Table 4.3 shows comparison of measured S-parameters performance of differential LNA taken at center frequency of 2.4GHz. It is shown that most of the s-parameter value taken using two-port VNA is nearly the same with 0.93- 22.5% difference as the measurement taken using four-port VNA. This result successfully validated and proven. This mark the goal of this work achieved.

Table 4.3: S-parameters Measurement using two-port and four-port VNA

S-Parameters	VNA Type		% Differences
	Two-port	Four-port	
S_{31} (dB)	17.12	17.28	0.93
S_{42} (dB)	17.40	17.29	0.63
S_{11} (dB)	-30.0	-24.50	22.5
S_{22} (dB)	-23.00	-22.00	4.5

4.5.3 Noise Figure Performance with de-embedding technique

Figure 4.19 illustrates the NF measurement performance of differential cascode PCSNIM LNA. The NF measurement is taken by using de-embedding technique and also by using normal method (without de-embedding). At frequency of 2.4 GHz, the NF is 1.2 dB for without de-embedding method, while 0.57 dB by using de-embedding method. This is a huge reduction of 0.63 dB.

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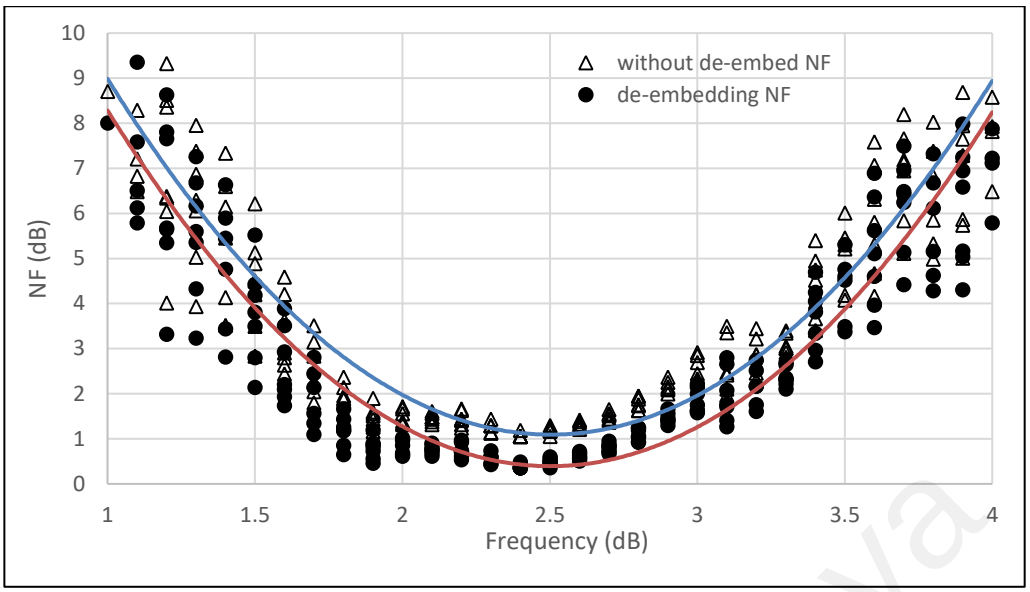

Figure 4.19: Comparison of Noise figure measurement using with and without de-embedding technique of differential cascode PCSNIM LNA

4.5.4 Comparison between theoretical, simulation and measurement of Noise Figure Performance with de-embedding technique

Figure 4.20 illustrates the NF performance obtained using theoretical analysis, simulation and measurement. The theoretical analysis obtained by using equation (2.20). It can be seen that the NF performance is good and satisfy the design requirement for the bandwidth base from the starting analytical analysis .The NF reading taken using de-embedding measurement method is greatly reduce the NF value by eliminating the unwanted noise from the system.

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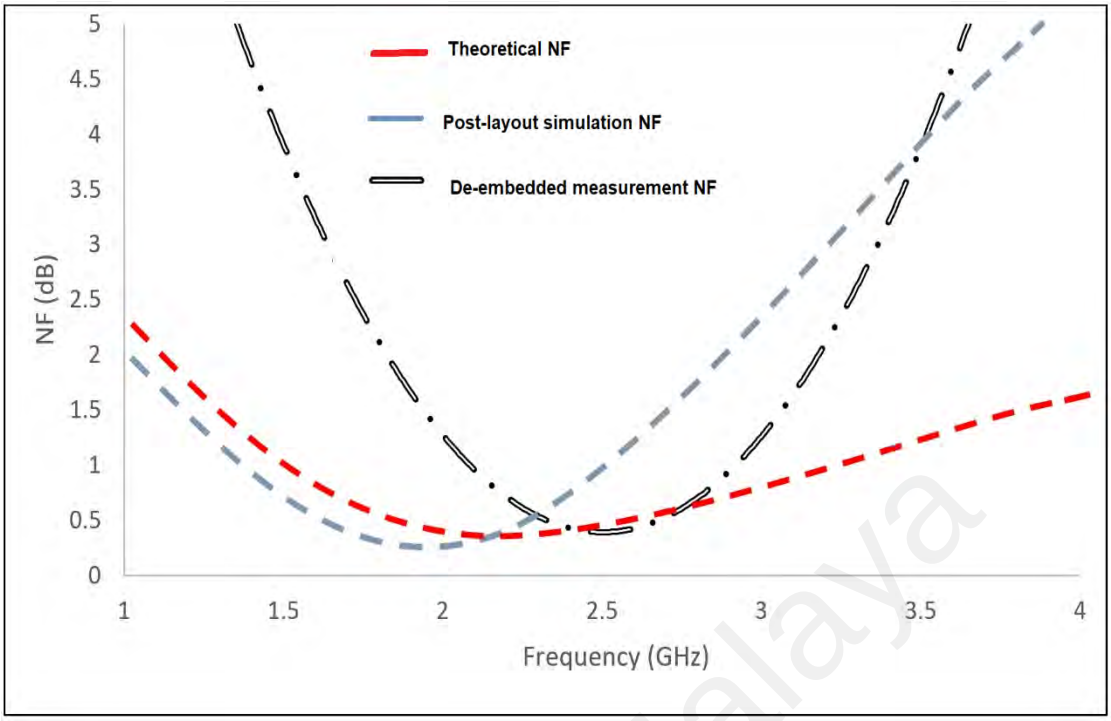

Figure 4.20: Noise Figure comparison between theoretical, simulation and de-embedded measurement.

4.5.5 IIP3

Another important aspect of LNA performance is the measure of measure of linearity given by 3rd order intercept point. The noise figure optimization technique by scaling the input transistor size tend to degrade the linearity of low noise amplifier. However still 3rd-order intercept point IIP3 is still better than -15dB at the required frequency range.The results are shown below. The linearity of the LNA illustrates in Figure 4.21 was measured in the conventional 2 port Network analyzer ports 2 and 4 terminated with 50 Ω. The measured IIP3 of the differential PCSNIM manage to get -10.5 dBm which is better than obtained in post layout simulation (-19.8).

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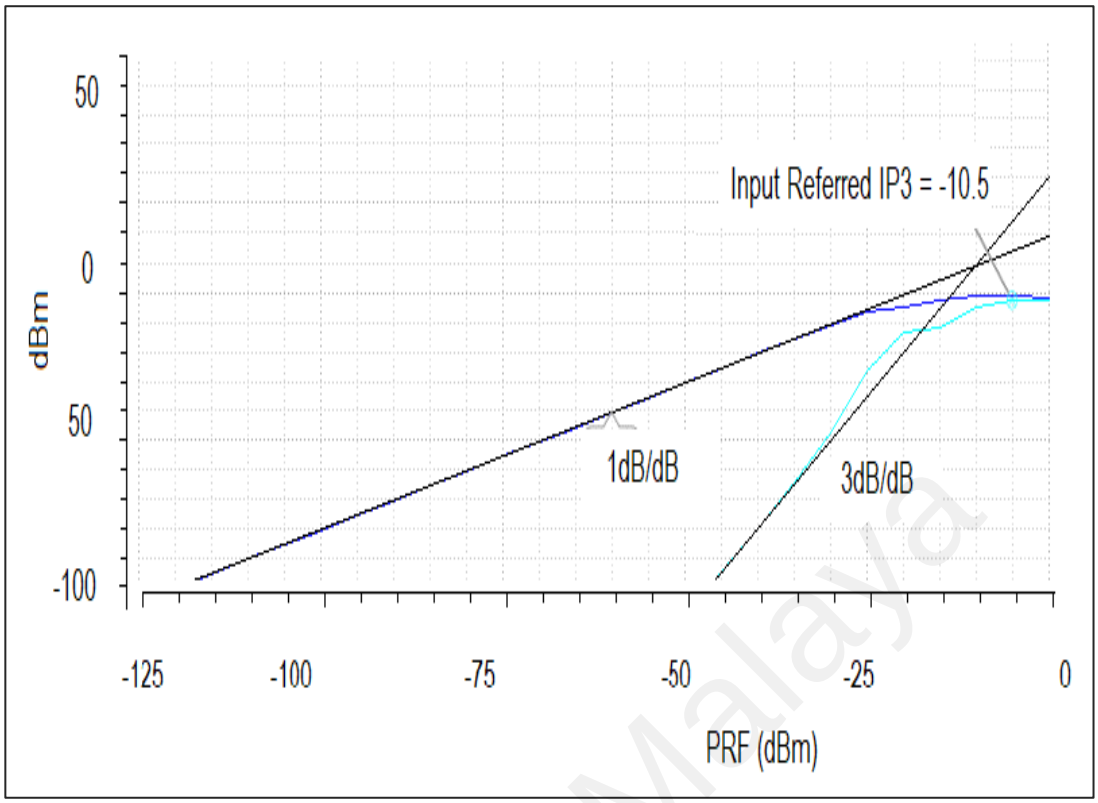

Figure 4.21: Third Order Intercept Point (IIP3) measurement of Differential PCSNIM LNA

Table 4.4 summarized the data for simulation and measurement for differential PCSNIM LNA.

Table 4.4: Differential PCSNIM LNA: Summary of simulation and on-wafer measurement data.

Data	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	S_{12} (dB)	NF (dB)	IIP3
Pre-layout	19.6	-19.6	-14.5	-36.6	1.7	-19.74
Post- layout	19.2	-32.2	-34.9	-36	2	-19.8
Measurement	17.12	-27	-19	-20	1.2^{+}, 0.57^{*}	-10.5

+: without de-embed; * : with de-embed technique

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4.6 Pre and Post Simulation Performance Differential LNA with differential inductor

In this section, the previous design of differential PCSNIM is being modify by using differential inductor instead of normal passive inductor. The performance of the LNA is being evaluate under for S-parameter, NF and linearity which is the IIP3 of the LNA. Apart from the it's area efficient in using differential inductor, other factor will be compared to evaluate the performance.

4.6.1 S-Parameter and Noise Figure

Figure 4.22 illustrates the pre-simulation of S- parameter and NF performance of differential LNA using differential inductor. As can be seen from the graph, S_{11} and S_{22}, the reverse coefficient for input and output port is – 23.9 dB and – 9.31 dB respectively at frequency of 2.4 GHz. Besides, in the frequency range of 2.1 GHz to 2.7 GHz, where the bandwidth is 0.6 GHz, the S_{11} and S_{22} are still below – 10 dB, as shown in Figure 4.22. Hence, the differential PCSNIM with differential inductor can be concluded as having good reflection coefficient.

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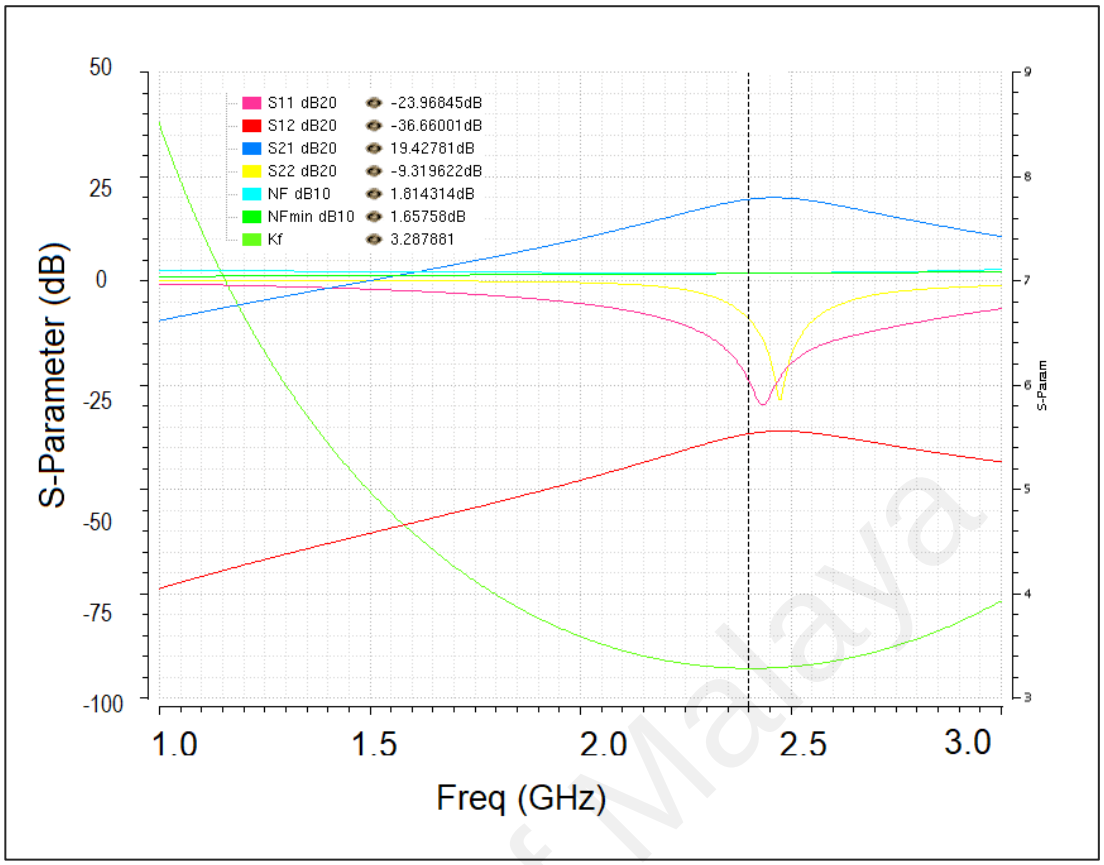

Figure 4.22: Pre-Simulation of S Parameters and Noise Figure performance

Having mention previously, the post-layout simulation results are typically worse than the results from the pre-layout simulations. This is because the post-layout simulation includes the parasitic effects of the substrate. As for the post simulation of the S parameter and NF performance of the differential PCSNIM with differential inductor, shown in Figure 4.23, the post simulation results are better than pre-simulation at the frequency 2.4GHz.

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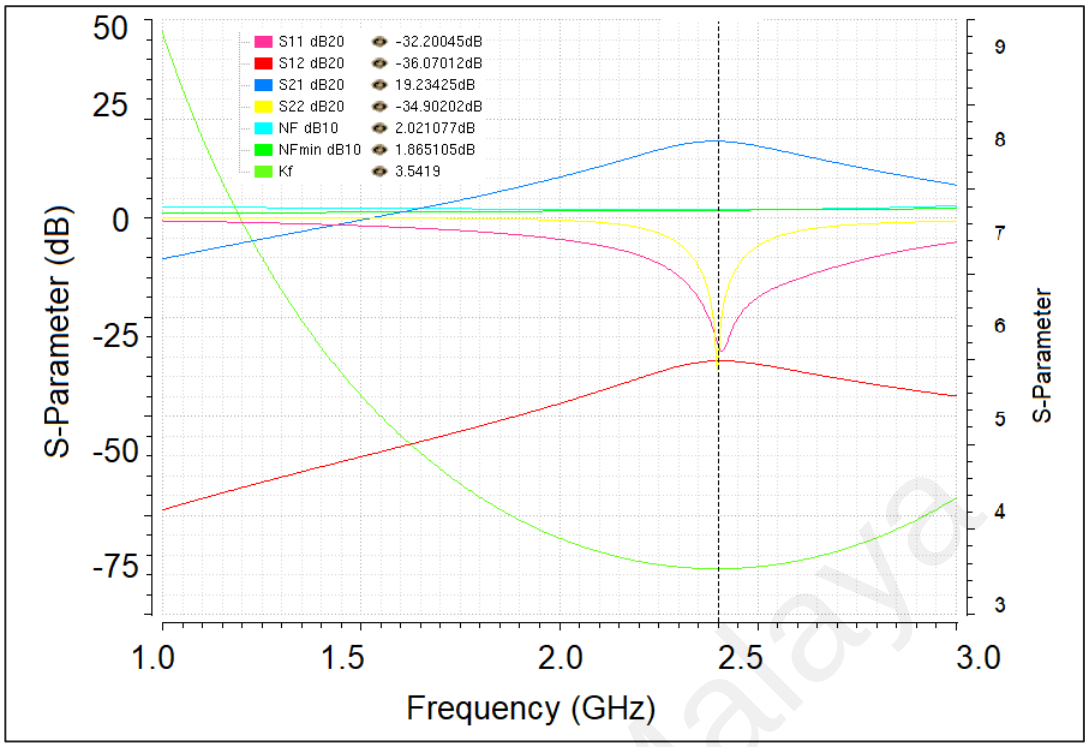

Figure 4.23: Post Simulation of S Parameters and Noise Figure performance

4.6.2 Third order intercept point, IIP3

Figure 4.24 and Figure 4.25 illustrates the Pre and Post- Simulation of Third Order Intercept Point (IIP3) performance of differential LNA using differential inductor. As can be seen from the graph, the IIP3 are -9.31dB and – 10.2 dB respectively at frequency of 2.4 GHz.

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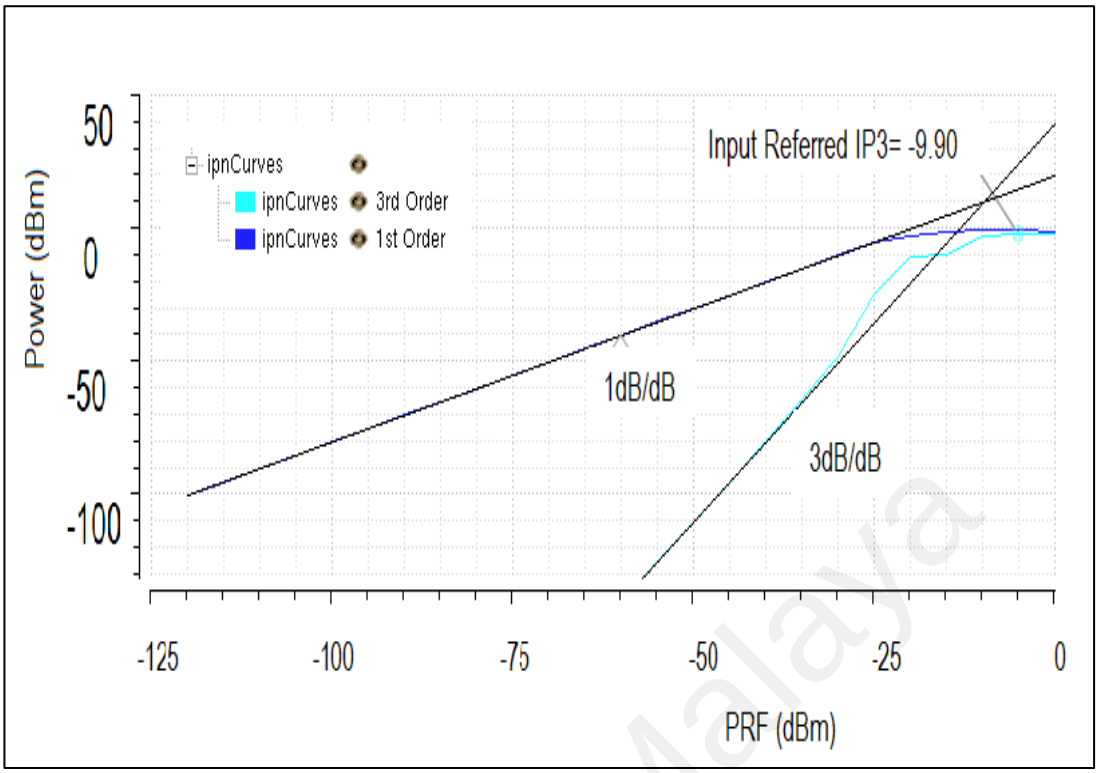

Figure 4.24: Pre-Simulation of Third Order Intercept Point (IIP3)

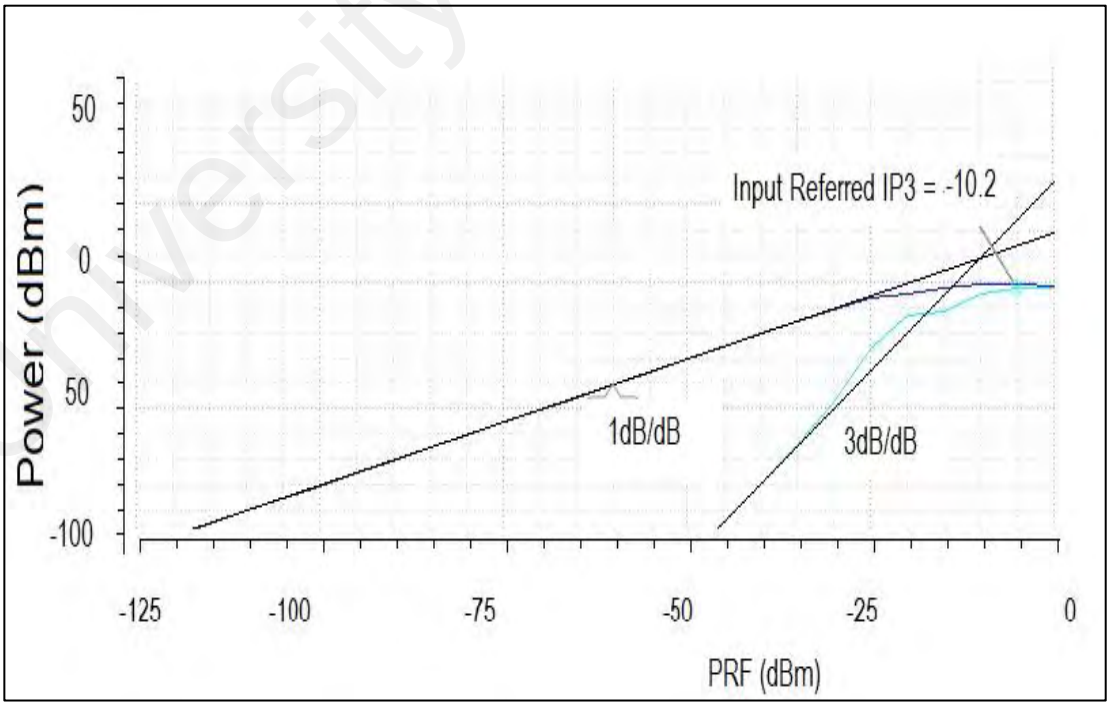

Figure 4.25: Post Simulation of Third Order Intercept Point (IIP3)

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4.7 Measurement Result Performance Differential LNA with differential inductor

4.7.1 S-Parameter

The measured S_{11} from Figure 4.26 shows that it is tuned to 2.8 GHz and has a value of -18 dB at 2.4 GHz, which shows that the input is not properly matched to 50 Ω at the operating frequency. On the other hand, the measured S_{21} shown indicates that this parameter is tuned to peak at 2.5 GHz and get 16 dB. Comparing with the simulation performance, this circuit manage to get good 19 dB gain with S_{11} is -32 dB (post). This indicates that the output of the LNA must be unmatched to 50 Ω at 2.4 GHz as the S_{21} is influenced by both the input and output matching. The matching performance at the output of the LNA can be seen from the plot of S_{22} in the same Figure 4.29. In this figure, it is seen that the measured S_{22} is only -9 dB at 2.5 GHz. As for the tuning of the input and output signals to 2.4 GHz, only S_{22} correspond well to the 2.4 GHz operating frequency.

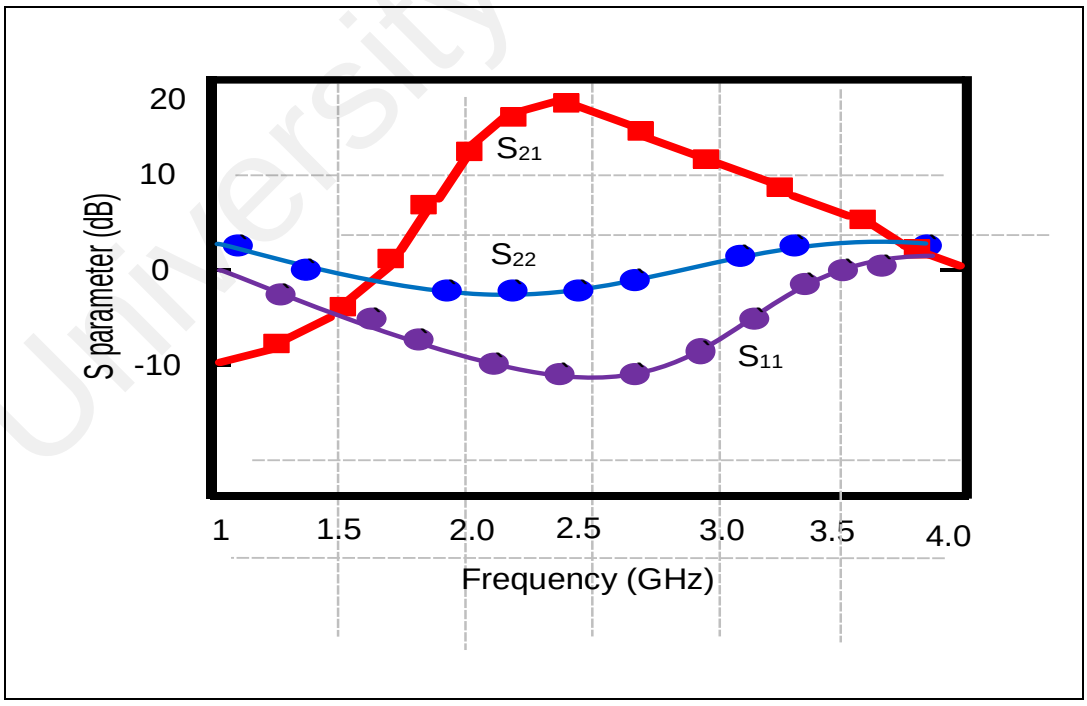

Figure 4.26: S-parameter measurement of differential LNA with differential inductor

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4.7.2 Noise Figure Performance

NF performance is very crucial in differential LNA. Figure 4.27 shows the measurement comparison of NF using de-embedding and without de-embedding technique for differential PCSIM with differential inductor which is 4.2 dB and 2.4 dB respectively. A huge reduction and improvement difference of 1.8 dB in NF.

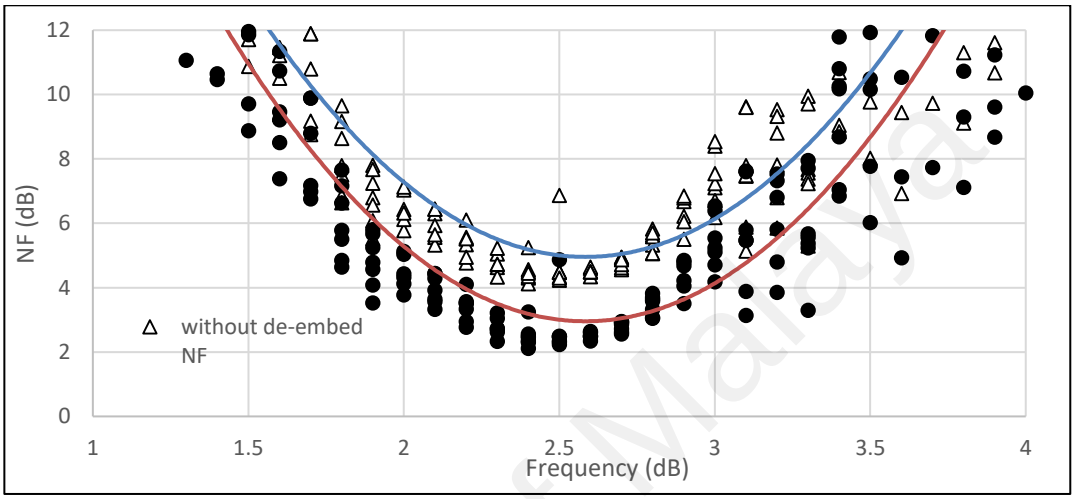

Figure 4.27: Comparison of Noise figure measurement using with and without de-embedding technique of differential cascode PCSNIM LNA implemented with differential inductor.

Base from the NF plot obtained from de-embedding technique as in Figure 4.28, the NF is compared with differential PCSNIM using normal inductor. It shows that by using normal inductor, the NF is better (0.57 dB) compare to using differential inductor the NF is 1.7 dB.

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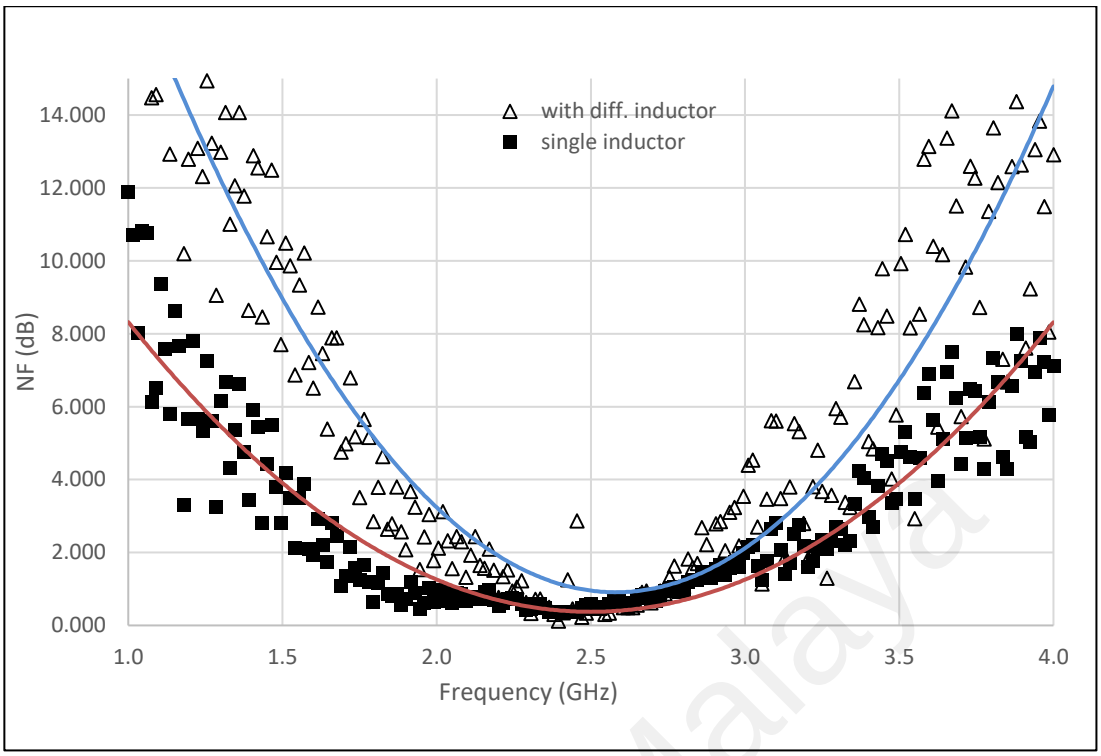

Figure 4.28: Comparison of Noise figure performance for both type differential LNA PCSNIM.

Table 4.5 summarized the differential PCSNIM LNA with differential inductor performance.

Table 4.5: Measurement data for differential PCSNIM with differential inductor LNA.

Data	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	S_{12} (dB)	NF (dB)	IIP3
Pre-layout	19.42	-23.9	-9.3	-36.6	1.8	-9.9
Post- layout	19.23	-32	-34.9	-36.07	2.02	-10.2
Measurement	16	-5, -8[#]	-10	-34	4.2[+], 1.7[*]	-10.5

+: without de-embedding, * : with de-embedding; #: peak at 2.6GHz

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Table 4.6 tabulated the layout and chip micrograph of the selected LNA designed in this research work. The layout is designed using Cadence Virtuoso using Silterra 0.13µm RF CMOS process design kit model. All the design have been fabricated in Silterra and all the measurements were conducted in Cedec, USM.

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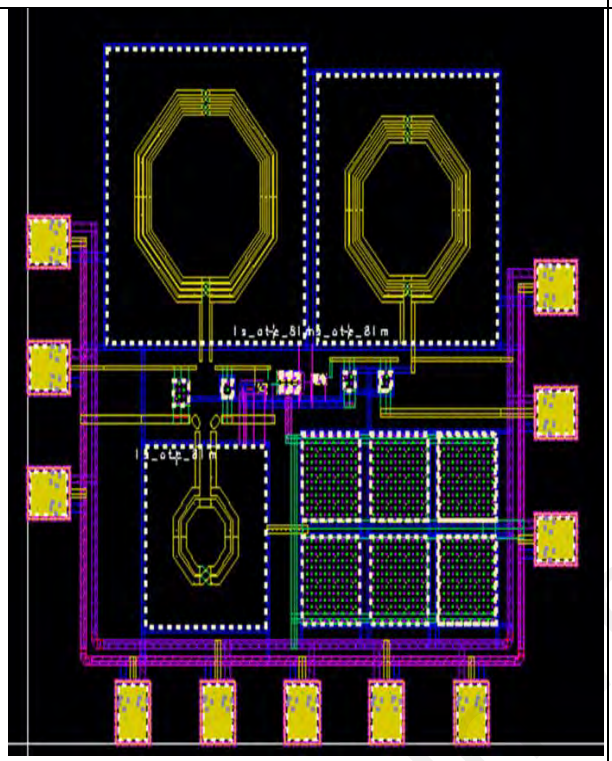
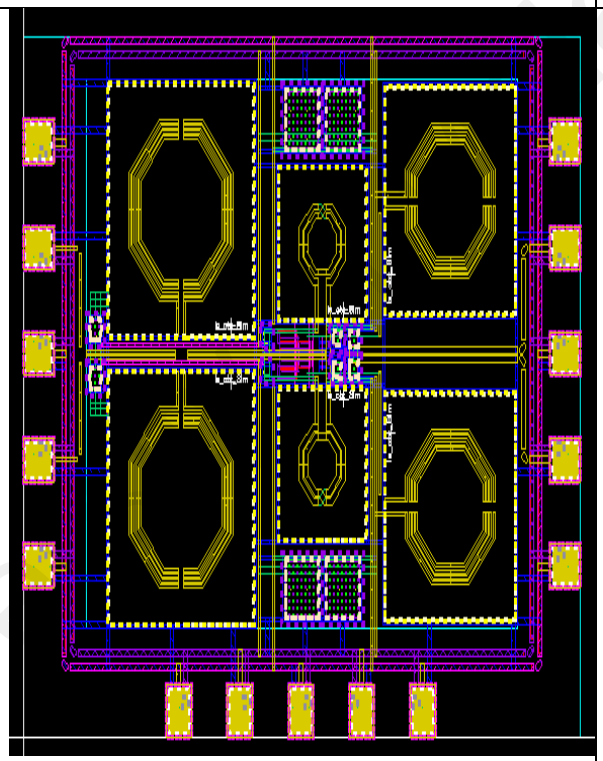
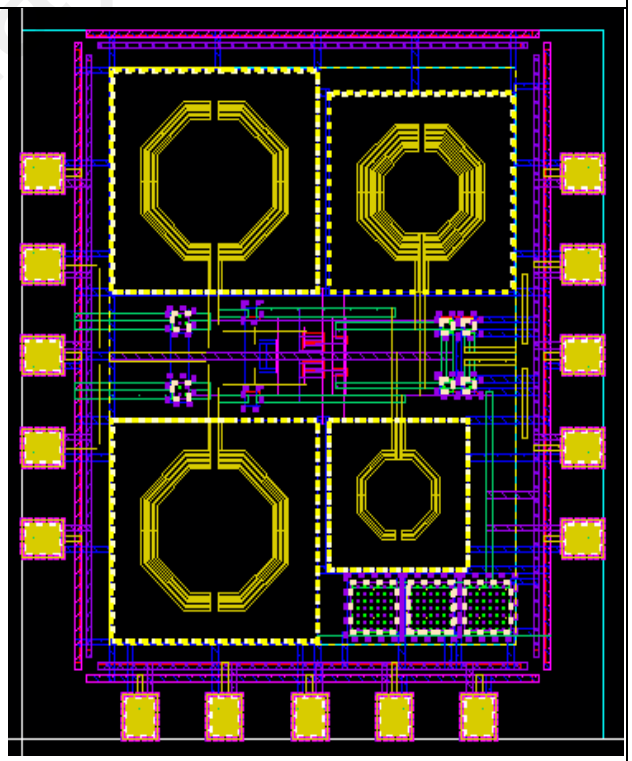
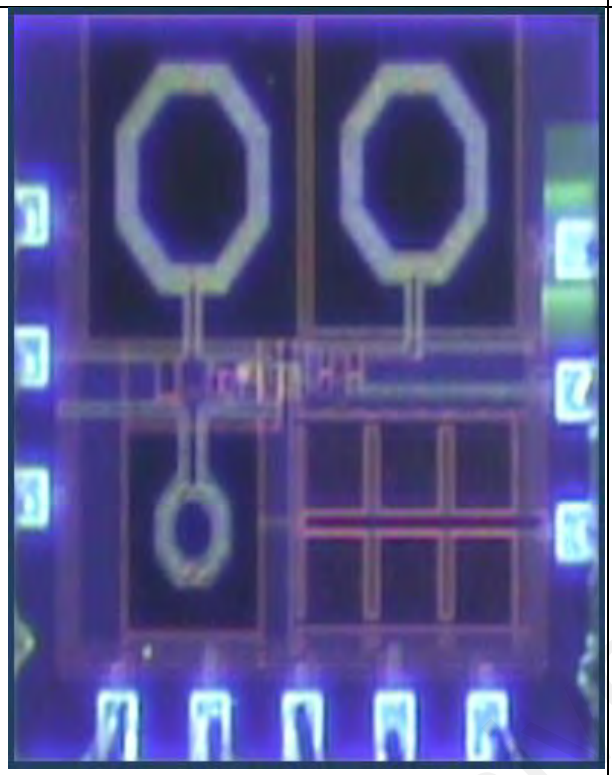
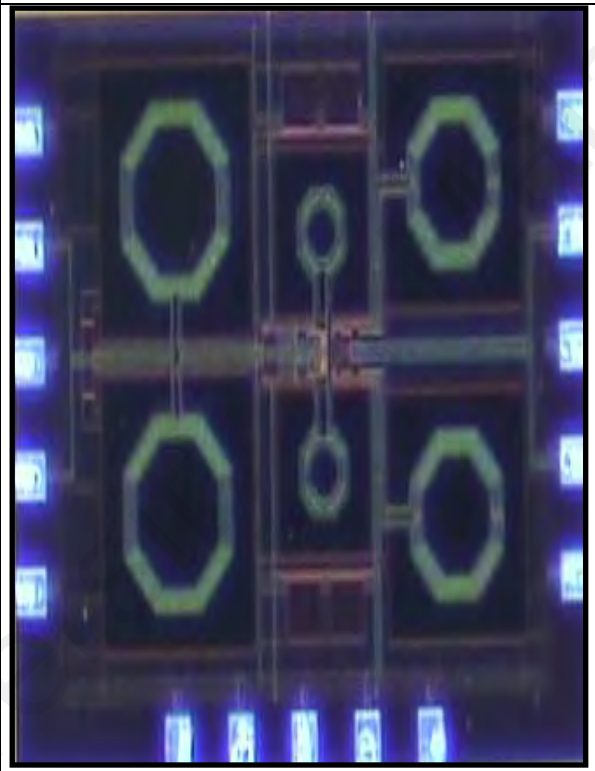
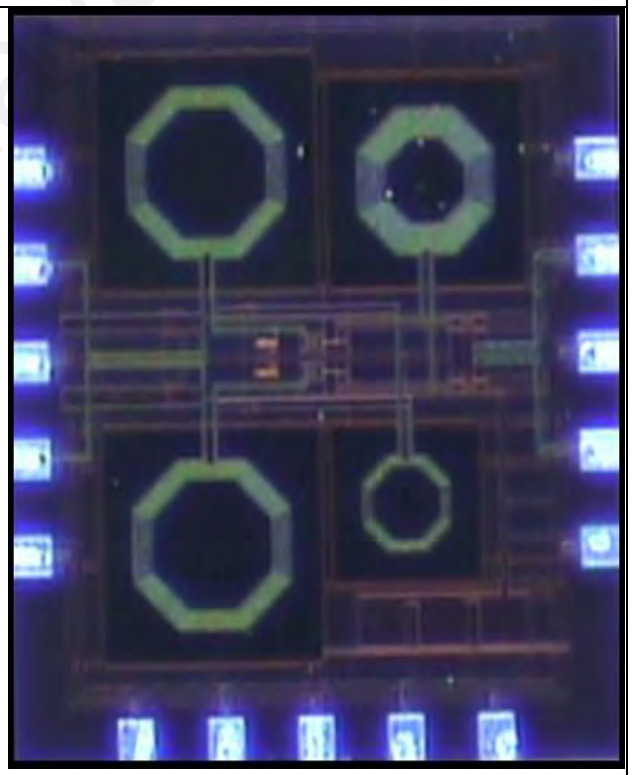
Table 4.6: Layout and chip micrograph of the selected LNA design in this work

Item	Single-ended PCSNIM	Differential PCSNIM	Differential PCSNIM with differential inductor
Layout			
Area	0.814mm^2	0.786mm^2	0.664mm^2

Item	Single-ended PCSNIM	Differential PCSNIM	Differential PCSNIM with differential inductor
Chip micrograph			

4.8 Comparison Performance of LNAs with recently published works

Table 4.7 is presented to compare LNAs proposed in this work and others. The figure of merit (FOM) is used in order to be a fair comparison of LNA tabulated in the table below, (Sahoolizadeh, Jannesari, & Dousti, 2017):

$$FOM = \frac{S_{21}\,(dB)}{P_{dc}(mW).\ NF\ (dB)} \quad \textbf{(4.1)}$$

LNA proposed in this work is considered with the lowest NF and the maximum FOM among the presented in recent years for differential CMOS.

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Table 4.7: Performance comparison with recently published works

References	Tech.	NF (dB)	Gain (dB)	S_{11} (dB)	IIP3 (dBm)	Power (mW)	Area (mm^2)	FOM
(Zokaei & Amirabadi, 2018)	65 nm	3-3.28	13.7-13.9	-10	11.9	16.5	0.113	0.28
(Zokaei et al., 2015)	130 nm	3.9	14	-15	4	21	0.315	0.17
(Abdulaziz et al., 2017)	65 nm	~2	25	-15	17	12.6	0.05	0.99
(Duan et al., 2012)	180 nm	3.2	15.6	-12	-	9.36	1.170	0.52
(Rastegar & Ryu, 2015)	130 nm	0.9-4.1	10.24	-10	6.8	17.2	-	0.24
(Yan & Lin, 2017)	180 nm	2.9 – 3.5	17.5	-	10.6	9.7	0.631	1.38
This work (single)	130 nm	2.1^{*}, 3.9^{+}	15.6	-20	-11	4.34	0.814	1.71
This work (Differential)	130 nm	0.57^{*}, 1.2^{+}	17.12	-27	-10.5	7	0.786	4.29^{*} 1.35^{+}
This work (with differential inductor)	130 nm	1.7^{*} ,4.2^{+}	16	-8.42	-10.5	4.8	0.664	1.38^{*} 0.79^{+}

+ without de-embedding, *; with de-embedding technique

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4.9 Conclusion

Results based on the major contribution in this work were discussed in this chapter. The discussion was made based on simulation and measurement results for single ended PCSNIM and both differential PCSNIM (with and without differential inductor). The end-design of the optimized differential low noise amplifier produces a power gain of 17.12dB with a dc power consumption of 7.2mW. A linearity of -10.5 dBm I achieved. The LNA has been experimentally verified for its functionality and results a validated peak the performance at 2.4 GHz of operating frequency.

A technique of on wafer S-parameters characterization of differential LNA using Two-Port VNA is presented. S-parameters results validated by using four-port network analyzer. This technique achieves to give measurement data as precise as four-port VNA equipment. Comparison for both measurement data is presented and show small percentage difference between the two. This difference might be due to probe placement position and planarity variation. However, this small difference still can be justified and show good agreement between the two equipment's set up.

On-wafer de-embedding measurement technique for differential LNA with the analysis of two gain definition was presented. A simple calibration and measurement have been presented. Insertion gain was compared to an available gain, and the influence of impedance mismatch on NF performance was analysed. The detailed procedure and equations for extracting differential NF based on Friis equation have been derived. The set-up of the de-embedding technique were proposed by utilizing the scattering parameter. An improvement in NF has been shown by utilizing the de-embedding technique by considering the proper gain definition. At 2.4 GHz LNA was measured as an example which shows accurate result compared with other methods. In addition, the results showed that the use of an insertion gain may not give a better result and an accurate

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NF measurement. A more accurate NF measurement can be achieved by using an available gain as an alternative while also considering input and output matching.

Lastly, the comparison between this work and published works are shown focusing on the s-parameter, noise figure and IIP3 of the LNA.

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CHAPTER 5: CONCLUSION AND FUTURE WORKS

5.1 Conclusion

LNAs are important as they help to reduce the overall NF of a receiver. There are four basic amplifier topologies described in thesis which are the CS with shunt-input resistor, CG, shunt-series and finally the inductively degenerated CS amplifier. From these topologies, the inductively degenerated CS amplifier is considered to be the topology capable of providing the best noise performance due to the absence of resistors in its circuit. Series resistors of the inductors used in this topology are the only resistances that will contribute to the resistors' thermal noise. More importantly, the degenerated inductor helps to bring the optimum noise impedance closer to the optimum source impedance without significantly affecting the noise resistance and minimum noise figure.

Subsequent to the determination of the right topology for good noise performance, the focus turned to enhancing the performance of the LNA in terms of the other performance metrics such as gain and reverse isolation. As the LNA is to be used in a DCR, the topology must be able to minimize the LO-band leakage problem existing in a DCR. Thus, the LNA needs to possess good reverse isolation characteristic. Due to this requirement, the cascode topology was to be implemented. A cascode can also increase the gain as compared to a single-stage CS LNA.

As the LNA is for the wireless LAN application, power consumption of the LNA is best kept to its minimum possible for implementations in mobile systems. For the WLAN standard, a typical current consumption for a single-input LNA is less than 4 mA and this results in a power consumption of approximately 7 mW at a supply voltage of 1.2 V for a design implemented on a 0.13 μm process. The end-design of the optimized differential low noise amplifier PCSNIM in this work manage to produce a power gain of 17.12dB with a dc power consumption of 7.2mW. The LNA has been experimentally

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verified for its functionality and results a validated peak the performance at 2.4GHz of operating frequency which is the center frequency for WLAN / IEEE 802.11b/g standard.

In order to achieve the many design goals targeted for the LNA, the correct choice of the LNA topology becomes very important. Many topologies were invented to optimize the performance of the LNA. The constraint with this LNA is the minimum noise figure may become worse if smaller devices are used. Under this condition, a higher degeneration inductor is required which will move the minimum noise figure away from the minimum noise figure of the classical input matching LNAs. In the PCSNIM LNA, a capacitor is connected between the G-S of the device to relax the requirement for large gate inductance if the device is small. In the CR, the input transistor of a conventional NMOS cascode is replaced with an inverter-like combination of PMOS and NMOS to reduce power consumption but maintaining the transconductance in order not to reduce the gain.

A detailed LNA design methodology is given in this thesis starting from the calculation of the transistor's size based on the power constrained NF optimization technique. The LNA topology chosen for describing the design methodology was from the SNIM type. The derivations for determining the transistor's size were meticulously detailed and comprehensive. The biasing circuit for all the LNAs designed in this work was based on the conventional simple current mirror.

A technique of on wafer S-parameters characterization of differential LNA using Two-Port VNA is presented. S-parameters results validated by using four-port network analyzer. This technique achieves to give measurement data as precise as four-port VNA equipment. Comparison for both measurement data is presented and show small percentage difference between the two. This difference might be due to probe placement position and planarity variation. However, this small difference still can be justified and show good agreement between the two equipment's set up.

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On-wafer de-embedding measurement technique for differential LNA with the analysis of two gain definition was presented. A simple calibration and measurement have been presented. Insertion gain was compared to an available gain, and the influence of impedance mismatch on NF performance was analysed. The detailed procedure and equations for extracting differential NF based on Friis equation have been derived. The set-up of the de-embedding technique were proposed by utilizing the scattering parameter. An improvement in NF has been shown by utilizing the de-embedding technique by considering the proper gain definition. At 2.4GHz LNA was measured as an example which shows accurate result compared with other methods. In addition, the results showed that the use of an insertion gain may not give a better result and an accurate NF measurement. A more accurate NF measurement can be achieved by using an available gain as an alternative while also considering input and output matching.

5.2 Accomplishments

The following are the accomplishments achieved following the objectives that had been set at the beginning of the study:

- A modified differential LNA Power Constrained Simultaneously Input Matching (PCSNIM) was designed. The performance metrics of this LNA showed that it is able to provide superior gain and noise performances as compared to the Simultaneously Noise Input Matching (SNIM) and conventional PCSNIM. The most important merit of this circuit is its ability to implement on-chip matching without the usage of bulky L-C matching network. A systematic approach on the design methodology of the inductively degenerated cascade LNA was presented. The methodology starts with determining the requirements imposed by the WLAN on the LNA, followed by small-signal derivations to determine gain and noise performances, matching steps for performance optimization to finally characterization of the fabricated design.

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- Detailed and systematic approach on the design methodology Power-Constrained Noise Optimization (PCNO) of the modified inductively degenerated cascode LNAs was given.
- Detailed and comprehensive design analysis and performance comparison gain, S-parameters and noise derivations for the inductively degenerated LNA were shown in this thesis. The gain and S-parameters were derived from the small-signal model of the inductively degenerated cascode LNA.
- A technique of on wafer S-parameters characterization of differential LNA using two-Port VNA is presented. S-parameters results validated by using four-port network analyzer. This technique achieves to give measurement data as precise as four-port VNA equipment. Comparison for both measurement data is presented and show small percentage difference between the two.
- On-wafer de-embedding measurement technique for differential LNA with the analysis of two gain definition was presented. A simple calibration and measurement have been presented. Insertion gain was compared to an available gain, and the influence of impedance mismatch on NF performance was analysed. The detailed procedure and equations for extracting differential NF based on Friis equation have been derived.

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5.3 Future works

Based on the work presented here, there are several aspects which can be extended. Firstly, the extend of this work can be done on the study and analysis of the process variation (namely the resistor, capacitor and device conditions) effects that influence the performance of the LNA. An extension to this work can be in determining the effects of the inductor on the circuit's performance. Besides this, the other contributors to the circuit's performance are the temperature and supply variations and investigations on their effects on the LNA performance should also be included in future work.

Future work should include analysis and characterization of the differential LNAs using active balun circuit to assist the measurement of differential structures. These will be more interesting as the supposedly enhanced linearity and noise capabilities of the differential topology can be determined physically.

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Journal under review:

1. M. Muhamad, N. Soin and H. Ramiah, **Integration the VLSI Journal by Elsevier** - *Noise Figure Optimization and Gain Enhancement Technique of 0.13µm CMOS Differential LNA*

2. M. Muhamad, N. Soin and H. Ramiah **International Journal of Electronics** – *On Wafer Noise Figure De-Embedding Method for CMOS Differential LNA*

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