SINGLE-PHASE CASCADED T AND π-TYPE GRID-CONNECTED PV INVERTERS WITH CAPACITOR VOLTAGE BALANCING

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SINGLE-PHASE CASCADED T AND π-TYPE GRID-CONNECTED PV INVERTERS WITH CAPACITOR VOLTAGE BALANCING

ABSTRACT

This thesis presents the development of single-phase T and π-type Cascaded H-Bridge inverters for a grid-connected photovoltaic (PV) system. The T-type Cascaded H-Bridge (TCHB) single-phase inverter utilizes two T-type Bidirectional Switches (BSs) and is capable of generating an output-voltage of nine levels (2Vdc, 3Vdc/2, Vdc, Vdc/2, 0, −Vdc/2, −Vdc, −3Vdc/2, −2Vdc) from two separate dc supply voltages. The π-type Cascaded H-Bridge (PiCHB) single-phase inverter employs two π-type BSs and can produce an output-voltage of thirteen levels (2Vdc, 5Vdc/3, 4Vdc/3, Vdc, 2Vdc/3, Vdc/3, 0, −Vdc/3, −2Vdc/3, −Vdc, −4Vdc/3, −5Vdc/3, −2Vdc) from two separate dc supply voltages. In addition, to validate the improved performance of the suggested structures, the TCHB and PiCHB topologies are compared against various other symmetric cascaded topologies, considering the parameters of number of switches N_{igbt} employed, number of gate drivers N_{driver} used, standing voltages V_{stand} on the semiconductor switches and cost function CF.

To realize a low frequency switching, the switching angles were optimized by the Optimized Harmonic Elimination Stepped Waveform (OHESW) technique, whose resulting transcendental equations were solved by an open bracketed numerical method technique. Among the multiple solution sets obtained, the solution offering least output-voltage THD was selected.

High frequency switching with one triangular carrier signal and identical modulation signals at eight and twelve different offsets generated the PWM signals for the stated TCHB and PiCHB inverters, respectively. The PWM switching pulses were attained by the intersection of a high-frequency triangular carrier against low-frequency sinusoidal

signals. These low-frequency signals were considered as the modulating (or reference) signals.

Maximum power point tracking (MPPT) technique based on modified incremental conductance (mINC) method, anti-islanding protection and a digital proportional–integral (PI) current-control algorithm had been employed for the grid-connected PV system application. A TMS320F28335 DSP and an ALTERA cyclone II FPGA board had been used to implement the proposed closed-loop control system.

To validate the performance of the Grid-tied PV system, simulation results were attained by utilizing Matlab/Simulink software, and the experiments, were performed on a hardware prototype.

Keywords: Maximum power point tracking (MPPT); modified incremental conductance (mINC) MPPT; T-type nine-level inverter; π-type thirteen-level inverter; pulse width-modulated (PWM).

PENYONGSANG PHOTOVALTAIK FASA TUNGGAL TERSAMBUNG GRID JENIS T DAN π DENGAN PENGIMBANGAN VOLTAN KAPASITOR

ABSTRAK

Tesis ini membentangkan pembangunan inverters H-Bridge Cascaded T dan π fasa tunggal untuk sistem photovoltaic (PV) yang terikat grid. Inverter fasa tunggal T-Cascaded H-Bridge (TCHB) menggunakan dua suis Bidirectional Tipe (BS) dan mampu menghasilkan voltan keluaran sembilan tahap (2Vdc, 3Vdc / 2, Vdc, Vdc / 2, 0, -Vdc / 2, -Vdc, -3Vdc / 2, -2Vdc) daripada dua voltan pembekalan dc yang berasingan. Sedangkan inverter satu fasa Cascaded H-Bridge (PiCHB) π-jenis Cascaded H-Bridge (PiCHB) menggunakan dua jenis π-jenis dan dapat menghasilkan voltan keluaran tiga belas (2Vdc, 5Vdc / 3, 4Vdc / 3, Vdc, 2Vdc / Vdc / 3, 0, -Vdc / 3, -2Vdc / 3, -Vdc, -4Vdc / 3, -5Vdc / 3, -2Vdc) daripada dua voltan pembekalan dc yang berasingan. Di samping itu, untuk mengesahkan peningkatan prestasi struktur yang dicadangkan, topologi TCHB dan PiCHB dibandingkan dengan pelbagai topologi casetik yang lain, memandangkan parameter bilangan suis N_{igbt} digunakan, bilangan pemandu pintu N_{driver} digunakan, voltan tetap V_{stand} pada semikonduktor suis dan fungsi kos CF.

Untuk mencapai peralihan kekerapan yang rendah, sudut pensuisan dioptimumkan oleh teknik Pengekalan Harmonik Kaedah Penghapusan Harmonik yang Dioptimumkan (OHESW), yang menghasilkan persamaan transenden yang telah diselesaikan oleh teknik kaedah berangka terbuka. Di antara pelbagai penyelesaian penyelesaian yang diperolehi, larutan yang menawarkan THD voltan keluaran minimum dipilih.

Pengalihan kekerapan tinggi dengan satu isyarat pembawa segitiga dan isyarat modulasi yang serupa pada lapan dan dua belas offset yang berbeza menghasilkan isyarat PWM untuk inverters TCHB dan PiCHB yang dinyatakan. PWM beralih denyutan dicapai oleh persimpangan pengangkut segi tiga frekuensi tinggi terhadap isyarat

sinusoidal frekuensi rendah. Isyarat frekuensi rendah ini dianggap sebagai isyarat modulasi (atau rujukan).

Teknik pengesanan titik kuasa maksimum (MPPT) berdasarkan kaedah konduktansifkan tambahan (mINC) yang telah diubahsuai, perlindungan anti-pulau dan algoritma kawalan semasa berkadar digital (PI) telah digunakan untuk aplikasi sistem PV yang berkaitan grid. Sebuah DSP TMS320F28335 dan sebuah papan FPGA siklon II ALTERA telah digunakan untuk melaksanakan sistem kawalan gelung tertutup yang dicadangkan.

Untuk mengesahkan prestasi sistem PV bertalian Grid, hasil simulasi dicapai dengan menggunakan perisian Matlab / Simulink, dan eksperimen, dilakukan pada prototaip perkakasan.

Kata kunci: pengesanan titik kuasa maksima (MPPT); ubah bentuk konduktansan tambahan (mINC) MPPT; penyongsang sembilan peringkat T; jenis penyongsang 13; denyutan lebar denyutan (PWM).

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS AND ABBREVIATIONS

Symbols

A	:	Ampere
a	:	The number of cascades.
α	:	Weight factor
Ah	:	Ampere-hour
a	:	Ideality factor
b	:	Capacitors in each cascade
C	:	Capacity/Capacitance
CF	:	Cost function
Δ	:	Change
D_{max}	:	Predefined maximum limit for the duty cycle
dI_{PV}	:	Change of current
dD	:	Change in duty ratio
D	:	Duty Cycle
dP_{PV}	:	Change in power
dV_{PV}	:	Change of voltage
dP_{PV}/dD	:	Change in power over change in duty ratio
dT	:	Temperature Change
dI_{PV}	:	Change of current
dD	:	Change in duty ratio
e	:	Tolerance error
E_g	:	Energy gap
G	:	Irradiance
G_n	:	Nominal Irradiance

Hz	:	Hertz
$I_{pv,cell}$	:	Current generated
$I_{o,cell}$	:	Diode leakage current
I_{MAX}	:	Maximum allowable current
I_{pv}	:	Current produced by photons
I_{mpp}	:	Current at MPP
I_0	:	Reverse saturation current corresponding to the diode
I_{sh}	:	Short circuit current
kW_p	:	Kilowatt-peak
k	:	Boltzmann constant
N_s	:	Number of cell in series
N_p	:	Number of cell in parallel
N_{level}	:	The number of output-voltage levels
N_{IGBT}	:	Semiconductor switches employed
N_{driver}	:	The number of gate drivers for the semiconductor switches
η_{mppt}	:	MPPT efficiency
$P_{dc}(V_O)$	:	Output power delivered
$P_{dc}(V_{mp})$	:	Theoretical power at the MPP voltage
Q	:	Electron charge
R_s	:	Series resistance
R_{sh}	:	Shunt resistance
T	:	Temperature at p-n junction
T_n	:	Nominal Temperature
V_t	:	Thermal Voltage
V_o	:	Output Voltage
V_{in}	:	Input Voltage

V_T	:	Thermal voltage of diode
V_c	:	Voltage on each capacitor
V_{stand}	:	Standing-Voltage on semiconductor switches
$V_{stand,i}$	:	Total Standing-Voltage
V_{oc}	:	Open circuit voltage
W/m^2	:	Watt per meter square

Abbreviations

AC		Alternating Current
ACO	:	Ant Colony Optimization
ADC	:	Analog to Digital Converter
Ah	:	Ampere-hour
ANN	:	Artificial Neutral Network
BN	:	Bayesian Network
BNM	:	Brent Numerical Method
BS	:	Bidirectional Switch
BSs	:	Bidirectional Switches
BSM	:	Bisection Search Method
BVS	:	Balanced Voltage Sharing
CC	:	Constant Current
CHB	:	Cascaded H-Bridge
CNM	:	Classical Numerical Methods
CV	:	Constant Voltage
DC	:	Direct Current
DSP	:	Digital Signal Processor
EMC	:	Electromagnetic Compatibility
EMI	:	Electromagnetic Interference

FA	:	Firefly Algorithm
FC	:	Flying Capacitor
FL	:	Fuzzy Logic
FPGA	:	Field Programmable Gated Array
HC	:	Hill Climbing
HT	:	Hybrid Techniques
IGBT	:	Insulated Gate Bipolar Transistor
InC	:	Incremental Conductance
I-V	:	Current-Voltage
I2C	:	Inter-Integrated Circuit
LED	:	Light Emitting Diode
LVT	:	Lower Voltage Threshold
MLI	:	Multi-level Inverter
MPP	:	Maximum Power Point
mINC	:	Modified Incremental Conductance
MCNM	:	Modified Classical Numerical Methods
MBSM	:	Modified Bisection Search Method
MRFM	:	Modified Regula Falsi Method
MNRM	:	Modified Newton Raphson Method
MSM	:	Modified Secant Method
MBNM	:	Modified Brent Numerical Method
MOSFET	:	Metal–Oxide–Semiconductor Field-Effect Transistor
NN	:	Neural Network
NRM	:	Newton Raphson Method
NPC	:	Neutral-Point Clamped
OHESW	:	Optimized Harmonic Elimination Stepped Waveform

OCC	:	One-Cycle Control
OP	:	Operating Point
OVP	:	Over-Voltage Protection
OFP	:	Over-Frequency Protection
PiCHB	:	π-type Cascaded H-Bridge
PSO	:	Particle Swarm Optimization
PI	:	Proportional–Integral
PID	:	Proportional-Integral-Derivative
PV	:	Photovoltaic
PWM		Pulse-Width Modulation
P&O	:	Perturb & Observe
P-V	:	Power-Voltage
PM	:	Predictor Method
PSO	:	Swarm Optimization
RCC	:	Ripple Correlation Control
RS		Reduced Switch
RFM	:	Regula Falsi Method
SM	:	Secant Method
SMC	:	Slide Mode Control
SEPIC	:	Single Ended Primary Inductor Converter
STC	:	Standard Test Conditions
SVM	:	Space-Vector Modulation
TCHB	:	T-type Cascaded H-Bridge
THD	:	Total Harmonic Distortion
UVT	:	Upper Voltage Threshold

LIST OF APPENDICES

CHAPTER 1: INTRODUCTION

1.1 Background

As technology rapidly develops, energy consumption across the globe is expected to increase and fossil energy is anticipated to be insufficient in the near future. This has called for an increase in extensive research on renewable energy these recent years (Chu & Majumdar, 2012). Solar energy, in particular, has received much attention because it is abundant, clean and reliable. According to (Kabir, Kumar, Kumar, Adelodun, & Kim, 2018), amongst the highest electricity generation in renewable energies field, solar energy yield is expected to grow continuously in near future.

Solar energy is clean and reliable. However, the PV array output is dependent on environmental variations. Therefore, harnessing maximum output from the solar PV array by MPPT techniques has been an advancing topic of research. A digital and analog classification of such techniques is presented in (A. Amir, Amir, Selvaraj, & Rahim, 2016). Most of these techniques are applicable to different PV systems. The PV system is classified into three types namely the grid-tied, stand-alone, and the hybrid PV system.

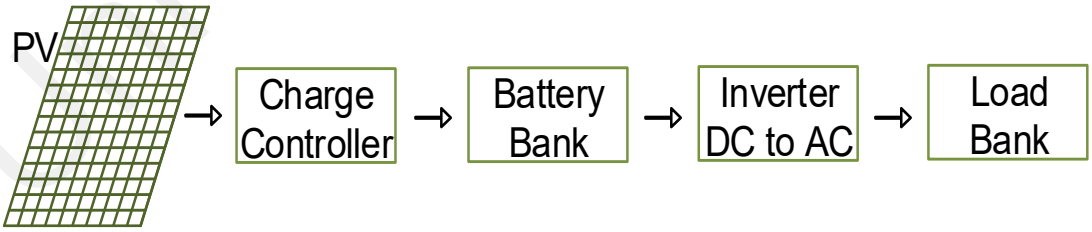


Figure 1.1: Block diagram for stand-alone PV system with battery pack

Stand-alone PV system uses solar energy as the only power source while grid-connected PV system and hybrid PV system use solar energy together with other types of energy. In remote and rural areas, standalone PV system is used where PV panels act as the only power source (Arricibita, Sanchis, González, & Marroyo, 2017). Figure 1.1

shows standard configuration of a stand-alone solar energy system consisting of an energy storage, charger controller and inverter.

By the application of a grid-tied PV system, power generated from the PV panels can be injected into the grid. In this configuration, PV panels act as a secondary power generator, which produce DC. However, before being fed to the grid, there remains a necessity for DC conversion into AC. Such systems can be used for residential (B. Liu et al., 2018), and industrial (Wu et al., 2017) applications.

Hybrid by definition is a combination of two different sources or methods, used together to achieve a common goal. Two or more sources of power merged together in a system to realize a hybrid power system in order to provide uninterrupted power supply to load (Halabi, Mekhilef, Olatomiwa, & Hazelton, 2017). A typical configuration of the hybrid battery-diesel generator system has been presented in Figure 1.2. The system also uses battery as energy storage to store excessive energy generated by PV panels.

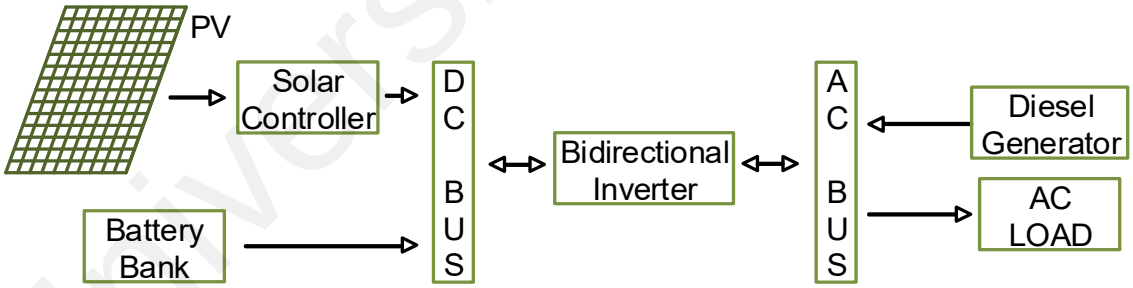


Figure 1.2: Block diagram for hybrid PV system

Considerable focus remains on grid connected systems. As most electrical loads take AC, whereas PV energy is DC, so a power converter is required to convert the DC power produced from the PV panels into AC power for electrical loads, known as PV inverter.

PV inverter classification is based on its output voltage waveform type. There are square wave, quasi-square wave, quasi-sine (multilevel) wave, and sine wave, inverters.

Most inverters for stand-alone PV systems are square wave, quasi square wave, or multilevel inverters (MLI) and use low frequency switching, whereas for grid-connected systems the inverters are sine wave or multilevel and use high frequency switching. Researchers have suggested various single-phase inverter topologies, yet the MLI acquire a prominent position (Malinowski, Gopakumar, Rodriguez, & Perez, 2010; Prabaharan & Palanisamy, 2017). Multilevel Stand-alone (Daher, Schmid, & Antunes, 2008) and Grid-tied inverters are favorable; as such topologies offer reduced standing voltages on the semiconductor devices, reduced switching losses, electromagnetic interference (EMI), filter size, better harmonic profile of output-current and voltage; resulting into a compact, economical and effective design (Prabaharan & Palanisamy, 2017). Considering the fundamental structure, MLI have been classified into three assemblies. Neutral-Point Clamped (NPC) (Busquets-Monge, Filba-Martinez, Alepuz, & Calle-Prado, 2017), flying capacitor (FC) or multicell (Farivar, Ghias, Hredzak, Pou, & Agelidis, 2017), and cascaded H-bridge (CHB) (Fuentes et al., 2017).

Owing to its structural requirements, the capacitor voltage balancing in the FC remains complex as it needs a higher amount capacitors for increased levels of the output voltage. Moreover, for synthesizing higher output-voltage levels, NPC requires a greater amount of clamping diodes. In addition, the balanced voltage at the input capacitors remains a shortcoming of the NPC. In contrast, CHB converters offer a nominal standing voltage, quality output and simpler DC-link voltage balancing. Considering symmetric CHB converters, balanced DC-link voltage sharing is required. As unbalanced state of operation can increase voltage stress on the switches damaging the entire system.

Improving quality of electricity to be injected into the grid requires the improvement in Total Harmonic Distortion (THD) for the output-voltage and current of the inverter. Reduced THD is acquired by increasing the levels produced by the inverter at the output

for voltage. As, increased EMI, THD and switching losses offered by three-level inverter make it less effective for Grid-Integration. Therefore, to reduce the switching losses, THD and EMI, MLI design configuration has been employed with a stand-alone and grid-tied PV system.

In this thesis, the development of a symmetric cascaded H-bridge single-phase MLI has been recounted with T and π-type bidirectional switches providing the TCHB and PiCHB topologies, respectively. These topological designs with high frequency switching were applied to a grid-tied PV system. Here, a self-voltage balancing PWM scheme has been provided for the TCHB topology and a passive balancing circuit comprised of an RLC branch had been utilized for the balanced voltage sharing (BVS) of the DC-link capacitors for the PiCHB design. Moreover, algorithms for MPPT based on mINC algorithm, linear current control based on a PI controller, and anti-islanding protection were also developed utilizing a TMS320F28335 DSP board.

1.2 Research Questions

Study of the grid-tied PV inverters and how they are beneficial, sparked interest for the following research questions:

i. Why is solar energy one of the best renewable energy options to tackle increasing energy demands?
ii. How to improve the Maximum Power Point Tracking technique to harness photovoltaic energy?
iii. What improvements can be made to the conventional PV inverters in terms of AC waveform quality, number of devices, number of switches, number of gate drivers, power losses, standing voltages and cost function?
iv. What is the necessity of an improved grid-tied PV system?

1.3 Research Objectives

Research objectives of this thesis are listed as follows:

1. To develop novel TCHB and PiCHB grid-connected PV inverters with PWM control schemes utilizing eight and twelve identical reference signals.
2. To compare the proposed TCHB and PiCHB configuration against various symmetric cascaded MLI topologies.
3. To verify and validate the self-balancing PWM scheme for the TCHB MLI topology and passive balancing circuit for PiCHB.
4. To simulate and develop a hardware prototype implementing the proposed PWM switching scheme for the TCHB and PiCHB grid-connected MLI.
5. To develop a control system for grid-connection employing algorithms for MPPT based on mINC, PI-based current control and anti-islanding protection.

1.4 Overview of the Chapters

This thesis is written in six chapters and each chapter can be briefly explained as follows:

Chapter 2: An overview of the solar energy system has been presented in this chapter. First, the fundamentals of PV panel characteristics, under various ambient irradiance levels and changing temperatures, are focused. In addition, theoretical analysis of the current-voltage (I-V) and power-voltage (P-V) graphical plots has been provided, followed by a comprehensive review on several analog and digital MPPT techniques employed for PV systems. Second, the chapter presents a novel mINC MPPT technique and compares its effective performance with the conventional MPPT techniques. Further, various single-phase inverter topologies have been surveyed, particularly focusing MLI design topologies. Here, different modulation schemes of operation and current-control techniques, feeding power to the grid, have also been explored.

Chapter 3: describes the proposed configuration for the single-phase TCHB nine-level and PiCHB thirteen-level inverters with capacitor voltage balancing. A comparative analysis has been presented of the proposed inverter topologies against various symmetric CHB topologies. Further, the chapter details the inverter operating principles, design considerations, proposed PWM schemes and offers theoretical analysis to validate the requirement of balanced voltage sharing at the DC-Link capacitors to attain a better harmonic profile for the output-voltage and current for grid-connection.

Chapter 4: Simulation results for the proposed TCHB and PiCHB inverters for low switching frequency, high switching frequency, and the PV application have been presented in this chapter. This chapter also recounts simulation of the current-voltage (I-V) and power-voltage (P-V) curves under varying environmental conditions.

Chapter 5: presents the hardware implementation, which comprises of hardware configuration, experimental results for high switching frequency, for the TCHB PWM scheme, PiCHB PWM scheme, operation of the passive balancing circuit for balanced voltage sharing and the PV application. Results for both stand-alone and grid-connected PV application with the proposed control algorithms implemented on DSP TMS320F28335 have been displayed.

Chapter 6: concludes with a summary, a listing of the author's contributions, and recommendations for possible future work.

CHAPTER 2: OVERVIEW OF SOLAR ENERGY SYSTEM

2.1 Introduction

Solar energy systems are one of various renewable energy sources (RES). Owing to the abundance of solar energy, PV systems remain reliable RES. Such systems have the capability to supply endless energy that would be limited only by the amount of solar irradiation and system inefficiencies. In addition, the PV systems remain clean, emission free and environment friendly (Kabir et al., 2018).

A PV system mainly comprises of PV panels made of PV cells, which are electronic devices that convert solar energy to electric energy, and Power converters employing various control systems to supply the required amount of power to the load.

This thesis focuses on the grid-connected PV systems. In particular, for grid-connection high power is needed to inject current into the grid. To maximize PV power generation, MPPT is considered a reliable control scheme (Aamir Amir, Amir, Selvaraj, Rahim, & Abusorrah, 2017). In this chapter an overview of the entire solar energy system has been presented by highlighting the PV panel characteristics (Villalva, Gazoli, & Ruppert Filho, 2009), reviewing different MPPT techniques (A. Amir et al., 2016), presenting a novel MPPT technique based on mINC (Aamir Amir et al., 2017), discussing power converters and surveying various MLI topologies employing different modulation and current-control schemes.

2.2 PV Panel Characteristics

Solar cell is made of semiconductor layers to form a p-n junction. Where, P channel material contains excessive holes and N channel material contains excessive electrons. By exposing solar cell to sunlight, the electrons and holes from n and p channel semiconductors will swap position due to the electrical field excitation, which creates the

electrical current. One cell generally produces around 0.5-0.6V at no load condition. In order to have a usable voltage, several cells are made in series connected fashion to design a panel. To form one PV panel, typically 36 or 72 cells are connected in a series fashion. The fundamental equation for an ideal PV cell can be written as follows (Villalva et al., 2009):

$$I_o = I_{prod} - I_{leak}\left[exp\left(\frac{qV_{out}}{akTemp}\right) - 1\right] \quad (2.1)$$

where I_{prod} is produced current, I_{leak} is the leakage diode current, *Temp* being the p-n junction temperature, Ideality constant of diode is a, Boltzmann constant is k, q Charge of an electron, I_o Output-current of PV and V_o Output-current of PV.

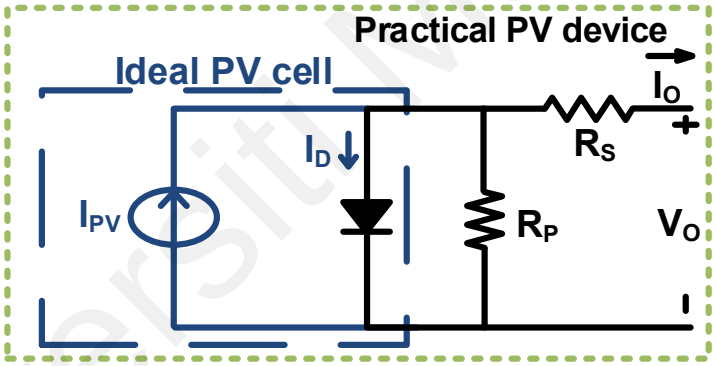


Figure 2.1: Electrical model of PV cell

A real PV panel characteristic cannot be modeled as presented by Figure 2.1, as practical PV module is made of various PV cells connected in series. Ideal PV cell model without resistor (highlighted in the dotted box) is illustrated in Figure 2.1. Here, additional resistors can be added to realize this practical PV panel. R_s remains series resistance to the PV, while R_p leakage current loss in the p-n junction which differs with fabrication method, utilized for PV cell manufacturing process or also known as shunt resistor. Generally, to simplify the calculation, one of these two resistance values is neglected. R_s is ideally zero and practically very low whereas R_p is ideally infinity and practically high in value.

Apart from these two internal parameters which influence the output values of solar cell. External parameters also contribute by significantly effecting the output-current and voltage produced by the PV cell. Therefore, the circuit in Figure 2.1 can be mathematically written as follow:

$$I_o = I_{cell} - I_{sat}\left[exp\left(\frac{V_o - R_s I}{V_t a}\right) - 1\right] - \frac{V_o + R_s I}{R_p} \tag{2.2}$$

I_{cell} and I_{sat} are light generated and the saturation current, respectively.

As PV cells are power sources, connecting PV cells in series will increase voltage value at the output terminal and parallel connection will increase current output. Output voltage of a series connection of PV cells can be obtained using (2.3) with N_s being number of series cells.

$$V_t = \frac{N_s kT}{q} \tag{2.3}$$

As aforementioned, I_{cell} remains in direct proportionality to the solar irradiance during the daytime. The relationship between irradiance, temperature and I_{pv} can be explained in the following equation:

$$I_{pv} = (I_{sc,n} + K_1 \cdot \Delta T) \cdot \frac{G}{G_n} \tag{2.4}$$

where $\Delta T = T - T_n$ remains difference between the nominal and measured temperature, $I_{sc,n}$ remains cell short circuit current, G_n the irradiance at nominal condition, K_1 being the PV current coefficiency and G the irradiance reading. I_{ds} diode saturation current, can be expressed as:

$$I_{ds} = I_{d,n}\left(\frac{T_n}{T}\right)^3 \cdot \left[exp\left(\frac{E_g q}{ak}\left(\frac{1}{T_n} - \frac{1}{T}\right)\right)\right] \tag{2.5}$$

where $I_{d,n}$ remains nominal diode saturation current and $E_g$is the bandgap energy (Villalva et al., 2009). In order to determine the I_{sc}, V_{oc}, MPP circuit and efficiency equation boundary conditions are to be employed on equation (2.1) as presented in (Cubas, Pindado, & Victoria, 2014):

For I_{sc} equation:

$$I_{sc} = I_{pv} - I_0 \left[exp\left(\frac{I_{sc}R_s}{aV_T}\right) - 1\right] - \frac{I_{sc}R_s}{R_p} \tag{2.6}$$

For V_{oc} equation:

$$0 = I_{pv} - I_0 \left[exp\left(\frac{V_{oc}}{aV_T}\right) - 1\right] - \frac{V_{oc}}{R_p} \tag{2.7}$$

The current and voltage generated at different irradiances can be observed in Figures 2.2 and 2.3 (Villalva et al., 2009). It is shown that with the increase of irradiance both voltage and current generated are increased. However, the increase of current is more significant compared to the increase in voltage.

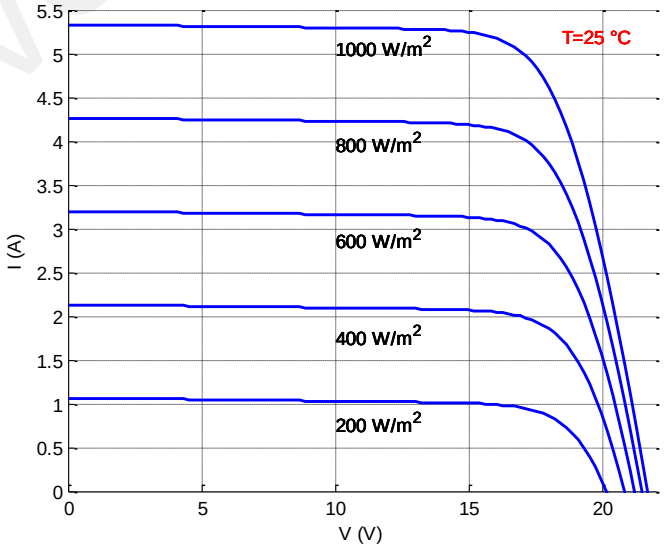


Figure 2.2: I-V curve of during variations in irradiance

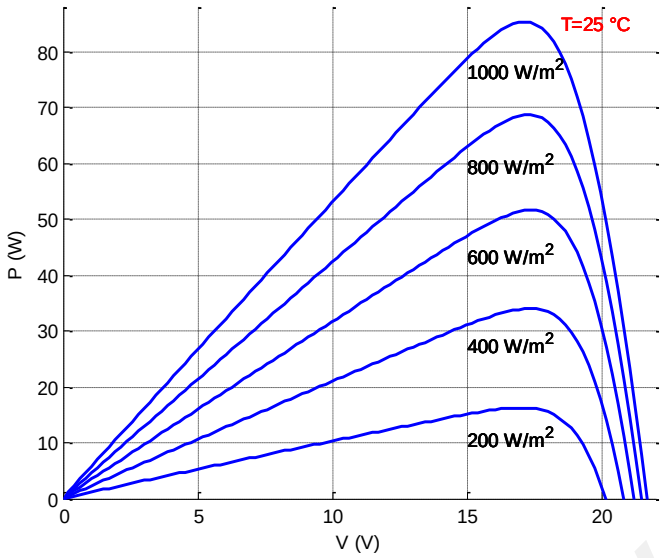


Figure 2.3: P-V curve during variations in irradiance

The MPPT efficiency can be determined as:

$$\eta_{mppt} = \frac{P_o}{P_{mpp}} \tag{2.8}$$

where P_o remains the delivered output-power and P_{mpp} remains the theoretical power determined at MPP voltage.

The MPP circuit equation can be expressed as:

$$I_{mp} = I_{pv} - I_0 \left[exp\left(\frac{V_{mp}+I_{mp}R_s}{aV_T}\right) - 1 \right] - \frac{V_{mp}+I_{mp}R_s}{R_{sh}} \tag{2.9}$$

In addition, Power at MPP circuit equation can be written as:

$$-\frac{I_{mp}}{V_{mp}} = -\frac{I_0}{aV_T}\left(1 - \frac{I_{mp}}{V_{mp}}R_s\right)\left[exp\left(\frac{V_{mp}+I_{mp}R_s}{aV_T}\right)\right] - \frac{1}{R_{sh}}\left(1 - \frac{I_{mp}}{V_{mp}}R_s\right) \tag{2.10}$$

2.3 Maximum Power Point Tracking (MPPT)

PV panel has a non-linear output current and voltage. Apart from sun tracking, which is done electromechanically, for extracting maximum power from solar panel, MPPT is introduced. It is a technique which adjusts operating point of the solar panel to operate at

the MPP at all-time regardless of changes in atmospheric condition (A. Amir et al., 2016). Without MPPT, the operating point of solar panels depends on intersection of the load line and solar panels' characteristic curve as seen in Figure 2.4. Here, most of the PV panel power is wasted as the operating point is below the MPP. In addition, solar irradiance is unpredictable and varies throughout the day, so the PV system is always over-sizing between load and power source to provide a reliable system during bad weathers.

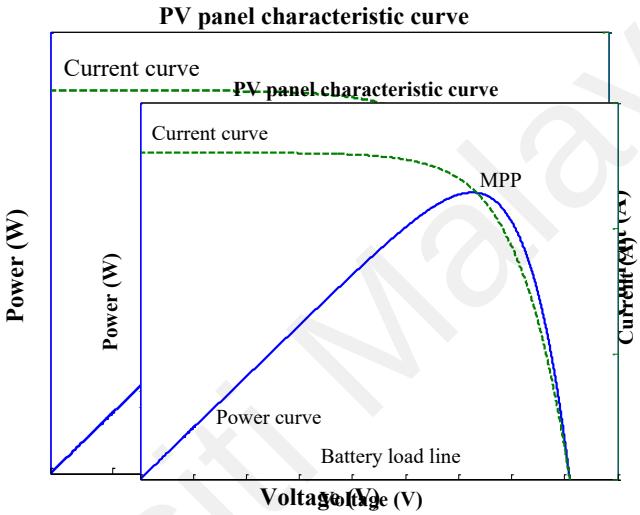


Figure 2.4: Intersection between battery load line and I-V curve of a PV panel

In order to adjust the operation of the PV panel at its MPP for all the times. MPPT is usually administered using a power converter as an intermediate device. There are numerous types of MPPT techniques with analog and digital implementation. Therefore, to critically analyze MPPT techniques found in present literature, analog and digital classification is considered the effective manner to present such techniques.

Every MPPT technique employed offers certain pros and cons. Generally, P&O and INC are the mostly widely reported MPPT techniques (A. Amir et al., 2016). P&O is slow in rapidly changing conditions and confronts a problem of oscillations around the MPP. In addition, methods with simpler implementation are less accurate as the Fractional Voc and Isc. Soft computing techniques are fast and efficient, but require expensive

implementation. Moreover, artificial intelligent techniques require pre-estimated values. Further, INC technique even after GMPPT modification confronts problem of slow tracking and less efficiency as these techniques become insufficient, when large PV strings are employed. Numerical Method techniques address most of the above mentioned shortcomings, as this scheme offers an iterative approach along with speed, accuracy, stand-alone application, feasible circuitry involved, no steady state oscillations, adjustability with rapid changing atmospheric conditions, does not require pre-estimated value for operation and PV array independence.

2.3.1 Digital Techniques

2.3.1.1 Newton-Raphson method (NRM)

Speed and open bracket limits remain the important traits of the NRM (Kreyszig, 2010). In order to track the MPP researchers have used NRM in (Chun & Kwasinski, 2011a; W. Xiao, Lind, Dunford, & Capel, 2006). Figure 2.5 displays the fundamental operation of the NRM (A. Amir et al., 2016). In addition, Figure 2.6 displays the MPPT operation by NRM.

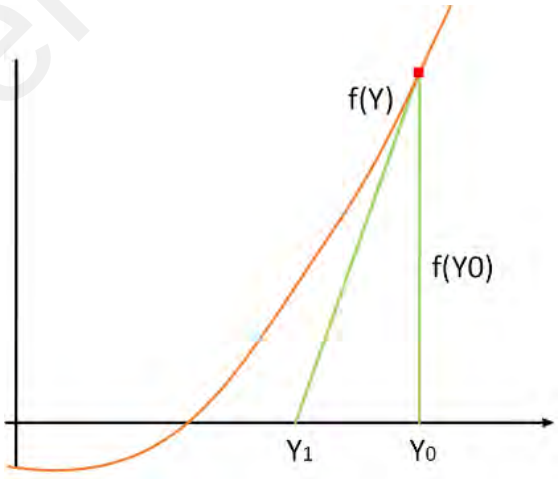


Figure 2.5: Basic Principle of NRM

NR method utilizes equation (2.11) for MPP tracking:

$$Y_1 = Y_0 - \frac{f(Y_0)}{f`(Y_0)} \tag{2.11}$$

Further iterations utilize equations (2.12):

$$Y_{n+1} = Y_n - \frac{f(Y_n)}{f`(Y_n)} \tag{2.12}$$

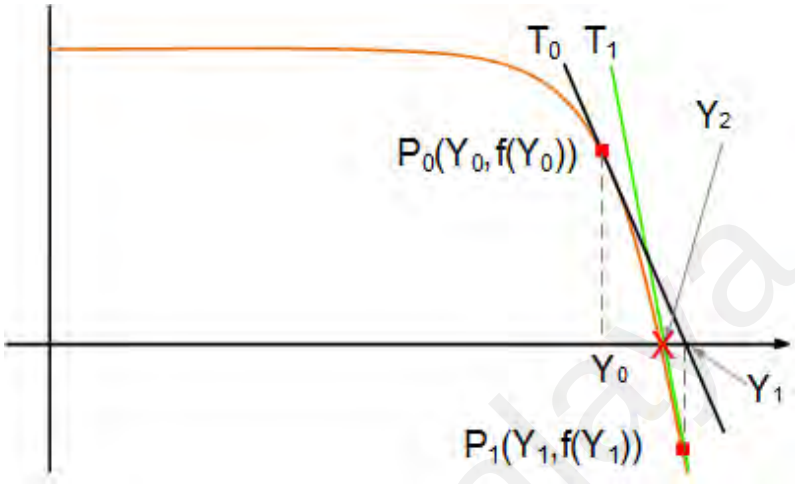


Figure 2.6: MPPT by NRM

2.3.1.2 The secant method (SM)

For MPPT, researchers have employed SM in (J Ma et al., 2013). Figure 2.7 displays the fundamental operation of the SM (A. Amir et al., 2016).

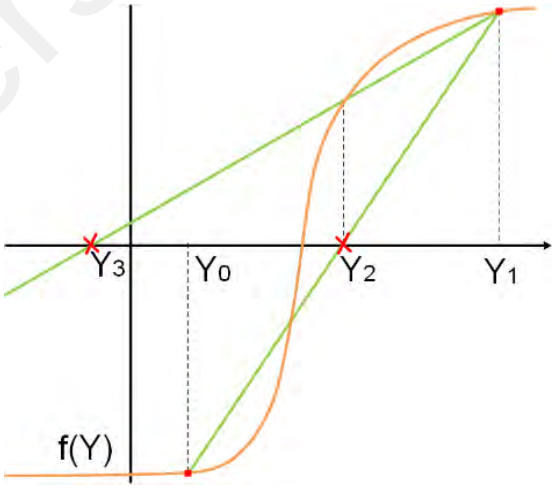


Figure 2.7: Basic Principle of SM

For successive iterations the SM employs the following equation (2.13):

$$Y_n = Y_{n-1} - f(Y_{n-1})\frac{(Y_{n-1})-(Y_{n-2})}{f(Y_{n-1})-f(Y_{n-2})} \tag{2.13}$$

Here, Y remains the input voltage, $f(Y) = \frac{dP}{dV}$ and n the iterations. Figure 2.8 the SM to track the MPP.

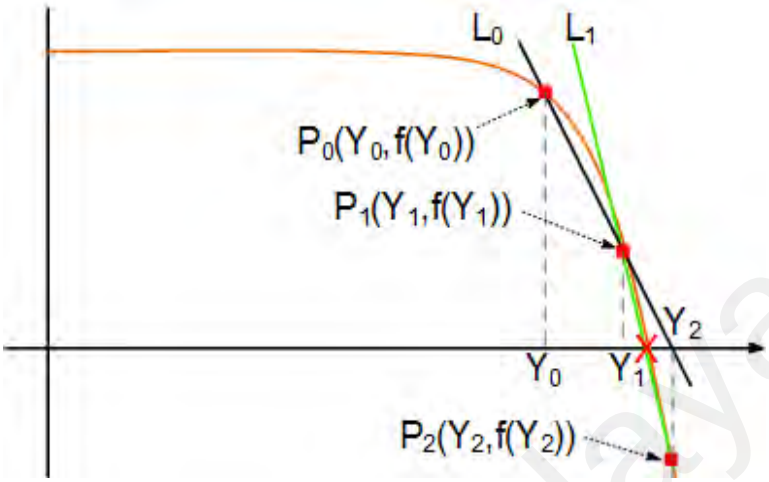


Figure 2.8: MPPT by SM

2.3.1.3 Bisection search method (BSM)

For MPPT, researchers have employed BSM in (Jieming Ma et al., 2013; Prianandа & Haikal, 2014; P. Wang et al., 2010). It is an efficient and simple method to implement. Figure 2.9 offers the fundamental operation of the close bracket technique.

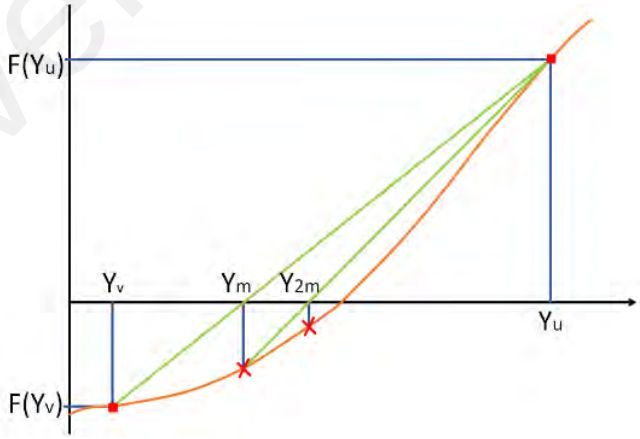


Figure 2.9: Basic Principle of BSM

The close bracket limits are denoted by Y_v and Y_u:

$$Y_{nm} = \frac{u+v}{2} \tag{2.14}$$

Here, the sign of the function deduces the direction of operation satisfying $f(Y_v)f(Y_u) < 0$. Figure 2.10 displays the MPP tracking by employing the BSM (A. Amir et al., 2016).

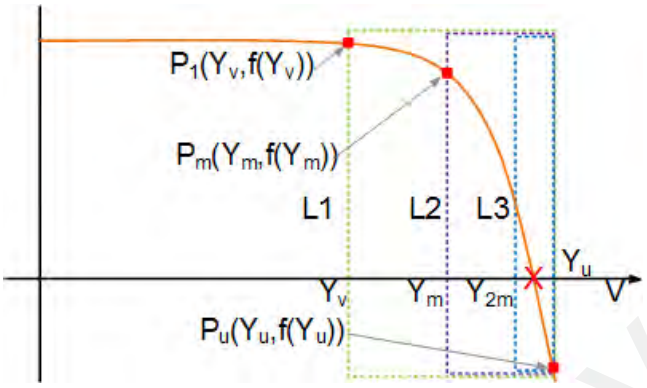


Figure 2.10: MPP tracking by BSM

2.3.1.4 The central point iterative method (CPIM)

For MPPT, researchers have utilized the CPIM in (Zhang et al., 2014). Here, for the iterative process, three points are required which are attained by quantifying a quad numbered non-overlapping intervals from control parameters. Here, iterative process is displayed in Figure 2.11.

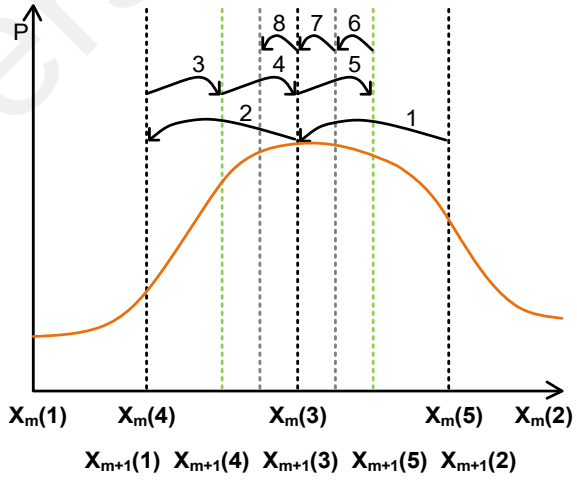


Figure 2.11: MPP tracking by CPI

Flowchart for CPI is given in Figure 2.12.

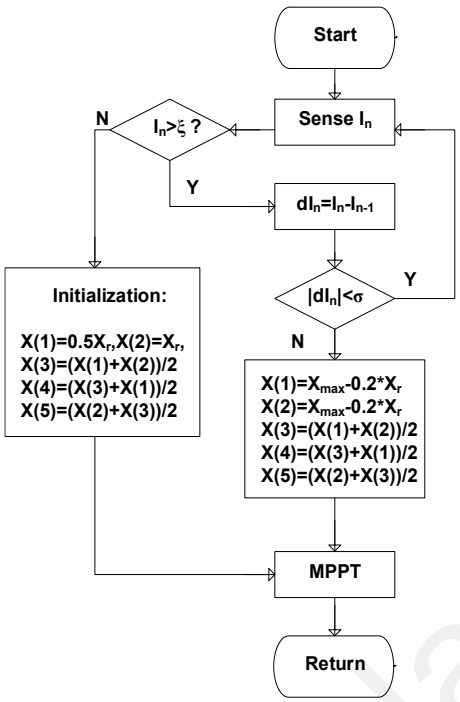


Figure 2.12: CPI Flowchart

2.3.1.5 False position method (FPM)

For tracking the MPP, FPM has been used in (Chun & Kwasinski, 2011a, 2011b). It remains a close bracket technique; its fundamental operation is displayed in Figure 2.13.

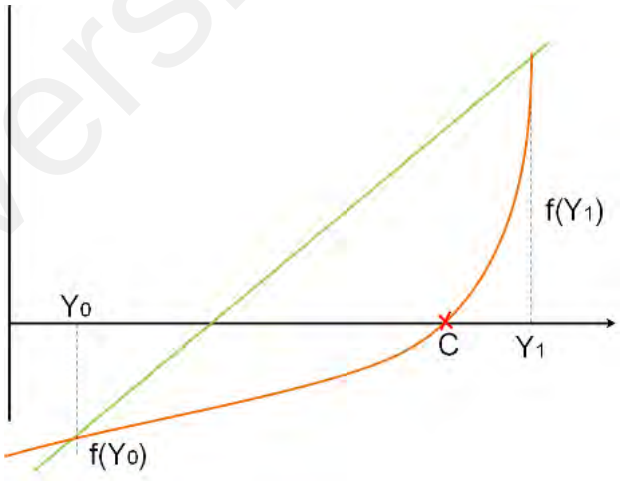


Figure 2.13: Basic Principle of FPM

Its operation is similar to BSM, however, it uses equation (2.15) for its operation:

$$C_{n+1} = \frac{Y_{n-1}f(Y_n) - Y_n f(Y_{n-1})}{f(Y_n) - f(Y_{n-1})} \tag{2.15}$$

To track the MPP, graphical representation for the FPM is presented in Figure 2.14.

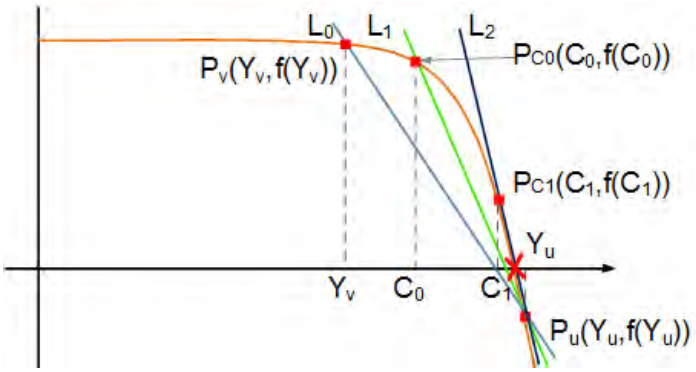


Figure 2.14: MPP tracking with FPM

2.3.1.6 Firefly algorithm (FA)

An optimization technique inspired by light illuminating flies, has been utilized to track the MPP (Sundareswaran, Peddapati, & Palani, 2014).

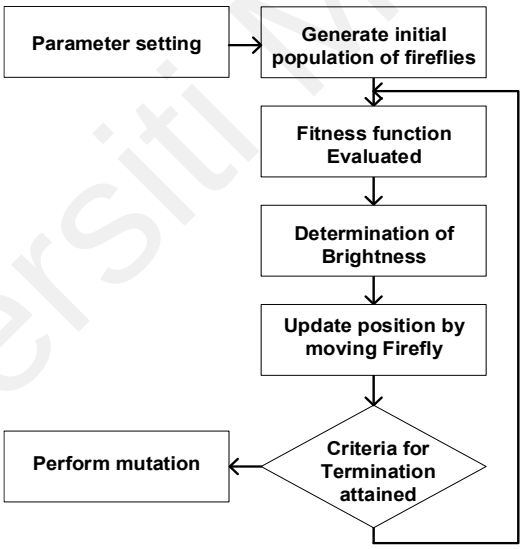


Figure 2.15: Flowchart of FA

To track the MPP firefly uses equation (2.16):

$$X_p^{t+1} = X_p^t + \beta(r)\left(X_p - X_q\right) + \left(rand - \frac{1}{2}\right) \tag{2.16}$$

Here, p and q remain the two fireflies, and their positions are represented by X_p & X_q. Figure 2.15 presents the flowchart of the firefly algorithm.

2.3.1.7 Predictor method (PM)

The PM is slightly different in its operation from the Numerical Interpolation technique (Pai & Chao, 2010; Pai, Chao, Ko, & Lee, 2011).

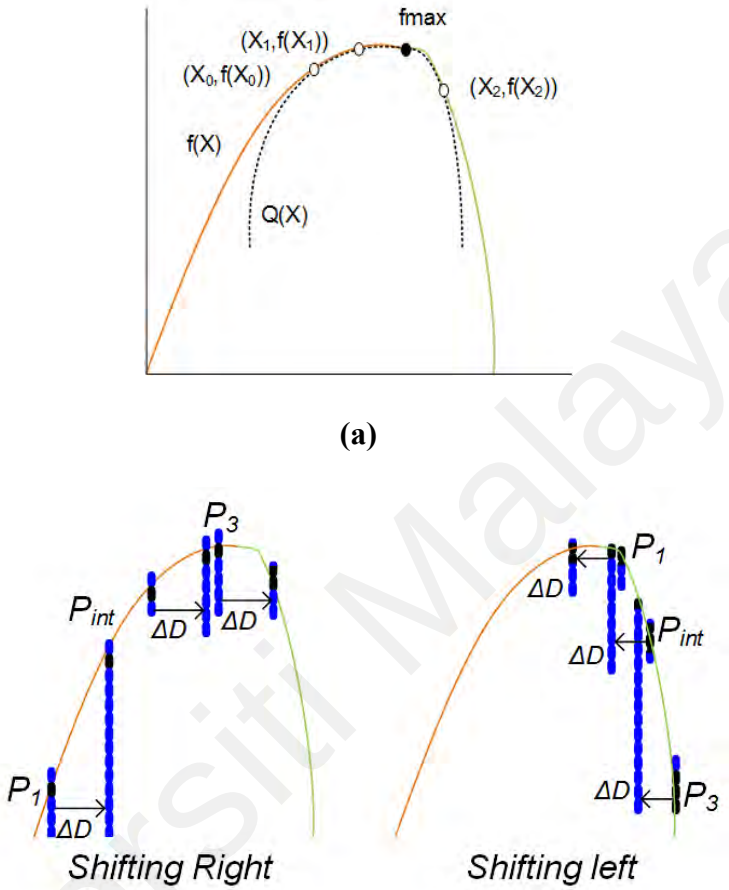


Figure 2.16: (a) MPP tracking by PM (b) MPP tracking by right and left shift employed by PM

As parabolic function, which is parametrically controlled, Q(X) as is used to approximate the root as presented in equation (2.17):

$$Q(X) = aX^2 + bX + c \tag{2.17}$$

Figure 2.16 presents the fundamental operation in predicting the three point to attain the objective function as:

$$Q(X) = f(X_0)\frac{(X-X_1)(X-X_2)}{\Delta X_{01}\Delta X_{02}} + f(X_1)\frac{(X-X_0)(X-X_2)}{\Delta X_{10}\Delta X_{12}} +$$

$$f(X_2)\frac{(X-X_0)(X-X_1)}{\Delta X_{20}\Delta X_{21}} \quad (2.18)$$

2.3.1.8 Ant colony optimization (ACO)

Here the tracking of the MPP is represented by the path followed by an individual ant, the pheromone laid by the ant for food represents the positive feedback for direction of the MPP and the food remains the MPP (Dorigo, Maniezzo, & Colorni, 1996). Greater the pheromone density, more the ant follows the path. Figure 2.17 (a & b) shows the ACO working principle (Logeswaran & SenthilKumar, 2014).

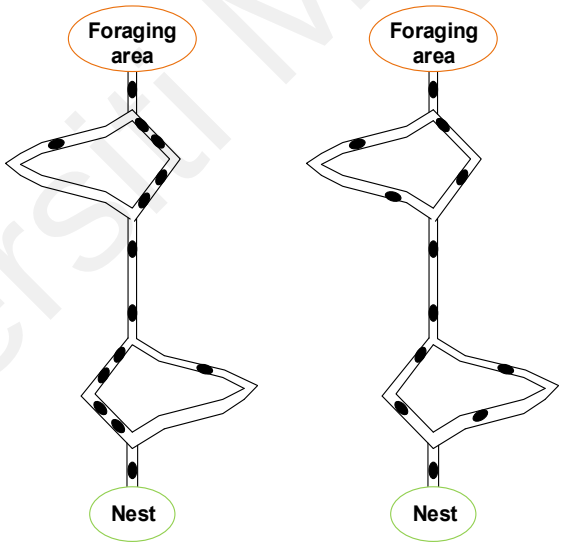


Figure 2.17: (a) Ant following the shortest path (b) Following a random path

For MPP the ACO utilizes equation (2.19):

$$\frac{|I(s_{i+1}) - I(s_i)|}{I(s_i)} > \Delta I \quad (2.19)$$

2.3.1.9 Neural network (NN)

Through a probabilistic control and intelligent training, NN possesses the capacity to optimize a certain parameter. Such an algorithm can involve more than one layer or hidden layers for optimization as presented in Figure 2.18. The atmospheric temperature, irradiance conditions Voc and Isc can be treated as input parameters. The weighted linkage are adjusted in the training process to finally attain an output signal to track the MPP (Sun et al., 2017). However, such a process requires pre-conceived information for the Neural System. NN maybe a complex technique, yet it can be implemented in a cost effective fashion (Yang, 2011).

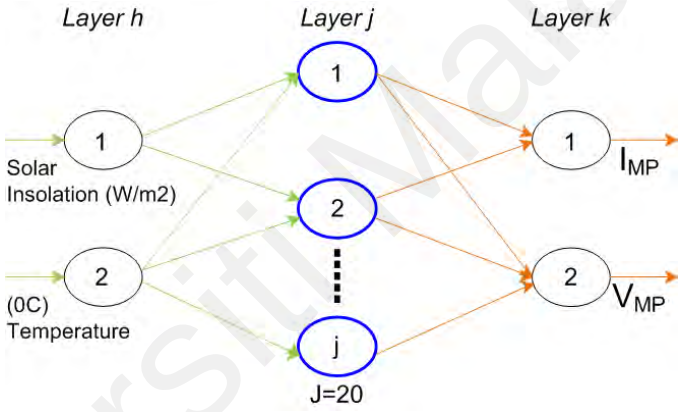


Figure 2.18: MPP tracking employing the NN technique

2.3.1.10 Fuzzy logic (FL)

For intelligent computation the FL employs the fuzzification and defuzzification stages (El Khateb, Rahim, Selvaraj, & Uddin, 2014). Fuzzification stage is employed, as presented in Figure 2.19, to attain linguistic notations from various input parameters, depending on membership function. Here, the input parameters are considered to be error (E) and the differential error (ΔE). In addition, Table 2.1 presents a rule base which is employed in between the two stages to optimize the required output. Where, e is the error, NB the negative big, NS the negative small, ZE the zero error, PS the positive small and PB the positive big (Mamdani & Assilian, 1975).

Table 2.1: Look-up table for rule base

Δe \ e	NB	NS	ZE	PS	PB
NB	ZE	ZE	NB	NB	NB
NS	ZE	ZE	NS	NS	NS
ZE	NS	ZE	ZE	ZE	PS
PS	PS	PS	PS	ZE	ZE
PB	PB	PB	PB	ZE	ZE

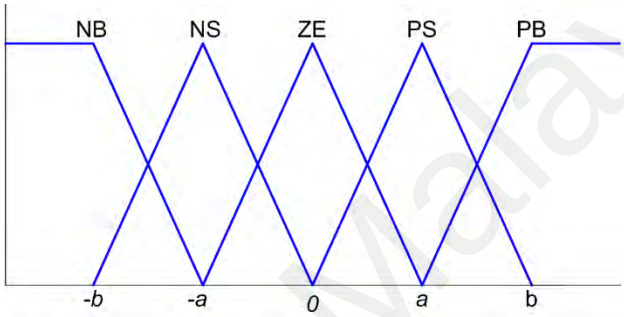


Figure 2.19: FL membership function

2.3.1.11 Hill-climbing (HC) techniques

Researchers had proposed the earliest incremental conductance (INC) technique for MPPT operation in (Wasynezuk, 1983). To compute dI/dV, harmonic component of the PV array was used offering analog operation. However, (Hussein, Muta, Hoshino, & Osakada, 1995) utilized perturbations to compute dI/dV term utilizing it digitally. Both the techniques are widely employed digitally (Soren Baekhoj Kjaer, 2012; K. Lee, Fujii, Sumiya, & Ikawa, 2010).

Considered parameter for MPPT, remains the change in power, for perturb and observe (P&O). For P&O, subsequent perturbation in output control signal of the MPPT would be in a similar direction to reach the MPP, if increase in power is detected and the algorithm would choose an opposite path, if the decrease in power is identified. This method can be implemented in a direct or an indirect fashion. As presented in (E. M.

Ahmed & Shoyama, 2010). Figure 2.20 displays a flowchart of the direct control operation of the P&O method and Figure 2.21 for INC.

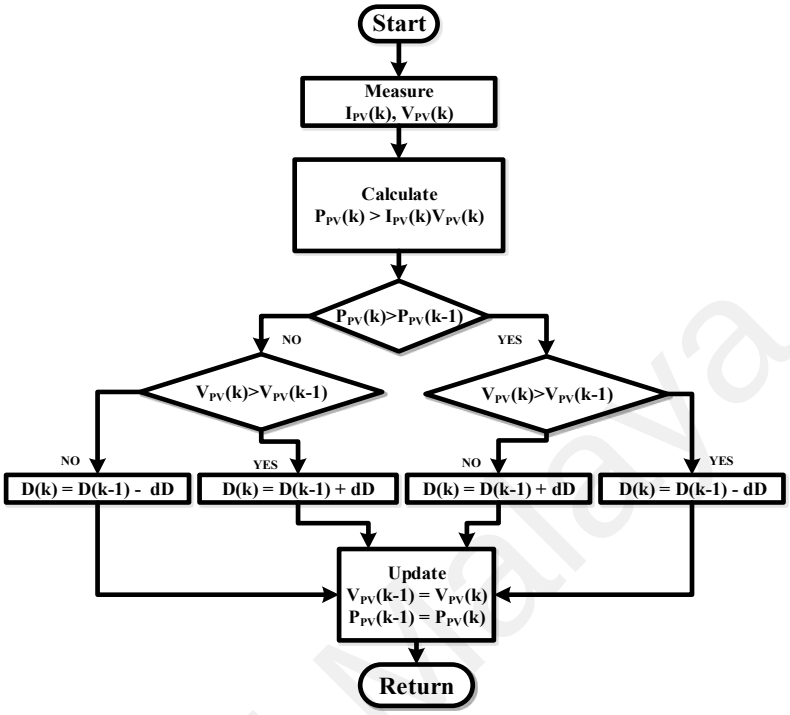


Figure 2.20: Direct control P&O method flowchart

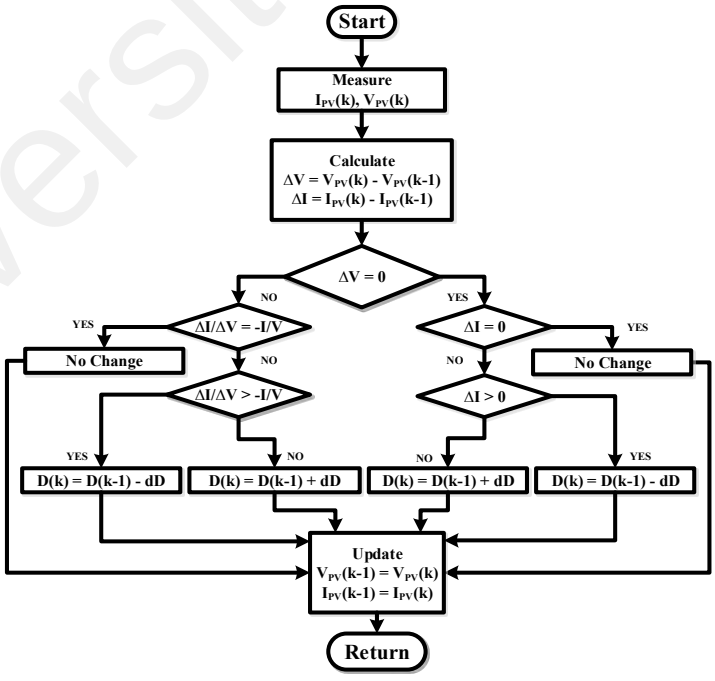


Figure 2.21: Direct control INC method flowchart

For INC method the requisite modifications are as follows (Safari & Mekhilef, 2011). The algorithms tracks the MPP by satisfying the following conditions:

$$\frac{\Delta P}{\Delta V} = 0 \qquad \text{MPP} \tag{2.20}$$

$$\frac{\Delta P}{\Delta V} > 0 \qquad \text{L of MPP} \tag{2.21}$$

$$\frac{\Delta P}{\Delta V} < 0 \qquad \text{R of MPP} \tag{2.22}$$

As,

$$\frac{\Delta P}{\Delta V} = \frac{\Delta(IV)}{\Delta V} = I + V\frac{\Delta I}{\Delta V} \cong I + V\frac{\Delta I}{\Delta V}$$

So,

$$\frac{\Delta I}{\Delta V} = -\frac{I}{V} \qquad \text{MPP} \tag{2.23}$$

$$\frac{\Delta I}{\Delta V} > -\frac{I}{V} \qquad \text{L of MPP} \tag{2.24}$$

$$\frac{\Delta I}{\Delta V} < -\frac{I}{V} \qquad \text{R of MPP} \tag{2.25}$$

L is Left and R is considered as Right of MPP. Here, INC is treated as a specific implementation of the P & O (Sera, Mathe, Kerekes, Spataru, & Teodorescu, 2013). In addition, both techniques are considered as HC techniques (Esram & Chapman, 2007).

2.3.2 Analog Techniques

2.3.2.1 Ripple correlation control (RCC)

RCC is PV array independent and its operational principle is underlined in (Krein, 1999; Midya, Krein, Turnbull, Reppa, & Kimball, 1996). It utilizes the current and voltage ripples to track the MPP. Such oscillations offer data on the power gradient which is further assessed for attaining MPP. As reported it is PV array independent, so it does

not required artificial perturbation to assess the gradient value (Casadei, Grandi, & Rossi, 2006; Esram, Kimball, Krein, Chapman, & Midya, 2006; Giustiniani, Petrone, Spagnuolo, & Vitelli, 2010; Kimball & Krein, 2008; Logue & Krein, 2001).

2.3.2.2 System oscillation technique (SOT)

Here a tracker control is utilized to offer self-oscillations, which in turn modifies the control signal for the main switch (Chung, Tse, Hui, Mok, & Ho, 2003; Ho, Chung, & Lo, 2004). To attain the quiescent duty cycle for converter's main switch, mean of the input voltage is compared with the ac component. For global MPP tracking it remains one of the finest approach (Ho et al., 2004).

2.3.3 Hybrid Techniques

2.3.3.1 Droop control MPPT (DCL) DC-link capacitor

DCL has been categorized hybrid the reported research presents a few analogue operational amplifiers for building the logic circuits for decision-making and the duty factor command remains digital (Matsui, Kitano, Xu, & Yang, 1999). Figure 2.22 represents the principle operation of the algorithm. For DCL if the d of the chopper attains the highest values I_{peak}^{*} only then the MPP is attained. However, P_{max} is higher, the DC Link voltage V_{link} decays. Notation of "DROOP" signifies such a rapid decay in DC Link voltage. It's operation is restricted to AC systems line with parallel connection (Kitano, Matsui, & Xu, 2001). The command factor (d) or duty is determined by:

$$d = 1 - \frac{V}{V_{link}} \tag{2.26}$$

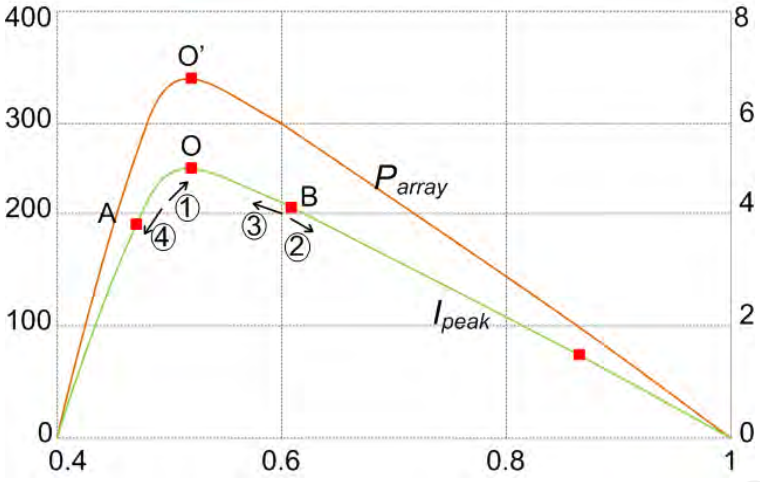


Figure 2.22: MPPT by DCL

2.3.3.2 Fractional V_{oc} and I_{sc} (FVI)

A direct proportionality exists between the Voltage at the MPP (V_{mpp}) and Open Circuit voltage (V_{oc}) as observed on the V-I characteristics (Subudhi & Pradhan, 2011):

$$V_{mpp} = K_{oc} V_{oc} \tag{2.27}$$

This technique utilizes equation (2.27) for tracking the MPP, it remains simple, inexpensive and easy to implement. But, at partial shading the constant K remains invalid and cannot offer exact MPP. In addition, current at MPP (I_{mpp}) and Short Circuit current *(Isc)* are also directly proportional, which is utilized by the Fractional Current method as presented in equation (2.28) (Masoum, Dehbonei, & Fuchs, 2002; Subudhi & Pradhan, 2011):

$$I_{mpp} = K_{sc} I_{sc} \tag{2.28}$$

Figure 2.23 summarizes the MPPT techniques under discussion.

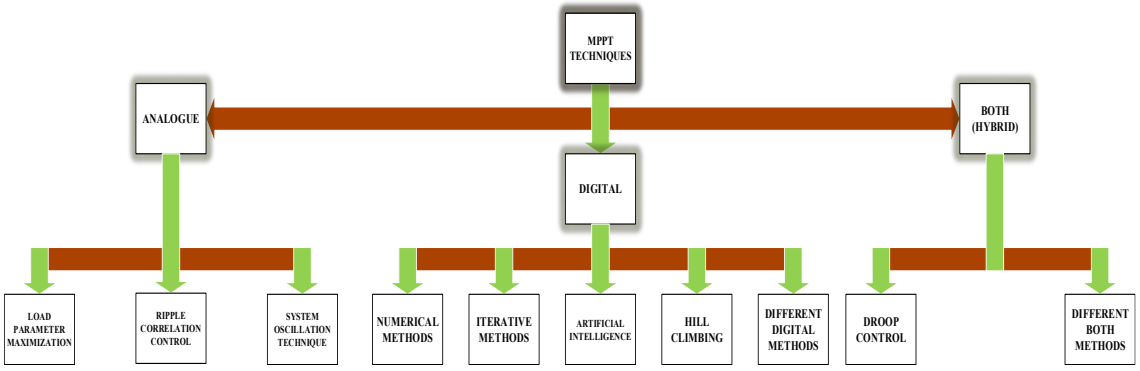


Figure 2.23: MPPT Classification

2.4 Power Converter Topologies

Number of MPPT techniques from those presented above, particularly the mINC approach had been applied to several power converter topologies (Aamir Amir et al., 2017; Asim Amir, Che, Amir, El Khateb, & Rahim, 2018). Comprehending that the output voltage generated by the PV panels can be transformed into a higher or lower voltage by the application of power converters. As intermediate devices such power converters are utilized to convert power generated from solar panels to desirable DC power level. There are several tasks of power converters in solar system application which are i) interface the PV panels with grid or load for DC loads, ii) adjust the operating point of PV panels to extract maximum power to use together with MPPT algorithm and iii) implement charging control ensuring that the battery undergoes healthy charging routine. When the electrical loads are DC, in order to extract maximum energy form PV panels a DC-DC converter is needed, along with a MPPT algorithm, whereas when electrical loads are AC, an inverter is also required because the PV power generated is DC.

2.4.1 DC-DC Converters

Power converters have been divided into two main blocks namely isolated (IS) and non-isolated (NIS) converter design topologies. With IS an electrical barrier is placed between the output and input of the DC-DC converter (so, only IS converters have a barrier placed, while NIS converters have no such galvanic isolation). A high-frequency transformer isolates the input side and the output side of an IS converter. IS converters

normally utilize a transformer while NIS converters usually comprise of different topologies.

Buck converter (Cho, Kim, & Kim, 2018), boost converter (Knecht, Bortis, & Kolar, 2018), buck-boost converter (Ramírez-Murillo et al., 2018), Cuk converter (Ananthapadmanabha, Maurya, & Arya, 2018), and single-ended primary inductance converter (SEPIC) (Moradpour, Ardi, & Tavakoli, 2018) are considered the five main topologies of the NIS converters. A very large output-voltage ripple and a linkage between input and output, are the primary problems of such converters (Singha & Kapat, 2018).

Buck converter is the simplest topology of the NIS power converters and is widely used in power electronic application, the schematic diagram of the Buck Converter has been presented in Figure 2.24. It is a stepdown NIS converter. Its operation is restricted in the first quadrant.

For Buck Converter with direct implementation of DMPPT, the effective resistance can be realized as,

$$R_{pv} = \frac{V_{pv}}{I_{pv}} = \frac{R}{D^2} \tag{2.29}$$

Convergence rate of V_{pv} can be attained as

$$\frac{\Delta V_{pv}}{\Delta D} = -\frac{2K}{D^3} \tag{2.30}$$

As observed from equation (2.30), the change in voltage for the Buck Converter establishes an inverse proportionality with duty cycle. Hence, the direction of convergence for the input voltage and duty cycle (D) remains opposite. As D is slightly

reduced a small change in voltage is observed. But, as D continues to decrease the change increases. Its output is:

$$V_o = \frac{t_{on}}{T} V_{in} = DV_{in} \tag{2.31}$$

Where, T remains repeating period $\left(T = {}^{1}/_{f}\right), f$ the chopping frequncy, t_{on} switch-on time and D the conduction duty cycle ($D = {}^{t_{on}}/_{T}$).

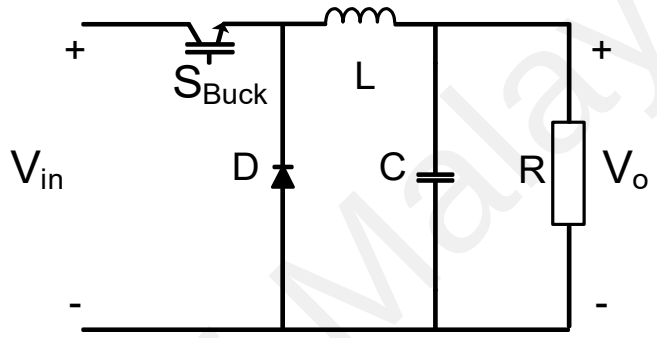


Figure 2.24: Schematic diagram of the Buck Converter

Boost converter remains a step-up NIS converter. The schematic diagram of the Boost converter has been presented in Figure 2.25. Its operation is restricted to the second quadrant. The effective resistance seen by the source for the boost converter can be presented as:

$$R_{pv} = \frac{V_{pv}}{I_{pv}} = R(1-D)^2 \tag{2.32}$$

As this region of operation can be considered as the constant current region so:

$$V_{pv} = R(1-D)^2 I_{sc} = k(1-D)^2 \tag{2.33}$$

where, $RI_{sc} = k$

Convergence rate of V_{pv} can be attained as

$$\frac{\Delta V_{pv}}{\Delta D} = (2D - 2)k = 2(D - 1)k \tag{2.34}$$

As observed from equation (2.34), the change in voltage for Boost converter establishes a direct proportionality with duty cycle. Hence, the direction of convergence for both the input voltage and duty cycle remains same. As D is slightly reduced a considerable change in voltage is observed. But, as D continues to decrease the change lessens. Its output voltage is:

$$V_o = \frac{T}{T - t_{on}} V_{in} = \frac{1}{1 - D} V_{in} \tag{2.35}$$

Where, f the chopping frequency, D the conduction duty cycle ($D = {t_{on}}/{T}$).

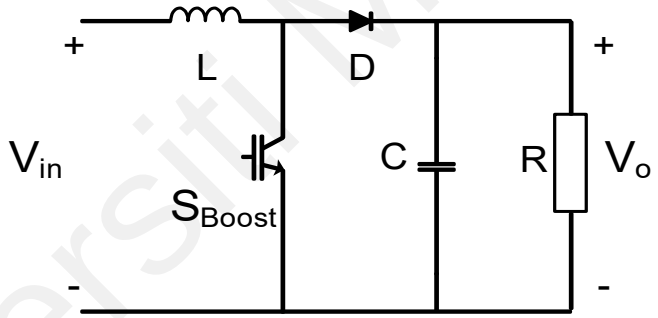


Figure 2.25: Schematic diagram of the boost converter

Buck-Boost converter remains a step-up/step-down converter topology. Its schematic diagram has been presented in Figure 2.26. Buck-boost converter offers flexible performance as output voltage is flexible for modification to higher or lower voltage in comparison with the input voltage. Drawback remains the inverse polarity of output-voltage. Its operation is restricted to the third quadrant. V_o can be determined by:

$$V_o = \frac{t_{on}}{T - t_{on}} V_{in} = \frac{D}{1 - D} V_{in} \tag{2.36}$$

Where, f the chopping frequncy, and D the conduction duty cycle ($D = {t_{on}}/{T}$).

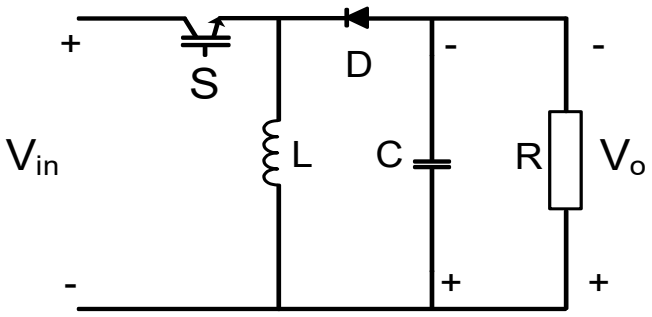


Figure 2.26: Schematic diagram of the Buck-Boost Converter

Cuk converter and SEPIC converters are attained by adding a low-pass filter to the boost converter. Figures 2.27 & 2.28 present the schematic diagrams of the Cuk and SEPIC circuits, respectively.

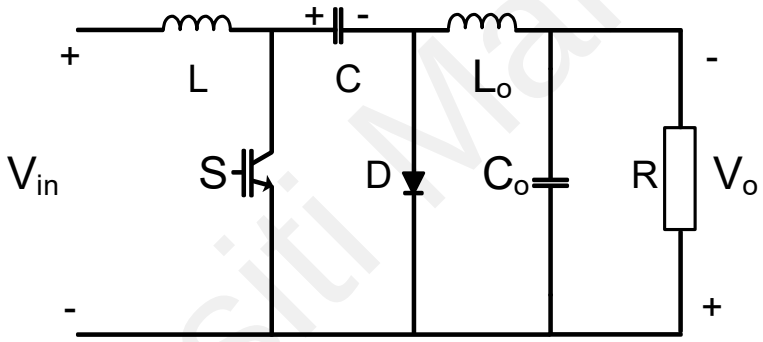


Figure 2.27: Schematic diagram of the Cuk Converter

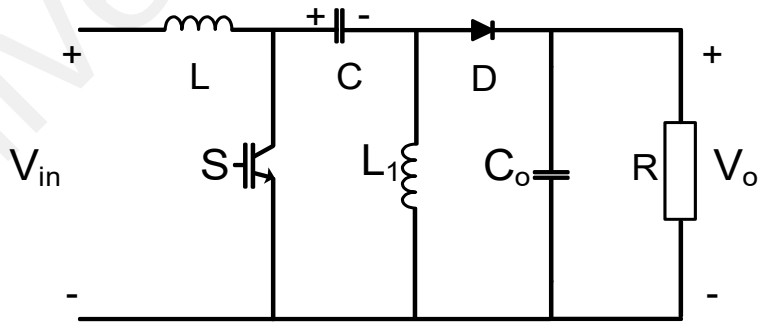


Figure 2.28: Schematic diagram of the SEPIC Converter

SEPIC offers an adjustability in output range of the converter with similar polarity but its low efficiency is the drawback of this converter topology (Singha et al., 2018). The output voltage is:

$$V_o = \frac{D}{1-D} V_{in} \tag{2.37}$$

2.4.2 DMPPT Implementation on Various DC-DC Converter Topologies

Considering direct control MPPT techniques, duty cycle (D) is taken as the main control variable. Therefore, performances of DMPPT techniques with direct control, show a trade-off between the transient response and the steady state error. Here, the primary issue remains that a constant voltage change is never guaranteed with a constant step size change in duty cycle.

A PV system can employ various Dc-Dc converter topologies. Here, the focus remains on the Buck Converter (Divakar & Sutanto, 1999) and Boost converter. In case of a PV system employing the Buck Converter, at operating points away from the MPP the system shows smaller steady state oscillations (Aamir Amir et al., 2017), as a constant step change offers small change in voltage, however, at operating points closer to MPP large steady state response is observed, as the constant step change offers large change in voltage. For Boost converter the conditions are entirely opposite to the ones observed for Buck Converter.

2.4.2.1 Change in voltage for duty cycle closer to MPP

Equations (2.30) and (2.31) present the change in voltage for high duty cycle on Buck Converter. In addition, equations (2.33) and (2.34) present the change in voltage for high duty cycle on Boost converter. For the case where the change in voltage for D is closer to MPP, behavior of the stated converters can be modeled as:

For Boost Converter

As it is evident that

$$\frac{\Delta P_{pv}}{\Delta D} = \frac{\Delta I_{pv} V_{pv}}{\Delta D} - \frac{I_{pv} \Delta V_{pv}}{\Delta D} \tag{2.38}$$

At MPP:

$$\frac{\Delta P_{pv}}{\Delta D} = 0 \tag{2.39}$$

Therefore,

$$0 = \frac{\Delta I_{pv} V_{pv}}{\Delta D} - \frac{I_{pv} \Delta V_{pv}}{\Delta D} \tag{2.40}$$

Change in voltage for duty cycle closer to MPP can be ascertained by,

$$I_{pv} = \frac{1}{R(1-D)^2} V_{pv} \tag{2.41}$$

Differentiating with respect to D

$$\frac{\Delta I_{pv}}{\Delta D} = \frac{1}{R}\left[\frac{(1-D)^2 \frac{\Delta V_{pv}}{\Delta D} - (-2+2D)V_{pv}}{(1-D)^4}\right] \tag{2.42}$$

Substituting we get,

$$V_{pv}\left(\frac{1}{R}\left[\frac{(1-D)^2 \frac{\Delta V_{pv}}{\Delta D} - (-2+2D)V_{pv}}{(1-D)^4}\right]\right) + \frac{I_{pv} \Delta V_{pv}}{\Delta D} = 0 \tag{2.43}$$

Further,

$$\frac{\Delta V_{pv}}{\Delta D} = \frac{(-2+2D)V_{pv}^2}{(\frac{V_{pv}}{(1-D)^2} + R I_{pv})(1-D)^4} \tag{2.44}$$

At MPP,

$$\frac{\Delta V_{pv}}{\Delta D} = \frac{(-2+2D)V_{MPP}^2}{(\frac{V_{MPP}}{(1-D)^2} + R I_{MPP})(1-D)^4} \tag{2.45}$$

Substituting we get,

$$\frac{\Delta V_{pv}}{\Delta D} = \frac{(-2+2D)V_{MPP}^2}{2V_{MPP}(1-D)^2} \tag{2.46}$$

$$\frac{\Delta V_{pv}}{\Delta D} = \frac{(D-1)V_{MPP}}{(1-D)^2} \tag{2.47}$$

Here equation (2.47) represents the change of input voltage with respect to the change in duty cycle, once the duty cycle remains closed to the MPP.

For Buck Converter

For Buck Converter the change in voltage with respect to D, closer to MPP can be realized as:

$$\frac{\Delta V_{pv}}{\Delta D} = \frac{-V_{MPP}}{D} \tag{2.48}$$

Considering equations (2.47 and 2.48) it is clear that at MPPT where the change in change in power with respect to change in duty cycle is almost equal to 0, the response of input voltage remains fast for Buck Converter and faster for Boost. As at MPP, D is certainly less than 1 and voltage at MPP is optimum. Hence, the change of voltage for all converters remains large.

2.4.2.2 Change in Voltage for Low Duty Cycle

For Boost Converter

Change in voltage for duty cycle far away from MPP with low D can be ascertained by differentiating equation (2.33),

$$\frac{\Delta V_{pv}}{\Delta D} = R\frac{\Delta}{\Delta D}\left(I_{pv}(1-D)^2\right) = R\left(\frac{\Delta I_{pv}}{\Delta D}(1-D)^2 + (-2+2D)I_{pv}\right) \tag{2.49}$$

Substituting I_{pv} into equation (2.47) we get,

$$\frac{\Delta V_{pv}}{\Delta D} = R\left(\frac{\Delta I_{pv}}{\Delta D}(1-D)^2\right) + \frac{(2D-2)V_{pv}}{(1-D)^2} \tag{2.50}$$

From equation (2.50), the directions of input voltage and the D remain the same, so the change in voltage is essentially positive. Therefore, at low D the change in voltage is high.

For Buck Converter

For Buck Converter the change in voltage with respected to D, at low D can be realized as,

$$\frac{\Delta V_{pv}}{\Delta D} = \frac{\Delta I_{pv}}{\Delta D}\left(\frac{R}{D^2}\right) - \frac{2V_{pv}}{D} \tag{2.51}$$

From equation (2.51), the directions of input voltage and the D remain opposite, so the change in voltage is essentially negative. As the term $\frac{\Delta I_{pv}}{\Delta D}\left(\frac{R}{D^2}\right)$ is smaller than $\frac{2V_{pv}}{D}$. Therefore, at low D the change in voltage is small and negative.

2.4.3 DC-AC Inverter

Power electronic devices that convert DC source to AC source are known as an inverter. Inverters are utilized for various applications. Here the discussion is limited to stand-alone and grid-tied PV systems. As reported earlier the stand-alone PV system is classified into three types. Differences in waveform output voltage (square wave modified square wave, sine wave) mark out three types of stand-alone PV inverters (Kang, Park, Cho, Kim, & Ise, 2005; Xue, Chang, Kjaer, Bordonau, & Shimizu, 2004). Square-wave inverters were the original electronic inverter. Presently, most common circuit topology producing a square-wave output is the push-pull. Square-wave inverters are the least

expensive, but they typically are the least efficient (Cheng, Bhattacharya, & Divan, 1998). A Square-wave output has been displayed in Figure 2.29.

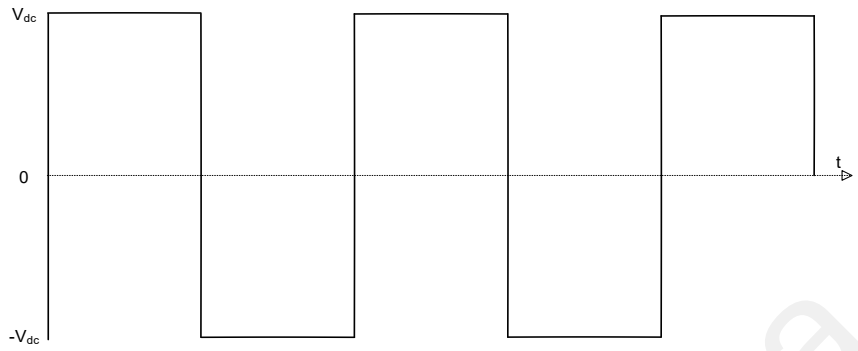


Figure 2.29: Square-wave output voltage

Modified-square-wave inverters produce modified sine-wave outputs. The modified-square-wave includes dead spots between positive and negative half cycles. As switching occurs at the line frequency, such inverters do not need high-frequency switching. The output is not completely sine wave as presented in Figure 2.30.

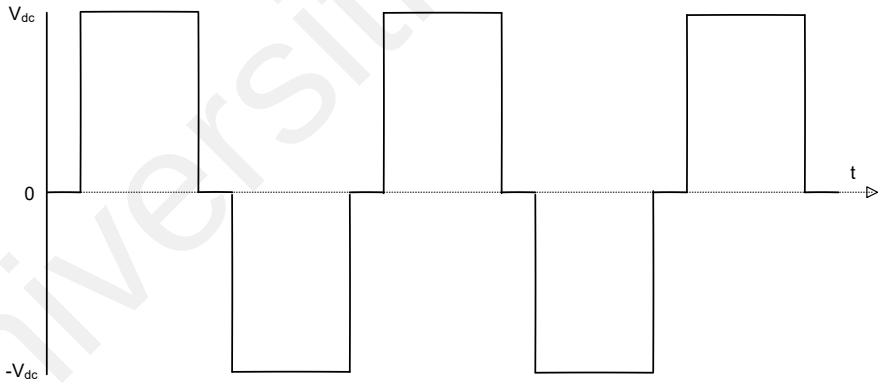


Figure 2.30: Modified-sine wave output voltage

Another way to approximate a sine wave uses high switching frequency at the inverter switches. A reference sine wave is modulated into a triangular wave. A filter is embedded onto the modulated wave, so the output voltage inverter shows a sine wave as of Figure 2.31.

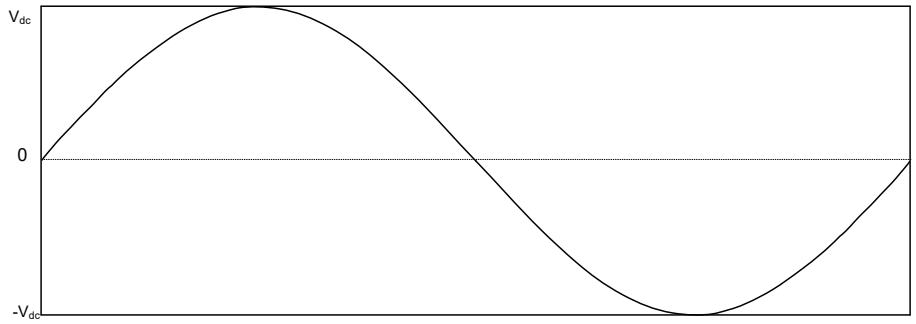


Figure 2.31: Sine-wave output voltage

In addition to stand-alone PV systems, inverters can be used for grid-tied PV systems. The necessity of an inverter in such a system is to offer synchronization with grid in its frequency, phase, and voltage. Output-voltage and current offered by the inverter must be sinusoidal and maintain a unity power factor with the grid. Chapter 3 details the grid-connected PV-system inverter.

2.5 Multilevel Inverter Topologies

Industry and academia have been focusing on Multilevel Inverters (MLI) due to the wide range of merits offered by such topological designs. Advancements in the design of MLI, have transformed it into a viable technology. As, MLI are utilized to attain a higher number of output-voltage levels N_{level}, with lesser semiconductor devices, reduced dv/dt stress, better voltage and current THD waveforms, reduced EMI and size of passive filters.

This chapter also highlights various MLI topologies focusing on the reduced switch MLI constructions by classifying them as asymmetric, symmetric and hybrid topologies. In addition, different modulation techniques and control algorithms for MLI have been presented. Here, the focus is on grid-connected inverters; therefore, a brief over of grid-tied inverters is presented before analyzing the MLI topologies.

2.5.1 Topologies of Single-Phase Grid-Tied Inverter

Single-phase grid-tied inverter topologies have been reviewed in (Blaabjerg & Yang, 2017; Jana, Saha, & Bhattacharya, 2017). Number of power-conversion stages can make classification of grid-connected PV inverters. Where, single-stage inverters, for all the PV power-processing tasks as the voltage boosting, MPPT, and grid-synchronization, present only one power-conversion stage. In contrast, more than one power-conversion stage is required by the multi-stage inverters power-processing tasks. In multistage inverters, the conditioning of the PV power requires a DC-DC converter in order to boost the voltage up to the grid requirements, along with tracking the MPP.

Grid-Tied power systems can be commonly grouped into two categories, namely, with transformer and transformerless. Here, a low-frequency transformer can be employed on the ac side or a high-frequency transformer can be engaged on the dc side (Blaabjerg, Teodorescu, Liserre, & Timbus, 2006). To avoid dc injection into the grid, boost the input voltage to the grid requirements, provide galvanic isolation and leakage current elimination is offer by a transformer in a grid-tied system. However, transformers remain heavy and costly. Therefore, systems without a transformer are employed to reduce the cost and size (Bae & Kim, 2014; H. Xiao, Xie, Chen, & Huang, 2011). Nevertheless, high leakage current remains a major safety challenges. As direct current path can be formulated for current flow from PV to grid. Stray capacitance is introduced, once the PV is grounded. Fluctuations in the stray capacitance, remains the prime reason for the generation of a high leakage current (Y. Wang & Li, 2013). In this thesis, to ensure safety and eliminate leakage current, degradation of PV system by growing grid current ripples, a PV system with transformer has been utilized.

2.5.1.1 Topologies for single-stage inverter

A survey of such topologies has been presented in (Jain & Agarwal, 2007). Caceres and Barbi propose a non-isolated boost inverter topology. Here, each converter is

operated complementarily, and its output is unipolar dc-biased sinusoid. In addition, the Sliding-mode control optimizes the inverter operation (Caceres & Barbi, 1999). Such topologies are not restricted to the boost converter design. An alternative buck-boost inverter by (Kasa, Iida, & Iwamoto, 1999) overcomes the shortcoming of asymmetric operation during the two half cycles of the grid voltage, Figure 2.32 presents the schematic diagram.

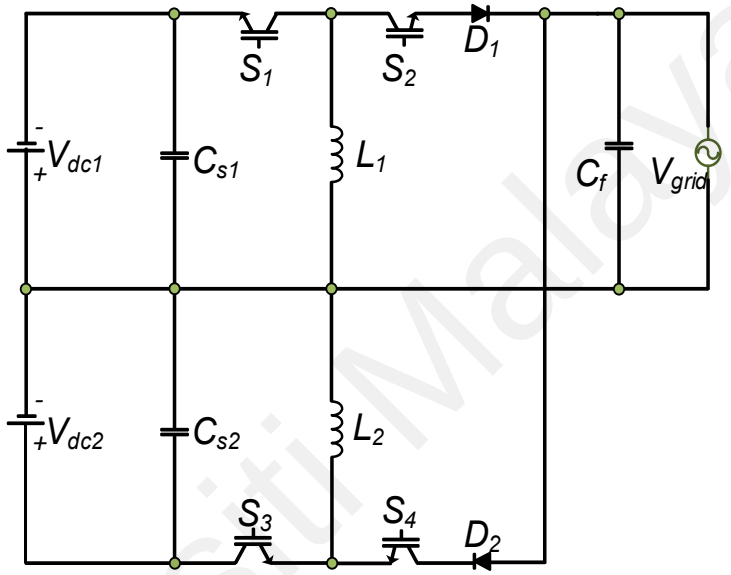


Figure 2.32: Buck-boost inverter

Figure 2.33 presents a buck-boost inverter topology with zero-current-switching (ZCS) proposed by (C.-M. Wang, 2003).

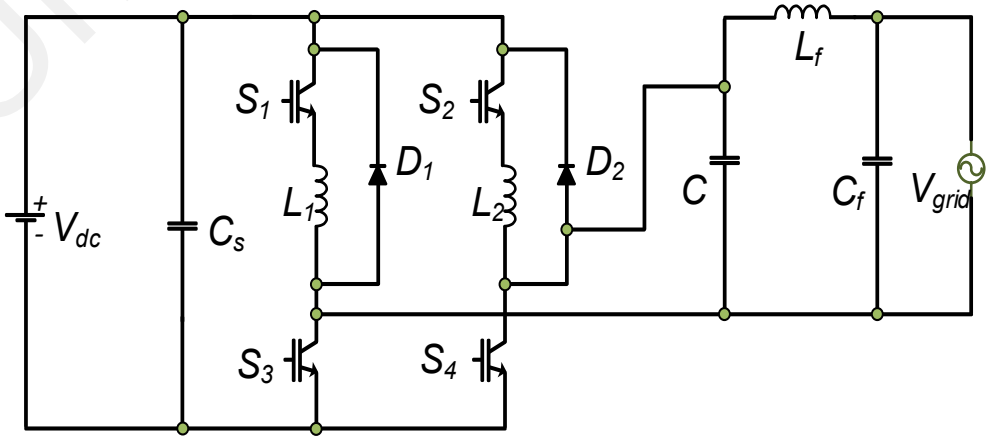


Figure 2.33: Four-switch resonant buck-boost inverter

2.5.1.2 Multi-stage inverter

In a two-stage or multi-stage power inverter, any kind of necessary isolation boosting are performed in the first stage. Here, second stage is restricted for inversion. In addition, all the stages can be monitored and controlled synchronously or individually. In multi-stage, both the boost and buck-boost converters can also be employed.

A two-stage boost inverter has presented in (M. E.-S. Ahmed, Orabi, & AbdelRahim, 2013) and displayed as Figure 2.34. The topology has been commonly investigated and applied to many commercial PV inverters.

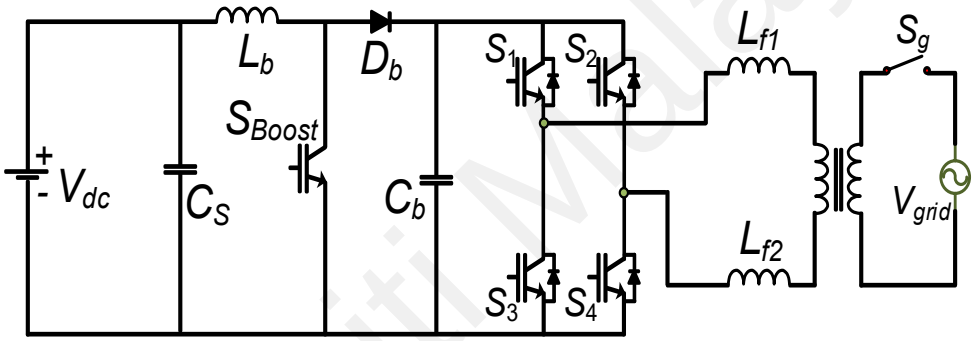


Figure 2.34: Two-stage boost inverter

Multi-stage inverters have also been designed with DC-AC-DC-AC concept. As presented in Figure 2.35, the topology involves a high-frequency step-up transformer, a rectifier, an intermediate DC-link; with boost and DC-link voltage control and DC-filter. Here, costs and losses are high, as both stages operate at high frequency. Figure 2.36 shows a "pseudo DC-link" topology, as it has fewer DC filters. In addition, for AC inversion the high-frequency DC pulse train is inverted as presented in (Xue & Chang,

2004). In (Bose, Szczesny, & Steigerwald, 1985) a multi-stage boost inverter involving current-source inverter in final power stage has been presented as shown in Figure 2.37.

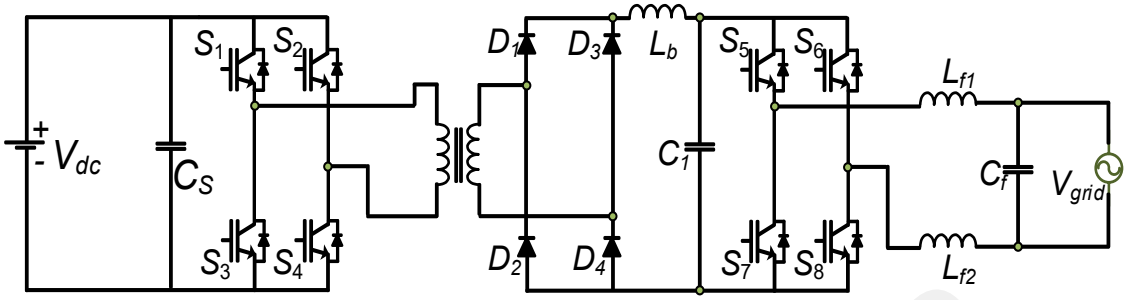


Figure 2.35: Multiple-stage inverter with DC-link between two-stages

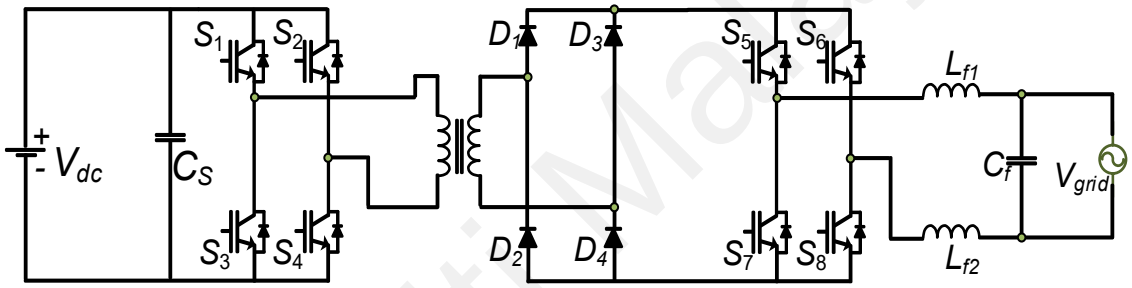


Figure 2.36: Multiple-stage boost inverter with pseudo-DC-link

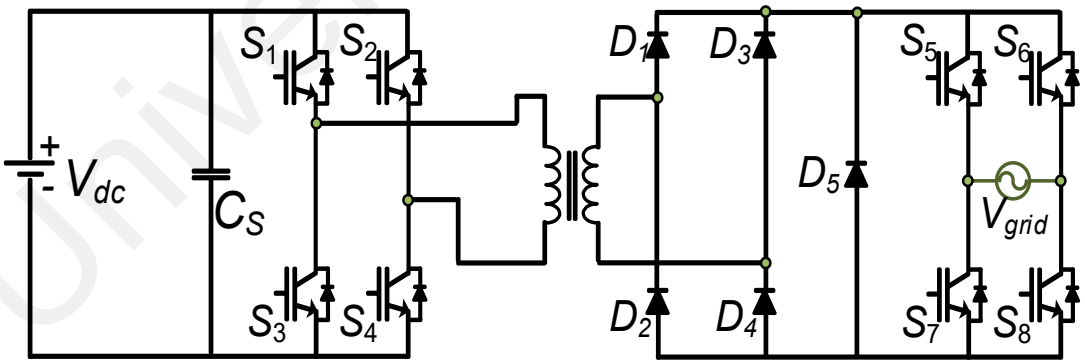


Figure 2.37: Multiple-stage boost inverter

2.5.2 Traditional Multilevel Inverter Topologies

MLI topologies were proposed 32 years ago. Such converters have been utilized to attain a preferred output-voltage from various symmetric or asymmetric levels of input dc voltages (J. Rodriguez, Jih-Sheng, & Fang Zheng, 2002; Yuan, 2017), stepping

forward to several residential and industrial applications (Abu-Rub, Holtz, Rodriguez, & Baoming, 2010; Baiju & Shiny, 2018; Boora, Nami, Zare, Ghosh, & Blaabjerg, 2010; Kouro et al., 2010; Sonti, Jain, & Bhattacharya, 2017; Yu, Konstantinou, Townsend, Aguilera, & Agelidis, 2017). Considering the fundamental structure, MLI have been classified into three assemblies, the flying capacitor (FC) converter (Antoniewicz, Jasinski, Kazmierkowski, & Malinowski, 2016; Farivar et al., 2017; Shukla, Ghosh, & Joshi, 2010), the neutral point clamped (NPC) converter (Busquets-Monge et al., 2017; X. Liu et al., 2017; Marchesoni & Tenca, 2002; Jose Rodriguez, Bernet, Steimer, & Lizama, 2010; Stala, 2011, 2013) and the Cascaded H-bridge converters (CHB) (Busarello et al., 2018; Fuentes et al., 2017; Malinowski et al., 2010; B. Xiao et al., 2015; Yu et al., 2017). Owing to its structural requirements, the balanced voltage sharing (BVS) in the FC remains complex as it needs a higher amount capacitors for increased levels of the output-voltage. Moreover, to synthesize higher levels of output-voltage, NPC requires a greater amount of clamping diodes. In addition, the BVS remains a shortcoming of the NPC. In contrast, CHB converters offer a nominal standing voltage, quality output and simpler DC-link voltage balancing.

2.5.2.1 Diode clamped multilevel inverter

Diode–clamped or NPC remains the most common MLI topology (Busquets-Monge et al., 2017; X. Liu et al., 2017; Marchesoni & Tenca, 2002; Jose Rodriguez et al., 2010; Stala, 2011, 2013). Advantages of NPC MLI include low-enough harmonic content that comes with high-enough number of levels making a filter unnecessary, controlled reactive power flow and high efficiency. BVS remains a major problem.

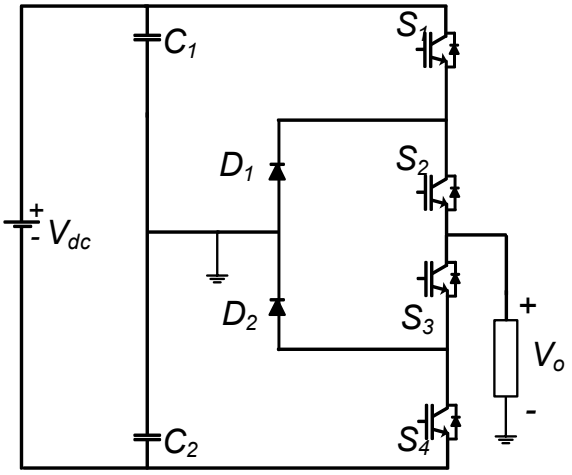


Figure 2.38: Three-level NPC MLI

The simplest NPC MLI has one leg made of two couples of switches connected in series, with two series capacitors connected in parallel. Figure 2.38 shows NPC multilevel inverter with one leg. It is called a single-phase H-bridge NPC three-level inverter.

2.5.2.2 Flying-Capacitor Multilevel Inverter

FC MLI do not require additional clamping diodes and isolated DC sides (Antoniewicz et al., 2016; Farivar et al., 2017; Shukla et al., 2010), and offer easy extensions to multiple levels. However, FC MLI confront BVS problem. Figure 2.39 presents a three-level FC MLI. This converter has a similar topology as that of the NPC with an exception of the FC.

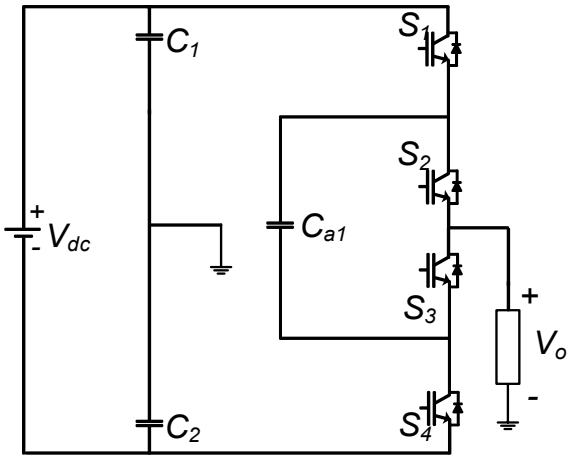


Figure 2.39: Three-level FC MLI

2.5.2.3 Cascaded H-bridge multilevel inverter

This topology has H-bridge converters or cascades employed for realizing a MLI (Busarello et al., 2018; Fuentes et al., 2017; Malinowski et al., 2010; B. Xiao et al., 2015; Yu et al., 2017). Figure 2.40 shows a three-level H-bridge topology. Here various DC sources, symmetric or asymmetric, are cascaded along with H-bridge arrangement of switches to increase the number of output-voltage levels.

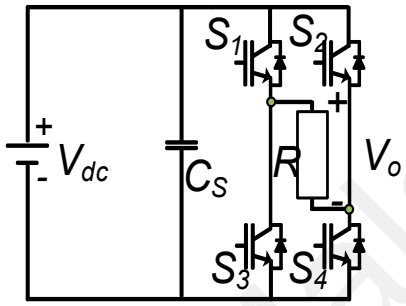


Figure 2.40: Three-level H-Bridge MLI

2.5.3 Reduced Switch (RS) MLI

Connection of H-Bridge with the RS MLI topology has been considered as the factor for classification of the RS design (Prabaharan & Palanisamy, 2017). RS MLI can be classified on the basis of symmetric and asymmetric topological arrangements.

2.5.3.1 No H-bridge MLI symmetric topologies

RS MLI was introduced in (Ebrahim Babaei, 2010; E Babaei, Hosseini, Gharehpetian, Haque, & Sabahi, 2007). Single DC source involving a quad combination of bidirectional switches (BSs) had been proposed for this topology. BSs can block the voltage and conduct the current in either direction. Here all switches were BSs.

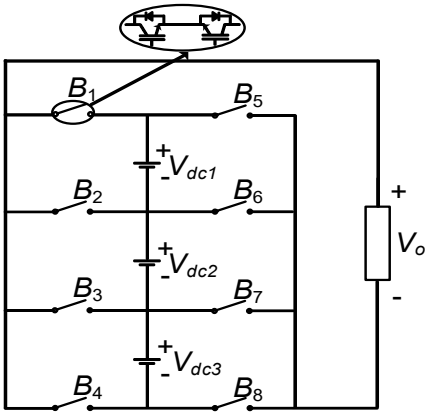


Figure 2.41: RS bidirectional MLI

Figure 2.41 presents the schematic diagram of the RS MLI topology. In (Ounejjar, Al-Haddad, & Gregoire, 2011) U-cells MLI topology was presented with unidirectional switches (US). Figure 2.42 presents the schematic of this topology. Recently in (Gurpinar & Castellazzi, 2016), RS MLI with various power switches had been presented.

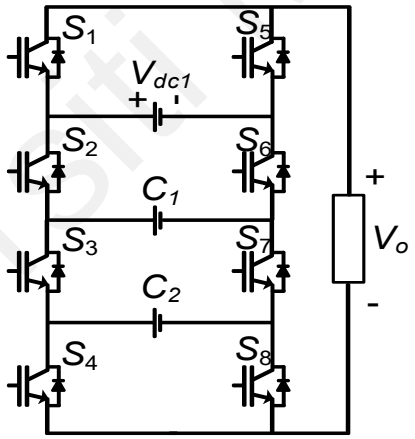


Figure 2.42: Packed U-Cell RS MLI

2.5.3.2 H-bridge MLI symmetric topologies

In (Ebrahim Babaei, 2008; Ebrahim Babaei & Hosseini, 2009; Ebrahim Babaei, Laali, & Bayat, 2015), a Cascaded Half-Bridge MLI was introduced as presented in Figure 2.43. Where, every cell requires individual DC source involving two Unidirectional Switches (US). Low-frequency switching is executed for the Full-Bridge Inverter switches and High-frequency operation is employed for the Half-bridge cells. In (Sze Sing Lee, Chu, Idris, Goh, & Heng, 2016), such a RS MLI topology for PV system is presented.

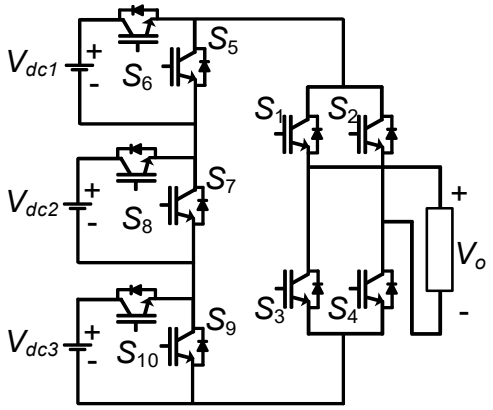


Figure 2.43: Cascaded half-bridge RS MLI

2.5.3.3 No H-Bridge MLI Asymmetric topologies

Various RS topologies deprived of the H-Bridge with symmetric operation are employed with an asymmetric fashion after necessary modifications. In (Ebrahim Babaei, 2010) two algorithms have been presented to calculate the asymmetric DC source values for the RS topology. The basic configuration has been presented in Figure 2.44 with binary sequence. Where, binary and trinary sequences have been adopted to attain asymmetry. When geometric progression of DC source values is increased with a factor of '3', it offers the trinary approach. Figure 2.45 displays the configuration for the trinary sequence.

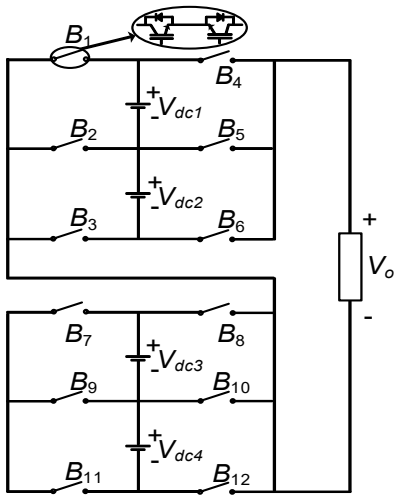


Figure 2.44: RS asymmetric MLI with binary sequence

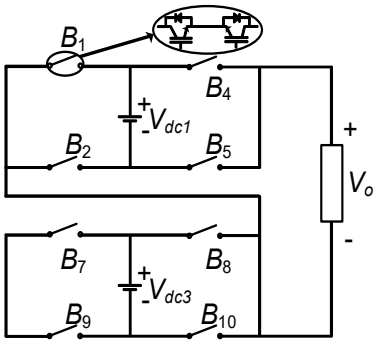


Figure 2.45: RS asymmetric MLI with trinary sequence

2.5.3.4 H-bridge MLI asymmetric topologies

MLI asymmetric topology involving H-bridge is presented in (Ebrahim Babaei, Dehqan, & Sabahi, 2013) and shown in Figure 2.46. Here, the fundamental unit is formed in series connection with H-Bridge inverter. Two individual DC sources are employed by the basic cell.

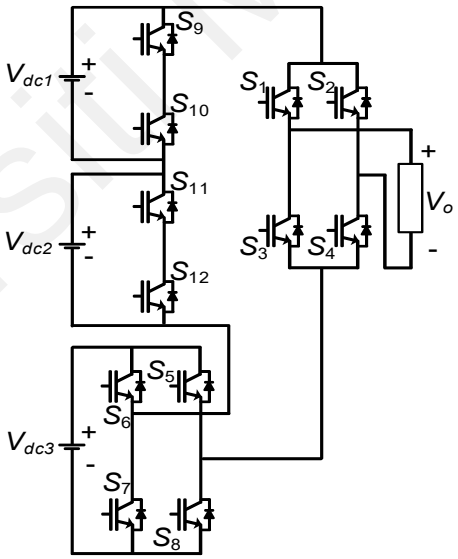


Figure 2.46: RS MLI asymmetric topology involving H-Bridge

2.5.3.5 Review of hybrid MLI

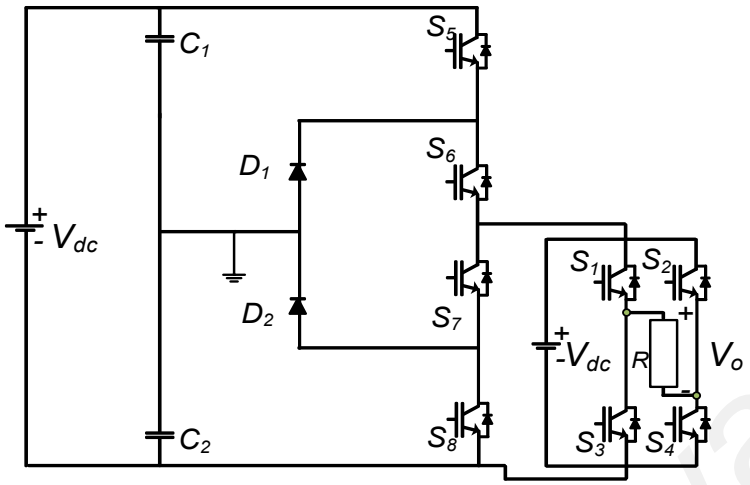


Figure 2.47: Hybrid MLI with NPC and CHB

As the name suggests the Hybrid MLIs remains an amalgamation of two different topologies. The NPC MLI is amalgamated with the CHB MLI (Jinghua & Zhengxi, 2008; Su, 2005) as presented in Figure 2.47.

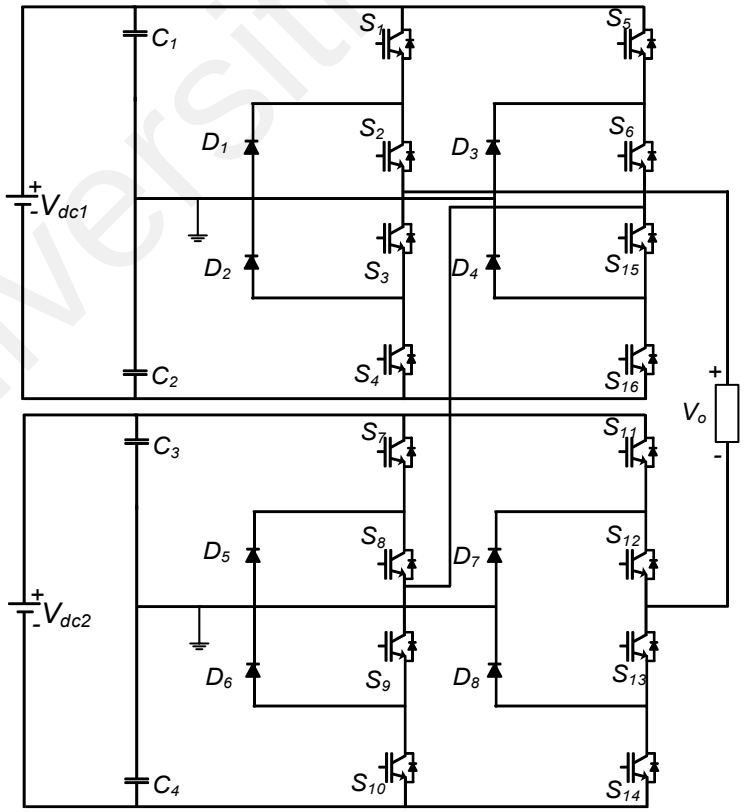


Figure 2.48: Hybrid MLI with NPC and half bridge inverter cells

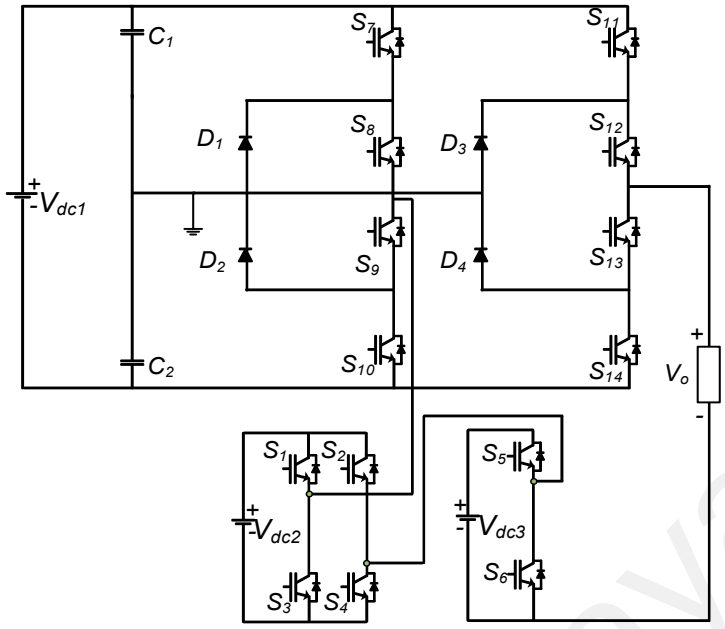


Figure 2.49: Hybrid MLI by two NPC and CHB

With an initial requirement of large output filter in various systems, these topologies can operate under both symmetric and asymmetric topologies. In addition, another hybrid MLI consisting of the H-bridge, NPC MLI and half-bridge inverter cells is shown in Figure 2.48 and presented in (Rech & Pinheiro, 2007).

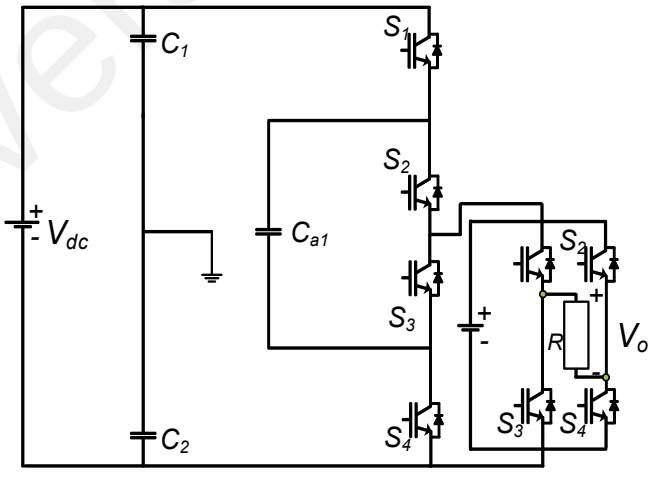


Figure 2.50: Hybrid MLI by FC and CHB

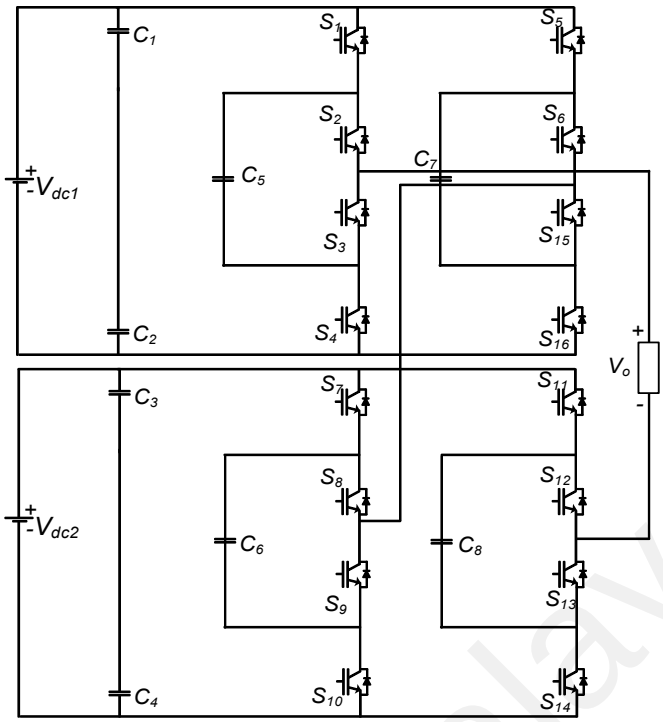


Figure 2.51: Hybrid MLI by two FC and CHB

Further, two NPC MLI are made in series connection with the CHB-MLI in an asymmetric sequence as presented in Figure 2.49 (Nami, Zare, Ghosh, & Blaabjerg, 2011). The CHB-MLI in amalgamation with FC-MLI is presented and proposed in (Su, 2005) and shown in Figure 2.50. In addition, with two FC-MLI (Edpuganti & Rathore, 2015; Jinghua & Zhengxi, 2008) has been presented in Figure 2.51.

2.5.4 Modulation Scheme

Inverter performance is influenced by the switching strategy employed as it directly relates to the output-voltage harmonic content. Inverter modulation schemes are low-switching-frequency and high-switching-frequency PWM.

Sinusoidal PWM, third harmonic PWM, 60^{o} PWM, space-vector PWM, and sigma-delta modulation are the well-known modulation techniques for three-phase conventional inverters (Cavalcanti et al., 2010). Modulation schemes for MLI also are classifiable as fundamental frequency or high frequency. Figure 2.52 shows tree diagram for inverter modulation control scheme (Prabaharan & Palanisamy, 2017).

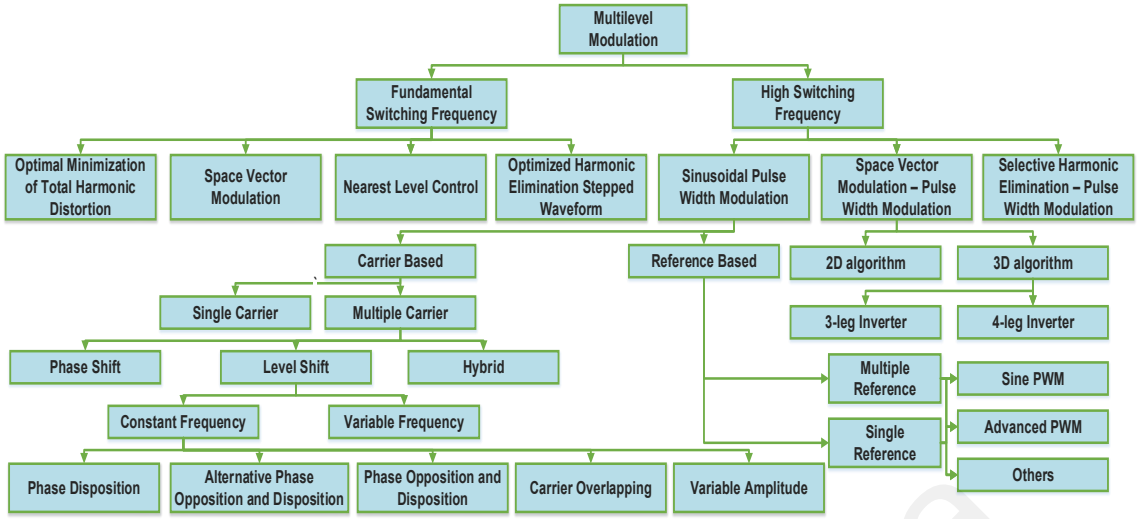


Figure 2.52: Classification of Modulation Control Scheme

In conventional H-bridge inverter, low-switching-frequency modulation can generate square-wave or modified-square wave output voltage. There are five high-switching-frequency PWM schemes: single PWM, sinusoidal PWM, modified sinusoidal PWM, and phase-displacement control.

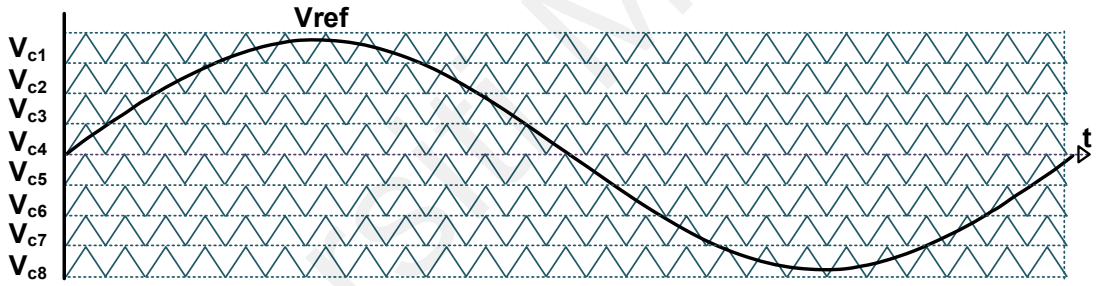
Common modulation techniques for MLI with low-frequency are Optimal Minimization of Total Harmonic Distortion (OMTHD), in which THD is minimized by minimizing all harmonics without focusing a specific component, and Optimized Harmonic Elimination Stepped Waveform (OHESW), in which specific harmonic components are eliminated (Dahidah & Agelidis, 2008; Sirisukprasert, 1999). In addition, Selective harmonic elimination PWM (SHE-PWM) technique for series H-bridge MLI applications can be used for an arbitrary number of levels and switching angles.

SPWM in MLI can be used for control switching. The number of carrier waves, however, exceeds one. An increased performance of the MLI is attained by the Multi-carrier SPWM control methods. Their classification depends on carrier signal arrangement (either vertical or horizontal). Definition of vertical carrier distribution techniques:

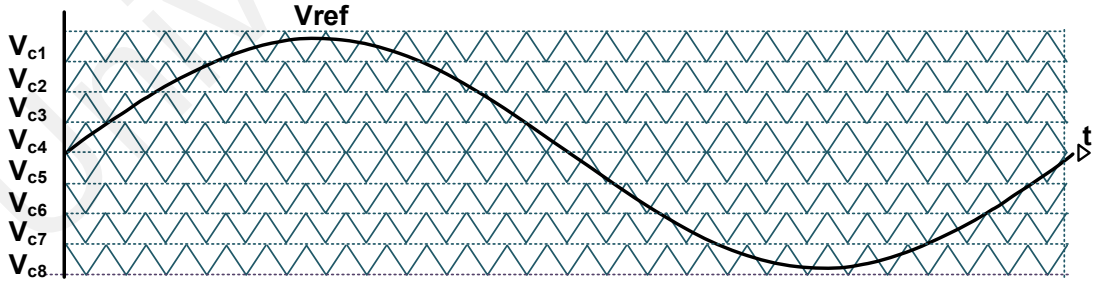
1. Each carrier is phase-shifted at 180^{o} degrees from the next carrier in alternative phase opposition disposition (APOD) method.
2. Carriers above sinusoidal reference point (SRP) zero are 180^{o} out-of-phase with the ones below SRP in the Phase opposition disposition (POD) method.
3. All carriers are in-phase for the Phase disposition (PD) method.

Moreover, the Phase Shifted-PWM is actually useful only to CHB and FC topologies. In addition, PD-PWM remains better in application for the NPC (Feng & Agelidis, 2002).

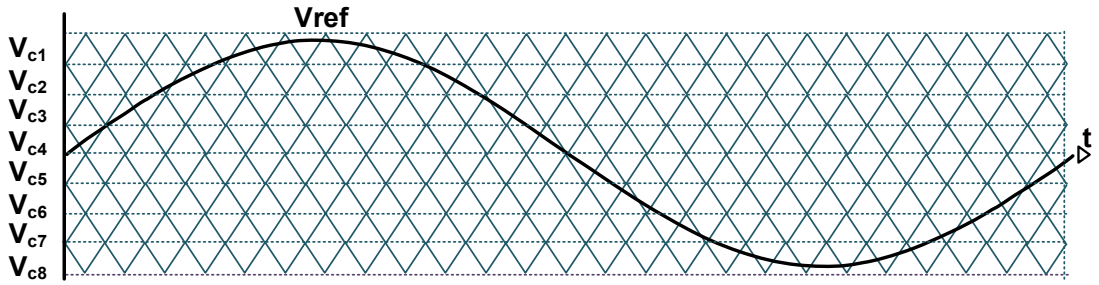
Figure 2.53 shows multicarrier SPWM control strategy for APOD, POD and PD. Whereas, Space Vector Modulation (SVM) method has been shown in Figure 2.54 mainly employed for three phase.



(a) Phase disposition



(b) Phase opposition disposition



(c) Alternative phase opposition disposition (APOD)

Figure 2.53: Multicarrier SPWM control strategies

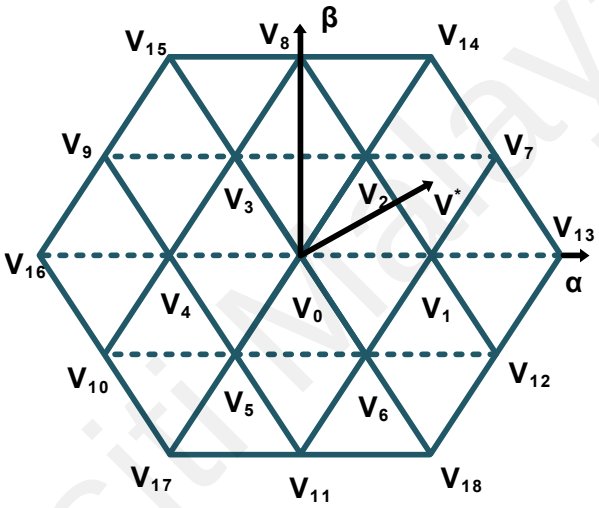


Figure 2.54: SVM Method

2.5.5 Current Control Schemes

Grid-connected PV inverter voltage cannot be controlled. Current quality determines power quality. Current control is important to system. Performance of complete system depends on their current-control strategy, which (Kazmierkowski & Malesani, 1998) achieves the fundamental requirements as offering a better harmonic profile of the output-current, regulation of DC-link voltage, and a better dynamic response. A grid-connected system is mainly employed to deliver optimum PV array power and energy and near unity power factor to the utility grid (Blaabjerg & Yang, 2017; S. B. Kjaer, Pedersen, & Blaabjerg, 2005). A current controller's main task is to force inject grid current into the grid following the reference signal.

Inverter's output-voltage modulation principle is often achieved by comparing actual measured current i_{grid} with desired reference i_{ref} as presented in Figure 2.55. A current controller to offer modulator with a control signal or directly generate switching states for the semiconductor devices in the converter, employs error signal δ.

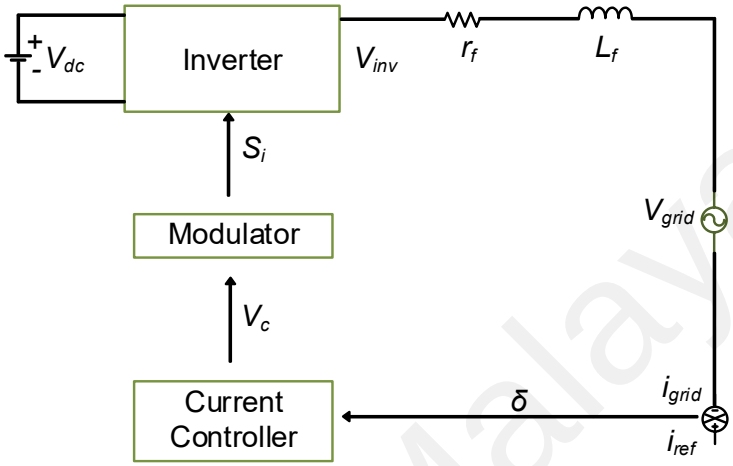


Figure 2.55: Basic current control scheme

Major strategies for output-current regulation of the VSI remain ramp, predictive, hysteresis, and ramp current control. Other current control methods are sliding mode, fuzzy, neural network, etc.

2.5.5.1 Hysteresis current control

Among control methods, hysteresis current control (HCC) remains easy to implement and the current control is robust against changes to the source parameters (Malesani, Mattavelli, & Tomasin, 1997). HCC has been implemented in (Bode & Holmes, 2000).

For HCC of the inverter in Figure 2.56, a comparison is made of the current-error signal δ against the hysteresis band. When δ crosses upper boundary $+h$, switches S1 and S4 turn ON, while the switches S2 and S3 are turned OFF. Further, when δ crosses the lower boundary $-h$, the semiconductor switches S1 and S4 turn OFF, while the switches S2 and S3 are turned ON. Figure 2.57 is the hysteresis modulator.

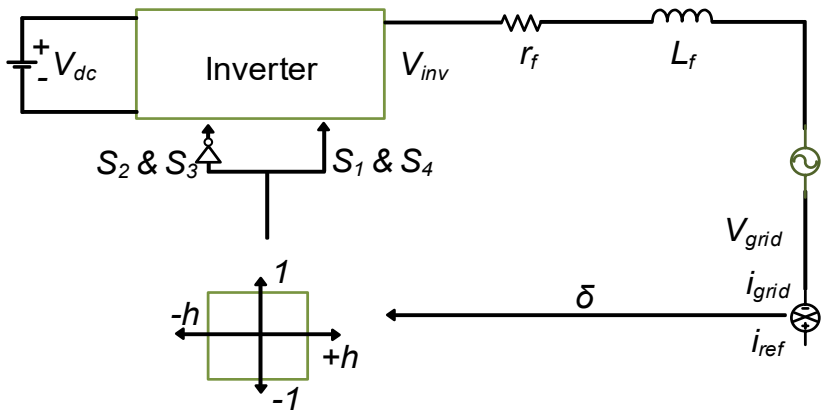


Figure 2.56: HCC with single-band

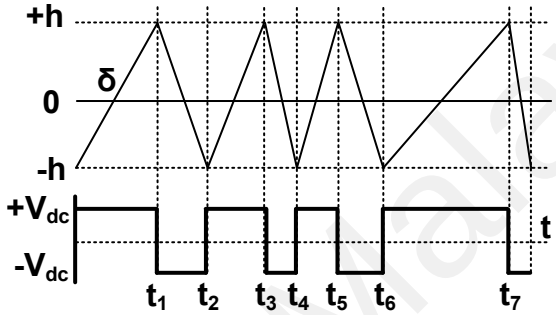


Figure 2.57: Hysteresis modulator

2.5.5.2 Linear current control

Ramp comparison controllers, stationary vector controllers, or synchronous vector controllers can be classified under the category of linear current controllers. Where, the ramp comparison for switching signals compares the current errors against the triangular wave (Castilla, Miret, Matas, de Vicuña, & Guerrero, 2008). Phase current error δ is given to the PI controller, and Vc remaining output from the controller is compared with the triangular carrier of the pulse-width modulator as presented in Figure 2.58.

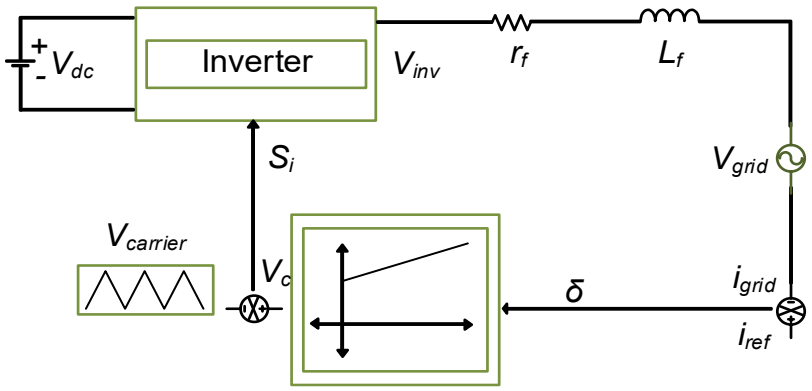


Figure 2.58: Ramp-comparison current-control scheme

Figure 2.59 presents output-voltage of inverter from comparing the control signal Vc with the triangular carrier Vcarrier. The switches are activated, when control signal is more than triangular signal offering +Vdc. By contrast, output-voltage is –Vdc, when control signal is less than carrier signal.

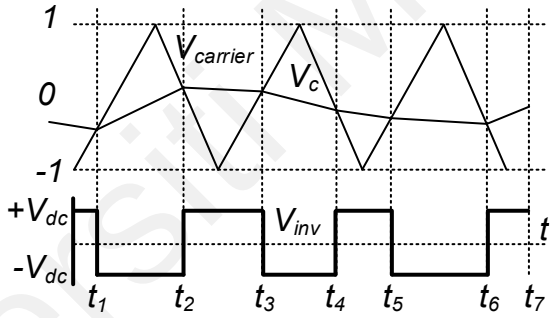


Figure 2.59: Inverter output voltage achieved via comparison between control signal V_c and triangular carrier voltage $V_{carrier}$

2.5.5.3 Predictive current control

Inverter voltages are computed by the predictive current control in order to push the determined currents to track the reference current (Moon & Yoon, 1998). The method has potential to achieve more-accurate current control with less noise. However, it requires more calculations and calibrations. Powerful, low-cost DSP-based microcontrollers have made for implementation of predictive strategies into digital controllers, particularly popular recently.

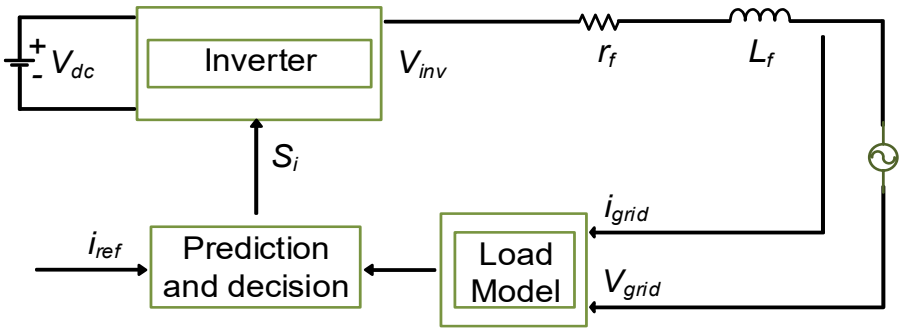


Figure 2.60: Basic structure of predictive current control

Predictive current controller's basic idea is a robust that chooses an optimum control scheme among all possibilities fulfilling a predefined criteria. Figure 2.60 presents the structure of the predictive current controller. Comparison of actual states against reference bases selection of the optimum switching state on the criteria decided upon (e.g., minimum switching frequency, minimum response time, minimum current distortion).

2.6 PV System Protection

Power stage, controller, DC interface, and AC interface are the four major components of the PV inverter. There remains a necessity to protect all four major components of the PV system. Considering the case of stand-alone PV systems, the protection is against: overload, galvanic isolation between DC and AC sides, over-temperature, auto-start/demand start features, reverse polarity, high and low battery voltages, surge capacity, and EMI. Stand-alone systems differ from grid-connected PV systems, which offer self-protection against: extreme conditions such as reverse polarity, high temperature, high current, over/under voltage and over/under frequency.

In addition, fundamental function of a grid-connected inverter is to deliver power to local distribution grid. Power outages or anomalies in the grid can be dangerous and damaging to the consumers and the appliances in use. Upon the detection of a power outage the grid-tied PV system disconnects from the grid, while feeding the grid as an

isolated island, which is known as Islanding (Khamis, Shareef, Bizkevelci, & Khatib, 2013; Vyas, Kumar, & Kavasseri, 2017).

2.6.1 Anti-Islanding Standard

With recent revisions, the major anti-islanding standards have been set under AS 4777.3-2005, IEC 62116, IEEE 1547, IEEE 929-2000, and VDE 0126-1-1 (Khamis et al., 2013; Vyas et al., 2017). The required islanding disconnection times, frequencies, and voltage operation ranges are determined with the quality factors (Q_f) (Khamis et al., 2013; Vyas et al., 2017).

Table 2.2: Anti-Islanding Standards

Standard	Islanding detection time	Q_f	Nominal Voltage Range	Nominal Frequency range
AS 4777.3-2005	t<2s	1	Setting Value	Setting Value
IEC 62116	t<2s	1	$85\% \leq V \leq 115\%$	$(f_o - 1.5\text{Hz}) \leq f and f \leq (f_o + 1.5\text{Hz})$
IEEE 1547	t<2s	1	$88\% \leq V \leq 110\%$	$59.3\ \text{Hz} \leq f \leq 60.5\ \text{Hz}$
IEEE 929-2000	t<2s	2.5	$88\% \leq V \leq 110\%$	$59.3\ \text{Hz} \leq f \leq 60.5\ \text{Hz}$
VDE-0126-1-1	t<0.2s	2	$80\% \leq V \leq 115\%$	$47.5\ \text{Hz} \leq f \leq 50.2\ \text{Hz}$

According to IEEE 929-2000 standard, quality factor is determined by equation (2.52):

$$Q_f = \tan(\cos^{-1}[pf]) \tag{2.52}$$

2.6.2 Anti-Islanding Technique

Anti-islanding technique can be classified as remote or local. On one hand, remote techniques are used usually at the utility site. Such approaches generally do not offer a no-detection zone (NDZ), but an effective and efficient performance in the multi-PV inverter systems, quality of PV-inverter output-power is not degraded, are too expensive

and can complicate system communication. On the other hand, local techniques, either active or passive, are set at the PV-inverter sites, and utilize information available onsite.

Considering the active anti-islanding techniques. Such techniques are cheaper and simpler for implementation, yet the output-power quality may be degraded, resulting into PV-inverter instability. Here, the NDZ is relatively small where disturbance is introduced to the PV-inverter output by the active techniques. The major active anti-islanding techniques include (Khamis et al., 2013; Vyas et al., 2017): Impedance Measurement (IM), Phase Shift (or Frequency Shift) and Reactive Power Export (RPE) Error Detection.

Table 2.3: OVP/UVP and OFP/UFP allowed according to Malaysian Standard

Detection algorithm	Threshold
UV	216V
OV	252V
UF	49Hz
OF	51Hz

Passive techniques can detect islanding-related anomalies, as over/under voltage protection (OVP/UVP) and over/under frequency protection (OFP/UFP). If voltage exceeds the range between OVP or OFP the device utilized for disconnection operates within a set period. Passive techniques are simpler to implement and inexpensive. The degradation of the PV-inverter power-generation quality is minimal, but the technique has a relatively large NDZ. Table 2.3 presents the OVP/UVP and OFP/UFP allowed according to Malaysian Standard.

2.7 Summary

This chapter presented the mathematical modelling for the PV-cell and analyzed the PV array performance under various atmospheric conditions. Further, MPPT algorithms

had been discussed by categorizing the techniques into digital, analog and hybrid methods. In addition, a modified INC technique has been proposed and explained.

Moreover, to realize a PV system and to extract maximum energy, power converters are used along with the MPPT techniques. Such power converters in PV applications have been surveyed. In addition, for PV system protection, anti-islanding standards, and anti-islanding techniques have been discussed.

Furthermore, MLI play an important role with high and medium powered applications. Where, the RS-MLI topologies offer numerous merits. Against the two-level traditional inverter, the RS-MLI are utilized to attain a higher number of output-voltage levels N_{level}, with lesser semiconductor devices, reduced dv/dt stress, better voltage and current THD waveforms, reduced EMI and size of passive filters.

Here, the focus was on grid-connected inverters; therefore, a brief overview of grid-tied inverters was presented before analyzing the MLI topologies. This chapter also focused on several MLI topologies focusing on the RS-MLI constructions by classifying them as asymmetric, symmetric and hybrid topologies. Finally, different modulation techniques and current control algorithms for MLI had been discussed.

CHAPTER 3: PROPOSED SINGLE-PHASE T AND π-TYPE GRID-CONNECTED PV INVERTERS

3.1 Introduction

Design and operating principles of single-phase T-type Cascaded H-Bridge (TCHB) and π-type Cascaded H-Bridge (PiCHB) Multilevel Inverters (MLI) have been presented in this chapter. TCHB MLI offers nine output-voltage values (2Vdc, 3Vdc/2, Vdc, Vdc/2, 0, −Vdc/2, −Vdc, −3Vdc/2, −2Vdc) from two separate dc supply sources, by utilizing two T-type Bidirectional Switches (BSs). Moreover, the PiCHB inverter offers thirteen output-voltage values (2Vdc, 5Vdc/3, 4Vdc/3, Vdc, 2Vdc/3, Vdc/3, 0, −Vdc/3, −2Vdc/3, −Vdc, −4Vdc/3, −5Vdc/3, −2Vdc) from two separate dc supply sources, by utilizing two π-type BSs. Moreover, owing to the balanced PWM technique utilized for the TCHB inverter, self-balancing of the capacitor voltages in the DC-link is attained. However, for Balanced Voltage Sharing (BVS) in the PiCHB inverter a passive balancing circuit has been utilized. In this work, both the inverters utilized the low-frequency and the high-frequency switching with PWM. The proposed MLI were applied to a PV system. The controlling algorithms were for MPPT based on mINC, current-controller based on PI technique, and islanding protection based on a passive technique.

In the low-frequency switching, Optimized Harmonic Elimination Stepped Waveform (OHESW) technique improved the output waveforms of the proposed inverter. Open-Bracketed Newton-Raphson Method (NRM) discussed in chapter 2 was utilized to solve the OHESW technique's transcendental equations, producing possible solutions with random initial guesses. The solution offering minimum harmonic profile for the output-voltage THD was selected amongst multiple solution sets obtained.

For high-frequency switching, two PWM techniques are introduced to generate the switching signals. These signals are employed to produce nine and thirteen output-voltage levels. For TCHB, the PWM technique utilized one carrier and eight reference signals. Modulation signals were complete sinewaves identical in shape and size except for an offset, whose value equaled the carrier-signal amplitude. For PiCHB, the PWM technique utilized one carrier and twelve reference signals. Similarly, complete sinewaves (modulation signals) identical in shape and size except for an offset were compared with the carrier.

3.2 Structure and Principle Operation of Proposed Inverters

3.2.1 TCHB Inverter

3.2.1.1 Proposed Circuit Configuration

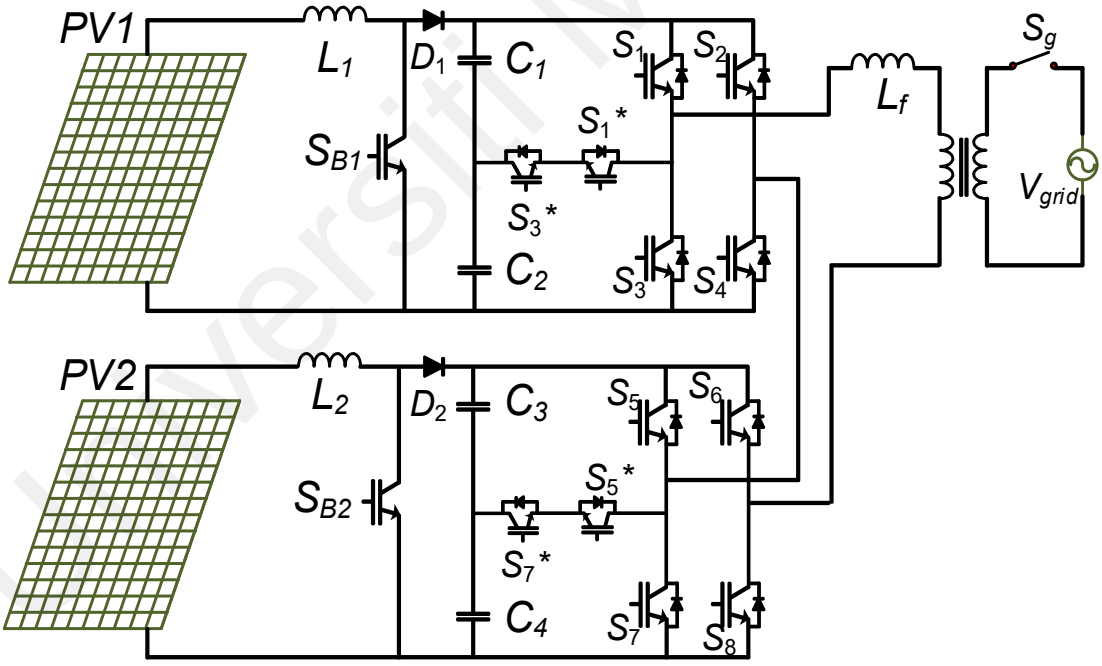


Figure 3.1: Proposed single-phase TCHB grid-tied inverter topology

The BVS is an additional requirement of the symmetric MLI topologies to guarantee a better harmonic profile of output-current and voltage (Khoucha, Lagoun, Kheloui, & Benbouzid, 2011; S. S. Lee, Sidorov, Lim, Idris, & Heng, 2018). Therefore, a greater number of output-voltage levels and a balanced DC-link is the necessity of the symmetric

MLI. However, for higher output-voltage levels, the Conventional CHB (CCHB) MLI utilizes a high number of switches and gate drives.

Therefore, the TCHB inverter topology has been proposed to attain higher level with reduced switches and gate drivers. It utilizes two T-type BS as presented in Figure 3.1, consequently lowering number of switches, gate drivers and switching losses. A grid-tied PV system was realized by employing a MPPT based on mINC and PI-based grid current-control techniques for the proposed TCHB topology.

3.2.1.2 Comparative Analysis

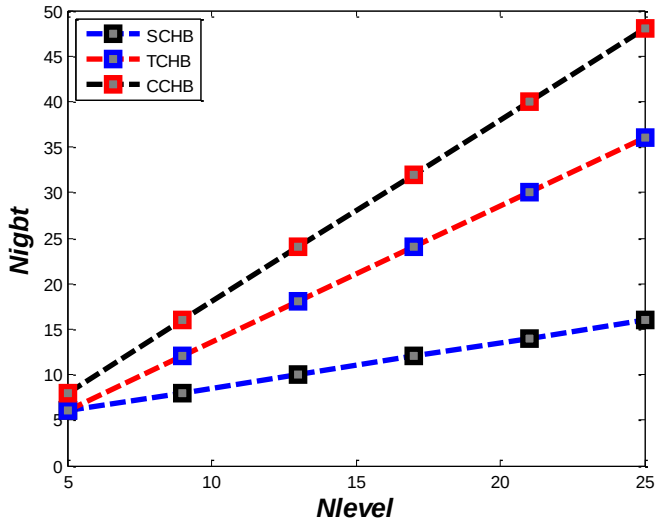
For symmetric MLI basic necessity is maintaining an equivalent values of all dc sources involved. Proposed TCHB inverter design can be modeled as:

$$V_{c1} = V_{c2} = V_c$$

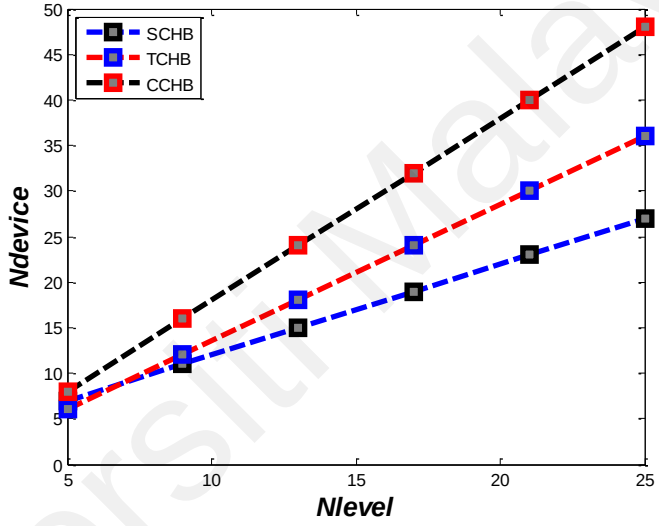
$$N_{level} = 2ab + 1 \tag{3.1}$$

$$N_{IGBT} = 2a(b + 1) \tag{3.2}$$

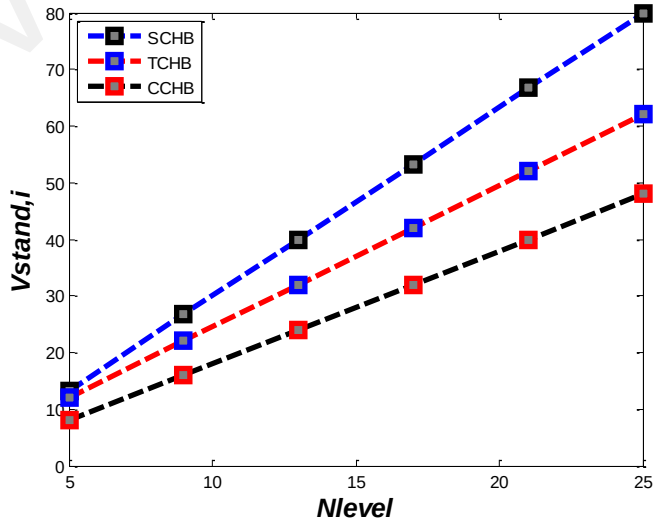
where V_c is voltage on each capacitor, N_{level} output-voltage levels, N_{IGBT} semiconductor switches employed, $N_{devices}$ the number of semiconductor switches and diodes, b capacitors in each cascade and a the number of cascades. Section 3.2.2 presents the plots of N_{IGBT}, N_{driver}, N_{device}, P_{cond}, P_{swit} and $V_{stand,i}$ while comparing the proposed topologies with the Symmetric Switch Capacitor H-Bridge Topology (SCHB) (Samanbakhsh & Taheri, 2016) and the Symmetric Conventional Cascaded H-Bridge (CCHB). For TCHB, Figure 3.2 presents a comparative analysis considering the parameters of N_{IGBT}, N_{device}, CF and $V_{stand,i}$.



a) N_{IGBT}

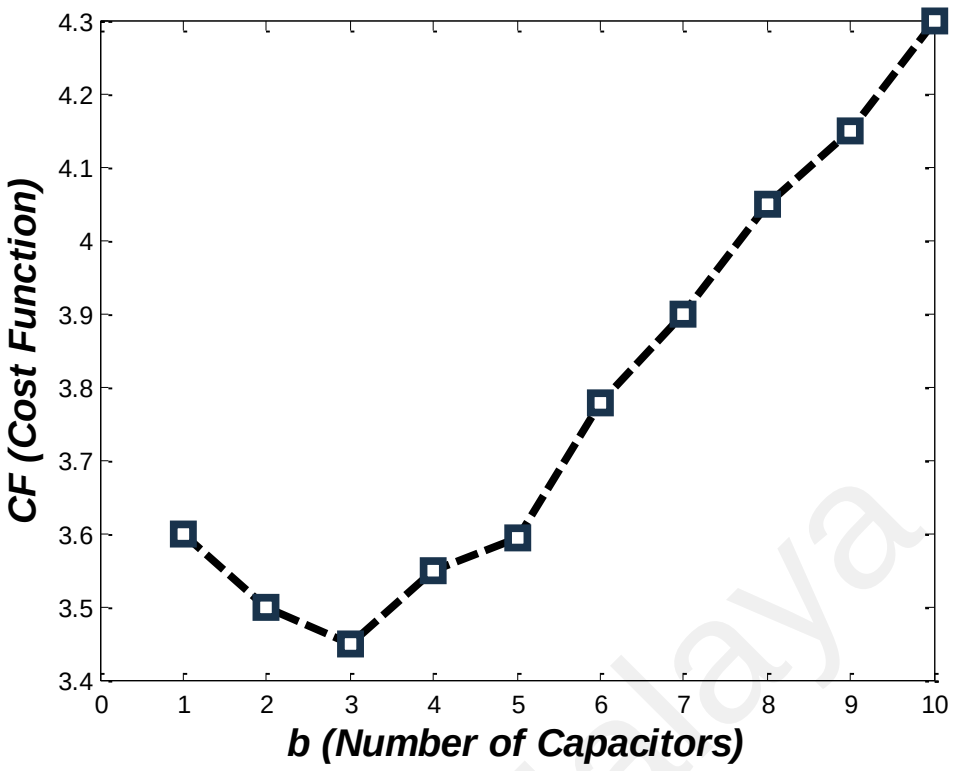


b) N_{device}

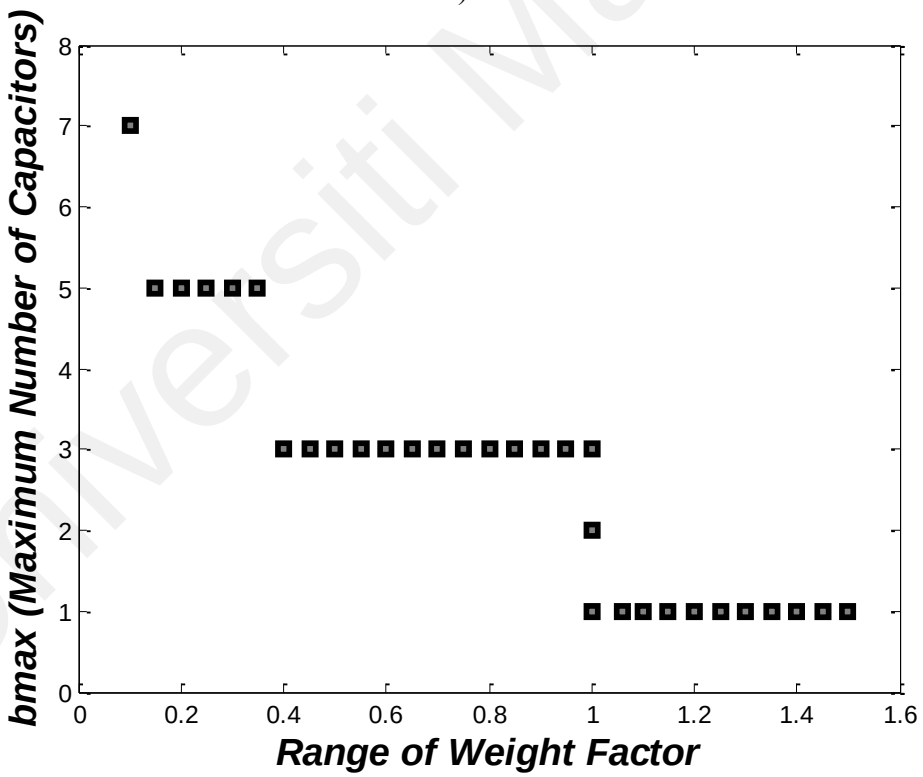


c) $V_{stand,i}$

Figure 3.2: Comparison of TCHB against SCHB and CCHB for a) N_{IGBT} b) N_{device} c) $V_{stand,i}$ d) CF and e) Range of α Vs b_{max}



d) CF



e) Range of α Vs b_{max}

Figure 3.2, Continued

Standing-voltage of TCHB can be attained as:

$$V_{out,a} = abV_c \tag{3.3}$$

$$V_{stand} = \left(\frac{3b^2+2b}{8} + 4b\right) V_c \qquad for \qquad b: even \tag{3.4}$$

$$V_{stand,i} = aV_{stand} \tag{3.5}$$

$V_{out,m}$ is the maximum output-voltage, V_{stand} semiconductor switches standing-voltage of each cascade and $V_{stand,i}$ standing voltage of the inverter. For the proposed TCHB grid-tied inverter, two cascades and two capacitors in each cascade are taken into consideration. As observed from above equations greater number of capacitors are appropriate taking into consideration the number of IGBTs. However, while taking into consideration the standing voltage, lesser number of capacitors is preferable. Hence, a tradeoff exists between the semiconductor switches and standing-voltage. To ascertain best performance, the cost function (CF) can be utilized:

$$CF = N_{IGBT} + \alpha V_{stand,i} \tag{3.6}$$

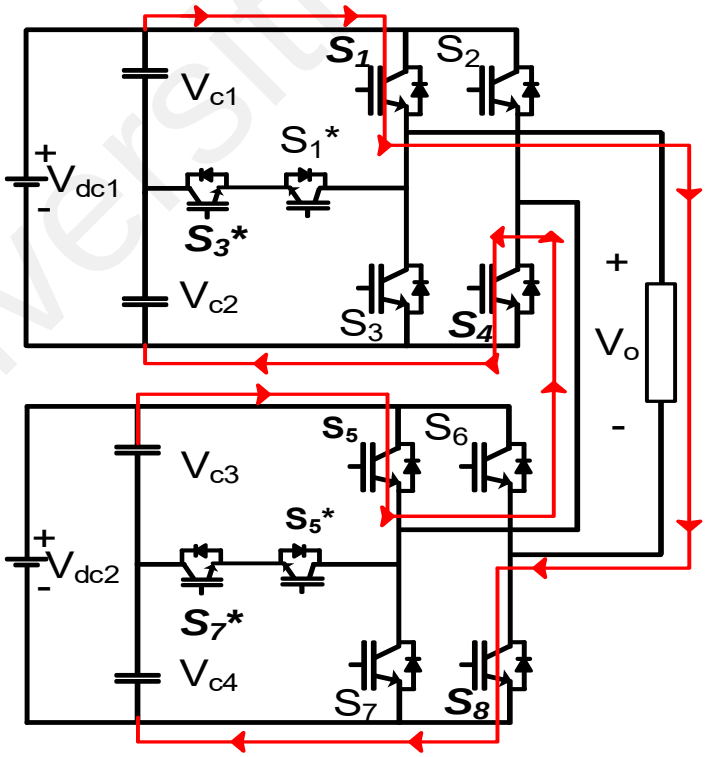
Where, the weight factor (parameter dependent on the semiconductor switch characteristics) of the $V_{stand,i}$ is represented by α, against N_{IGBT}. When N_{IGBT} is vital, α should be kept low. By contrast, if the $V_{stand,i}$ is more important, then α should be higher. Figure 3.2 (d) displays the variation of CF against b or number of capacitor (NC) for α = 0.8 (Ali et al., 2018). It remains quite evident from the plot of CF that TCHB can be further improved as it employs $b = 2$. In addition, Figure 3.2 (e) presents the maximum number of capacitors (b_{max}) against α. b_{max} offers a correspondence with reduced CF against a wide range of α values.

Table 3.1: Input Capacitor Current, Linked with the Output Current, Against Switching States for TCHB

Iout	**S1**	**S1***	**S3**	**S3***	**S2**	**S4**	**S5**	**S5***	**S7**	**S7***	**S6**	**S8**	**Vout**
Ic2 = -Iout ^ 0	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	ON	*Vdc/2*

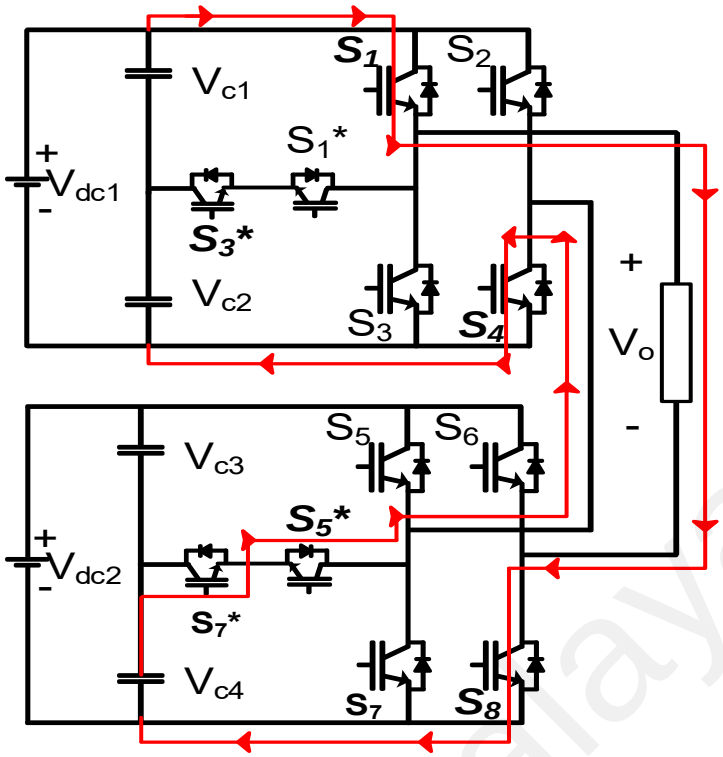
Ic1=Ic3=Ic4=0													
Ic1 = -Iout ^ 0 **Ic3=Ic4=0, Ic2=-Iout**	ON	OFF	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	ON	*Vdc*
Ic4 = -Iout ^ 0 **Ic3=0, Ic1=Ic2=-Iout**	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	*3Vdc/2*
Ic3 = -Iout ^ 0 **Ic1=Ic2=Ic4=-Iout**	ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	ON	OFF	ON	*2Vdc*
Ic1=Ic2=Ic3=Ic4=0	OFF	ON	ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	ON	*0*
Ic4=Ic3=Ic2=Ic1=0*	ON	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	ON	ON	OFF	*0**
Ic4 = Iout ^ 0 **Ic1=Ic2=Ic3=Iout**	OFF	ON	ON	OFF	ON	OFF	OFF	ON	ON	OFF	ON	OFF	*-2Vdc*
Ic3 = Iout ^ 0 **Ic4=0, Ic1=Ic2=Iout**	OFF	ON	ON	OFF	ON	OFF	OFF	ON	OFF	ON	ON	OFF	*-3Vdc/2*
Ic2 = Iout ^ 0 **Ic3=Ic4=0, Ic1=Iout**	OFF	ON	ON	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	*-Vdc*
Ic1 = Iout ^ 0 **Ic2=Ic3=Ic4=0**	OFF	ON	OFF	ON	ON	OFF	ON	OFF	OFF	ON	ON	OFF	*-Vdc/2*

3.2.1.3 Principles of operation

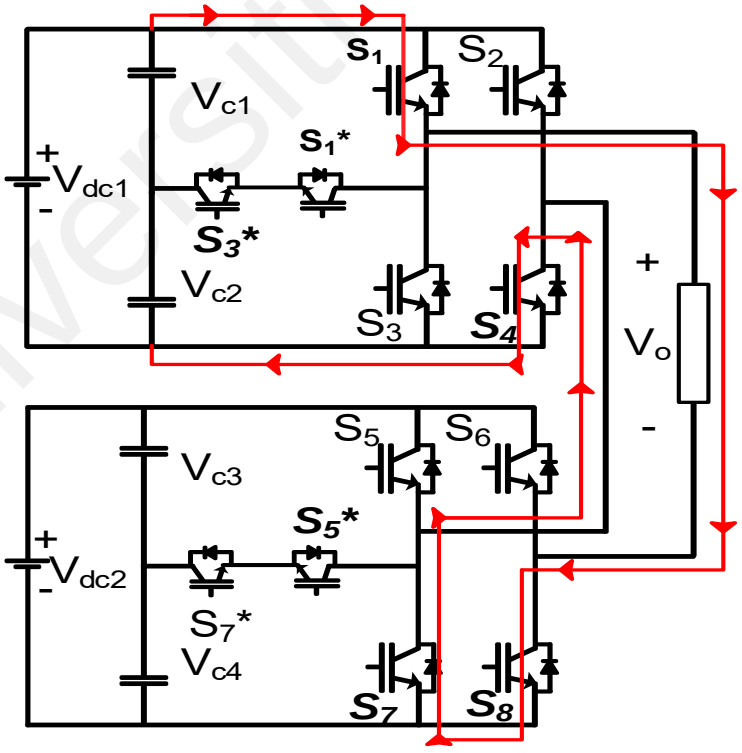


a) 2Vdc (S1, S4, S5 and S8 are ON)

Figure 3.3: (a-d) Modes of Operation for $V_{out} > 0$, (e-h) Modes of Operation for $V_{out} < 0$ and (i-j) Modes of Operation for Zero and Zero*

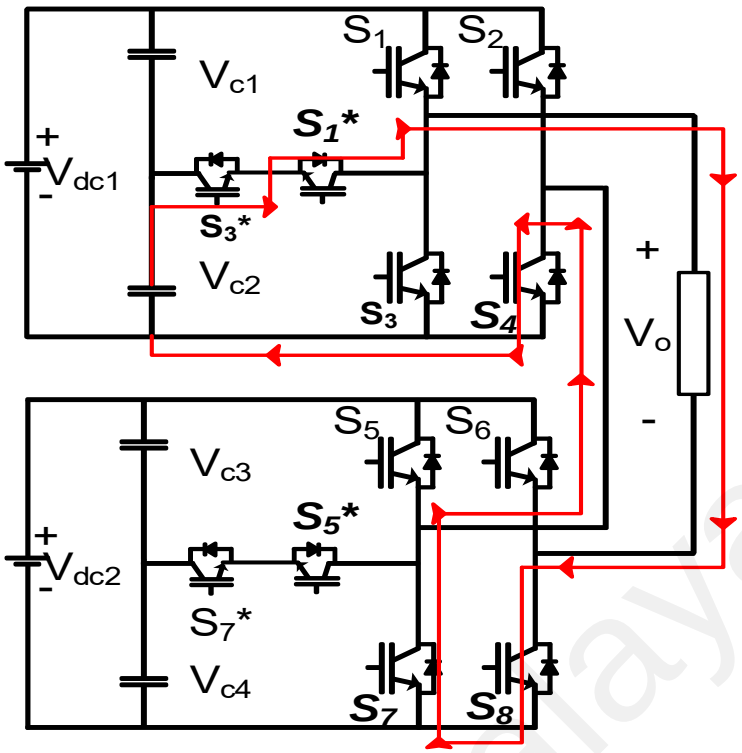


b) 3Vdc/2 (S1, S4, S8 and the bidirectional T-type switch formed by S5* and S7* is ON)

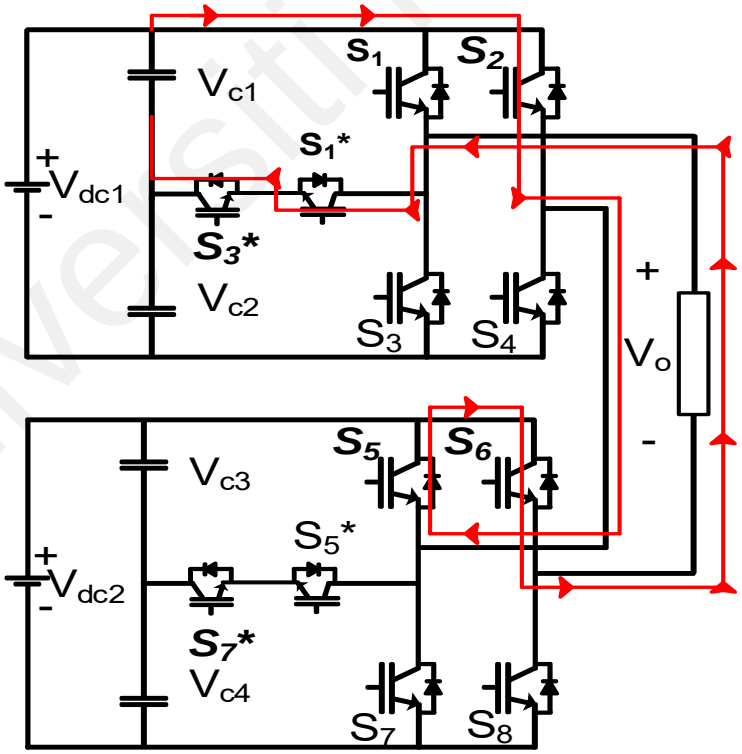


c) Vdc (S1, S4, S7 and S8 are ON)

Figure 3.3, continued

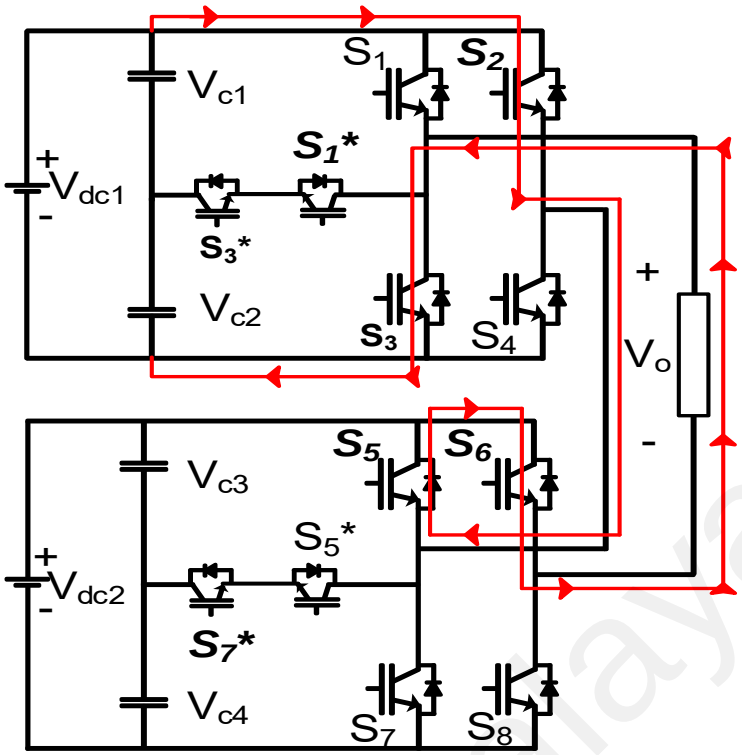


d) Vdc/2 (S4, S7 and S8 and the bidirectional T-type switch formed by S1* and S3* is ON)

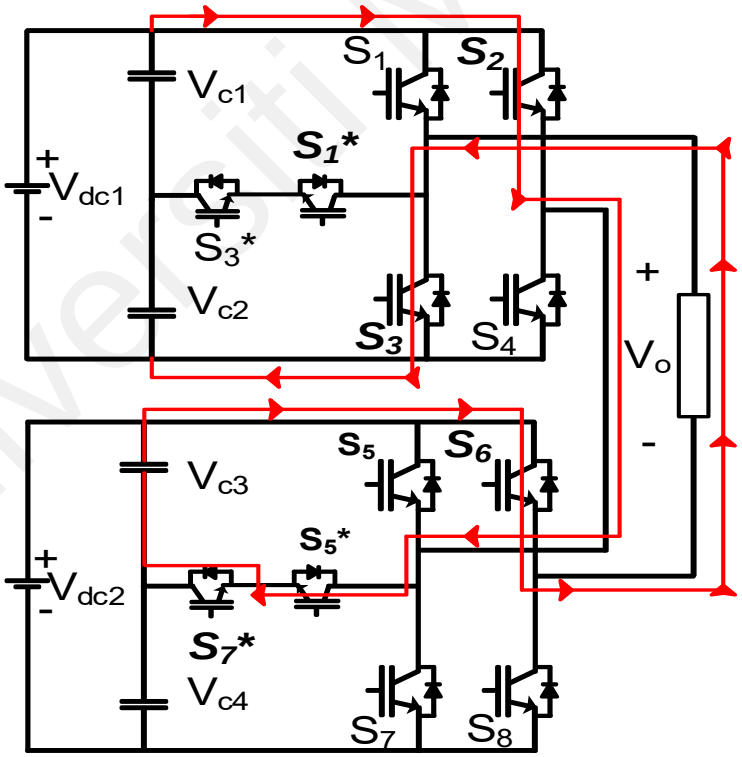


e) –Vdc/2 (S2, S5, S6 and the bidirectional T-type switch formed by S1* and S3* is ON)

Figure 3.3, continued

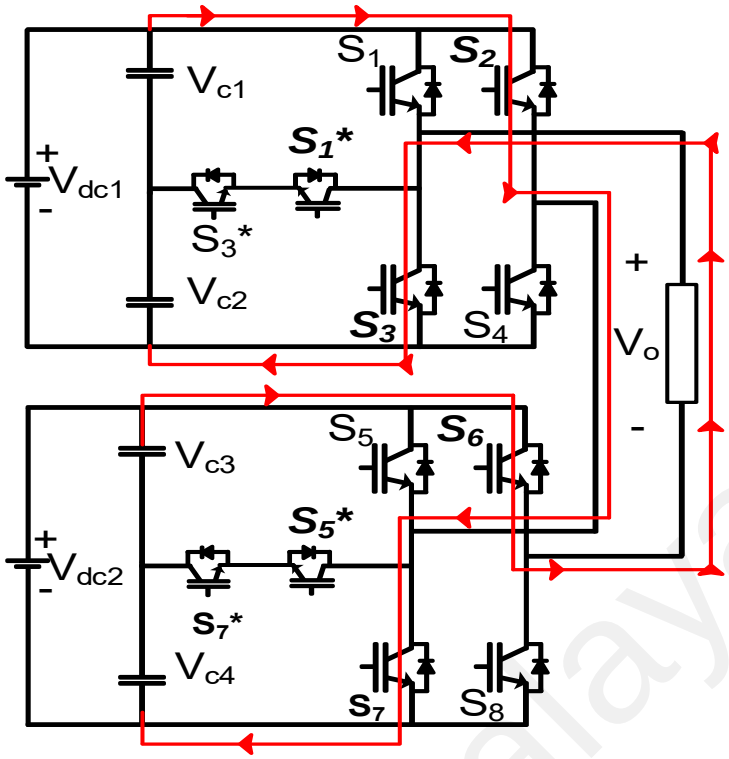


f) –Vdc (S2, S3, S5 and S6 are ON)

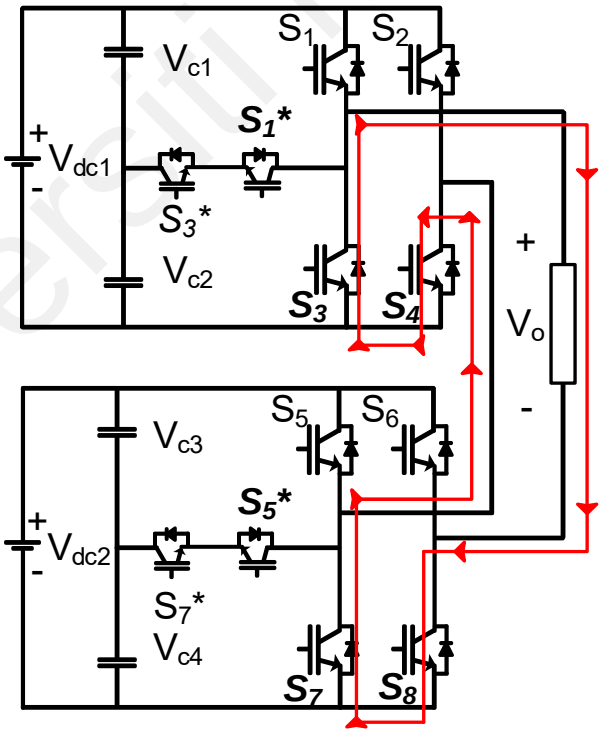


g) –3Vdc/2 (S2, S3, S6 and the bidirectional T-type switch formed by S5* and S7* is ON)

Figure 3.3, continued

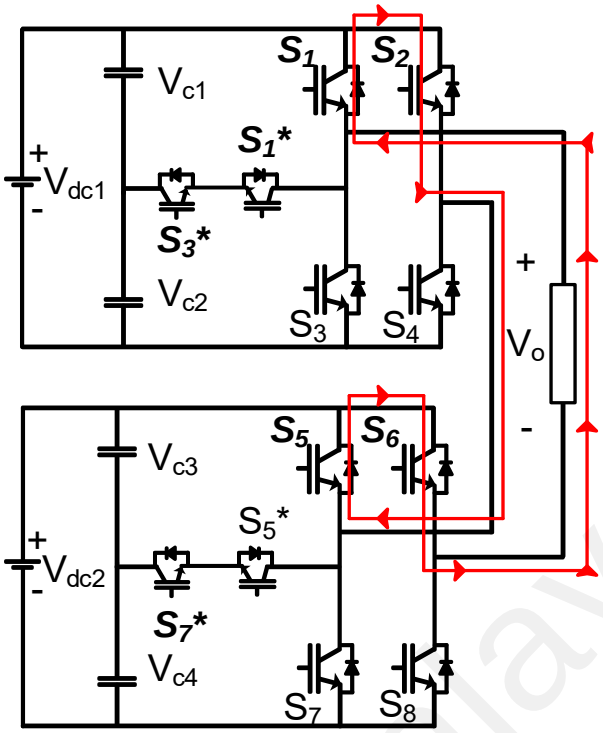


h) –2Vdc (S2, S3, S6 and S7 are ON)



i) Zero (S3, S4, S7 and S8 are ON)

Figure 3.3, continued



j) Zero* (S1, S2, S5 and S6 are ON)

Figure 3.3, continued

Taking into consideration the CF variations, the proposed TCHB inverter was established. It comprises of two H-bridges, two T-Type BS, and four voltage-dividing capacitors. Each cascade possesses one T-type BS and two capacitors, as presented in Figure 3.1. To boost voltage to grid requirements, two Dc–Dc boost converters were utilized. The converters were placed between the PV arrays and each cascade of the inverter. A filtering inductance Lf was employed at the output. Therefore, by utilizing a suitable PWM control for the cascaded inverter, nine output-voltage levels (2Vdc, 3Vdc/2, Vdc, Vdc/2, 0, −Vdc/2, −Vdc, −3Vdc/2, −2Vdc) were produced.

Nine switching states define the operation for the TCHB inverter, as presented in Figure 3.3(a)–(d) for $V_{out} > 0$ and in Figure 3.3(e)-(h) for $V_{out} < 0$, with zero and zero* presented in Figure 3.3 i & j, respectively. Table 3.1 shows the input-capacitor-current, linked with output-current, against switching states. For Figure 3.3, the red track

represents the current path for the specific mode of operation to attain the desired maximum voltage output.

1) 2Vdc positive output - S1, S4, S5 and S8 are ON. Here, S1 forms the path to connect the load positive terminal to V_{C1}, and S8 connects the load negative terminal to ground of V_{C4}. Current path in red of Figure 3.3(a) displays when the output voltage is 2Vdc.

2) 3Vdc/2 positive output - The bidirectional T-type switch formed by S5* and S7* is ON. Here, switching states for the first cascade remain unchanged from the preceding state. However, the load negative terminal, through S8, connects to the ground of V_{dc2}. Current completes its path through the bidirectional switch, which offers a trimmed voltage. Figure 3.3(b) shows the current paths in red when the output voltage is 3Vdc/2.

3) Vdc positive output - S1, S4, S7 and S8 are ON. Switches S7 and S8 form a closed circuit path through the second cascade. Figure 3.3(c) presents current path in red when the output voltage is 3Vdc/2.

4) Vdc/2 positive output - Bidirectional T-type switch formed by S1* and S3* is ON. Here, switching states for the second cascade remain unchanged from the preceding state. The load positive terminal connects to V_{dc1} via the bidirectional switch offering a trimmed voltage. Figure 3.3(d) shows the current paths in red when the output voltage is Vdc/2.

5) -Vdc/2 negative output - Bidirectional T-type switch formed by S1* and S3* is ON. However, S5 and S6 offer a short circuit path in the second cascade. The load terminal connects to V_{dc1} via the bidirectional switch, completing its path through S2. Figure 3.3(e) shows the current paths in red when the output voltage is -Vdc/2.

6) -Vdc negative output - S2, S3, S5 and S6 are ON. Here, switching states for the second cascade remain unchanged from the preceding state. The current passing from S2

completes its path through S3. Figure 3.3(f) shows the current paths in red when the output voltage is -Vdc.

7) -3Vdc/2 negative output - The bidirectional T-type switch formed by S5* and S7* is ON. Here, switching states for the first cascade remain unchanged from the preceding state. However, the load positive terminal, through S6, connects to the ground terminal of V_{dc1}. The current completes its path through the bidirectional T-type switch formed by S5* and S7*, which offers a trimmed voltage. Figure 3.3(g) shows the current path in red when the output voltage is -3Vdc/2.

8) -2Vdc negative output: S2, S3, S6 and S7 are ON. Here, S3 connects the load positive terminal to V_{C1}, and S6 connects the load negative terminal to V_{C3}. Figure 3.3(h) shows the current paths in red when the output voltage is -2Vdc.

9) Zero output: Two switching combinations can produce this level; either S3, S4, S7 and S8 are ON as presented in Figure 3.3(i), or S1, S2, S5 and S6 are ON as displayed in Figure 3.3(j). Voltage applied to the load is zero as the load line is short circuited.

3.2.1.4 PWM method involved

Figure 3.4 presents the PWM switching signal generation introduced for the proposed topology. Here, S2, S4, S6 and S8 would operate at fundamental frequency and Switches S1, S3, S1*, S3*, S5, S5*, S7 and S8 at the rate of carrier signal frequency. Figure 3.5 presents the inverter output-voltage of TCHB.

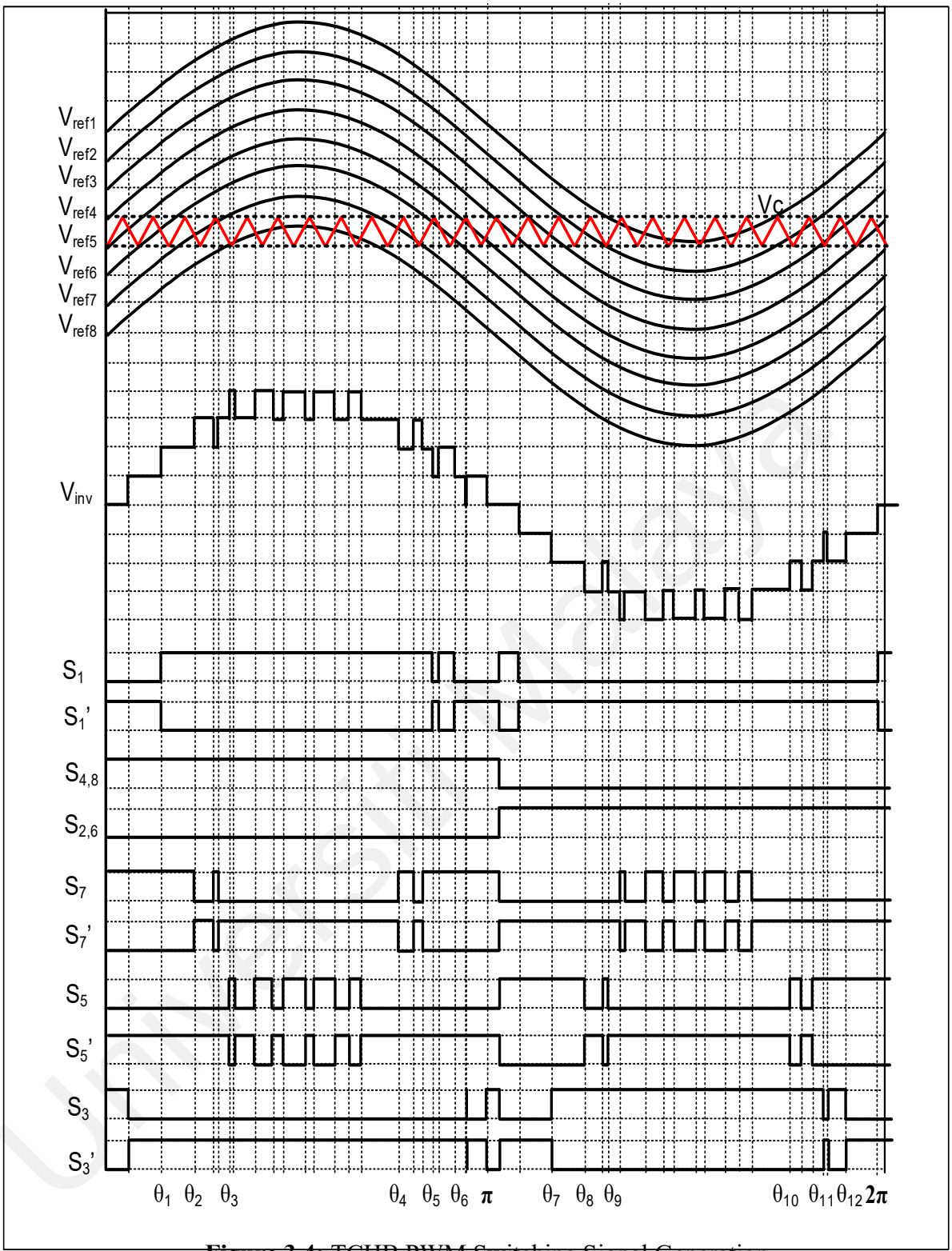


Figure 3.4: TCHB PWM Switching Signal Generation

Table 3.2: Range of Modulation Index and Phase Angle Displacement

Range of Ma	***Ma< .25***	***.25<Ma< .5***	***.5<Ma< .75***	***Ma>.75***
θ1	$\frac{\pi}{2}$	$\sin^{-1}(\frac{Ac}{Am})$	$\sin^{-1}(\frac{Ac}{Am})$	$\sin^{-1}(\frac{Ac}{Am})$
θ2	$\frac{\pi}{2}$	$\frac{\pi}{2}$	$\sin^{-1}(\frac{2Ac}{Am})$	$\sin^{-1}(\frac{2Ac}{Am})$
θ3	$\frac{\pi}{2}$	$\frac{\pi}{2}$	$\frac{\pi}{2}$	$\sin^{-1}(\frac{3Ac}{Am})$

θ4	$\frac{\pi}{2}$	$\frac{\pi}{2}$	$\frac{\pi}{2}$	π-θ_3
θ5	$\frac{\pi}{2}$	$\frac{\pi}{2}$	π-θ_2	π-θ_2
θ6	$\frac{\pi}{2}$	π-θ_1	π-θ_1	π-θ_1
θ7	$\frac{3\pi}{2}$	π+θ_1	π+θ_1	π+θ_1
θ8	$\frac{3\pi}{2}$	$\frac{3\pi}{2}$	π+θ_2	π+θ_2
θ9	$\frac{3\pi}{2}$	$\frac{3\pi}{2}$	$\frac{3\pi}{2}$	π+θ_3
θ10	$\frac{3\pi}{2}$	$\frac{3\pi}{2}$	$\frac{3\pi}{2}$	2π-θ_3
θ11	$\frac{3\pi}{2}$	$\frac{3\pi}{2}$	2π-θ_2	2π-θ_2
θ12	$\frac{3\pi}{2}$	2π-θ_1	2π-θ_1	2π-θ_1

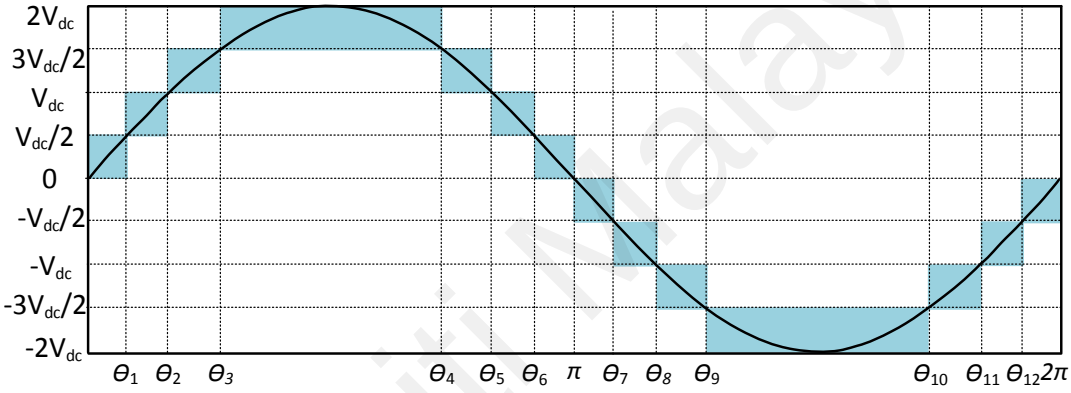


Figure 3.5: Nine-level Inverter Voltage $\boldsymbol{V_{inv}}$

Table 3.2 presents the range on modulation index and Figure 3.6 presents the respective low-frequency inverter output-voltage of the TCHB inverter with switching angles (Odeh & Nnadi, 2013). For Modulation index less than or equal to 0.25, $M_a \leq 0.25$, the inverter offers a three-level PWM output. For Modulation index greater than 0.25 and less than 0.5, $M_a > 0.25$ && $M_a < 0.5$, five-level inverter output is attained. At Modulation index greater than 0.5 and less than 0.75, $M_a > 0.5$ && $M_a < 0.75$, seven-levels of the output-voltage are attained. All signals are intersected against one carrier signal to attain nine-level output at Modulation index greater than 0.75 and less than 1, $M_a > 0.75$ && $M_a < 1$.

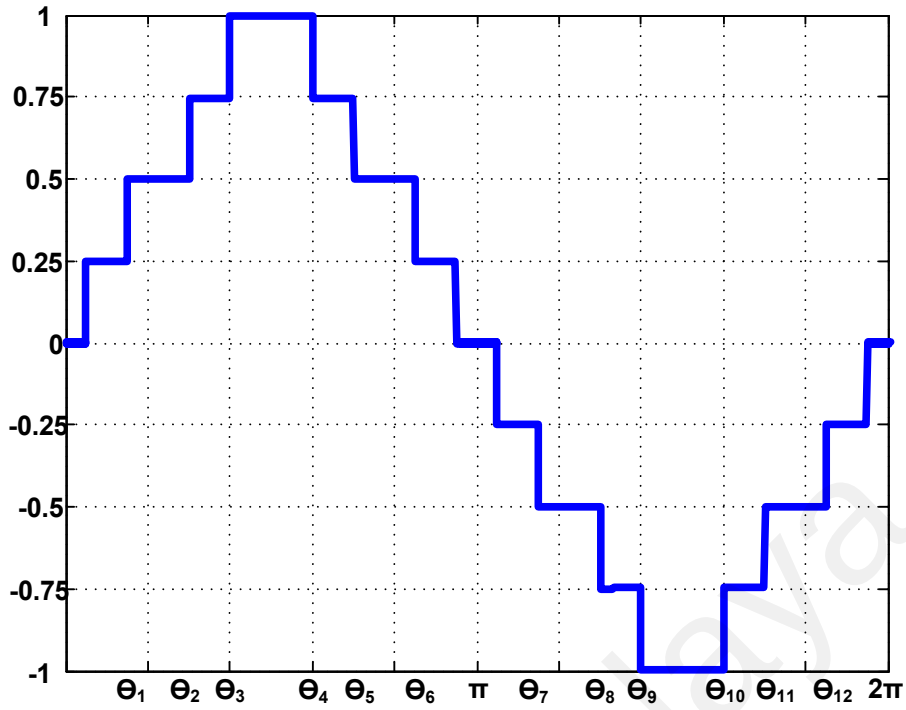


Figure 3.6: Nine-level output voltage with switching angles

Considering modulation strategy presented in Figures 3.4 and 3.5, output-voltage of the inverter can modelled as:

$$V_{out} = V_{c1}[(S_1)(1-S_2)(1-S_1^*) - (S_2)(1-S_1)(S_1^*)] + V_{c2}[(S_4)(1-S_3)(S_3^*) - (S_3)(1-S_4)(1-S_3^*)] + V_{c3}[(S_5)(1-S_6)(1-S_5^*) - (S_6)(1-S_5)(S_5^*)] + V_{c4}[(S_8)(1-S_7)(S_7^*) - (S_7)(1-S_8)(1-S_7^*)] \quad (3.7)$$

$$(S_1) = not(S_1^*), (S_2) = not(S_4), (S_3) = not(S_3^*), (S_5) = not(S_5^*), (S_6) = not(S_8), \& \ (S_7) = not(S_7^*)$$

$$V_{out} = V_{c1}[(S_1)(S_4)(S_1) - (S_2)(S_1^*)(S_1^*)] + V_{c2}[(S_4)(S_3^*)(S_3^*) - (S_3)(S_2)(S_3)] + V_{c3}[(S_5)(S_8)(S_5) - (S_6)(S_5^*)(S_5^*)] + V_{c4}[(S_8)(S_7^*)(S_7^*) - (S_7)(S_6)(S_7)] \quad (3.8)$$

As $S_n \in \{0,1\}, (S_n)^2 = S_n$

$$V_{out} = V_{c1}[(S_4)(S_1) - (S_2)(S_1^*)] + V_{c2}[(S_4)(S_3^*) - (S_3)(S_2)] + V_{c3}[(S_8)(S_5) - (S_6)(S_5^*)] + V_{c4}[(S_8)(S_7^*) - (S_6)(S_7)] \quad (3.9)$$

$$V_{outp} = V_{c1}[(S_4)(S_1)] + V_{c2}[(S_4)(S_3^*)] + V_{c3}[(S_8)(S_5)] + V_{c4}[(S_8)(S_7^*)] \quad (3.10)$$

$$V_{outn} = V_{c1}[-(S_2)(S_1^*)] + V_{c2}[-(S_3)(S_2)] + V_{c3}[-(S_6)(S_5^*)] + V_{c4}[-(S_6)(S_7)] \quad (3.11)$$

The switching frequency of switches $S_8 = S_4 = S_6 = S_2$, while operating at fundamental frequency, and rest operate at switching frequency of the output-voltage. In addition, S_1 and S_3 are 180 degrees phase shifted, similarly S_5 and S_7 are phase shifted. Equations (3.10) and consequently (3.11) offer complementary functions where each function is represented as $f_n = (S_i)(S_j), where\ i = 2,4,6,8\ and\ j = 1,3,5,7$. Such a complementary switching, operating at the switching frequency of the output voltage allows self-voltage balancing. The concept of self-voltage balancing was adopted from (Alishah, Hosseini, Babaei, Sabahi, & Gharehpetian, 2017). Here, the switching signals were generated by the intersection of one carrier and eight reference signals.

3.2.2 PiCHB Inverter

3.2.2.1 Proposed Circuit Configuration

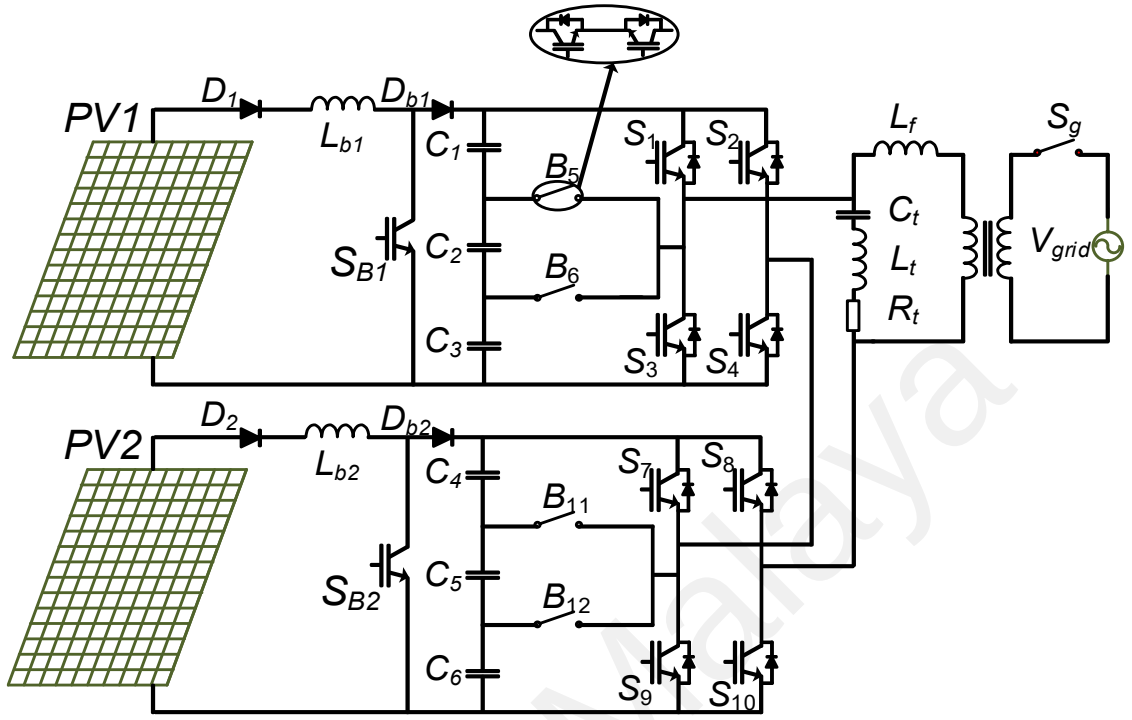


Figure 3.7: Proposed single-phase PiCHB grid-tied multilevel inverter

Considering symmetric CHB converters, balanced voltage sharing (BVS) on dc-link input capacitors is required. As the unbalanced state of operation can increase voltage stress on the switches damaging the entire system. Considering the design and dynamics of the single and three phase systems, several control techniques have been suggested for the three fundamental MLI topologies to confront the shortcomings of voltage imbalance (Giri, Chakrabarti, Banerjee, & Chakraborty, 2017; J.-S. Lee & Lee, 2014; López et al., 2017; Stala, 2011, 2013; C. Wang & Li, 2010). In addition, supplementary converters and switching circuits have also been employed to overcome the input capacitor voltage imbalance (Boora et al., 2010; Busquets-Monge et al., 2015; Shu, He, Wang, Qiu, & Jing, 2013). Further, various researchers have utilized the technique of natural balancing for the equal DC-link voltage sharing (McGrath & Holmes, 2009; Stala, 2011, 2013; Stala, Pirog, Baszynski, et al., 2009; Stala, Pirog, Mondzik, et al., 2009; K. Wang, Zheng, Xu, & Li, 2014). Such techniques have been utilized for CHB DC-Link capacitor voltage

balancing in (Napoles et al., 2013; Summers, Betz, & Mirzaeva, 2009; Watson, Wheeler, & Clare, 2007). Here, a passive balancing (RLC) circuit has been utilized for natural balancing to attain BVS. This technique remains independent of the load, dc voltage measurements, supplementary converters, switching circuits or complex control algorithms. Here, the load current or the current through the passive balancing (RLC) branch contributes for BVS at DC-link capacitors. Resonant frequency of passive RLC branch and the switching frequency of the proposed topology are adjusted to equalize the component frequency arising in output-voltage because of the imbalance. Balancing circuit current remains trivial when the input capacitors are balanced.

Further, an analysis of the PWM method has been presented to justify the natural balancing process in a single-phase CHB inverter with a passive RLC circuit as shown in Figure 3.7. The "π-Type" notation has been utilized following (Yuan, 2017).

3.2.2.2 Comparative Analysis

As discussed in the previous section with symmetric multilevel inverters, there remains a necessity to maintain the equivalent values of dc sources. Considering the symmetric condition for the proposed PiCHB inverter, it can be modeled as:

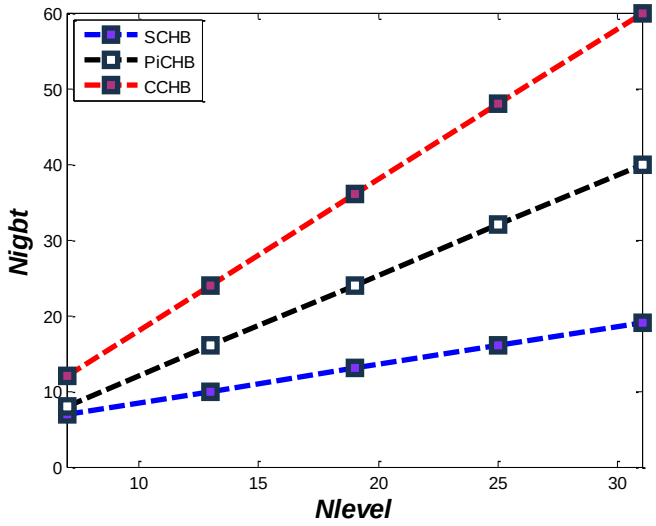
$$V_{c1} = V_{c2} = V_{c3} = V_{c4} = V_{c5} = V_{c6} = V_c$$

$$N_{level} = 2ab + 1 \tag{3.12}$$

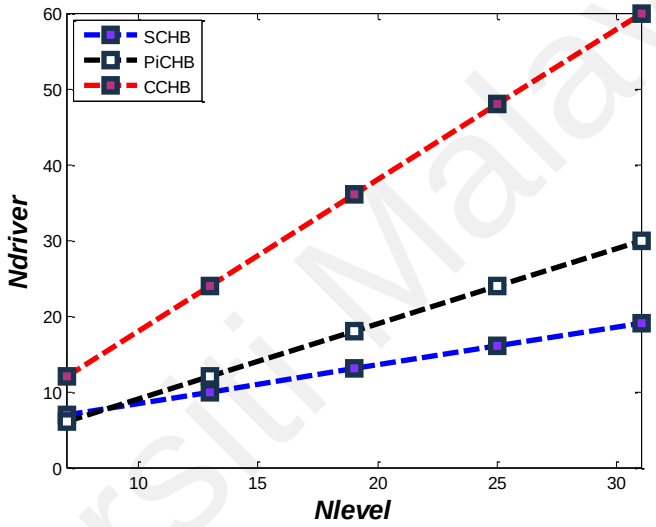
$$N_{driver} = 2a(b) \tag{3.13}$$

$$N_{IGBT} = 2a(b + 1) \tag{3.14}$$

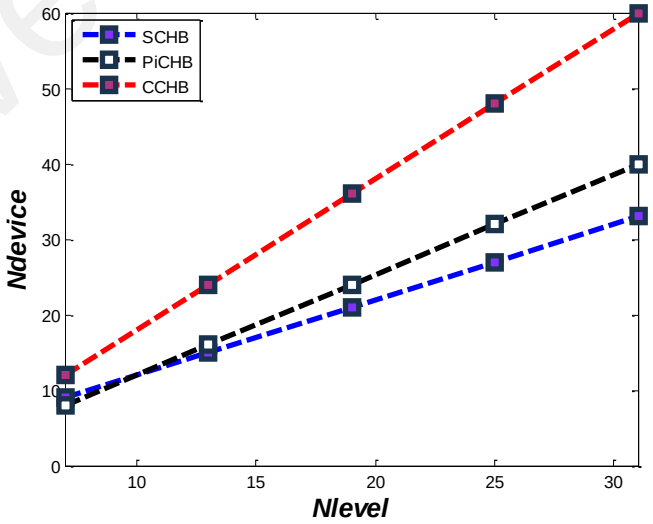
where V_c is voltage on each capacitor, N_{level} is the number of output-voltage levels, N_{IGBT} semiconductor switches, N_{driver} the number of gate drivers for the semiconductor switches, b capacitors in each cascade and a the number of cascades.



a) N_{IGBT}

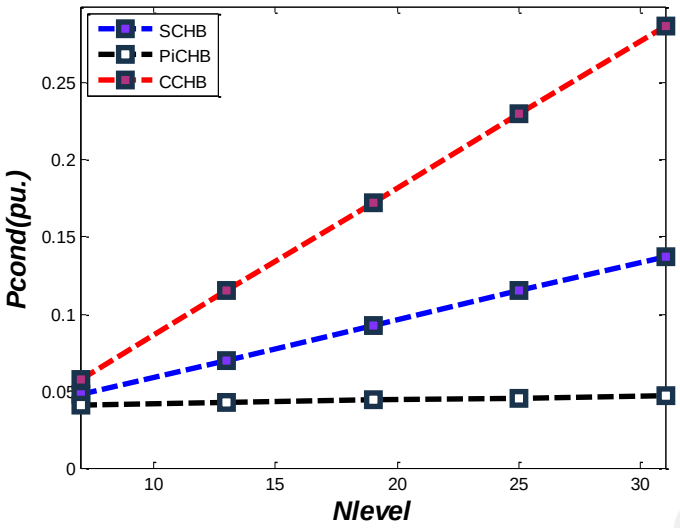


b) N_{driver}

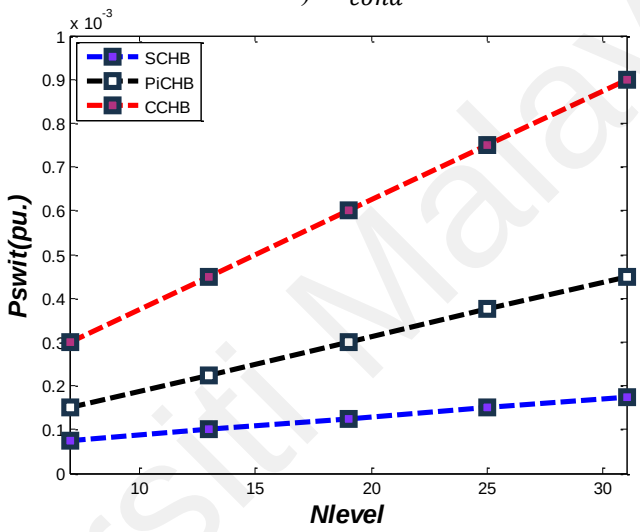


c) N_{device}

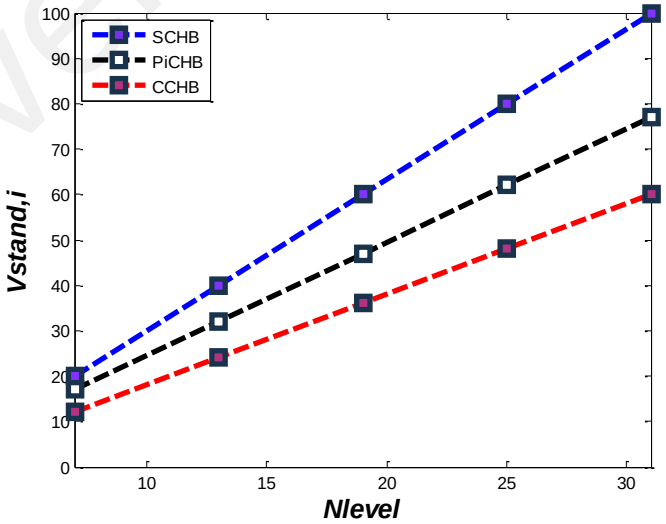
Figure 3.8: Comparative Analysis for PiCHB against SCHB and CCHB for (a) $\boldsymbol{N_{IGBT}}$, (b) $\boldsymbol{N_{driver}}$, (c) $\boldsymbol{N_{device}}$, (d) $\boldsymbol{P_{cond}}$, (e) $\boldsymbol{P_{swit}}$ (f) $\boldsymbol{V_{stand,i}}$ (g) CF and (h) Range of weight factor Vs Maximum Number of Capacitors



d) P_{cond}

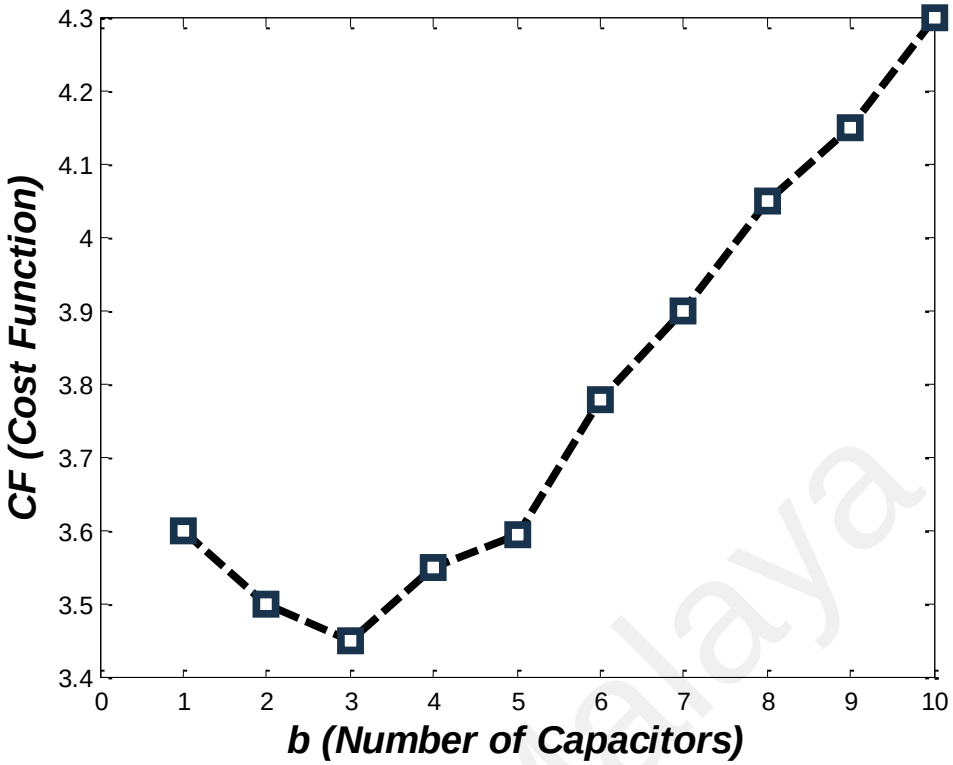


e) P_{swit}

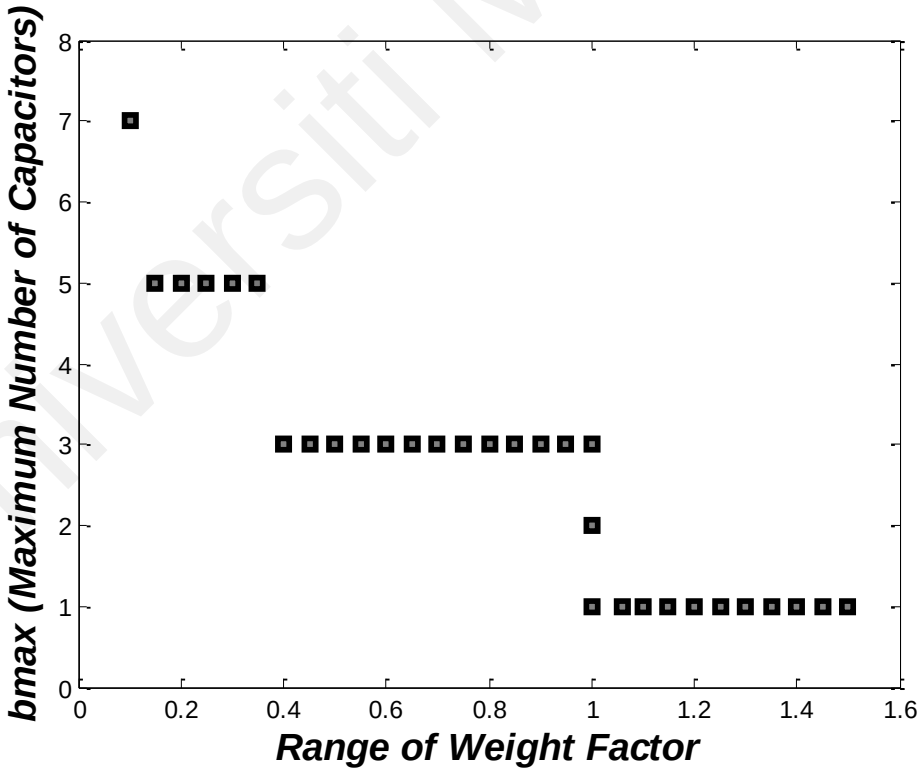


f) $V_{stand,i}$

Figure 3.8, continued



g) CF



h) Range of weight factor Vs Maximum Number of Capacitors

Figure 3.8, continued

For the consideration when $b = 3$, Figure 3.8(a) presents the graphical plot of N_{level} against N_{IGBT}, Figure 3.8(b) the plot of N_{level} against N_{driver} and Figure 3.8(c) the plot of N_{level} against N_{device}, while comparing the PiCHB topology with the Symmetric Switch Capacitor H-Bridge Topology (SCHB) (Samanbakhsh & Taheri, 2016) and the Conventional Symmetric Cascaded H-Bridge (CCHB). For PiCHB, 16 switches utilized 12 gate drivers. As, one bidirectional switch utilizes one gate driver (Ebrahimi, Babaei, & Gharehpetian, 2012).

For PiCHB the power loss during conduction (P_{cond}) is determined by the product of the ON-state $V_{on}(t)$ voltage drop by the current $I(t)$ that flows through the device as (Ebrahimi et al., 2012):

$$P_{cond} = V_{on}(t) \cdot I(t) \tag{3.15}$$

Conduction losses of semiconductor devices namely transistor $P_{cond,T}$ and diode $P_{cond,D}$ are:

$$P_{cond,T} = \left[V_{on,T}(t) + R_T \cdot I^{\beta}(t)\right] \cdot I(t) \tag{3.16}$$

$$P_{cond,D} = \left[V_{on,D}(t) + R_D \cdot I(t)\right] \cdot I(t) \tag{3.17}$$

where β remains constant, and the equivalent resistance of the transistor and diode are represented as R_T and R_D, respectively. For PiCHB the conduction power loss of the bidirectional switches ($P_{cond,B}$) is given by:

$$P_{cond,B} = \frac{1}{\pi}\int_0^{\pi}\left[V_{on,T} + V_{on,D} + R_T \cdot I^{\beta}(t) + R_D \cdot I(t)\right] \times I(t) d(\omega t) \tag{3.18}$$

With thirteen-level output of the PiCHB, the output current is considered to be almost sinusoidal.

$$I(t) = I_p \sin(\omega t) \tag{3.19}$$

Therefore,

$$P_{cond,B} = \frac{2}{\pi} I_P \left[V_{on,T} + V_{on,D}\right] + ½R_D \cdot I_P^2 + \frac{R_T \cdot I_P^{\beta+1}}{\pi} \int_0^{\pi} \sin^{\beta+1}(\omega t) d(\omega t) \tag{3.20}$$

For PiCHB the conduction power loss of the unidirectional switches ($P_{cond,U}$) is given by:

$$P_{cond,U} = \frac{1}{\pi}\left[\int_0^{\varphi} P_{cond,D} d(\omega t) + \int_{\varphi}^{\pi} P_{cond,T} d(\omega t)\right] = \frac{1}{\pi}\Big[V_{on,D} I_P (1 - \cos(\varphi)) + ¼R_D \cdot I_P^2 (2\varphi - \sin(2\varphi)) + (V_{on,T} I_P (1 + \cos(\varphi)) + R_T I_P^{\beta+1} \int_{\varphi}^{\pi} \sin^{\beta+1}(\omega t) d(\omega t))\Big] \tag{3.21}$$

Hence, the total power conduction losses (P_{cond}) are:

$$P_{cond} = P_{cond,B} + P_{cond,U} \tag{3.22}$$

To determine the switching losses, the energy loss of an IGBT during turn ON-time (E_{on}) and turn OFF-time (E_{off}) are calculated by (Ebrahimi et al., 2012):

$$E_{off} = \int_0^{t_{off}} V(t).I(t) dt$$

$$= \int_0^{t_{off}} \left[\left(\frac{V_{IGBT} t}{t_{off}}\right)\left(-\frac{I(t - t_{off})}{t_{off}}\right)\right] dt$$

$$E_{off} = ⅙ V_{IGBT} I t_{off} \tag{3.23}$$

where t_{off} is the switch turn-off time, I is the ON-time current and V_{IGBT} is the OFF-time voltage. E_{on} is:

$$E_{on} = \int_0^{t_{on}} V(t).I(t)dt$$

$$= \int_0^{t_{on}} \left[\left(\frac{V_{IGBT}t}{t_{on}}\right)\left(-\frac{I(t-t_{on})}{t_{on}}\right)\right] dt$$

$$= ⅙V_{IGBT}It_{on} \quad (3.24)$$

For PiCHB, From (3.23) and (3.24), the average switching power loss for a bidirectional switch ($P_{swit,B}$) is:

$$P_{swit,B} = 2 \times 2f\left[\sum_{i=1}^{n}\left(E_{off} + E_{on}\right)\right]$$

$$= \frac{2}{3}fI\left(t_{on} + t_{off}\right)\sum_{i=1}^{n}\left(V_{IGBT,i}\right) \quad (3.25)$$

For a full bridge, the mean switching power loss ($P_{swit,H}$) is:

$$P_{swit,H} = 2f \times \left(E_{off} + E_{on}\right) = \frac{1}{3}fI\left(t_{on} + t_{off}\right)V_{IGBT} \quad (3.26)$$

Therefore, the total switching loss of the PiCHB (P_{swit}) is:

$$P_{swit} = P_{swit,B} + P_{swit,H} \quad (3.27)$$

Considering the CCHB, PiCHB also offers higher levels of output-voltage at reduced switching losses, number of switches and gate drivers. However, even with PiCHB, SCHB can provide higher output-voltage levels at fewer numbers of switches and gate drivers, yet the SCHB has higher switching losses, resulting into higher standing voltage on the switches. The standing voltage of the PiCHB can be attained as:

$$V_{out,m} = abV_c \quad (3.28)$$

$$V_{stand} = \left(\frac{3b^2+2b-1}{8} + 4b\right)V_c \qquad for \qquad b: odd \quad (3.29)$$

$$V_{stand,i} = aV_{stand} \tag{3.30}$$

$V_{out,o}$ is the optimum output voltage, V_{stand} semiconductor switches withstanding voltage of each cascade, $V_{stand,i}$ is the complete standing voltage of the switches utilized by the inverter, CF is the cost function and the weight factor of $V_{stand,i}$ is represented by α, against N_{IGBT}. Figure 3.8(d) presents the graphical plot of N_{level} against P_{cond}, Figure 3.8(e) is the plot of N_{level} against P_{swit} (t_{off} and t_{on} are considered to be $2\mu s$), and Figure 3.8(f) is the plot of N_{level} against $V_{stand,i}$. Comparing PiCHB with CCHB, the proposed topology offers higher levels of output-voltage at reduced power losses, number of switches and gate drivers. However, considering the parameter of total standing voltage on the semiconductor switches the CCHB offers the best characteristics. Comparing PiCHB with SCHB, the SCHB can provide higher output-voltage levels with fewer switches and gate drivers, yet the SCHB has a considerable number of devices (transistors and diodes), higher conduction losses and a higher switch standing voltage, making it less reliable. $V_{out,m}$ is the maximum output voltage, V_{stand} semiconductor switches standing voltage of each cascade and $V_{stand,i}$ standing voltage of the inverter. As observed from above equations greater number of capacitors are appropriate while considering the number of IGBTs. However, while taking into consideration the standing voltage, lesser number of capacitors is preferable. Hence, a tradeoff exists between the semiconductor switches and standing voltage. To ascertain best performance, the cost function (CF) can be utilized:

$$CF = N_{IGBT} + \alpha V_{stand,i} \tag{3.31}$$

Where, the weight factor (parameter dependent on the semiconductor switch characteristics) of the $V_{stand,i}$ is represented by α, against N_{IGBT}. When N_{IGBT} is vital, α should be kept low. By contrast, if the $V_{stand,i}$ is more important, then α should be higher.

For PiCHB, two cascades and three capacitors in each cascade are taken into consideration. Figure 3.8(g) displays the variation of CF against b or number of capacitors (NC) for α = 0.8. It remains quite evident from the plot that the CF is least when $b = 3$. Figure 3.8(h) presents the maximum number of capacitors against α. b_{max} offers a correspondence with reduced CF against a wide range of α values. Figure 3.8(h), affirms the tradeoff between the semiconductor switches and the standing voltage. As CCHB utilize only one capacitor, it remains most favorable while considering the with stand voltage and worst when considering N_{IGBT} employed. Proposed TCHB and PiCHB provide a compromise between the two. So, based on the application and practical limitations the required topology can be employed (Ali et al., 2018).

Taking into consideration the CF variations, the proposed inverter was established. It comprises of two H-bridges, two π-Type bidirectional switches, and six voltage-dividing capacitors. Each cascade possesses one π-type bidirectional switch and three capacitors, as presented in Figure 3.7. Reduced switching losses, diodes, gate drives and N_{IGBT} make the PiCHB topology an effective choice. In order to boost the voltage to the grid requirements, two Dc–Dc boost converters were utilized. The converters were placed between the PV arrays and each cascade of the inverter. A filtering inductance L_f was employed at the output. By utilizing a suitable PWM control for the cascaded inverter, thirteen output-voltage levels (2Vdc, 5Vdc/3, 4Vdc/3, Vdc, 2Vdc/3, Vdc/3, 0, −Vdc/3, −2Vdc/3, −Vdc, −4Vdc/3, −5Vdc/3, −2Vdc) were produced.

3.2.2.3 Principles of operation

Thirteen switching states define the operation for PiCHB, as presented in Figure 3.9(a)–(f) for $V_{out} > 0$ and in Figure 3.9(g)-(l) for $V_{out} < 0$, with Figure 3.9 m and n displaying the zero and zero* state, respectively. Table 3.3 shows the input-capacitor-current, linked with output-current, against switching states. For Figure 3.9, the red track

represents the current path for the specific mode of operation to attain the desired maximum voltage output. Required output-voltage with thirteen-levels was attained as:

1) 2Vdc positive output - S1, S4, S7 and S10 are ON. S1 forms the path to connect the load positive terminal to Vdc1, and S10 connects the load negative terminal to ground of Vdc2. Further, S7 forms the path to connect the load to Vdc2, and via S4 completes the current path. The voltage applied to the load terminals is 2Vdc. Current path in red of Figure 3.9(a) displays when the output voltage is 2Vdc.

2) 5Vdc/3 positive output - The bidirectional T-type switch formed by B11 is ON. Here, switching states for the first cascade remain unchanged from the preceding state. However, the load negative terminal, through S10, connects to the ground of V_{dc2} and the current completes its path through the bidirectional switch, which offers a trimmed voltage. Figure 3.9(b) shows the current paths in red when the output voltage is 5Vdc/3.

3) 4Vdc/3 positive output - S1, S4, S10 and B12 are ON. The operation remains similar to the preceding, but with B12 in operation. Figure 3.9(c) presents current path in red when the output voltage is 4Vdc/3.

4) Vdc positive output - S1, S4, S9 and S10 are ON. Switches S9 and S10 form a closed circuit path through the second cascade. Figure 3.9(d) presents current path in red when the output voltage is Vdc.

5) 2Vdc/3 positive output - Bidirectional T-type switch formed by B5 is ON,. Here, switching states for the second cascade remain unchanged from the preceding state. The load positive terminal connects to V_{dc1} via the bidirectional switch B5 offering a trimmed voltage. Figure 3.9(e) shows the current paths in red when the output voltage is 2Vdc/3.

6) Vdc/3 positive output - Bidirectional T-type switch formed by B6 is ON. Here, switching states for the second cascade remain unchanged from the preceding state. The load positive terminal connects to V_{dc1} via the bidirectional switch B6 offering a trimmed voltage. Figure 3.9(f) shows the current paths in red when the output voltage is Vdc/3.

7) -Vdc/3 negative output - S2, B5, S7 and S8 are ON. However, S7 and S8 offer a short circuit path in the second cascade. The load terminal connects to V_{dc1} via the bidirectional switch B5, completing its path through S2. Figure 3.9(g) shows the current paths in red when the output voltage is -Vdc/3.

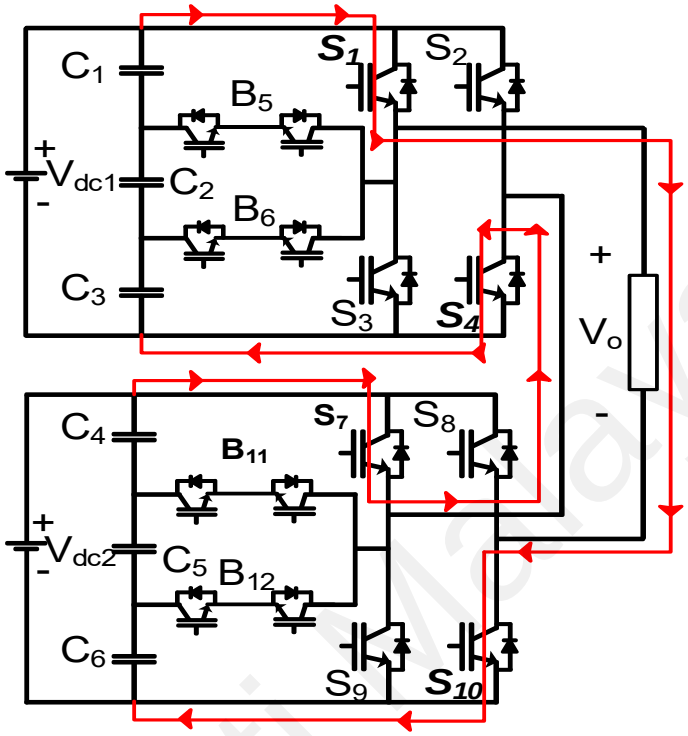
8) -2Vdc/3 negative output - S2, B6, S7 and S8 are ON. Here, switching states for the second cascade remain unchanged from the preceding state. The current passing from S2 completes its path through B6, providing a trimmed output-voltage. Figure 3.9(h) shows the current paths in red when the output voltage is -2Vdc/3.

9) -Vdc negative output - S2, S3, S7 and S8 are ON. Switches S7 and S8 form a closed circuit path through the second cascade. Figure 3.9(i) presents current path in red when the output voltage is -Vdc.

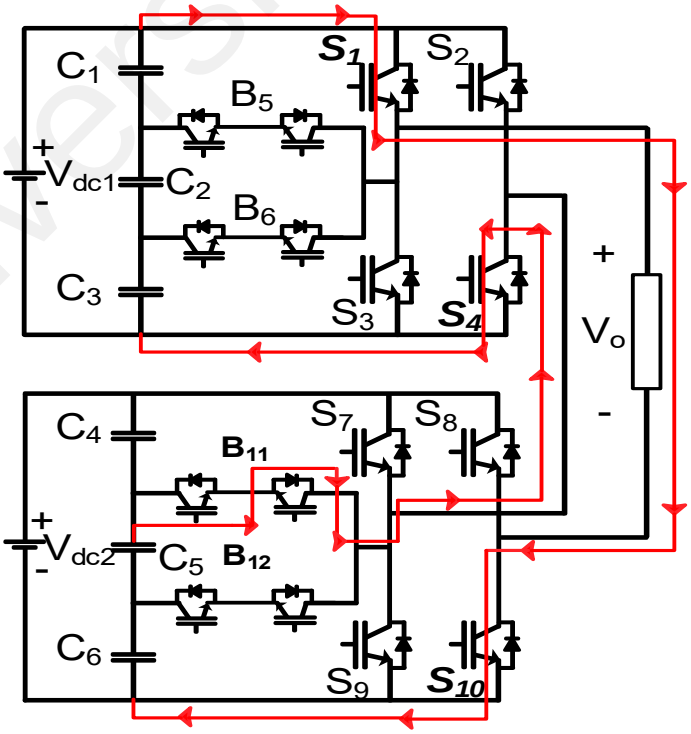
10) -4Vdc/3 negative output - S2, S3, S8 and B11 are ON. With S2 and S3 forming short circuit path in the first cascade the load negative terminal, connects to V_{dc2} via the bidirectional switch B11, which offers a trimmed voltage. Figure 3.9(j) shows the current paths in red when the output voltage is -4Vdc/3.

11) -5Vdc/3 negative output - S2, S3, S8 and B12 are ON,. The operation remains similar to the preceding, but with B12 in operation. Figure 3.9(k) presents current path in red when the output voltage is -5Vdc/3.

12) -2Vdc negative output - S2, S3, S8 and S9 are ON. Here, S3 connects the load positive terminal to Vdc1, and S8 connects the load negative terminal to Vdc2. Figure 3.9(l) shows the current paths in red when the output voltage is -2Vdc.

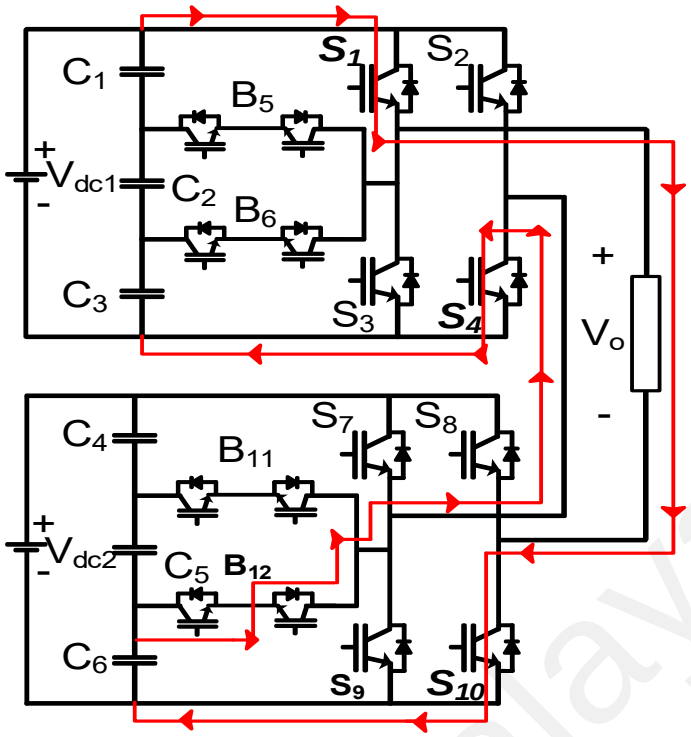


a) 2Vdc (S1, S4, S7 and S10 are ON)

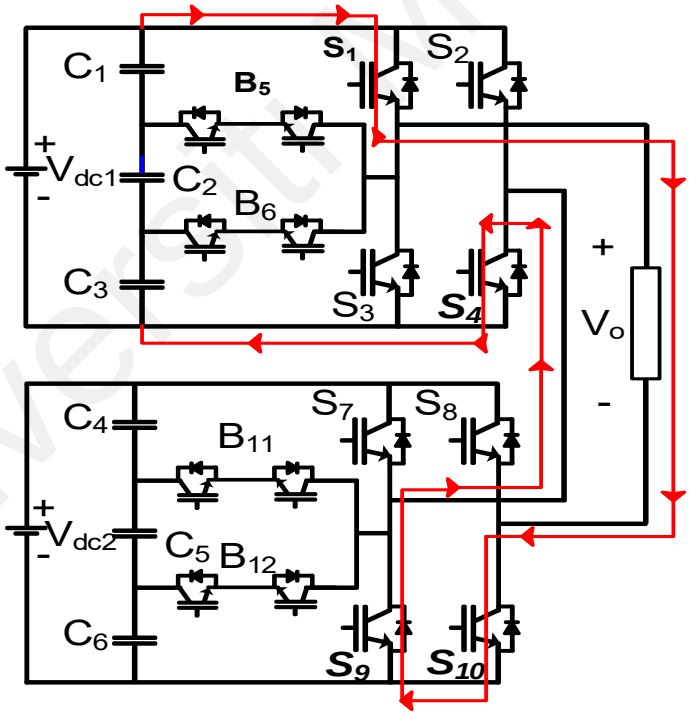


b) 5Vdc/3 (S1, S4, S10 and bidirectional T-type switch by B11 are ON)

Figure 3.9: (a-f) Modes of Operation for $V_{out} > 0$, (g-l) Modes of Operation for $V_{out} < 0$ and (m-n) Modes of Operation for Zero and Zero*

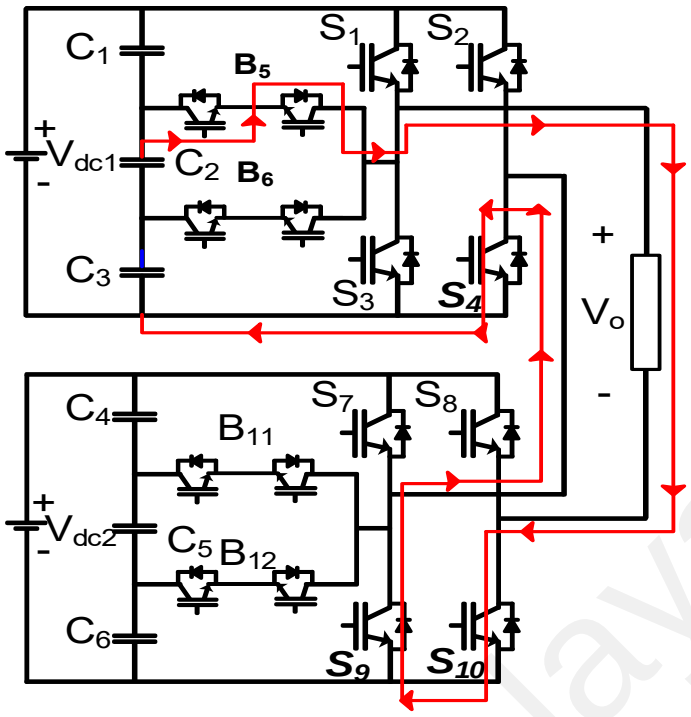


c) 4Vdc/3 (S1, S4, S10 and B12 are ON)

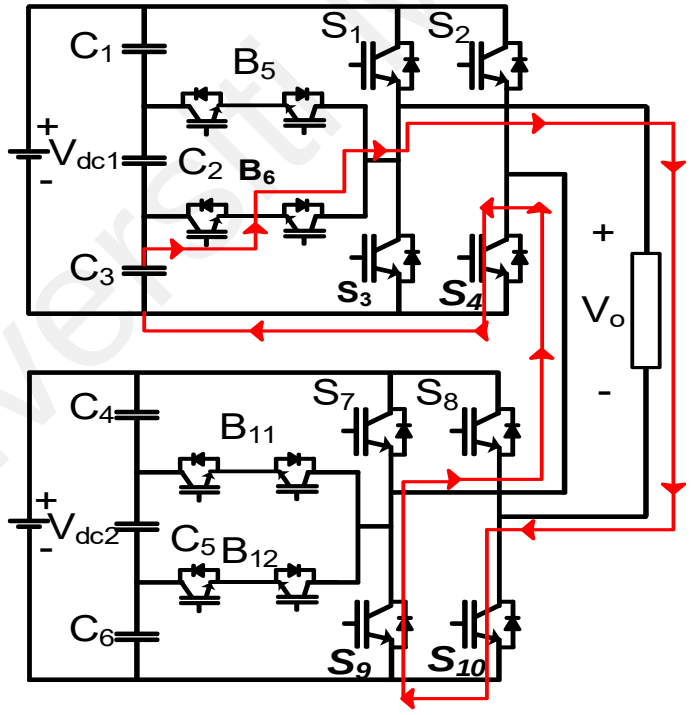


d) Vdc (S1, S4, S9 and S10 are ON)

Figure 3.9, continued

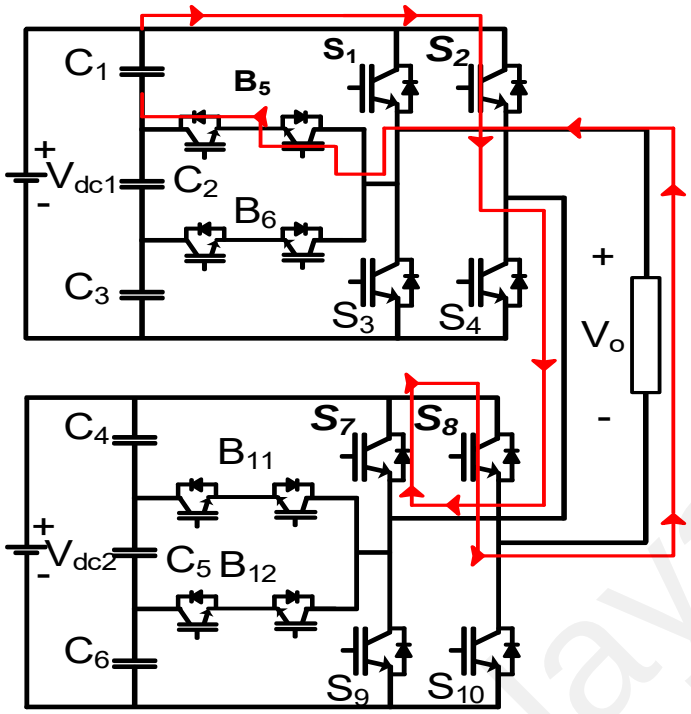


e) 2Vdc/3 (S4, S9, S10 and the bidirectional T-type switch formed by B5 is ON)

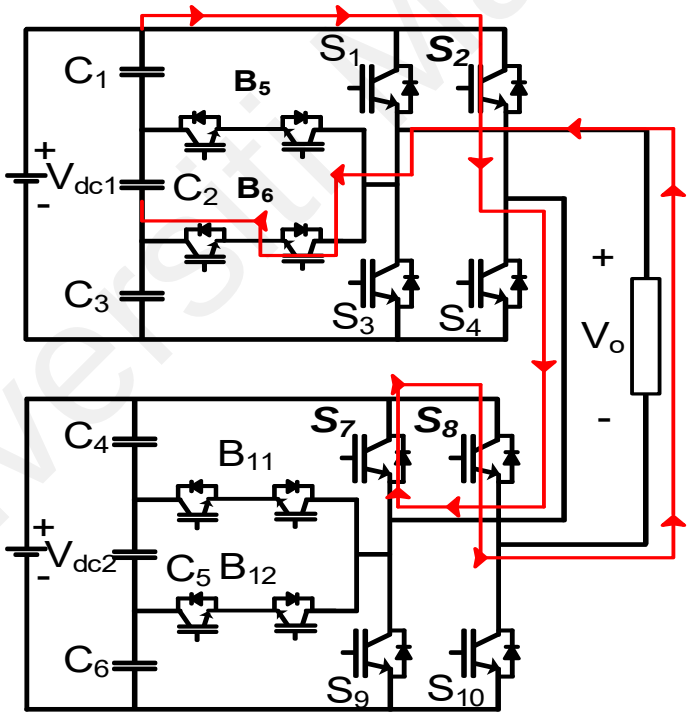


f) Vdc/3 (S4, S9, S10 and the bidirectional T-type switch formed by B6 is ON)

Figure 3.9, continued

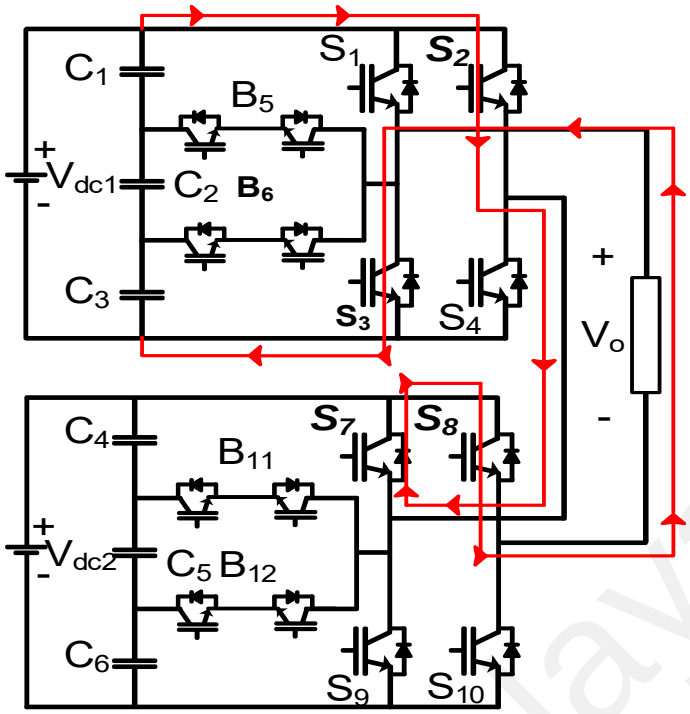


g) –Vdc/3 (S2, B5, S7 and S8 are ON)

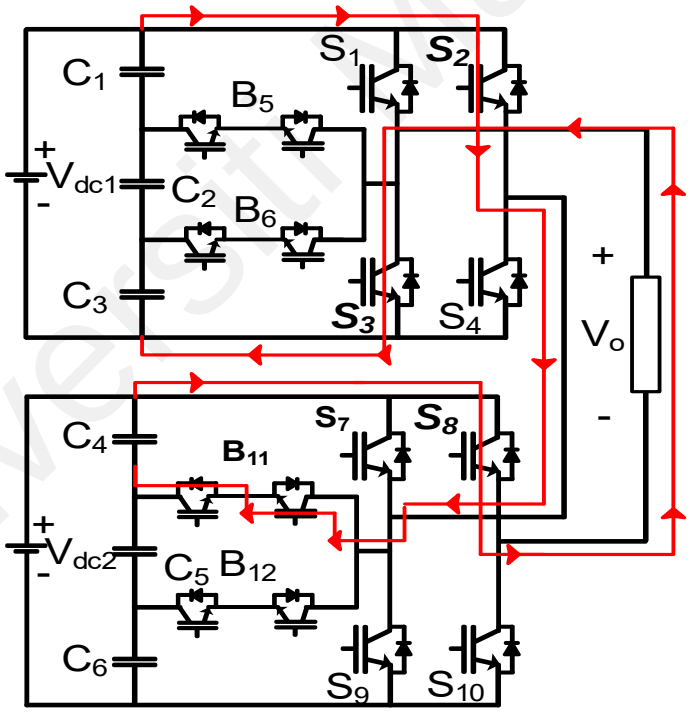


h) –2Vdc/3 (S2, B6, S7 and S8 are ON)

Figure 3.9, continued

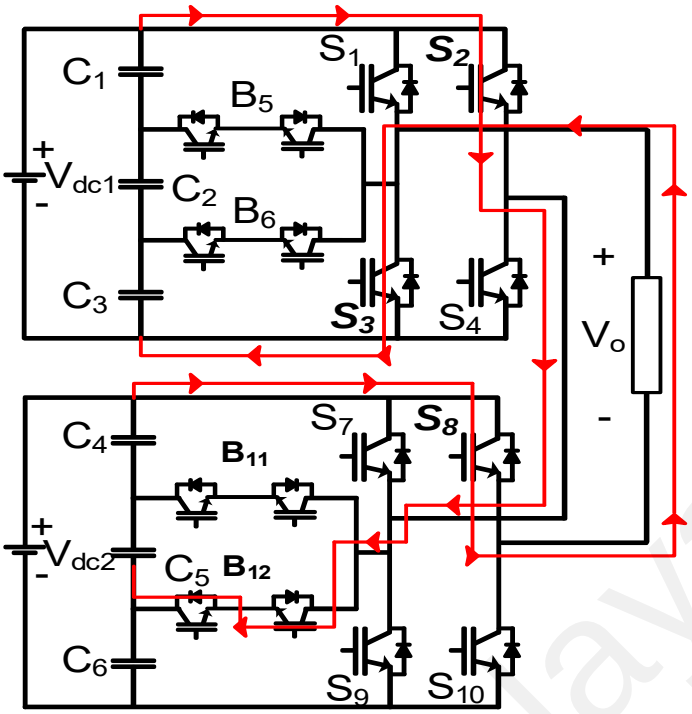


i) –Vdc (S2, S3, S7 and S8 are ON)

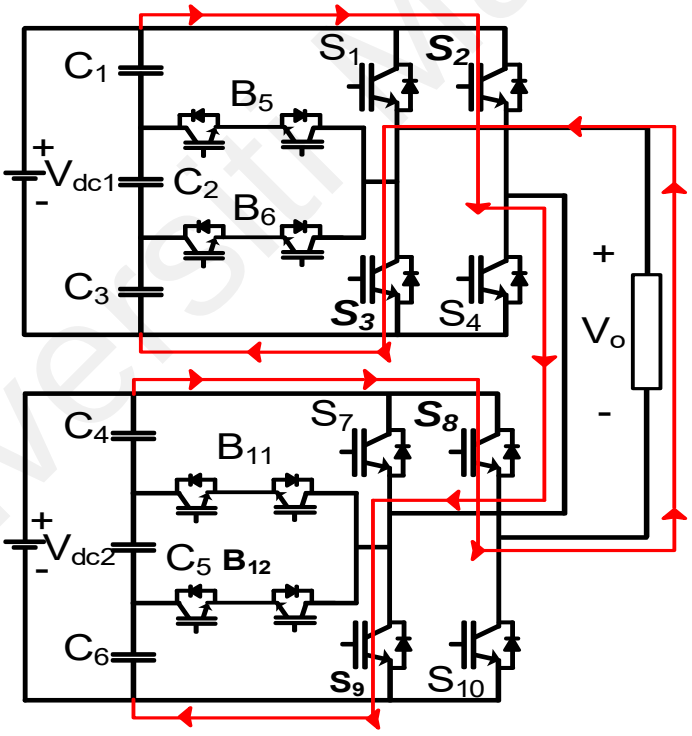


j) –4Vdc/3 (S2, S3, S8 and B11 are ON)

Figure 3.9, continued

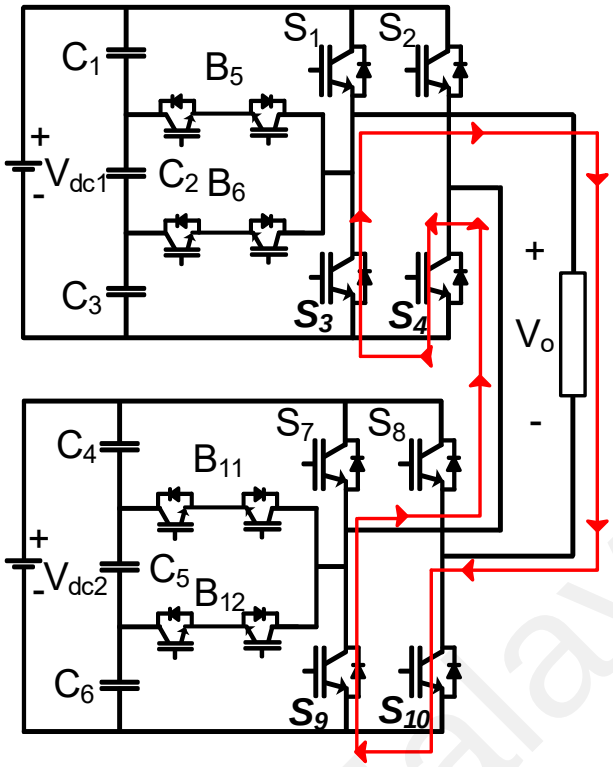


k) –5Vdc/3 (S2, S3, S8 and B12 are ON)

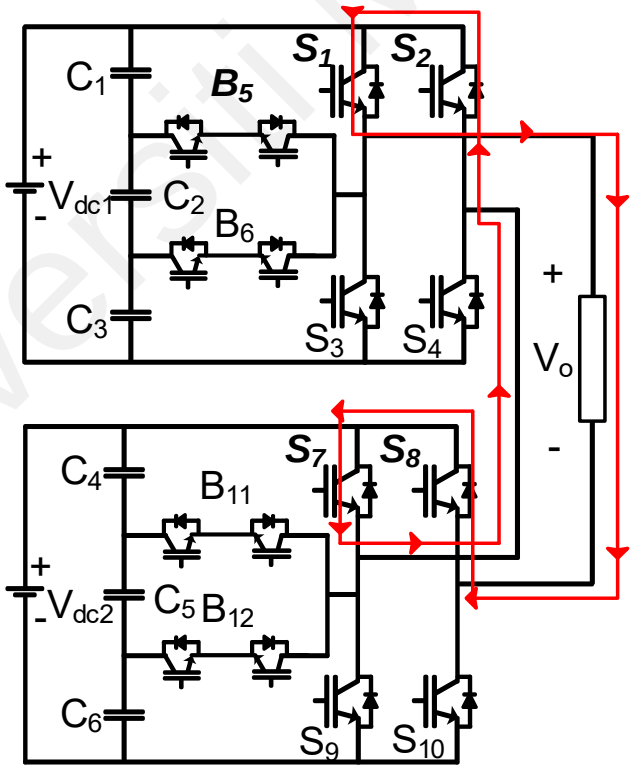


l) –2Vdc (S2, S3, S8 and S9 are ON)

Figure 3.9, continued



m) Zero (S3, S4, S9 and S10 are ON)



n) Zero* (S1, S2, S7 and S8 are ON)

Figure 3.9, continued

Table 3.3: Input Capacitor Current, Linked with the Output Current, Against Switching States for PiCHB

Iout	S1	S2	S3	S4	B5	B6	S7	S8	S9	S10	B11	B12	Vinv
Ic3 = -Iout ^ 0 Ic1=Ic2=Ic4=Ic5=Ic6=0	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	$\frac{Vdc}{3}$
Ic2 = -Iout ^ 0 Ic1=Ic4=Ic5= Ic6=0, Ic3=-Iout	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	$\frac{2Vdc}{3}$
Ic1 = -Iout ^ 0 Ic4=Ic5=IC6=0, Ic2=Ic3=-Iout	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	Vdc
Ic6 = -Iout ^ 0 Ic4=Ic5=0, Ic1=Ic2=Ic3=-Iout	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	$\frac{4Vdc}{3}$
Ic5 = -Iout ^ 0 Ic4=0, Ic1=Ic2=Ic3=Ic6=-Iout	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	$\frac{5Vdc}{3}$
Ic4 = -Iout ^ 0 Ic1=Ic2=Ic3=Ic5=Ic6=-Iout	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	$2Vdc$
Ic1=Ic2=Ic3=Ic4=0	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	0
Ic4=Ic3=Ic2=Ic1=0*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	$0*$
Ic6 = Iout ^ 0 Ic1=Ic2=Ic3=Ic4=Ic5=Iout	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	$-2Vdc$
Ic5 = Iout ^ 0 Ic6=0, Ic1=Ic2=Ic3=Ic4=Iout	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	$-\frac{5Vdc}{3}$
Ic4 = Iout ^ 0 Ic5=Ic6=0, Ic1=Ic2=Ic3=Iout	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	$-\frac{4Vdc}{3}$
Ic3 = Iout ^ 0 Ic4=Ic5=Ic6=0, Ic1=Ic2=Iout	OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	$-Vdc$
Ic2 = Iout ^ 0 Ic3=Ic4=Ic5=Ic6=0, Ic1=Iout	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	$-\frac{2Vdc}{3}$
Ic1 = Iout ^ 0 Ic2=Ic3=Ic4=Ic5=Ic6=0	OFF	ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	$-\frac{Vdc}{3}$

13) Zero output: Here either the switches S3, S4, S9 & S10 are ON presented in Figure 3.9(m) for zero state, or S1, S2, S7 & S8 are ON presented in Figure 3.9(n) for zero* state, making the two switching combinations for the zero state where the load line is short-circuited. Therefore, the load terminals is applied with zero voltage.

3.2.2.4 PWM method involved

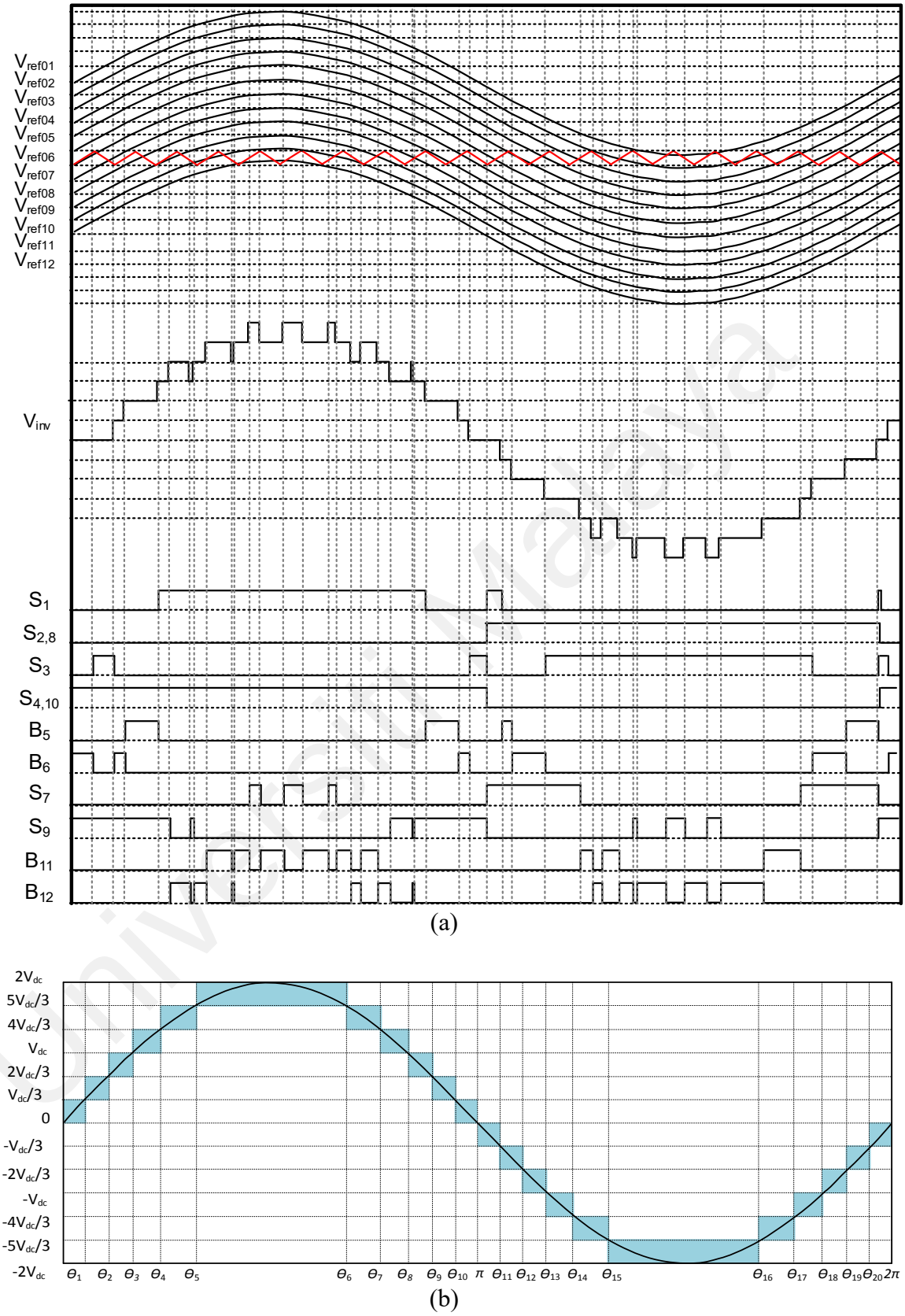


Figure 3.10: Thirteen-level (a) Switching Signals and (b) Inverter Output-Voltage

Twelve reference signals, operating at equivalent amplitude, frequency and phase, excepting an offset value were intersected against the carrier. Figure 3.10 presents the Thirteen-Level Inverter Output-Voltage V_{inv}. Here, S2, S4, S8 and S10 would operate at fundamental frequency and Switches S1, S3, B5, B6, S7, S9, B11, and B12 at the frequency of the carrier.

Taking into consideration the switching modulation strategy as shown in Figures 3.9 and 3.10, PiCHB output-voltage can be modelled as:

$$V_{out} = V_{c1}[(S_1)(1-S_2)(1-B_5)(1-B_6) - (S_2)(1-S_1)(1-B_6)] + V_{c2}[(S_4)(1-S_3)(1-B_6) - (S_2)(1-S_1)(1-B_5)] + V_{c3}[(S_4)(1-S_3)(1-B_5) - (S_3)(1-S_4)(1-B_5)(1-B_6)] + V_{c4}[(S_7)(1-S_8)(1-B_{11})(1-B_{12}) - (S_8)(1-S_7)(1-B_{12})] + V_{c5}[(S_{10})(1-S_9)(1-B_{12}) - (S_8)(1-S_7)(1-B_{11})] + V_{c6}[(S_{10})(1-S_9)(1-B_{11}) - (S_9)(1-S_{10})(1-B_{11})(1-B_{12})] \quad (3.32)$$

As,

$$(S_2) = not(S_4), (S_1) = not(S_3), (1-B_5)(1-B_6) = (S_1) + (S_3), (1-B_{11})(1-B_{12}) = (S_7) + (S_9) \quad (3.33)$$

So,

$$V_{out} = V_{c1}[(S_1)(S_4)(S_1+S_3) - (S_2)(S_3)(1-B_6)] + V_{c2}[(S_4)(S_1)(1-B_6) - (S_2)(S_3)(1-B_5)] + V_{c3}[(S_4)(S_1)(1-B_5) - (S_3)(S_2)(S_1+S_3)] + V_{c4}[(S_7)(S_{10})(S_7+S_9) - (S_8)(S_9)(1-B_{12})] + V_{c5}[(S_{10})(S_7)(1-B_{12}) -$$

$$(S_8)(S_9)(1 - B_{11})] + V_{c6}[(S_{10})(S_7)(1 - B_{11}) - (S_9)(S_8)(S_7 + S_9)]$$

(3.34)

For all high cases, when A=1:

$$(1 - B_5)(S_1) = (S_1), (1 - B_5)(S_3) = (S_3), (1 - B_5)(S_7) = (S_7), (1 - B_5)(S_9) = (S_9)$$

Considering a similar case for $(1 - B_n)$, Therefore,

$$V_{out} = V_{c1}[(S_1)(S_4)(S_1 + S_3) - (S_2)(S_3)] + V_{c2}[(S_4)(S_1) - (S_2)(S_3)] + V_{c3}[(S_4)(S_1) - (S_3)(S_2)(S_1 + S_3)] + V_{c4}[(S_7)(S_{10})(S_7 + S_9) - (S_8)(S_9)] + V_{c5}[(S_{10})(S_7) - (S_8)(S_9)] + V_{c6}[(S_{10})(S_7) - (S_9)(S_8)(S_7 + S_9)] \quad (3.35)$$

$$V_{outp} = V_{c1}[(S_1)(S_4)(S_1 + S_3)] + V_{c2}[(S_4)(S_1)] + V_{c3}[(S_4)(S_1)] + V_{c4}[(S_7)(S_{10})(S_7 + S_9)] + V_{c5}[(S_{10})(S_7)] + V_{c6}[(S_{10})(S_7)] \quad (3.36)$$

$$V_{outn} = V_{c1}[-(S_2)(S_3)] + V_{c2}[-(S_2)(S_3)] + V_{c3}[-(S_3)(S_2)(S_1 + S_3)] + V_{c4}[-(S_8)(S_9)] + V_{c5}[-(S_8)(S_9)] + V_{c6}[-(S_9)(S_8)(S_7 + S_9)] \quad (3.37)$$

Considering equation (3.35), the switching frequency of switches $S_2 = S_4 = S_8 = S_{10}$, is made to operate at fundamental frequency, while rest of the switches operate at switching frequency of the output voltage. In addition, S_1 and S_3 are 180 degrees phase shifted, similarly S_7 and S_9 are phase shifted. Equations (3.36) and consequently (3.37) offer complementary functions where each function is represented as $f_n =$

$(S_i)(S_j), where\ i = 2,4,8,10\ and\ j = 1,3,7,9$. However, in (3.36) to maintain Vc1 and Vc4 additional switching is required and for (3.37) additional switching is required for maintaining Vc3 and Vc6. The additional switching causes a rise of a component frequency at the switching frequency of the output voltage. Such a complementary switching, due to the rise of an additional component frequency, results for imbalance of the DC-Link capacitor voltage.

In order to overcome this issue, RLC passive balancing circuit has been employed. The load current or the current through the passive balancing (RLC) branch contributes to attain BVS at the DC-link capacitors by suppressing such a component of frequency. Here, the resonant frequency is required to be equal to the component frequency. The resistor R_t is employed to evade unwanted oscillations in the system due to the balancing circuit.

Therefore, the balancing RLC circuit current, with a similar resonant frequency as the switching frequency, and the load current contribute to compensate the extra component of frequency at the switching frequency of the PiCHB. For all modes of operation such roots are obtained. Figure 3.11 presents the balanced low-frequency inverter output-voltage with switching angles for the PiCHB inverter topology.

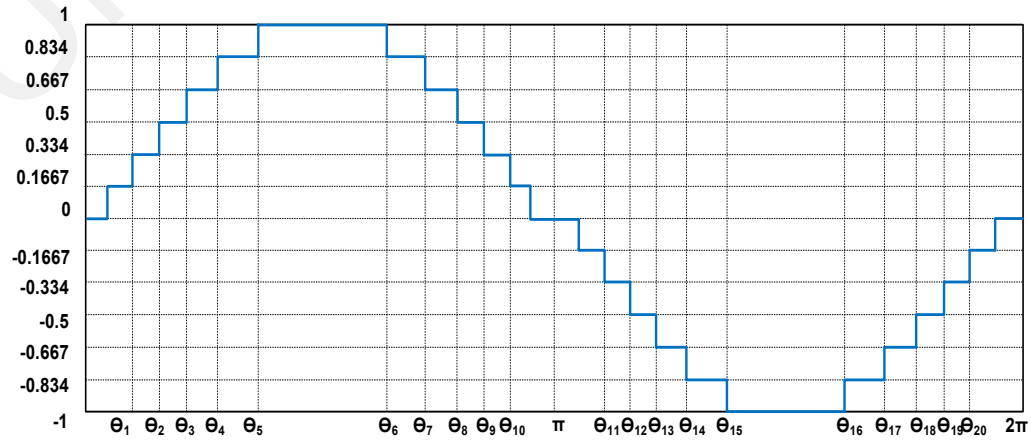


Figure 3.11: Inverter Output-voltage of the proposed PiCHB inverter

3.3 Proposed Modified Incremental (mINC) Technique

The adaptive term involving a ratio of power change over voltage change (dP_{PV}/dV_{PV}) has been utilizing for adaptive stepping in various conventional MPPT techniques. In addition, power change over current change (dP_{PV}/dI_{PV}) or power change over duty change (dP_{PV}/dD) has also been used. By contrast, in order to reduce the complexity of the adaptive stepping the proposed technique offers a term utilizing only power change (dP_{PV}). The proposed adaptive step decreases complexity, offers better transient response, and responds to dynamic changes in ambient irradiance in an efficient manner. It has been applied with conventional MPPT techniques, particularly on modified Incremental Conductance (mINC) method. Flowchart of mINC has been presented in Figure 3.12. In addition, this technique offers simple implementation by eradicating the division complexity of INC to mINC, concluding that INC is a specific implementation of P&O (Aamir Amir et al., 2017):

$$\frac{V(\Delta I)+I(\Delta V)}{V\Delta V} = 0 \qquad \text{MPP} \tag{3.38}$$

$$\frac{V(\Delta I)+I(\Delta V)}{V\Delta V} > 0 \qquad \text{L of MPP} \tag{3.39}$$

$$\frac{V(\Delta I)+I(\Delta V)}{V\Delta V} < 0 \qquad \text{R of MPP} \tag{3.40}$$

At MPP:

$$V(\Delta I) + I(\Delta V) = 0$$

L of MPP:

$$(V(\Delta I) + I(\Delta V) > 0)\ \&\&\ (\Delta V > 0) \tag{3.41}$$

R of MPP:

$$(V(\Delta I) + I(\Delta V) > 0)\ \&\&\ (\Delta V < 0) \tag{3.42}$$

Therefore the equation for the Right of the MPP can be written as:

$$(V(\Delta I) + I(\Delta V) < 0)\ \&\&\ (\Delta V > 0) \tag{3.43}$$

Similarly, the equation for the Left of the MPP remains:

$$(V(\Delta I) + I(\Delta V) < 0)\ \&\&\ (\Delta V < 0) \tag{3.44}$$

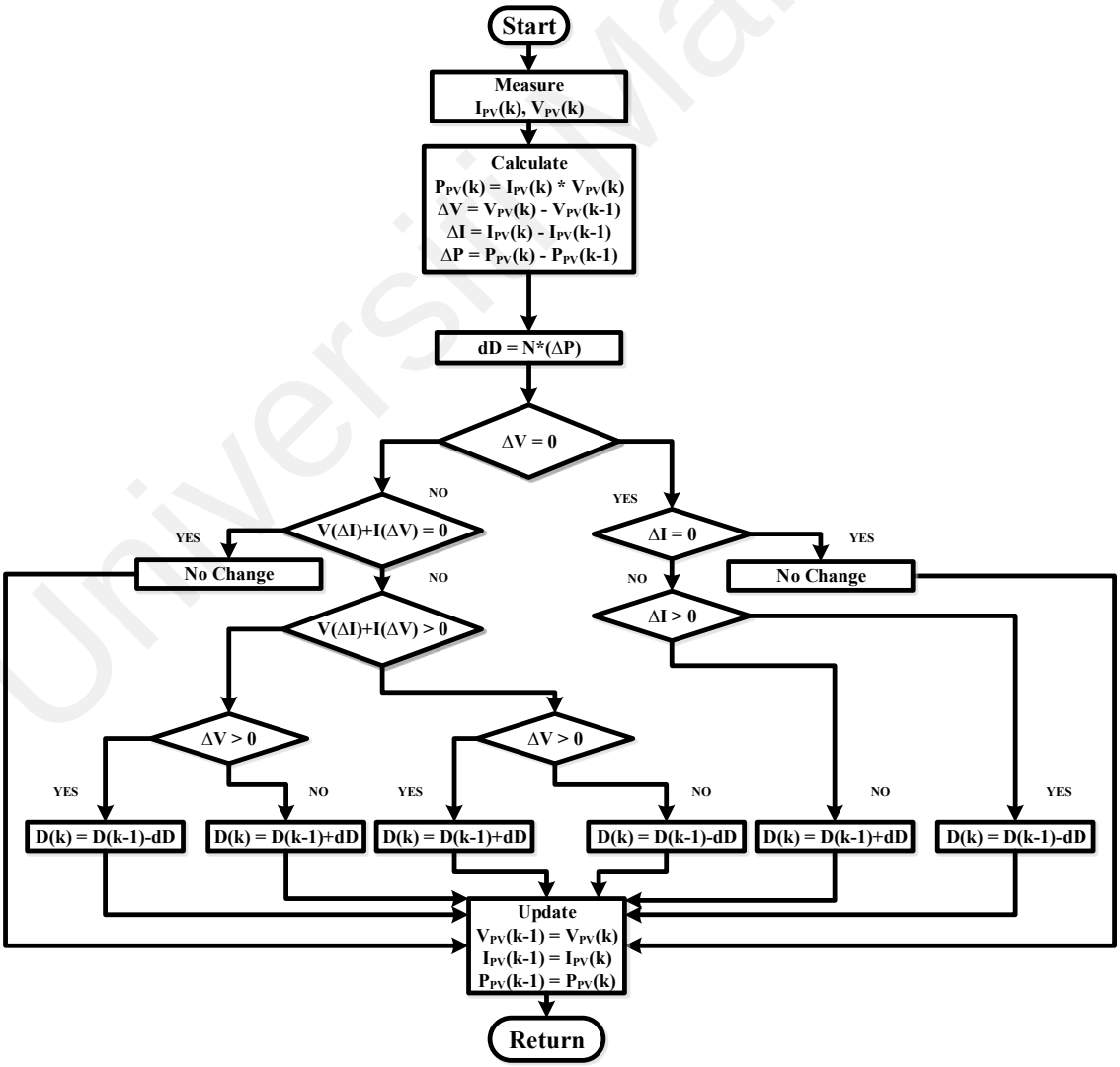


Figure 3.12: mINC Flowchart

3.4 OHESW for Low-Frequency

For TCHB and PiCHB MLI, by solving the Selective Harmonic Elimination (SHE) equations, the switching angles at the fundamental frequency can be attained. Here, the fundamental voltage is attained at the output and lower order harmonics are nearly nullified.

The Fourier series for a period function $V_o(\omega t)$ can be expressed as:

$$Vo(\omega t) = a_0 + \sum_{n=1}^{\infty}[a_n \cos(n\omega t) + b_n \sin(n\omega t)] \quad (3.45)$$

The Fourier series of odd functions contain only sine terms: $a_0 = 0$ and $a_n = 0$ for all n. The sine function is odd as,

$$b_n = \begin{cases} \frac{4}{\pi}\int_0^{\frac{\pi}{2}} V_o(\theta)\sin(n\theta)d\theta & for\ odd\ \ n \\ 0 & for\ even\ n \end{cases} \quad (3.46)$$

Therefore,

$$V_{ab}(\omega t) = \sum_{n=odd}^{\infty}[b_n \sin(n\omega t)] \quad (3.47)$$

By replacing the ωt with the desired switching angles θ_n the transcendental equations can be attained. The open bracket NRM has been used to solve non-linear equations from OHESW technique.

Solution sets are then examined for their THD, for choosing a set producing lower harmonic distortion THD by:

$$THD(\%) = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} * 100\% \quad (3.48)$$

3.4.1 Open-Bracket Technique for Optimization of Switching Angles

NRM can easily generalize the problem of optimization and finding solutions to a system of non-linear equations. NRM has been discussed in detail in chapter 2. Generally, system of nonlinear equations in s variables can be represented as:

$$\begin{aligned} f_1(\theta_1, \theta_2, \dots, \theta_s) &= b_1 \\ f_1(\theta_1, \theta_2, \dots, \theta_s) &= b_1 \\ &\vdots \\ f_1(\theta_1, \theta_2, \dots, \theta_s) &= b_s \end{aligned}$$

This can be rewritten in vector notation by:

$$F(\theta) = B(m_a) \tag{3.49}$$

Where,

$F = [f_1, f_2, \dots, f_s]^T$,

$\theta = [\theta_1, \theta_2, \dots, \theta_s]^T$,

$B = [b_1, b_2, \dots, b_s]^T$; and F, θ, B are sx1 matrices.

A system of nonlinear equations can be solved by linearization technique, where the nonlinear equations are linearized about an approximated solution. Here a non-linear equation in a single independent variable $y = f(\theta)$ is considered, starting with an estimate of θ near the root of $f(\theta) = b$. Intersection of the line tangential to the graph at this estimate with the θ axis is computed. The intersection is used as the abscissa of the new estimate. The iterative process is continued until the roots are attained.

A NRM solution to such equation can be utilized to attain the optimized switching angles in order to eliminate the odd harmonic components as follows:

1. Assume a set of random initial value for switching angles θ with $j = 0$,

   Let $\theta^0 = [\theta_1^0 \quad \theta_2^0 \quad \theta_3^0]^T$ with $0^0 < \theta_1 < \theta_2 < \theta_3 < 90^0$

2. Set $m_a = 0$

3. Calculating $F(\theta^0)$, Jacobian $J(\theta_0)$ and $B(m_a)$

   $$F(\theta^0) = \begin{bmatrix} \cos(\theta_1^0) & \cos(\theta_2^0) & \cos(\theta_3^0) \\ \cos(3\theta_1^0) & \cos(3\theta_2^0) & \cos(3\theta_3^0) \\ \cos(5\theta_1^0) & \cos(5\theta_2^0) & \cos(5\theta_3^0) \end{bmatrix} = F^0; \text{ and } B(m_a) =$$

   $[3m_a \quad 0 \quad 0]^T$

   The Jacobian matrix of the function $F(\theta)$ is

   $$J_F(\theta_1, \theta_2, \theta_3) = \left[\frac{\partial F^0}{\partial \theta}\right] = \begin{bmatrix} -\sin(\theta_1^0) & -\sin(\theta_2^0) & -\sin(\theta_3^0) \\ -3\sin(3\theta_1^0) & -3\sin(3\theta_2^0) & -3\sin(3\theta_3^0) \\ -5\sin(5\theta_1^0) & -5\sin(5\theta_2^0) & -5\sin(5\theta_3^0) \end{bmatrix}$$

4. Linearize the equation (3.49) about θ^0

   $F^0 + \left[\frac{\partial F^0}{\partial \theta}\right].d\theta^0 = B(m_a)$; and $d\theta^0 = [d\theta_1^0 \quad d\theta_2^0 \quad d\theta_3^0]^T$

5. Compute correction $d\theta^0$ during iteration, through

   $d\theta^0 = J^{-1}(\theta^0).[B(m_a) - F(\theta^0)]$, where $J^{-1}(\theta^0)$ is inverse matrix of $\left[\frac{\partial F^0}{\partial \theta}\right]$

6. Update the switching angles, i.e., $(\theta^{j+1} = \theta^j + d\theta^j)$

7. Perform a transformation of $\theta^{j+1} = cos^{-1}[abs(\cos(\theta^{j+1}))]$ to attain switching angles into a feasible range.

8. Iterate steps (3) to (7) until $d\theta^j$ is satisfied to the desired accuracy.

9. Increase m_a step by step by a fixed step, with $0 < m_a < 1$

10. Reiterate steps (2) to (9) for the whole range of M_a.

11. One solution set at one time needs to be considered to compute the switching angles; select the best solution set offering an optimum response in terms of output voltage and current THD.

These steps enable simple computation of all the possible solution sets where they exist.

3.5 Control System of the Proposed Inverter in Grid-Tied PV System

Figure 3.13 presents control system comprising of MPPT algorithm, and PI based current controller for the TCHB grid-tied topology. In addition, Figure 3.14 presents the control system for the proposed PiCHB gird-tied topology

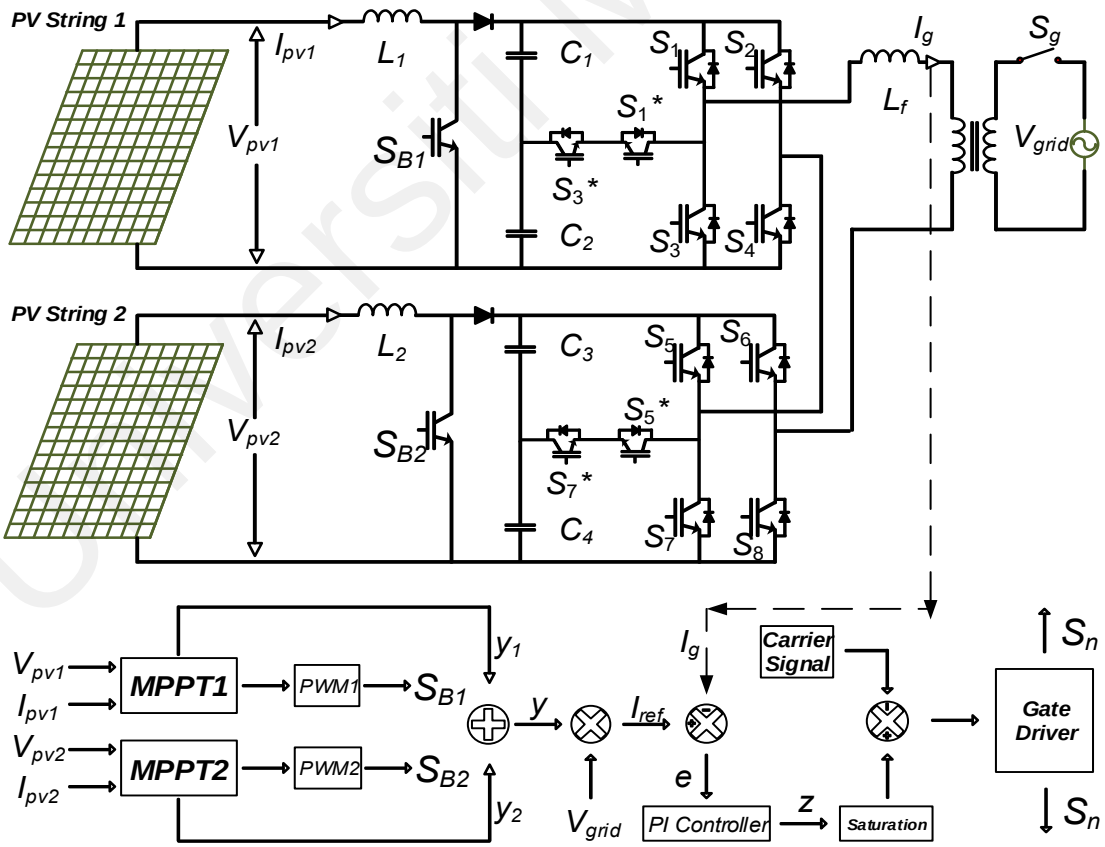


Figure 3.13: Proposed closed-loop control for the single-phase nine-level grid connected inverter topology

Figure 3.15 presents the MPPT technique based on the modified INC technique. The control system is employed to deliver maximum amount of energy from PV system to grid and attain a better harmonic profile of the output-current and voltage. Here, current injected into the grid, I_g is the feedback signal for comparison with reference current I_{ref}. The utility grid voltage V_g is transformed into the reference signal by multiplying it with the variable y. y is attained by the mINC MPPT schemes. By (3.50):

$$I_{ref} = V_g * y \tag{3.50}$$

$$y = y_1 + y_2 \tag{3.51}$$

Where the variable y is the sum of y_1 and y_2. For the PV strings 1 and 2, these variables correspond to the mINC MPPT algorithm.

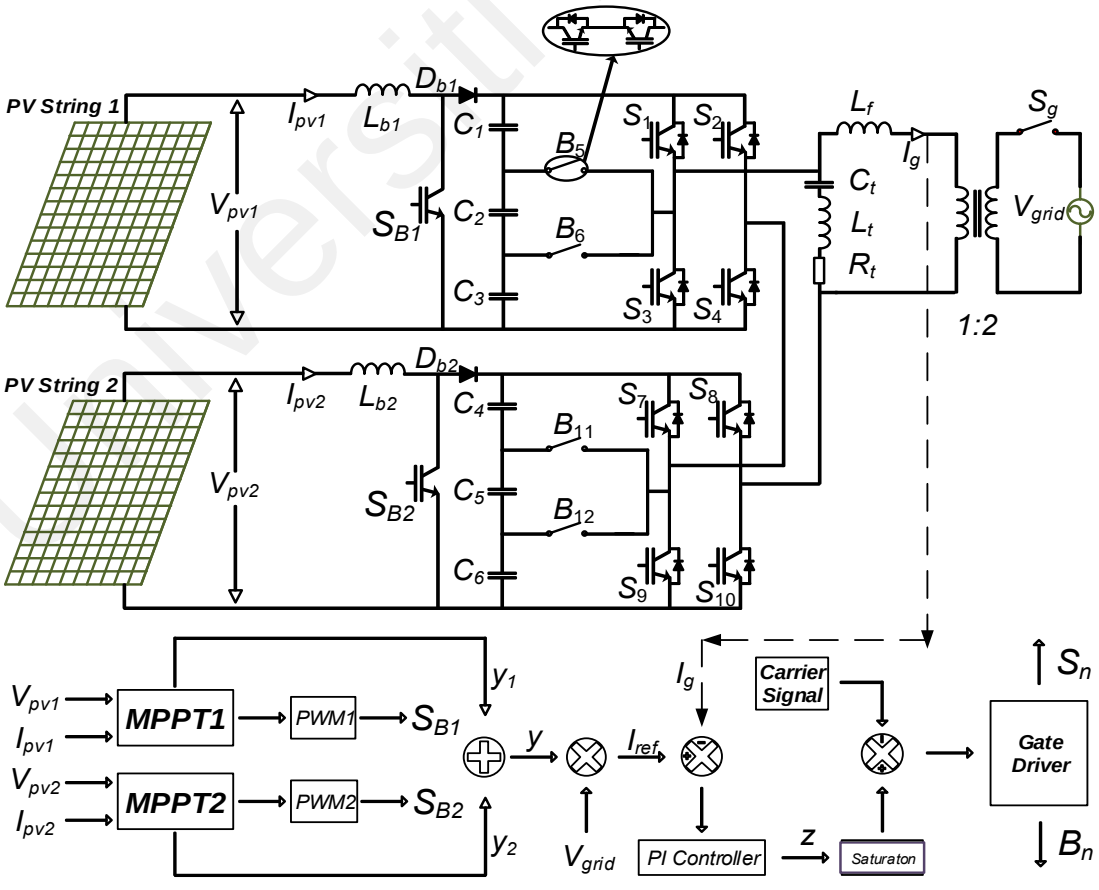


Figure 3.14: Proposed closed-loop control for the single-phase thirteen-level grid connected inverter topology

Variables y_1 and y_2, correspond to PV strings 1 and 2, respectively, as presented in Figure 3.12. For each PV string an individual mINC MPPT algorithm is employed to attain y_1 and y_2 while maintaining optimum power in each cascaded. These variables are dependent on the environmental conditions of changing temperature and ambient irradiance. With higher irradiance, a higher I_{ref} is obtained and consequently larger output-current.

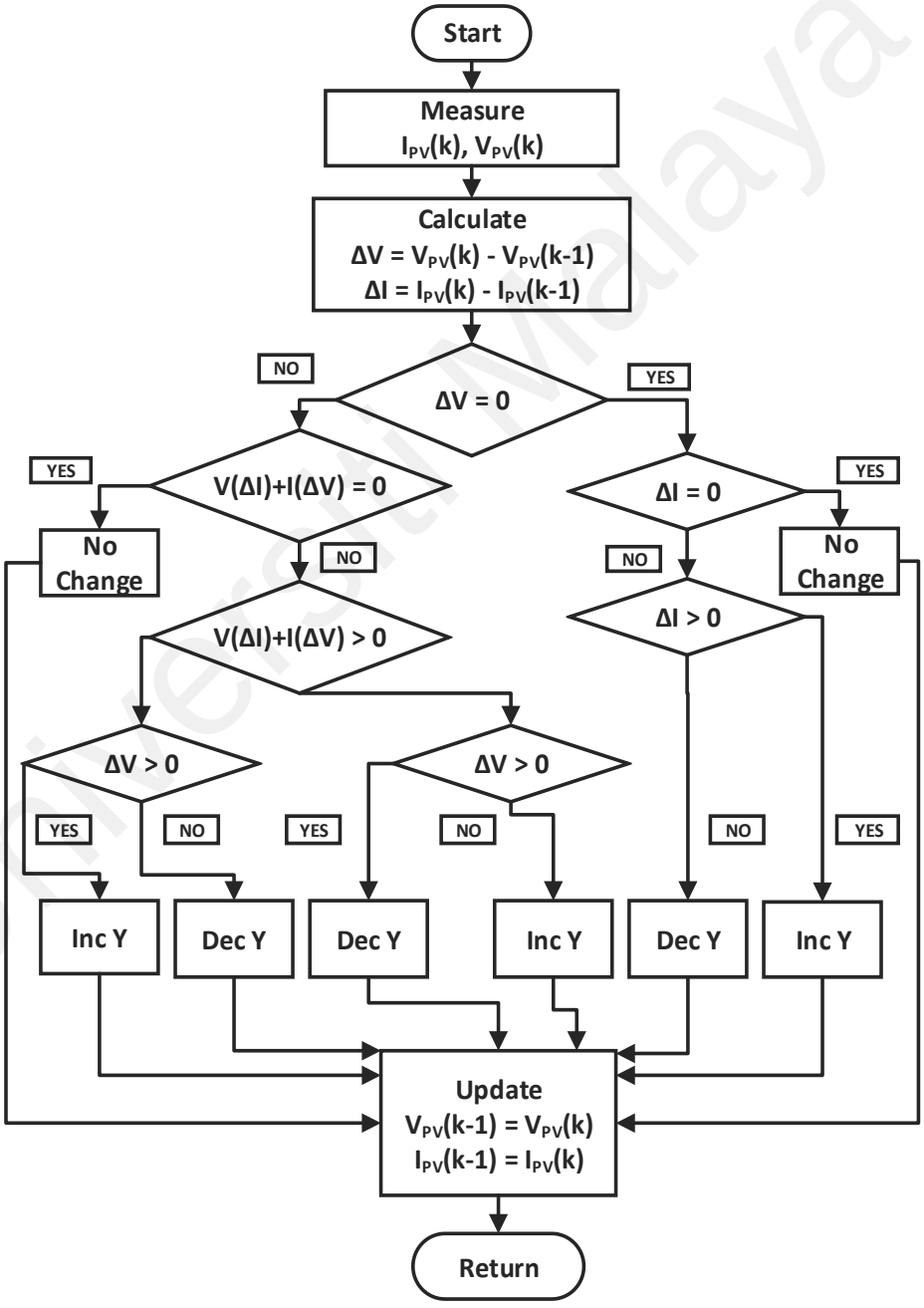


Figure 3.15: mINC MPPT Algorithm

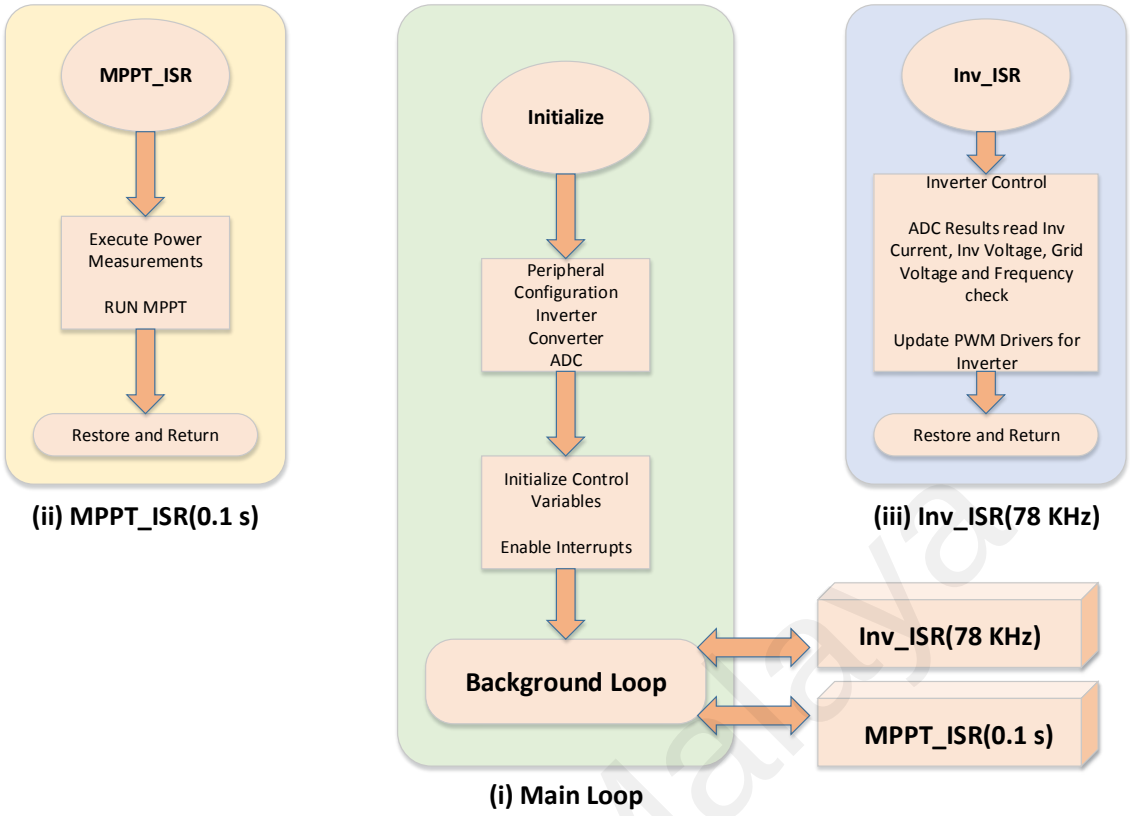


Figure 3.16: PV Inverter Software Structure (i) Main Loop (ii) MPPT ISR (iii) Inverter ISR

Error signal e attained is provided to the PI controller. Subsequent error signal z, after passing through an antiwindup process forms the reference. These reference signals are made to intersect with carrier to obtain switching signals for semiconductor switches. Such an approach offers almost-unity power factor for the inverter operation where I_g and V_g are in-phase. Figure 3.16 presents the PV inverter software structure. Continuous time domain PI algorithm can be written as:

$$z(t) = K_p e(t) + K_i \int_{\tau=0}^{t} e(\tau) d\tau \tag{3.52}$$

$z(t)$ remains the control signal, K_i the integral gain; K_p the proportional gain; $e(\tau)$ being the error signal and τ calculus variable of integration. Here, the trapezoidal sum approximation is used for discrete-time domain transformation. The steady-state error

was minimized while operating the PI controller at the most suitable coefficients after trial and error method. This control scheme was proposed by (Rahim & Selvaraj, 2010).

3.6 Summary

This chapter discussed the design and operating principles of the proposed TCHB and PiCHB single-phase MLI with two T-type and π-type BS, respectively. The TCHB offers nine-levels of output-voltage (2Vdc, 3Vdc/2, Vdc, Vdc/2, 0, −Vdc/2, −Vdc, −3Vdc/2, −2Vdc) from two separate dc supply voltages, whereas the PiCHB offers a thirteen-level output-voltage (2Vdc, 5Vdc/3, 4Vdc/3, Vdc, 2Vdc/3, Vdc/3, 0, −Vdc/3, −2Vdc/3, −Vdc, −4Vdc/3, −5Vdc/3, −2Vdc).

The proposed MLI are designed to operate with optimized switching angles in low switching-frequency and with PWM in high switching frequency. These MLI were applied to a grid-connected PV system. The closed-loop control system for the proposed MLI, with MPPT based on mINC and PI-based current-controller had been detailed.

CHAPTER 4: SIMULATION RESULTS

4.1 Introduction

This chapter presents the simulation results for the proposed mINC MPPT, single-phase TCHB and PiCHB inverters with stand-alone and grid-tied PV systems. The simulation results of the proposed TCHB and PiCHB MLI were attained through the MATLAB/SIMULINK® software tools for low switching-frequency, PWM switching, and PV applications. For low switching frequency, optimization of the switching angles was acquired for the harmonic content of the inverter output voltage to be the lowest. For high switching frequency, various modulation indices were simulated to discover how modulation index relates with output waveform and THD.

A model of the characteristic PV module is simulated. Current-Voltage (I-V) curves and Power-Voltage (P-V) curves for varying environmental conditions are simulated for their relation to module performance. The PV module model is used for the simulation of the grid-connection PV inverter systems with the proposed TCHB and PiCHB inverters. Here, the major focus has been on the high-frequency PWM switching, nonetheless, the low-frequency switching technique has also been highlighted.

4.2 Simulations at Low-Frequency Switching

4.2.1 TCHB Inverter

Matlab/Simulink software simulated the proposed TCHB MLI topology. The setup has been shown in the Figure 4.1, with two separate DC voltage sources (100V each), H-bridge conventional inverter with two T- type bidirectional switches (BSs), an AC load of (R=250Ω), and four DC-Link capacitors of 2200uF each, had been connected. Here, eight pulses drive the twelve switches of the proposed TCHB inverter. As observed in

Figure 4.1 the T-type Bidirectional Switch utilizes two semiconductor switches with an emitter-emitter configuration.

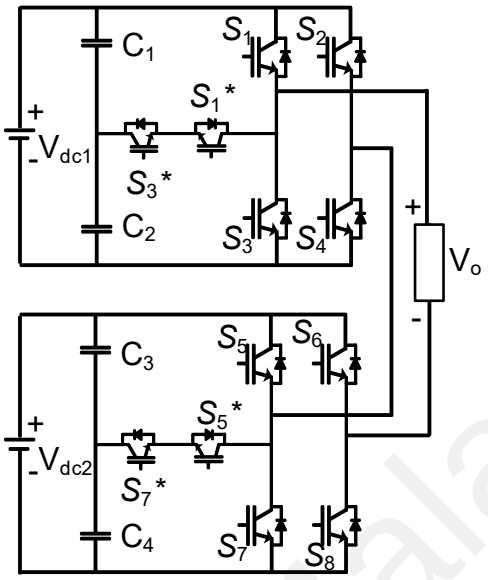


Figure 4.1: Setup of the proposed TCHB inverter in low-frequency-switching simulation

Figures 4.2 and 4.3 present the switching signals for the switches S1, S2, S3 and S4, S5, S7, respectively. As S2=S6, S4=S8, S1*=not(S1), S3*=not(S3), S5*=not(S5) and S7*=not(S7). In addition, for the applied low-frequency switching, Figures 4.4 and 4.5 show the TCHB's output-voltage and output-current, respectively.

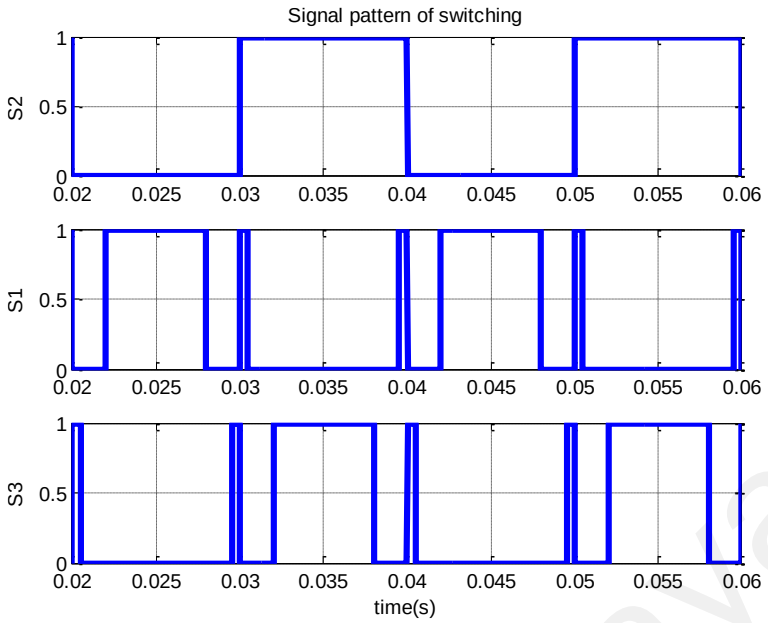


Figure 4.2: Switching signals for switches S1, S2 and S3

Figure 4.6 shows the FFT analysis of the output-current displaying the harmonic content of the proposed TCHB inverter to be 9.90%. Here, the simulation was made to operate for a total time 0.06 seconds, 2 of 3 cycles have been displayed in the FFT window to display the operation at 50 Hz.

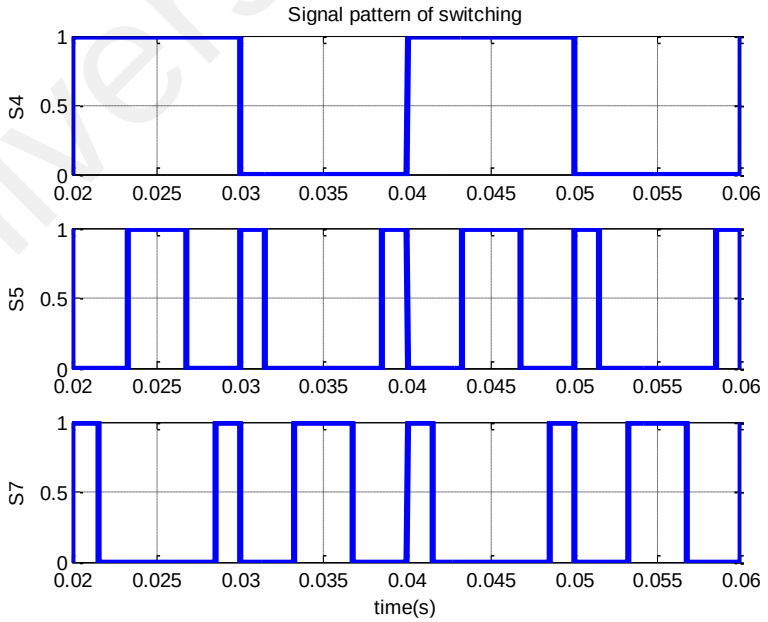


Figure 4.3: Switching signals for switches S4, S5 and S7

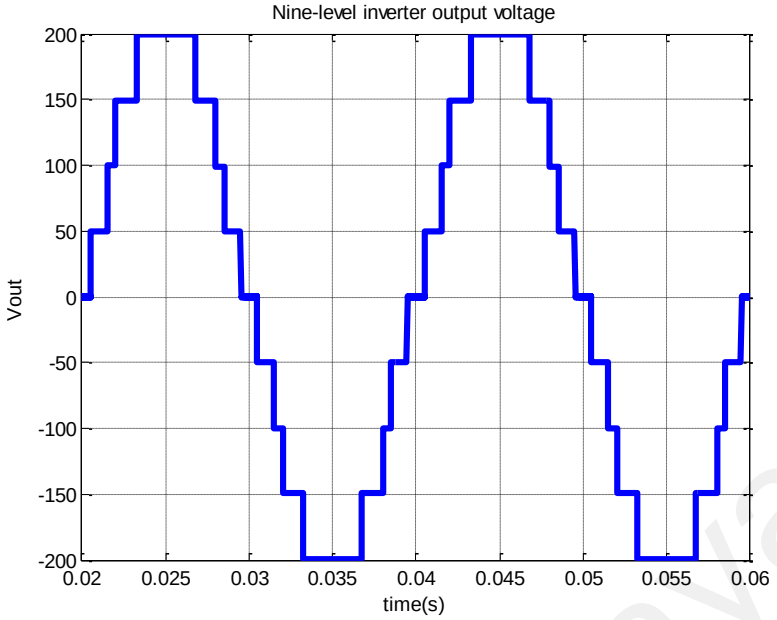


Figure 4.4: Resulting Output-Voltage for the low-frequency switching signals

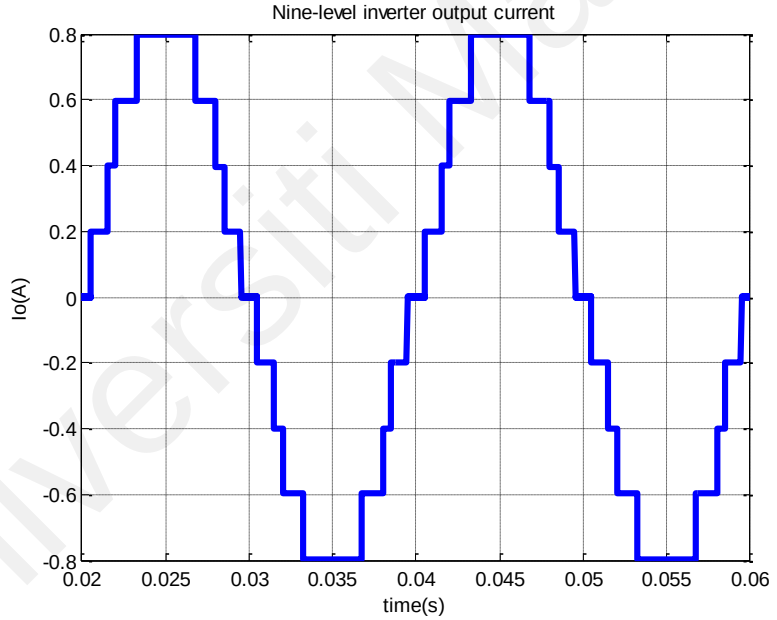


Figure 4.5: Resulting Output-Current for the low-frequency switching signals

For TCHB inverter, in order to attain a reduced harmonic content the modulation index M_a was made to operate between 0.75 and 1. Such a low frequency switching attains a nine-level low frequency output voltage.

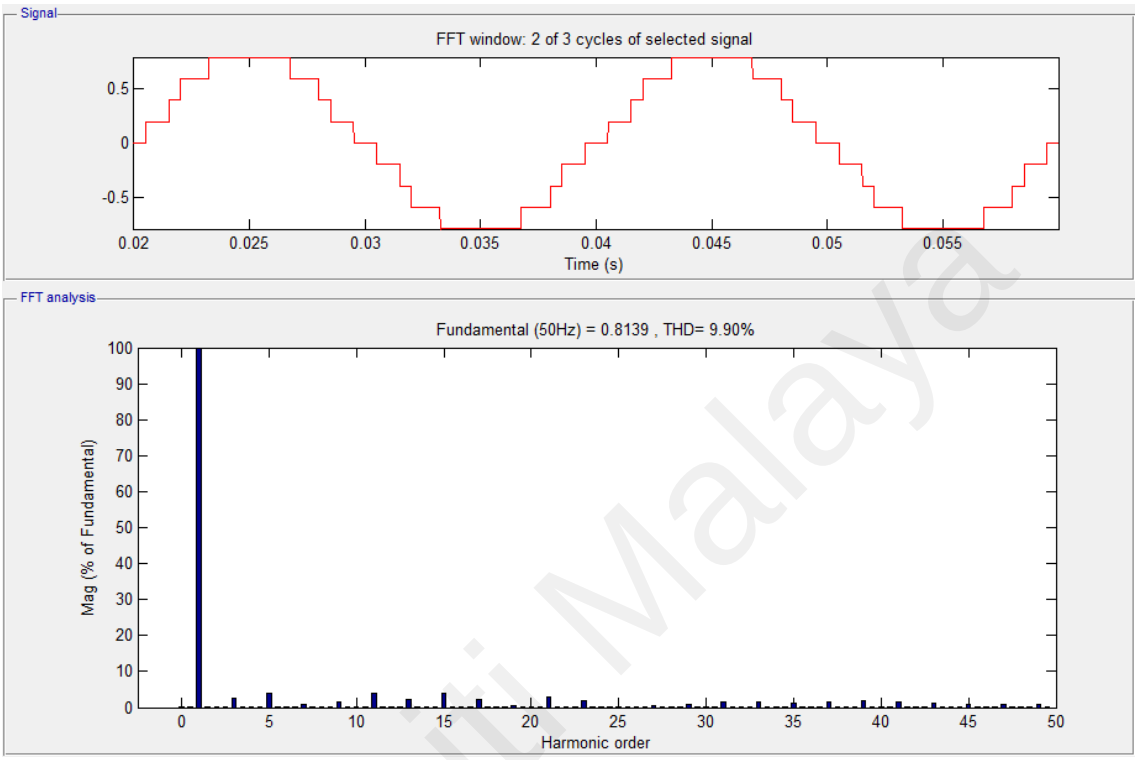


Figure 4.6: FFT analysis of Output-Current

4.2.2 PiCHB Inverter

Matlab/Simulink schematic diagram simulated the proposed PiCHB multilevel inverter topology as presented in Figure 4.7. The setup utilizes two separate DC voltage sources (100V each), H-bridge conventional inverter with two π-type BS, an AC load of (R=250Ω), and six DC-Link capacitors of 2200uF each had been connected. The PiCHB MLI uses twelve pulses in order to drive the sixteen switches. Moreover, the π-type BS employees four semiconductor switches, where the emitter-emitter configuration has been utilized for the bidirectional switches. To attain least amount of harmonic content for the output-voltage the modulation index was kept between 0.83 and 1. Figures 4.8 and 4.9 present the switching signals for the switches S1, S2, S3, B5, B6 and S4, S7, S9, B11, B12, respectively. As S2=S8, S4=S10, B5=S5, B6= S6, B11=S11 and B12=S12. Such

low frequency switching pulses were utilized to attain a thirteen-level output-voltage from the PiCHB MLI.

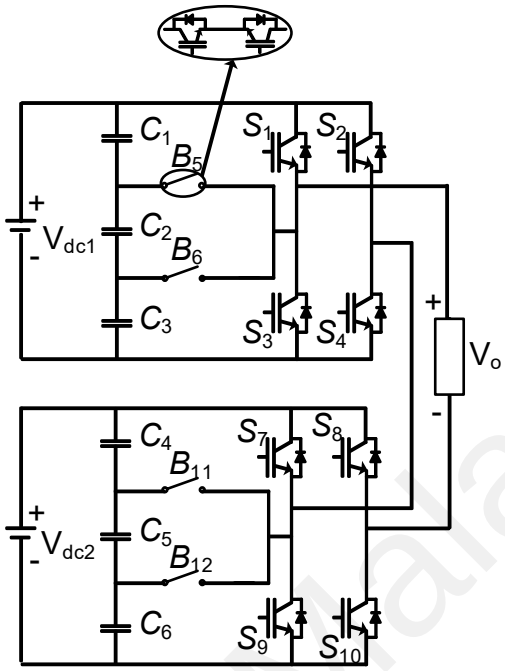


Figure 4.7: Setup of the proposed inverter in low-frequency-switching simulation

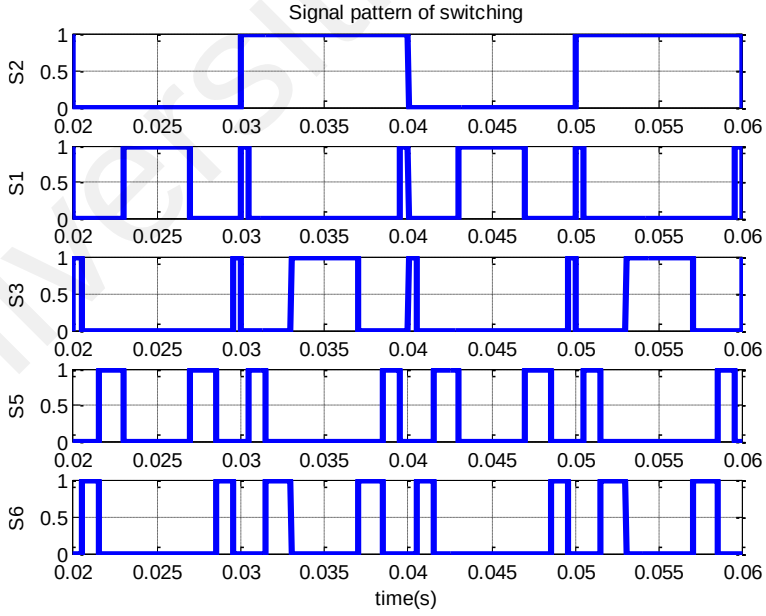


Figure 4.8: Switching signals for the switches S1, S2, S3, B5 and B6

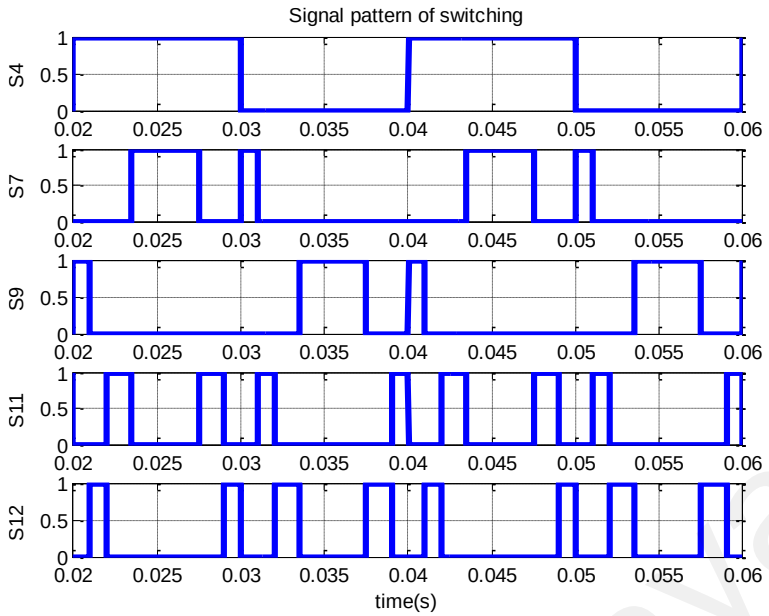


Figure 4.9: Switching signals for the switches S4, S7, S9, B11 and B12

In addition, Figures 4.10 and 4.11 display the resulting output-voltage and output-current, respectively, due to the applied switching signals. As observed the TCHB MLI offered an output-voltage of nine-levels, whereas the PiCHB MLI attained an output-voltage of thirteen-levels. Thus, the PiCHB is utilized to attain higher levels with lower output harmonics as presented in Figure 4.12. However, the number of switches and gate drivers for the PiCHB remain greater than the TCHB.

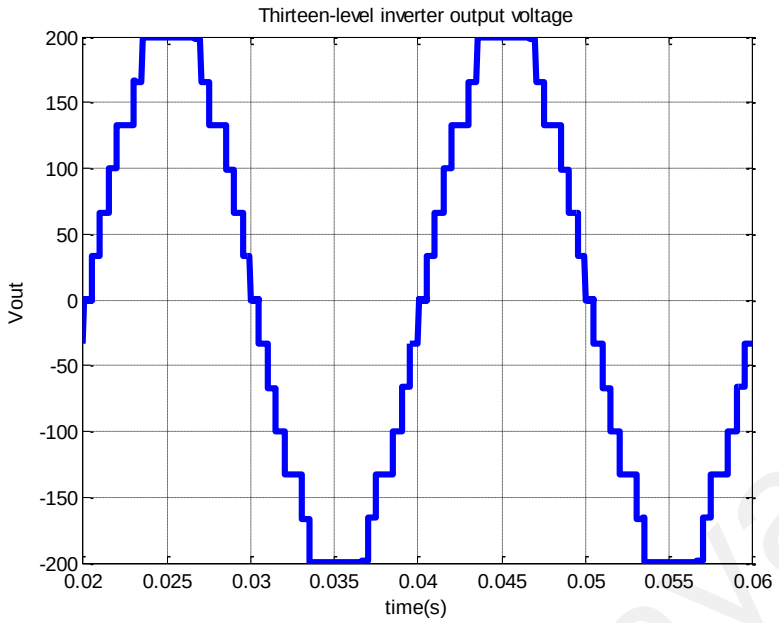


Figure 4.10: Resulting Output-Voltage for the low-frequency switching signals

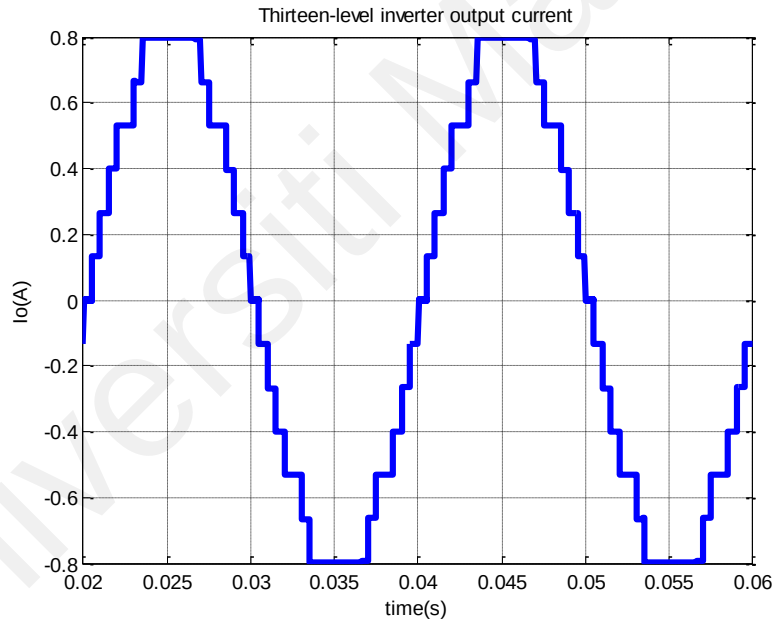


Figure 4.11: Resulting Output-Current for the low-frequency switching signals

Figure 4.12 shows the FFT analysis of the output-current displaying a lower harmonic content of the proposed PiCHB inverter output-current to be 6.25%, against the TCHB inverter's output-current harmonic content to be 9.90%. Here, the simulation was made to operate for a total time 0.06 seconds, 2 of 3 cycles have been displayed in the FFT window to display the operation at 50 Hz.

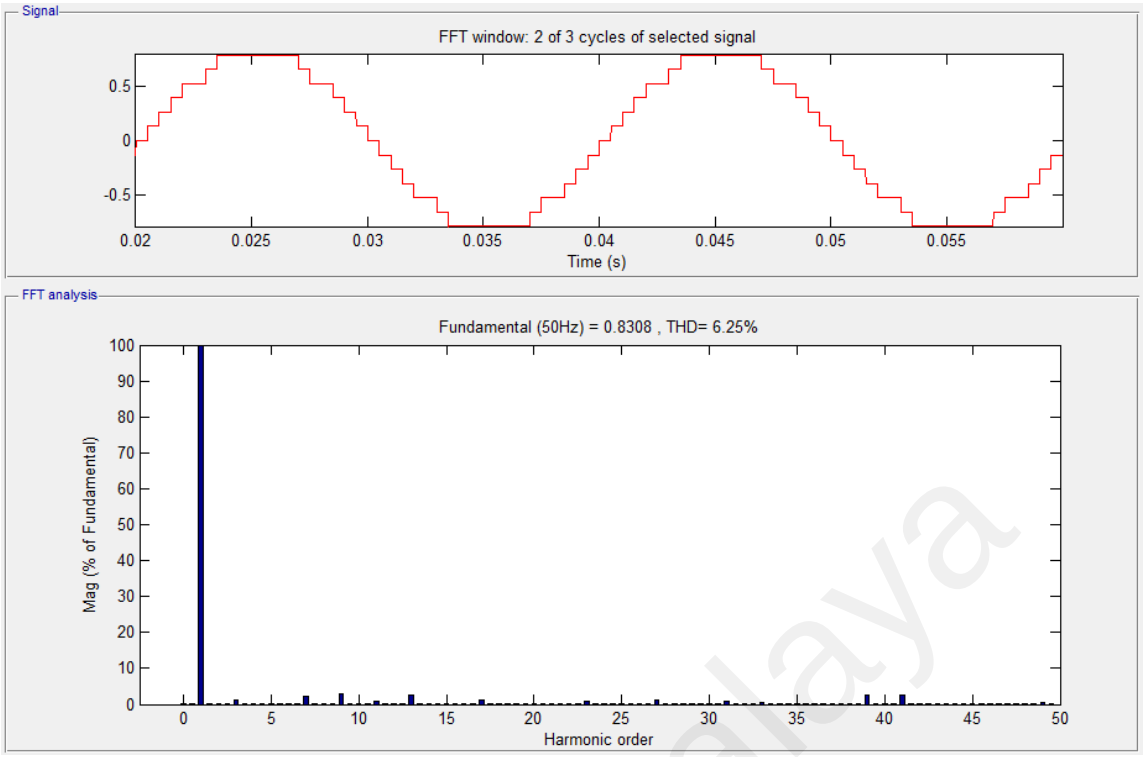


Figure 4.12: FFT analysis of the Output-Current

4.3 Simulation of the PWM Control Scheme

4.3.1 TCHB Inverter

Figure 4.13 is a diagram of the simulation setup for the proposed TCHB inverter in PWM high switching application. The simulations were performed at 20 kHz switching frequency. The filtering inductor Lf was 5mH and the resistor load bank was 100 Ohm. The DC bus capacitors were 2200 μF each and DC Voltage Source was kept at 100 V each.

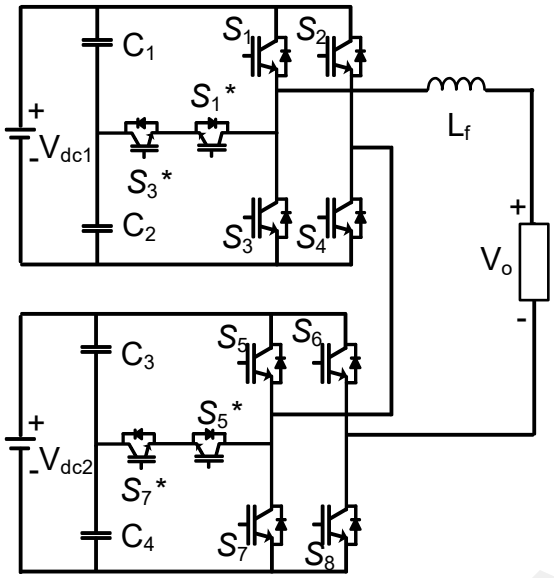


Figure 4.13: Setup of the proposed TCHB inverter at high frequency switching

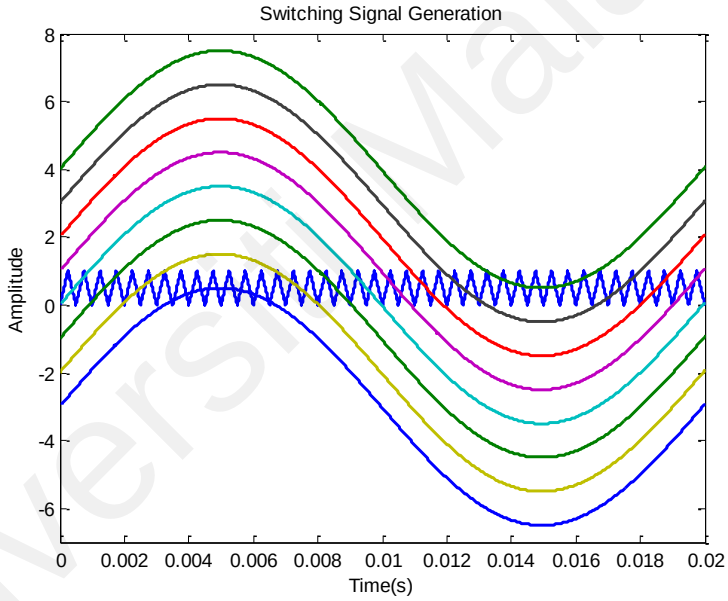


Figure 4.14: Switching Signal Generation for high frequency switching

Figure 4.14 demonstrates the PWM signal generation technique, which utilizes the modulation (reference) signals Vref1, Vref2, Vref3, Vref4, Vref5, Vref6, Vref7 and Vref8 and one triangular carrier signal Vcarrier. Figures 4.15 and 4.16 show the resulting PWM switching signals for the switches S1-S8. Switches S1, S3, S1*, S3*, S5, S5*, S7 and S7* are switched at the carrier-signal frequency, whereas S2, S4, S6 and S8 are operated at the same frequency as the fundamental frequency (50Hz). Here, M_a was set at 0.87.

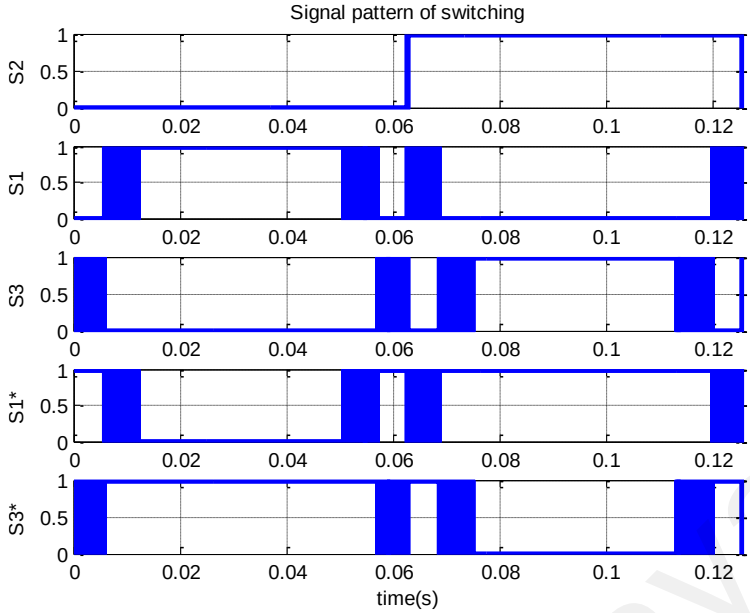


Figure 4.15: Switching Signals for Switches S1, S1*, S3, S3*, & S2

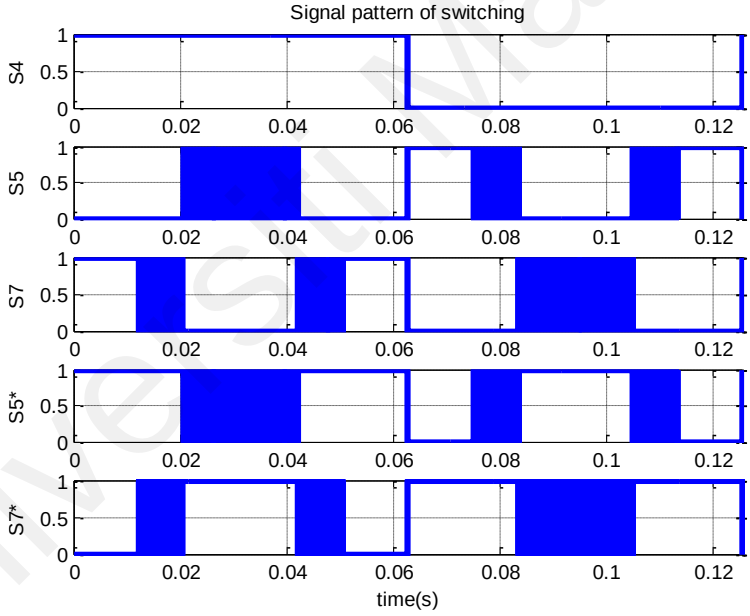


Figure 4.16: Switching Signals for Switches S5, S5*, S7, S7* and S4

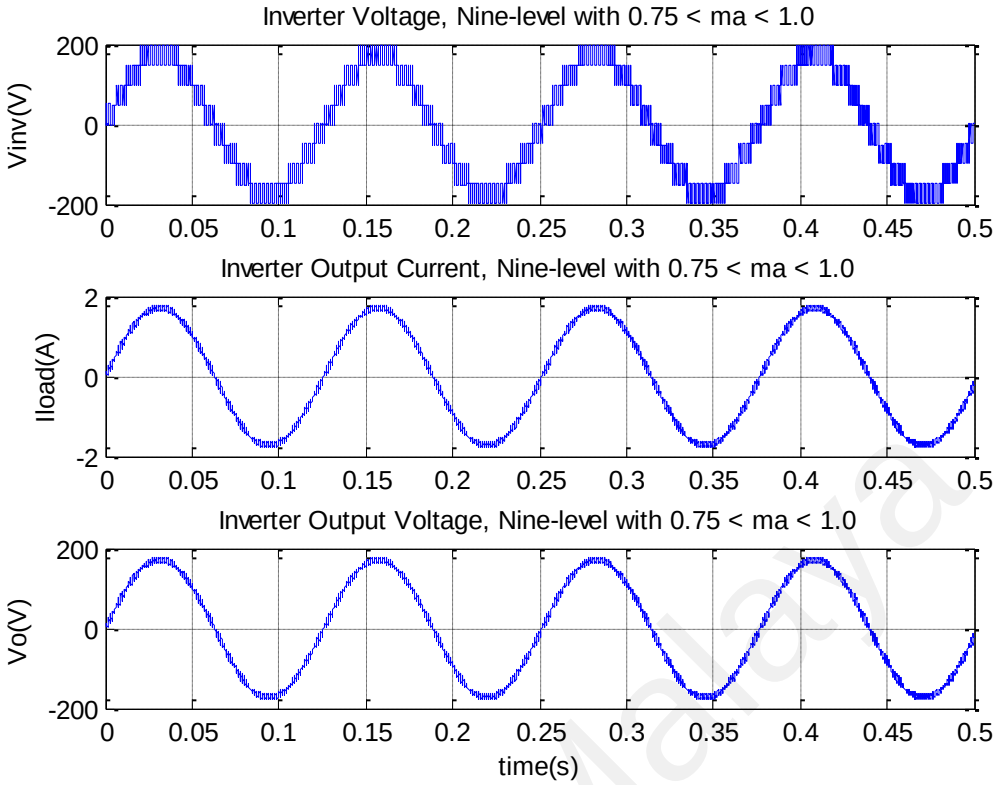


Figure 4.17: Inverter-Voltage, Output-Current and Output-Voltage waveforms of the proposed TCHB inverter when $\boldsymbol{M_a = 0.87}$ was set between 0.75 and 1

For the modulation index (M_a) set to exceed 0.75 but below 1, the proposed TCHB MLI will generate a nine-level output-voltage waveform to form the pre-filtered voltage Vin.

Figure 4.17 shows the inverter-voltage, output-current and the output-voltage waveforms of the proposed TCHB inverter when the M_a was set to be between 0.75 and 1. The post filtering output voltage waveform and the output current waveform were sinusoidal at the load terminal, but pre-filtering, the output voltage waveform was quasi sinusoidal. Figure 4.18 and 4.19 respectively show the harmonic content of the output-voltage and of the output-current. The output-voltage THD was 2.56%. At these conditions the output current THD was also 2.56%. As observed, the simulation was performed for 0.02 seconds to attain one cycle of operation at 50 Hz output frequency.

The switching signals for all switches and the respective standing voltages are displayed in Figure 4.20 and Figure 4.21, respectively.

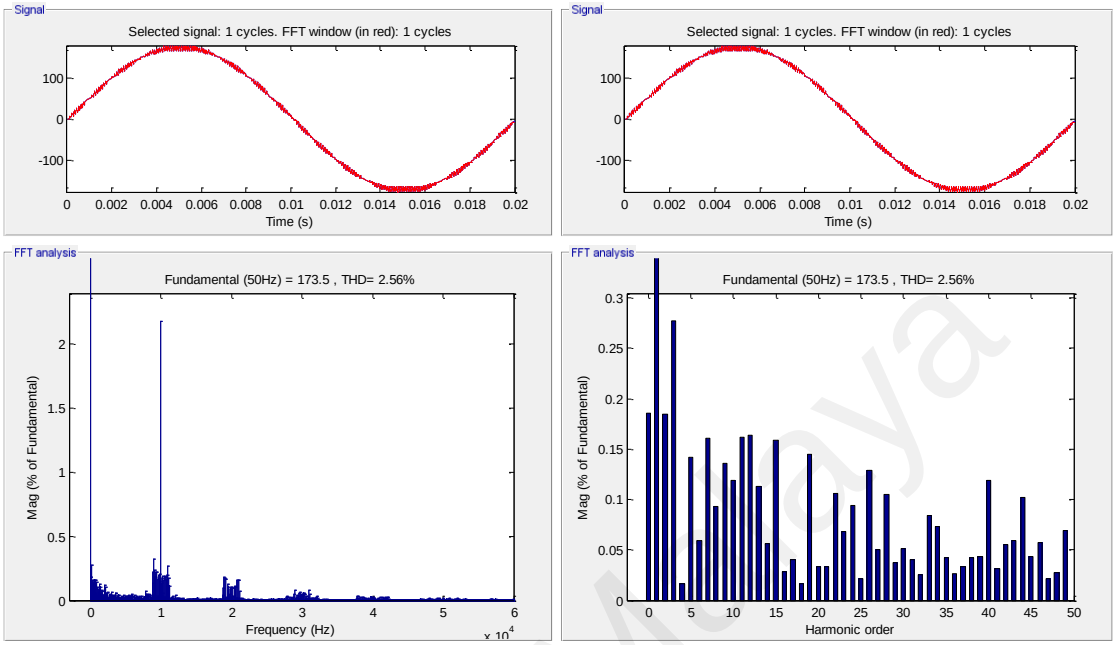


Figure 4.18: FFT analysis of Output-Voltage waveforms of the proposed TCHB inverter when $\boldsymbol{M_a}$ was set between 0.75 and 1

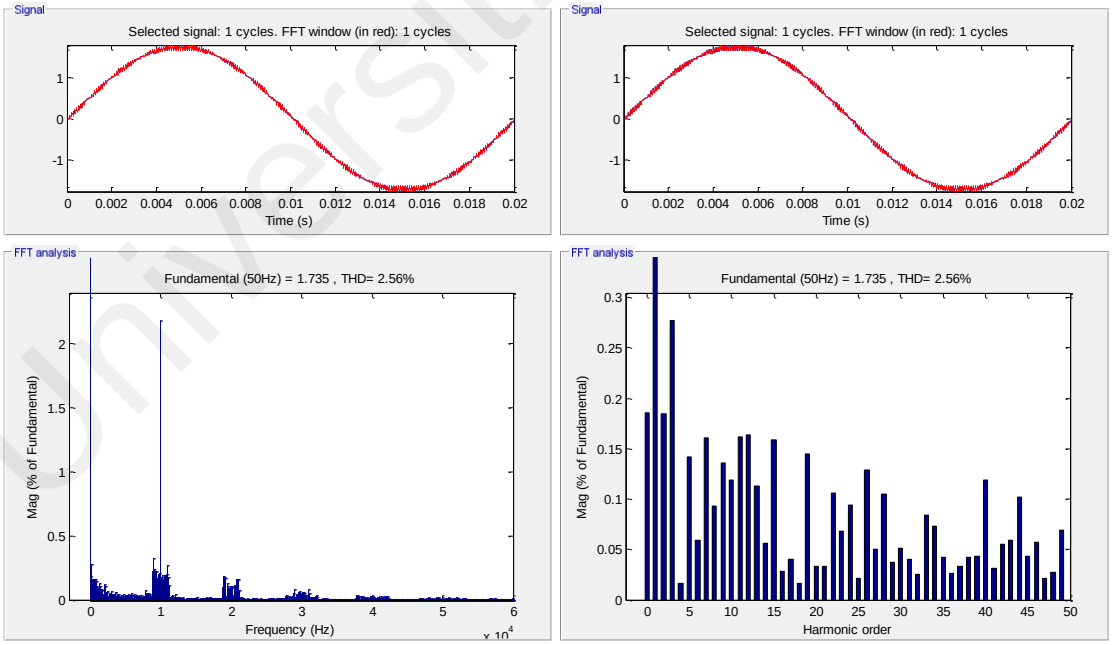


Figure 4.19: FFT analysis of Output-Current waveforms of the proposed TCHB inverter when $\boldsymbol{M_a}$ was set between 0.75 and 1

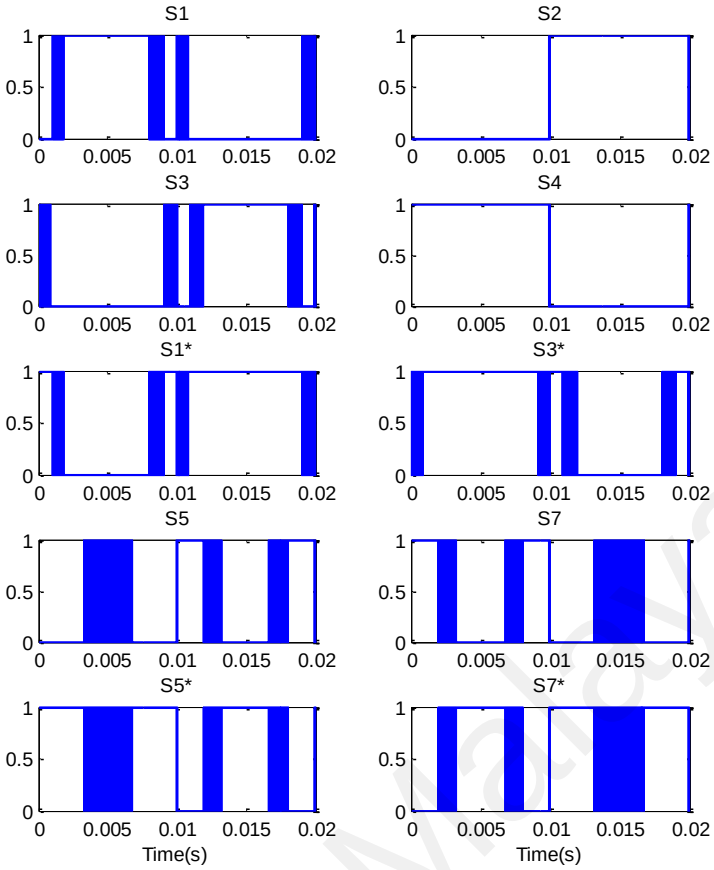


Figure 4.20: Switching signals for all switches

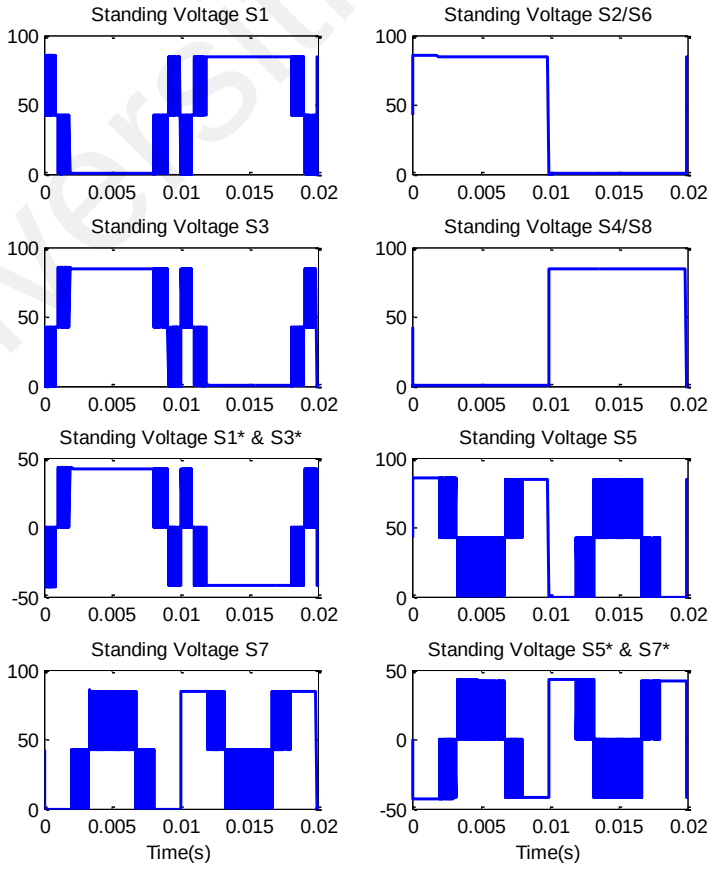


Figure 4.21: Corresponding Standing-Voltages

For M_a set to exceed 0.5 but below 0.75, the proposed TCHB MLI will generate a seven-level output-voltage waveform to form the pre-filtered voltage Vin. This reduction in modulation index offered an output-voltage with lesser levels and higher THD. Thus, with similar number of switches and gate drivers the TCHB with lower M_a offers lower output-voltage levels.

Figure 4.22 shows the switching signals for the switches S1, S3, S1*, S3* and S2. In addition, Figure 4.23 presents the switching signals for the switches S5, S7, S5*, S7* and S4. Here, the M_a was set at 0.67. Figure 4.24 presents the inverter-voltage, output-current and the output-voltage waveforms of the proposed TCHB inverter when the modulation index M_a was set to be between 0.5 and 0.75.

Figures 4.25 and 4.26 show the harmonic content of the output-voltage and of the output-current, respectively.

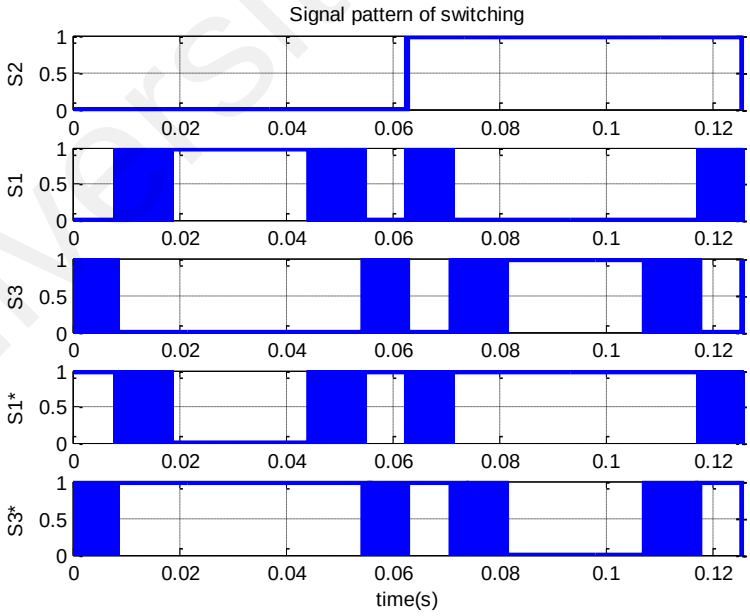


Figure 4.22: Switching signals for S1, S3, S1*, S3* and S2

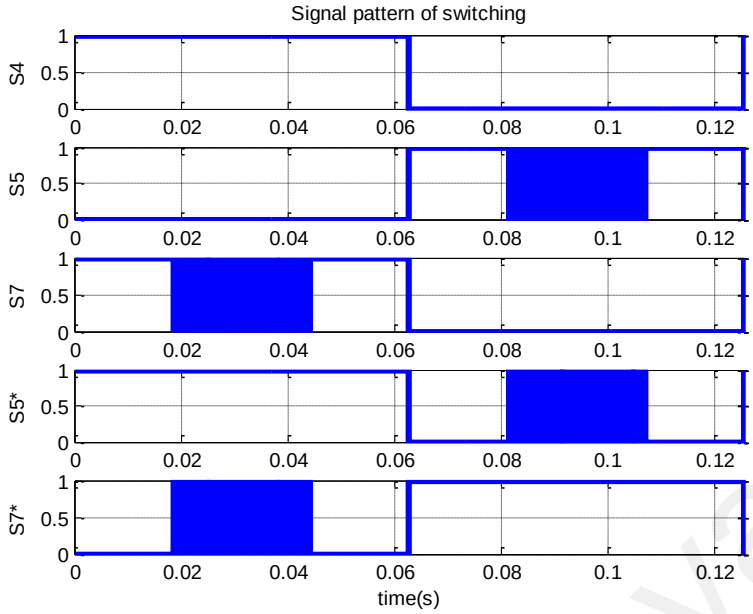


Figure 4.23: Switching signals for the switches S5, S7, S5*, S7* and S4

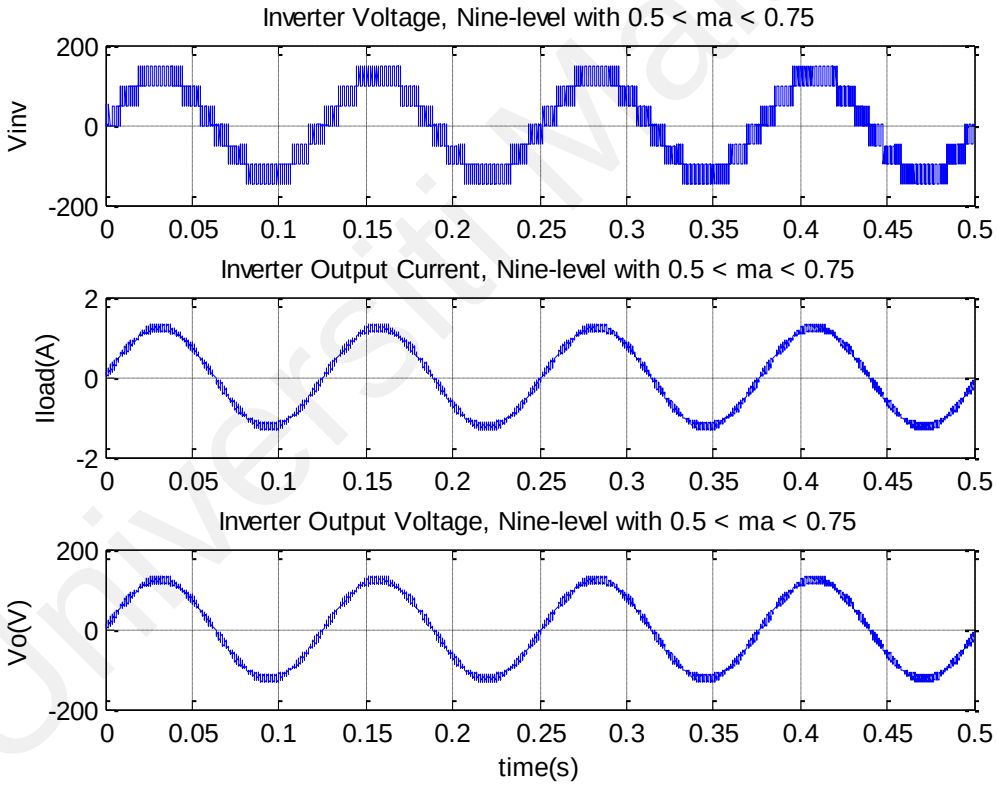


Figure 4.24: Inverter-voltage, output-current and the output-voltage waveforms when $\boldsymbol{M_a = 0.67}$ was set to be between 0.5 and 0.75

The output-voltage THD was 3.59%. At these conditions the output current THD was also 3.59%. As observed, the simulation was performed for 0.02 seconds to attain one cycle of operation at 50 Hz output frequency.

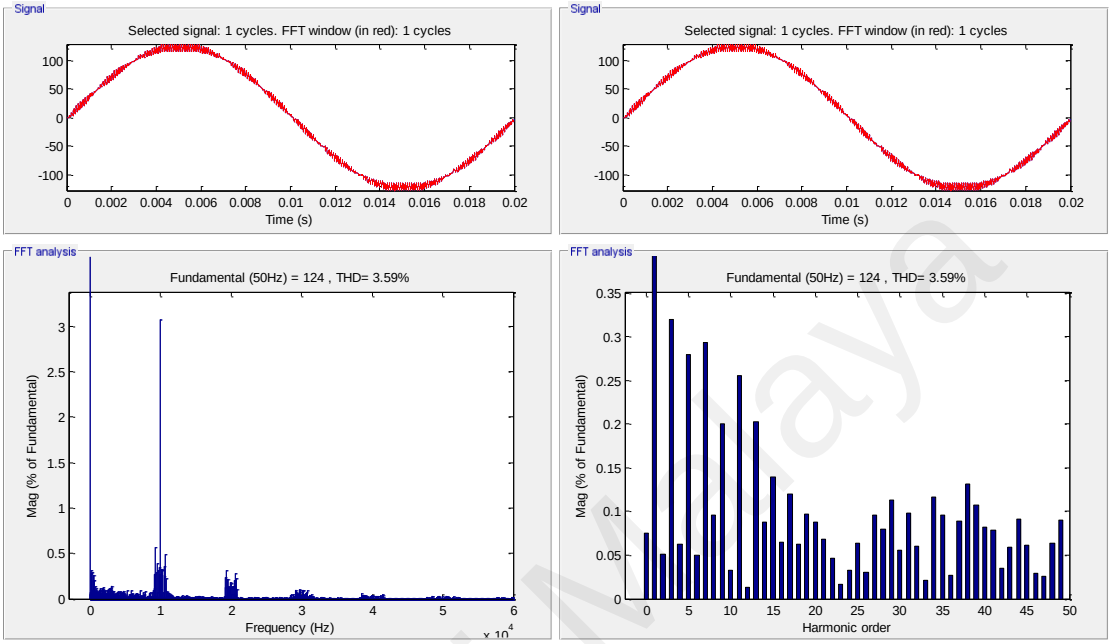


Figure 4.25: FFT analysis of Output-Voltage waveforms of the proposed TCHB inverter when $\boldsymbol{M_a}$ was set between 0.5 and 0.75

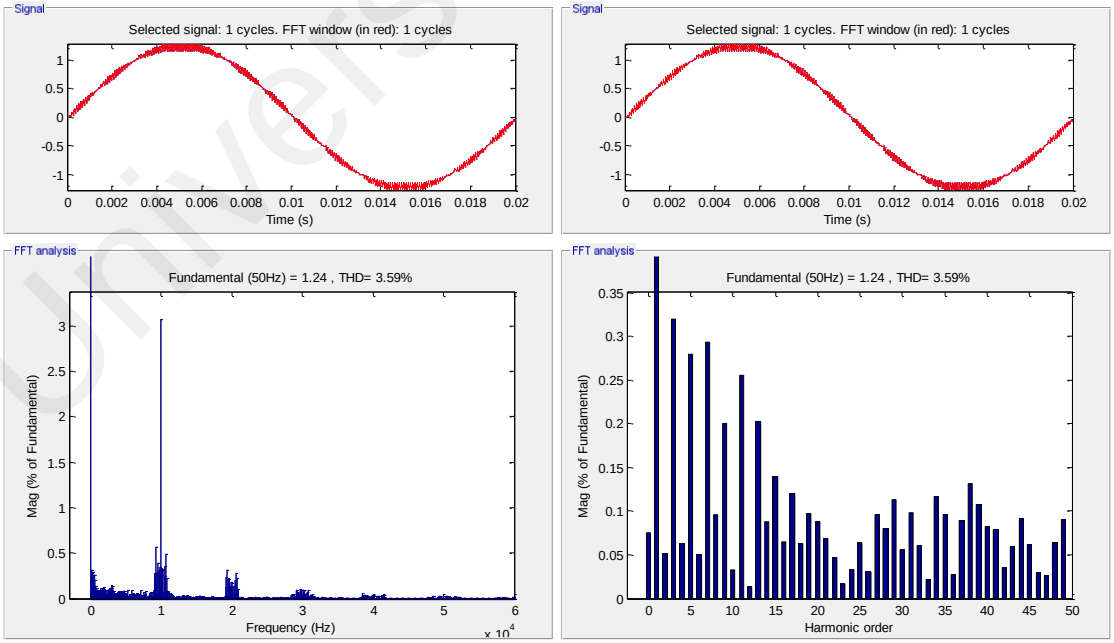


Figure 4.26: FFT analysis of Output-Current waveforms of the proposed TCHB inverter when $\boldsymbol{M_a}$ was set between 0.5 and 0.75

For M_a set to exceed 1, the proposed TCHB MLI will generate an output-voltage waveform to form the pre-filtered voltage Vin with chopped highest level. The chopped highest level is observed mainly due to the widening of the switching pulses applied to the inverter.

Contrasting to the reduction phenomenon in modulation index, the excess increase in M_a offered an output-voltage with a chopped highest level and highest THD. Thus, with similar number of switches and gate drivers the TCHB with M_a greater than 1 offers chopped output-voltage levels.

Figure 4.27 shows the switching signals for the switches S1, S3, S1*, S3* and S2. In addition, Figure 4.28 presents the switching signals for the switches S5, S7, S5*, S7* and S4. Here, the M_a was set at 1.17.

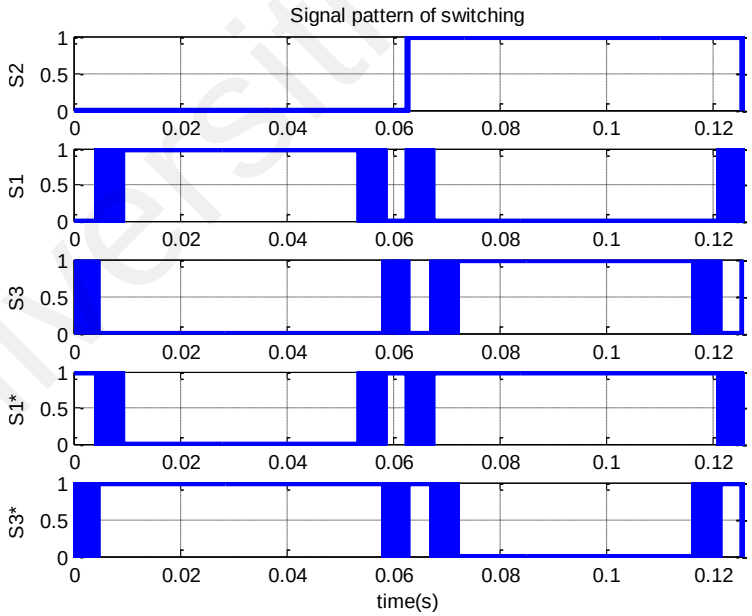


Figure 4.27: Switching signals for the switches S1, S3, S1*, S3* and S2

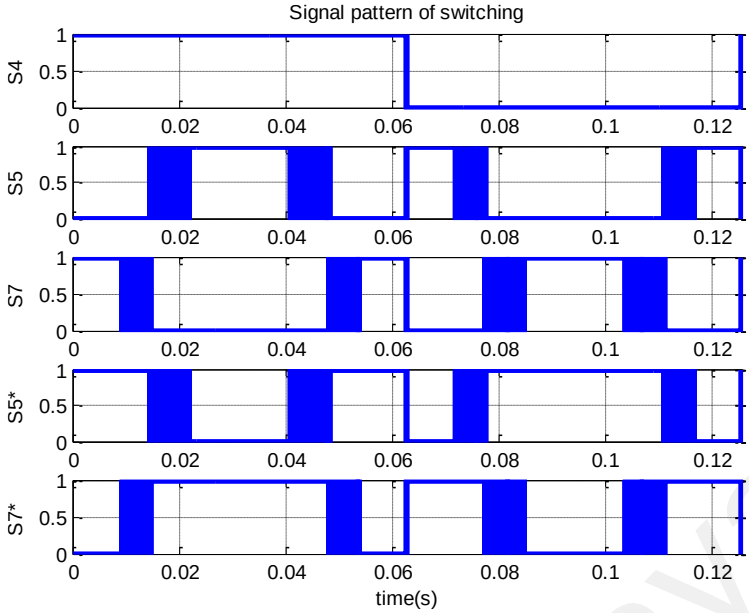


Figure 4.28: Switching signals for the switches S5, S7, S5*, S7* and S4

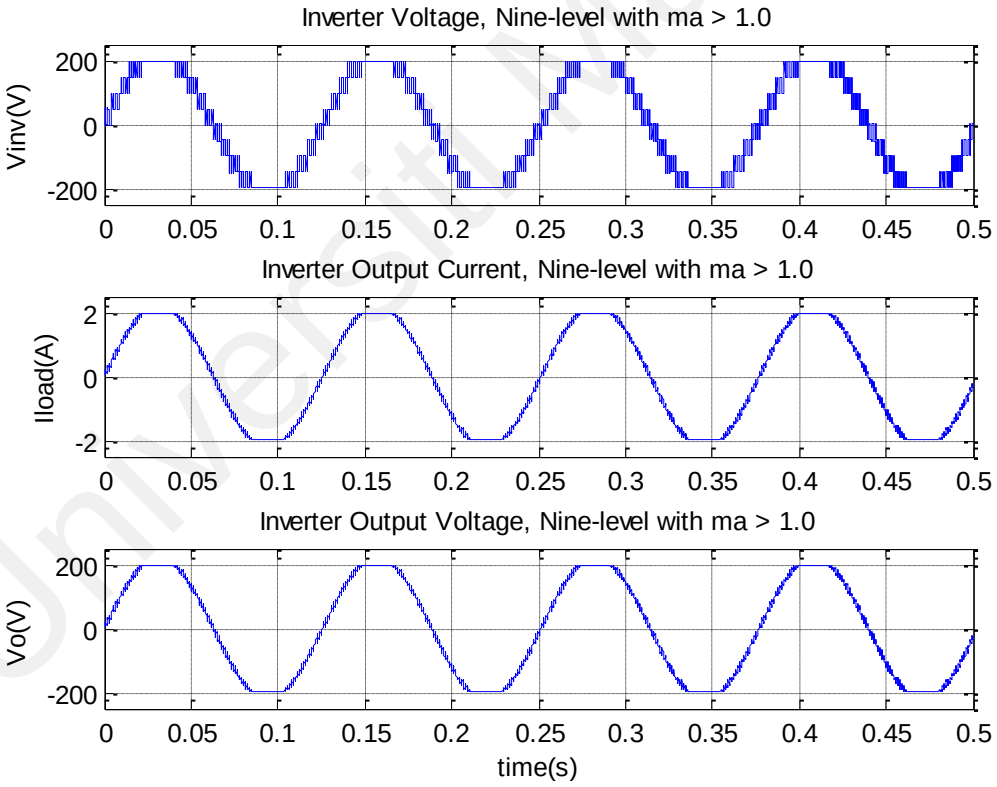


Figure 4.29: Inverter-voltage, output-current and the output-voltage waveforms of the proposed TCHB inverter when the modulation index $\boldsymbol{M_a = 1.17}$ exceeded 1

Figure 4.29 presents the inverter-voltage, output-current and the output-voltage waveforms of the proposed TCHB inverter when the modulation index M_a exceeded 1.

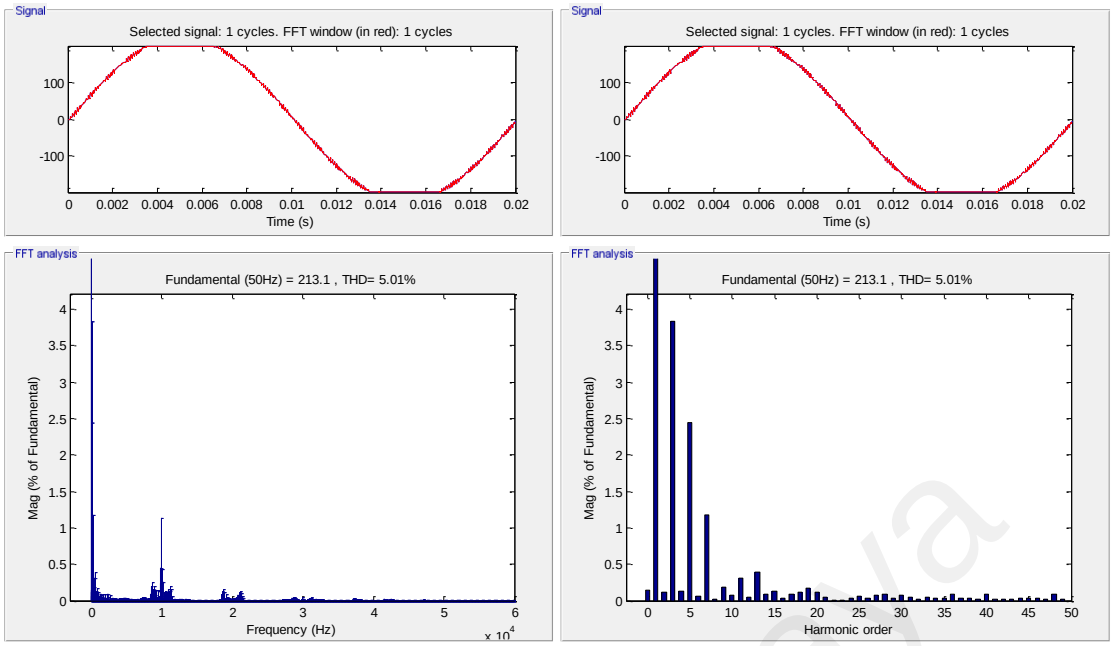


Figure 4.30: FFT analysis of Output-Voltage waveforms of the proposed TCHB inverter when $\boldsymbol{M_a}$ was set to exceed 1

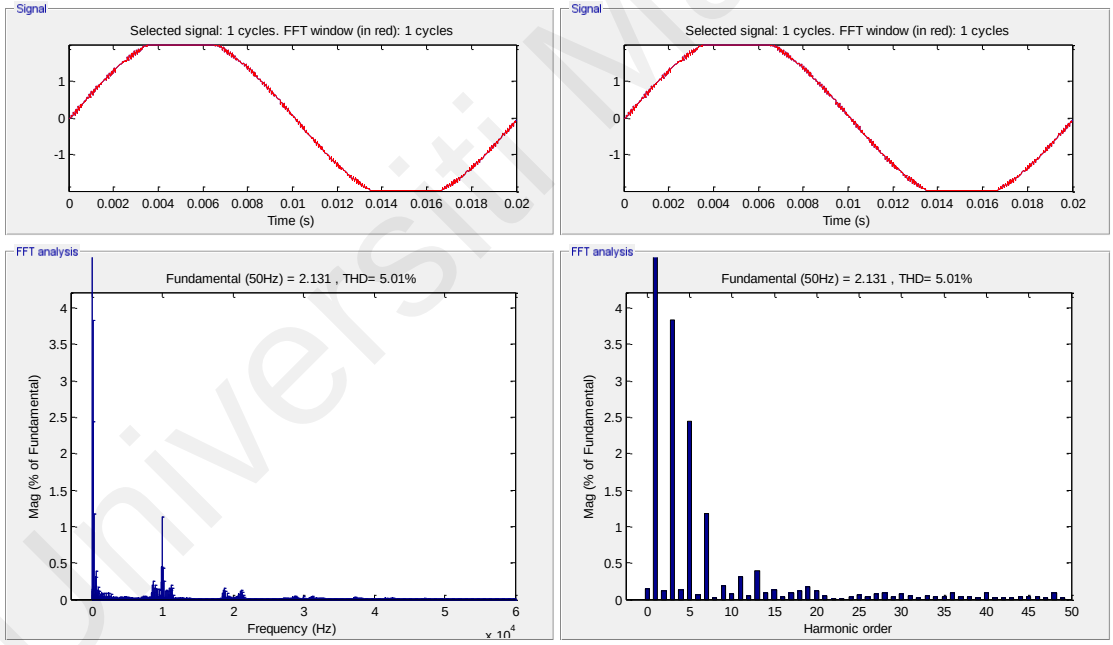


Figure 4.31: FFT analysis of Output-Current waveforms of the proposed TCHB inverter when $\boldsymbol{M_a}$ was set to exceed 1

Figure 4.30 and 4.31 show the harmonic content of the output-voltage and of the output-current, respectively. The output-voltage THD was 5.01%. At these conditions the output current THD was also 5.01%. As observed, the simulation was performed for 0.02 seconds to attain one cycle of operation at 50 Hz output frequency.

4.3.2 PiCHB Inverter

Figure 4.32 is the diagram of the simulation setup for the proposed PiCHB inverter in high switching application. The simulations were performed at 20 kHz switching frequency with 100 V DC source to each cascade. The filtering inductor Lf was 5mH and the resistor load bank was 100 Ohm. The DC bus capacitors were 2200 μF each.

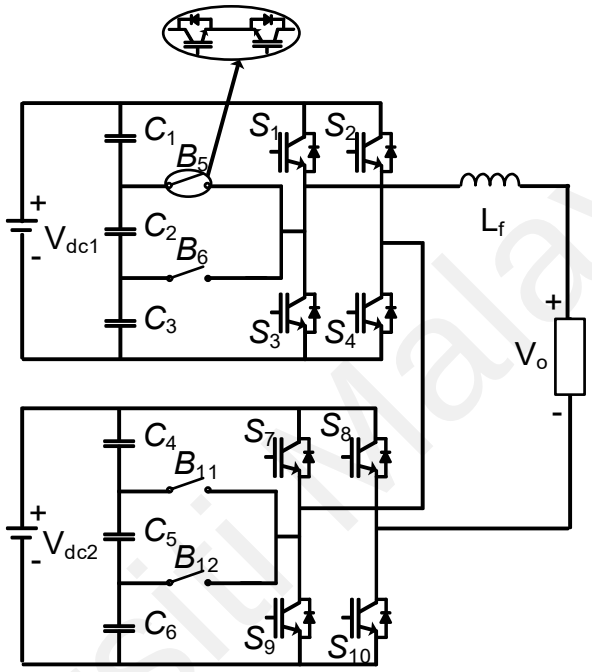


Figure 4.32: Setup of the PiCHB inverter at high frequency switching

Figure 4.33 demonstrates the PWM signal generation with modulation (or reference) signals Vref1, Vref2, Vref3, Vref4, Vref5, Vref6, Vref7, Vref8, Vref9, Vref10, Vref11 and Vref12 against one triangular carrier signal Vcarrier.

Figures 4.34 and 4.35 show the resulting PWM switching signals for switches S1-B12. Switches S1, S3, B5, B6, S7, S9, B11 and B12 are switched at the carrier-signal frequency whereas S2, S4, S8 and S10 are operated at the same frequency as the fundamental frequency (50Hz). Here, the M_a was set at 0.93.

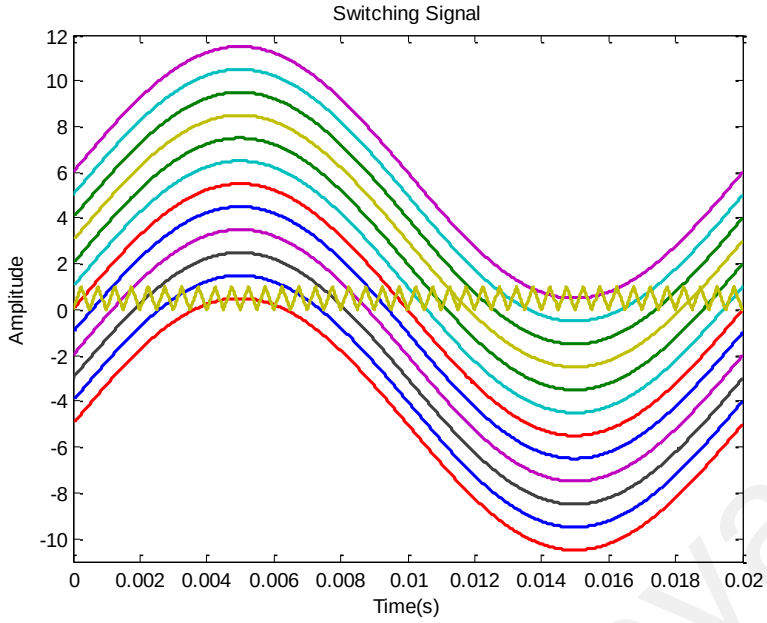


Figure 4.33: Switching Signal Generation

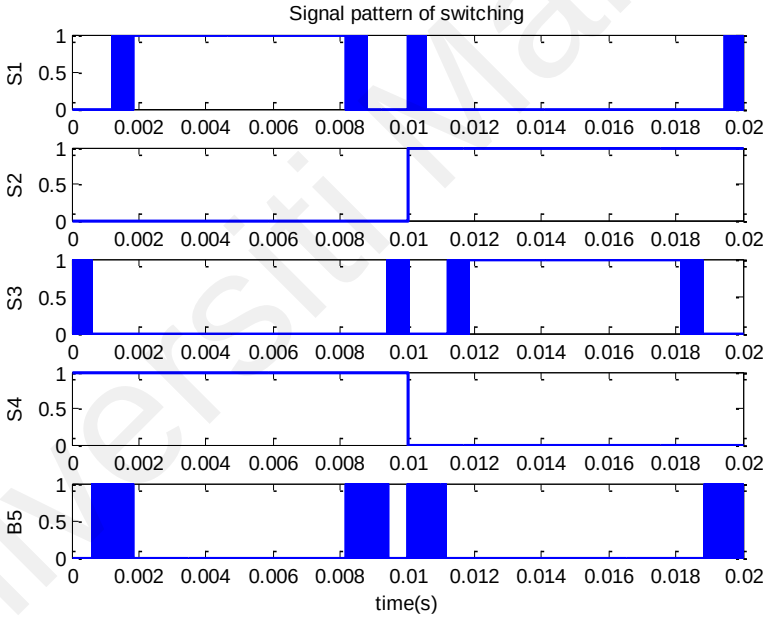


Figure 4.34: Switching Signals for Switches S1, S2, S3, S4, & B5

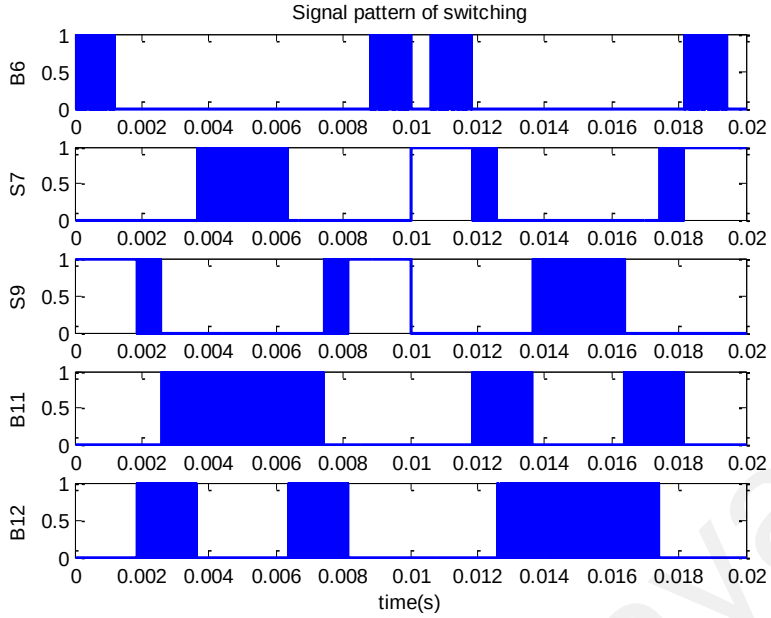


Figure 4.35: Switching Signals for Switches B6, S7, S8, S9, & S4

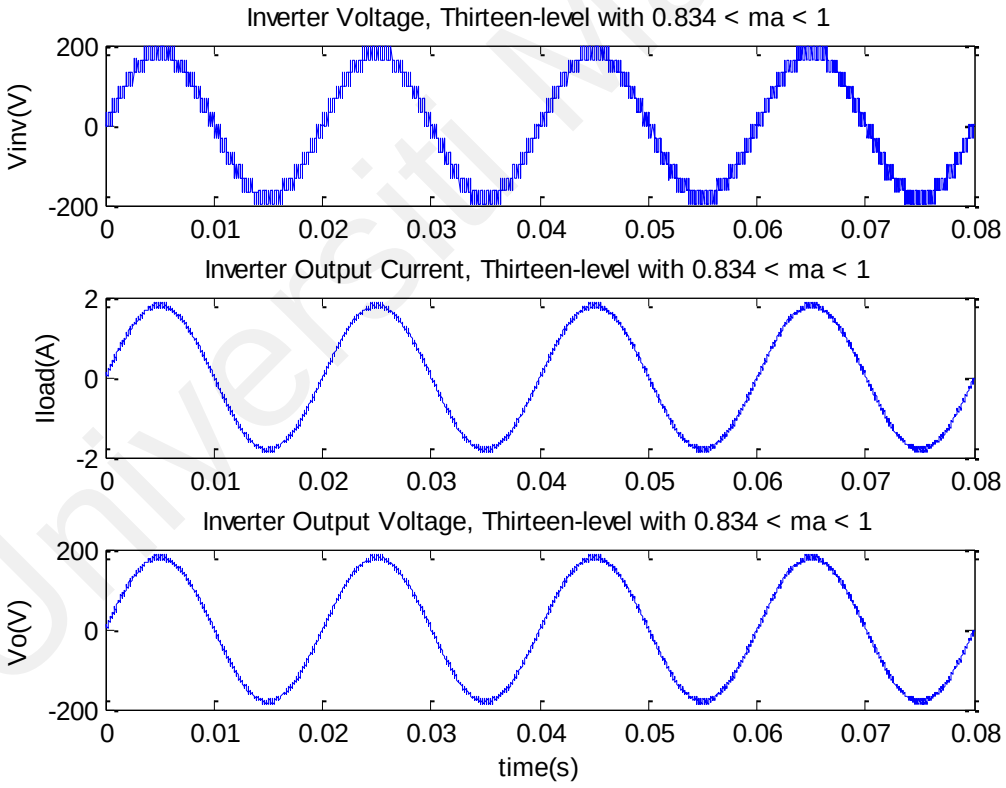


Figure 4.36: Inverter-Voltage, Output-Current and Output-Voltage waveforms of the proposed PiCHB inverter when $\boldsymbol{M_a = 0.93}$ was set between 0.83 and 1

For M_a set to exceed 0.83 but below 1, the proposed PiCHB MLI will generate a thirteen-level output-voltage waveform to form the pre-filtered voltage Vin.

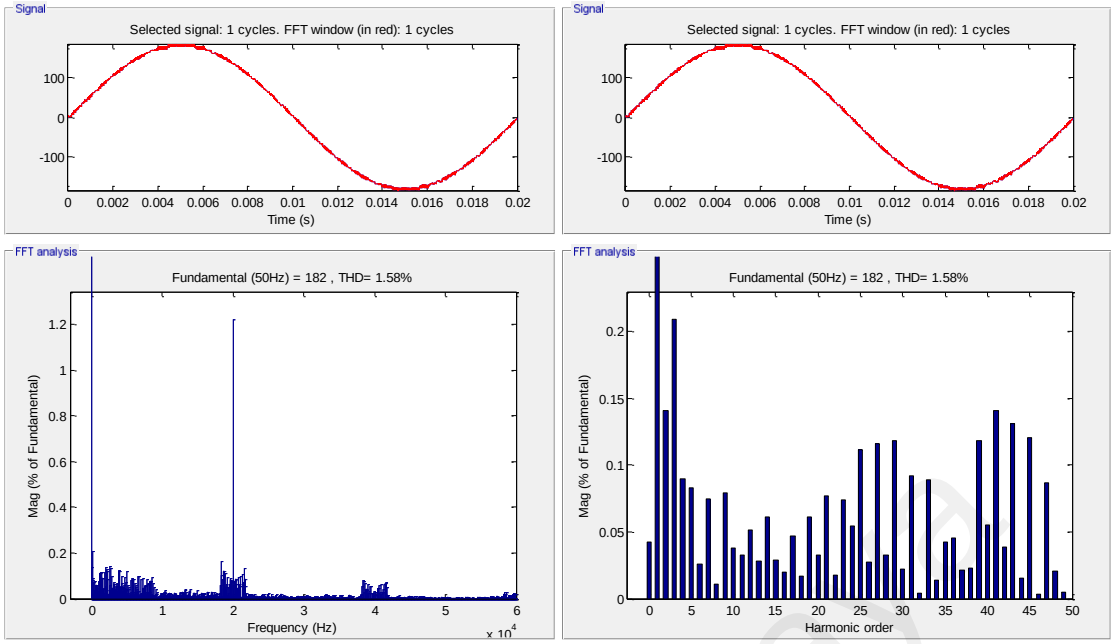


Figure 4.37: FFT analysis of Output-Voltage waveforms of the proposed TCHB inverter when $\boldsymbol{M_a}$ was set between 0.83 and 1

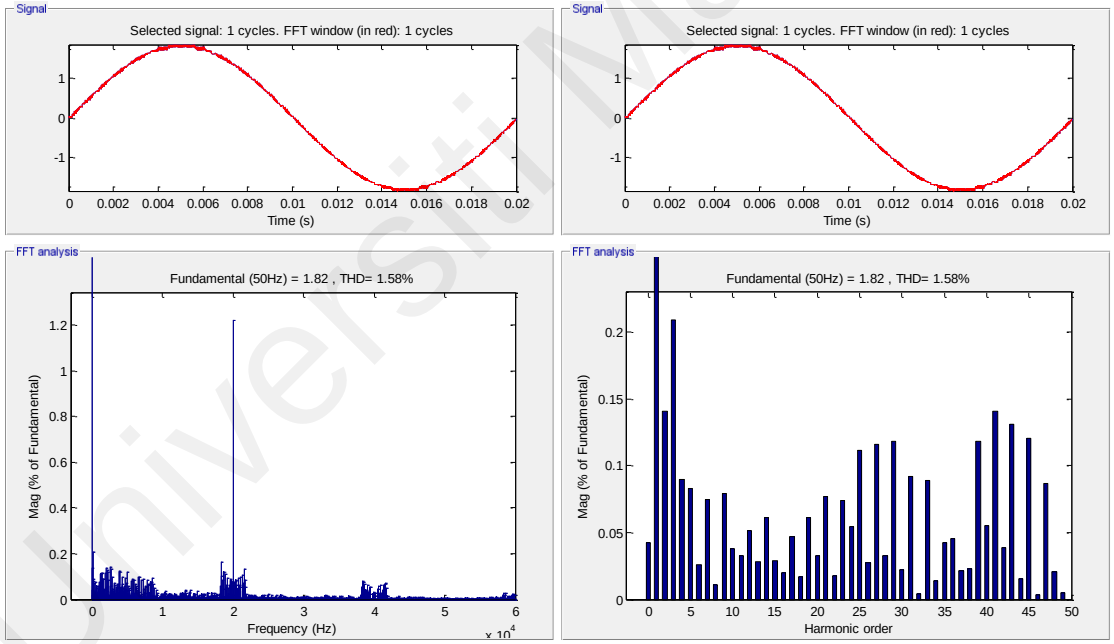


Figure 4.38: FFT analysis of Output-Current waveforms of the proposed TCHB inverter when $\boldsymbol{M_a}$ was set between 0.83 and 1

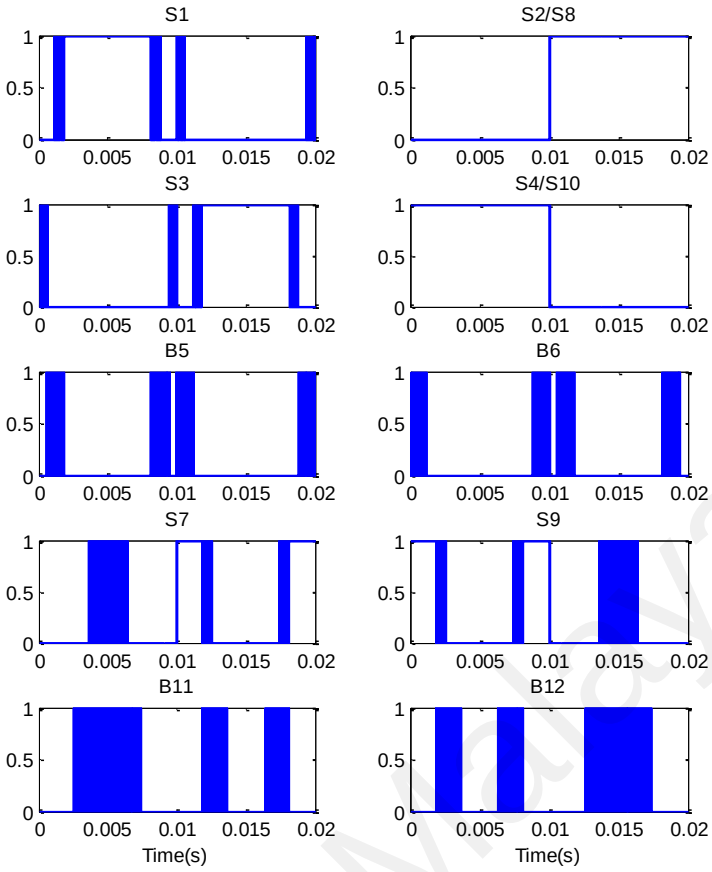


Figure 4.39: Switching signals for all switches

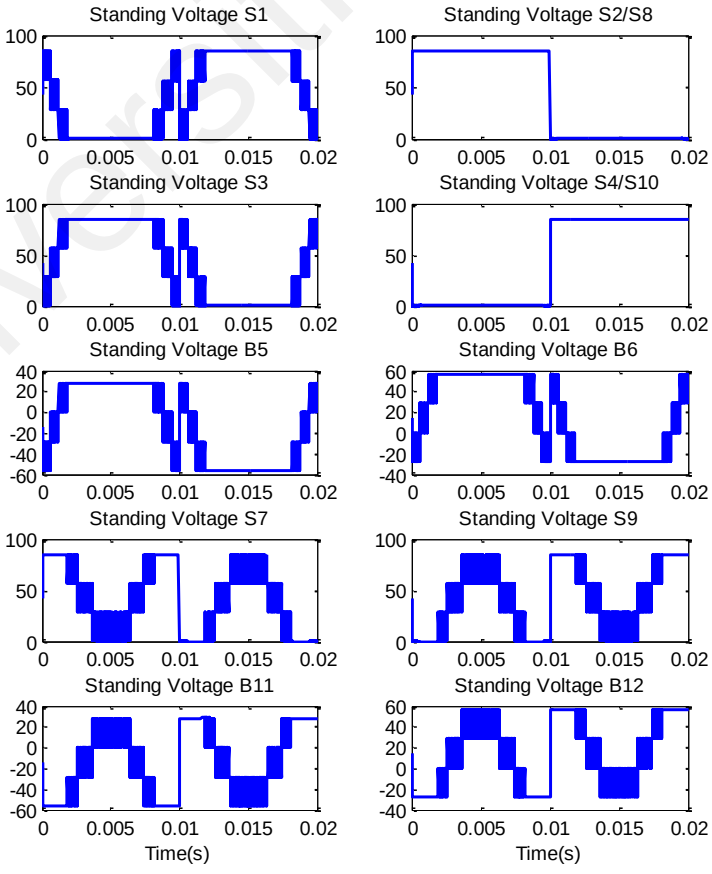


Figure 4.40: Corresponding standing-voltage on the Switches

Figure 4.36 shows inverter-voltage, output-current and the output-voltage waveforms of the proposed PiCHB inverter when the modulation index M_a was set to be between 0.83 and 1. The post-filtering output voltage waveform and the output current waveform were sinusoidal at the load terminal, but pre-filtering, the output voltage waveform was quasi sinusoidal.

Figure 4.37 and 4.38 respectively show the harmonic content of the output-voltage and of the output-current. The output-voltage THD was 1.58%. At these conditions the output current THD was also 1.58%. Figure 4.39 displays the switching signals for all switches and Figure 4.40 the corresponding standing voltages on the semiconductor switches. For M_a set to exceed 0.667 but below 0.83, the proposed PiCHB MLI will generate an eleven-level output-voltage waveform to form the pre-filtered voltage Vin. As observed, the simulation was performed for 0.02 seconds to attain one cycle of operation at 50 Hz being the output frequency.

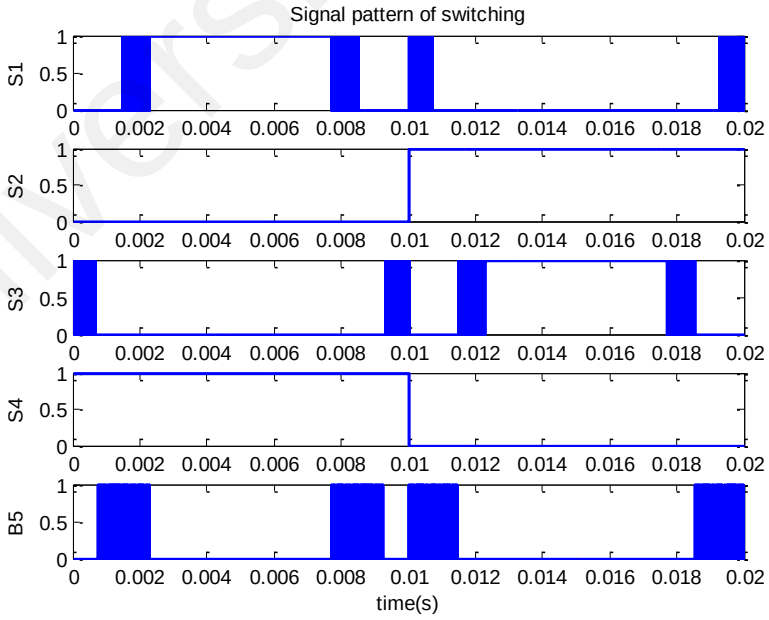


Figure 4.41: Switching Signals for Switches S1, S2, S3, S4, & B5

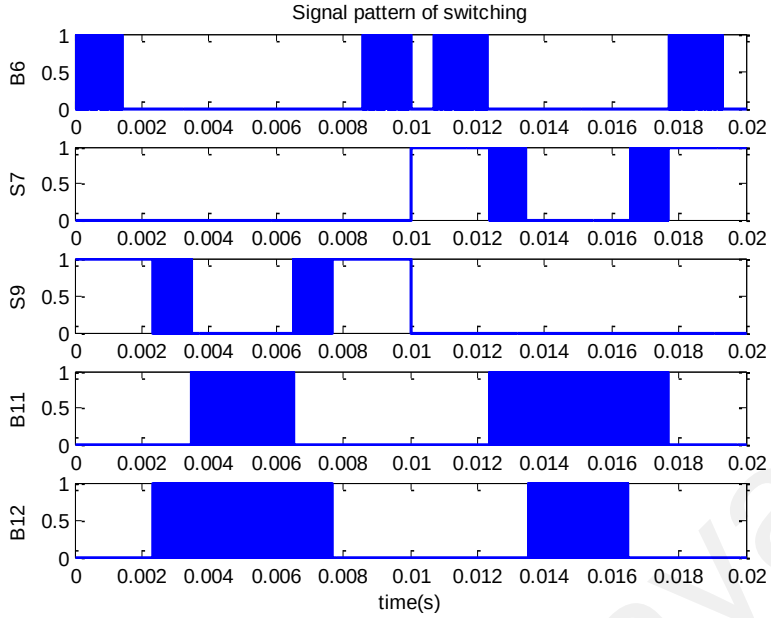


Figure 4.42: Switching signals for switches B6, S7, S9, B11 and B12

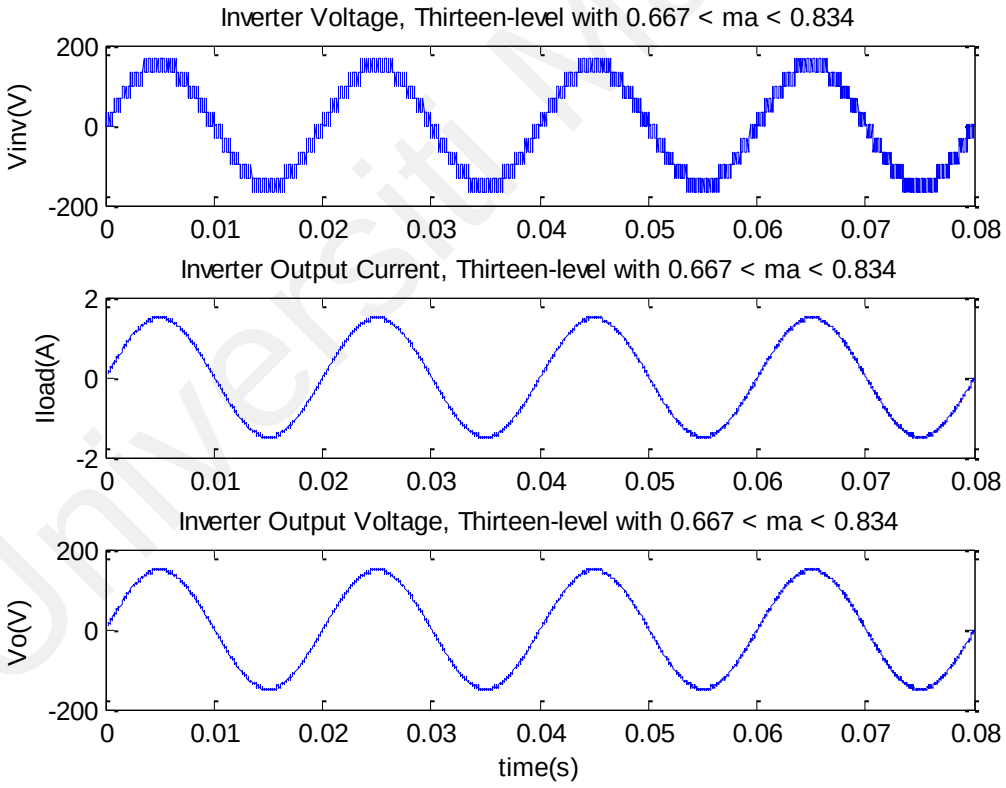


Figure 4.43: Inverter-Voltage, Output-Current and Output-Voltage waveforms of the proposed PiCHB inverter when $\boldsymbol{M_a = 0.75}$ was set between 0.67 and 0.83

Figure 4.41 and 4.42 show the resulting PWM switching signals for switches S1-B12.

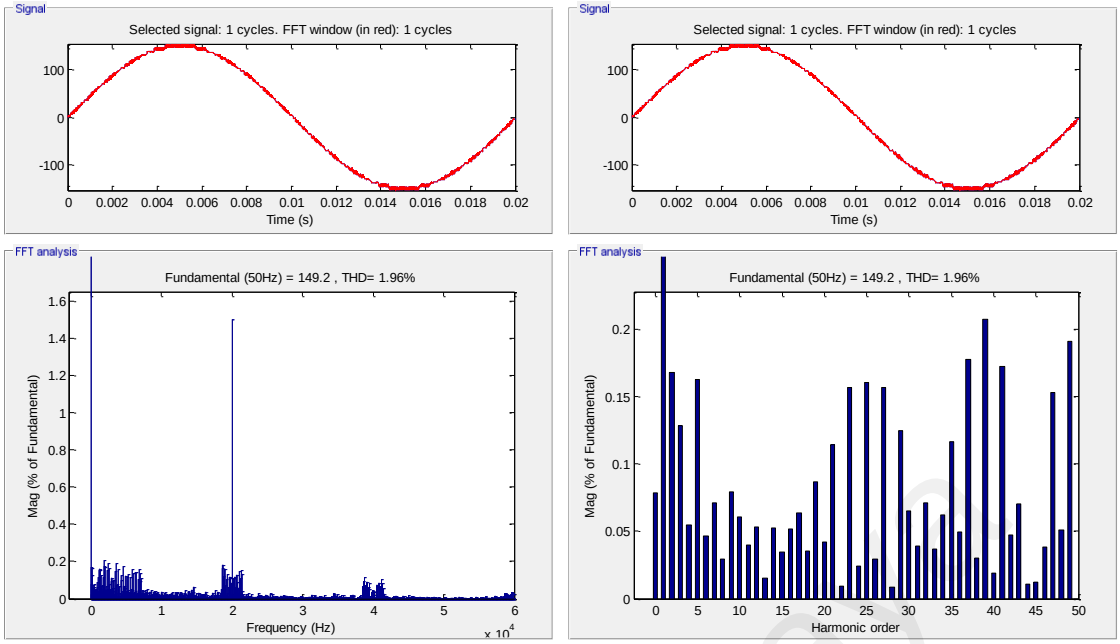


Figure 4.44: FFT analysis of Output-Voltage waveforms of the proposed TCHB inverter when $\boldsymbol{M_a}$ was set between 0.67 and 0.83

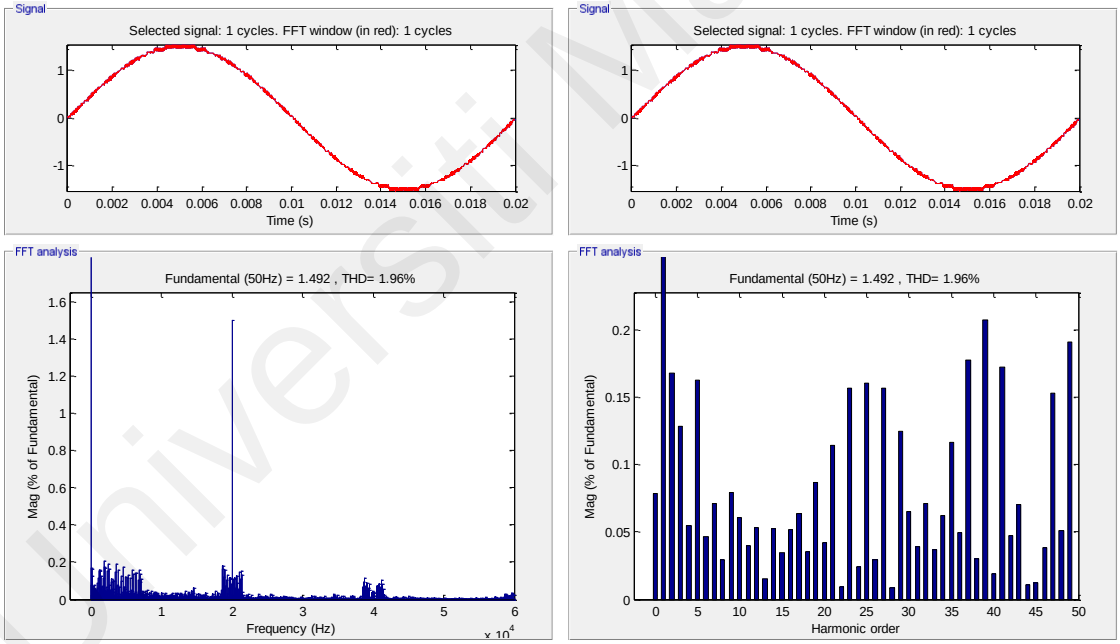


Figure 4.45: FFT analysis of Output-Current waveforms of the proposed TCHB inverter when $\boldsymbol{M_a}$ was set between 0.67 and 0.83

Figure 4.43 shows the inverter-voltage, output-current and the output-voltage waveforms of the proposed PiCHB inverter when the modulation index M_a was set to be between 0.67 and 0.83. Here, the M_a was set at 0.75.

The post-filtering output voltage waveform and the output current waveform were sinusoidal at the load terminal, but pre-filtering, the output voltage waveform was quasi sinusoidal. Figure 4.44 and 4.45 show the harmonic content of the output-voltage and of the output-current, respectively. The output-voltage THD was 1.96%. At these conditions the output-current THD was also 1.96%.

For M_a set to exceed 1, the proposed PiCHB MLI will generate an output-voltage waveform to form the pre-filtered voltage Vin with chopped highest level. Figure 4.46 and 4.47 show the resulting PWM switching signals for switches S1-B12. Figure 4.48 shows the inverter-voltage, output-current and the output-voltage waveforms of the proposed PiCHB inverter when the modulation index M_a was set to exceed 1.

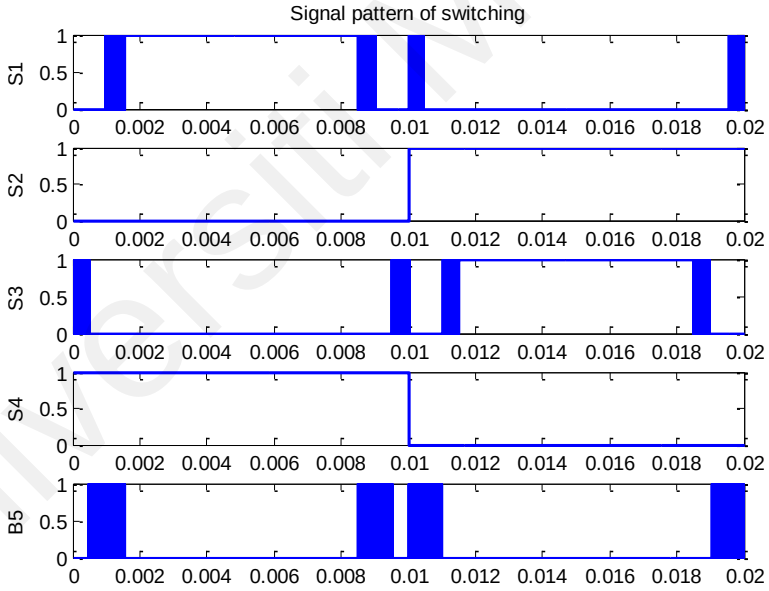


Figure 4.46: Switching signals for switches S1,S2,S3 and S4

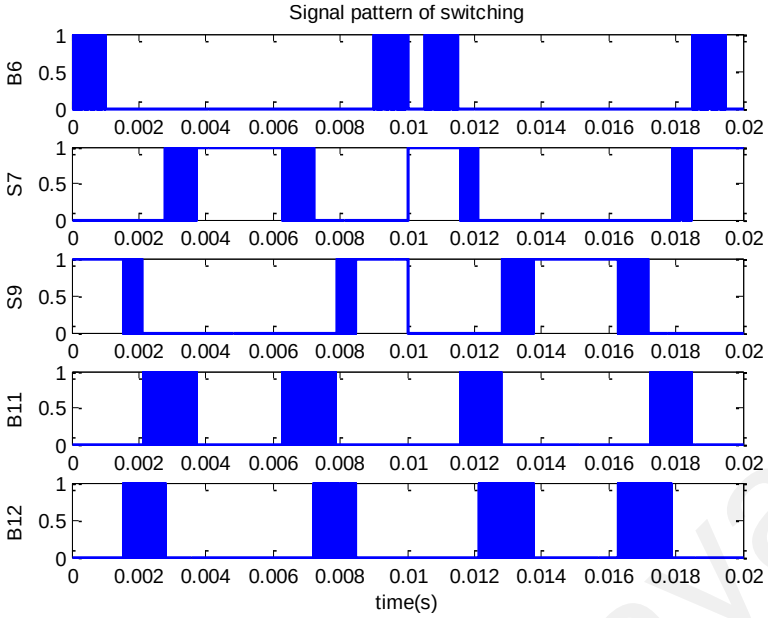


Figure 4.47: Switching signals for switches B6, S7, S9, B11 and B12

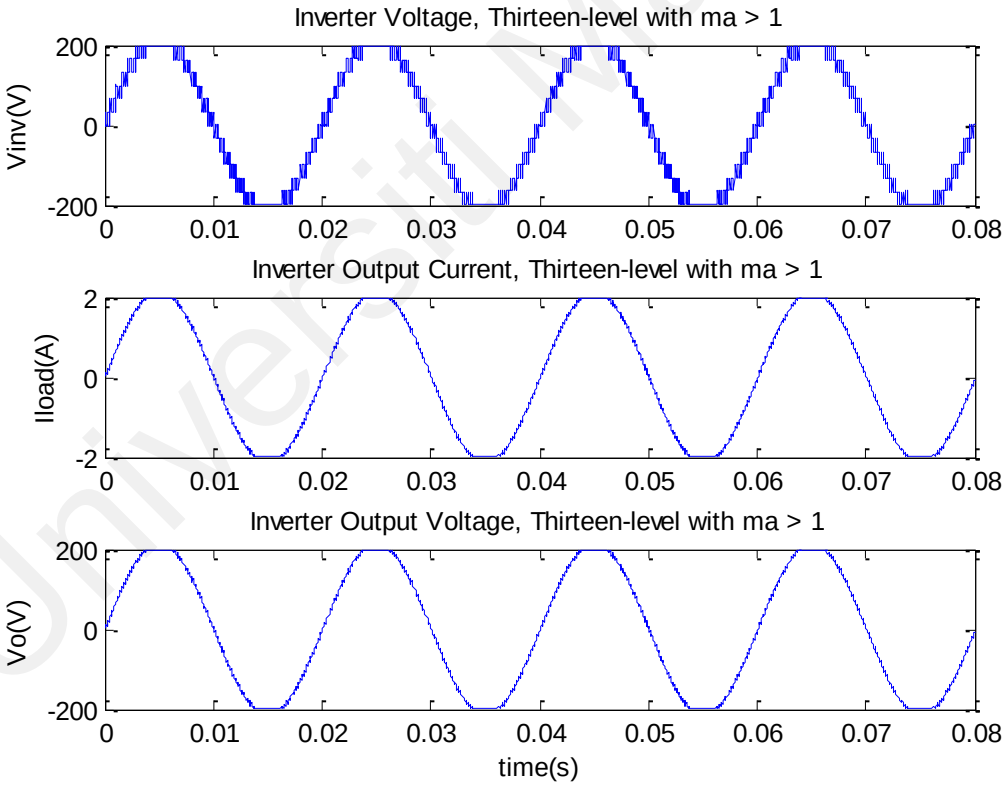


Figure 4.48: Inverter-voltage, output-current and output-voltage waveforms of proposed PiCHB inverter when modulation index $\boldsymbol{M_a = 1.17}$ was set to exceed 1

The post-filtering output voltage waveform and the output current waveform were sinusoidal at the load terminal, but pre-filtering, the output voltage waveform was quasi sinusoidal. Here, the M_a was set at 1.17.

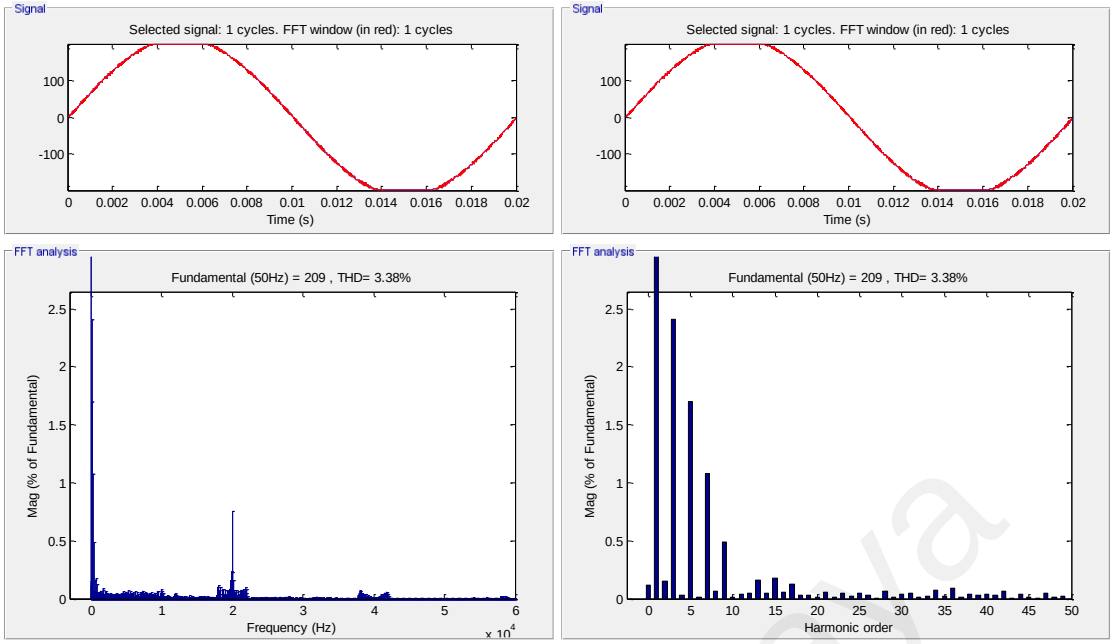


Figure 4.49: FFT analysis of Output-Voltage waveforms of the proposed PiCHB inverter when $\boldsymbol{M_a}$ was set exceed 1

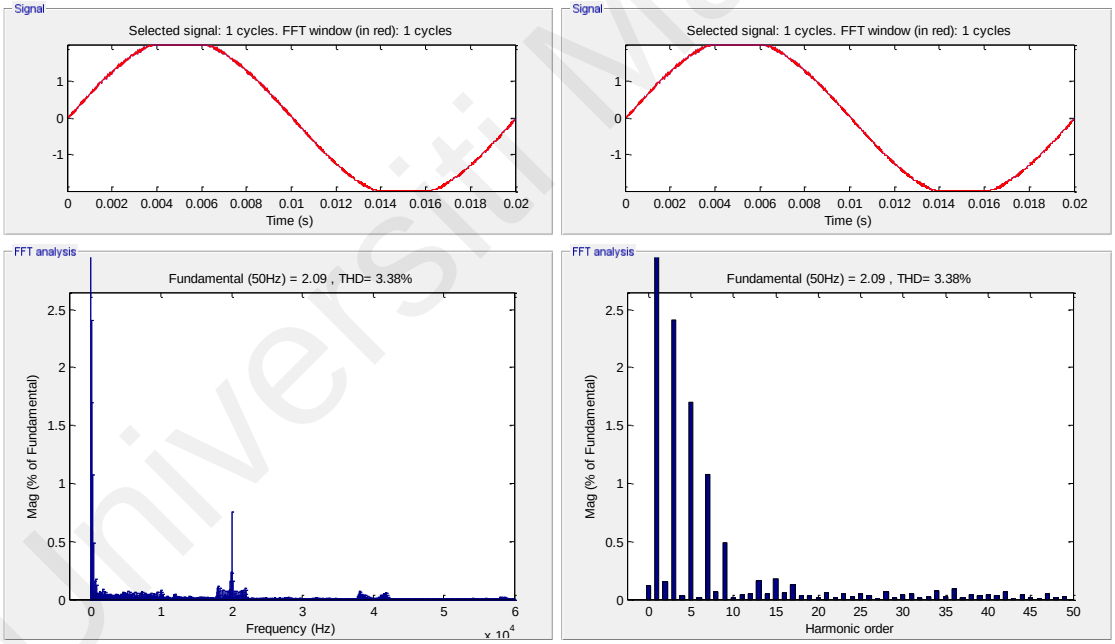


Figure 4.50: FFT analysis of Output-Current waveforms of the proposed PiCHB inverter when $\boldsymbol{M_a}$ was set exceed 1

Figure 4.49 and 4.50 show the harmonic content of the output-voltage and of the output-current, respectively. The output-voltage THD was 3.38%. At these conditions the output-current THD was also 3.38%. As observed, the simulation was performed for 0.02 seconds to attain one cycle of operation at 50 Hz being the output frequency. Table 4.1 presents a comparative analysis of the TCHB and PiCHB MLI considering the parameters

of output-voltage and output-current THD for low-frequency (LF) and high frequency (PWM) switching. Figure 4.51 presents the THD comparison of the MLI against a wide range of Modulation Index (Ma).

Table 4.1: THD Comparison of the proposed MLI

MLI	Output-Voltage THD (%)	Output Current THD (%)
TCHB with LF	9.90	9.91
PiCHB with LF	6.25	6.3
TCHB with PWM, M_a > 0.75 and < 1	2.56	2.56
PiCHB with PWM, M_a > 0.83 and < 1	1.58	1.58
TCHB with PWM, M_a > 0.5 and < 0.75	3.59	3.59
PiCHB with PWM, M_a > 0.67 and < 0.83	1.96	1.96
TCHB with PWM, M_a > 1	5.01	5.01
PiCHB with PWM, M_a > 1	3.38	3.38

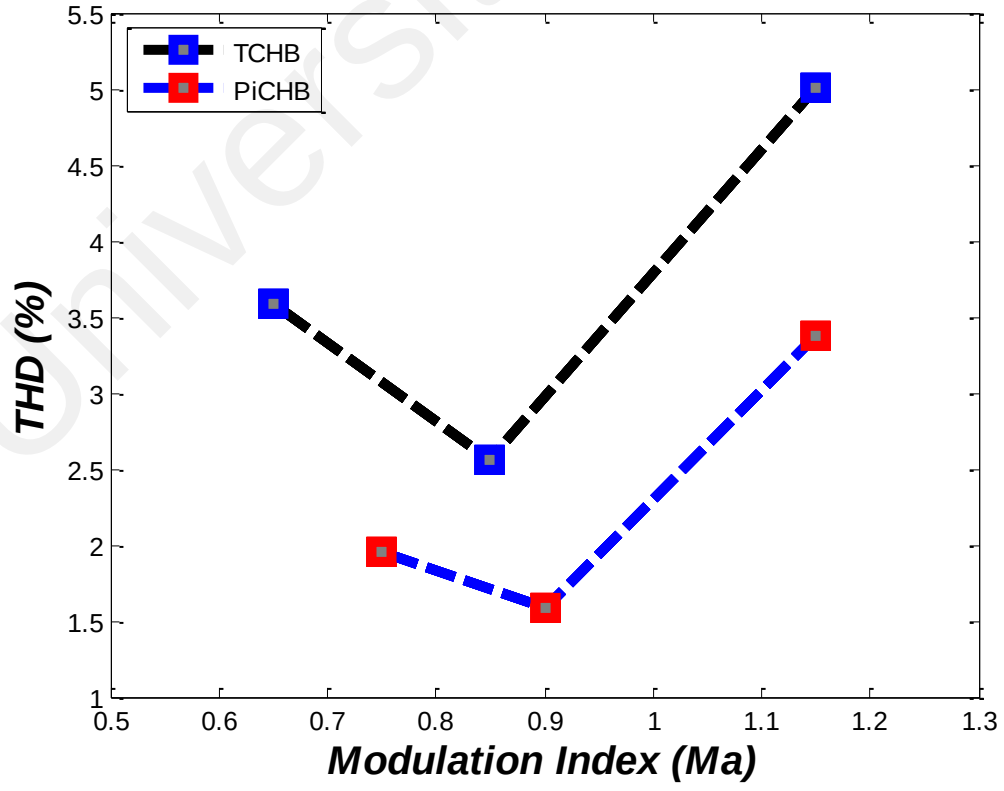


Figure 4.51: Comparison of THD (%) Vs Modulation Index (Ma)

4.4 Simulation for mINC MPPT on Various DC-DC Converters

Matlab/Simulink software was utilized to simulate the performances of the mINC on modified boost and buck converters. Table 4.2 and 4.3 present the system and PV module parameters utilized for the attaining the simulation results. The MPPT frequency was set to be 0.1 s.

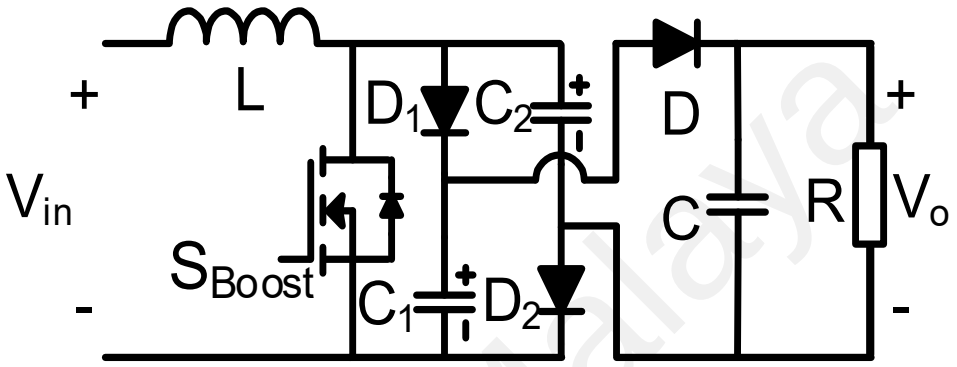


Figure 4.52: Modified Boost Converter

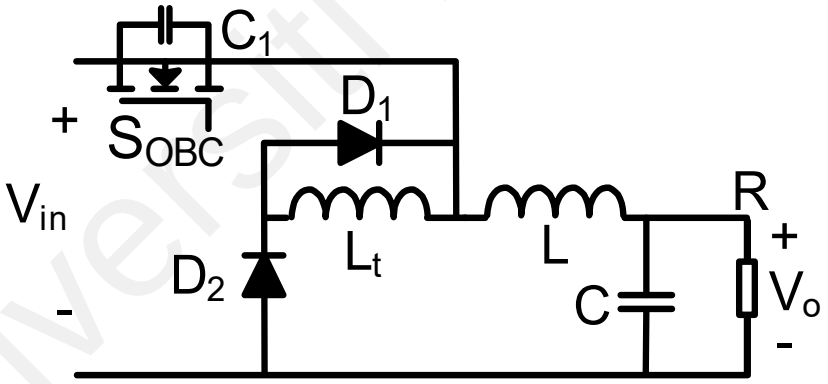


Figure 4.53: Modified Buck Converter

Figure 4.52 presents the schematic diagram of the modified boost converter and the Figure 4.53 presents the schematic for the modified buck converter. The PV system used to attain the simulation results has been displayed in Figure 4.54. From time 0 s to 3 s the results are obtained under Standard Test Conditions (STC). PV voltage and PV power change for the modified Boost and Buck Converters of MINC have been presented in Figures 4.55 and 4.56, respectively.

Table 4.2: System parameters for DC-DC Converters

Parameters	2-SSC Boost Converter	Optimized Buck Converter
Switching frequency	20kHz	20kHz
Sampling time	0.1s	0.1s
Input capacitor	2200 µF	2200 µF
Switch capacitor	1 µF	-
Inductor (L)	560 µH	560 µH
Inductor (Lt)	-	0.5 µH
Filter capacitor	220 µF	220 µF
Load	15Ω	1Ω

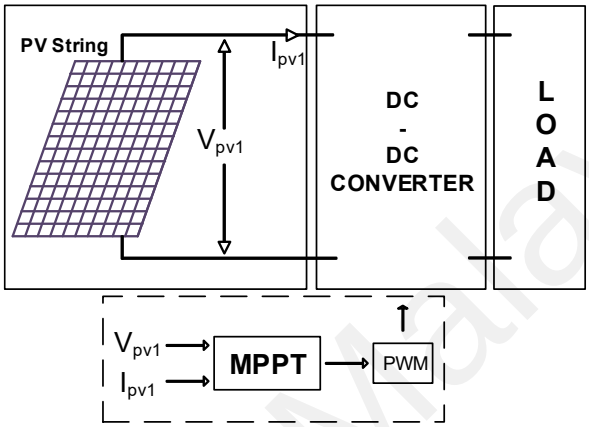


Figure 4.54: PV system with proposed mINC MPPT

Table 4.3: Parameters for Kyocera KC85T PV Panel

Parameters	Value
Vmpp	17.4 V
V_{OC}	21.7 V
Impp	5.02 A
I_{SC}	5.34 A
Pmpp	87 W
Series cells	36

Table 4.4 presents the evaluation of the mINC MPPT implementation on the modified Boost and Buck converter. As displayed for Modified Boost converter the mINC MPPT oscillates during the steady state of operation and the actual MPP attain remains 84.7 W, whereas the exact MPP was 87 W. The MPPT efficiency was 97.35%. Similarly, as displayed for Modified Buck converter the mINC MPPT oscillates during the steady state

of operation and the actual MPP attain remains 84.5 W, whereas the exact MPP was 87 W. The MPPT efficiency remained 97.12%.

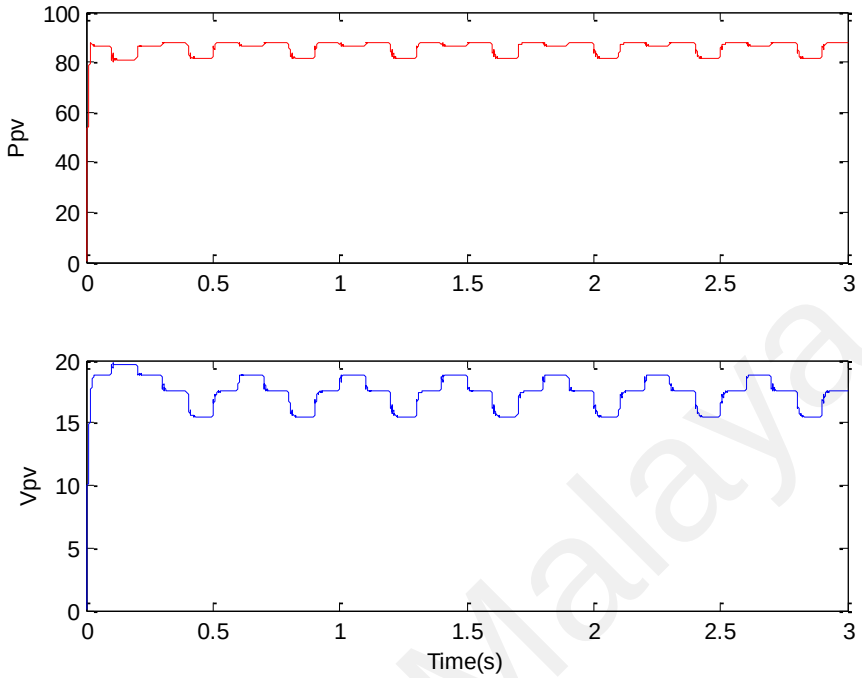


Figure 4.55: Simulation results for MINC on Modified Boost Converter

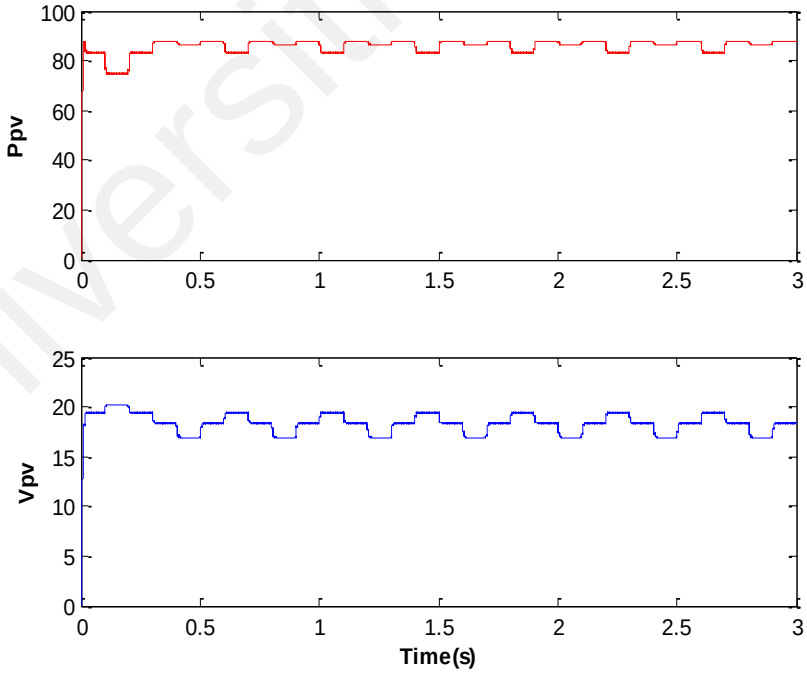


Figure 4.56: Simulation results for MINC on Modified Buck Converter

Table 4.4: Evaluation of mINC MPPT implemented on DC-DC Converters

MPPT Technique	No. of Steps	Settling time	Exact MPP	Actual MPP	Efficiency
mINC on Modified Boost Converter	-	Oscillating	87 W	84.7 W	97.35 %
mINC on Modified Buck Converter	-	Oscillating	87 W	84.5 W	97.12 %

4.5 Simulation for Grid-Tied PV Application

In order to simulate the proposed-inverter models for the grid-tied PV application, a PV-module model representative of PV-module characteristics was also employed. I-V and P-V curves were simulated on MATLAB, for various irradiances. The SIEMENS SP75 module was utilized, in the MATLAB simulation and experiment prototype. Table 4.5 indicates the SIEMENS SP75 PV module's characteristics. In addition, Table 4.6 presents the module characteristics for a PV string with five panels connected in series.

Table 4.5: Characteristics of the PV module

Model: SIEMENS SP75	
Parameter	**Value**
No. of Panels	1
$\mathbf{V_{MPP}}$	17.0 V
$\mathbf{V_{OC}}$	21.7 V
$\mathbf{I_{MPP}}$	4.4 A
$\mathbf{I_{SC}}$	4.8 A
$\mathbf{P_{MPP}}$	75 W

Table 4.6: Characteristics of the five PV modules connected in series

Model: SIEMENS SP75	
Parameter	**Value**
No. of Panels	5
$\mathbf{V_{MPP}}$	85.0 V
$\mathbf{V_{OC}}$	108.5 V
$\mathbf{I_{MPP}}$	4.4 A
$\mathbf{I_{SC}}$	4.8 A
$\mathbf{P_{MPP}}$	375 W

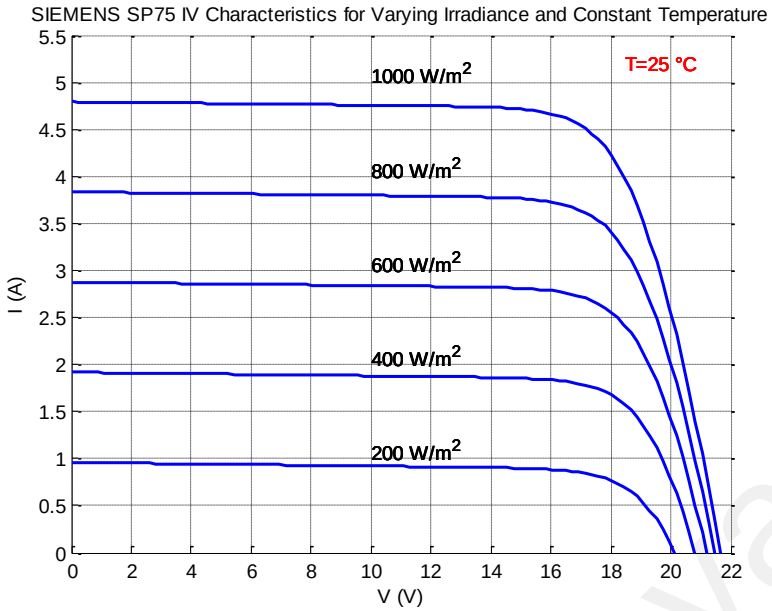


Figure 4.57: I-V curves for various irradiances and constant temperature

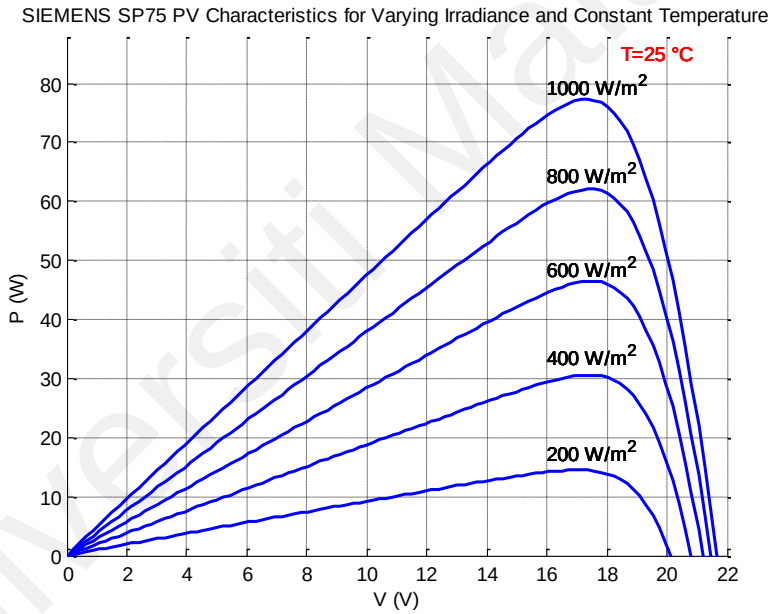


Figure 4.58: P-V curves for various irradiances but constant temperature

Figure 4.57 is the I-V curve for the PV-module simulated at constant 25°C temperature and variable irradiance. In addition, the P-V curves were simulated on MATLAB, for various irradiances and constant temperature as presented in Figures 4.58.

4.5.1 TCHB inverter

Figure 4.59 is the simulation setup of the proposed TCHB multilevel inverter in grid-connected PV application. Five SIEMENS SP 75 modules were serially-connected for

each cascade. The boost converters had inductors $L = 3m$H, the filter inductor being $L = 5m$H and capacitors C_1, C_2, and C_3, each 2200μF. Ratio of the primary and the secondary of the low-frequency transformer was 1:2. The grid-frequency was 50Hz and the AC voltage rms was 240V.

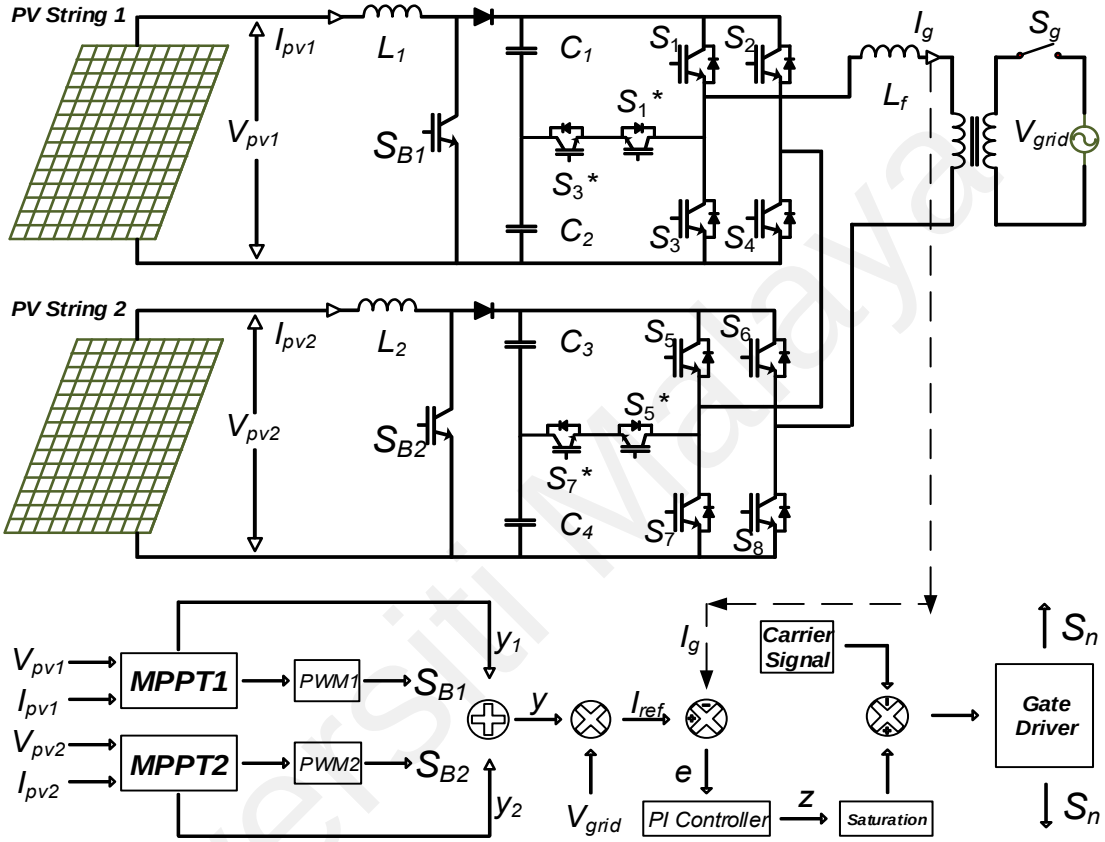


Figure 4.59: Simulation setup of the TCHB grid-connected PV inverter

Extraction of maximum power from the PV modules was by mINC method. Proportional (P) controller was used for the voltage-regulating boost converter, its proportional gain $K_p = 100$. Proportional Integrator (PI) controller was applied to the current controller, with proportional gain $K_p = 10$ and integrator gain $K_i = 0.1$. Table 4.7 presents the system parameters for the TCHB inverter. Here, a 1:2 ratio transformer has been utilized to step up the inverter voltage V_{inv}. Higher than $\sqrt{2}\ of\ V_{grid}$ at the DC-bus is required to inject current into the grid, so a boost converter of each individual cascade has been is utilized. Figure 4.60 presents the reference tracking by the step

response of the PI current control scheme, while Figure 4.61 presents the zoomed view of the reference tracking.

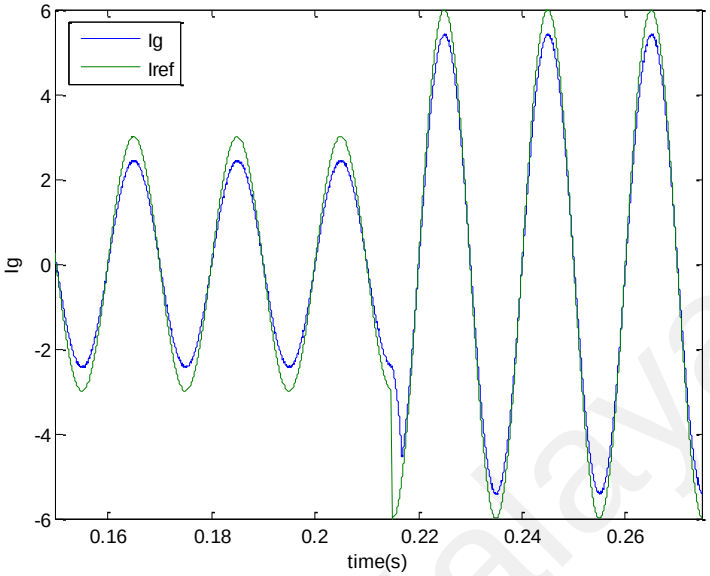


Figure 4.60: Step response of PI current control scheme

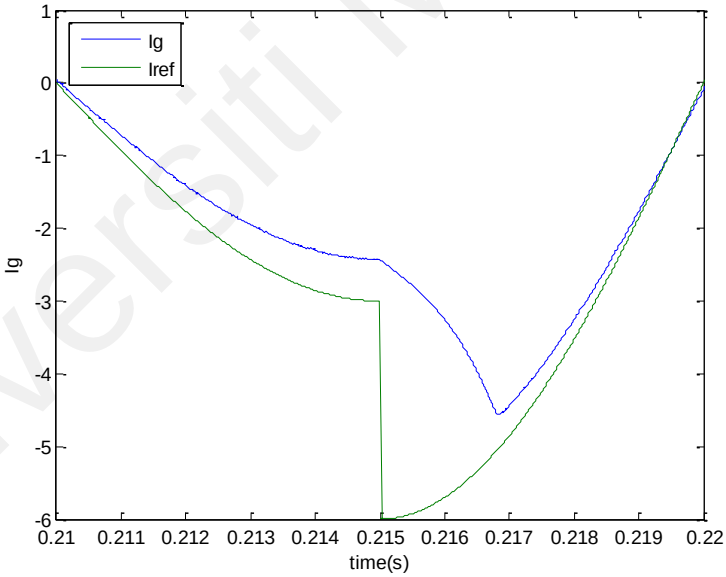


Figure 4.61: Zoomed view of the reference tracking

Table 4.7: System parameters for TCHB

Parameter	Value
Switching Frequency	20kHz
Sampling Frequency	78kHz
$\mathbf{C_{1,2,3,4}}$	2200μF
$\mathbf{L_{1,2}}$	3mH
$\mathbf{L_f}$	5mH
$\mathbf{K_P}$	10
$\mathbf{K_i}$	0.1

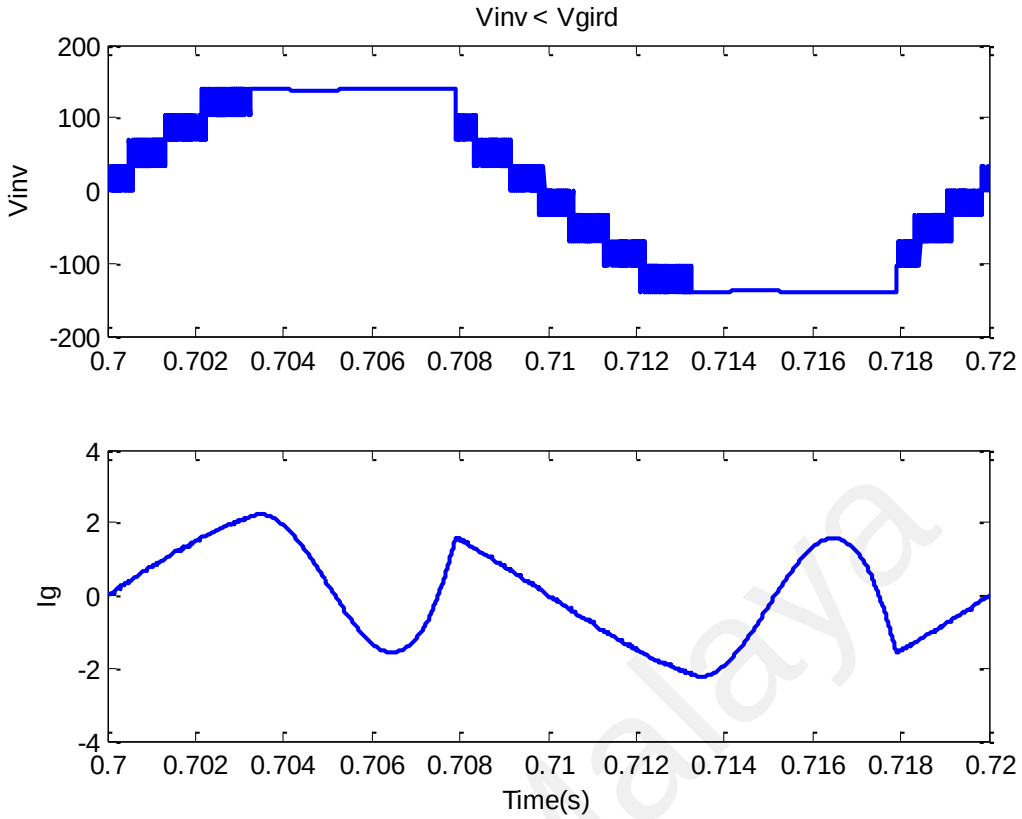


Figure 4.62: Output-Current and Voltage when $\boldsymbol{V_{inv} < V_g}$

As for the case where $V_{inv} < V_{grid}$ current will be injected from the grid into the inverter. When the V_{inv} is made higher than V_{grid} for the case $V_{inv} > V_{grid}$ the current is injected into the grid and the V_{grid} and I_{grid} are completely in-phase. Figure 4.62 displays the case where the $V_{inv} < V_{grid}$ and the opposite has been presented in Figure 4.63. Therefore, to attain a nine-level grid-connection the inverter operation was confined between $M_a > 0.75$ && < 1.

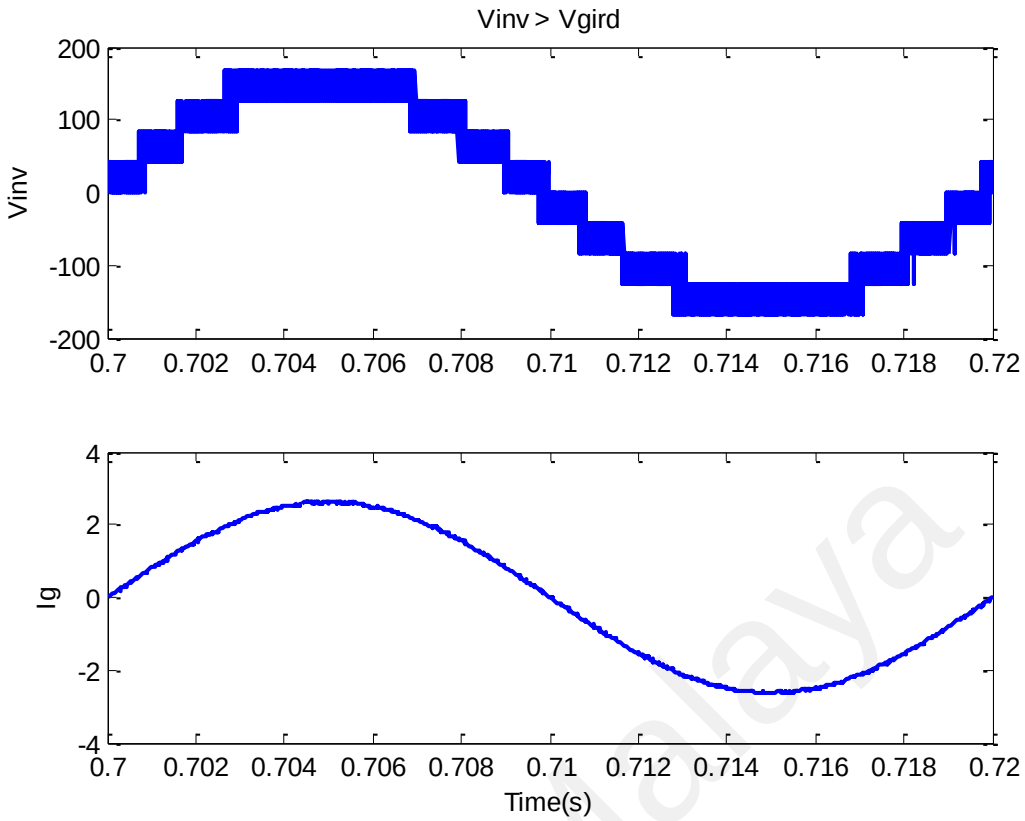


Figure 4.63: Output-Current and Voltage when $\boldsymbol{V_{inv} > V_g}$

Figure 4.64 shows the time response of the inverter's output voltage before filter, inverter's output voltage after filter, grid voltage and pre-transformer output current for MPPT mode with a linear transformer with 1:1 ratio. As observed, the TCHB MLI takes almost 0.3 seconds to attain a state where current and voltage are in phase. From 0 seconds to 0.1 seconds the MPPT tracks the optimum voltage to offer a voltage greater than the grid voltage. From 0.1 seconds to 0.3 seconds a stable steady state is attained where the current and voltage are brought in-phase with nearly unity power factor.

The post-filtering output voltage waveform and the output current waveform were sinusoidal at the load terminal, but pre-filtering, the output voltage waveform was quasi sinusoidal. In addition, Figure 4.65 shows the time response of the inverter when disconnected from the grid. Figure 4.66 is the zoomed version for the time response of the inverter when disconnected from the grid.

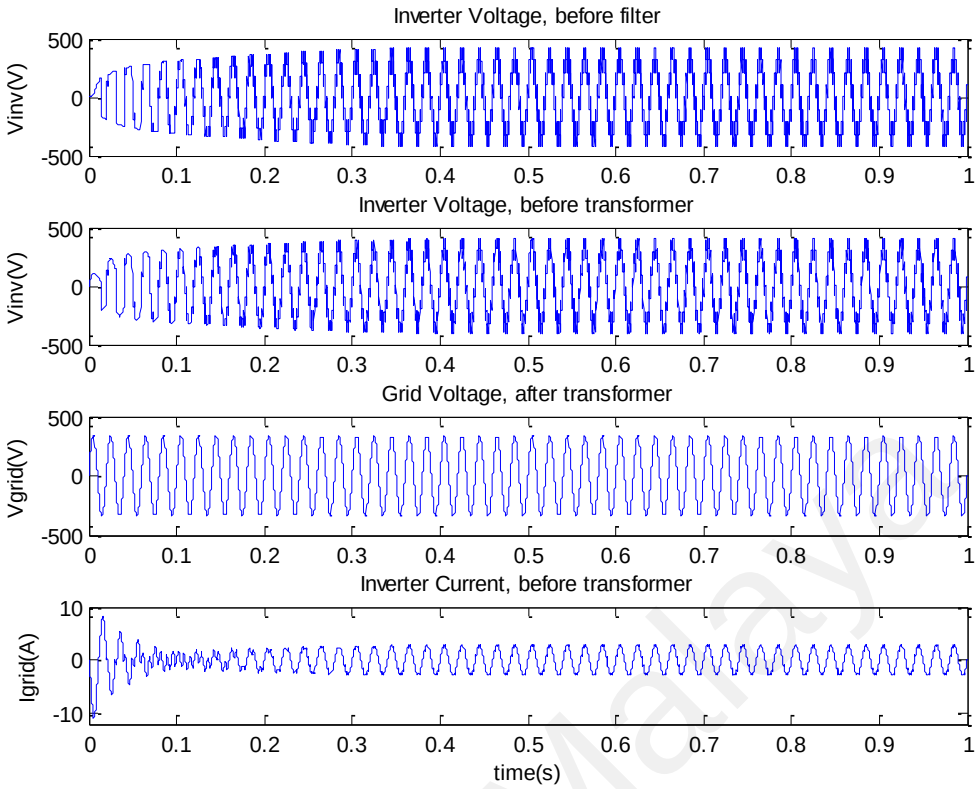


Figure 4.64: Time response of TCHB inverter

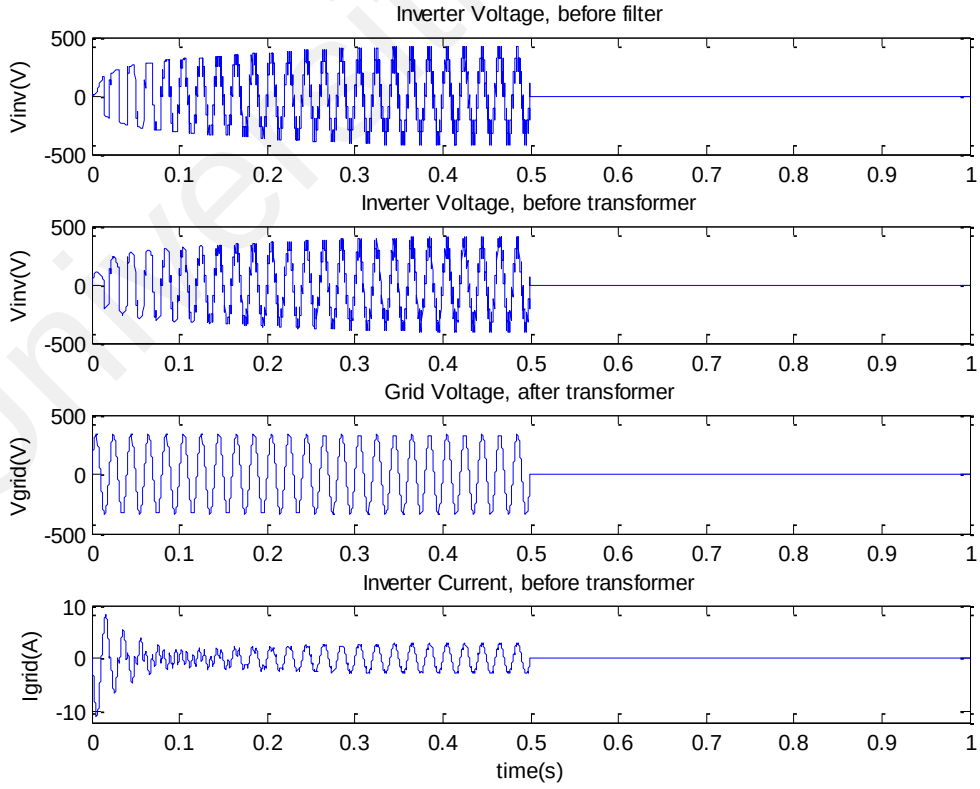


Figure 4.65: Time response of TCHB when grid is disconnected

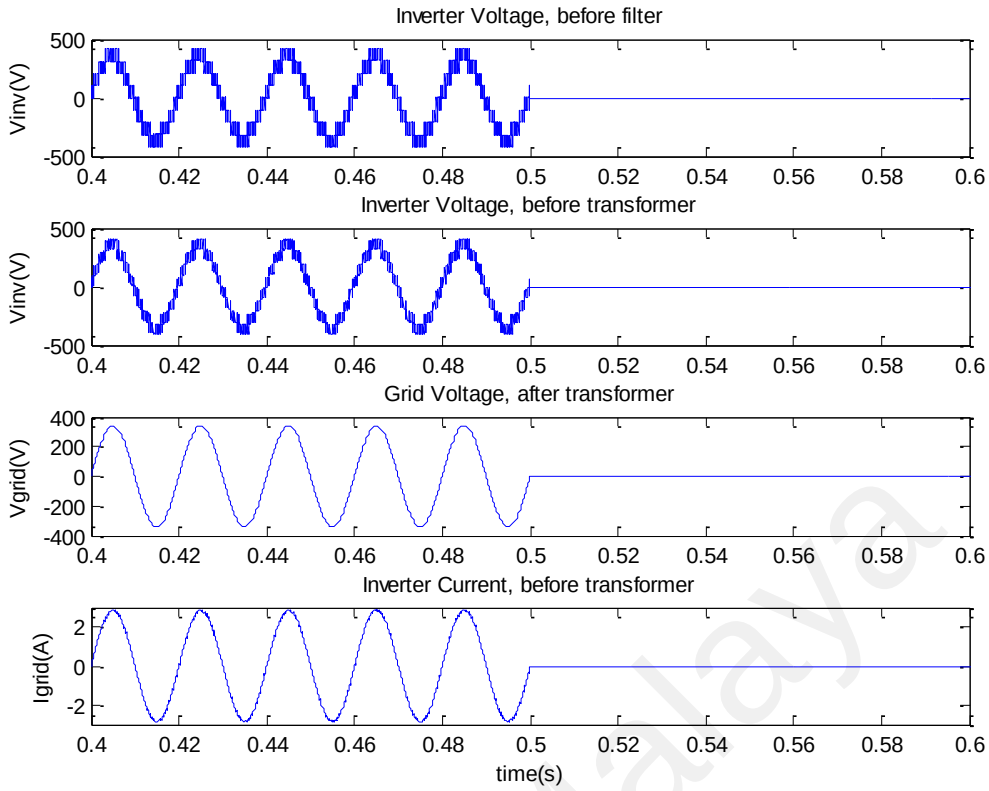


Figure 4.66: Zoomed view for the time response when grid is disconnected

4.5.2 PiCHB inverter

Figure 4.67 is the simulation setup of the proposed PiCHB multilevel inverter in grid-connected PV application. Five SIEMENS SP75 modules were serially-connected for each cascade. The boost converters had an inductor $L = 3m$H. Each cascaded utilized DC-Link capacitors C_1, C_2, and C_3, of 2200 µF each. The filter inductor was $L = 5m$H. The ratio of the primary and the secondary of the low-frequency transformer was 1:2. The grid-frequency was 50Hz and the AC voltage rms was 240V.

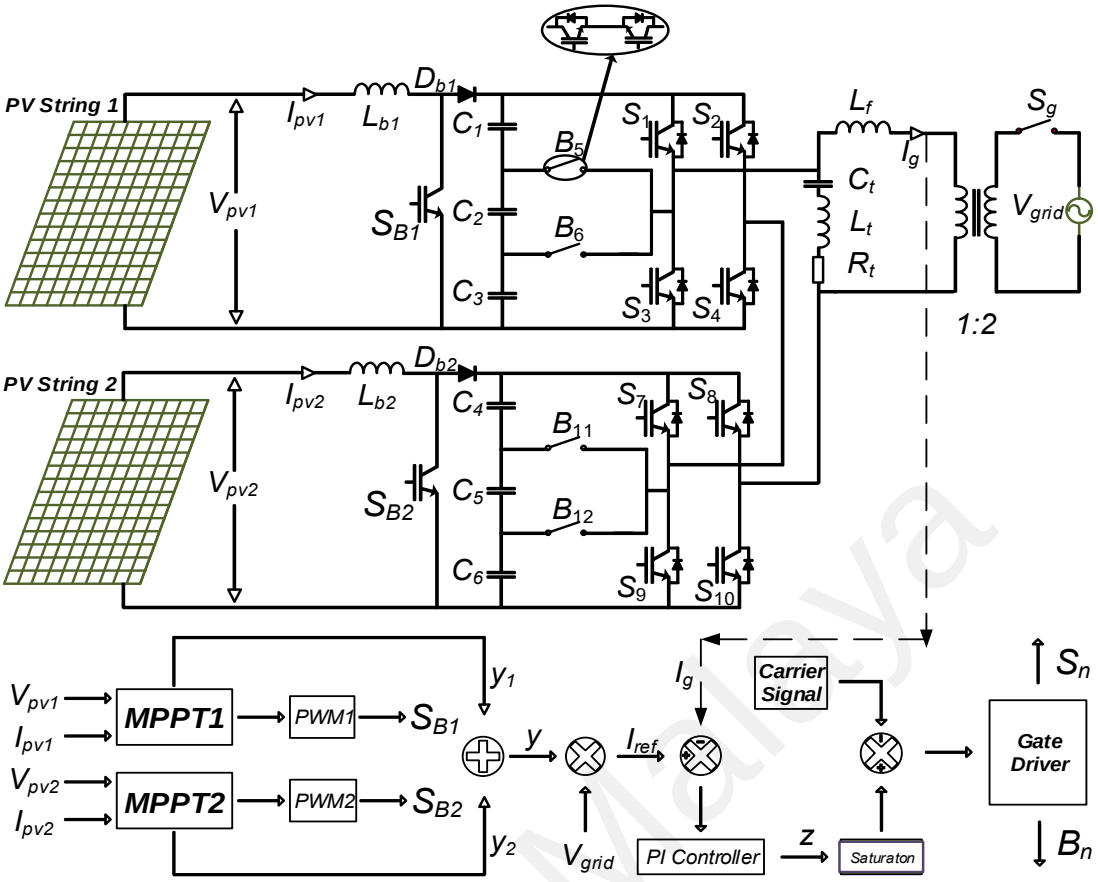


Figure 4.67: Simulation setup of the PiCHB grid-connected PV inverter

Extraction of maximum power from the PV modules was by mINC method. Proportional (P) controller was used for the voltage-regulating boost converter, its proportional gain $K_p = 100$. Proportional Integrator (PI) controller was applied to the current controller, with proportional gain $K_p = 10$ and integrator gain $K_i = 0.1$.

As, for grid current injection the dc-bus voltage must always be kept higher than $\sqrt{2}\, of\, V_{grid}$, two boost converters, one with each cascade and a 1:2 ratio transformer has been utilized to step up the inverter voltage V_{inv}. Table 4.8 presents the PiCHB system parameters.

4.5.2.1 RLC passive balancing

The passive RLC branch can provide balanced voltage sharing, however, it increases the size and cost, and decreases the efficiency of the system. Figure 4.68 presents the schematic diagram of the RLC passive circuit.

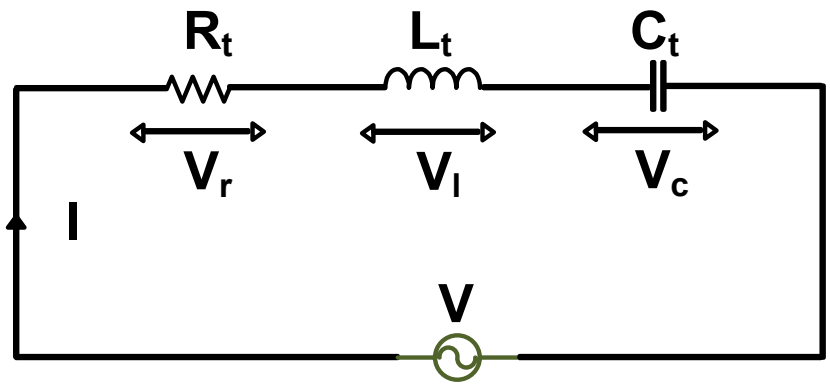


Figure 4.68: RLC passive balancing circuit

For power converters, the total harmonic distortion (THD) is a popular performance index, which evaluates the quality of the harmonic contents in the output waveform (Ali et al., 2018). For sinusoidal waveform, the THD is obtained as follows:

$$THD = \frac{\sqrt{\left(\sum_{h=3,5,7,\ldots}^{\infty} V_{o_h}\right)}}{V_{o_1}} = \sqrt{\left(\frac{V_{o_{rms}}}{V_{o_1}}\right)^2 - 1}$$

In this relation, h represents the order of the corresponding harmonic, whereas subindex 1 corresponds to the fundamental frequency. Therefore, V_{o_h} and V_{o_1} are the rms of the nth-order harmonic and fundamental of the output voltage waveform, respectively. Moreover, $V_{o_{rms}}$ represents the rms values of the output voltage. The magnitude of V_{o_1} and $V_{o_{rms}}$ can be obtained using the following relations, respectively:

$$V_{o_{rms}} = \frac{2\sqrt{2}V}{\pi} \times \sqrt{\sum_{h=1,3,5,\ldots}^{\infty} \left(\sum_{j=1}^{N_{level}} \left(\frac{\cos(h\theta_j)}{h}\right)\right)^2}$$

$$V_{o_1} = \frac{2\sqrt{2}V}{\pi} \times \sum_{j=1}^{N_{level}} \left(\cos\theta_j\right)$$

Where the values of θ_1, θ_2, …, $\theta_{N_{level}}$ are switching angles and calculated by the following equation:

$$\theta_j = \sin^{-1}\left(\frac{j-0.5}{N_{level}}\right), \quad j = 1,2,3,\ldots,Nlevel$$

In a multilevel converter, to evaluate the efficiency of the converter (η) using measurements, it is important to measure the total input power (Pinput) and output power (Poutput). Then, the efficiency of a multilevel converter is evaluated by the following equation:

$$\eta = \frac{P_o}{P_i}$$

A Trapezoidal sum approximation is used for the discrete-time domain transformation, where $z(t)$ remains the control signal, K_i the integral gain; K_p the proportional gain; $e(\tau)$ the error signal, τ the integration variable and P_o the output power. Table 4.8 presents a comparative analysis of the PiCHB inverter topology with RL load against SCHB and the topology proposed in (Ebrahimi et al., 2012).

Table 4.8: Comparative analysis with RL load based on THD (%) and $\boldsymbol{\eta}$ (%)

Inverter Topology	Level	R (Ω)	L (mH)	Voltage THD %	Current THD %	η %
Proposed in (Ebrahimi et al., 2012)	13	20	55	5.90	0.64	Not given
Proposed in (Samanbakhsh & Taheri, 2016)	23	115	100	4.23	2.74	92.8
PiCHB	13	100	5	1.58	1.57	91.7

Figure 4.69 presents the capacitor voltage levels for all the DC Link capacitors involved in the PiCHB design. In case the RLC passive balancing circuit is not utilized,

the Balanced Voltage Sharing at the DC Link is disturbed and an unbalanced output voltage is obtained at the output as presented in Figure 4.70.

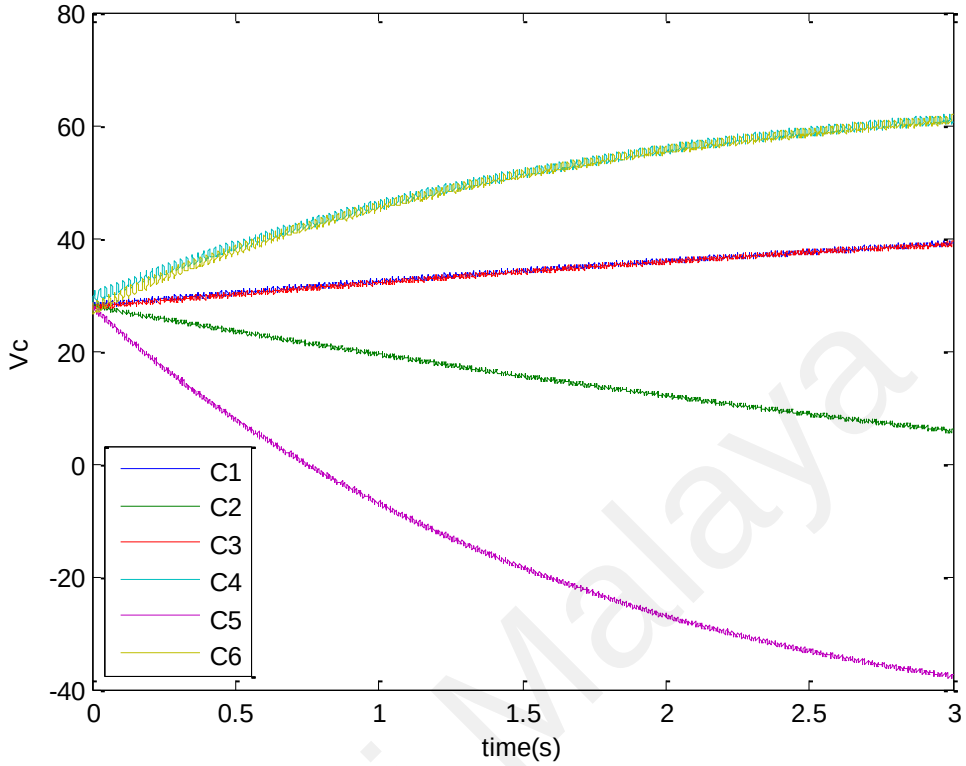


Figure 4.69: Capacitor voltage levels in unbalanced case

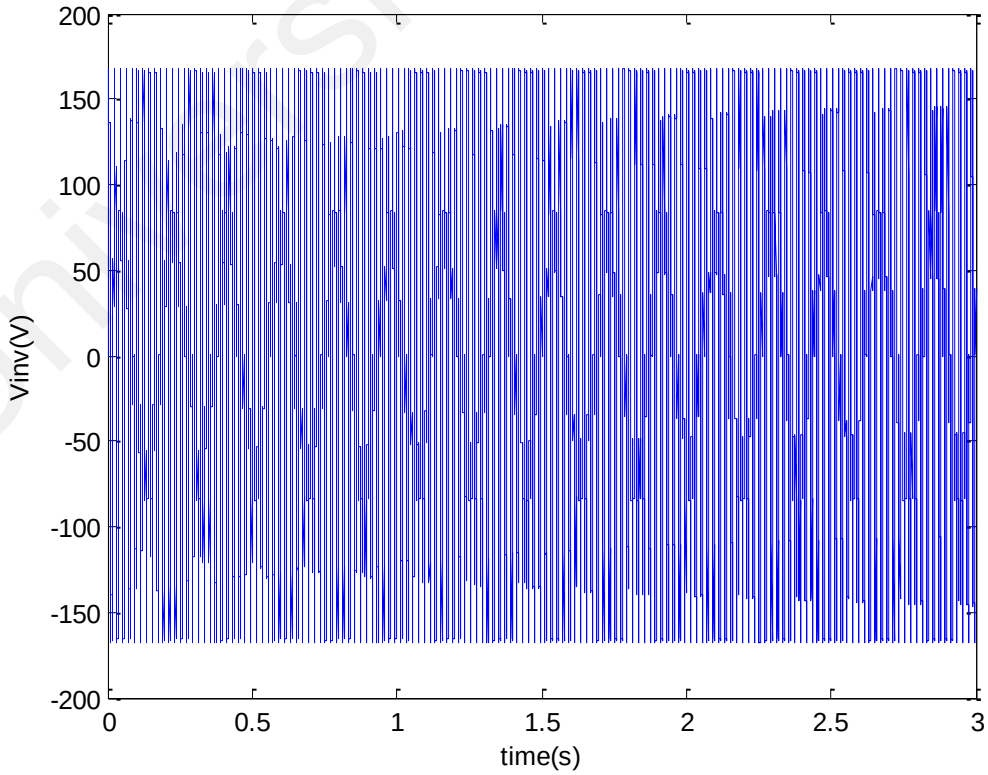


Figure 4.70: Inverter Output Voltage in Unbalanced case

Owing to its unbalanced state, the unbalanced voltage can damage the entire PV system. Figure 4.71 presents the zoomed view of the unbalanced output voltage and Figure 4.72 presents the simulation result in correspondence with experimental results.

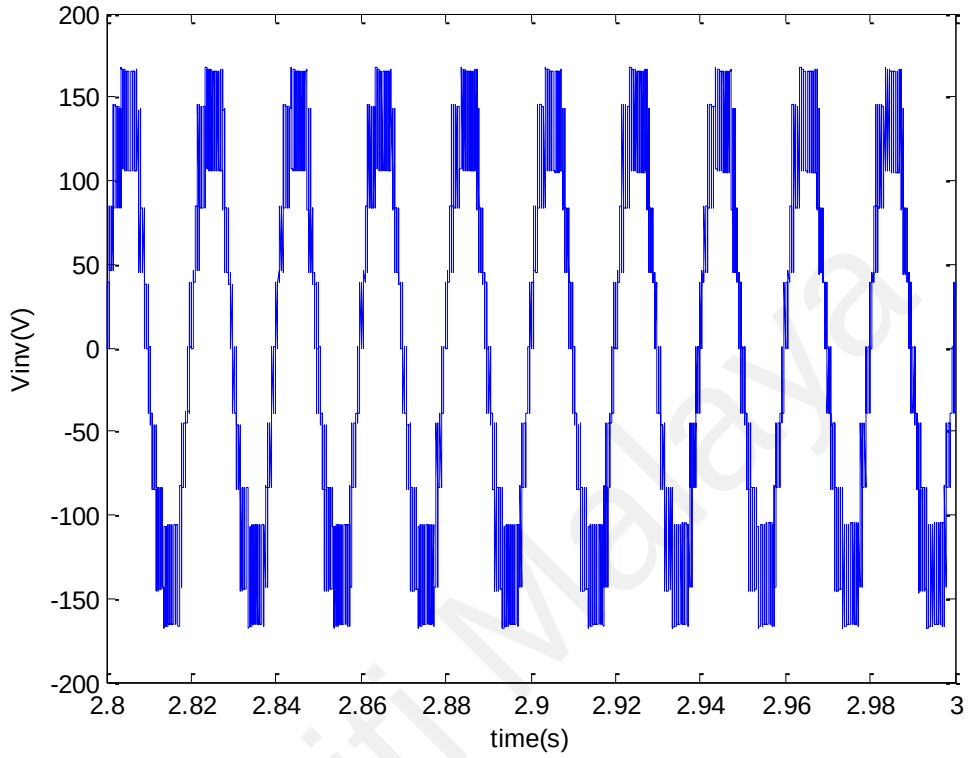


Figure 4.71: Zoomin view of the Inverter Output Voltage

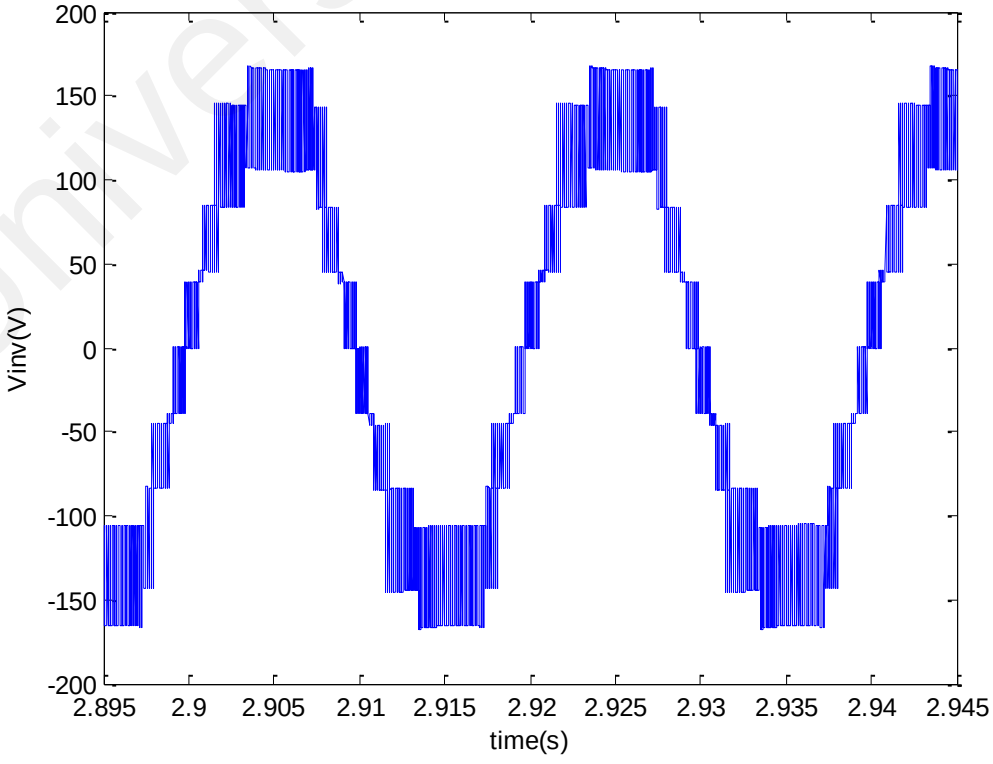


Figure 4.72: Simulation results of Vinv in correspondence with experimental results

$$V_R = IR \quad (in\ phase\ with\ I) \qquad V_l = IX_l \quad \left(leading\ I\ by\ \frac{\pi}{2}\right)$$

$$V_c = IX_c \quad \left(lagging\ I\ by\ \frac{\pi}{2}\right)$$

$$V = \sqrt{(V_r)^2 + (V_l - V_c)^2} \quad V = \sqrt{(IR)^2 + (IX_l - IX_c)^2} \quad Z$$

$$= \sqrt{(R)^2 + (X_l - X_c)^2}$$

$$V = I\sqrt{(R)^2 + (X_l - X_c)^2} = IZ$$

$$\tan\varphi = \frac{V_l - V_c}{V_r}$$

$$\varphi = \tan^{-1}\left(\frac{V_l - V_c}{V_r}\right) = \tan^{-1}\left(\frac{IX_l - IX_c}{IR}\right) = \tan^{-1}\left(\frac{X}{R}\right)$$

$$\text{Power factor} \quad \cos\varphi = \frac{R}{Z} = \frac{R}{\sqrt{(R)^2 + (X_l - X_c)^2}}$$

$$P = VI\cos\varphi$$

Figure 4.73 presents the capacitor voltage levels for all the DC Link capacitors involved in the PiCHB design for the balanced case. In case the RLC passive balancing circuit is utilized, the Balanced Voltage Sharing at the DC Link is attained and a balanced output voltage is obtained at the output as presented in Figure 4.74. Owing to its balanced state, the balanced voltage can optimize the entire performance of the PV system. Figure

4.75 presents the zoomin view of the balanced output voltage and Figure 4.76 presents the simulation result in correspondence with the experimental results.

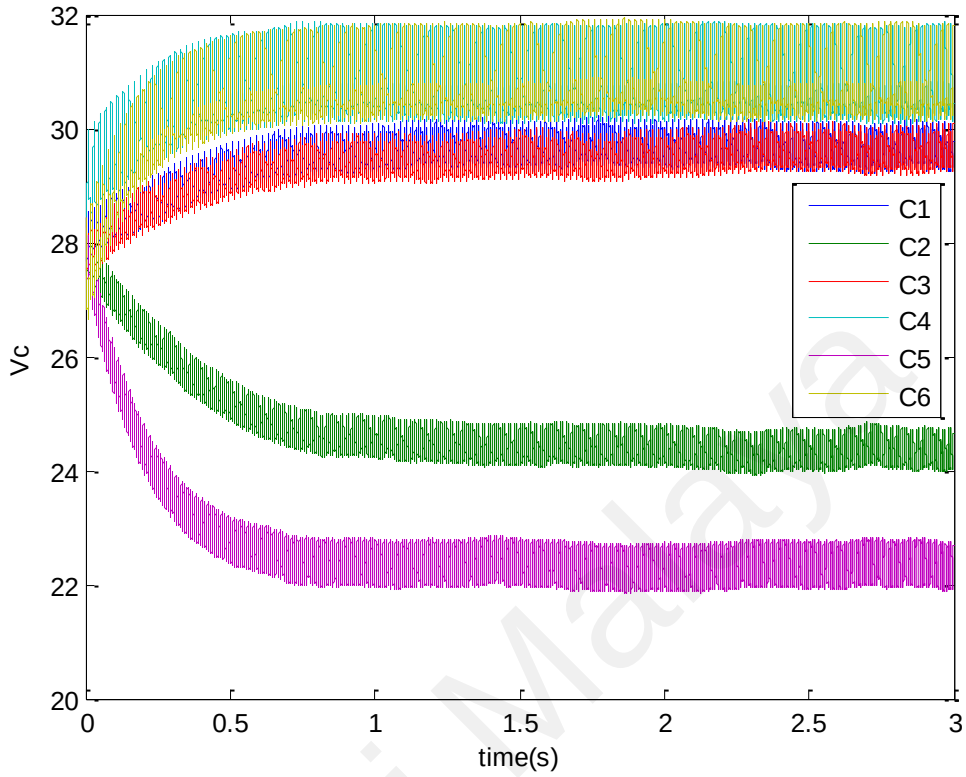


Figure 4.73: Capacitor voltage levels in balanced case

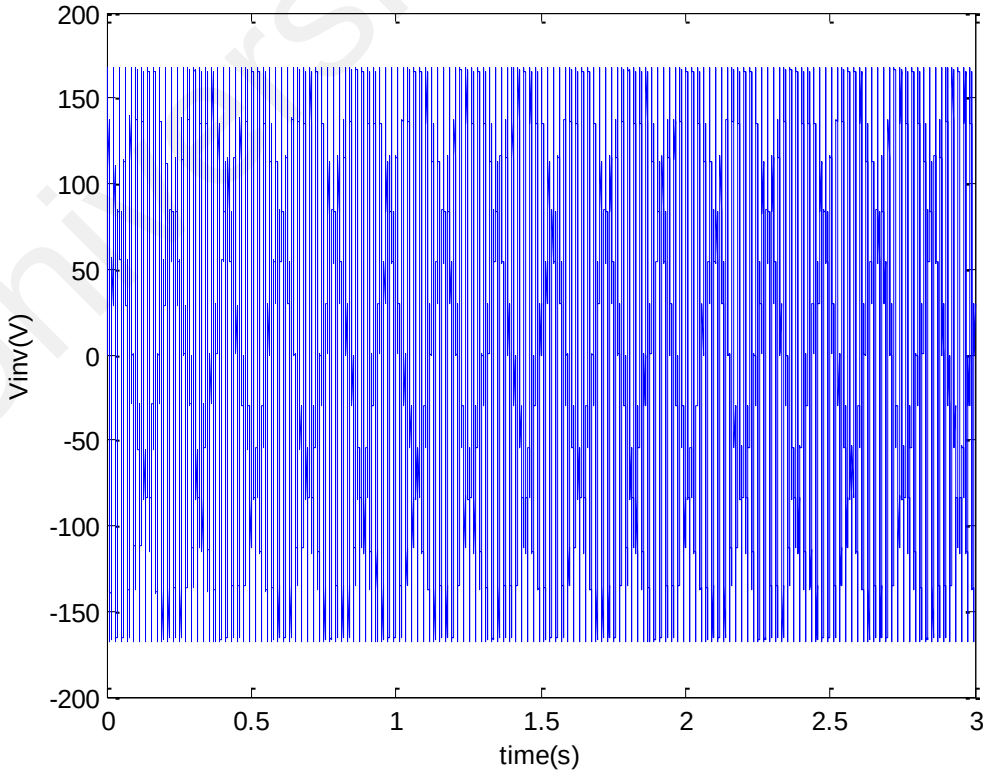


Figure 4.74: Inverter Output Voltage in balanced case

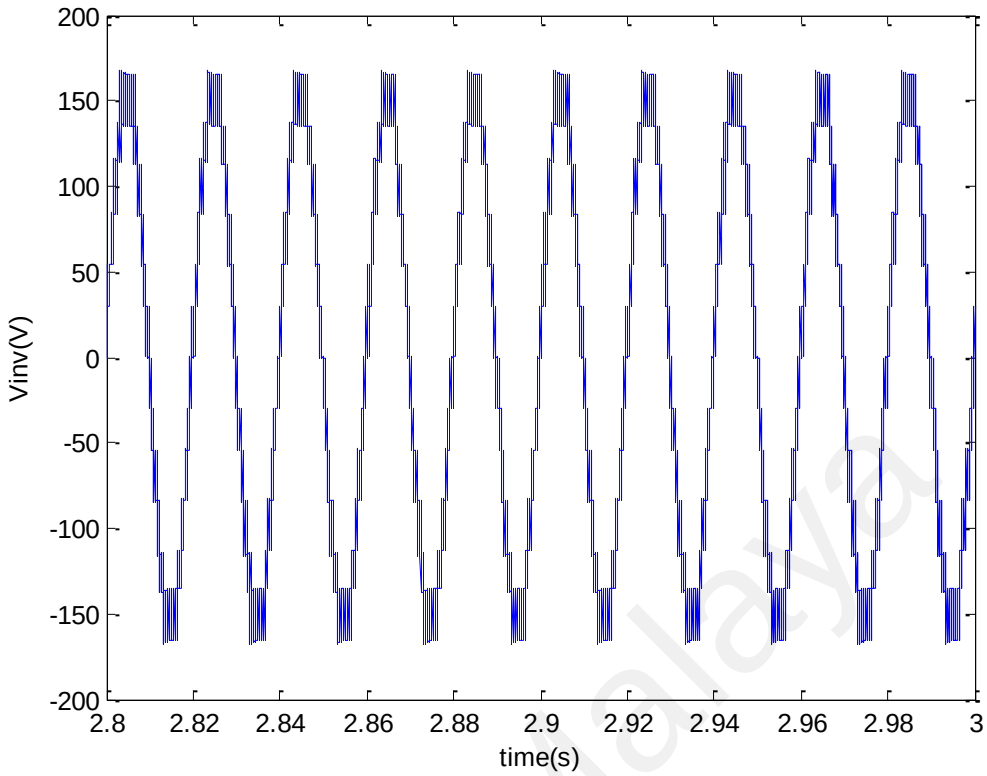


Figure 4.75: Zoomin view of the Inverter Output Voltage in balanced case

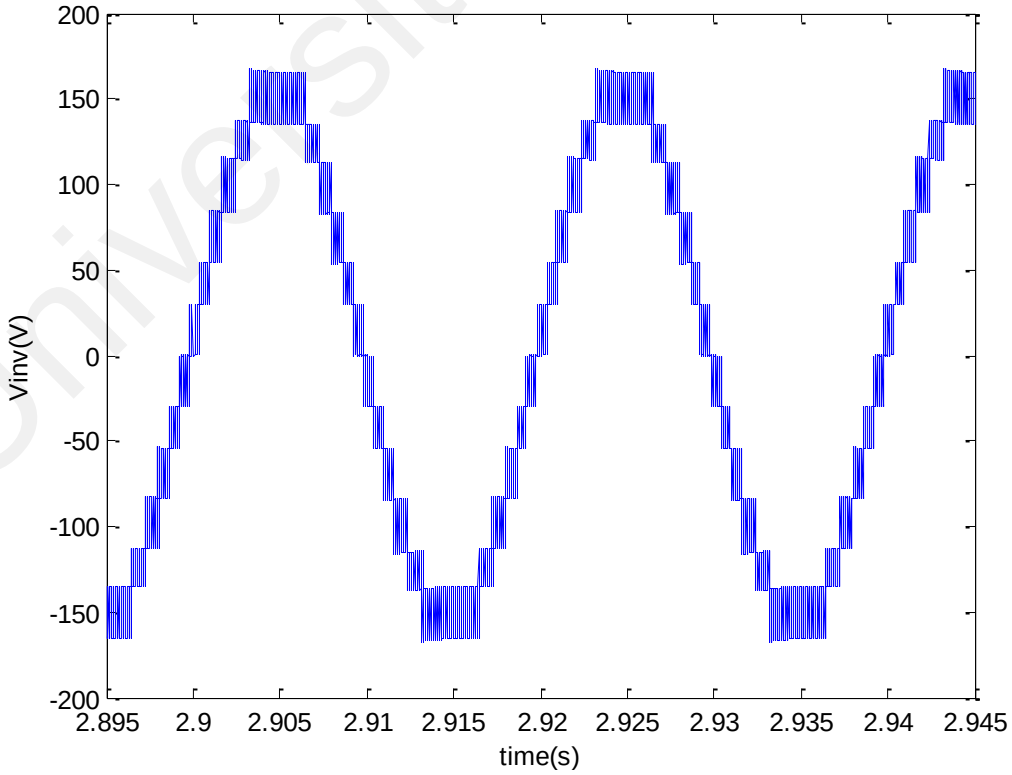


Figure 4.76: Simulation results of Vinv in correspondence with experimental results

Figure 4.77 presents the FFT analysis for the PiCHB in the unbalanced state without the passive circuit and Figure 4.78 the FFT analysis for the balanced case employing the passive RLC branch.

Table 4.9: System Parameters for PiCHB

Parameter	Value
Switching Frequency	20kHz
Sampling Frequency	78kHz
Resonant Frequency	20kHz
$C_{1,2,3,4,5,6}$	2200µF
C_t	225nF
$L_{1,2}$	3mH
L_t	280µH
L_f	5mH
R_t	2.2Ω
K_P	10
K_i	0.1

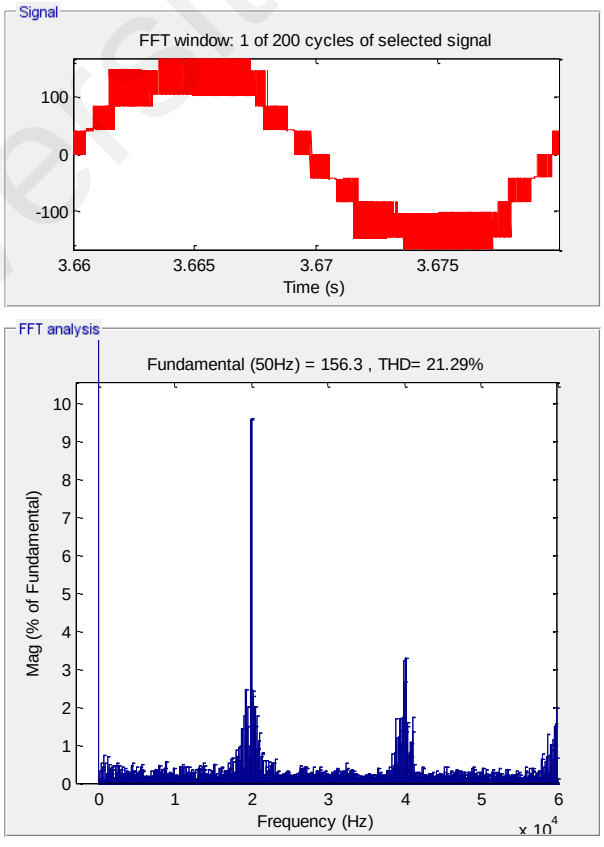


Figure 4.77: FFT for Unbalanced Output-Voltage

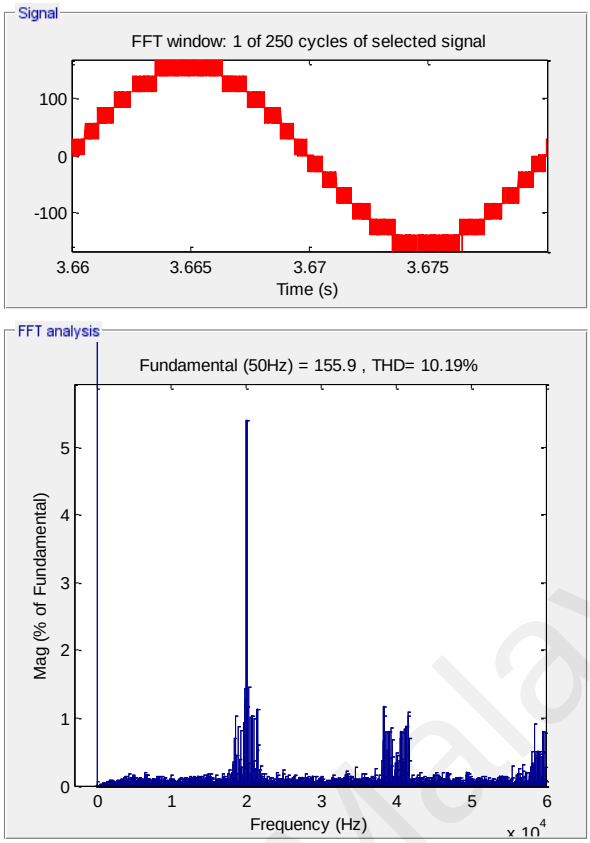


Figure 4.78: FFT for Balanced Output-Voltage

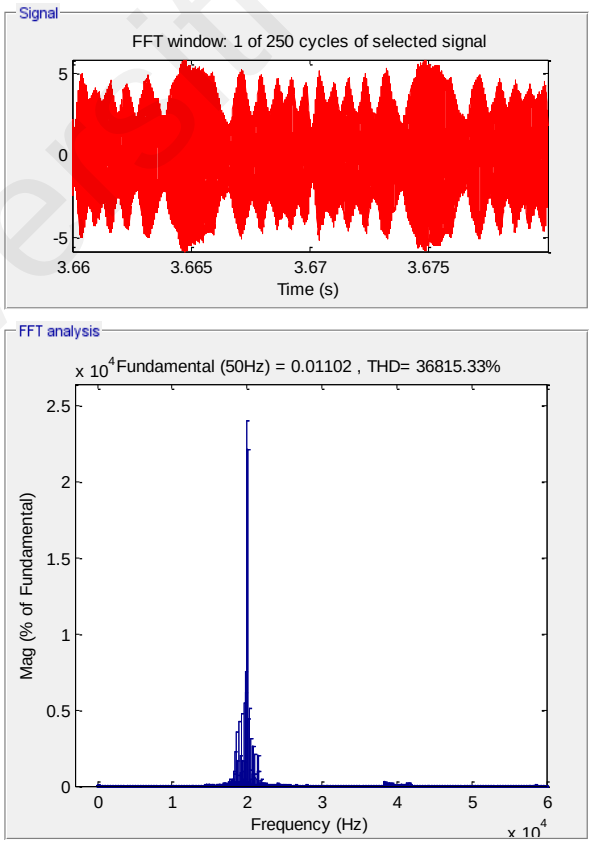


Figure 4.79: FFT for Balancing Current

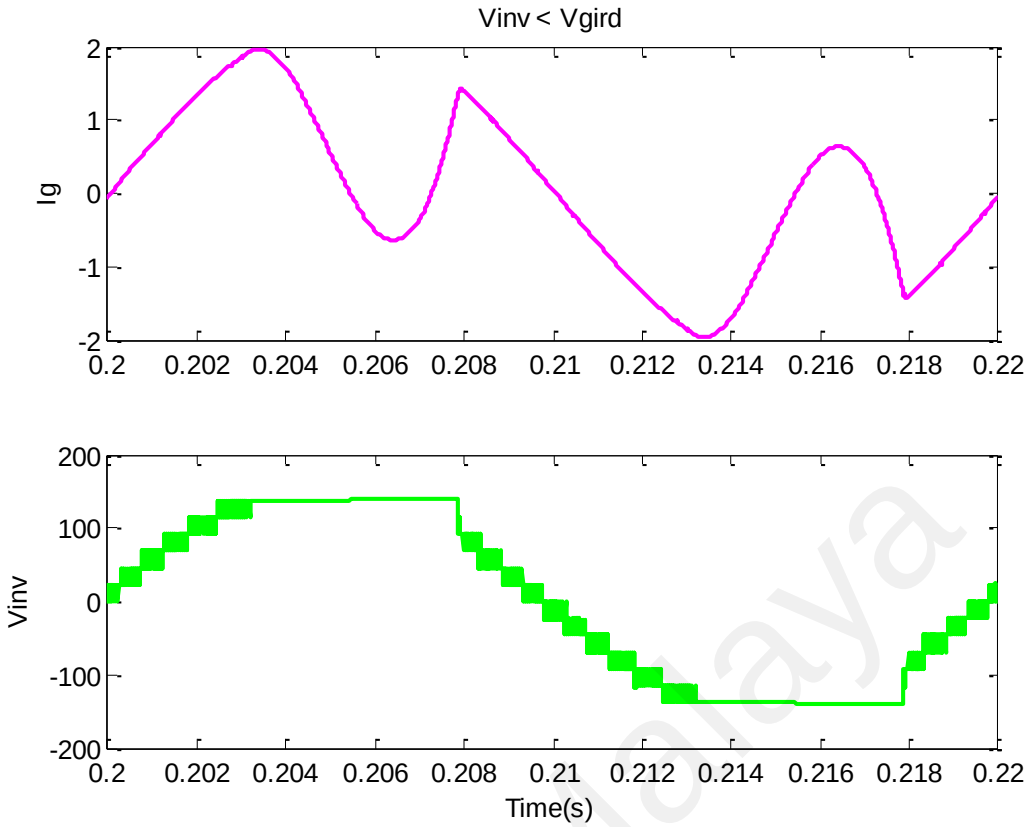


Figure 4.80: Output-Current and Voltage when $\boldsymbol{V_{inv} < V_g}$ for PiCHB

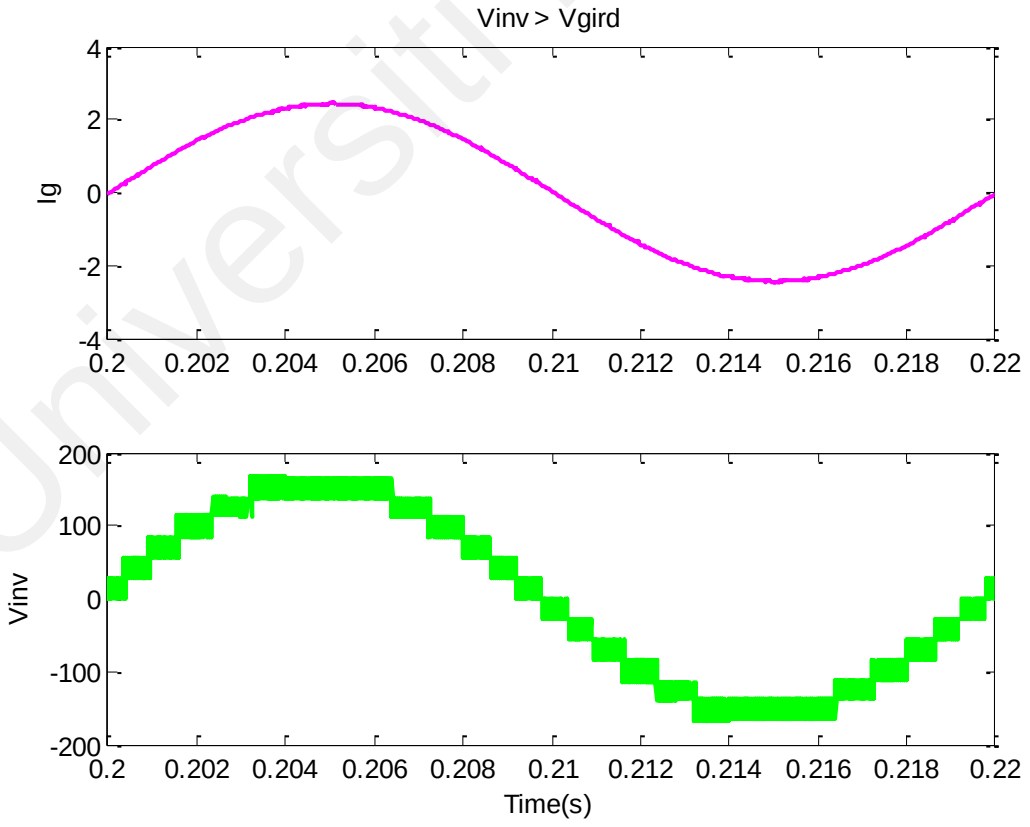


Figure 4.81: Output-Current and Voltage when $\boldsymbol{V_{inv} > V_g}$ for PiCHB

As observed the component frequency at the switching frequency for the unbalanced state remains higher which results into the DC-link capacitor voltage imbalance. Figure 4.79 displays the FFT of the balancing circuit current required to compensate the component frequency of the output voltage in the unbalanced case. Figure 4.80 displays the case where the $V_{inv} < V_{grid}$, where the current is injected from the grid to the inverter. When the V_{inv} is made higher than V_{grid} for the case $V_{inv} > V_{grid}$ the current is injected into the grid and the V_{grid} and I_{grid} are completely in-phase as presented in Figure 4.81.

Therefore, the system operation endorsed for the thirteen-level PiCHB is to be maintained with $M_a > 0.83$ && < 1. Where all the reference signals are in intersection against the carrier signal. Figure 4.82 shows the time response of the PiCHB inverter's output voltage before filter, inverter's output voltage after filter, grid voltage and pre-transformer output current for MPPT mode with a linear transformer 1:1 ratio.

As observed, the PiCHB MLI takes almost 0.3 seconds to attain a state where current and voltage are in phase. From 0 seconds to 0.1 seconds the MPPT tracks the optimum voltage to offer a voltage greater than the grid voltage. From 0.1 seconds to 0.3 seconds a stable steady state is attained where the current and voltage are brought in-phase with nearly unity power factor. In addition, Figure 4.83 shows the time response of the inverter when disconnected from the grid. Figure 4.84 is the zoomed version for the time response of the inverter when disconnected from the grid.

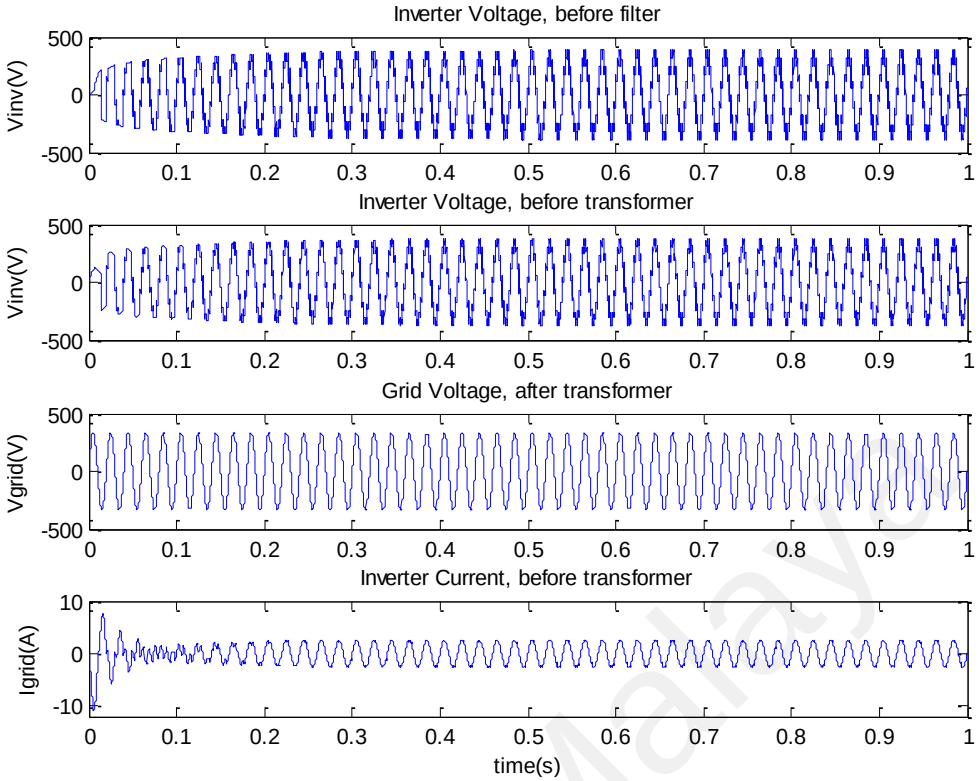


Figure 4.82: Time response of the PiCHB inverter with MPPT mode

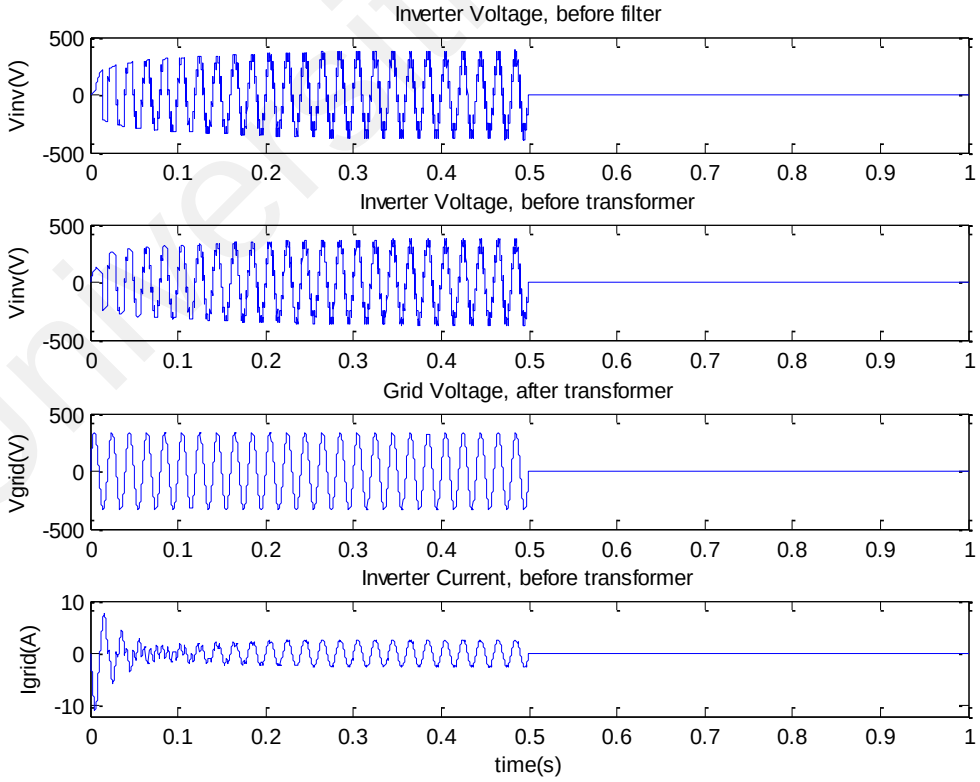


Figure 4.83: Time response PiCHB with MPPT mode when grid is disconnected

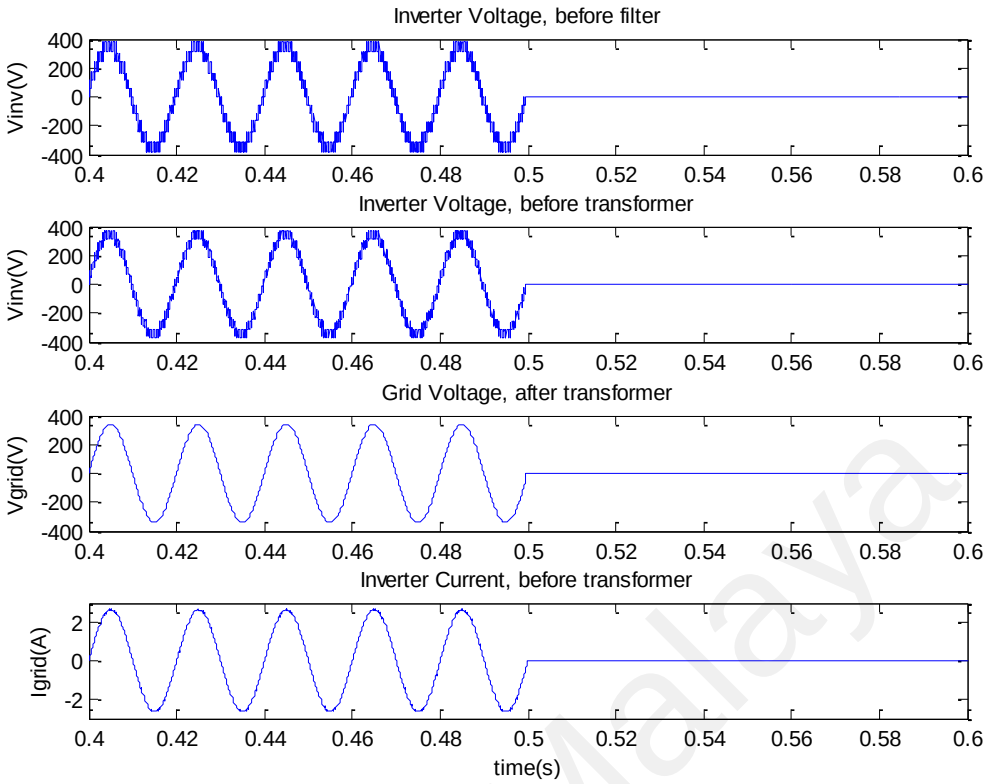


Figure 4.84: Zoomed view for time response when grid is disconnected

4.6 Summary

This chapter dealt with simulations of the proposed multilevel inverter in low-frequency switching, PWM switching and the proposed inverter's application in PV systems. Two PWM techniques were introduced to generate the switching signals. These signals are employed to produce nine and thirteen output-voltage levels. For TCHB, the PWM technique utilized one carrier and eight reference signals.

Modulation signals were complete sinewaves identical in shape and size except for an offset, whose value equaled the carrier-signal amplitude. For PiCHB, the PWM technique utilized one carrier and twelve reference signals. Similarly, complete sinewaves (modulation signals) identical in shape and size except for an offset were compared with the carrier.

The proposed MLI were applied to a PV system. The controlling algorithms were for MPPT based on mINC, current-controller based on PI technique, and islanding protection based on a passive technique. This chapter also presented the modeling characteristics of the PV module. The Current-Voltage (I-V) curves and the Power-Voltage (P-V) curves for various irradiances were simulated and their relationship to the modules' performance sought. The PV-module model used the stated PWM switching schemes for the inverter in grid-connected PV system.

CHAPTER 5: EXPERIMENTAL RESULTS

5.1 Introduction

This section describes implementation of the hardware prototype for testing of the proposed inverter and validation of the simulation results. The hardware platform was a TMS320F28335 DSP that drove a lab-prototype multilevel inverter aided by Texas Instrument's Code Composer Studio™ (CCStudio 3.1) and an ALTERA Cyclone II FPGA to implement the logic circuitry aided by the Quartus II 13.0sp1. The system used high switching frequencies and was implemented with both stand-alone and grid-tied PV applications.

5.2 Implementing for PWM Switching Frequency

5.2.1 Hardware Configuration

Measurements were made on a Fluke-437 SERIES-II power quality and energy analyzer and Tektronix TDS 2024B. In addition, Chroma 62000H Solar Array Simulator was utilized to simulate the SIEMENS SP-75 module PV operational parameters. The hardware prototype has been shown in Figure 5.1. In addition, enlarged images of all the sections in the hardware prototype have been displayed in the appendix section.

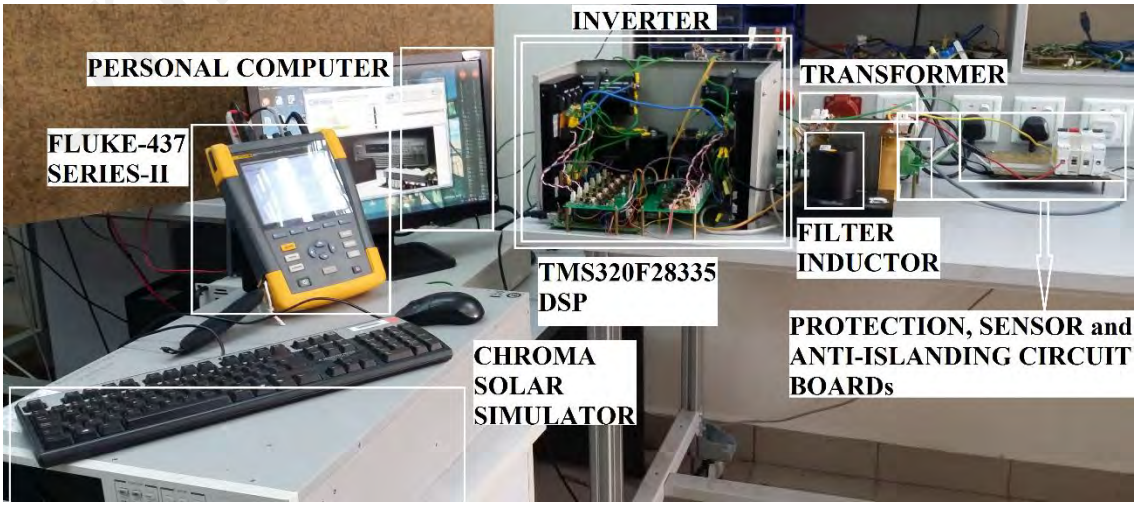


Figure 5.1: Hardware Prototype

A Texas Instrument TMS320F28335 DSP and the ALTERA cyclone II FPGA generated the IGBT switching signals. The DSP and the FPGA board have nearly all the peripheral signals available on their headers, so interfacing them with the other system hardware was easy.

Switches S1-S8 for nine-level inverter, S1-B12 for thirteen-level and SB1-SB2 for the boost converter were IRG4PC40UDPBF IGBTs. 30CPF12 were the diodes for the boost converters. C1-C4 for nine-level and C1-C6 for thirteen-level were 2200 uF/400V electrolyte capacitors.

The F28335 board allows power conditioning system control via existing (no extra circuit needed) on-board setting of the PWM. Another advantage is its built-in ADC, which allows digitizing of the feedback signals from the sensors and storing of the signals for further processing. The hardware for this experiment with high switching frequency involved a load R=250Ω, but with an additional 5mH inductor.

5.2.2 TCHB Inverter

The PWM switching frequency was 20 kHz, which was fed to the gate-drive circuit, switching the IGBT on and off. Modulation index M_a was applied to see its effect on THD. The proposed TCHB multilevel inverter topology generated a nine-level output voltage when M_a was above 0.75 but below 1.0. M_a was set to be 0.87.

Figure 5.2 gives the switching patterns of S1, S2, S3 and S4 whereas Figure 5.3 the switching patterns of S5, S6, S7 and S8. The switching frequencies of S1, S3, S5 and S7 were high whereas of S2 and S4 was 50 Hz and opposing.

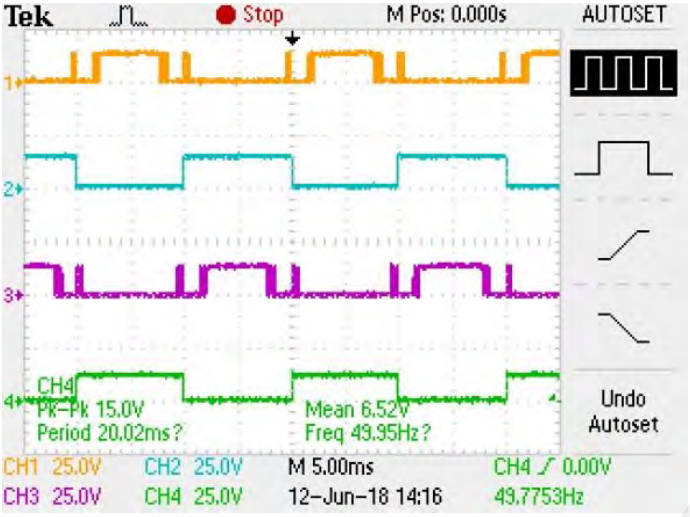


Figure 5.2: Switching Signals for 1) S1, 2) S2, 3) S3 and 4) S4

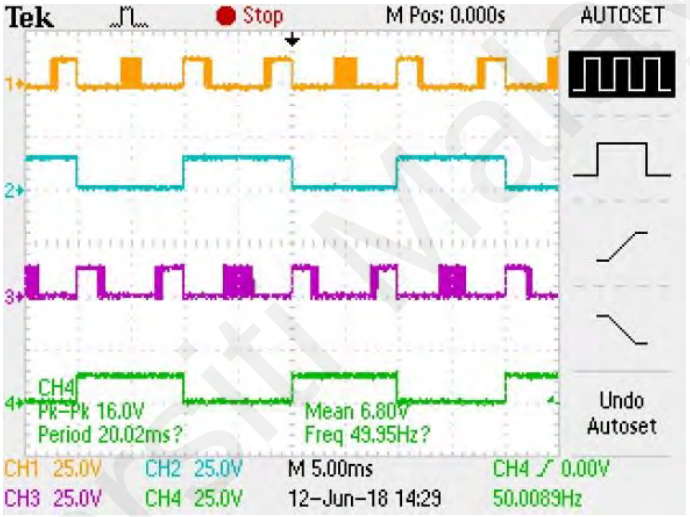
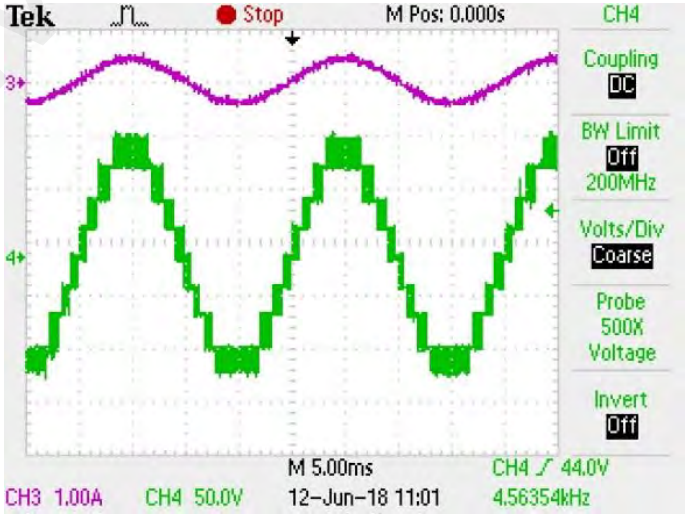
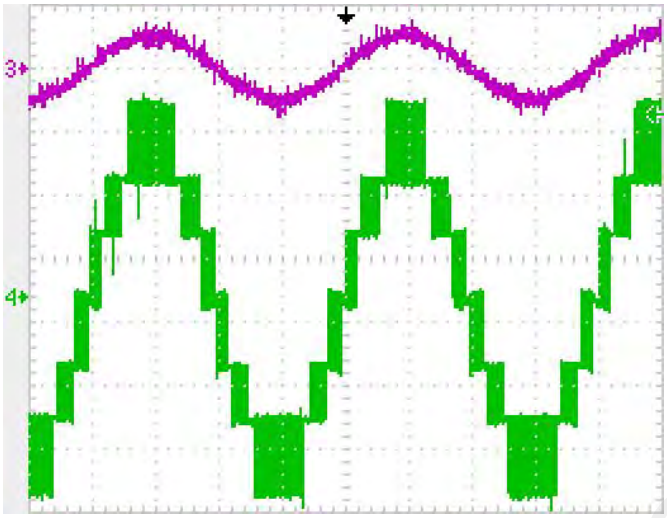


Figure 5.3: Switching Signals for 1) S5, 2) S6, 3) S7 and 4) S8

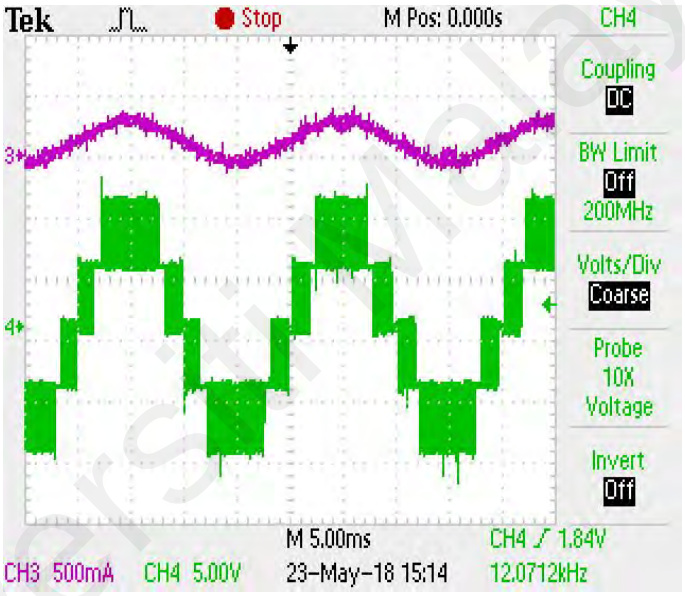


(a)

Figure 5.4: Nine-Level Output (a) when $\boldsymbol{M_a = 0.87}$ was above 0.75 but below 1.0 (b) $\boldsymbol{M_a}$ was above 0.5 but below 0.75 and (c) $\boldsymbol{M_a}$ was above 0.25 but below 0.5



(b)



(c)

Figure 5.4, continued

Figure 5.4 shows the output voltage and output current of the proposed inverter, which generated a nine-level output voltage waveform at the output terminals, when the modulation index was above 0.75 but below 1.0, for the pre-filtered sinusoidal voltage and current at the load terminal.

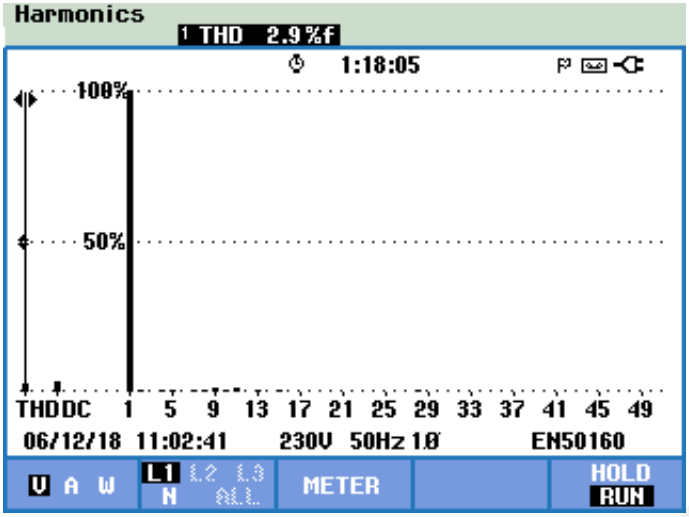


Figure 5.5: Output-Voltage THD

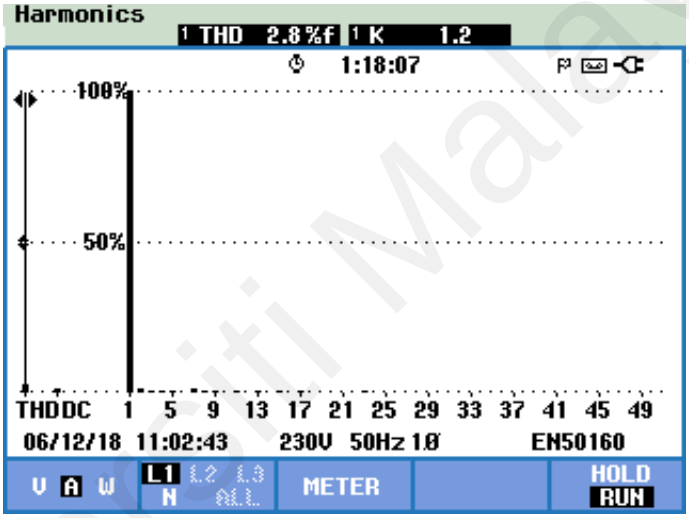


Figure 5.6: Output-Current THD

Figures 5.5 and 5.6 respectively show, for 0.75<M_a<1, the voltage THD (2.9%) and current THD (2.8%) of the TCHB MLI.

5.2.3 PiCHB Inverter

The proposed PiCHB MLI topology generated a thirteen-level output voltage when M_a was above 0.83 but below 1.0. Figure 5.7 gives the switching patterns of S1, S2, S3 and S4, with Figure 5.8 showing the corresponding standing-voltages.

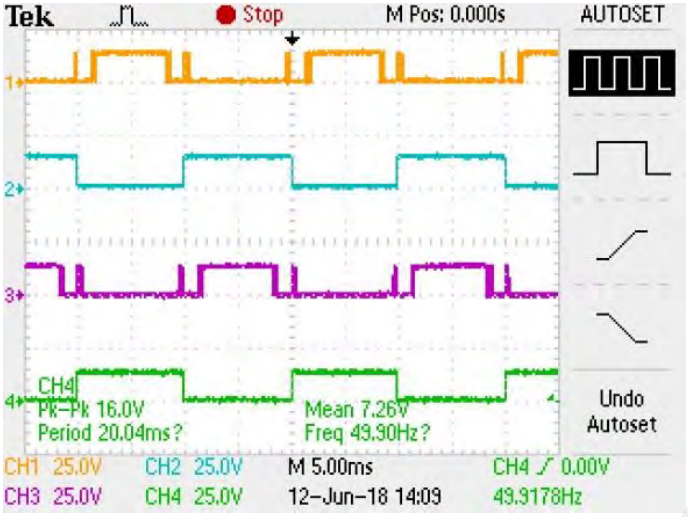


Figure 5.7: Switching signals for S1, S2, S3 and S4

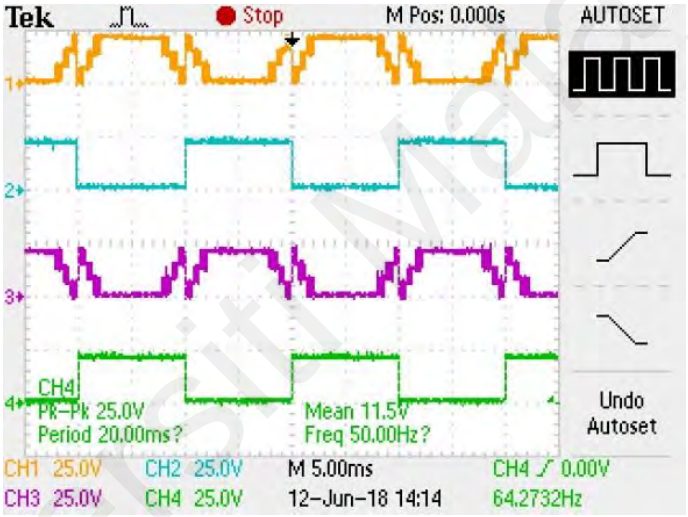


Figure 5.8: Corresponding Standing-Voltages for S1, S2, S3 and S4

In addition, Figure 5.9 the switching patterns of S7, S8, S9 and S10, along with Figure 5.10 showing corresponding standing-voltages and the switching patterns for B5, B6, B11 and B12 being displayed in Figure 5.11 and the standing-voltage in Figure 5.12. The switching frequencies of S1, S3, B5, B6, S7, S9, B11 and B12 were high whereas of S2 and S4 were 50Hz.

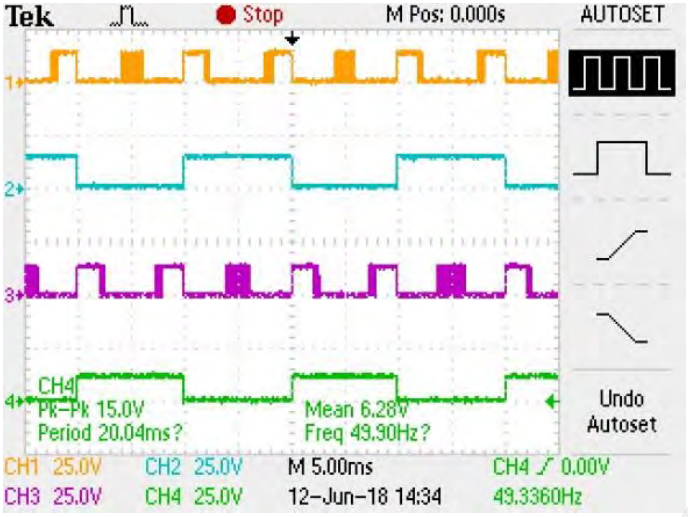


Figure 5.9: Switching signals for S7, S8, S9 and S10

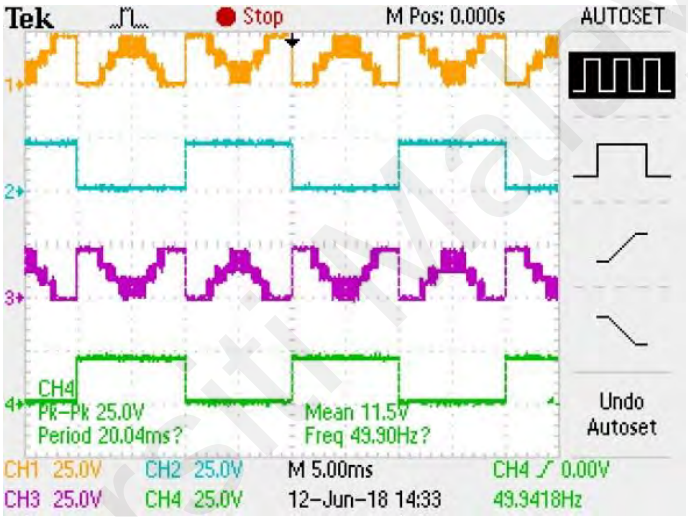


Figure 5.10: Corresponding Standing-Voltages for S7, S8, S9 and S10

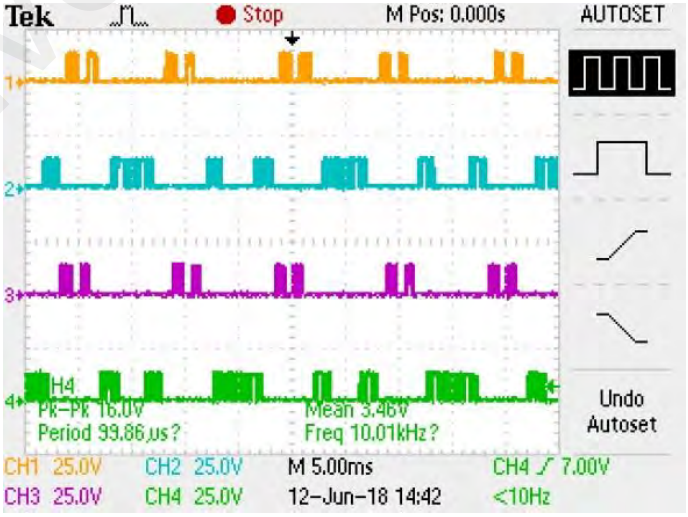


Figure 5.11: Switching signals for B5, B11, B6 and B12

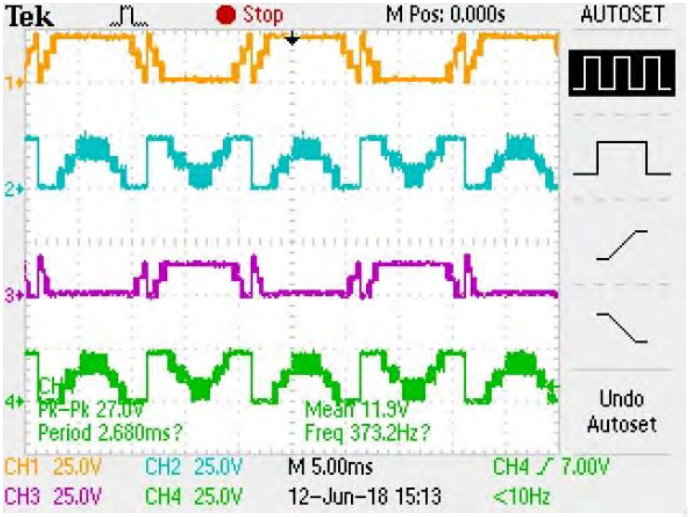


Figure 5.12: Corresponding Standing-Voltages for B5, B11, B6 and B12

Figure 5.13 shows the output voltage and output current of the proposed inverter, which generated a thirteen-level output voltage waveform at the output terminal, or, when the modulation index was above 0.83 but below 1.0, with pre-filtered sinusoidal voltage and current at the load terminal. Here, the M_a was set to be 0.93.

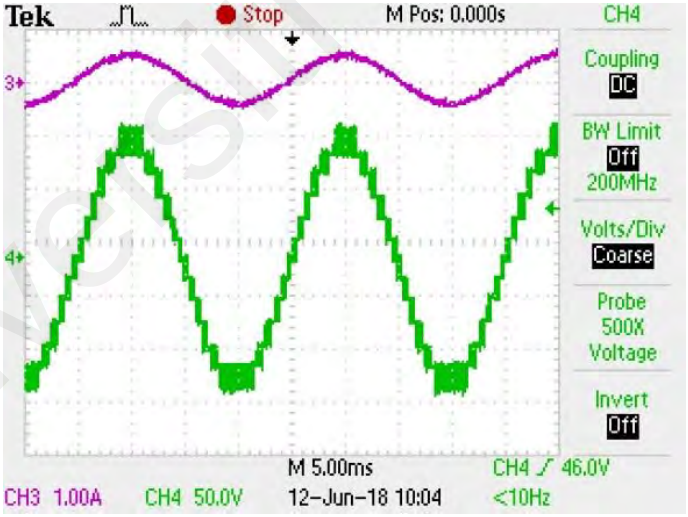


Figure 5.13: Output-Voltage and Current with $\boldsymbol{M_a = 0.93}$

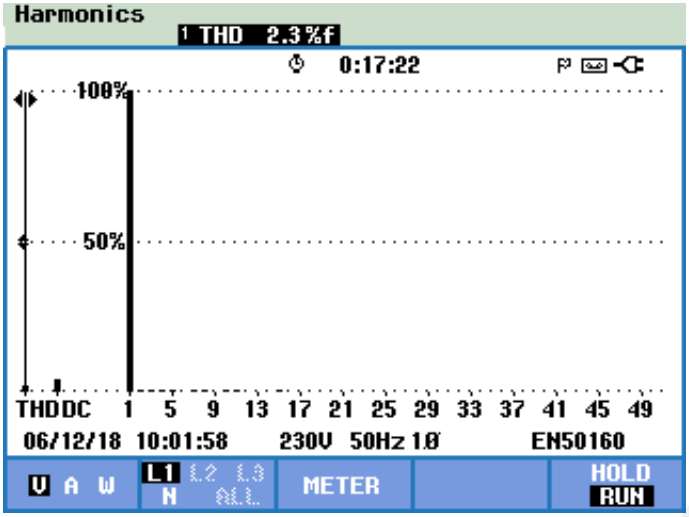


Figure 5.14: Output-Voltage THD being 2.3 %

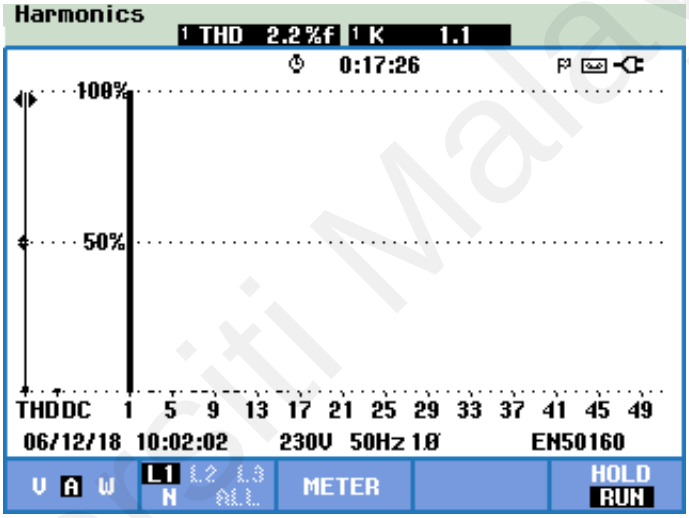


Figure 5.15: Output-Current THD being 2.2 %

Figures 5.14 and 5.15 respectively show, for 0.83<M_a<1, the voltage THD (2.3%) and current THD (2.2%) of the proposed multilevel inverter. The proposed PiCHB MLI topology generated an eleven-level output voltage when M_a was above 0.67 but below 0.83. Figure 5.16 gives the switching patterns of S1, S2, S3 and S4. In addition, Figure 5.17 the switching patterns of S7, S8, S9 and S10, and the switching patterns for B5, B6, B11 and B12 being displayed in Figure 5.18. The switching frequencies of S1, S3, B5, B6, S7, S9, B11 and B12 were high whereas of S2 and S4 were 50Hz.

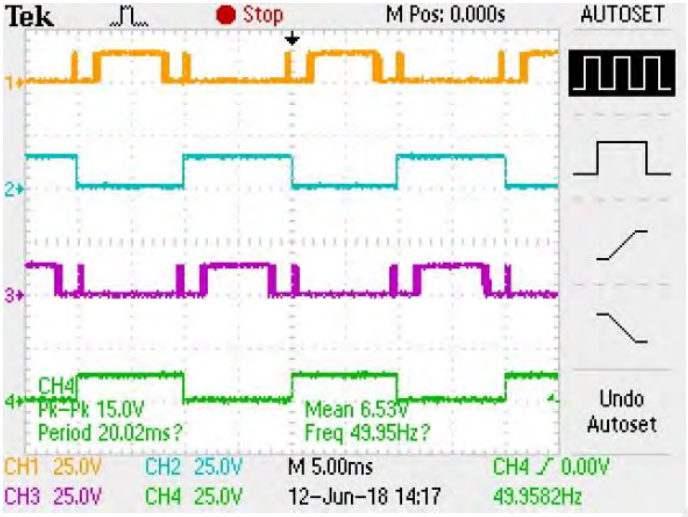


Figure 5.16: Switching signals for S1, S2, S3 and S4

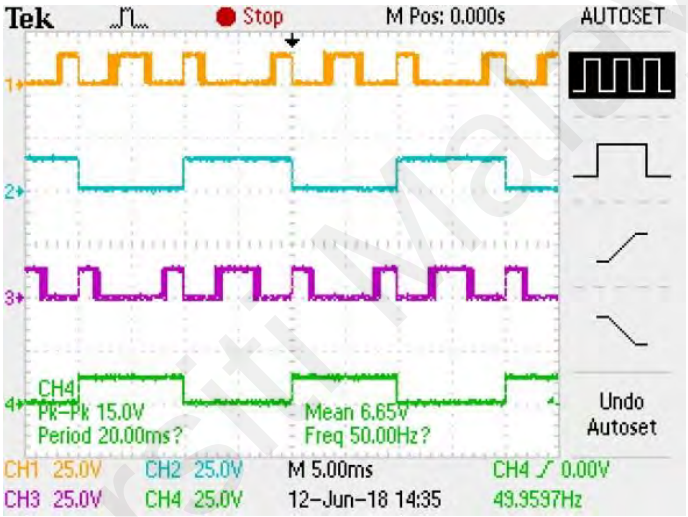


Figure 5.17: Switching signals for S7, S8, S9 and S10

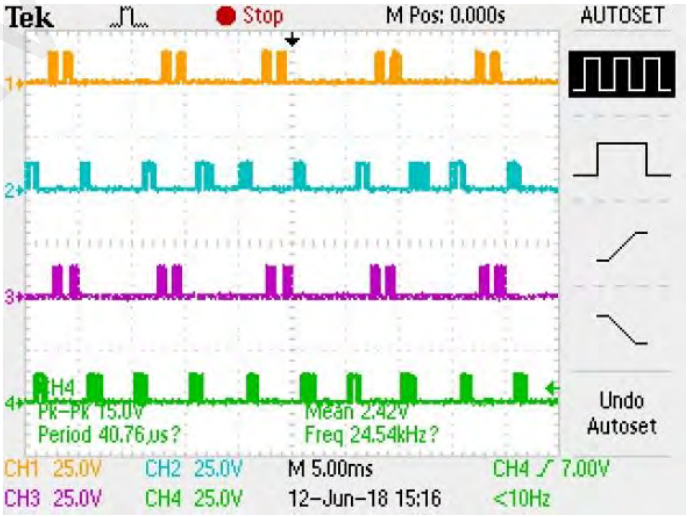


Figure 5.18: Switching signals for B5, B11, B6 and B12

Figure 5.19 shows the output voltage and output current of the proposed inverter, which generated a nine-level output voltage waveform at output terminal, or, when the modulation index was above 0.67 but below 0.83, with pre-filtered sinusoidal voltage and current at the load terminal. Here, M_a is set to be 0.75.

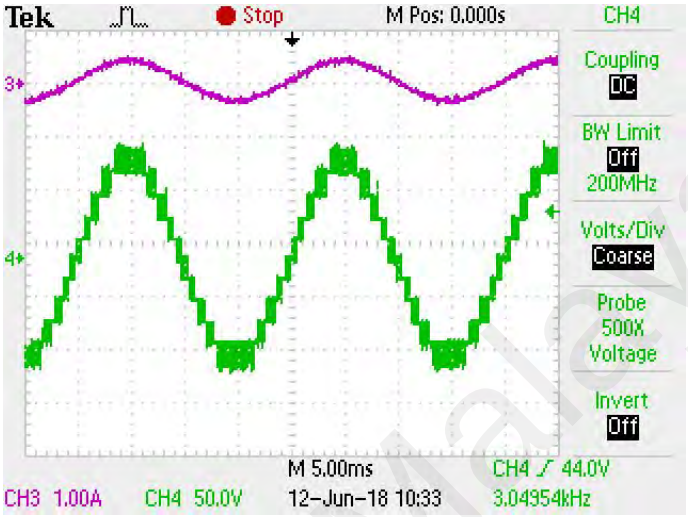


Figure 5.19: Output-Voltage and current for PiCHB with $\boldsymbol{M_a = 0.75}$ above 0.67 and below 0.83

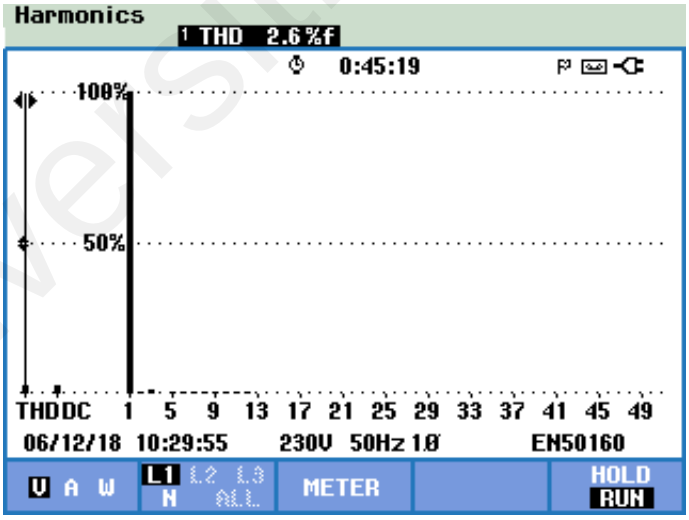


Figure 5.20: Output-Voltage THD being 2.6 %

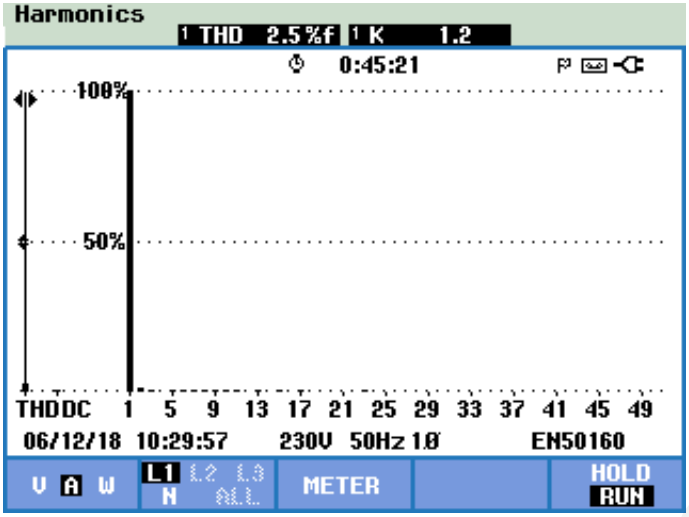


Figure 5.21: Output-Current THD being 2.5 %

Figures 5.20 and 5.21 respectively show, for 0.67<M_a<0.83, the voltage THD (2.6%) and current THD (2.5%) of the proposed MLI. The proposed PiCHB MLI topology generated a chopped output voltage when M_a exceeded 1. As the signals widened due to the increase in the modulation index.

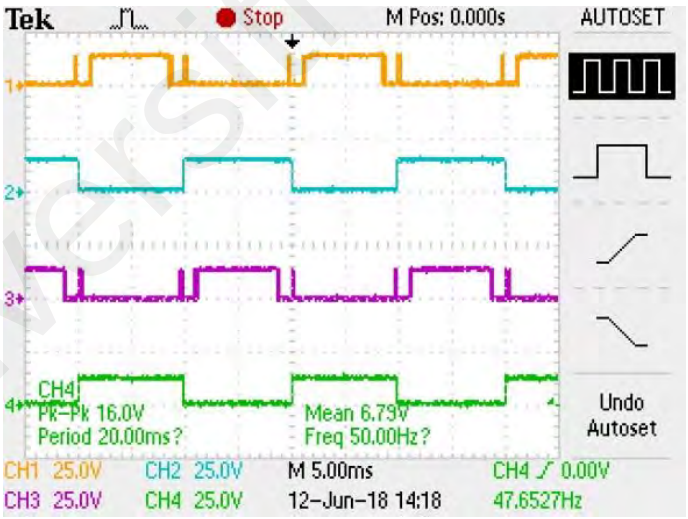


Figure 5.22: Switching signals for S1, S2, S3 and S4

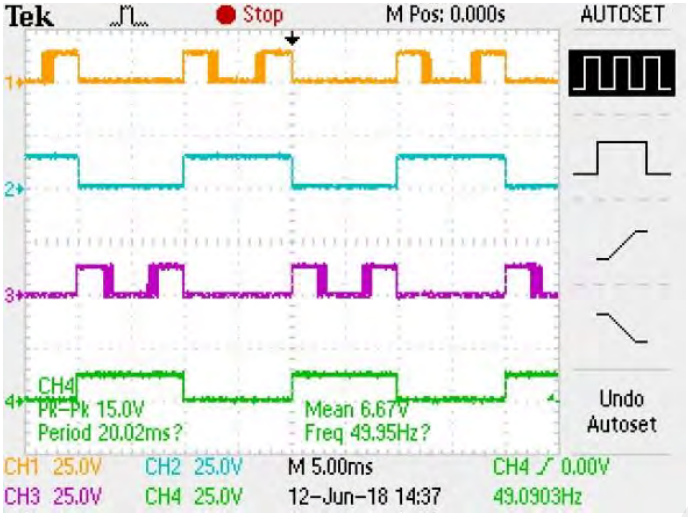


Figure 5.23: Switching signals for S7, S8, S9 and S10

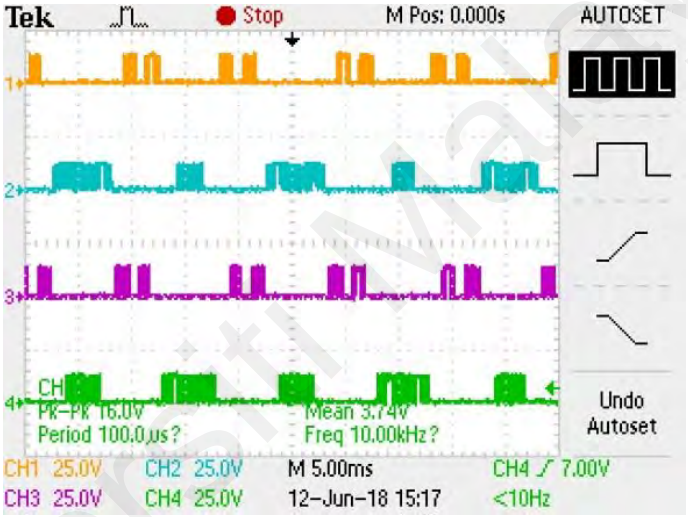


Figure 5.24: Switching signals for B5, B11, B6 and B12

Figure 5.22 gives the switching patterns of S1, S2, S3 and S4. In addition, Figure 5.23 the switching patterns of S7, S8, S9 and S10, and the switching patterns for B5, B6, B11 and B12 being displayed in Figure 5.24. The switching frequencies of S1, S3, B5, B6, S7, S9, B11 and B12 were high whereas of S2 and S4 were 50Hz.

Figure 5.25 shows the output voltage and output current of the proposed inverter, which generated a chopped output voltage. Here, M_a was set to be 1.17.

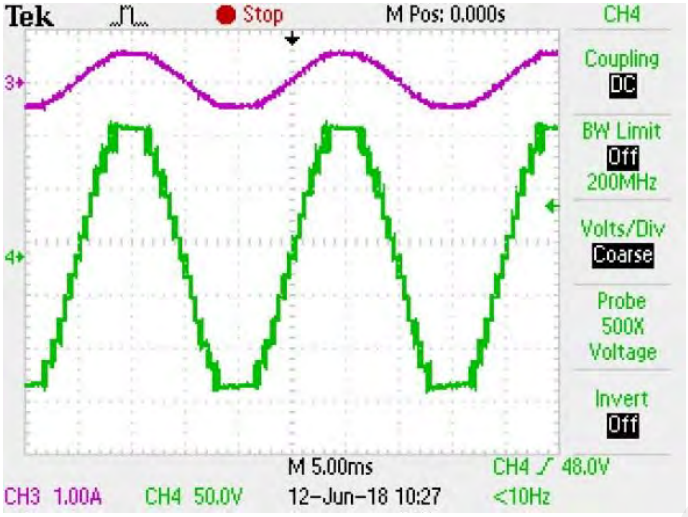
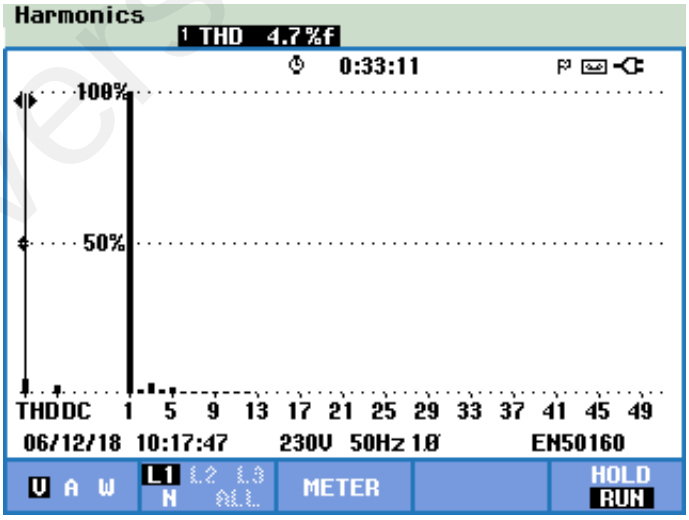


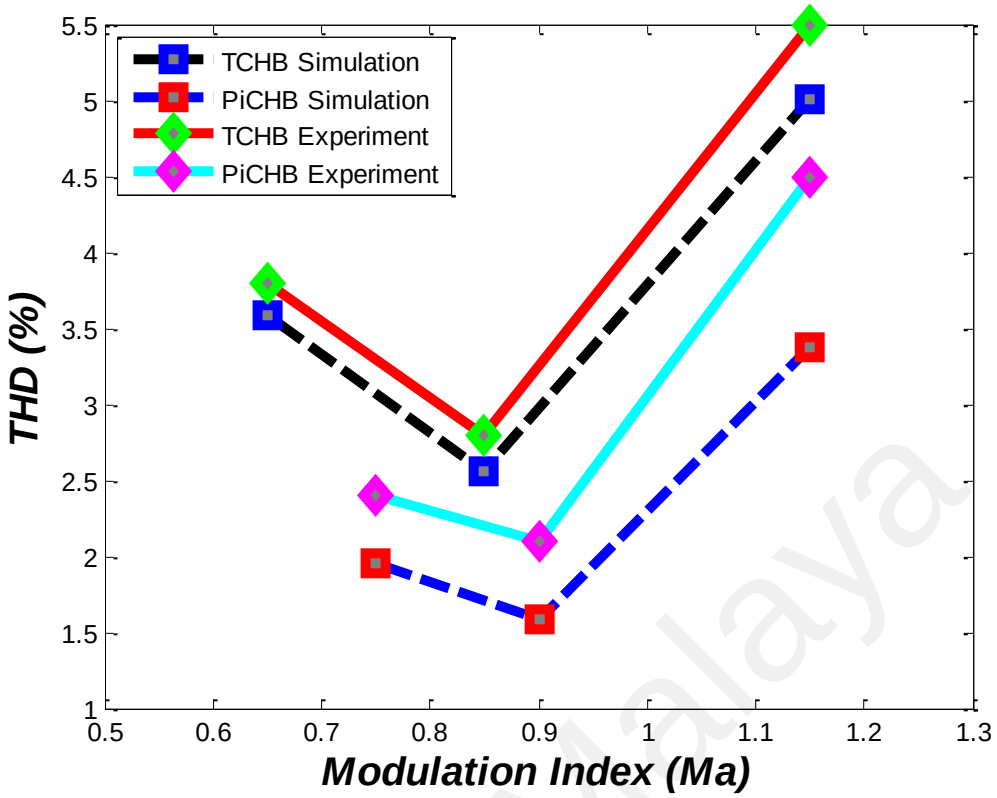
Figure 5.25: Output-Voltage and Current when $\boldsymbol{M_a = 1.17}$ exceeded 1

Figures 5.26(a) shows, for M_a>1, the voltage THD (4.7%) and Figure 5.27 the current THD (4.6%) of the proposed MLI. Figure 5.26(b) shows the comparison of simulation and experimental results for the THD (%) variation of TCHB and PiCHB inverter topologies for varing Modulation Index.



(a)

Figure 5.26: $\boldsymbol{M_a}$>1 (a) Output-Voltage THD (b) Output-Voltage THD (4.7%) comparison of simulation and experimental results



(b)

Figure 5.26, continued

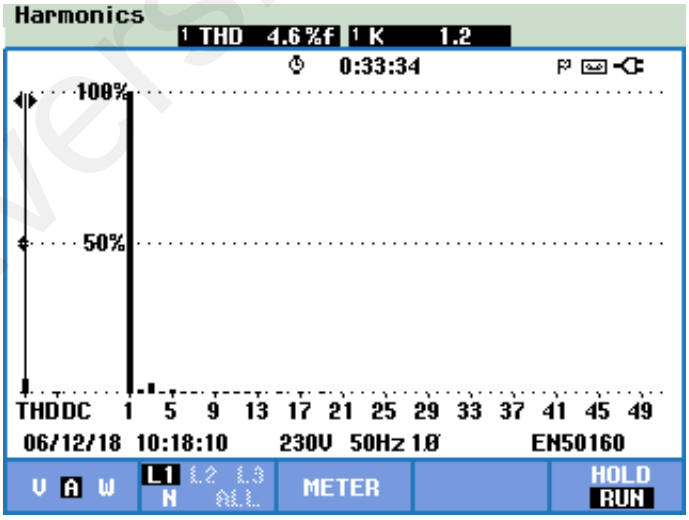


Figure 5.27: Output-Current THD being 4.6 %

5.3 Implementing the mINC MPPT on various DC-DC Converters

As explained and detail in the simulation section, the proposed mINC MPPT had been implemented in a PV system on various DC-DC converters. Here, the Modified Boost and Buck Converter had been utilized to validate the improved performance of the mINC

MPPT. For experimental results presented in Figures 5.28 and 5.29 the operational time is 50 seconds for Converter . Here the plot for probe 2 represents PV input current, probe 1 represents PV input voltage and Math function, M, represents power.

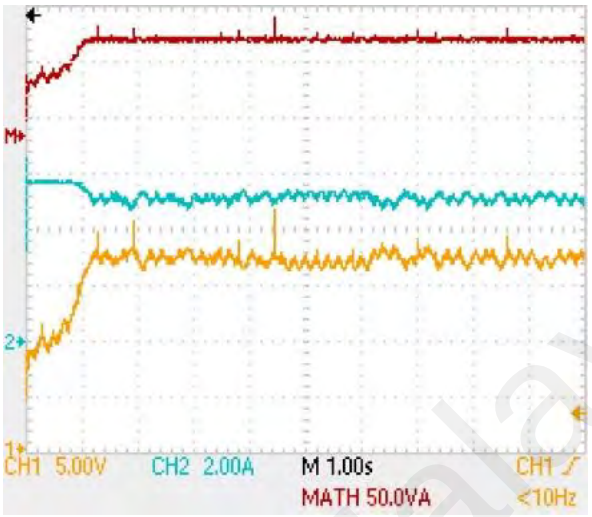


Figure 5.28: Experimental Results for mINC on Modified Boost Converter

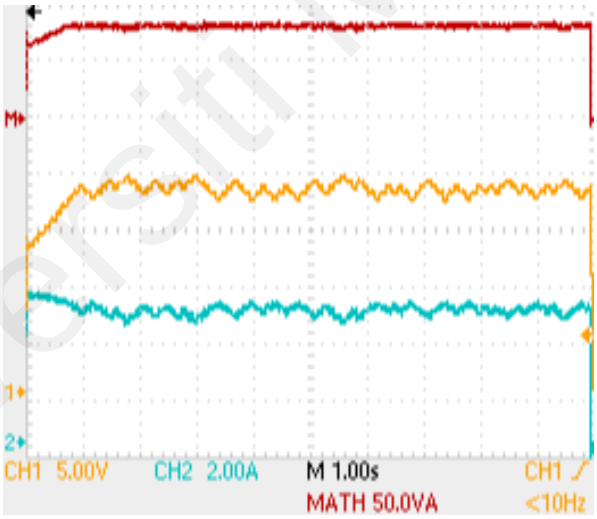


Figure 5.29: Experimental Results for mINC on Modified Buck Converter

where Figure 5.28 displays the experimental results for mINC on the Modified Boost Converter and Figure 5.29 displays the experimental results for mINC on the Modified Buck Converter. All the results have been attained under STC. PV voltage has been displayed by channel 1, current with channel 2 and power with Math function of the mentioned mINC MPPT method. As observed, during the steady state operation the

mINC oscillates around the MPP, yet it remains easy to implement reduces the complexity of the PV system control.

5.4 Implementing the Grid-Tied PV Application

5.4.1 Hardware Configuration

Chroma 62000H (Programmable Photovoltaic Array Simulator) replaced the DC power supply to simulate the PV module parameters of SIEMENS SP75. The load was the utility grid. A DC-DC boost converter was also present with each cascade. The proposed inverters were housed in a box and had circuits for DC/AC current, and voltage sensors, and protection relays. A TMS320F28335 DSP along with an ALTERA FPGA Cyclone II was utilized to validate the simulation outcomes. The intersection of eight and twelve reference signals with one carrier, permissible in the DSP, obtained the switching signals for the TCHB and the PiCHB inverter, respectively.

The complete hardware setup of the proposed multilevel inverter for PV application consists of PV array, two-stage power conditioning system, low frequency 1kVA transformer 1:2, utility grid, current sensor circuit, voltage sensor circuit, gate drive circuits, zero-crossing detector, relay, FPGA and DSP board were utilized. Here, accessories circuit namely voltage, DC and AC current sensor circuit, zero crossing detector and relay as protection circuit were utilized. All the control signals were processed in the TMS320F28335 board. The output signal from the sensor circuit was fed to the ADC pins.

Ten serial SIEMENS SP75 modules produced 750W peak power. For each cascade, PV arrays of 375 W were employed as inputs. To produce 375 W of P_{MPP} for each cascade, five modules of SIEMENS SP75 were connected in series.

Figure 5.30 presents the PV module parameters for one SIEMENS SP75 module simulated in CHROMA 62150H-1000S. In addition, to replicate real weather conditions the reference irradiance was kept at 300 W/m^2 for five PV panels under consideration to be connected in series. Further, Figure 5.31 presents the operational mINC MPPT efficiency for one cascade in the PV system.

In each cascade five PV panels had been connected in series. As observed, the mINC takes 7 seconds to reach the steady state from the transient state. Yet, during the steady state the mINC MPPT oscillates around the MPP. Such an oscillation slightly reduces the MPPT efficiency. The merits of the mINC MPPT include, easy implementation, reduced complexity and PV array independence. However, oscillations around the MPP remain the demerit of the mINC MPPT.

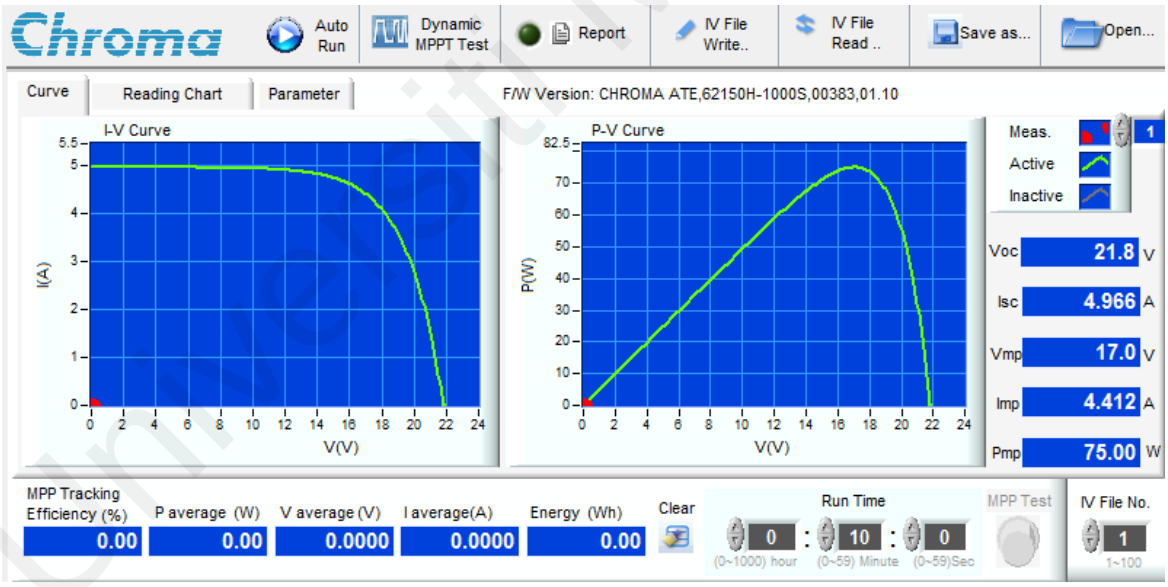


Figure 5.30: PV module parameters for one SIEMENS SP75 module

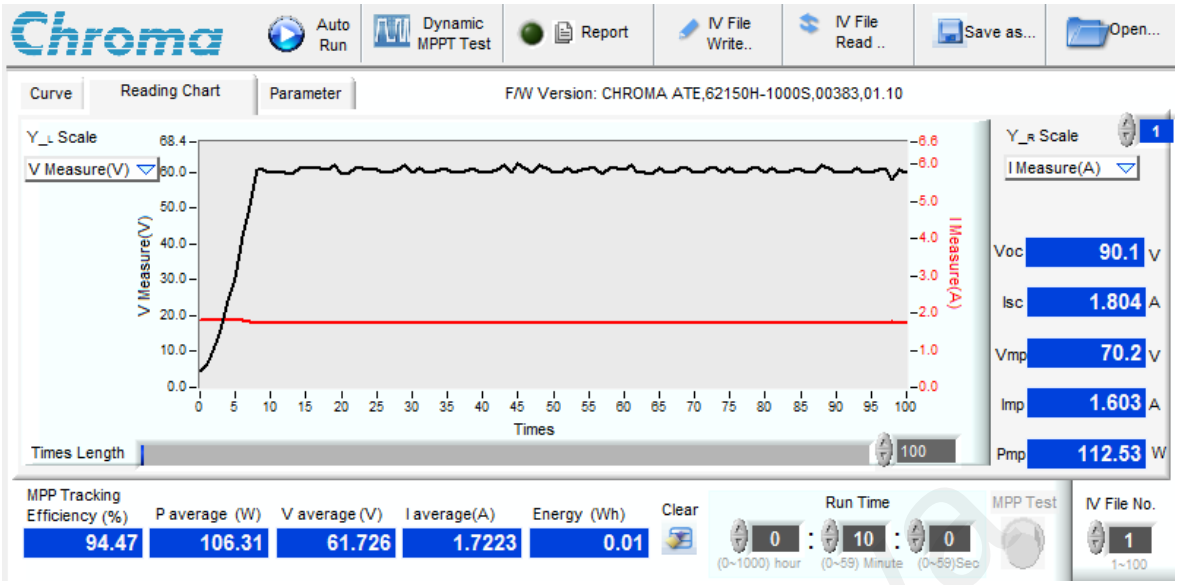


Figure 5.31: mINC MPPT efficiency for one cascade in the PV system at 300 W/m^2 irradiance

5.4.2 TCHB Inverter

Figure 5.32 gives the experiment results for the TCHB inverter's output-voltage Vinv, and the output current Iinv. The grid voltage had been stepped down to half the actual voltage through a 1:2 ratio transformer, so Vgrid was 120V. As discussed, to inject current into the grid, Vinv > $\sqrt{2}$ * Vgird, so Vinv was set to 300V. As expected, Vinv comprises Nine-levels of output voltage for TCHB and Thirteen-levels for PiCHB.

The dc-bus voltage was set greater than $\sqrt{2}\ of\ V_{grid}$ and I_{grid} had been filtered by a filter inductor L_f to resemble a nearly sinewave. V_{inv} consists of nine-levels of output-voltage as, $M_a > 0.75\ \&\&\ < 1$ was chosen for current injection into the gird. On one hand, in the case where $V_{inv} < V_{grid}$, the grid injects current into the inverter, the I_{grid} and V_{inv} for this case have been displayed in Figure 5.32. On the other hand, for the case where $V_{inv} > V_{grid}$ grid-current and output-voltage are in phase. This condition with nearly-unity power factor is sufficient for current injection into the grid. The I_{grid} and V_{inv} for this case have been displayed in Figure 5.33. The corresponding output-voltage

waveform THD and Current THD have been displayed in Figures 5.34 and 5.35, respectively. Here, the PWM technique utilized offers self-capacitor voltage balancing.

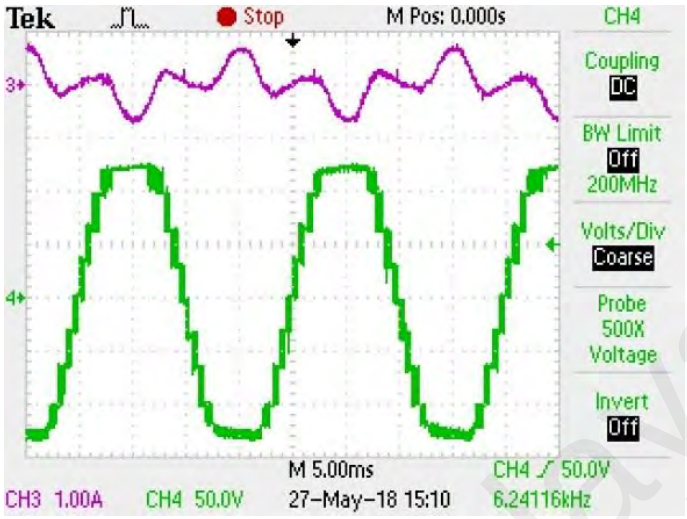


Figure 5.32: Output-Voltage and Current for $\boldsymbol{V_{inv} < V_g}$

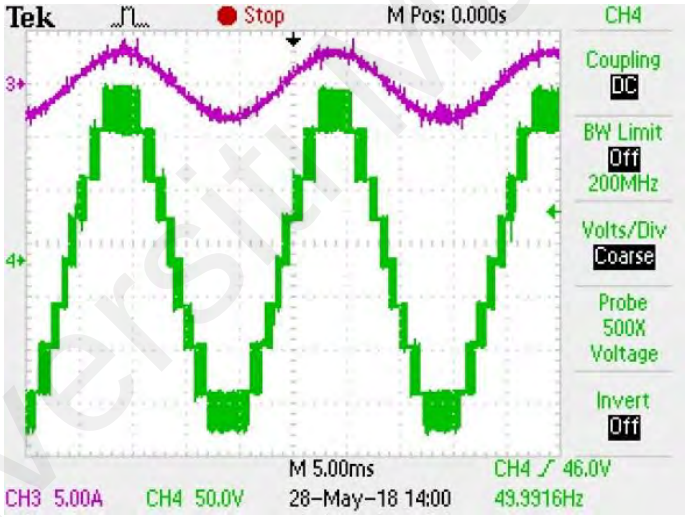


Figure 5.33: Output-Voltage and Current for $\boldsymbol{V_{inv} > V_g}$

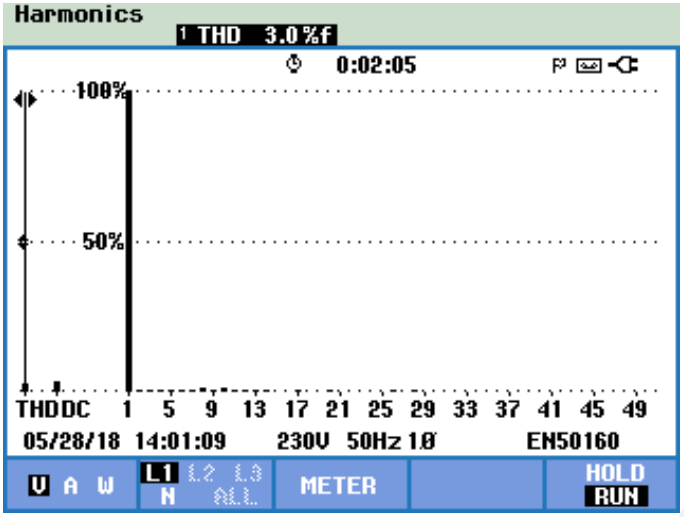


Figure 5.34: Output-Voltage THD being 3.0 %

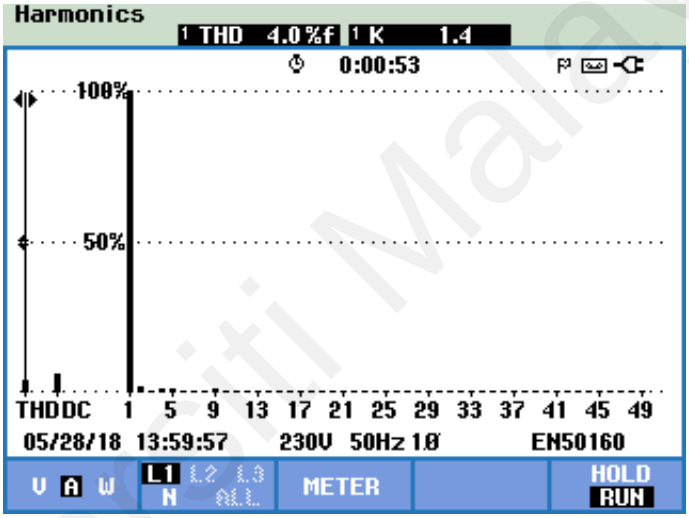


Figure 5.35: Output-Current THD being 4.0 %

5.4.3 PiCHB Inverter

Similarly for PiCHB, the dc-bus voltage was set greater than $\sqrt{2}\ of\ V_{grid}$ and I_{grid} had been filtered by a filter inductor L_f to resemble a nearly sinewave. V_{inv} consists of thirteen-levels of output-voltage as, $M_a > 0.83$ && $M_a < 1$ was chosen for current injection into the gird. On one hand, for the case where $V_{inv} > V_{grid}$ grid-current and output-voltage are in phase. This condition with nearly-unity power factor is sufficient for current injection into the grid.

However, the current remains distorted in the unbalance condition, as presented in Figure 5.36 and the corresponding FFT of the output-voltage for the unbalanced condition

has been offered in Figure 5.37. The corresponding current THD for unbalanced output-voltage has been shown in 5.38.

By employing the balancing circuit, the BVS condition is attained, where I_{grid} and V_{inv} are in phase with a better harmonic profile as displayed in Figure 5.39, and the corresponding output-voltage FFT in Figure 5.40. The balancing circuit current and its FFT have been displayed in Figure 5.41 and Figure 5.42, respectively. In the case where $V_{inv} < V_{grid}$, the grid injects current into the inverter, the I_{grid} and V_{inv} for this case have been displayed in Figure 5.43.

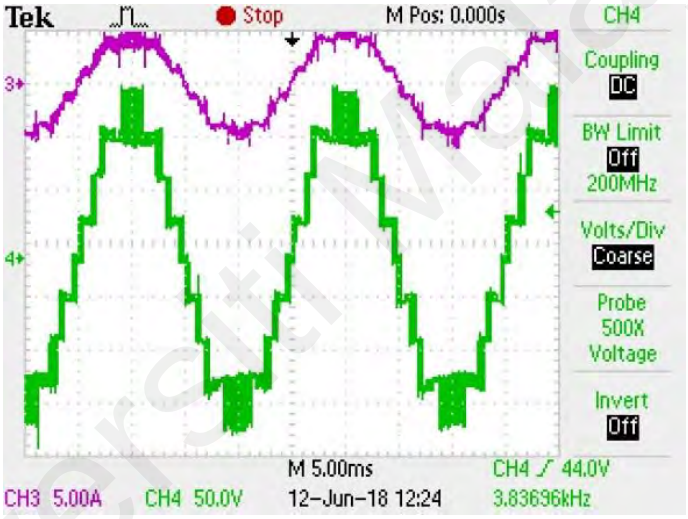


Figure 5.36: Thirteen-level Unbalance

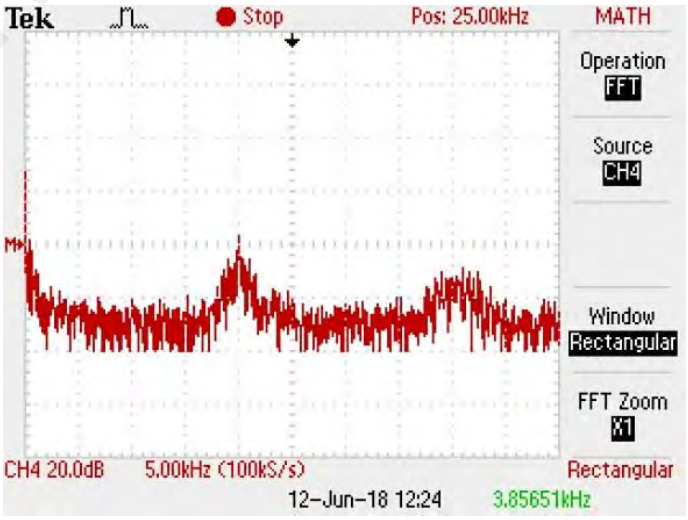


Figure 5.37: FFT of Output-Voltage for Unbalance condition

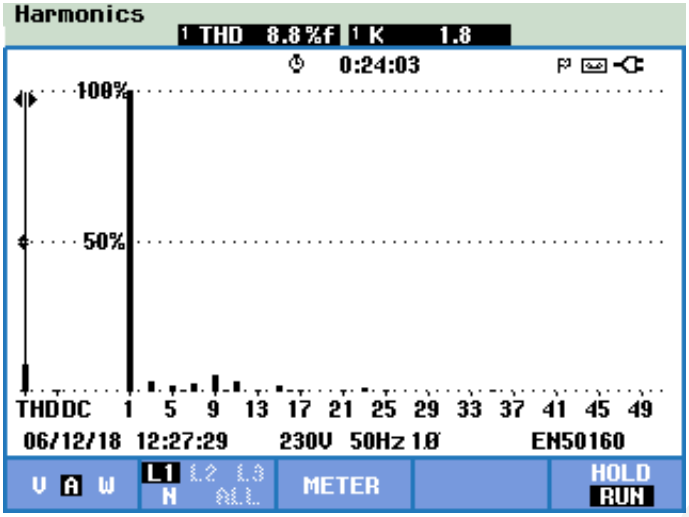


Figure 5.38: Output-Current THD being 8.8 %

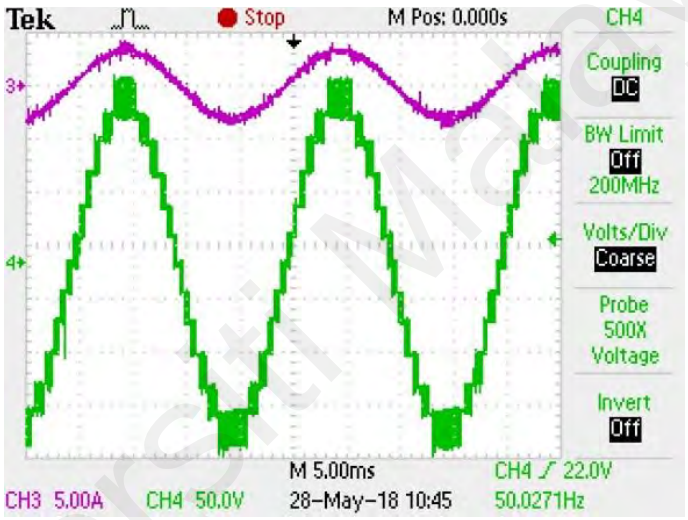


Figure 5.39: Thirteen-level Balanced

Figure 5.40: FFT of Output-Voltage for Balanced condition

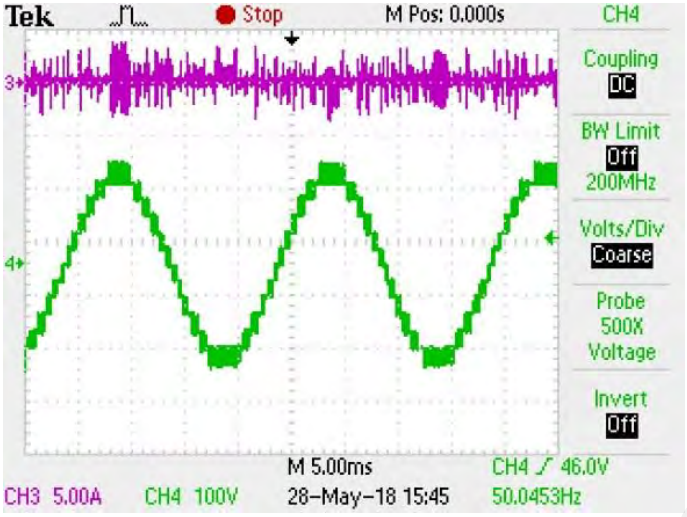


Figure 5.41: Thirteen-level Balancing Current

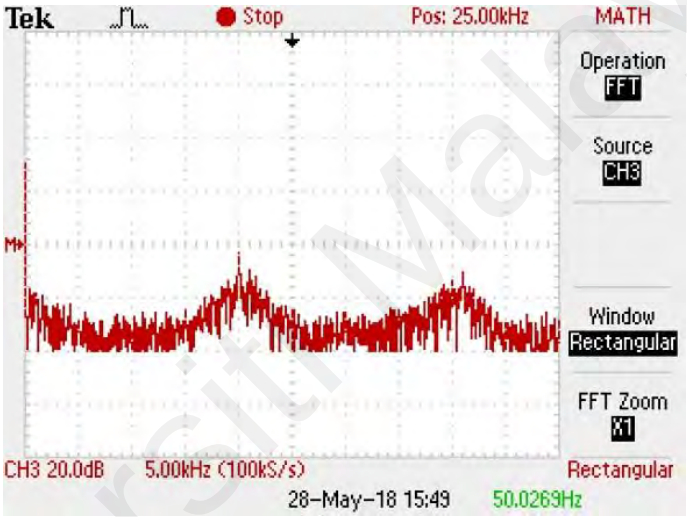


Figure 5.42: FFT of Balancing Current

The addition of a passive RLC branch compensates the imbalance, but offers a demerit as it increases the cost of the system due to the addition of passive circuit elements. The Voltage and Current THD for the balanced condition have been shown in Figures 5.44 and 5.45, respectively. Therefore, the proposed TCHB and PiCHB MLI are utilized to attain a higher number of output-voltage levels N_{level}, with lesser semiconductor devices, reduced dv/dt stress, better voltage and current THD waveforms, reduced EMI and size of passive filters.

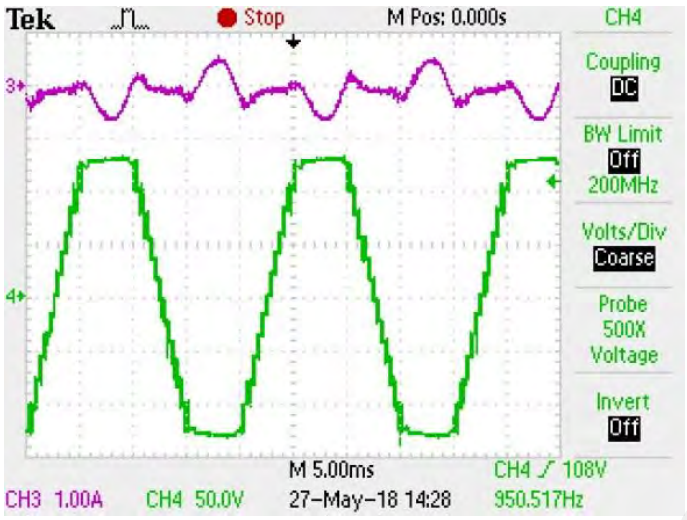


Figure 5.43: Output-Voltage and Current when $\boldsymbol{V_{inv} < V_g}$

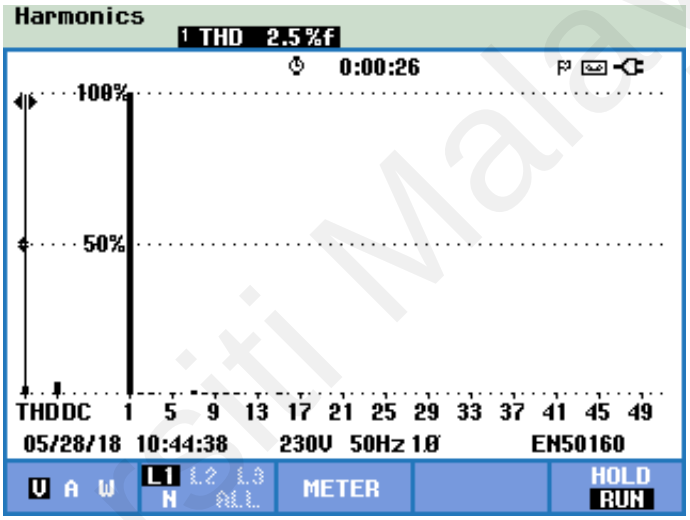


Figure 5.44: Output-Voltage THD for Balanced Condition being 2.5 %

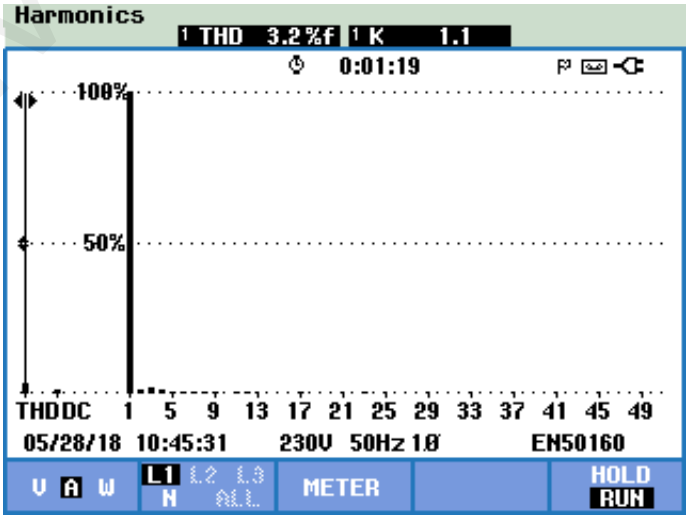


Figure 5.45: Output-Current THD for Balanced Condition being 3.2 %

5.5 Summary

This chapter presented the hardware implementation and experimental results for the proposed MLI topologies. Two PWM control schemes were used. For TCHB eight reference signals identical to each other and with an offset equaling the amplitude of the triangular carrier signal were used to generate the PWM signals. For PiCHB twelve reference signals identical to each other and with an offset equaling the amplitude of the triangular carrier signal were used to generate the PWM signals.

First the architecture of the TMS320F28335 DSP platform and the ALTERA Cyclone-II FPGA was examined. Followed, by the hardware configuration for high-switching-frequency experiment with various modulation indices, and application of the proposed inverters in a PV systems. Here, the PV applications were stand-alone and grid-connected systems. Some of the tests were based on the Australian Standards As 4777.3-2005, IEC 61727 and the IEC 61683:1999 for grid-connected PV application, as the Malaysian standard also refers to these standards. Two PV-inverter hardware prototypes were built: The proposed TCHB, and the PiCHB inverter topologies. Those inverters were tested in a grid-connected PV system. The experiment results were recorded, and the values measured were compared.

CHAPTER 6: CONCLUSIONS AND FUTURE WORK

6.1 Concluding Remarks

This work comprised of theoretical analysis, computations, simulations, and experiments on single-phase T-type Cascaded H-Bridge (TCHB) and π-type Cascaded H-Bridge (PiCHB) Multilevel Inverters (MLI) that generate nine-level and thirteen-level output-voltage, respectively.

The proposed MLI of this study consists mainly of two H-Bridges cascaded along with two T-type Bidirectional Switches (BSs) for TCHB and two π-type BSs for PiCHB. The CHB inverter, along with the auxiliary circuits comprising of the BSs, remains the main inverter of the proposed topologies. This offers higher number of the output-voltage levels and reduces the harmonic content of the output waveform. Comparatively analyzing the proposed techniques against the Conventional Cascaded H-Bridge (CCHB) and the Switch Capacitor based H-Bridge (SCHB), the proposed TCHB and PiCHB offer lesser standing-voltages on the semiconductor switches, consequently with reduced cost function. In addition, lesser number of switches and the corresponding gate drivers required to produce the desired output-voltage levels make the proposed techniques a favorable choice.

PWM control schemes were utilized for high switching frequency application in the proposed TCHB and PiCHB MLI. For TCHB, eight identical reference signals were intersected against one carrier signal. All the reference signals were equal in phase and amplitude, except that they were kept at an offset that was equivalent to the amplitude of the triangular carrier signal. Control of the modulation index gave the desired number of levels of the inverter's output voltage. The PWM was designed in such a fashion to attain self-balancing on the DC-Link capacitors. Similarly for PiCHB, twelve identical

reference signals were intersected against one carrier signal. By controlling the modulation index, desired number of output-voltage levels could be attained. However, to attain Balanced Voltage Sharing (BVS) at the DC-Link Capacitors, an extra RLC passive balancing circuit was added to the system.

The proposed MLI were employed to both stand-alone and grid-tied PV systems. Particularity for grid-connection, a DC-DC boost converter and low frequency transformer were provided to the proposed MLI. The control system for grid-connected PV system comprised of mINC MPPT, PI current control, and islanding protection.

Matlab/Simulink computed the optimized switching angles and simulated the proposed MLI in those applications. The simulation results were verified by experiment through a laboratory prototype. In the experiment, all the algorithms were implemented in a TMS320F28335 DSP.

The experiment results indicate that the higher the modulation index, the lower the THD of the proposed inverter.

6.2 Author's Contribution

The development of single-phase nine and thirteen-level inverters with fewer switches and lower-distortion output waveform was crucial to this study. Two PWM control schemes, and grid-connected PV system applications were introduced. The study described the proposed MLI, the numerical and algebraic analysis for the applied control method, the DC-Link capacitor voltage balancing techniques, the computer simulations, and the laboratory prototype measurements. Major contributions of this work are:

1) TCHB configuration employing 12 power switches and 10 gate drivers that emerged from the additional two bidirectional circuits containing four switches, with one BS in each cascade. The harmonic waveforms improved, and a nine-

level output-voltage was achieved. (publication: IET Power Electronics – Under review).

2) PiCHB configuration employing 16 power switches and 12 gate drivers that emerged from the additional four bidirectional circuits containing eight switches, with two BSs in each cascade. The harmonic waveforms attained were even better than the TCHB inverter, and a thirteen-level output-voltage was attained. (publication: IEEE TRANSACTIONS on Power Electronics – Under review).
3) NRM solution of the non-linear equations of the OHESW technique for low frequency switching. (publication: Renewable and Sustainable Energy Reviews journal).
4) Two PWM control schemes generating the pulses for the switching devices. For TCHB the PWM control used eight reference signals instead of one to generate the PWM signals. The eight reference signals were identical except for an offset value, which equaled the amplitude of the carrier signal. The TCHB PWM control offered BVS. Similarly, for PiCHB the PWM control used twelve reference signals instead of one to generate the PWM signals. The twelve reference signals were identical except for an offset value, which equaled the amplitude of the carrier signal. However, to achieve BVS a passive balancing circuit was added to the system.
5) Use of two-stage power converter configuration comprising DC-DC boost converter and the proposed cascaded MLI in the grid-connected PV system. (publication: Solar Energy journal).
6) A control system employed for grid-connection of cascaded inverters with MPPT based on mINC, current controller based on PI technique, and islanding protection.

6.3 Future Works

Future work can be performed on the existing designs, to increase power conversion and decrease the harmonic content of the inverter output waveforms. Suggested future works are:

1) To increase power capacity of the grid-tied MLI to 10kW for residential and industrial applications.
2) Shifting to a transformer-less topology employing leakage current reduction.
3) Utilizing active islanding protection techniques for islanding protection.
4) Utilizing filters of reduced size and low-pass filter as LC and LCL filters.
5) Along with the cascaded inverters, utilization of cascaded DC-DC boost converters in the proposed MLI.
6) Utilization of different MPPT techniques as FL, NN, ACO etc.
7) Employing different switching frequency modulation techniques as the SVM and OMTHD.
8) Solving the non-linear transcendental equations by NN or ACO.
9) Utilization of different current-control techniques mentioned.

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5. Amir, A., Amir, A., Selvaraj, J., Rahim, N. A. (2016). Study of the MPP tracking algorithms: Focusing the numerical method techniques. Renewable and Sustainable Energy Reviews. Volume 62, September 2016, Pages 350 371" (*ISI-Indexed*)

Journal Papers Under Review:

1. Amir, A., Amir, A., Selvaraj, J., Rahim, N. A., Williams, W. B. (2019). “Single-Phase π-Type Thirteen-Level Cascaded Grid Connected Inverter with Passive Balancing Circuit for Photovoltaic System.” IEEE TRANSACTIONS on Power Electronics

2. Amir, A., Che, H. S., Amir, A., ElKhateb, A., Elias, M. F. M., Rahim, N. A., Williams, W. B. (2019). "Ultra-High Gain DC-DC Converters Based on Fullwave Voltage Multipliers." IEEE TRANSACTIONS on Power Electronics

3. Amir, A., Amir, A., Selvaraj, J., Rahim, N. A. (2019). "Single-Phase T-Type Cascaded H-Bridge Nine-Level Grid-Connected Inverter for Photovoltaic System." IET Power Electronics

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