# DESIGN OF A SINGLE-CARRIER PULSE WIDTH MODULATION WITH SUBMODULE FAULT-TOLERANT CAPABILITY FOR MODULAR MULTILEVEL CONVERTER

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2020

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**THESIS SUBMITTED IN FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF MASTER OF ENGINEERING SCIENCE**

**FACULTY OF ENGINEERING**
**UNIVERSITY OF MALAYA**
**KUALA LUMPUR**

**2020**

**UNIVERSITY OF MALAYA**

**ORIGINAL LITERARY WORK DECLARATION**

Name of Candidate: **TUANKU BADZLIN HASHFI**

Matric No: **KGA 160002 / 17013606/1**

Name of Degree: **Master of Engineering Science**

Title of Project Paper/Research Report/Dissertation/Thesis :

**DESIGN OF A SINGLE-CARRIER PULSE WIDTH MODULATION WITH SUBMODULE FAULT-TOLERANT CAPABILITY FOR MODULAR MULTILEVEL CONVERTER**

Field of Study: **Power Electronics**

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**DESIGN OF A SINGLE-CARRIER PULSE WIDTH MODULATION WITH SUBMODULE FAULT-TOLERANT CAPABILITY FOR MODULAR MULTILEVEL CONVERTER**


## ABSTRACT

Multilevel converters are attracting a lot of attention and becoming one of the energy conversion choices for new topologies and control in industry applications and research fields. Modular multilevel converters (MMCs) are considered very promising among converter topologies for future medium-voltage and high-power applications compared to NPC, FC and CHB topologies.

The improved phase disposition pulse width modulation (PDPWM) technique control for MMCs, which has a fault-tolerant capability, is presented. This study presents two methods to distribute pulses into submodules (SMs) by using PDPWM which has drawback to distribute the power equally among the submodules (SMs). First method, this study used conventional PDPWM to distribute the power equally among the SMs. Second, this study utilized one single carrier that can improve modulation strategy that has flexibility for fault-tolerant capability. Fault tolerance can enhance converter reliability, which is one of the essential issues of half-bridge MMCs with substantial switching devices. An excellent overall control system is also required for MMCs to rebalance the capacitor after a fault.

An understanding of the basic operating principle is essential in order to find the dimensioning factors of modular multilevel converter (MMC). The dimension of MMC was designed in MATLAB/Simulink by ensuring the performance is well governed in circulating current and energy balance for closed-loop control. The improvement of modulation technique was tested in a simulation platform and hardware implementation.

In this study, an MMC with a fault condition was analyzed. Afterward, a modulation control for the fault-tolerant method was proposed and described in detail. The proposed method bypassed the faulty SM when a faulty switching device occurs in an SM. The proposed method was tested in MATLAB/Simulink platform to verify the proposed method in the simulation platform. Experimental results were included to verify the fault-tolerant capability of the proposed modulation strategy for MMCs.

Keywords: Modular multilevel converter (MMC), fault-tolerant control, modulation technique, reliability.

**REKABENTUK PEMBAWA TUNGGAL PERMODULATAN LEBAR DENYUT DENGAN KEMAMPUAN BOLEH TERIMA KEGAGALAN SUBMODUL UNTUK PENGUBAH PELBAGAI PERINGKAT BERMODUL**


**ABSTRAK**

Pengubah pelbagai berperingkat semakin banyak perhatian dan menjadi salah satu pilihan penukaran tenaga untuk topologi dan kawalan baru dalam bidang aplikasi dan penyelidikan industri. Pengubah pelbagai peringkat bermodul (MMC) boleh dianggap sangat menjanjikan di kalangan topologi penukar untuk masa depan seperti voltan sederhana dan aplikasi berkuasa tinggi berbanding dengan topologi pengapit titik neutral (NPC), pemuat terbang (FC) dan lata jambatan-separuh (CHB).

Pelupusan fasa pemodulatan lebar denyut (PDPWM) pengawal untuk MMC, yang mempunyai keupayaan toleransi kegagalan, telah dibentangkan dalam kajian ini. Kajian ini membentangkan dua kaedah untuk mengedarkan denyutan ke submodul (SM) dengan menggunakan PDPWM. PDPWM mempunyai kelemahan untuk mengedarkan kuasa yang sama di antara submodul – submodul (SMs). Kaedah pertama, kajian ini masih menggunakan PDPWM konvensional untuk mengedarkan kuasa yang sama di susunan SM. Kedua, kajian ini menggunakan satu pembawa tunggal yang dapat meningkatkan strategi modulasi yang mempunyai kelonggaran untuk keupayaan toleransi kegagalan. Toleransi kegagalan boleh meningkatkan kebolehpercayaan penukar, yang merupakan salah satu isu penting bagi MMC setengah jambatan dengan peranti penukaran besar. Sistem kawalan keseluruhan yang sangat baik juga diperlukan MMCs untuk mengimbangi kapasitor selepas kegagalan.

Prinsip operasi asas adalah penting untuk mencari faktor dimensi dari MMC. Dimensi MMC direka bentuk dalam MATLAB/Simulink dengan memastikan prestasi pengawalan baik edaran aliran gelung semasa dan tenaga yang beredar. Peningkatan teknik modulat diuji dalam platform simulasi dan pelaksanaan perkakasan.

Dalam kajian ini, MMC yang mempunyai keadaan kegagalan telah dianalisis. Selepas itu, kawalan modulasi untuk kaedah toleran kegagalan telah dicadangkan dan diterangkan secara terperinci. Kaedah yang dicadangkan memintas SM yang gagal apabila peranti penukaran yang gagal berlaku pada SM. Kaedah yang dicadangkan telah diuji menggunakan MATLAB / Simulink untuk mengesahkan kaedah yang dicadangkan dalam simulasi. Keputusan eksperimen dimasukkan untuk mengesahkan keupayaan toleransi kegagalan strategi strategi modulasi yang dicadangkan untuk MMCs.

Kata kunci: Pengubah pelbagai peringkat bermodul (MMC), kawalan toleransi kegagalan, teknik modulat, kebolehpercayaan.

## ACKNOWLEDGEMENTS

First of all, I would like to thank almighty ALLAH SWT. I also want to express my highest appreciation to my supervisor Prof. Dr. Saad Mekhilef and Dr. Marizan Mubin for their support, assistance and understanding. I have been very grateful and honored to work with such brilliant and warm-hearted advisors.

All the research friends in Power Electronics and Renewable Energy Research Laboratory (PEARL) cooperate very friendly during this research work and I would like to extend my gratitude to them.

Furthermore, I would like to thank my parents (Ir. Tuanku Muntazar and Ravita), siblings (Tuanku Badral Maruzi SE., Ak, dr. Tuanku Radhi Sura and Tengku Yumna Dara Yani, S. Ars) and friends ( Leong Wen Chek, Haidar, Nasser, Zahir, Immad, Dr. Faradila, Shammem and Ahmed) for giving continuous emotional support and prayers during my study period.

Finally, I would like to thank administrative staffs in the Department of Electrical Engineering, Faculty of Engineering and Institute of Graduate Studies for providing valuable assistance and facilities during my study.

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| | | |
|---|---|---|
| $V_{DC}$ | : | Direct Current (DC) Voltage |
| $dV/dt$ | : | Change in Volts / Change in Time; Rapid Voltage Rise at Each Pulse in a PWM |
| $m$ | : | Modulation Index |
| $m_f$ | : | Frequency Modulation Index |
| $m_a$ | : | Amplitude Modulation Index |
| $n$ | : | Number of Level |
| $A_m$ | : | Amplitude Modulation |
| $A_c$ | : | Amplitude Carrier |
| $n-1$ | : | Number of Carrier |
| $\emptyset$ | : | Phase Shift in PSPWM |
| $T_d$ | : | Time Interval |
| $N$ | : | Number of Submodule |
| $N_{faulty}$ | : | Number of Faulty Submodule |
| $V_{SM}$ | : | Submodule Voltage |
| $f_{eff}$ | : | Effective Frequency |
| $f_{sw}$ | : | Switching Frequency |
| $u$ | : | Upper |
| $l$ | : | Lower |
| $N_{Ju}$ | : | Number of Submodule for Upper Arm |
| $N_{Jl}$ | : | Number of Submodule for Lower Arm |
| $N_J$ | : | Total Number of Submodule |
| $V_{eJ}^{ref}$ | : | Voltage Reference Signal |

| | | |
|---|---|---|
| $I_{upper}$ | : | Upper Current |
| $I_{lower}$ | : | Lower Current |
| $I_{DC}$ | : | DC Current |
| $I_{circ}$ | : | Circulating Current |
| $I_{diff}$ | : | Differential Current Mode |
| $cos\ \theta$ | : | Power Factor |
| $\theta$ | : | Power Factor Angle |
| $N_u$ | : | Insertion Index for Upper Arm |
| $N_l$ | : | Insertion Index for Lower Arm |
| $V_{out}$ | : | Out Voltage / AC Voltage |
| $I_{out}$ | : | Out Current / AC Current |
| $V_{lower}$ | : | Lower Voltage |
| $V_{upper}$ | : | Upper Voltage |
| $V_{internal}$ | : | Internal Voltage |
| $L$ | : | Arm Inductance |
| $R$ | : | Equivalent Arm Resistance |
| $P_{upper}$ | : | Upper Arm Power |
| $P_{lower}$ | : | Lower Arm Power |
| $V_c$ | : | Capacitor Voltage |
| $W_c^{\Sigma}$ | : | Total Input Energy Supplied |
| $W_c^{\Delta}$ | : | Differential Energy Supplied |
| $C_{PR}$ | : | Proportional Resonant Controller Transfer Function |
| $C_{PI}$ | : | Proportional Integral Controller Transfer Function |
| NPC | : | Neutral Point Clamped |
| FC | : | Flying Capacitor |

| | | |
|---|---|---|
| CHB | : | Cascaded H-Bridge |
| MMC | : | Modular Multilevel Converter |
| PWM | : | Pulse Width Modulation |
| LSPWM | : | Level Shifted Pulse Width Modulation |
| PSPWM | : | Phase Shifted Pulse Width Modulation |
| CBSPWM | : | Carrier-Based Sinusoidal Pulse Width Modulation |
| DC | : | Direct Current |
| AC | : | Alternating Current |
| IGBT | : | Insulated Gate Bipolar Transistor |
| THD | : | Total Harmonic Distortion |
| KVL | : | Kirchhoff's Voltage Law |
| KCL | : | Kirchhoff's Current Law |
| HVDC | : | High Voltage Direct Current |
| HB | : | Half-Bridge |
| FB | : | Full-Bridge |
| PDPWM | : | Phase Disposition Pulse Width Modulation |
| PODPWM | : | Phase Opposition Disposition Pulse Width Modulation |
| APODPWM | : | Alternate Phase Opposition Disposition Pulse Width Modulation |
| THD | : | Total Harmonic Distortion |
| EMI | : | Electrmagnetic Intefrence |
| HVDC | : | High Voltage Direct Current |
| SVM | : | Space Vector Modulation |
| SHE | : | Selective Harmonic Elimination |
| NLM | : | Nearest Level Modulation |

| | | |
|---|---|---|
| SM | : | Submodule |
| PI | : | Proportional Integral |
| PR | : | Proportional Resonant |

# CHAPTER 1: INTRODUCTION

## 1.1 Introduction

Based on the operation in growing energy demand of modern civilization and the substitutions of human activities have brought the new level of complexity association and sophisticated devices. Studies on electric power generation for renewable resources and power conversion devices has become increasingly essential everyday (Bahrman & Johnson, 2007; Han et al., 2017; Islam et al., 2015) to overcome the circumstance of modern civilizations. The illustration power system from generation to industry and home is as shown in Figure 1.1 (Bahrman & Johnson, 2007). The developments of new technologies and power electronics devices in the 21$^{th}$ century have boosted the concentration in smart electric power systems.

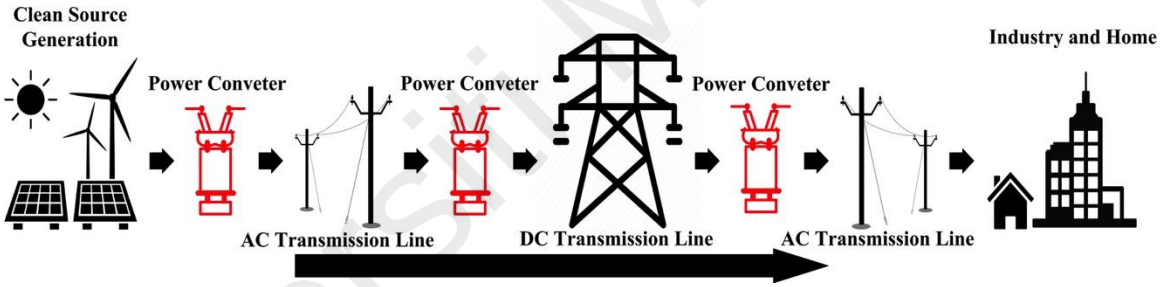



**Figure 1.1:** Illustration of power system.

Nowadays in industry and academia, multilevel converters are considered as one of the best for power conversion due to innovative topologies and controls. Presently, multilevel converters have been commercialized and customized in a wide range of products for several powers applications, such as reactive power compensation, renewable energy conversion, railway-traction, and high-voltage direct-current (HVDC) transmission. Eventhough the technology of multilevel converters has already been developed so that they can be considered established and verified technologies, they still have quite a few associated challenges. These challenges persuade many researchers to overcome the problems and discover new ways to advance energy efficiency, reliability,

power density. It also stimulates and enlarges the application fields as they become more attractive and superior than the conventional topologies (Zhang et al., 2017).

The first concept was the stepped-wave switching power converter circuit using a series-connected H-bridge. Then, the concept of the neutral point clamped (NPC) converter was proposed in the late 1970s. Afterward, the Flying capacitor (FC) multilevel topology was introduced for low-power applications. The three-level NPC converter was developed and the technology came into industries in the mid-1990. Similarly, Flying Capacitor converters increased industrial relevance in the early 1990s (Rodríguez et al., 2007).

These multilevel voltage source converter topologies were classified into single DC supply and multiple DC supply. Basically, the hybrid topologies are combination of the existing multilevel converter topologies combined together to obtain a new multilevel structure, which can provide superior performance in some aspects (Kouro et al., 2010; Rodríguez et al., 2007). The topology of interest in this thesis is Modular Multilevel Converter (MMC) that was introduced by A Lesnicar and R Marquardt in 2003 (Lesnicar & Marquardt, 2003). The emergence of the modular multilevel converters have become a very attractive topology due to their various advantages, such as remarkable advacement in designing modularity scheme; high availability, including redundant operation; failure management, reliability, and simple structure-based converter design; high front-end flexibility; grid connection via standard transformer or transformerless and very promosing topology for high voltage direct current (HVDC) (Debnath et al., 2014).

## 1.2 Problem Statement

The traditional two-level inverters have numerous problems related to the frequency switching which produced common-mode voltage and high voltage change $dV/dt$ rates to the motor windings (Manjrekar et al., 1999). Multilevel converters can overcome all

these problems because their devices can switch at lower frequency and less voltage $dV/dt$ rates. As advanced technology, multilevel converters have hogher complexity compared to the conventional converter, where the multilevel converter required more component and higher complexity to design the control. Due to the continuous emergence of multilevel converter, especially MMC, many questions about the modeling, control, advantages, and disadvantages were arised. Consequently, a significant effort has been devoted to develop the converter for medium voltage applications such as motor drives. First, since the design of the MMC requires a good understanding of the operation principles of the converter, the modeling approach should be chosen to provide an analysis of the converter's operation. Afterward, another issue is to consider the controller for the MMC (Debnath et al., 2014; Perez et al., 2014).

Power switch and control in converter are needed to be safe reliable and accessible in order to achieve all the requirements and reduce the environmental impacts. A redundant switching state is provided by some of the multilevel topology by allowing the converter to maintain normal operation under internal fault conditions (device fault) (Lu & Sharma, 2009). The MMC with half-bridge Submodule (SM) has a simple circuit configuration, which can limit redundancy switching. Generally, the half-bridge MMC needs to include redundant SM or reserved SM to eliminate the limitation of half-bridge SM. In MMC structure, there are many potential internal failure points based on semiconductor devices such as IGBT and diodes in SMs. When a switching device fails, the faulty SM including the faulty switching device is bypassed and redundant SM or reserved SM is inserted to replace the faulty SM, and it is so vital to detect and locate the fault after the occurrence within a short time in the way of system reliability (F. Deng et al., 2016; Li et al., 2016). The unbalanced SM voltages of arms and loss of some parts of the voltage level are found during SM failure. Few SM redundancy strategies have been proposed (Ahmed et al., 2015; Kim, Kim, Han, & Yoon, 2015; Saad, Guillaud, Mahseredjian, Dennetière, &

Nguefeu, 2015) to solve faulty SM. All these strategies have been reviewed in some journals (Farias, Cupertino, Pereira, Junior, & Teodorescu, 2018). Most of the strategies use phase shifted pulse width modulation (PS-PWM) and nearest level modulation (NLM). In this technique, each of SM needs multiple carrier waves, which is phase shifted from the other SM carriers. NLM technique is used to control the converter which creates high fluctuation on capacitors voltage for this technique. Modulation technique and the control algorithm are the main part to control the pulses at each of SM to keep the balance among the SMs. Thus, simple modulation technique is developed in this work that has only a single carrier for all the SMs and may respond with the failure of SM.

## 1.3 Research Objective

The main objective of this thesis is to develop a new solution to avoid the unbalanced SM voltages created by a faulty SM. A single-phase MMC is firstly tested through simulation and implemented in real laboratory setup. The objectives are listed as follows:

1. To model the modular multilevel converters (MMC) in the MATLAB/Simulink.
2. To design and test the model circulating current and energy balance closed-loop control for MMC in MATLAB/Simulink.
3. To validate the improvement of the modulation technique during submodule failure in MATLAB/Simulink and hardware implementation.

## 1.4 Thesis Outline

The research methodology adopted in this research work consisted of five stages. The first stage discusses about the background of this work, including the problem statements and research objectives that need to be achieved.

In chapter 2, Literature review is carried on to arrange the state of art about the multilevel voltage source converter technologies including the well-known existing

multilevel converter topologies, MMC technologies and modulation schemes being used by MMC topologies. The presented literature review is carried out by the help of journals, magazines, conference papers, and theses.

Additionally, chapter 3 presents the mathematical derivations, working principles of the MMC and control strategies used in this project. The multilevel converters need multiple PWM (sawtooth waveform) to decide the level of the output voltage. Each pulse is generated by comparison of the sawtooth waveform and the reference signal will trigger a particular switch to generate a certain level of the output voltage. Chapter 4 presents the study of the phase disposition pulse width modulation (PWM) for the MMC topology. The developed modulation strategy of phase disposition pulse width modulation (PDPWM) with capability of working under internal fault (device fault) is well explained in this chapter.

Furthermore, chapter 5 presents a practical implementation of the designed converter and the effectiveness of the developed modulation control scheme. The obtained simulation and experimental result are compared and the validity of the single-phase MMC prototype is presented. A laboratory prototype of the MMC is built and some loads are connected to verify their performances. The converter design includes the switching device and sensor circuit. The appropriate switching gate signals for inverter's switches are generated by the Speedgoat Real-Time Target Machine controller. The voltages and current measurements are presented to demonstrate the converter performance with the proposed modulation control strategies. Then, the achievements of the project objectives are evaluated.

In chapter 6, conclusion of study results are presented. As this study is baseline for fault-tolerant capability during SM failure. This chapter also provides some

recommendations those can be considered in conducting future studies to increase the performance fault-tolerant capability and more case studies during the failure.

# CHAPTER 2: REVIEW OF MULTILEVEL CONVERTER TOPOLOGIES AND MODULATION CONTROL STRATEGIES

## 2.1 Introduction

This chapter aims to describe the modular multilevel converters (MMCs) and put into multilevel converter context. This chapter starts with a review of the other converter topologies. The basic decription and analysis of the development of MMC are compared to the other similar topologies.

Renewable energy sources, energy storages, distribution power generations and high voltage interconnected grids such as high voltage direct current (HVDC) need to be in the interconnected system. Voltage source converters are power conversion system formed by a group of switches, diodes, power supplies (either AC supply or DC supply) and capacitors. These are the common items inside the power conversion either converting AC-to-DC, DC-to-AC, AC-to-AC, or DC-to-DC. This demonstrates the difference between the conventional two-level voltage source inverter and the multilevel inverters.

The previous voltage source converter topology was the two-level converter and it is still the choosen solution for low-voltage application. The traditional two-level inverter can produce adjustable amplitude and frequency output voltage waveform by controlling the modulation index and a time average of their two voltage levels (Tolbert et al., 1999). This is usually achieved by pulse width modulation (PWM) schemes.

The modification to multilevel converter topologies can offer important expansions for large applications. The benchmark of multilevel converter is the number of voltage levels that produced by the converter. Visually, it can be described as the number of voltage stairs, where each phase of the converter has to generate at least three different voltage levels as shown in Figure 2.1. The three different bridge-leg structures composed by different number series-connected DC voltage supplies and output voltage levels

terminals are controlled to achieve the desired stepped waveform with two, three and four voltage levels.

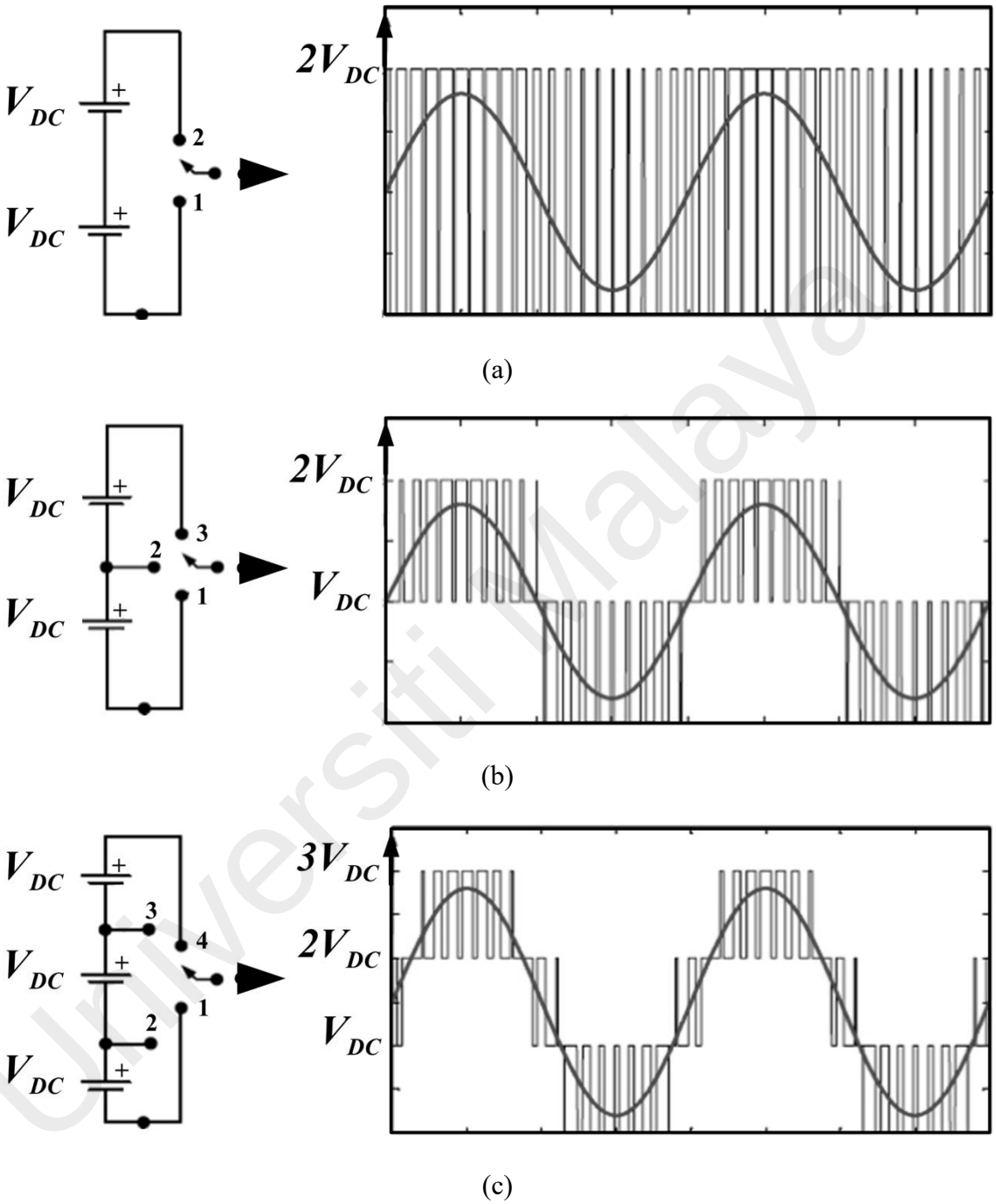



**Figure 2.1:** Bridge-leg with their stepped voltage waveforms (a) two-level (b) three-level and (c) four-level.

Comparing the traditional two-level converter and the multilevel converter can generate more voltage levels improving the power quality as stated below:

1. The voltage waveform shape is closer to the pure sine wave. Therefore the total harmonic distortion THD can be reduced significantly as well as the size of the filter.
2. The more voltage steps result in reducing the $dV/dt$ stress and therefore electromagnetic compatibility EMC can be reduced.
3. The availability of a higher number of voltage level eases the need for the high switching frequency PWM and provides the potential to reduce switching losses in the switching device. When lower switching frequency is used, lower switching loss and a higher efficiency are obtained.
4. Multilevel converters usually generate a smaller common-mode voltage. As a result, less stress in the motor bearing is generated in the motor drive system.

Multilevel converters also have some drawbacks and limitations. This can be observed from higher number of switches required and higher complexity of electrical wiring compared to the conventional converter. The basic multilevel converters design use the capacitive voltage at the DC-side in order to divide the DC input voltage; which means increasing the difficulty of the controller to regulate the stability of the converter system compared to the conventional two-level converter.

## 2.2 Multilevel Voltage Source Converter Topologies

The differences between the multilevel converter topologies have been developed in the research field and applied in industrial applications. The most general multilevel converters configurations are Neutral Point Clamped (NPC), Flying Capacitor (FC), Cascaded H-Bridge (CHB) and Modular Multilevel Converter (MMC) (Mahrous et al., 2007; Rodríguez et al., 2002). The configurations of multilevel converters are divided

into 2 categories: 1) Single input voltage; 2) Separate Isolated Multiple Input voltages, as shown in Figure 2.2.

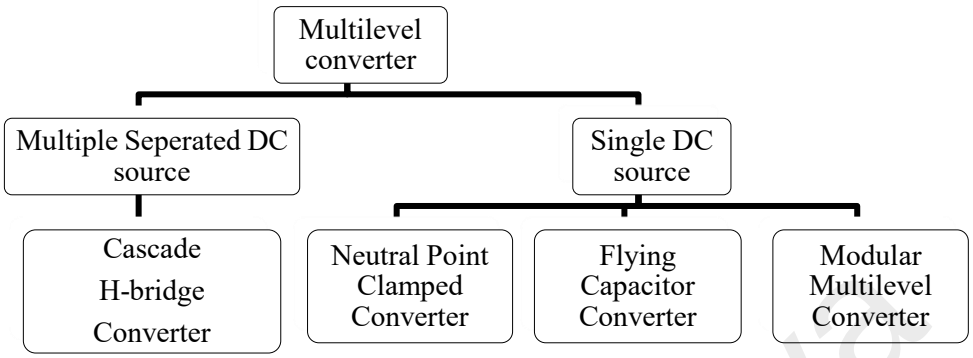
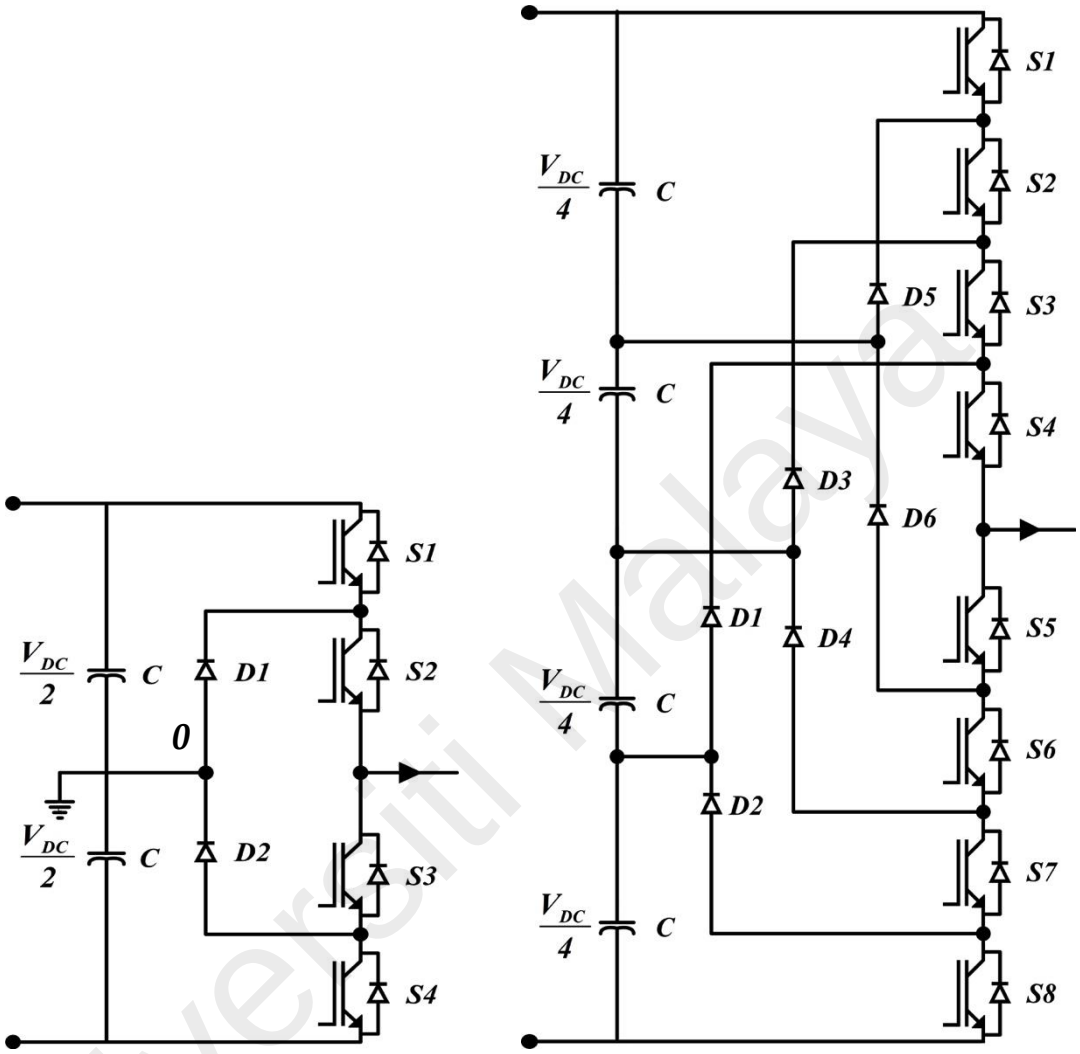



**Figure 2.2:** Classification multilevel converter topology.

### 2.2.1 Neutral Point Clamped Multilevel (NPC) Converter

NPC converter is also called the diode-clamped converter when it was first used in three-level. Figure 2.3(a) depicts the basic circuit diagram of the three-level NPC bridge-leg. Four power switches build the bridge-leg, *S1* to *S4*. On the other side of bridge-leg, the DC-link capacitors split into two, forming a neutral-point '*0*'. Two diodes, *D1* and *D2* are connected to '*0*' are called as clamping diodes. The essential purpose of clamping diodes is to connect the AC terminal to the middle-point (neutral point) of the DC-link (Rodriguez et al., 2010). As the first generation of multilevel converter, NPC uses lower switching frequency compared to conventional two-level converters as well as producing lower switching losses and higher efficiency at the output terminal. The other advantages of NPC are each semiconductor switch has lower blocking voltage and still has simple control method. In contrast, a large number of clamping diodes is required when the number of level increases and results in increasing the complexity in mechanical construction. NPCs do not have a failure management due to the model of construction, nor do they have redundant switching state. The difficulty in balancing the capacitor voltage is more complex along with increasing the number of level. Obviously, increase

in the number of level will demand more component lists as shown in Figure 2.3(b). The number of component is indicated in Table 2.1.




(a) (b)

**Figure 2.3:** Neutral point clamped (NPC) multilevel converter.

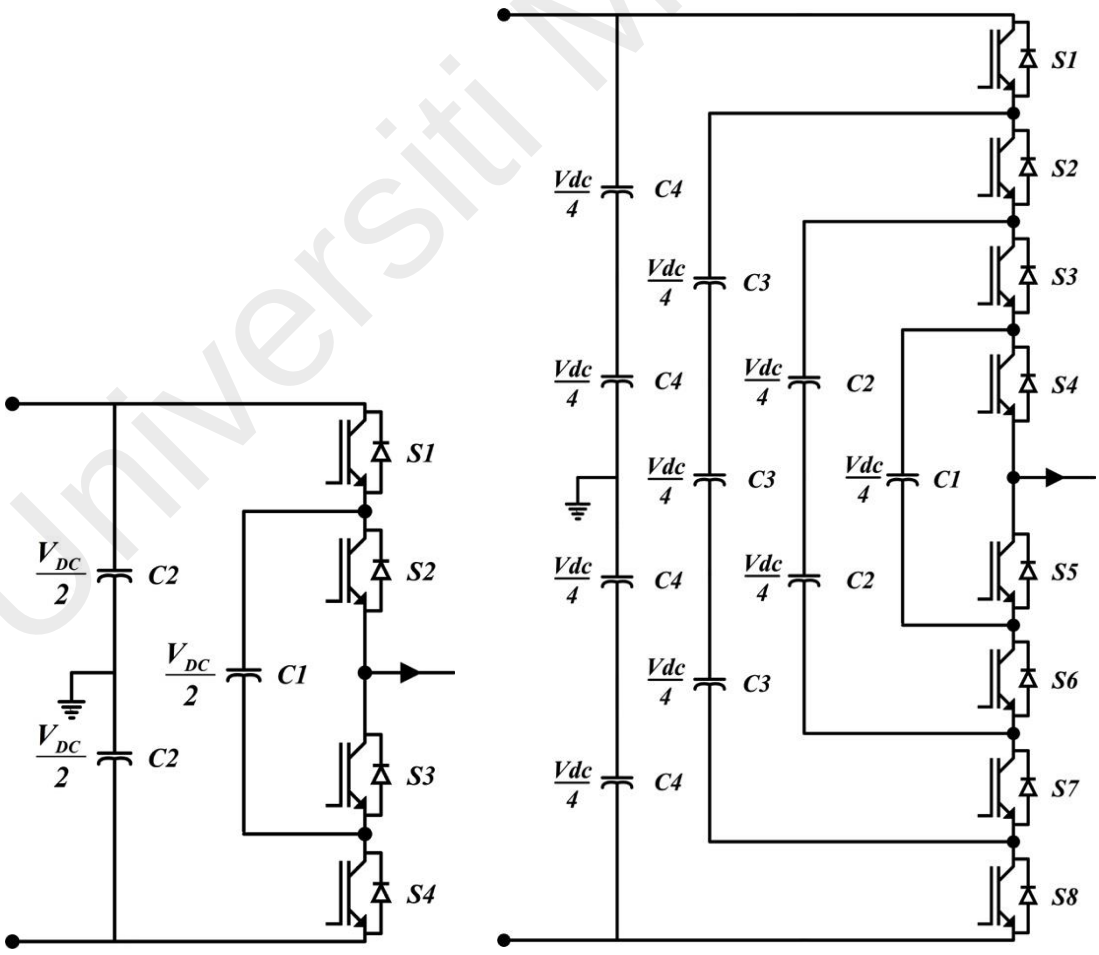
**Table 2.1: Number of component in NPC converter.**

| Power Switches | Clamping Diodes | Clamping Capacitors | DC Bus Capacitors |
|---|---|---|---|
| $2(n-1)$ | $(n-1)(n-2)$ | 0 | $(n-1)$ |

### 2.2.2 Flying Capacitor (FC) Multilevel Converter

The basic circuit diagram of a three-level FC bridge-leg is in some ways similar to three-level NPC bridge-leg, with the main difference is that the clamping diodes are

replaced by floating capacitors, as can be seen in Figure 2.4. FC converters employ many capacitors that are maintained at a different voltage level to generate different output voltage by linking different capacitors to the output (Zhang & Watkins, 2007). FC converters have similar advantages to NPC converters which can eliminate the drawbacks of the conventional two-level converters. The main features of the FC are redundancy switching state during combination in order to balance the different levels. FC converters also have fault-tolerance issues due to the redundancy switching state and a large number of capacitors. The configuration of FC converters are not modularity configuration that have more difficulties in packaging the converter and more complex control for high number of levels due to a large number of floating capacitors. The number of component in FC converter per leg is indicated in Table 2.2.




(a) (b)

**Figure 2.4:** Flying capacitor (FC) multilevel converter; (a) three-level, (b) five-level.

**Table 2.2: Number of component in FC converter.**

| Power Switches | Clamping Diodes | Floating Capacitors | DC Bus Capacitors |
|---|---|---|---|
| $2(n-1)$ | 0 | $\frac{(n-1)(n-2)}{2}$ | $(n-1)$ |

### 2.2.3 Cascaded H-Bridge (CHB) Multilevel Converter

CHB is multilevel converter built by two or more H-bridge power cells (single-phase with four switches) connected in a series chain, as shown in Figure 2.5. Each of the H-bridge power cells is able to produce three different voltage levels. Based on magnitudes of the DC voltage supplies of H-bridge power, the CHB multilevel converter can be called as symmetrical and asymmetrical CHB multilevel inverters (Latran & Teke, 2015; Taleb et al., 2015). CHB topology can be utilized as symmetrical topology using equal DC voltage supplies and asymmetrical topology which uses unequal DC voltage supplies. This converter has cascadeds or modularity structure that can optimize the circuit layout. CHB structure also has fault-tolerant capabilities and can work with a reduced number of levels in case of a fault by bypassing the faulty module. This topology needs separate DC supply or a coupling transformer to separate multiple sources by means that each bridge cell will need a transformer and increase both the cost of converter and increase the volume of the converter. The number of component in FC topology per leg is indicated in Table 2.3.

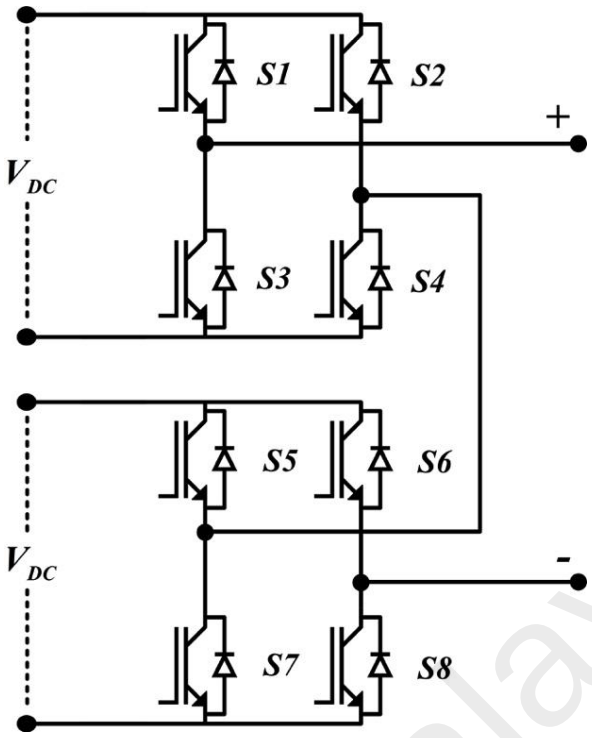



**Figure 2.5:** 5-level Cascaded H-bridge (CHB) multilevel converter.

**Table 2.3: Number of component in CHB topology.**

| Power Switches | Clamping Diodes | Clamping Capacitors | DC power supply |
|---|---|---|---|
| $2(n-1)$ | 0 | 0 | $\frac{(n-1)}{2}$ |

### 2.2.4 Modular Multilevel Converter (MMC)

MMC was first introduced by Lesnicar, which finally provides a significant breakthrough in the area of medium voltage power conversion and high voltage application (Lesnicar & Marquardt, 2003). It has obvious advantages over other types of voltage source converters such as flying capacitor (FC) converter, neutral point clamped (NPC) converter and cascaded H-bridge (CHB), as mentioned previously. It has high voltage quality based on the PWM controlled power stage, redundancy ability from multiple levels based on its hierarchical structure, and energy storage capability based on the embedded capacitor within each module. The hierarchical structure of single-phase MMC can be seen in Figure 2.6. The number of component in MMC topology per leg is

indicated in Table 2.4. In addition, the DC voltage level of module internal capacitor can be balanced by the properly controlled algorithm at the topology level; thus, no extra voltage balancing circuit will be needed as in the NPC converter and FC converter (Fazel et al., 2007; Latran & Teke, 2015). Table 2.5 compares among multilevel converter topologies This topology can accommodate any possible power conversion function, capable of reaching any voltage, as current and power levels using identically rated modules. Following the research professions in this area, more and more potential of MMC will be discovered and realized in the near future. MMC is capable of incorporating a very high number of SM to produce high voltage levels with small distortions. Therefore, it has become one of the most attractive and promising converters, especially for HVDC applications. Siemens commercially installed the first MMC-HVDC transmission in 2010 and some projects using MMC-HVDC for the interconnection of large wind farms will be commissioned in the next few years.

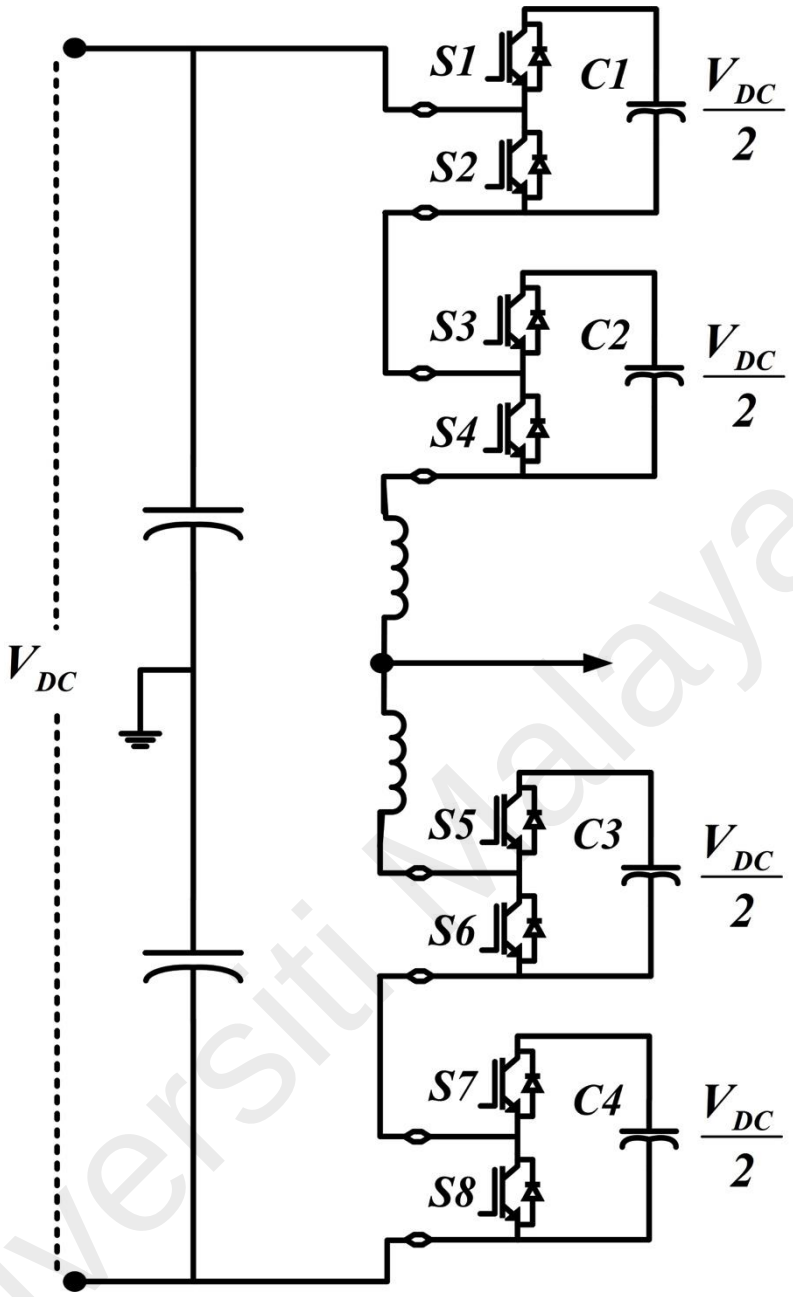



**Figure 2.6:** 2 submodule half-bridge modular multilevel converter.

**Table 2.4: Number of component half-bridge MMC topology.**

| Power Switches | Clamping Diodes | Floating Capacitors | DC Bus Capacitors |
|---|---|---|---|
| $2(n-1)$ | 0 | $\frac{(n-1)(n-2)}{2}$ | 2 |

**Table 2.5: Comparison multilevel converter topology.**

| Converter | Voltage Quality | DC-balance | Redundancy | Capacitors Volume |
|---|---|---|---|---|
| 2-levels VSC | Poor | No Concern | None | High |
| NPC/ANPC | Medium | Difficult above 3-levels | None | High |
| FC | Medium | Difficult above 4-levels | Yes | Extra High |
| CHB | High | Isolated DC-source | Possible | None |
| MMC | High | Obtainable | Yes | High, distributed |

One of the drawbacks of MMC topology is circulating current that causes power losses, increases stress on the devices and decrease the stability of the system. Circulating current has been studied in a lot of publications and several methods have been proposed to minimize circulating current in converter's phase leg (Sreedhar, Panigrahi, Kumar, & Das, 2015; Zhang, Huang, Yao, & Lu, 2014). Capacitor voltage balancing plays a vital role in the stability operation of MMC system and reduce the circulating current. Several control strategies were also proposed to improve the equal voltage sharing among SM capacitors (Adam et al., 2010; Deng & Chen, 2014; Goncalves, Rogers, & Liang, 2018; Liu, Jiang, & Wei, 2013).

There are a number of point failures that need to be considered in MMC converter system, such as DC-side short-short circuit, internal device fault, etc. Based on those failures, MMC has several submodules (SM) configuration that can withstand some certain faults. There are three major topologies that have been proposed so far, namely, the half-bridge (HB) SM, full-bridge (FB) SM and clamp double SM (Debnath et al., 2014). The configurations of the submodules are shown in Figure 2.7.

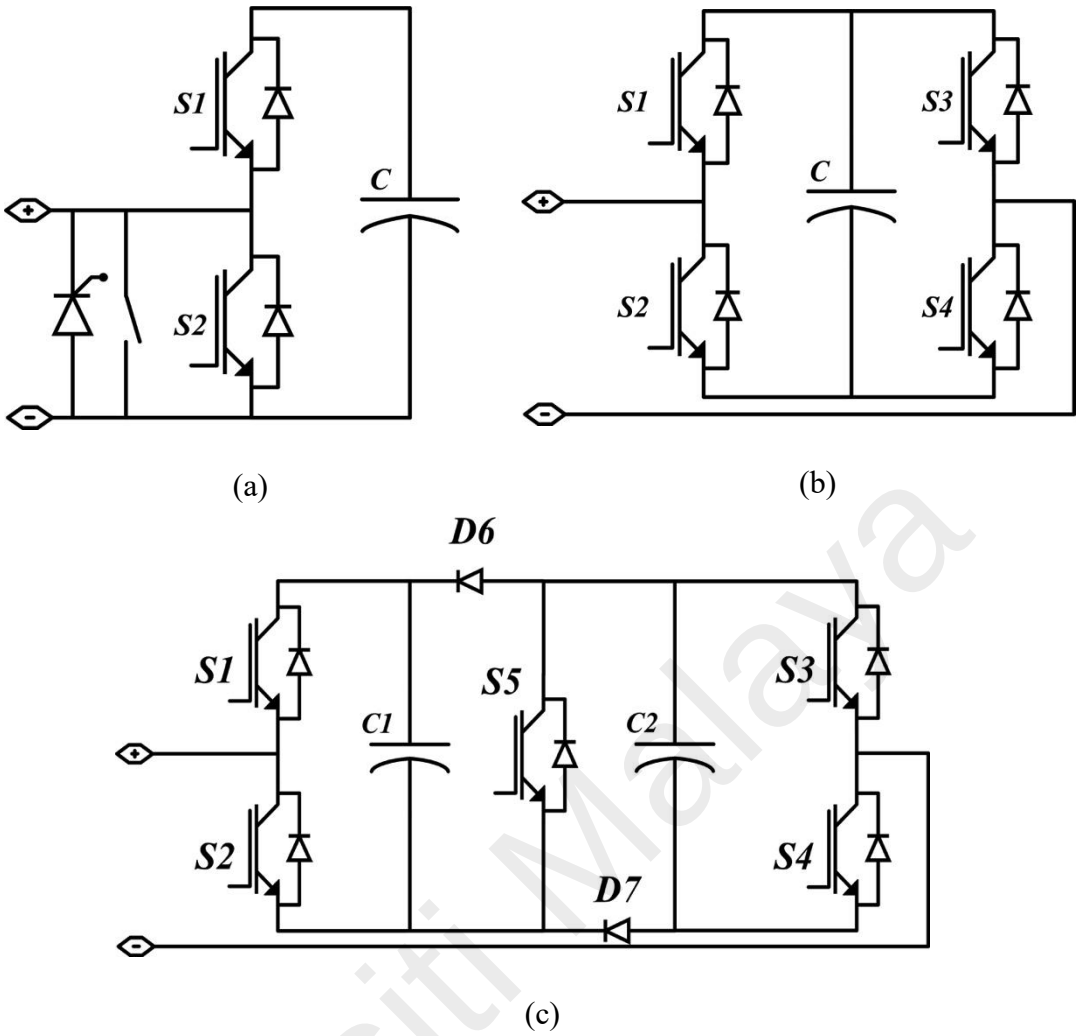



**Figure 2.7:** Various SM structure of MMC: (a) half-bridge (HB), (b) full-bridge (FB) and (c) double-clamped.

The MMC based on HB submodule has the lowest component number compared to other multilevel converter topologies used for HVDC application; however, it has the possibility of one output voltage polarity. In the MMC based on full-bridge (FB) submodule, the SM has more switches, but it does not have the same problem as HB SM configuration which is during DC-side short-circuit faults. The double-clamped submodule is also designed to block the DC-side short-circuit fault purposely. When DC-side fault occurs, the middle switch in double-clamped submodule is able to divide the arm current between two capacitors. However, these configurations require more components, need extra control points and increase the losses in the submodule (Qin et al., 2015). The modification of submodule keeps increasing in order to increase the

reliability of submodule to withstand some sort of failure and also increase the number of level in submodule by integrating the existing topology such as neutral point clamped (NPC) and flying capacitor (FC) as submodule in MMC topology, as shown in Figure 2.8. These type of topology may increase the level of the output voltage and bring better performance during the faults. In contrast, these topologies also increase the complexity in control structure. For example, FC-submodule needs extra control to charge the capacitors where each capacitor has different voltage level. Thus, the balancing structure of capacitor in each submodule also turns out difficult. Table 2.6 presents the advantages and disadvantages study from the standpoint of several submodule configuration.

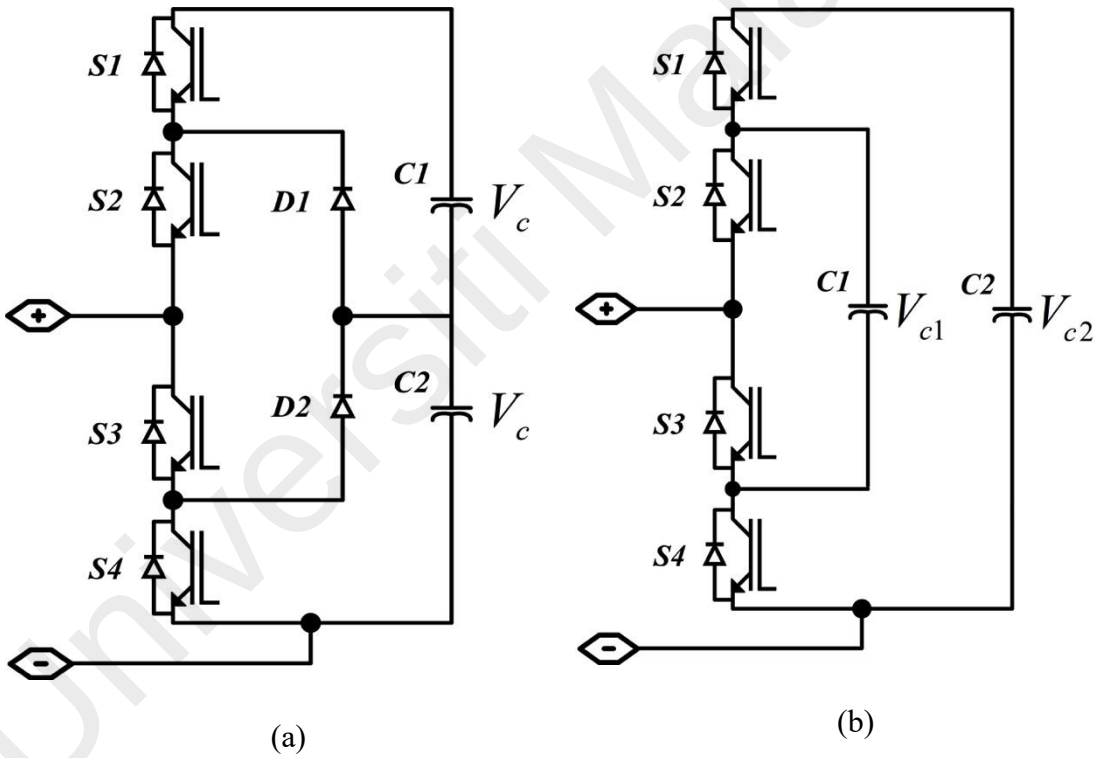



**Figure 2.8:** (a) NPC-submodule and (b) FC-submodule.

**Table 2.6: Comparison of submodule configuration.**

| No | Submodule (SM) Configuration | Advantange | Disadvantage |
|---|---|---|---|
| 1 | Half-Bridge (HB) SM | 1. The simplest SM configuration.<br>2. The simplest control configuration. | 1. There is no spare (back up) alternative to block DC-side fault<br>2. There is no spare (back up) alternative state if there is internal fault (device fault). |
| 2 | Full-Bridge (FB) SM, (Akagi, 2011) | 1. Provide unipolar state.<br>2. Provide ability to block fault current caused by DC-side fault.<br>3. Provide spare (back up) alternative state if there is internal fault (device fault). | 1. The conduction losses are higher than HB SM.<br>2. Require more switching devices.<br>3. Unipolar state in FB SM is not very useful in normal operation due to a reverse voltage polarity at the DC-bus is not required in the main operation |
| 3 | Double Clamped SM, (Qin et al., 2015) | 1. Facilitate DC-side fault blocking with less conduction losses.<br>2. There are two HB SM that seperated by a switch and two diode. | 1. Conduction loss is higher than HB SM, but better than FB SM.<br>2. Need to charge the voltage capacitor separately. |
| 4 | NPC SM, (Solas et al., 2013). | 1. Generate higher voltage level.<br>2. Provide spare (back up) alternative state if there is internal fault (device fault). | 1. Require more complex control.<br>2. Need to charge the voltage capacitor separately. |

| | | | |
|---|---|---|---|
| 5 | FC SM, (Solas et al., 2013). | 1. Generate higher voltage level.<br>2. Provide spare (back up) alternative state if there is internal fault (device fault). | 1. Require more complex control.<br>2. Need to charge the voltage capacitor separately. |

The modification of MMCs also occurrs in the arm structure or leg structure, as shown in Figure 2.9 in order to increase the MMC performance for a certain application. MMC with tansformer in the middle has an advantange to reduce voltage rating of power devices as well as reduce total DC bus magnitude and also diminish capacitor size (Nademi et al., 2016), as shown in Figure 2.9(a). In FC-MMC topology (Figure 2.9(b)), there is a floating capacitor in the between the upper and lower arm. This floating capacitor aims to reach the power balance and minimize the ripple of capacitor's voltage between the upper and lower arm for medium-voltage motor drive in the whole speed range, especially at low speed under valued torque condition (Du et al., 2017). The alternate arm converter as shown in Figure 2.9(c) consist of the multiple switches on each arm. These switches act as valves or director switches which have a function to control the current flow during DC-side faults (Merlin et al., 2014). As shown in Figure 2.9(b), when there is an internal device fault in the submodule, the spare or reserved submodules are inserted to replace the faulty SM. This type of configuration has an advantage due to the position that can serve both arms if needed. However, it will increase the volume of the converter and mechanical wiring in the converter (Farias et al., 2018a).

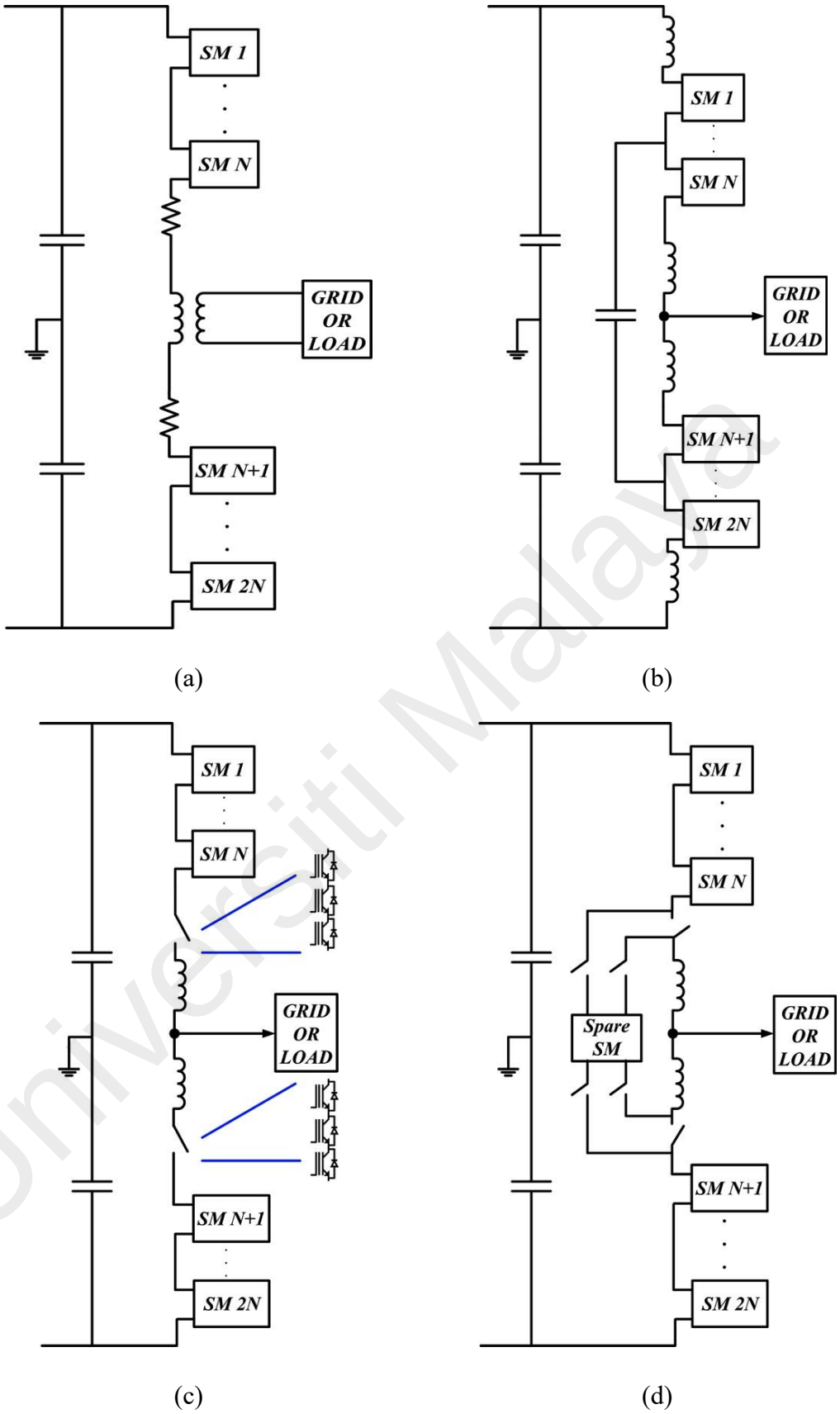



**Figure 2.9:** (a) MMC with transformer, (b) FC-MMC, (c) Alternate arm converter (AAC) and (d) MMC with spare submodule.

Growing number of MMC installations for high voltage applications shows the success and market acceptance of MMC converter. There are still a small number of publications focusing on performance improvement of MMC systems under internal fault (device fault) and fast penetration of MMC in high voltage application demands more researchs on the performance of this converter and detail studies of the operation and control system (Farias, Cupertino, Pereira, Junior, & Teodorescu, 2018).

## 2.3 Multilevel Voltage Source Converter Modulation Methods

Many modulation techniques have been proposed and presented according to the structure, design, and application of the multilevel converters. The multilevel converter control is classified based on the switching frequency such as high and low switching frequency, as shown in Figure 2.10. The multilevel converter topologies utilize the modulation control in order to achieve the desired target and output results. Furthermore, the modulation type is classified based on switching frequency where the low frequency indicates up to few multiples pulse generated and high-frequency range starts at 1 kHz.

Since multilevel converters can generate more voltage levels, they can be worked at much lower switching frequencies, and the switching losses in the switches will be considerably smaller. Another reason for an increased interest in these topologies is that they can implement controlled rotational movement in medium and high power applications to equalize device stresses (Latran & Teke, 2015).

Several modulation techniques are proposed for multilevel converters, which can be classified into two categories based on the switching frequency. The carrier-based pulse width modulation (CBPWM) techniques operate at higher switching frequencies and achieve higher output quality at the cost of increased switching losses (McGrath & Holmes, 2002). The fundamental frequency modulations techniques, on the other hand, have lower switching losses but the decreased number of produced voltage levels criteria

due to high complexity calculation for higher number generated (McGrath et al., 2003; Memon et al., 2018). Space-vector modulation (SVM), nearest level modulation (NLM), and selective harmonic elimination (SHE) are among the well-known low switching modulation or fundamental switching frequency modulation techniques.

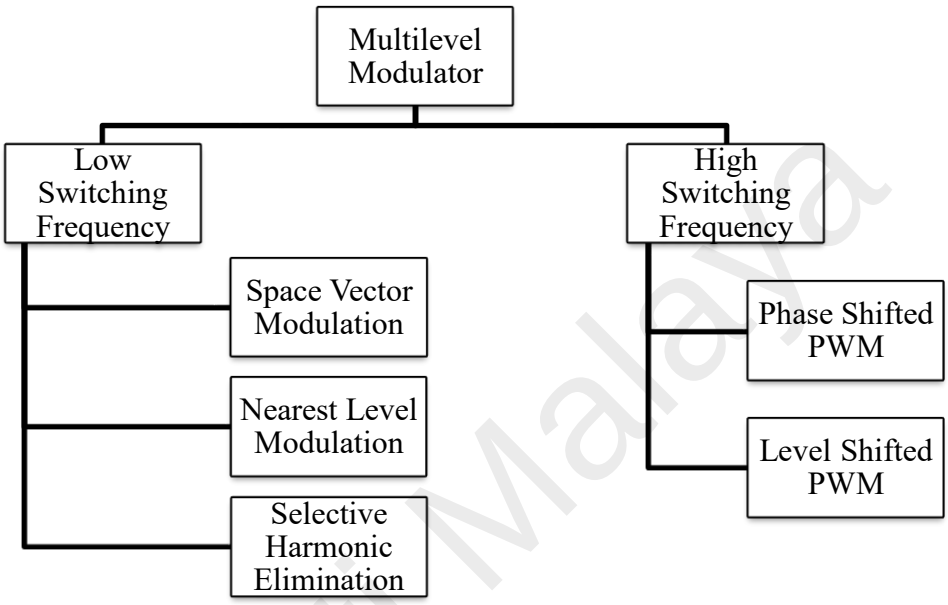



**Figure 2.10:** Classification of multilevel modulation methods.

### 2.3.1 Carrier-Based Sinusoidal Pulse Width Modulation

Carrier-based sinusoidal PWM (CBS-PWM) is a prevalent method in industrial applications for high switching frequency. In carrier-based modulation techniques, each generated level in a phase requires a carrier, so each group of switches has its own carrier waveform, which is compared to the reference waveform and the intersections defining the switching pulses (McGrath & Holmes, 2002). The carriers of the first module changes from 0 to $V_{dc}$, the second module changed between $V_{dc}$ and $2V_{dc}$ and the range increases to $(m-1)V_{dc}$ to $mV_{dc}$ for last units to cover the whole voltage range. The carriers are re-arranged for the negative side in the opposite order and there can be a phase shift between carriers. Generally, The carrier based modulation techniques are divided into two categories: the phase-shifted pulse width modulation (PS-PWM) and level-shifted

pulse modulation (LS-PWM). LS-PWM have several categories, which differ by allocation of carrier with respect to each other.

#### 2.3.1.1 Level Shifted PWM (LS-PWM)

The use of level shifted LS-PWM needs $(n-1)$ triangular carrier waves. All carriers have the same frequency and amplitude range. The $(n-1)$ triangular carrier is arranged in vertical shifts and each carrier wave is set between two voltage levels (Jeevananthan et al., 2006) as shown in Figure 2.11. The frequency modulation index $(m_f)$ of each carrier remains the same, while the amplitude is allocated vertically to cover whole voltage range. The amplitude index $(m_a)$ is given in equation 2.1:

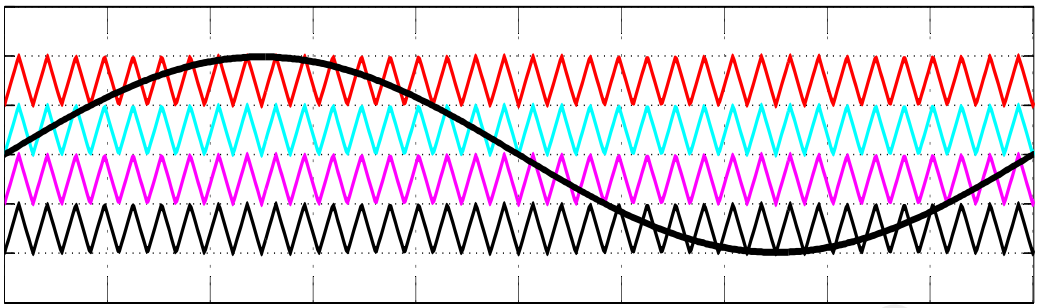
$$m_a = \frac{A_m}{(n-1)A_c} \tag{2.1}$$

Where, $A_m$ is amplitude modulation and $A_c$ is amplitude carrier.

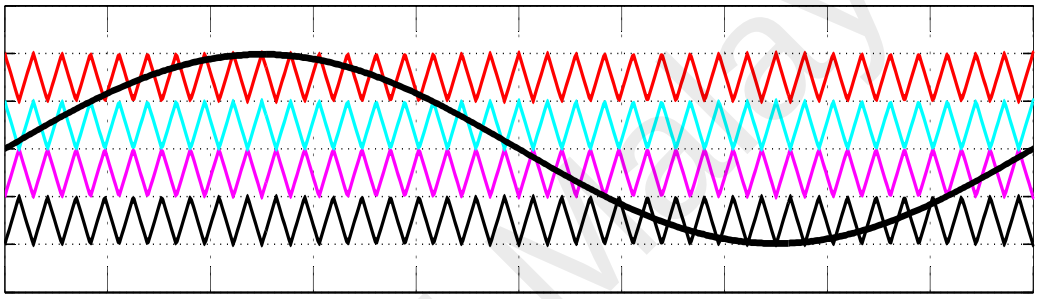
LS-PWM modulations can be performed in 3 (three) models, which are phase disposition PWM (PD-PWM), phase opposition disposition PWM (POD-PWM), and alternate phase opposition disposition PWM (APOD-PWM). As part of LS-PWM modulation, all those models have carriers which all the carriers are re-arranged vertically and distinguished by the phase of carriers. PD-PWM has all the carriers waveform in the same phase as shown in Figure 2.11(a). POD-PWM has all positive carrier waveforms in the same phase, but the negative carrier waveforms have the opposite phase from the positive one, as shown Figure 2.11(b). Then, the waveform of a carrier is phase-shifted by 180$^o$ from the waveform of the next carrier for APOD-PWM, as shown in Figure 2.11(c).

The level-shifted PWM leads into unequal loading of modules in some applications. Therefore, the DC-link capacitors of the modules are loaded differently, which cause the

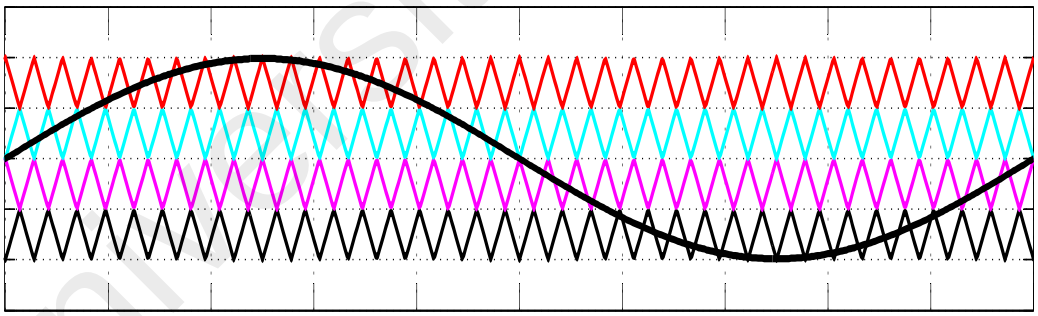
voltage of the capacitor unbalance problem in topologies such as MMC because the first module will absorb most of the energy flowing back from the load (Angulo et al., 2007).



(a)



(b)



(c)

**Figure 2.11:** Level shifted pulse width modulation waveform; (a) phase disposition PWM (PDPWM), (b) phase opposition disposition PWM (PODPWM) and (c) alternate phase opposition disposition PWM (APODPWM)

#### 2.3.1.2 Phase-shifted Pulse Width Modulation

Phase Shifted PWM technique is also a popular technique of scalar PWM technique. A multilevel converter using PS-PWM requires multiple carriers to generate the switching signals. It employs phase-shifted carrier to distribute the switching angles

among sub-waveform and reduce the frequency of each component. This multiple carriers spread throughout a time-period that corresponds to the switching cycle (X. Liu et al., 2014; McGrath & Holmes, 2002). A number of carriers required for a multilevel converter is the same as the number of level in the output voltage where 10-level converter requires 10 carriers. The phase shift (∅) between any two adjacent carrier signals is calculated in equation 2.2. Figure 2.12 shows the basic principle of the phase-shifted PWM modulation technique.

$$\emptyset = \frac{360^0}{n-1} \tag{2.2}$$

Where $n-1$ is the number of carrier.

Thus, the time interval ($T_d$) between the carrier signals is expressed in equation 2.3.

$$T_d = \frac{1}{nf_{SW}} \tag{2.3}$$

Where $f_{SW}$ is the switching frequency of the carrier signals.

The relationship between peak amplitudes of modulation and carrier waves can be expressed in equation 2.4.

$$m_a = \frac{A_m}{A_c} \; and \; m_a \; \epsilon \; [0,1] \tag{2.4}$$

While the relationship between frequency modulation and carrier waves can be expressed in equation 2.5.

$$m_f = \frac{f_c}{f} \tag{2.5}$$

$f$ and $f_c$ are the frequency of modulation and carrier waves, respectively.

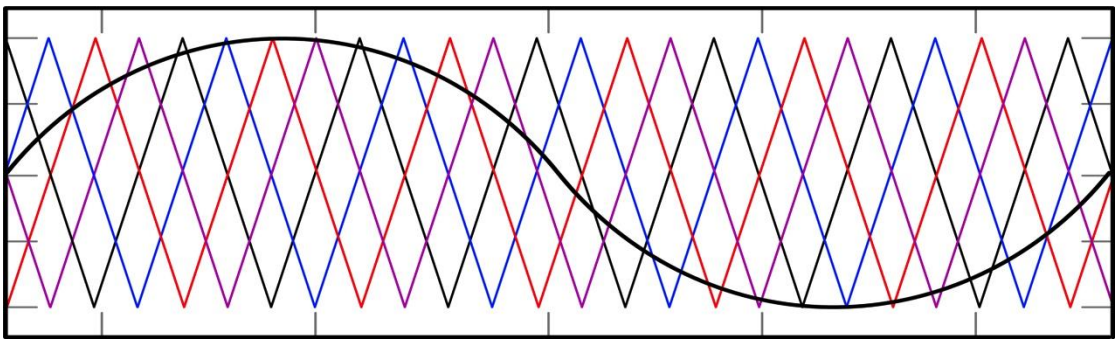


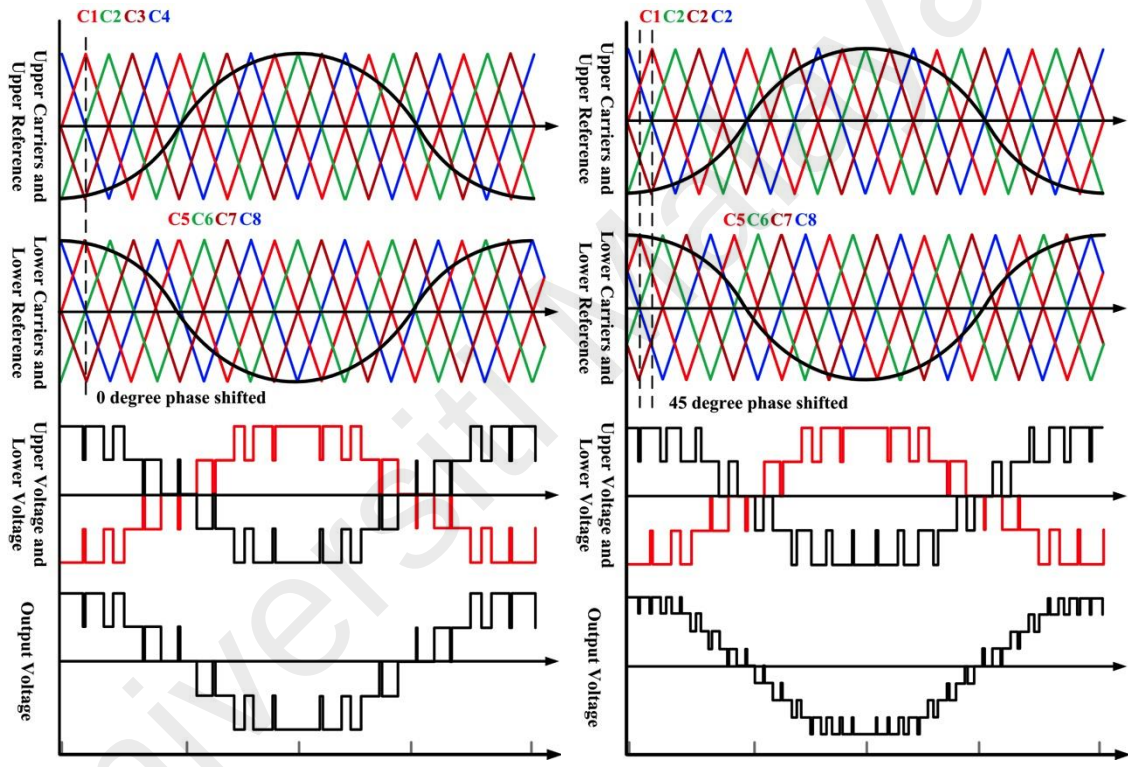
**Figure 2.12:** Phase-shifted pulse width modulation (PSPWM) waveform.

PS-PWM technique can solve the load-sharing problem that created by LS-PWM. Thus, the phase-shifted PWM technique is recognized for producing a load voltage with smaller distortion for multilevel inverters implemented using cascaded cells such as CHB converter. For MMC, the phase of carriers for each submodule ($N$) is shifted by angle of $\emptyset = 360/N$. The carriers are usually allocated using two approaches to produce the different level either $2N + 1$ or $N + 1$ level. In the even number of SM as shown in Figure 2.13, the first approach uses the same shifted angle between upper and lower carriers to produce $N + 1$ level at the output side. The second method uses different shifted angle at each of carrier for upper and lower arm that can be expressed in equation 2.6. For that reason, the upper voltage and lower voltage have independent pulses to produce $2N + 1$ level. However, it needs multiple carriers with different angles for all the SMs in the leg that can increase the computational burden in the controller (Liu et al., 2014).

$$C_1 = y_c(\omega_c, 0);\ C_2 = y_c(\omega_c, \pi/2);\ C_3 = y_c(\omega_c, \pi);\ C_4 = y_c(\omega_c, 3\pi/2)$$
$$C_5 = y_c(\omega_c, \pi/4);\ C_6 = y_c(\omega_c, 3\pi/4);\ C_7 = y_c(\omega_c, 5\pi/4);\ C_8 = y_c(\omega_c, 7\pi/4) \quad (2.6)$$

In PS-PWM, the SM capacitor is well balanced by using individual balancing algorithm (not centralized algorithm) with a PI controller at each SM (Hagiwara & Akagi, 2009; Konstantinou & Agelidis, 2009). Therefore, the PS-PWM distributes an equal amount of power between the SMs, resulting in the inner current control and voltage

balance to the capacitor at a satisfactory level. PS-PWM has better load sharing and output quality at the price of increased switching losses (Darus et al., 2014). It is caused by PS-PWM for MMC converters use one carrier for each submodule in the MMC and these carrier waveforms have the same amplitude and frequency which are shifted by angle (delta) depending on the number of SMs in the arm. However, this method cannot obtain the closest level PWM, which results in worse harmonic performance compared to the PDPWM strategy at the output voltage.




(a) (b)

**Figure 2.13:** Carrier PS-PWM for MMC when $\boldsymbol{N = 4}$ (even number); (a) $\boldsymbol{N + 1}$, (b) $\boldsymbol{2N + 1}$.

### 2.3.2 Space Vector Modulation (SVM)

Space vector modulation (SVM) is a modulation technique that calculates the average duty cycle of switches in linear operating region diagram to synthesize a desired output voltage. SVM is firstly applied for conventional two-level converter which has 8 possible switching states. SVM technique can be expanded to more than three-level with

appropriate modifications, thus it can be used for multilevel converters (Deng, Wang, Teo, Saeedifard, & Harley, 2018; McGrath et al., 2003). SVM has been applied for all type of multilevel topologies including MMC. The output voltages ($V_{abc0}$) can be defined by an algebraic way that consists of switching states and voltage of DC source ($V_j$) is described in equation 2.7 until equation 2.9.

$$V_{abc0} = H_{abc} V_j \tag{2.7}$$

$$V_j = [V_{j1}\ V_{j2}\ V_{j3}\ \cdots V_{jn}],\ V_{abc0} = \begin{bmatrix} V_{a0} \\ V_{b0} \\ V_{c0} \end{bmatrix},\ H = \begin{pmatrix} H_{a1} & \cdots & H_{an} \\ \vdots & \ddots & \vdots \\ H_{c1} & \cdots & H_{cn} \end{pmatrix} \tag{2.8}$$

The elements of the above array are given in equation 2.9.

$$H_{aj} = \sum_{i}^{m} \delta(h_a - j) \tag{2.9}$$

For $m = n - 1$, where $n$ is the number of voltage level produced by multilevel converter. $h_a$ is the switching state, it is an integer from 0 to $m$, and $\delta(x)$ is defined in equation 2.10.

$$\delta(x) = 1, if\ x \geq 0$$
$$\delta(x) = 0, if\ x < 0 \tag{2.10}$$

As mentioned before, SVM can produce some possible switch combinations. Therefore, some particular output voltages can be generated by more than one switching combinations. In an *n*-level neutral point clamped (NPC) converter, the number of switching combinations for an output voltage state $(x, y, z)$ is given by $n - 1 - max(x, y, z)$. Then, the number of possible switching state for zero states is the same as the number of levels $(n)$. For example, a three-level NPC converter, the zero voltage states

that it generated are $(0, 0, 0)$, $(1, 1, 1)$, and $(2, 2, 2)$. The total number of possible switch combinations can be found by the cube of the level ($n^3$). The illustration of SVM in linear operating region diagram for 3-level is shown in Figure 2.14. There are *27* possible switching states for the three-level multilevel converter. The number of distinct or unique states for an *n*-level converter is given in equation 2.11.

$$n^3 - (n-1)^3 = \left[6 \sum_{n-1}^{m-1} n\right] + 1 \qquad 2.11$$

Therefore, the SVM can provide remarkable flexibility in selecting redundant vectors to optimize switching waveforms that can generate less THD. However, increasing the voltage level will expand the linear operating region diagram as the result in a complex calculation algorithm.

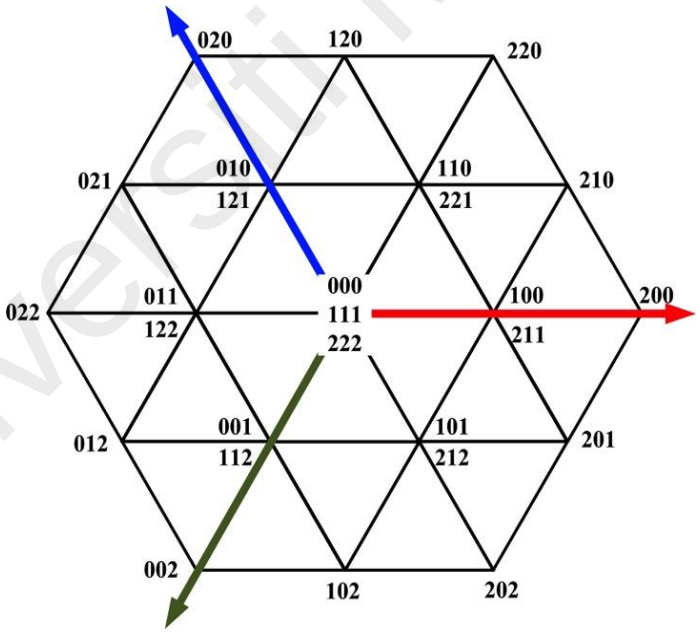



**Figure 2.14:** Space vector modulation (SVM) linear operating region diagram for 3-level.

### 2.3.3 Selective Harmonic Elimination PWM (SHE-PWM)

The concept of selective harmonic elimination (SHE) emerged in the multilevel power converter to reduce the switching losses and increase the overall efficiency of the

converter while eliminating low-order harmonics. SHE is a method to generate PWM with low baseband distortion and has initially been more successful in low switching frequency applications. Conventional PWM eliminates baseband harmonics for frequency ratios of $10:1$ or higher but SHE has recently received attention because the digital implementation has become more frequent and there have been many solutions to SHE that was previously unknown. SHE is usually a two-step digital process where first is the offline calculation of the switching angles and second is storing angels in a look-up table to be read in real-time (Memon et al., 2018).

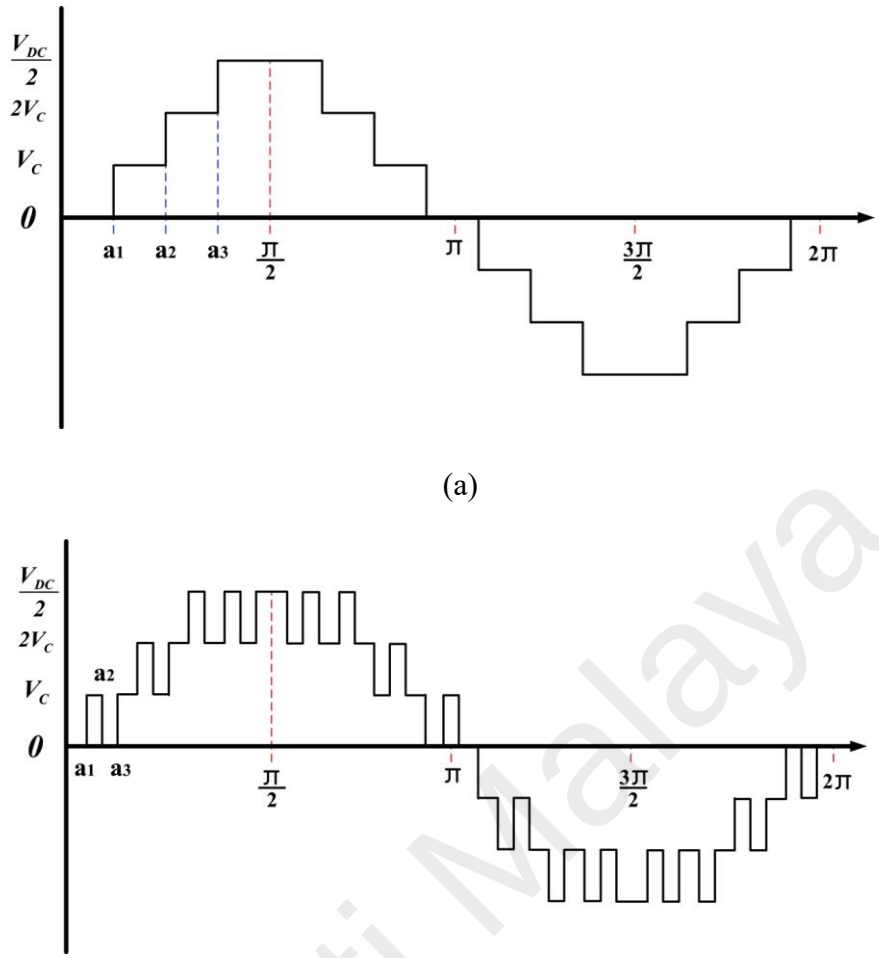
SHE works by calculating the Fourier transformation for a stepped waveform consisting of steps given in equation 2.12. The switching angles calculated by using digital process will be used to decide the switching pattern, as shown in Figure 2.15.

$$V(\omega t) = \frac{4V_{DC}}{\pi} \sum_{n} [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)] \frac{\sin(n\omega t)}{n} \quad 2.12$$

$$where\ n = 1, 3, 5, 7, \cdots$$

and $\theta_1$ to $\theta_s$ are to satify the condition that $\theta_1 < \theta_2 < \cdots < \theta_s < \pi/2$.

Generally, these angles are found either in online or offline calculation to eliminate harmonics at predominant low frequency, such as 3rd-order, 5th-order and 7th-order harmonic. Mostly, the amplitudes of all even harmonics are zero at three-phase. Application of SHE in MMCs is a new trend and applied in some journals (Konstantinou et al., 2013) and (Pérez-Basante et al., 2018). However, The SM capacitor voltage balancing is the main issue in MMC by using SHE and also increasing the voltage level will result in a complex calculation.




(a)




(b)

**Figure 2.15:** Staircase output voltage waveform using SHE based on; (a) single switching per level SHE and (b) multiple switching per level.

### 2.3.4 Nearest Level Modulation (NLM)

One of the most popular modulation techniques for MMC with large number of SMs is nearest level modulation (NLM). NLM technique works by dividing the reference voltage by individual submodule voltage and generating the closest integer to the real number (Moranchel et al., 2015; Tu & Xu, 2011), as shown in Figure 2.16. Equations 2.13, 2.14, 2.15 and 2.16 showthe total number of submodules in MMC arm, the AC reference voltage and a number of calculated submodules by NLM upper and lower arm.

$$V_c = \frac{V_{DC}}{N} \qquad 2.13$$

$$V_{ej}^{ref} = \frac{1}{2} m V_{DC} \cos(\omega t + \varphi_j) \quad 2.14$$

$$N_{jupper} = round(\frac{0.5V_{DC} - V_{ej}^{ref}}{V_c^{ref}}) \quad 2.15$$

$$N_{jlower} = round(\frac{0.5V_{DC} + V_{ej}^{ref}}{V_c^{ref}}) \quad 2.16$$

The total number of submodules inserted in each phase is constant and defined by equation 2.17.

$$N_j = N_{jupper} + N_{jlower} \quad 2.17$$

NLM is also one of simple modulation techniques used pratically in multilevel converter. However, NLM technique is suitable to the MMC, which have a large number of SMs due to small voltage steps. This means if it is used with small scale MMC which means a low number of switching may cause more considerable voltage fluctuation in the capacitor voltages. It needs a high capacitance value to reduce sorting issues and bringimplementation complexity.

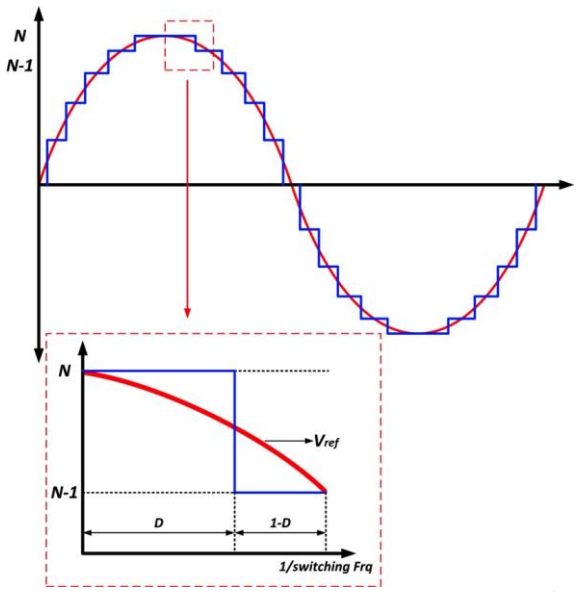



**Figure 2.16:** Nearest level modulation operating principle.

### 2.3.5 Comparison of modulation technique

The overview of modulation techniques applied in the multilevel converter, especially on MMC, has been discussed above. The comparison among those techniques is summarized in the Table 2.7.

**Table 2.7 Comparison of modulation techniques for MMC.**

| No | Control Scheme | Advantages | Disadvantages |
|---|---|---|---|
| 1. | LSPWM; (Jeevananthan et al., 2006) | 1. The simplest modulation method.<br>2. Easy to implement pratically.<br>3. Obtain the closest level PWM, which results in better harmonic performance compared to PSPWM. | 1. Need to generate and arrange the multiple carriers on the top of each other with the specified amplitude range.<br>2. More voltage levels being used will increase the number of carrier and require higher controller specifications.<br>3. Unequal power delivered to the submodules. |

| | | | |
|---|---|---|---|
| 2. | PSPWM; (X. Liu et al., 2014; McGrath & Holmes, 2002). | 1. The simplest modulation method.<br>2. Easy to implement pratically.<br>3. Distribute an equal amount of power between the SMs.<br>4. More suitable cascaded topology, such as CHB and MMC topolgy | 1. Need to generate and arrange the multiple carriers with difference phases of each other in the same amplitude range.<br>2. More voltage levels being used will increase the number of carrier and require higher controller specifications. |
| 3. | SVM; (Y. Deng et al., 2018; McGrath et al., 2003) | 1. Provide redundant switching state that may reduce the percentage of THD. | 1. Need complex mathematical algorithm to setup the diagram. Higher level will increase the complexity. |
| 4. | SHE; (Konstantinou et al., 2013) and | 1. Provide ability to eliminate the higher order harmonics, which results in the best harmonic performance compared to the other methods. | 1. Require complex calculation and algorithm. |
| 5. | NLM; (Moranchel et al., 2015; Tu & Xu, 2011) | 1. Simple modulation method.<br>2. Easy to implement pratically. | 1. Small scale MMC with low number of SMs may cause voltage fluctuation in the capacitor voltages. So, It needs a high capacitance value to reduce voltage flactuation. |

## 2.4 Fault Location in MMC

The power flowing from the converter to the load system should be able to balance over time to make sure the reliability of the converter. Some faults may occur in the system either from the internal or external disturbance. MMCs have modularity or hierarchy structure that have potentiality in managing the failure. Figure 2.17 summarized

in Table 2.8 shows SM and converter level fault mappings. In SM level, faults which are related with IGBTs such as open / short circuit and intermittent gate misfiring faults are showed as one of the most common fault types which may disrupt the operation of MMC and also destroy the device due to the effect on current and voltage.

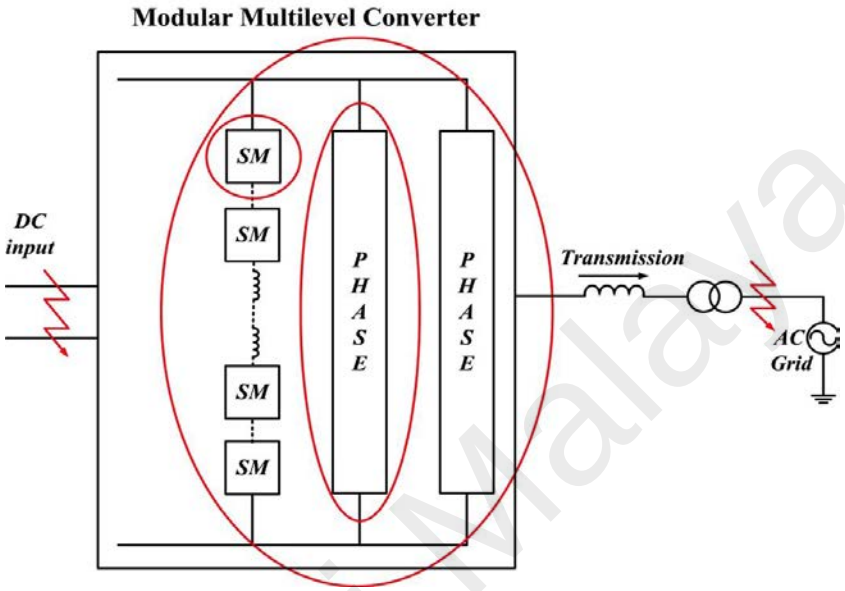



**Figure 2.17:** Possible fault locations in MMC system.

**Table 2.8: Fault locations in MMC system.**

| Level | | Fault Types |
|---|---|---|
| Submodule | IGBT | Open / short circuit fault |
| | | Discontinuous gate misfiring fault |
| | Diode | Open diode fault |
| | | Short circuit fault |
| | Capacitor | Capacitor structure fault |
| Converter | | Unbalance between upper and lower arm voltage |
| | | Single-phase to ground fault |
| | | Double-phase to ground fault |
| | | Three-phase to ground fault |

| | | |
|---|---|---|
| System level | AC side | AC grid voltage unbalance |
| | | Open / short circuit fault |
| | DC-side | Open / short circuit fault |

MMCs require considerable SMs for increasing voltage levels. Therefore, some faults can occur internally within an SM. Several studies are available for diagnosis and tolerance switching device faults. If a faulty SM exists, the converter will be able to detect and continue power delivery to guarantee converter reliability. The unbalanced SM voltages of arms and loss of some parts of the voltage level occur during SM failure. The unbalanced SM voltages can be done by short-circuiting the faulty SM. This strategy can be achieved by inserting a bidirectional thyristor to the SM device parallelly, which is used to bypass the SM during normal or fault operation (Deng et al., 2016). Therefore, the current flows without any disturbance through the series-connected SMs in the arm. It will stay bypassed until the next planned maintenance occasion even during a faulty SM is short-circuited.

Some of the multilevel converter provide a redundant switching state allowing the converter to carry on normal operation under internal fault (device fault) conditions. The simple circuit configuration of half-bridge SMs has a limited redundancy switching. Generally, the half-bridge MMC needs to include redundant SMs to abolish the drawback of half-bridge SM. When a switching device fails, the faulty SM including the faulty switching device is bypassed and the reserved SM is inserted to replace the faulty SM. In (Deng et al., 2018; Zhou et al., 2014), the authors suggested that redundant SMs should be considered even during normal operations.

A few SM redundancy strategies have been proposed in (Ahmed et al., 2015; Choi et al., 2016; Hu et al., 2019; D. H. Kim et al., 2015; Gaoren Liu et al., 2015; Saad et al., 2015). All these types have been categorized into four strategies, specifically standard

redundancy (SR), redundancy additional submodule (RAS), redundancy additional submodule optimized (RASO) and redundancy based on spare submodule (Farias et al., 2018). Most of these strategies use PS-PWM. In this technique, each of SM needs carrier wave, which is phase-shifted from the other SM carriers. In (Kim et al., 2015; Gaoren Liu et al., 2015), the NLM technique to control the converter was used, which creates high fluctuation on capacitors voltage. The authors in (S. Kim et al., 2018) presented a fault tolerance by injecting a zero-sequence offset voltage to change the reference signals. However, this strategy decreases the power quality and increases the THD of the phase voltage. Table 2.9 presents a comparison study from the standpoint of several fault-tolerants based on SM failure.

**Table 2.9: Comparison of fault-tolerant methods.**

| No | Control Scheme | Advantage | Disadvantage |
|---|---|---|---|
| 1. | PSPMW; Proposed by (Choi et al., 2016; Farias et al., 2018a) | This method uses conventional PS-PWM technique and does not use a spare or back up SM. In other words, all the SMs should be able to withstand the fault with a certain percentage limit (the rating of components). It gives good performance and fast response. | This method removes one level. In term of cost, this method is more suitable for large number of SMs. |
| 2. | NLM; Proposed by (D. H. Kim et al., 2015; Gaoren Liu et al., 2015) | This method uses NLM technique and uses a spare or back up SM. In other words, there is a standby SM if the fault occurs. It gives good performance and keeps the number of level. | In term of cost, this method requires more cost and increases the volume of converter. Then, the response will take some times to charge the voltage capacitor of the spare SM. |

| | | | |
|---|---|---|---|
| 3. | PSPWM; Proposed by (S. Kim et al., 2018) | This method modifies the waveform of the reference signal by giving zero-sequence offset voltage. All the capacitor voltages remain the same. Thus, it does not use a spare or back up SM and does not need to consider the rating of components to whistand the fault. | All the capacitor voltages remain the same but it cuts the portion of the voltage level. This method creates higher THD in the phase output voltage. |

## 2.5 Summary

This chapter presents a comprehensive review of the multilevel converters along with their modulation techniques. The discussion starts with the basic concept of multilevel converters and its classification. Then, the well-known converter topologies such as neutral point clamped multilevel converter, flying capacitors multilevel converter and cascaded H-bridge multilevel inverters are reviewed. The detailed modulation applicable for multilevel converters is presented and classified into several categories. For MMCs, there are several submodule configurations that have been proposed, such as full-bridge submodule, double-clamped submodule, NPC submodule and FC submodule. The structure of arms or leg of MMC is also modified such as alternate arm converter MMC, spare submodule and flying capacitor MMC. Those modifications have superiority to increase the output voltage and to avoid the failure, either external or internal fault. However it may increase component demand as well as control complexity.

# CHAPTER 3: MATHEMATICAL MODEL AND CONTROL STRUCTURE

## 3.1 Introduction

The aim of this chapter is to derive the models of the modular multilevel converter (MMC) topology. First, this is done by deriving the mathematical model of the converter. Then, the mathematical model is analyzed by focusing on a specific part that relates to the criteria of the MMC control. The findings are validated either through simulation and experimental in Chapter 5.

## 3.2 Working Principle and Mathematical Derivation of MMC

The basic understanding of operating principle of converter is an essential step in order to define the dimensioning factors and features of MMC. The schematic topology of three phases leg of MMC is shown in Figure 3.1. In inverter mode, the DC power supply acts as the input at DC terminal, which is connected between the phase leg consisting of two arms, namely upper arm and lower arm. The AC terminal is positioned at the midpoint between the two arms as the output. Each arm is composed by one inductor ($L$) and SM ($N$) series, which consist of two switches with half-bridge configuration and parallel with single DC capacitor. Each arm is composed by a resistive losses which is modeled as an equivalent resistor inside arm inductors. The arm inductors are necessary to bound the current at the voltage steps and are also used for an internal current filter.

As part of the multilevel converter, MMCs have superior advantages compared to the conventional two-level converter, specifically low switching frequency, low stress voltage stepwise change of time ($dV/dt$) in the switch and higher efficiency. MMCs have a simple mechanical construction that allows increasing the number of levels easily compared to the other NPC and FC converter. The floating capacitors on the leg of converter need to be monitored to reach the balancing of SM capacitors' voltage. CHB converters need multiple separate DC supply, while MMCs need only single DC power

supply. The multiple of floating capacitor and modularity structure can provide failure management ability in MMC topology which is the main strengths of the MMC.

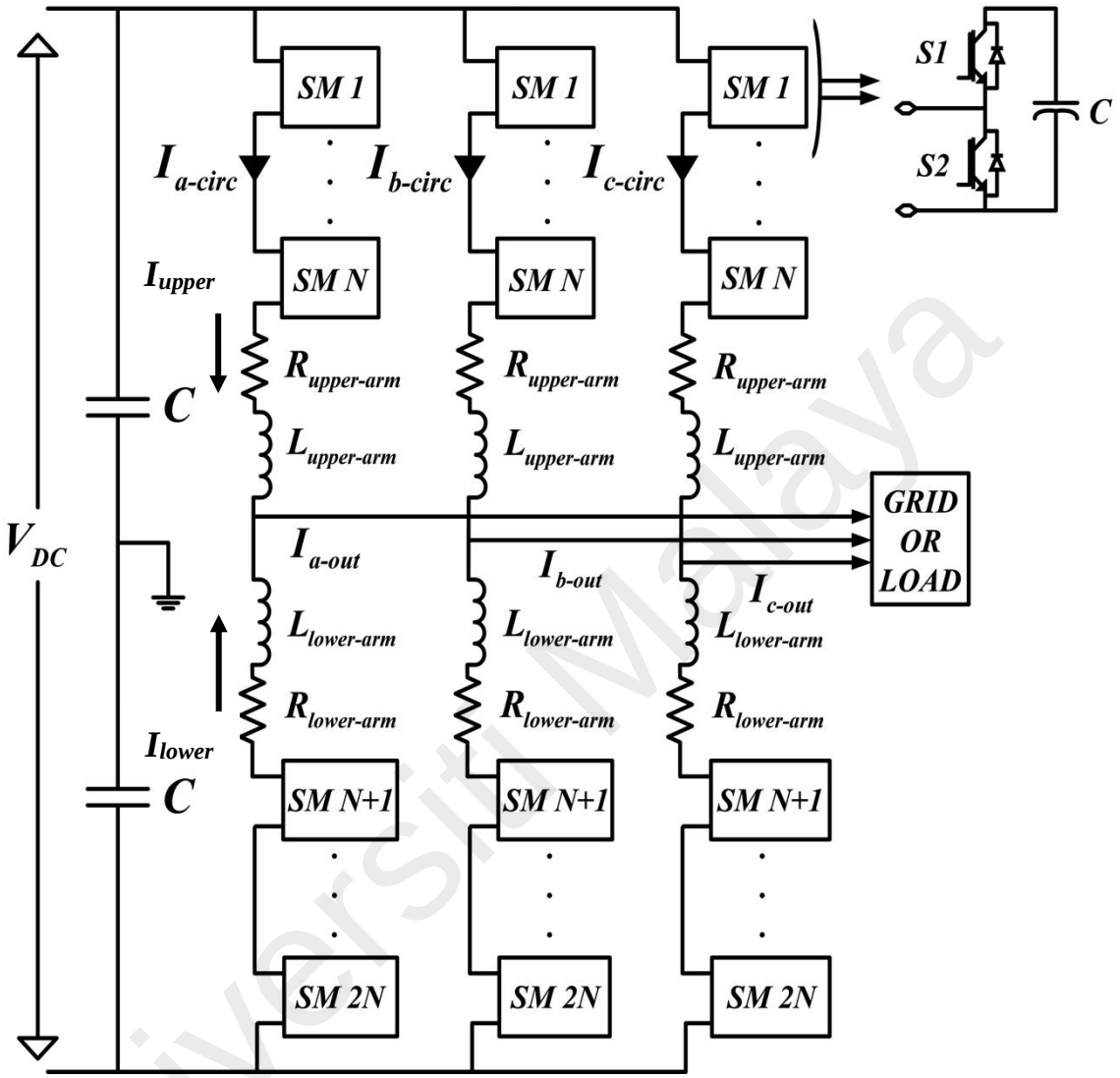



**Figure 3.1:** Schematic of three-phase MMC.

The sum of common-mode component or also known as circulating current ($I_{circ}$) and differential mode component express the arm current or called as upper ($I_{upper}$) and lower ($I_{lower}$) arm current. The circulating current ($I_{circ}$) flows between the DC terminals, while the differential mode component flows to the AC terminal, as shown in Figure 3.2. The upper ($I_{upper}$) and lower arm currents ($I_{lower}$) can be expressed by using Kirchoff Current Law (KCL) as expressed in equation 3.1 and equation 3.2.

$$I_{upper} = I_{circ} + I_{diff} \quad 3.1$$

$$I_{lower} = I_{circ} - I_{diff} \quad 3.2$$

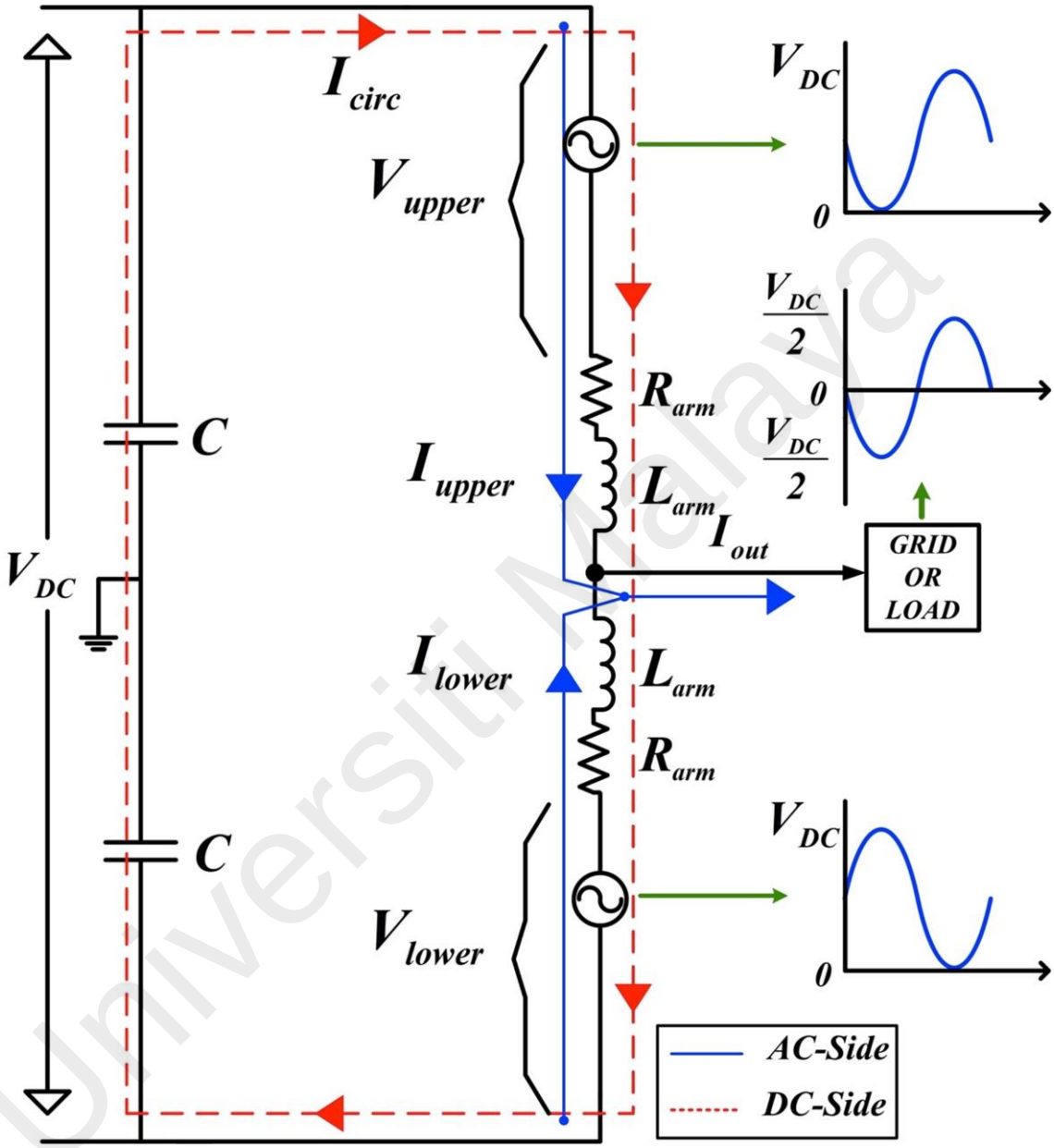



**Figure 3.2:** AC and DC current flow within a leg of MMC.

$I_{circ}$ is the circulating current component and $I_{diff}$ is the differential mode component that have half of the AC-side current. The circulating current can have some numbers of harmonic components as expressed in equation 3.3. In the ideal operation, the circulating current ($I_{circ}$) must have pure DC current ($I_{DC}$) in order to reach good quality active power

transfer. The differential mode component is presented as the half of the AC terminal current output as expressed in equation 3.4.

$$I_{circ} = I_{DC} + \sum_{n=2}^{\infty} I \tag{3.3}$$

$$I_{diff} = \frac{1}{2} I_{out} \tag{3.4}$$

$I_n$ is the $n^{th}$ order-harmonic in the circulating current composing second-order harmonic, while $I_{out}$ is the AC-side current. The total of the input power must be the same as the total of the output power if the converter is assumed to be no losses. It can be formulized in equation 3.5.

$$V_{DC} I_{DC} = \frac{V_{out} I_{out}}{2} \cos(\theta) \tag{3.5}$$

$V_{DC}$ and $I_{DC}$ are the DC voltage and DC curent input, respectively. $V_{out}$ is the amplitude of the AC voltage, $I_{out}$ is the amplitude of the AC current, and $\theta$ is the power factor angle. Relationship amplitude of DC input voltage and AC voltage could be derived in equation 3.6.

$$m = \frac{2V_{out}}{V_{DC}} \tag{3.6}$$

From the expression in equation 3.6 where $m$ is the modulation index, the relationship between DC–side current and AC–side current can be formed in equation 3.7.

$$I_{DC} = \frac{I_{out}}{4} m * \cos(\theta) \tag{3.7}$$

Since the capacitors should perform as voltage sources that can be inserted and bypassed in the series-connected submodule (SM), the control system of the converter

should be able to control the voltages across the SM capacitors that is maintained nearly constant and balance among them. Subsequently, each arm can produce a voltage of $N+1$ level. The level of voltage generated in chain of series connected SMs is indicated to as inserted voltage. In this way, the AC voltage at each arm with half of DC-offset will generate pure alternating voltage at AC terminal. Depending on how the converter is controlled, the number of output voltage levels in the AC terminal can be either $N+1$ or $2N+1$.

Assuming that SM capacitors' voltage in each arm is constant and ideal, the average of the upper and lower arm voltage are in sinusoidal waveform with respecting to time. The average duty ratio in each arm voltage is indicated as the insertion index. Accordingly, equation 3.8 and 3.9 express the insertion index of $N_{lower}$ and $N_{upper}$ for the lower and upper arms, respectively.

$$N_{upper} = \frac{1 - m\,cos(\omega_1 t)}{2} \tag{3.8}$$

$$N_{lower} = \frac{1 + m\,cos(\omega_1 t)}{2} \tag{3.9}$$

The MMC scheme can be simplified into AC and DC-sides. The output AC voltage is the difference between the lower and upper arm voltages. The operation principle of the MMC is to control the upper and lower arm voltages of the sinusoidal with a DC offset up to a half of the DC-link voltage with an antiphase of 180°. In this way, the DC-side voltage controls the AC side phase voltage as a sinusoidal with the magnitude of up to half of the DC-link. Based on Kirchhoff's Voltage Law (KVL), the output voltage ($V_{out}$) can be expressed in equation 3.10 and equation 3.11.

$$V_{out} = \frac{V_{DC}}{2} - L_{arm}\frac{dI_{upper}}{dt} - R_{arm}I_{upper} - V_{upper} \quad 3.10$$

$$V_{out} = -\frac{V_{DC}}{2} + L_{arm}\frac{dI_{lower}}{dt} + R_{arm}I_{lower} + V_{lower} \quad 3.11$$

Refering to Kirchhoff's Current Law (KCL), AC current can be found and stated in equation 3.12.

$$I_{out} = I_{upper} - I_{lower} \quad 3.12$$

The output voltage can be expressed by adding equation 3.10 into equation 3.11, thus the mathematical AC model can be shown in equation 3.13.

$$V_{out} = \frac{(V_{lower} - V_{upper})}{2} - \frac{L_{arm}}{2}\frac{dI_{out}}{dt} - \frac{R_{arm}}{2}I_{out} \quad 3.13$$

The equivalent circuit of the AC side is shown in Figure 3.3, where $L_{arm} = L_{upper} = L_{lower}$ and $R_{arm} = R_{upper} = R_{lower}$.

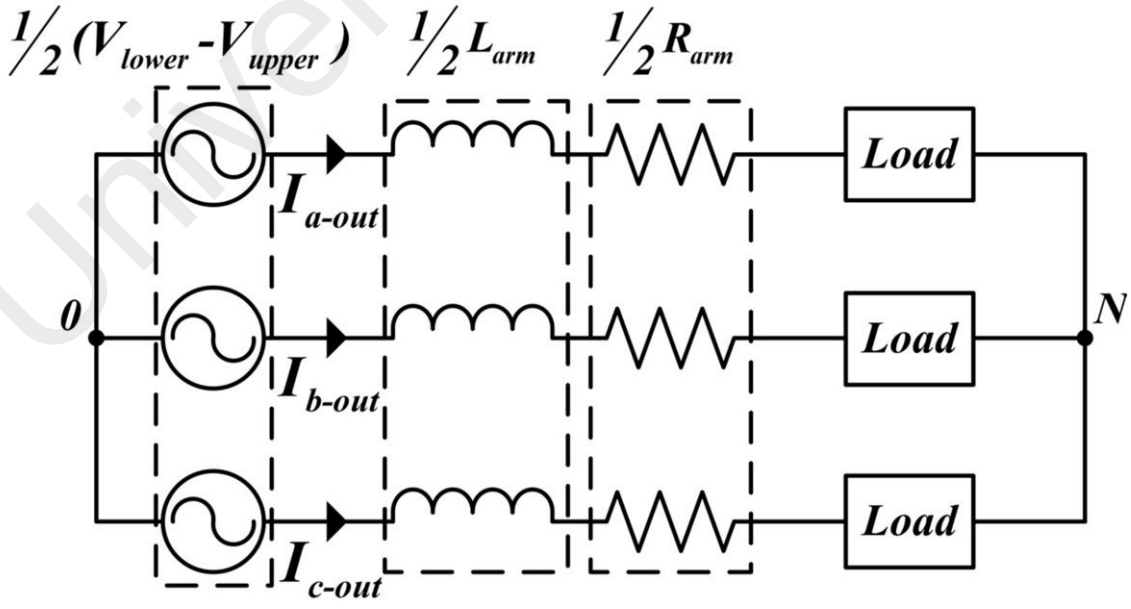



**Figure 3.3:** Equivalent three-phase circuit of AC side

Controlling the DC-side of the MMC is essential by controlling the balancing between the upper arm and lower arm to achieve the stability of this converter. Based on Kirchhoff's Voltage Law (KVL), the loop of the DC-side can be expressed as:

$$V_{DC} = \left[V_{lower} + L_{arm}\frac{dI_{lower}}{dt} + I_{lower}R_{arm}\right] + \left[V_{upper} + L_{arm}\frac{dI_{upper}}{dt} + I_{upper}R_{arm}\right] \quad 3.14$$

Based on Kirchhoff's Current Law (KCL), DC current can be found and stated in equation 3.15.

$$I_{circ} = \frac{I_{upper} + I_{lower}}{2} \quad 3.15$$

Substitute equation 3.15 into equation 3.14.

$$V_{DC} = \left(V_{lower} + V_{upper}\right) + 2L_{arm}\frac{dI_{circ}}{dt} + 2R_{arm}I_{circ} \quad 3.16$$

Using,

$$V_{internal} = L_{arm}\frac{dI_{circ}}{dt} + R_{arm}I_{circ} \quad 3.17$$

The internal voltage can be expressed in equation 3.18.

$$V_{internal} = \frac{V_{DC} - (V_{upper} + V_{lower})}{2} \quad 3.18$$

The equivalent circuit of the DC-side is shown in Figure 3.4, $L_{arm} = L_{upper} = L_{lower}$ and $R_{arm} = R_{upper} = R_{lower}$.

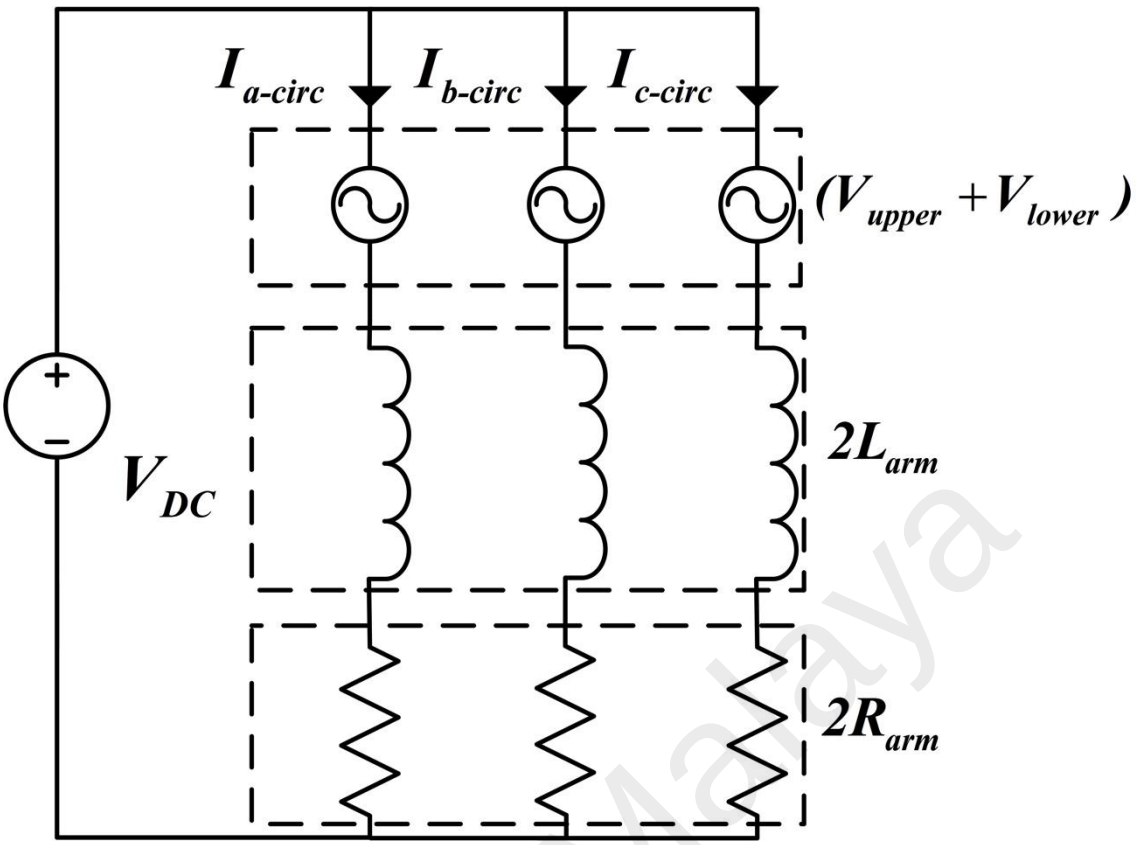



**Figure 3.4:** Equivalent three-phase circuit of DC-side.

From equation 3.17, the internal voltage ($V_{internal}$) is linked to the circulating current ($I_{circ}$). The transfer function relationship between the internal voltage and circulating current can be stated in equation 3.19 and the transfer function block diagram of the control structure is shown in Figure 3.5.

$$I_{circ} = \frac{1}{sL_{arm}+R_{arm}}\left(\frac{V_{DC}}{2} - \frac{(V_{upper}+V_{lower})}{2}\right) \quad 3.19$$

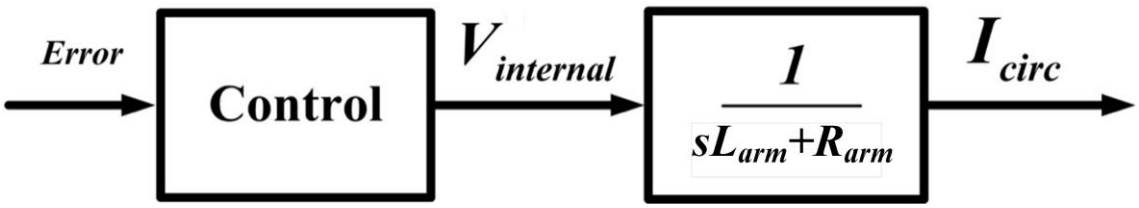



**Figure 3.5:** The general control structure of circulating current.

The schematic of the MMC with cascaded SMs series are able to react as a nearly ideal voltage source within boundaries specified by the number series of SM, throughout the power balance where the arms is managed. Thus, the power exchange of each the SMs needs to be considered. Instantaneous power expression of the phase arms can be defined by multiplying the upper voltage with the upper current for upper arm power and lower voltage with the lower current for lower arm power as expressed in equation 3.20 and equation 3.21.

$$P_{upper} = V_{upper} * I_{upper} \quad 3.20$$

$$P_{lower} = V_{lower} * I_{lower} \quad 3.21$$

The total of SM capacitors' voltage is essential issue in regulating the stability of pure alternating voltage and current appearing at the AC terminal. As mentioned before, when the DC voltage is equal to the sum capacitor voltage, the magnitude range of AC voltage is maximized and stabled. Therefore, the sum capacitors' voltage of the SM series in upper or lower arm is customarily equal to the DC-side voltage as stated in equation 3.22.

$$V_{c\_lower}^{\Sigma} = V_{c\_upper}^{\Sigma} = V_{DC} \quad 3.22$$

For the operation of the cascaded SMs, it is compulsory that the power flow must be balanced over the time (i.e., the power transferred at the terminal is not always constant). When all SMs are conducted or inserted, all the capacitors are connected in series connection. Thus, the equivalent capacitance or called arm capacitance ($C_{arm}$) can be calculated via the basic circuit theorem. The general transfer function of the total sum of the SMs in the arm can be stated in equation 3.23 and the control law is shown in Figure 3.6.

$$V_{c\_lower\ or\ upper}^{\Sigma} = \frac{1}{sC_{arm}} I_{circ} \quad 3.23$$

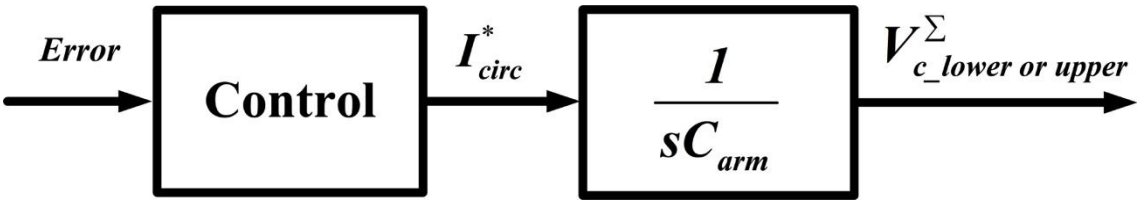



**Figure 3.6:** The general control of total voltage arms control.

From the basic theorem of capacitor, an electrical potential energy is stored in a capacitor when a input power is connected across the capacitor terminals, thus such the constant term will result in a controlled increase or decrease in the capacitor's energy, as well as controlling the capacitor voltage. This expression can be written in equation 3.24 and equation 3.25.

$$V_{c\_upper}^{\Sigma} = \sqrt{\frac{2W_{c\_upper}^{\Sigma}}{C_{arm}}} \quad 3.24$$

$$V_{c\_lower}^{\Sigma} = \sqrt{\frac{2W_{c\_lower}^{\Sigma}}{C_{arm}}} \quad 3.25$$

The stored energy among the arms can also be calculated by integrating the power delivered into the arm. The expression can be written in equation 3.26 and equation 3.27, where $V_{circ}$ is circulating voltage. The derivation of $V_{circ}$ can be seen in equation 3.18.

$$\frac{dW_{upper}}{dt} = P_{c\_upper} = (V_{circ} - V_{out})(\frac{I_{out}}{2} + I_{circ}) \quad 3.26$$

$$\frac{dW_{lower}}{dt} = P_{c\_lower} = (V_{circ} + V_{out})(-\frac{I_{out}}{2} + I_{circ}) \quad 3.27$$

The sum capacitor voltages of the SM series are essential issue to be controlled. For the half-bridge SM series with the total capacitor voltage, the AC voltage magnitude range is fairly ideal when the direct voltage is half of this value. Therefore, the sum of energy of the SM series in each arm is set equal to input energy supplied from input DC-side. This expression can be written in equation 3.28.

$$W_c^{\Sigma}(t) = W_{c\_upper}^{\Sigma}(t) + W_{c\_lower}^{\Sigma} \tag{3.28}$$

The imbalance among the arms can be sensed by subtracting the upper energy arm from the lower energy arm, which is in ideal situation the subtraction among the arm become "zero" to make sure the energy among the arms is balanced. The expression can be expressed in equation 3.29:

$$W_c^{\Delta}(t) = W_{c\_upper}^{\Sigma}(t) - W_{c\_lower}^{\Sigma} \tag{3.29}$$

Equation 3.28 and 3.29 give the dynamic relation involving the balancing of the SMs capacitor voltages within the string. The capacitor voltage slightly varies between the SMs given that all the SMs are not inserted or bypassed simultaneously. The controller locally regulates each arm to keep the individual capacitor voltage between the upper and lower arms identical.

## 3.3 Controller Structure of MMC

One of the common concepts to control the operation MMC is to achieve the balancing capacitor voltage by using a centralized control. All the control signals are generated using calculations based on feedback variable that sensed from all submodule capacitors' voltages. Since this approach should be realized across boundaries of power converting modules that belong to different phases, and are operating at various floating voltages, it compromises the advantage of modularity and leads to enormous system-level complexity.

The distributed control approach will resolve the disadvantages caused by a centralized controlled MMC system. Such an approach would realize control and modulation strategies inside each power converting module using highly integrated circuits, and release most of the time-critical control responsibilities from the central controller divided into multiple subtasks and distributed these tasks into individual module local controllers. As a result, a slower supervisory controller can be used to sustain performance of the whole system, instead of the original high-speed central controller, with enormous communication needs.

This work uses centralized methods to achieve voltage balancing by selecting particular SMs for specific switching states depending on the capacitor voltage, current arm direction ($I_{upper}$ and $I_{lower}$), and number of SMs under the ON state. Figure 3.7 and Figure 3.8 present the overall DC-side control structure of the MMC performance as an inverter. The outer loop controller consists of the total and differential energy controller having a function to control all the SMs capacitor voltage according to its command, wherein the circulating current reference is being the output. Therefore, the circulating current facilitates the transfer of energy to and from both arms and between the upper and lower arms. Afterward, the circulating current through the DC input and converter leg of the capacitor voltages are regulated by the inner circulating current control loop.

The total and differential energy controllers are designed by using proportional-integral (PI) controllers, as shown in Figure 3.7. The outer energy-based controller uses the PI control techniques where the sum of the SM capacitor voltage applies the low pass filter (LPF) with 50-Hz and 100-Hz cut-off frequency. The circulating current controllers are designed by using a proportional-resonant (PR) controller, in which the feedback circulating current is calculated from the upper and lower arm currents, as shown in Figure 3.8. This control strategy is used due to its capability to reduce a negative sequence

current controller compared with that in DQ stationary-reference-fram (SRF). Moreover, this method is also convenient to use for a single phase and is stable because PLL is not used. The transfer functions of PI and PR are written in equation 3.30 and equation 3.31. Generally, different forms of closed-loop controls are required to maintain the capacitor voltage balance at the desired setpoint over time.

$$C_{PR} = K_P + K_I \frac{S}{S^2 + \omega_o^2} \tag{3.30}$$

$$C_{PI} = P + I\frac{1}{S} \tag{3.31}$$

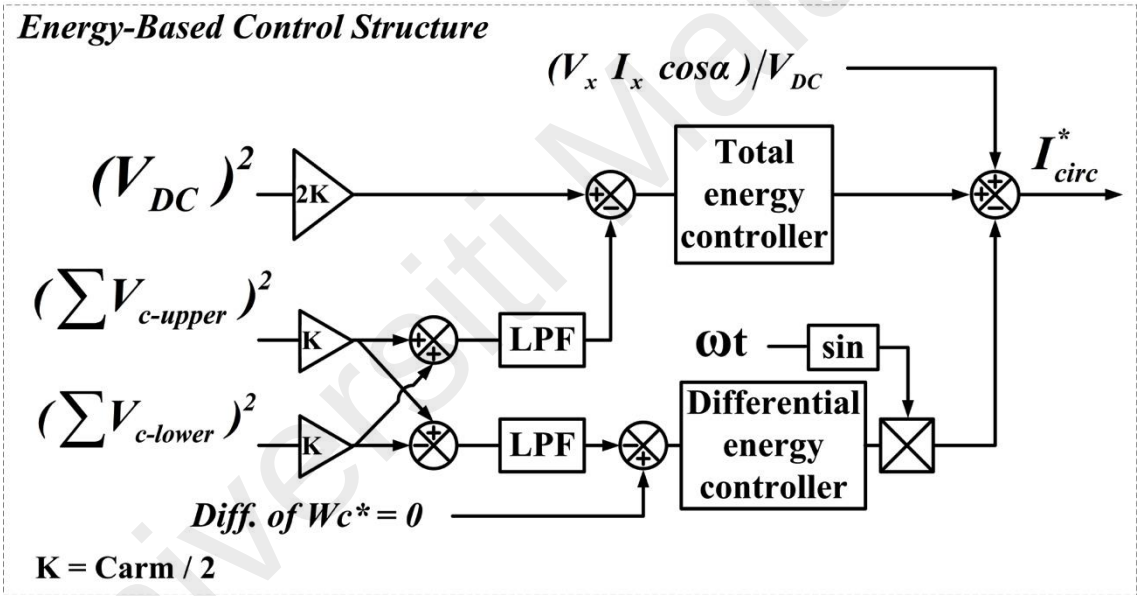



**Figure 3.7:** Energy-based control structure.

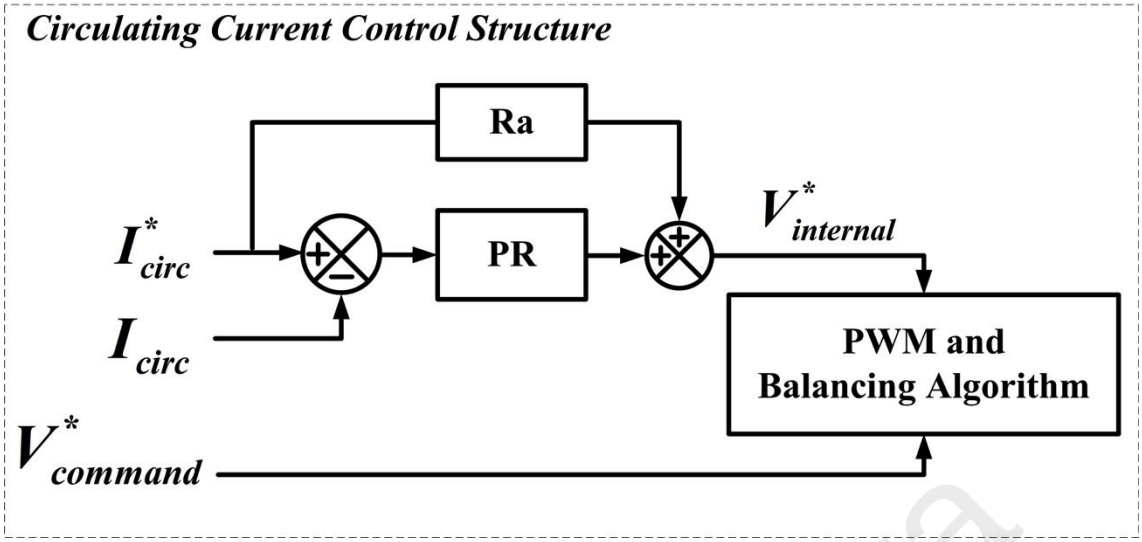



**Figure 3.8:** Circulating current control structure.

In the three-phase system, the Clarke transformation and Park transformation are the most common method being used to simplify the three-phase parameters into the two-dimensional static reference or known as stationary-reference-frame (SRF). The Clarke transformation is used to convert the balanced three-phase parameters into the orthogonal two-dimensional space or sometimes knows as the 3-2 (three to two) transformation. Then, the Park transformation is commoly used to transform the rotating reference frame into two-dimensional static reference by eliminating time-variance and it is knows as 2-2 (two to two) transform. The equation of Clarke and Park transformation is stated in equation 3.32 and 3.33 Finally, the transformation can be employed in the controller structure easily.

$$\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{matrix} f_a \\ [f_b] \\ f_c \end{matrix} \tag{3.32}$$

$$\begin{bmatrix} f_d \\ f_q \end{bmatrix} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix} \begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} \tag{3.33}$$

## 3.4 Summary

This chapter presents the mathematical derivation and the control structure of the MMC. The discussion starts with analyzing the MMC circuit using basic theorem of circuit theory, such as Kirchhoff Voltage Law (KVL) and Kirchhoff Current Law (KCL). The detailed control structure for the converter is presented well by finding the transfer function of the converter. The control structures for DC-side are devided into two loops, which are energy-base as outer-loop control and circulating current control as inner-loop control. These forms of closed-loop controls are required to maintain the capacitor voltage balance at the desired setpoint over time.

# CHAPTER 4: ADAPTIVE CARRIER BASED PHASE DISPOSITION PWM (PDPWM) TECHNIQUES

## 4.1 Introduction

The intention of this chapter is to describe the control in distributing the pulses into the submodule and to explain well the proposed adaptive carrier based phase disposition PWM (PDPWM). The case study and the findings are validated in simulation and experimental setup in Chapter 5.

## 4.2 Selection of SMs and Capacitor Voltage Balancing

Each of SM capacitors' voltage placed in arms must be sensed and kept equal among them over time. An SM has two conditions of voltage, which are $V_c$ and zero depending on the state of each SM (i.e., "Inserted" and "Bypassed", respectively). The capacitor will be charged or discharged during the inserted-state, and according to the direction of arm current ($I_{SM}$). When the upper and lower arm current is positive, the corresponding capacitor inside the SM will be charged and its voltage increases. In reverse, when the current in the upper or lower arm is negative, the capacitor of the inserted SM is discharged and its voltage drops. Then, the corresponding capacitor will be bypassed and its voltage remains unchanged if an SM is OFF or bypassed regardless of the direction of the upper or lower arm current.

The SM capacitor voltages of each arm are measured and sorted in ascending algorithm in order to do the capacitor voltage-balancing task of the SMs at each arm during each PDPWM period. The selection of the number of the inserted SM is identified according to the sorting number of capacitors' voltage. If the upper or lower arm current is positive polarity, the number of SMs at upper ($N_{upper}$) or lower ($N_{lower}$) arm with the lowest voltages are inserted by turning ON switch $S1$ as shown in Figure 4.1, MODE I, where the grey line indicates no current flow. Hence, the selected SMs capacitors'

voltages are charged and their voltages increase. If the upper or lower arm current is negative polarity, the number of SMs at upper ($N_{upper}$) or lower ($N_{lower}$) arm with the highest voltages are inserted by turning ON switch $S1$. Consequently, the selected SMs capacitors' voltages are discharged and their voltages drop, as shown in Figure 4.1, MODE II. When it is ON or Inserted-state, the corresponding switching function of each SM is "1" for switch $S1$ and "0" for switch $S2$, complementary to each other. Otherwise, it is "0" for $S1$ and "0" for switch $S2$ when it is OFF or Bypassed-state.

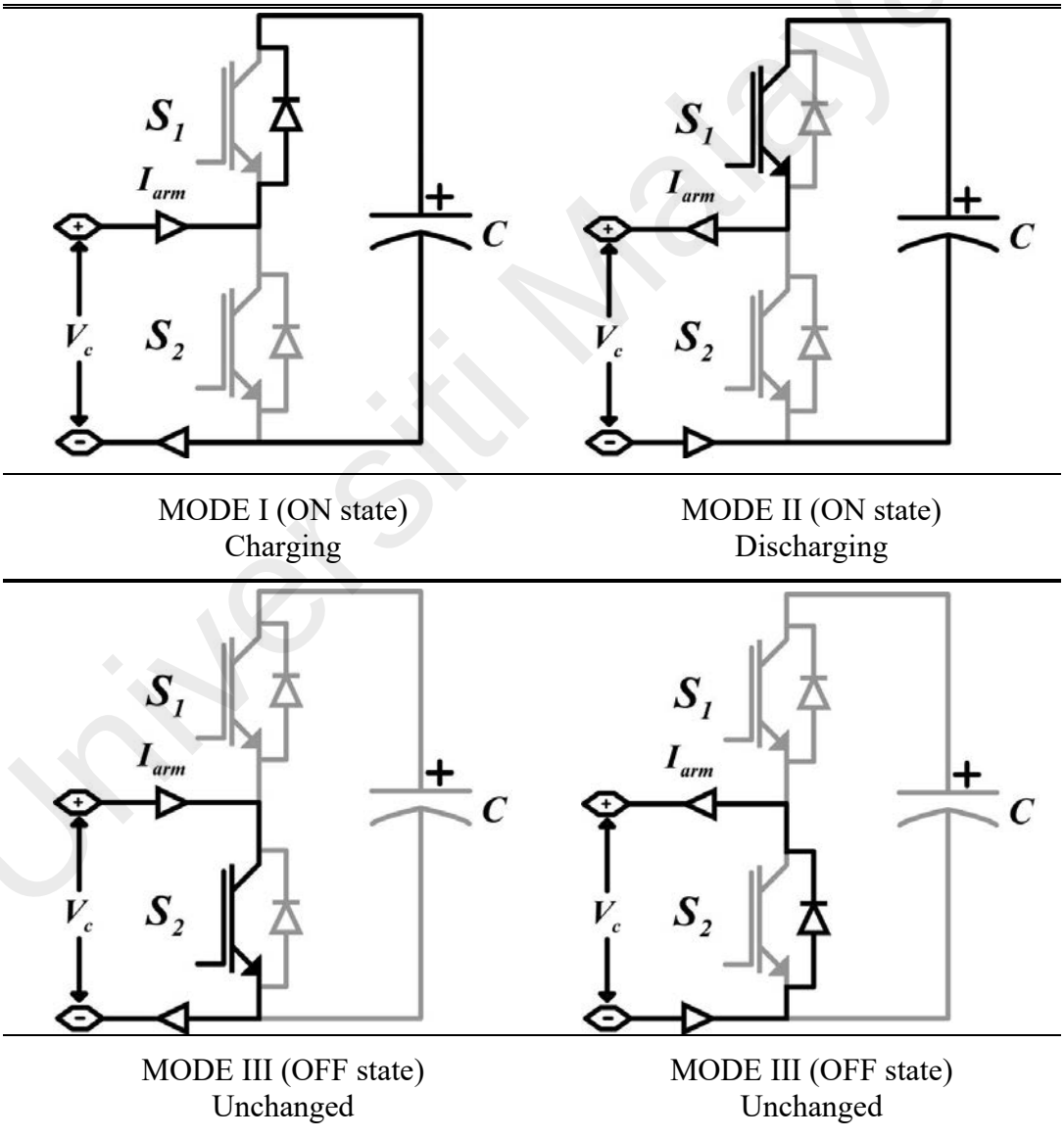
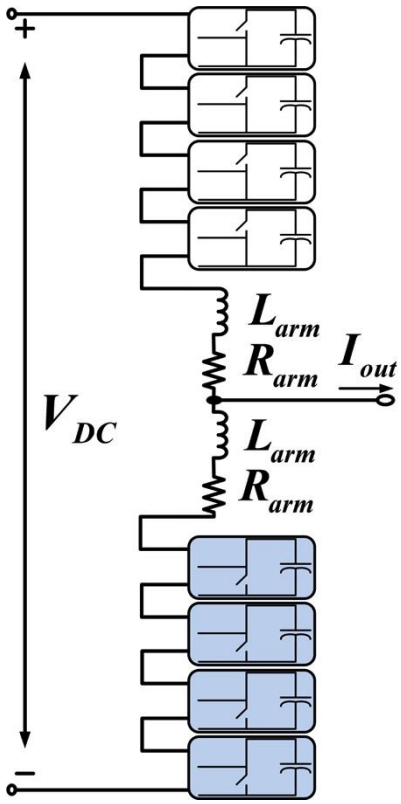


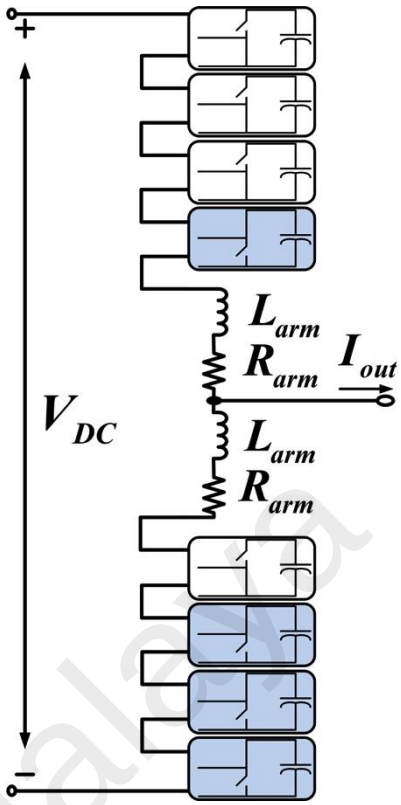

**Figure 4.1:** The current flow in SM.

The sequence of the inserted number of SMs can be described below and illustrated in Figure 4.2, where blue colour indicates ON state:

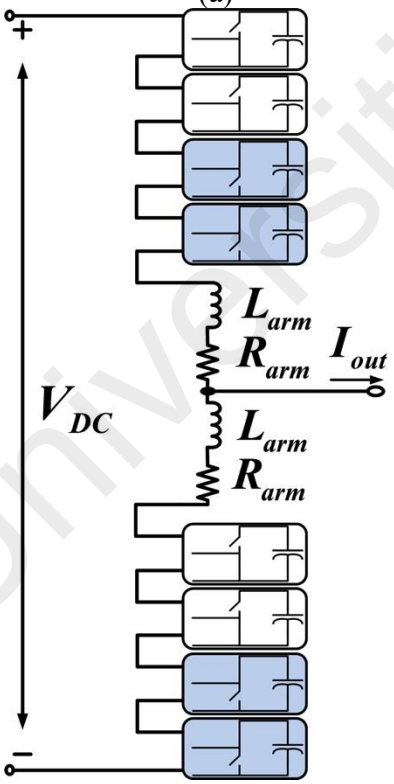
1. **State 1;** for voltage level 5, $V_{AC}(t) = V_{DC}/2$, All of four upper SMs are OFF and All of lower SMs are ON (i.e., $N_{upper} = 0$ and $N_{lower} = 4$), as shown in Figure 4.2(a).
2. **State 2;** for voltage level 4, $V_{AC}(t) = V_{DC}/4$, three upper SMs are OFF and three lower SMs are ON (i.e., $N_{upper} = 1$ and $N_{lower} = 3$), as shown in Figure 4.2(b).
3. **State 3;** for voltage level 3, $V_{AC}(t) = 0$, two upper SMs are OFF and two SMs lower are ON (i.e., $N_{upper} = 2$ and $N_{lower} = 2$), as shown in Figure 4.2(c).
4. **State 4;** for voltage level 2, $V_{AC}(t) = -V_{DC}/4$, three upper SMs are ON and three lower SMs are OFF (i.e., $N_{upper} = 3$ and $N_{lower} = 1$), as shown in Figure 4.2(d).
5. **State 5;** for voltage level 1, $V_{AC}(t) = -V_{DC}/2$, All of four upper SMs are ON and All of lower SMs are OFF (i.e., $N_{upper} = 4$ and $N_{lower} = 0$), as shown in Figure 4.2(e).




(a)




(b)

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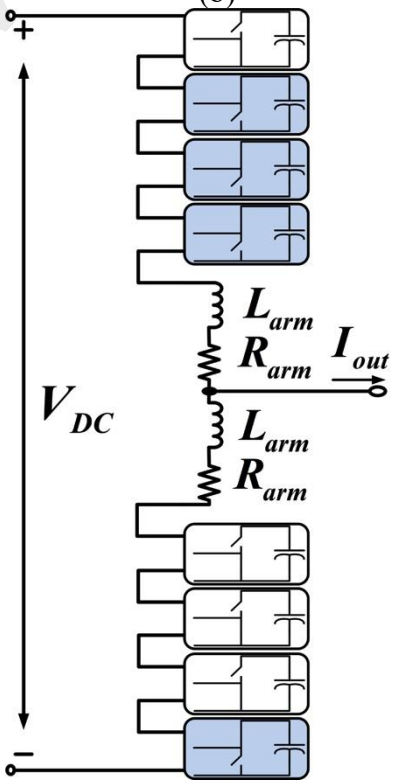
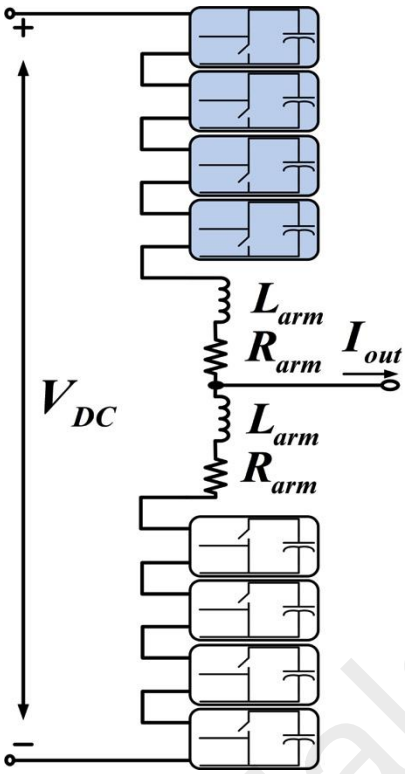



(d)




(e)

**Figure 4.2:** Different switching states of an MMC for acquiring the five different levels of the waveform.

## 4.3 Adaptive PDPWM Method

MMCs have interesting modulation control methods. On the basis of the mathematical model of MMC, the output voltage is controlled by upper and lower arm voltage references, which can be expressed as follows:

$$V_{upper} = \frac{V_{internal}}{2} - V_{command} \quad 4.1$$

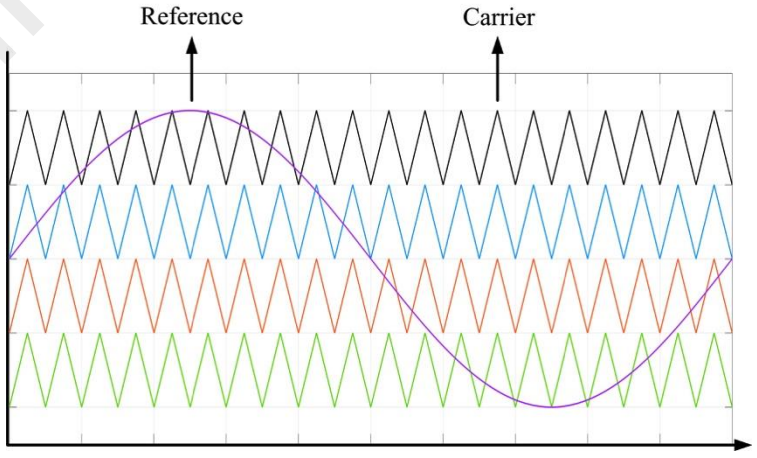
$$V_{lower} = \frac{V_{internal}}{2} + V_{command} \quad 4.2$$

From equation 4.1 and equation 4.2, the reference signals of the upper arm ($V_{upper}$) and lower arm ($V_{lower}$) have a 180° phase shift. In the PWM strategies, the reference signals are compared with the specified carriers, which are the specific pulses sent to

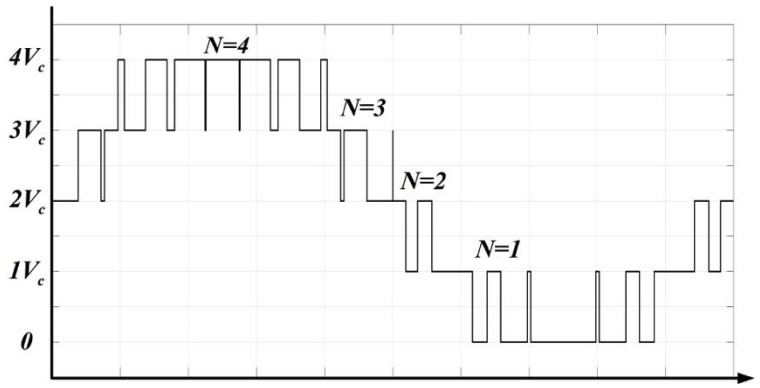
SMs. The MMC can generate two types of voltage level, that is, $N + 1$ or $2N + 1$ level. The difference of the 180° phase shift between the upper and lower arms provide independent pulses to the upper and lower arm SMs, and the output level is $2N + 1$. The output pulses for the upper and lower arms depend on each other by interleaving the carrier signals, and the output level is $N + 1$.

As shown in Figure 4.1, the SM can work in either ON or OFF state, and the output is the capacitor voltage or zero voltage, respectively. The required waveform can be synthesized with different combinations of the SM switching states. Therefore, a proper PWM strategy is needed to determine the SM state and achieve appropriate power quality and low losses simultaneously.

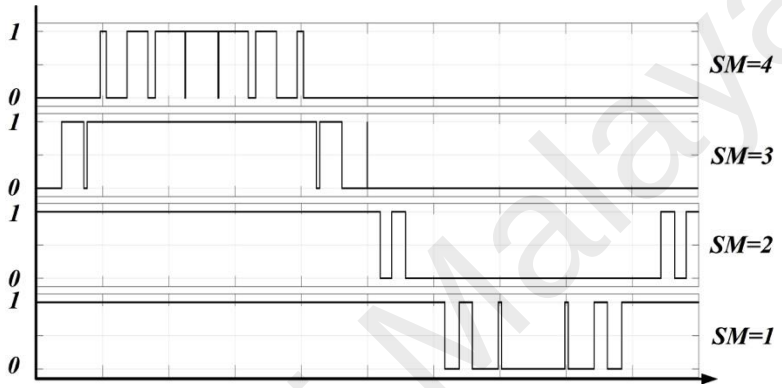
The PDPWM is a type of level-shifted carrier method that has been greatly used for multilevel converters. Figure 4.3 illustrates PDPWM method. PDPWMs use one voltage reference and some carriers that are stacked on top of each other, thereby dividing the available direct voltage range between them. After generating the pulses, the pulses are being distributed to all the SMs. The power flow from/into the SMs slightly varies if assigning the pulse distribution directly into the $N$-th SM as shown in Figure 4.3(c).




(a)




(b)




(c)

**Figure 4.3:** Conventional PDPWM with a single reference and four carriers, (b) Pulse distribution for PDPWM with four SMs in one arm, (c) Direct pulse distribution.

An asceding sorting algorithm is used in this study to arrange the position of SMs based on the voltage stored in the capacitor. Then, based on the position of SMs, each of SMs is decided in the ON-, OFF-, and PWM-state, which gives the commands to distribute the pulses among the SMs. Figure 4.4 shows that the command signal is divided into 4 regions which refer to the number of SMs used in this work. This process is called selection algorithm. Hence, a staircase signal is generated due to an intersection between the command signal and four defined areas. Thus, the staircase signal will follow the time and frequency of the command signal. The staircase waveform is needed to determine the number of SM that should be ON and OFF in each arm.

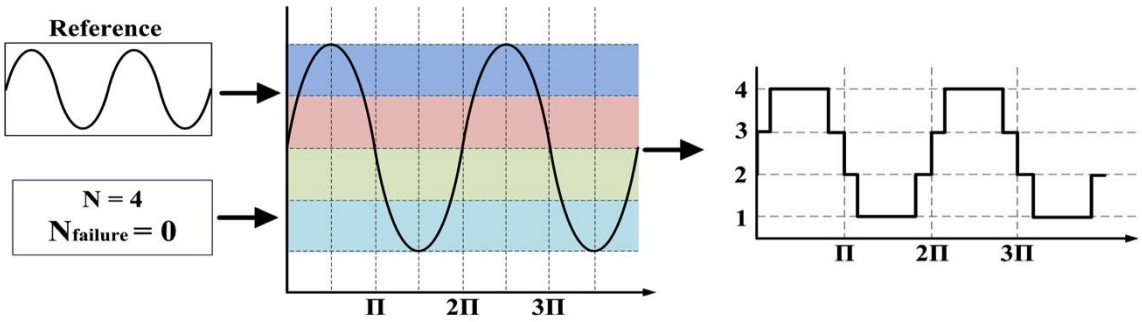



**Figure 4.4:** Illustration of staircase generation.

This study also presents two methods of pulse distribution into the SMs. First, the multiport block is used to arrange the pulses into the same level on the basis of the staircase signal generated by the upper or lower arm references. The illustration of the multiport process is shown in Figure 4.5. The generated pulses in the multiport are mapped through the selection algorithm. So that the pulses can be distributed to all the SMs equally, and the balancing among the SMs can be achieved faster.

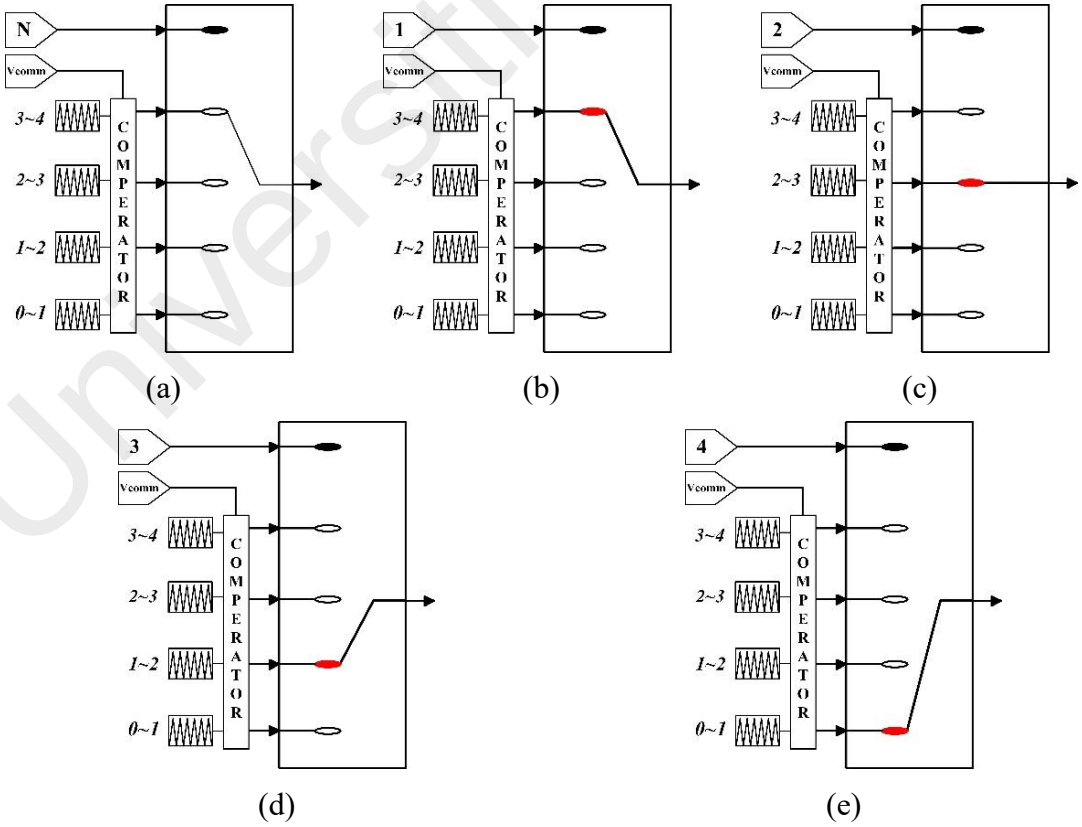



**Figure 4.5:** PWM signal generation using a multiport block.

PDPWM methods have the same phase angle and varying level offsets. Logically, only one type of triangle carrier and one voltage reference are necessary for each arm. This study shows how to use only one triangle by utilizing the voltage reference. In the second method, the staircase waveform is used to arrange the carrier in accordance with the upper and lower reference signals instead of using the multiport block to organize the pulses similar to that in the first method. Thus, this approach can be called adaptive carrier, as shown in Figure 4.6. This method uses one carrier signal that can help program more flexible carrier signals than conventional ones, because the carrier can change with different level. Moreover, if SM failure and maintenance exist, then this method can respond by immediately changing the scale of the carrier waveform without turning off the converter. Figure 4.7 shows the overall PWM block diagram for the MMC. The voltages of SM at each arm are sensed through the sensor, so that the algorithm will operate the carrier based on the failure situation. The algorithm is shown in the Figure 4.8. then, the selection algorithm has a function to choice which SM that need to be ON or OFF. The operation of selection algorithm work based on the sorting algorithm where it has function to arrange the SMs. Finally, the pulses are distributed to the all switched based on the condition that given by the fault-tolerant algorithm and selection algorithm.

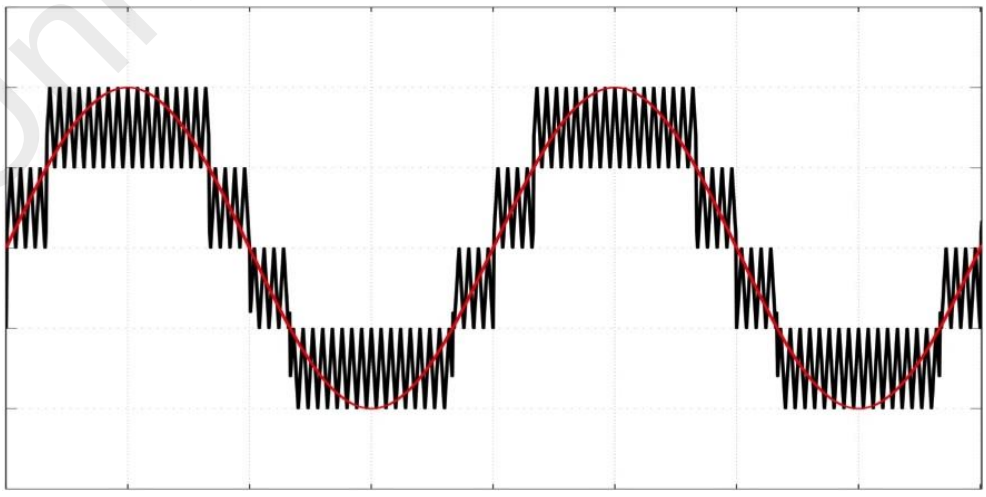


**Figure 4.6:** Waveform of the reference signal and the adaptive carrier.

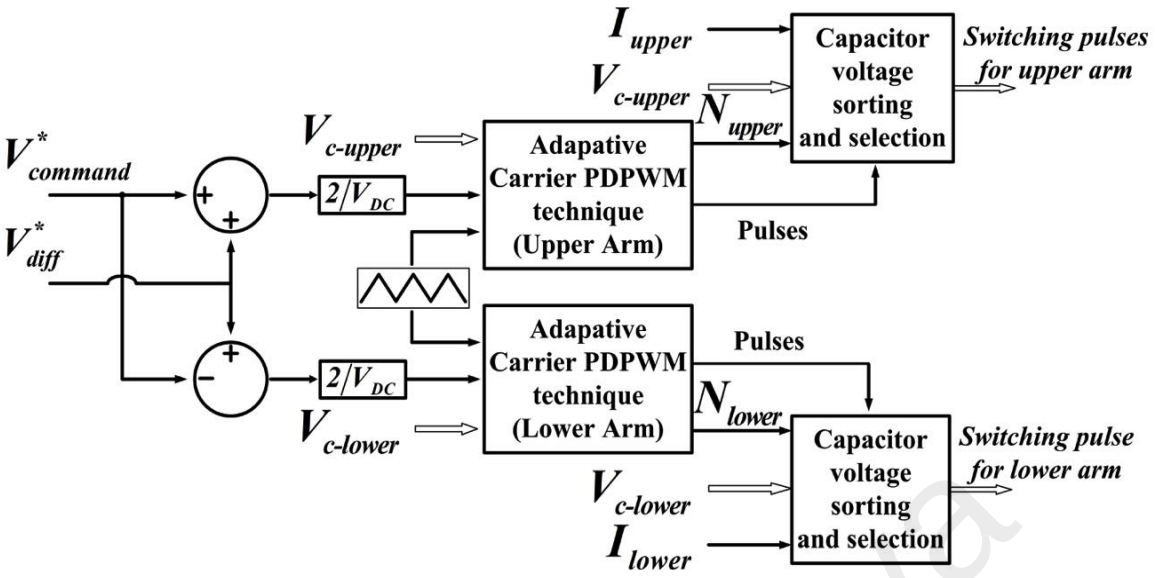



**Figure 4.7:** PWM block diagram.

## 4.4 Fault-Tolerant Ability

Fault happens in one of the SMs in any arm of the MMC, $V_{diff}$ between the healthy phase units and faulty one gets larger. This condition brings the circulating current fluctuation and unstability at the output side (AC terminal). When PWM block dictates all SMs in the same arm to be switched on after the fault occurrence, healthy capacitor voltages increase to recover faulty submodule. In this period, the arm current negative polarity is suppressed because of circulating current is boosted by fault free phase units. In normal operation, each capacitor voltage can be expressed in equation 4.3.

$$V_c = \frac{V_{DC}}{N} \tag{4.3}$$

In case of fault, healthy SM capacitor voltages are expected to increase to reach the voltage, which can be shown in equation 4.4.

$$V_{c,threshold} = \frac{V_{DC}}{N - N_{fauly}} \tag{4.4}$$

Where $N_{fauly}$ is number of faulty submodule.

This voltage can be used as a threshold to detect the fault in any phase unit of the MMC system. An SM voltage ($V_c$) reach or exceed the voltage threshold for a certain period of time that arm can be labeled as faulty and it can be proceeded to locate the faulty module in the arm. From equation 4.4, it can be understood from this that if in a real application where hundreds of SM are used, the threshold voltage for fault detection becomes smaller. The faulty detection period can work well and fast.

The number of SM being used in this project is 4 modules per arm. According to the theoretical explanation from the Chapter 3, it can generate nine-level voltages ($2N+1$) in normal operation. In the following, it is assumed that the SM number 4 (SM#4) in lower arm in the phase is malfunctioned. Therefore, the sensor will detect the abnormal SM, and the faulty SM#4 is bypassed; thus, the output voltage of the SM#4 is expressed as follows in 4.5.

$$SM_{\#4\_lower} = 0 \qquad 4.5$$

The total numbers of the SMs (N) are four, but when the SM#4 fails and needs to be bypassed, the number of SMs that can be inserted is limited to three. Therefore, the faulty SM in the lower arm can generate three-pole voltage levels (i.e., $V_{DC}/3$, 0, $V_{DC}/2$, and $V_{DC}/1$, except $V_{DC}/4$).

The above condition can cause an imbalance among the capacitor voltages. This study uses the scenario; when an upper arm SM fails, a lower arm SM is removed to maintain the phase voltage symmetry. One of the other SMs at the other arm should also be in a bypassed mode, even in a healthy condition, to balance the capacitor voltage among the arms. When the faulty SMs apply bypassed mode, the rest of the healthy SMs tend to rise. The percentage of the increment can be calculated by equation 4.6. This percentage needs to be considered for selecting the rating of capacitor and IGBT during the fault.

$$Tolerance\ (\%) = \frac{N_{fault}}{N_{total} - N_{fault}} x\ 100\% \quad 4.6$$

Figure 4.8 shows a simple flowchart that illustrates a fault occurring among the SMs. The sensors provide a fault signal to the controller. Here, SM#4 in the lower arm is assumed to have a malfunctioned operation. The controllers sense the failure and start to deactivate SM#4 in the lower arm. The other SM in the upper arm is also placed in an OFF state (deactivated). The new number of SM ($N$) is obtained, and the converter automatically works with difference number of submodules. This failure signal is also responded by the staircase signal. The illustration is depicted in Figure 4.9. The colours indicate the area that generated based on the number of submodules. Then, the generated staircase is resulted based on the comparison algorithm between the area and the reference signal.

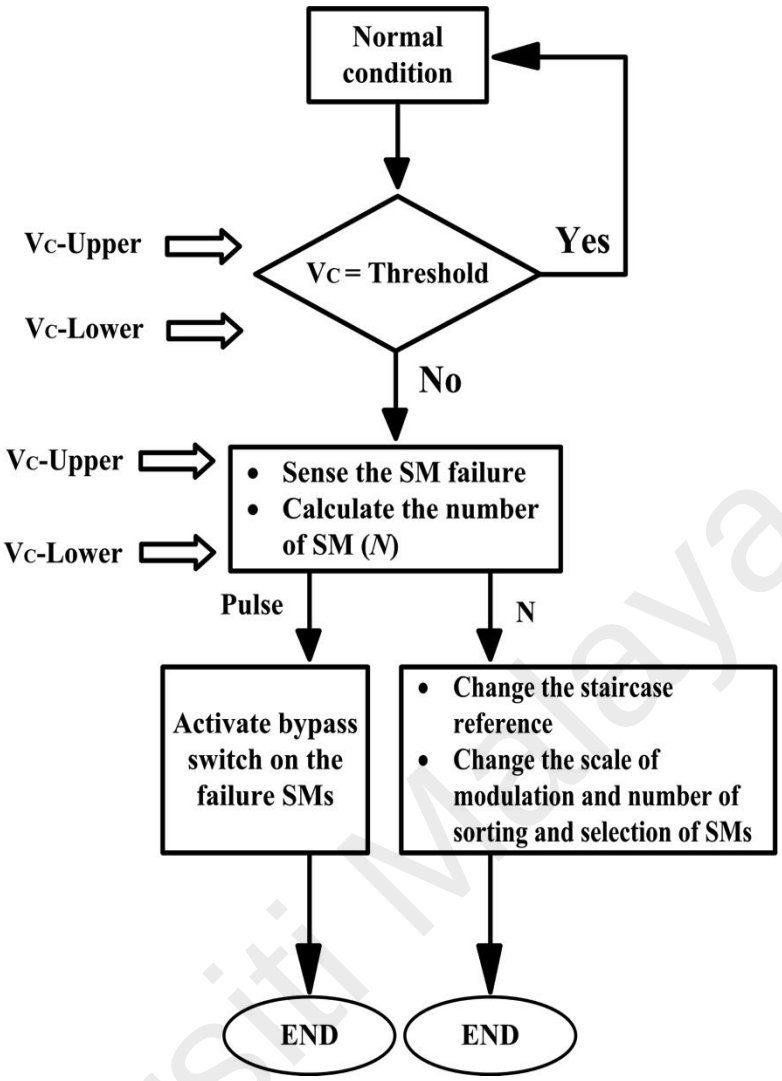



**Figure 4.8:** Flowchart of the fault-tolerant action.

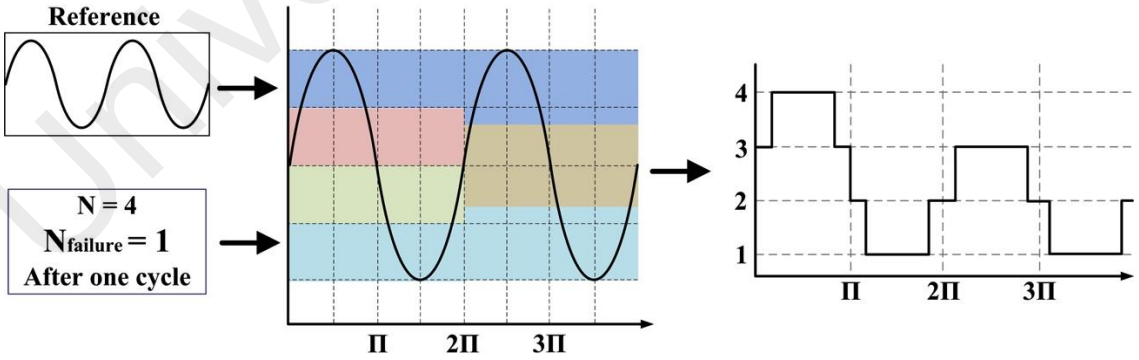



**Figure 4.9:** Illustration of fault-tolerant after one cycle.

## 4.5 Summary

This chapter presents the selection algorithm along with the proposed fault-tolerant strategy. MMCs have attractive modulation control methods where the upper arm ($V_{upper}$) and lower arm ($V_{lower}$) have a 180° phase shift. The difference of the 180° phase shift between the upper and lower arms provides independent pulses to the upper and lower arm SMs, and the output level is $2N + 1$ by using PDPWM. After generating the pulses, the pulses are distributed to all the SMs through selection algorithm to achieve a well balance among all the SMs.

This method uses one carrier signal that can help program more flexible carrier signals than conventional ones. The sensors provide a fault signal to the controller. Here, an SM in the lower arm or upper arm is assumed to have a malfunctioned operation. The controllers sense the failure and start to deactivate the faulty SM in one arm. The other SM in the other arm is also placed in an OFF state (deactivated) to achieve symmetrical between the arms. The new number of SM ($N$) is obtained, and the converter automatically can works with difference number of submodule.

# CHAPTER 5: SIMULATION AND EXPERIMENTAL RESULT

## 5.1 Introduction

Simulations using MATLAB/Simulink and experiments were carried out using laboratory prototype to verify the validity and feasibility of the proposed control strategies presented in Chapter 4. The single-phase MMC laboratory prototype was assembled and employed to study the performance of the proposed algorithm.

This chapter is organized as follows: initially, the simulation results of the proposed method for MMC are presented and discussed. Then, the setup of single-phase MMC laboratory prototype is described in this chapter. Finally, the experimental result of the single-phase MMC laboratory prototype is presented and discussed.

## 5.2 Simulation Results

The simulation model of single-phase MMC inverter was designed in MATLAB/Simulink to verify the MMC topology with the control scheme before the hardware implementation. The flow chart of control structure is shown in Figure 5.1. Table 5.1 states the parameters of the simulation and also used for experimental validation.

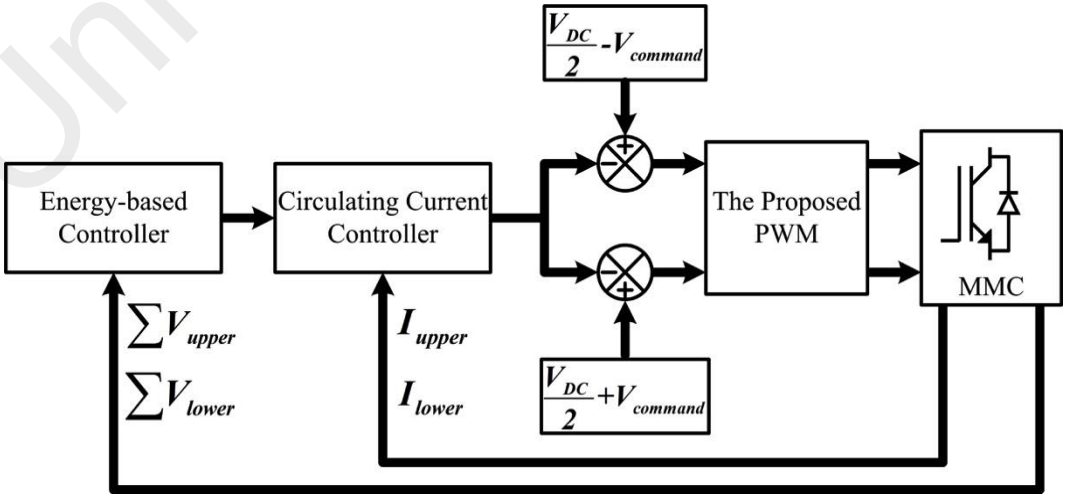



**Figure 5.1:** Flow chart of control structure.

**Table 5.1: The Parameters of Single Phase MMC under Simulation and Experimental Validation**

| Items | Value |
|---|---|
| Fundamental Frequency | 50 Hz |
| DC-Link Voltage | 200 V |
| Arm Inductance | 5 mH |
| Arm Equivalent Resistance | 0.2 Ω |
| SM Capacitor | 3300 $\mu$F |
| Number of SM in each arm | 4 |
| Switching Frequency | 2.5 kHz |

### 5.2.1 Normal State Operation

At the start of the operation, the voltages of the SM capacitors are firstly energized via passive (or noncontrolled) pre-charged method at condition MODE I (or all switches are OFF state) until half of the desired voltage. This passive pre-charged may reduce the inrush current. Then, the whole of SMs are charged to the desired voltage ($V_{DC}/N$) by energy-based control under a zero-output condition. Throughout the charging process, the ripple in capacitor voltages is less, as shown in Figure 5.2. The low-frequency ripple increases when the terminal output, which is the AC voltage, is connected to the load at 1.6 s. This phenomena occurs because each capacitor works as an energy storage where the amount of energy released and taken from the DC power supply proportionally depends on the load.

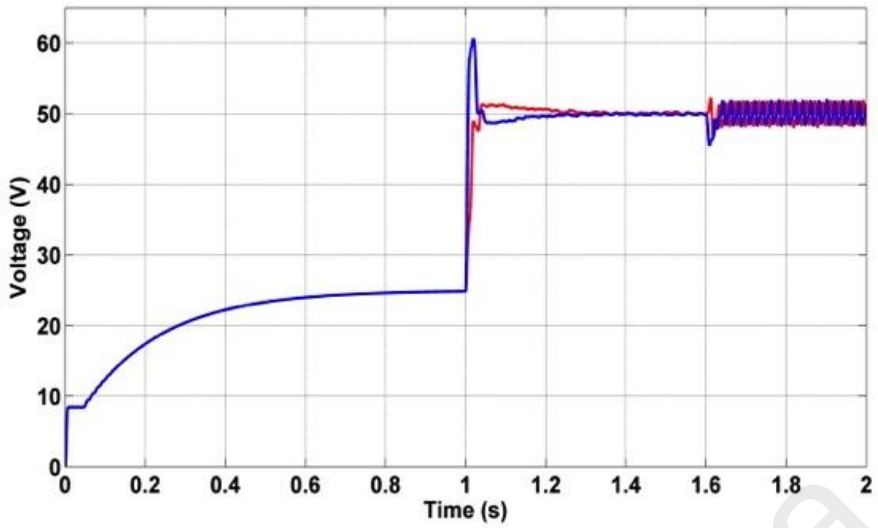



**Figure 5.2:** The waveform of capacitor voltage during start-up.

In the steady-state condition, the output waveform of the simulated nine-level voltage in the normal condition is shown. Figure 5.3, Figure 5.4, and Figure 5.5 show the MMC output voltage, the load current, and the upper/lower arm SM capacitor voltages at each arm respectively after giving an inductive load. Evidently, the capacitor voltage average is 50 V with having an approximate peak-to-peak voltage of 2 V. Those results indicate the total energy control, differential energy control, and balancing control work effectively.

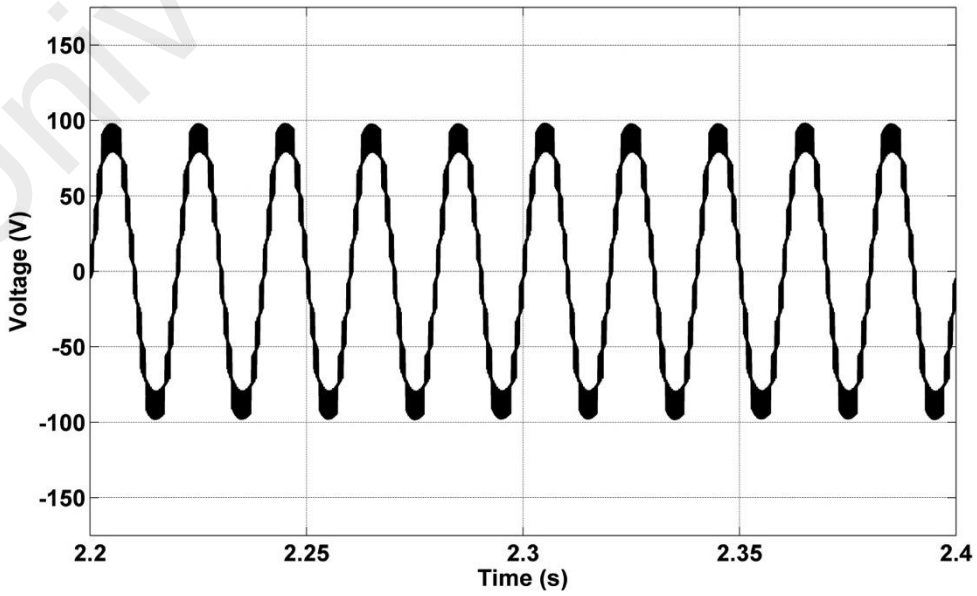



**Figure 5.3:** Waveform of output nine-level AC voltage.

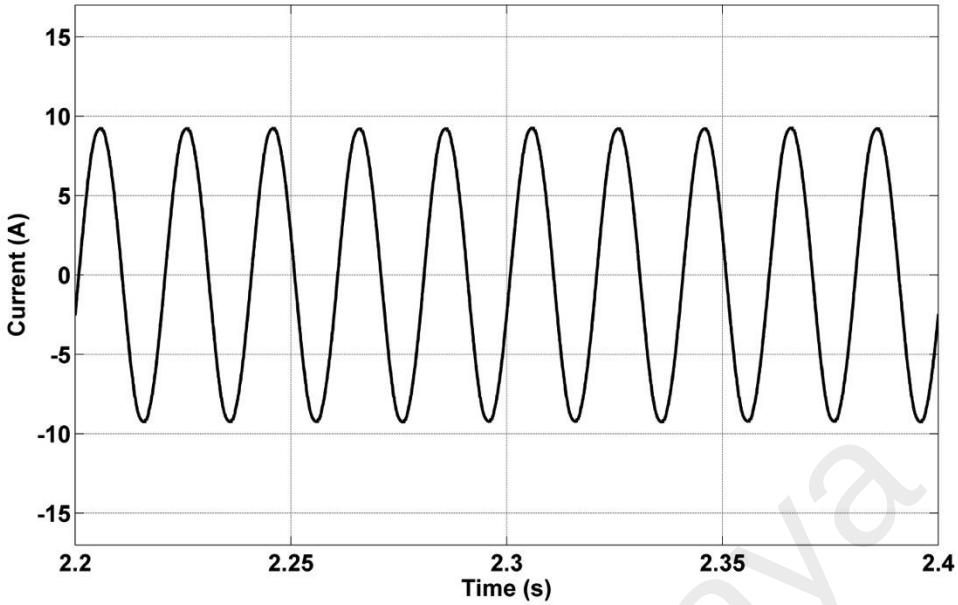



**Figure 5.4:** Waveform of output AC current.

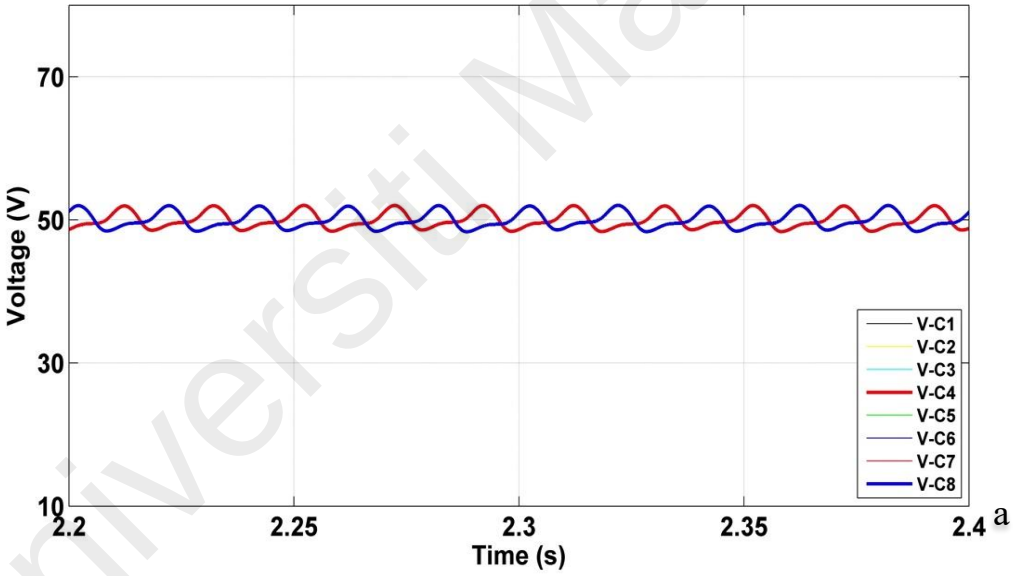



**Figure 5.5:** Waveform of upper and lower arm capacitor voltages.

Figure 5.6 shows the simulation of switching pulses diagram of 2500 *Hz* switching frequency carrier and the switching pulse of each of SMs in the arm. The switching carrier (2500 *Hz*) is generated from the adaptive carrier PDPWM in one cycle. It can be observed clearly that the real switching pulses of each of SMs are much lower than the carrier frequency. So that in hardware implementation, the switching losses in the IGBT is very low compared to conventional converter and the other multilevel converter.

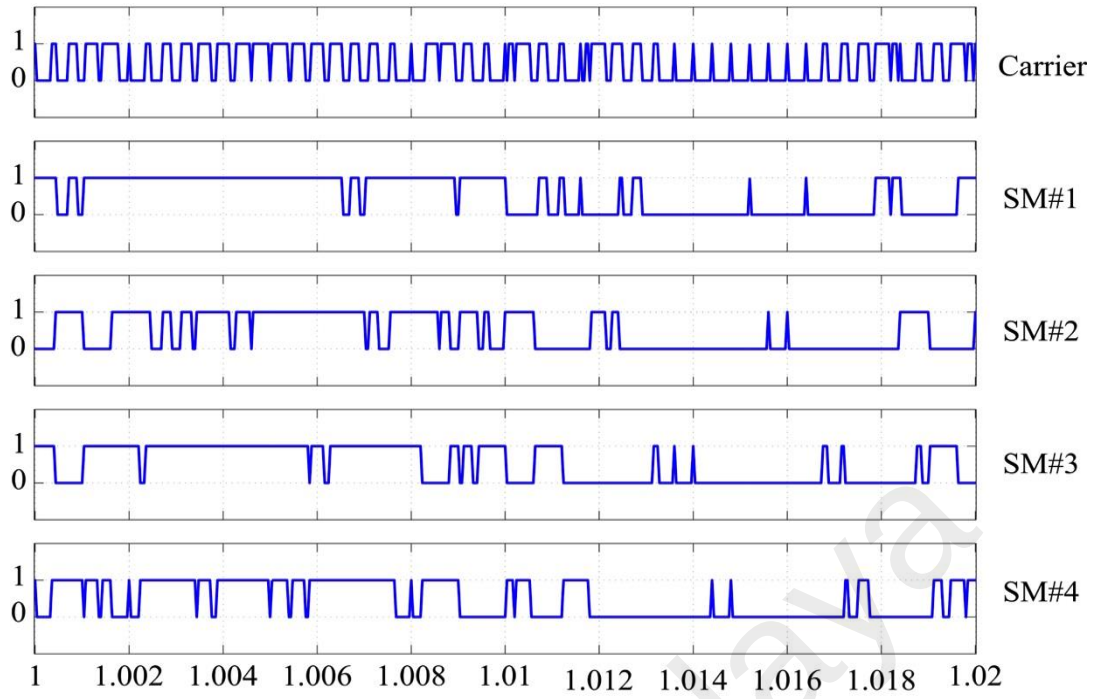



**Figure 5.6:** Pulses signals of switching carrier and SM#1-4 pulse signals in one cycle.

### 5.2.2 Fault State Operation

SM#4 at the upper arm is programmed to face the fault at 4 s to highlight the performance of the balancing control and proposed modulation technique. As shown in Figure 5.7, SM#4 at the upper arm and one of the SM at the other arm are bypassed. The remaining SMs must be rebalanced by the energy-based control to the new desired voltage ($V_{dc}/N; N = 3$). Thus, the overall characteristics of MMC do not change which is caused by no signal additional to the reference. Figure 5.8 shows the internal circulating current. A total of three SMs work on the upper and lower arms. Thus, the output level immediately becomes seven.

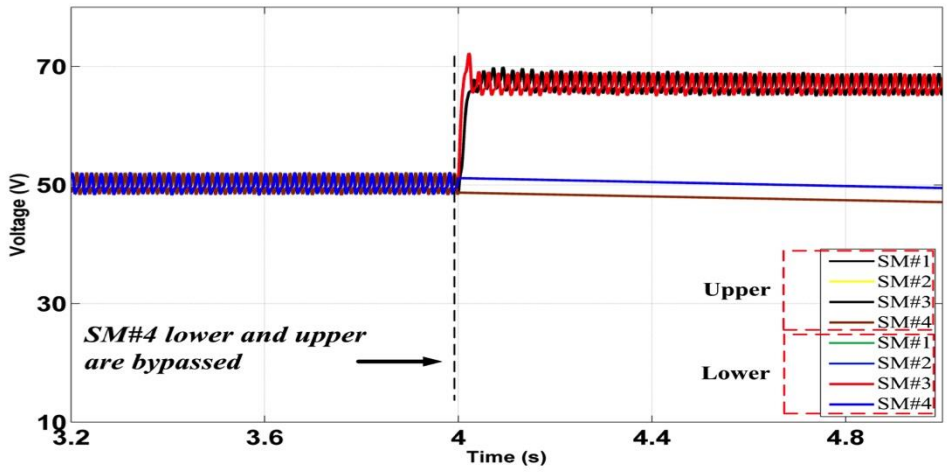



**Figure 5.7:** Bypassed waveform SM#4 at the upper and lower arms.

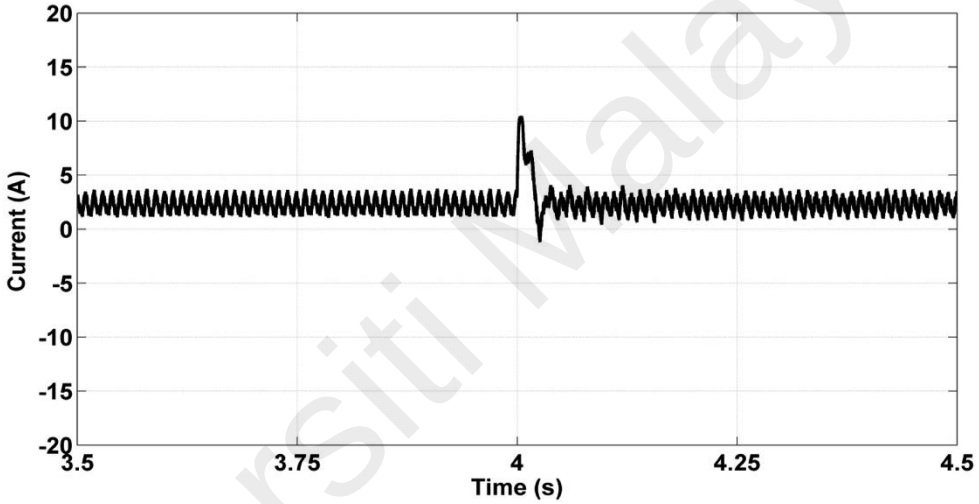



**Figure 5.8:** Circulating current waveform during failure of SM#4.

The faulty signal from SM#4 at the upper arm changes the staircase signal at 4 s. The change of the staircase signal influences the waveform of the adaptive carrier of PDPWM. Figure 5.9 shows the change of the adaptive carrier. Thus, the proposed technique does not interrupt the upper and lower arm reference signals and the reference signals are well adapted with a new carrier level. Figure 5.10 shows the corresponding pulses sent into each of the SM when the SM#4 is under fault. When the fault occurs in the SM#4, the control algorithm automatically gives zero-pulse to the SM#4 and activates the bypassed-mode for SM#4. The rest of healthy SMs, which are SM#1 – SM#4 remain ON in the

short time where it has purpose to rebalance the rest of healthy SMs to the new output level.

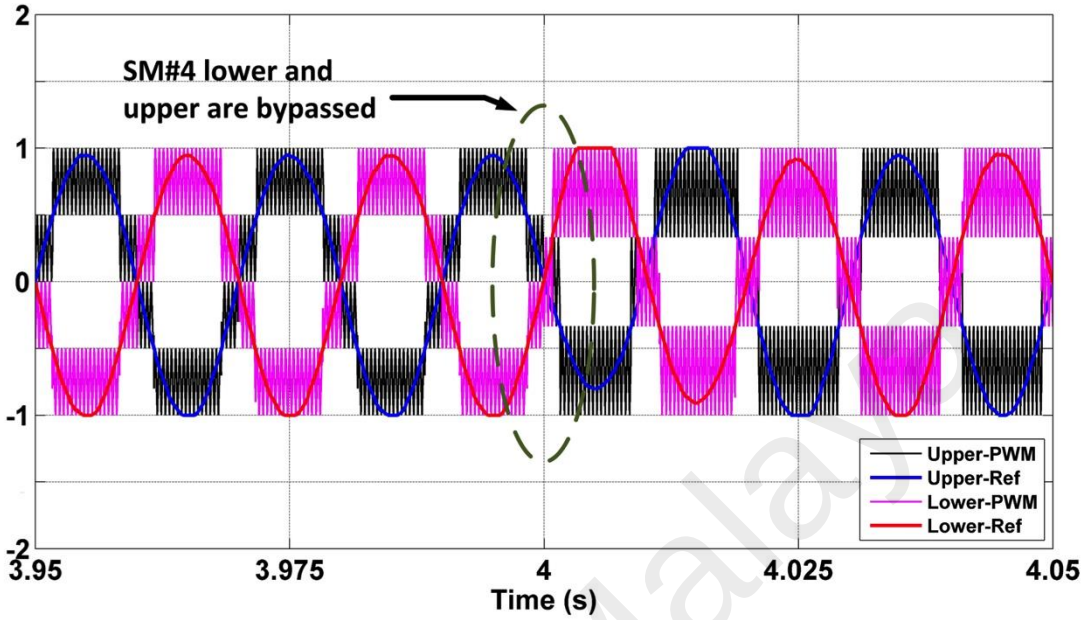



**Figure 5.9:** Change of adaptive carrier waveforms when SM#4 at lower arm is failure (bypassed).

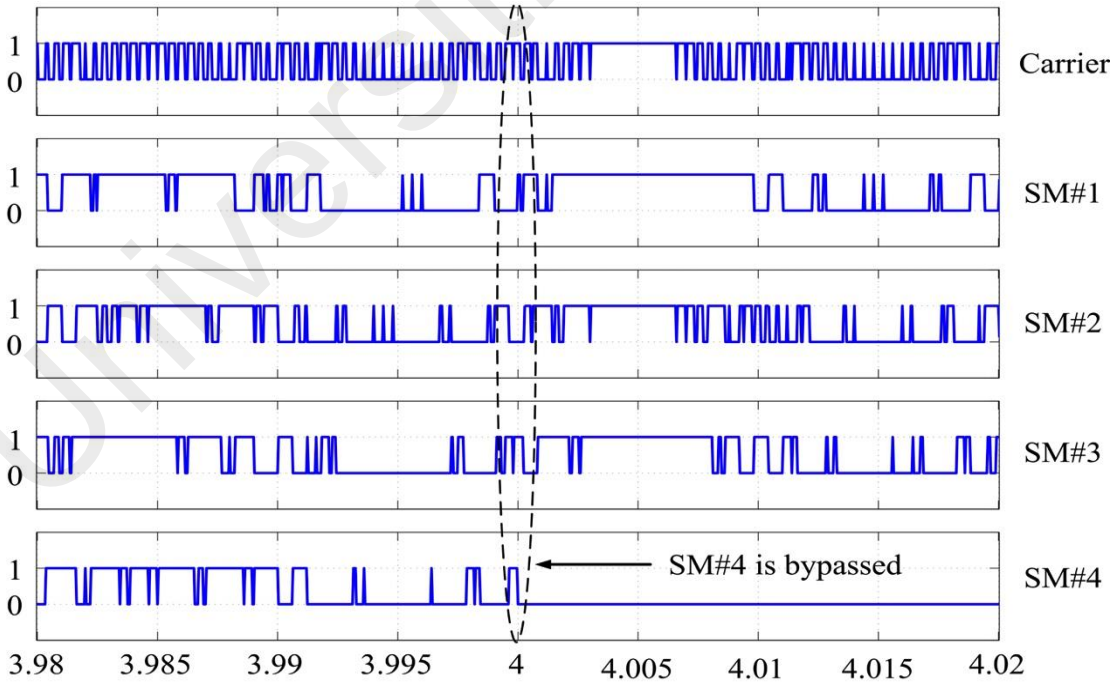



**Figure 5.10:** Pulses signals of switching carrier and SM#1-4 pulses signal when SM#4 is bypassed.

After clearing the fault, the SM#4 is re-inserted into the arm at 8 s. At this time, SM#4 in the lower arm and other SMs in the upper arm are reactivated. The voltage balancing and energy-based controls are recalculated with $(V_{dc}/N; N = 4)$ for all the capacitor voltages. All the capacitor voltages in the SMs after clearing the fault are rebalanced to the desired voltage $(V_{dc}/N; N = 4)$, as shown in Figure 5.11. This change also affects the internal circulating current to rebalance all the SMs, as shown in Figure 5.12. The change of the staircase signal influences the waveform of the adaptive carrier of PDPWM, as shown in Figure 5.13. Figure 5.14 shows that when the fault is eliminated, the SM#4 starts to receive the pulses and reaches to the desired voltage again.

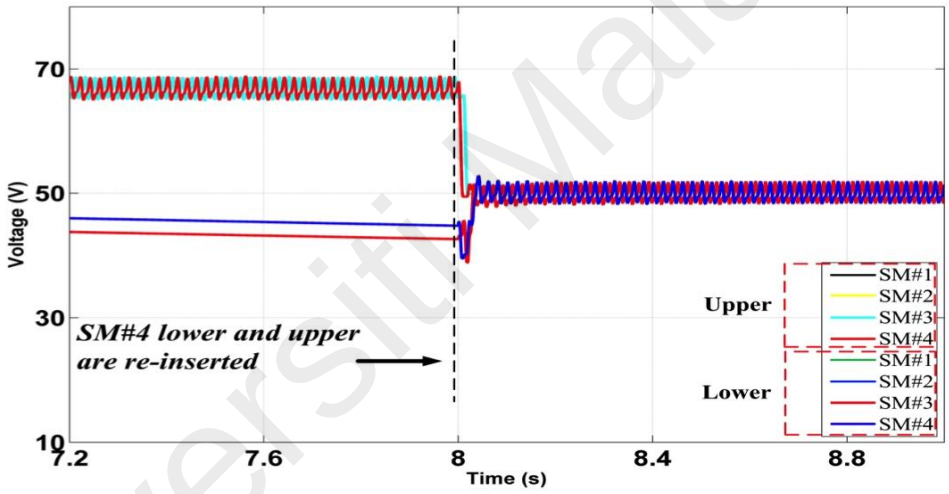



**Figure 5.11:** Waveform of the upper and lower arms after SM#4 is re-inserted.

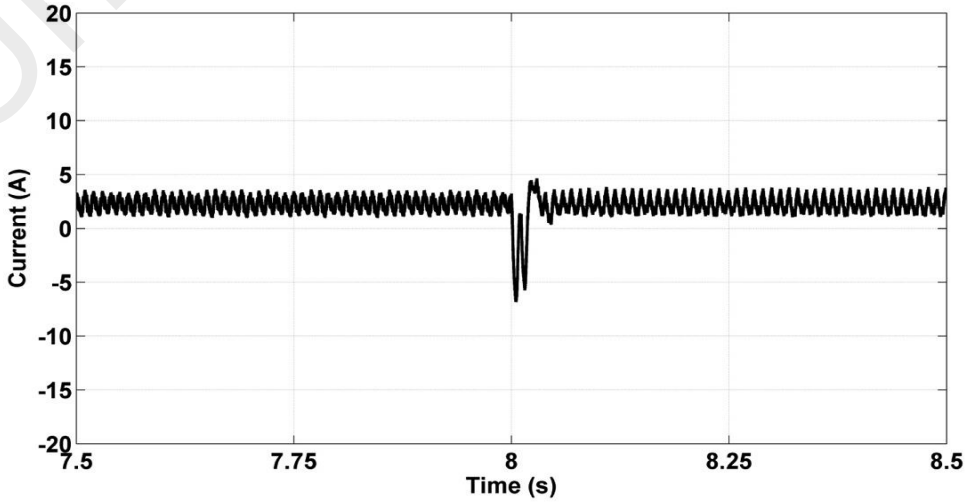



**Figure 5.12:** Circulating current waveform after re-inserting SM#4.

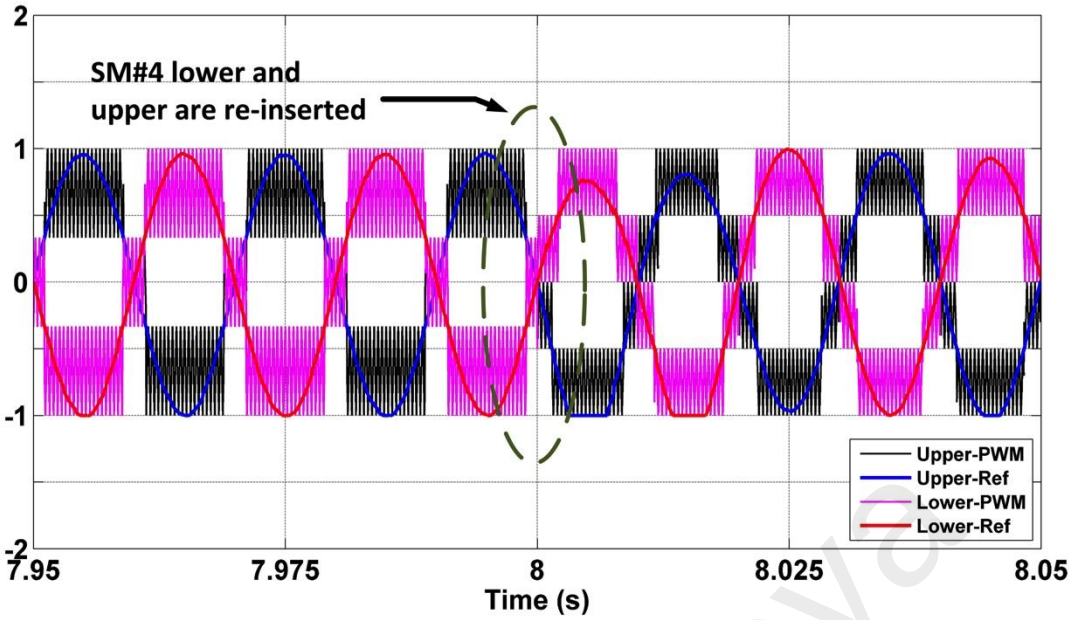



**Figure 5.13:** Change of adaptive carrier waveforms when SM#4 at the lower arm is re-inserted.

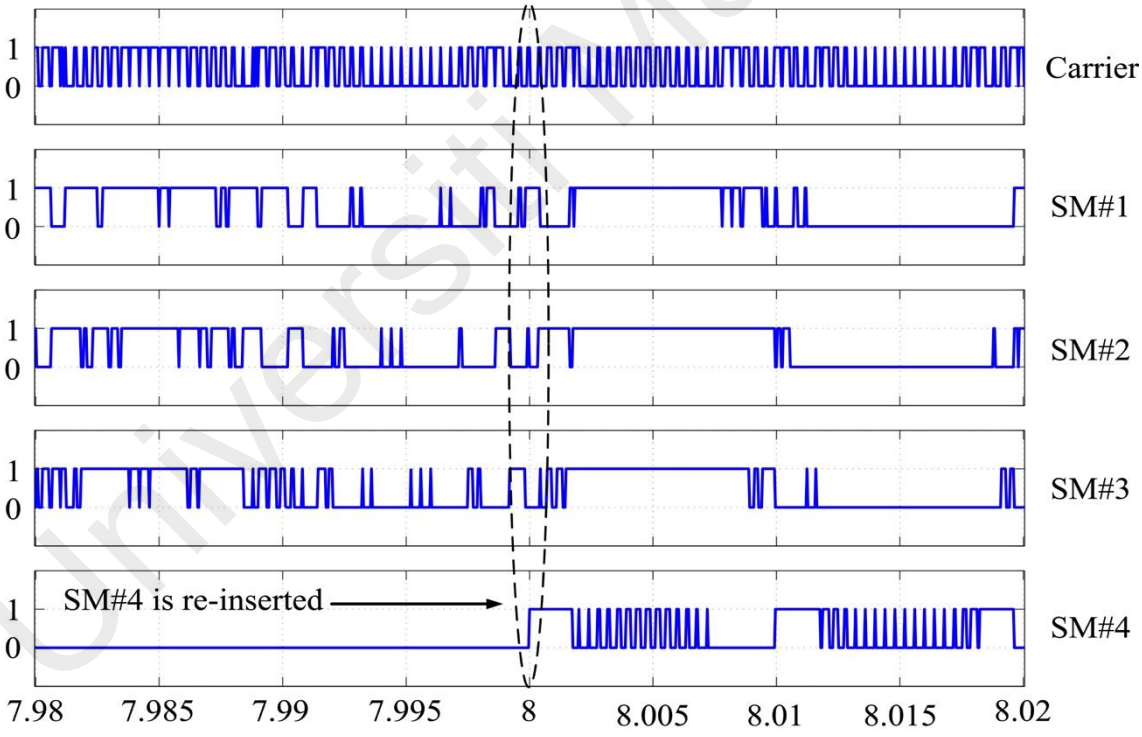



**Figure 5.14:** Pulses signals of switching carrier and SM#1-4 pulse signals when SM#4 is re-inserted.

Figure 5.15 and Figure 5.16 show the corresponding output voltage and output current of the MMC when the faulty SM#4 occured at 4 is bypassed. The level of the voltage changes from 9 level to 7 level and reaches normal state after one cycle. After clearing

the fault which means SM#4 is re-inserted at 8s, the output voltage and output current are showed in the Figure 5.17 and Figure 5.18. The level of voltage returns to 9 level from 7 level immediately.

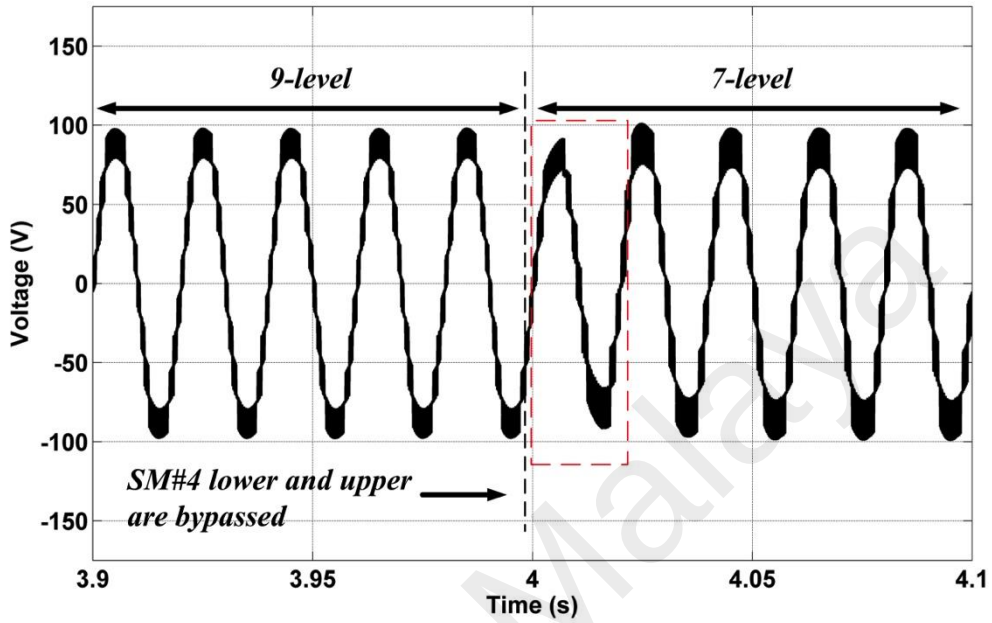



**Figure 5.15:** Output voltage before and after SM#4 at the upper and lower arms are bypassed at 4 s.

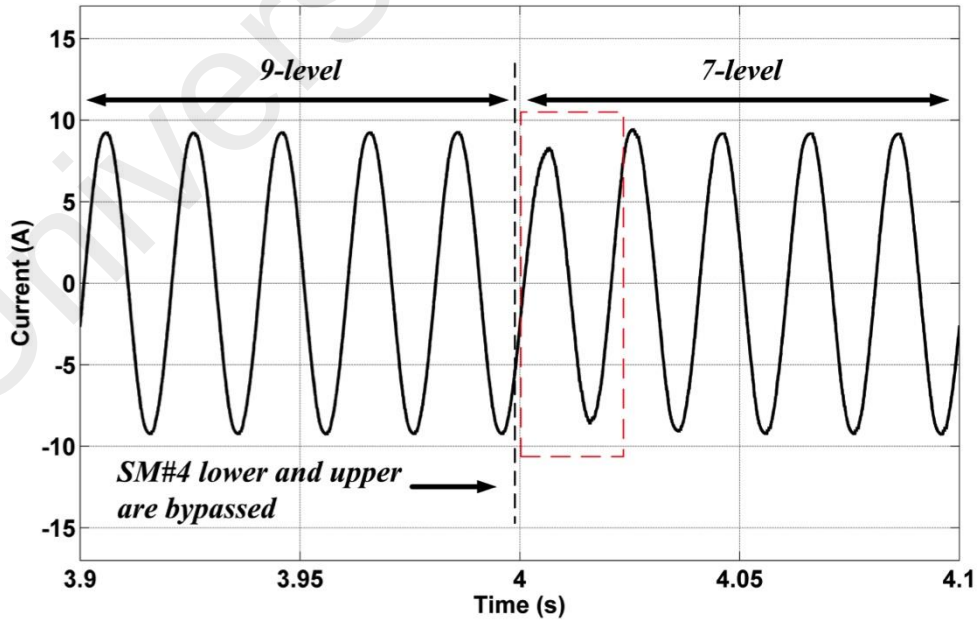



**Figure 5.16:** Output current before and after SM#4 at the upper and lower arms are bypassed at 4 s.

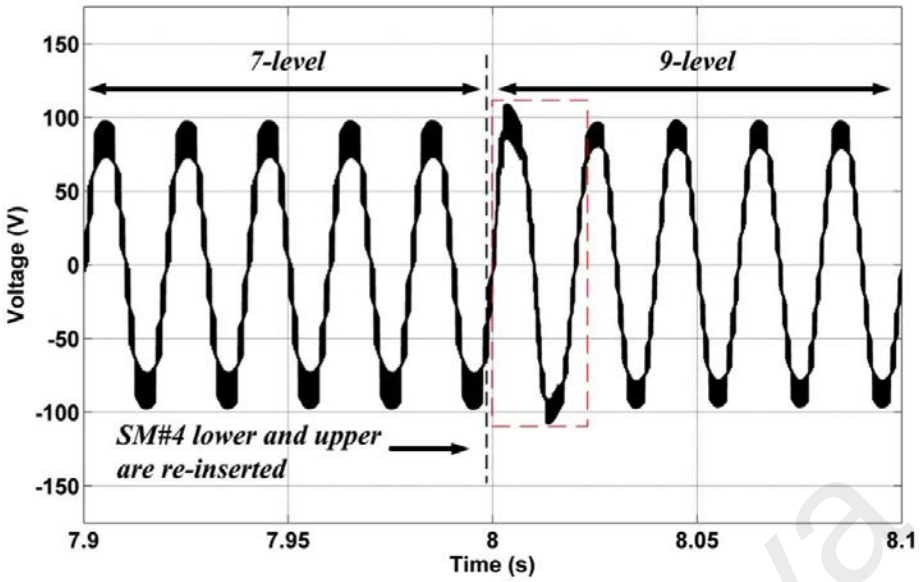



**Figure 5.17** Output voltage before and after SM#4 at the upper and lower arms are re-inserted at 8 s.

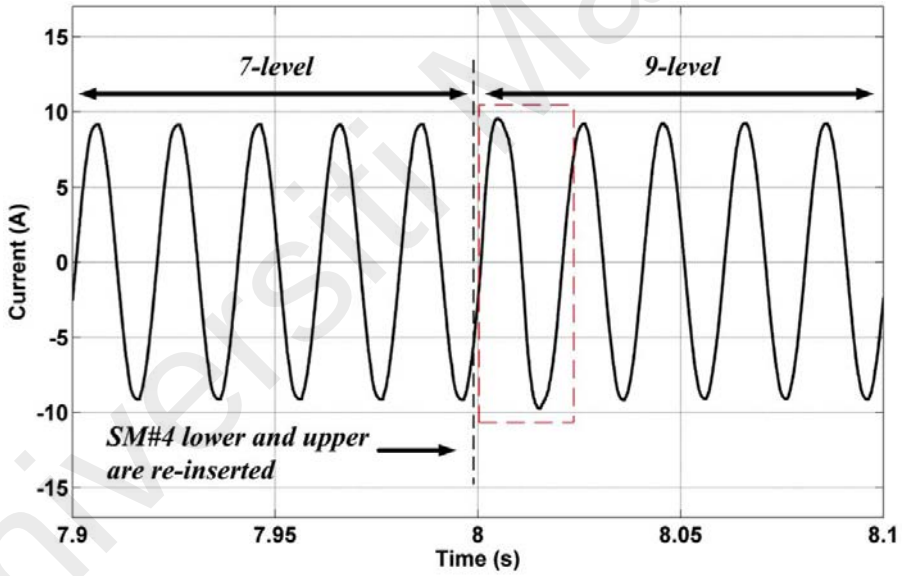



**Figure 5.18:** Output current before and after SM#4 at the upper and lower arms are re-inserted at 8 s.

## 5.3 Experimental Result

The prototype of single-phase MMC inverter is designed to verify the MMC topology with the proposed control scheme using the the same parameters as simulation as stated in Table 5.1. In this section, the prototype is tested and discussed to validate the proposed method in real implementations.

### 5.3.1 Experimental Setup

The single-phase MMC laboratory prototype inverter is shown in Figure 5.19. The resistive and inductive loads are connected to the prototype. The parameters used in the experiment are similar to those listed in Table 5.1. The DC-link voltage is directly generated by using the DC power supply TDK-Lamda. The control and modulation methods are programmed in a SpeedGoat Real-Time target machine with 0101 port. The flow chart of hardware implementation is shown in Figure 5.20. This chapter describes the design of all the hardware and controller component of the proposed MMC.

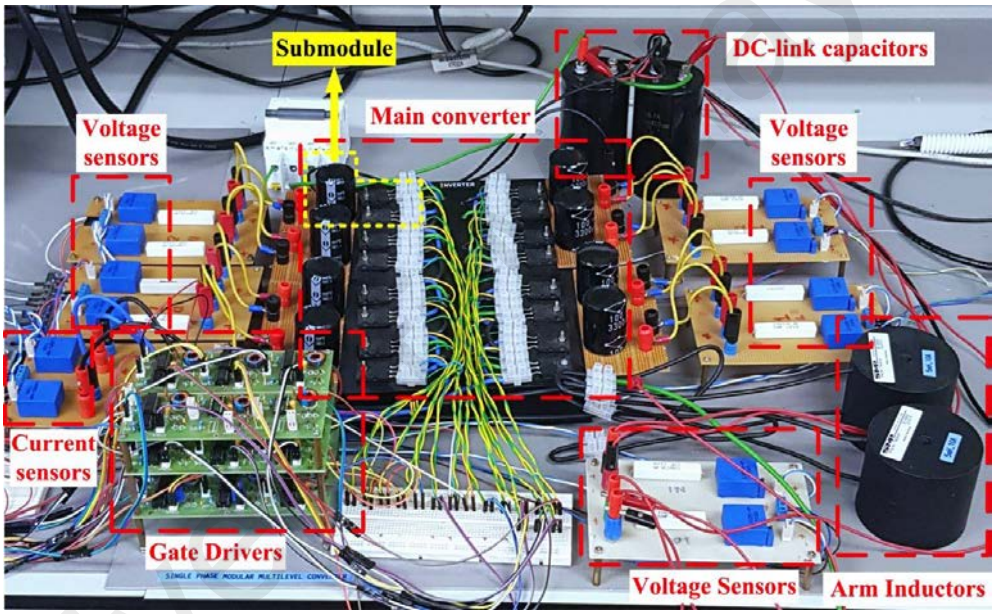



**Figure 5.19:** Experiment setup.

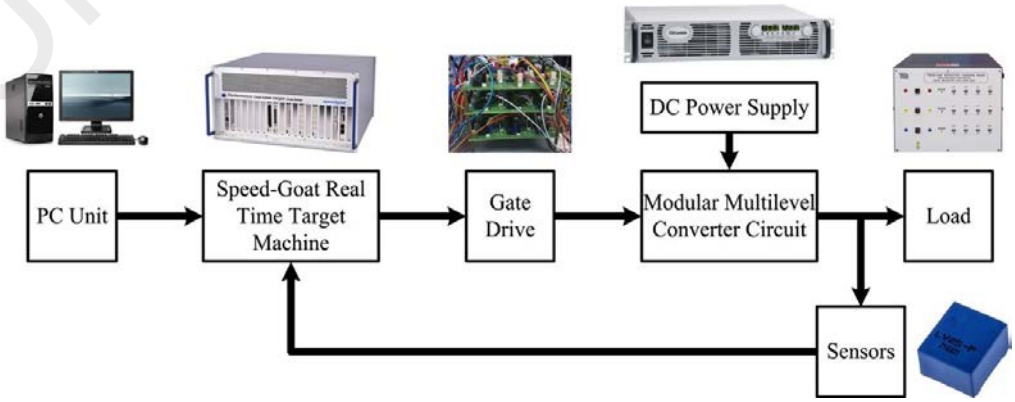



**Figure 5.20:** Flow chart of hardware implementation.

#### 5.3.1.1 Hardware Component of MMC

The feasibility of the Modular Multilevel Converter is verified using a prototype model consisting of gate drives, a SpeedGoat Real-Time Target Machine as controller unit, a personal computer to run the algorithm developed in MATLAB/Simulink, one isolated DC voltage source, 16 IGBT Switches, 8 capacitors, a heat sink, and an adjustable resistive-inductive load.

*(a)* ***IGBT, Capacitor, and Inductor***

IGBTs are the power switch devices that are selected for high voltage applications due to their performance for high power but having lower switching frequency performance compared to MOSFETs. IGBTs are completely off when the gate voltage are below the threshold value, normally in the range of $0 - 4\ V$. When the gate voltage reaches approximately $11\ V - 15\ V$, which is above that threshold value, the drain current starts to flow depending on the gate voltage and the rated value is obtained. There are 16-IGBTs for 4-SM in each arm being used in the hardware. The choice of IGBT voltage rating closely depends on the input voltage of the equipment in which it will be installed. The choice of the IGBT rating should consider the fault tolerance in which the IGBT can operate in safety margin. In this design, the IGBT voltage rating is at least two times higher than the rated voltage on a submodule due to a space for safety margin.

The capacitance of each SMs capacitor is 3300 $\mu F$ and the nominal voltage rating of each of SMs capacitor is $100\ V$. The choice of capacitor voltage rating also need to be selected based on the tolerance that given while designing the converter. In this design, the capacitor voltage rating is two times higher than the rated voltage on a submodule due to a space for safety margin. The converter is connected directly to $200\ V$ TDK-Lamda DC power supply. In the experiment, the inductance value of the arm inductors is 5 $mH$ with the internal resistance of each of the arm inductor is 0.2 Ω.

*(b)* ***Gate Driver***

A gate driver circuit needs to be designed to trigger the IGBT / MOSFETs based on the switching pulses generated from controller. The circuit of gate drive is shown in Figure 5.21, where three gate drive circuits are assembled in one set of PCB. The gate drive circuits have a low output impedance that are able to supply relatively large current to the IGBT in order to attain a switching speed of 50 $kHz$ or more.

An optocoupler is one of the most essential components in the gate driver circuit. It integrates a silicon phototransistor and an infrared light-emitting diode. The gate drive circuit consists of 2 inputs which are 5 $V$ DC input and 5 V input from the controller. The input signal from the controller is applied to the infrared light-emitting diode pins, while the 5 $V$ DC supply that already boosted to $11\ V - 15\ V$ is passed from the phototransistor pins. It is used to interface the logic circuit with the IGBT gate terminals in order to obtain the required level shifting.

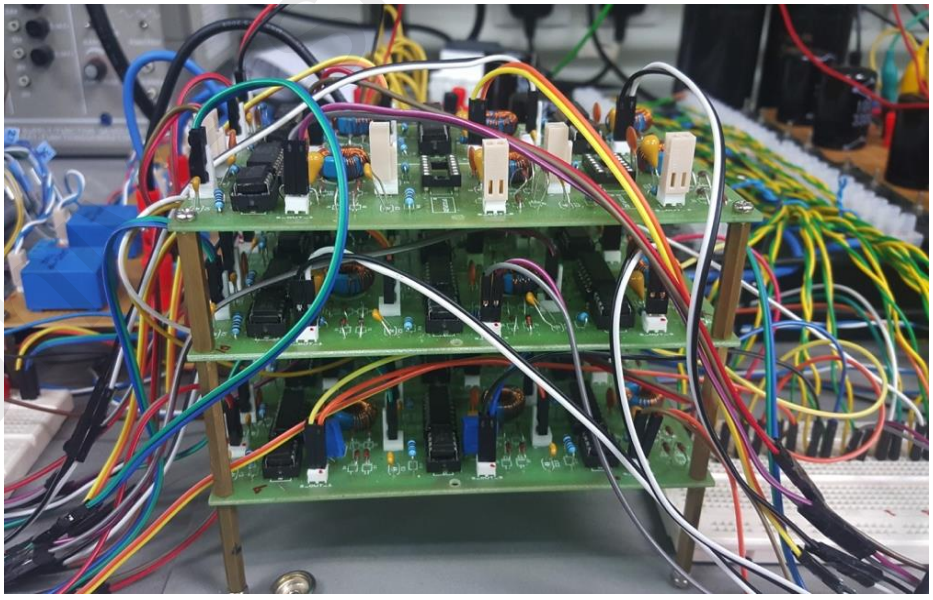


**Figure 5.21:** Gate driver circuit.

### *(c) Sensors*

Sensors are the basic component in the electrical circuit for sensing or reacting to a specific signal. Voltage sensor and current sensor are the conventional components to measure voltage and current. These components are needed in this converter to give feedback signal to the controller for taking action on selection of SMs, capacitor voltage balancing, and internal controller. These sensors are placed on all of the capacitor voltages in the arm and the arm currents. LV25-P voltage sensor and LA25-NP current sensor are used in the hardware setup. Voltage sensors for every SMs and current sensors for upper and lower current are shown in Figure 5.22 and Figure 5.23, respectively.

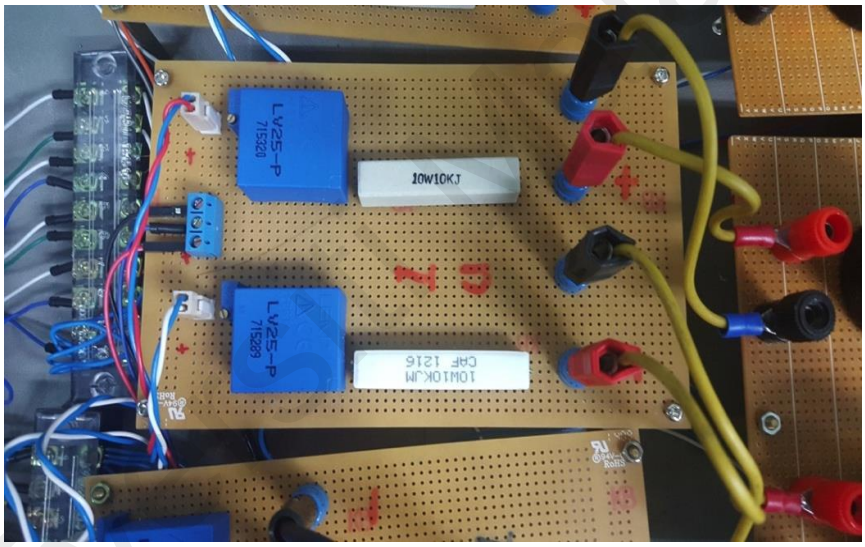



**Figure 5.22:** Voltage sensor circuit.

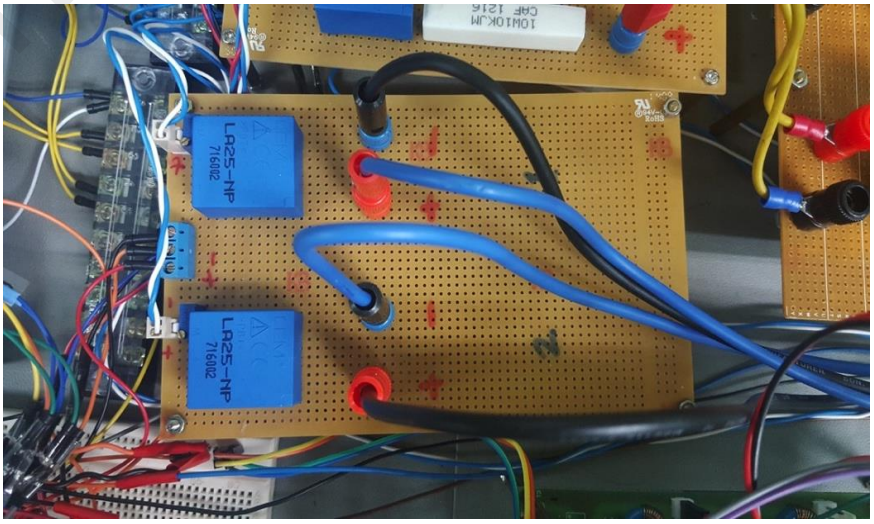



**Figure 5.23:** Current sensor circuit.

### 5.3.2 Normal State Operation

The converter can work with 2 (two) types voltage level, namely 2N + 1 and N + 1, as mentioned in Chapter 4. Figure 5.24 and Figure 5.25 show the steady-state waveform of the output voltage with different voltage level without connecting load, wherein all the capacitor voltages are well balanced at 50 V with a particularly small ripple, as shown in Figure 5.26. By using 2N + 1 voltage level, the THD is generated smaller than N + 1 because more voltage level can be generated. However, this technique has more complexities to be controller, caused by each of arms are controlled independently.

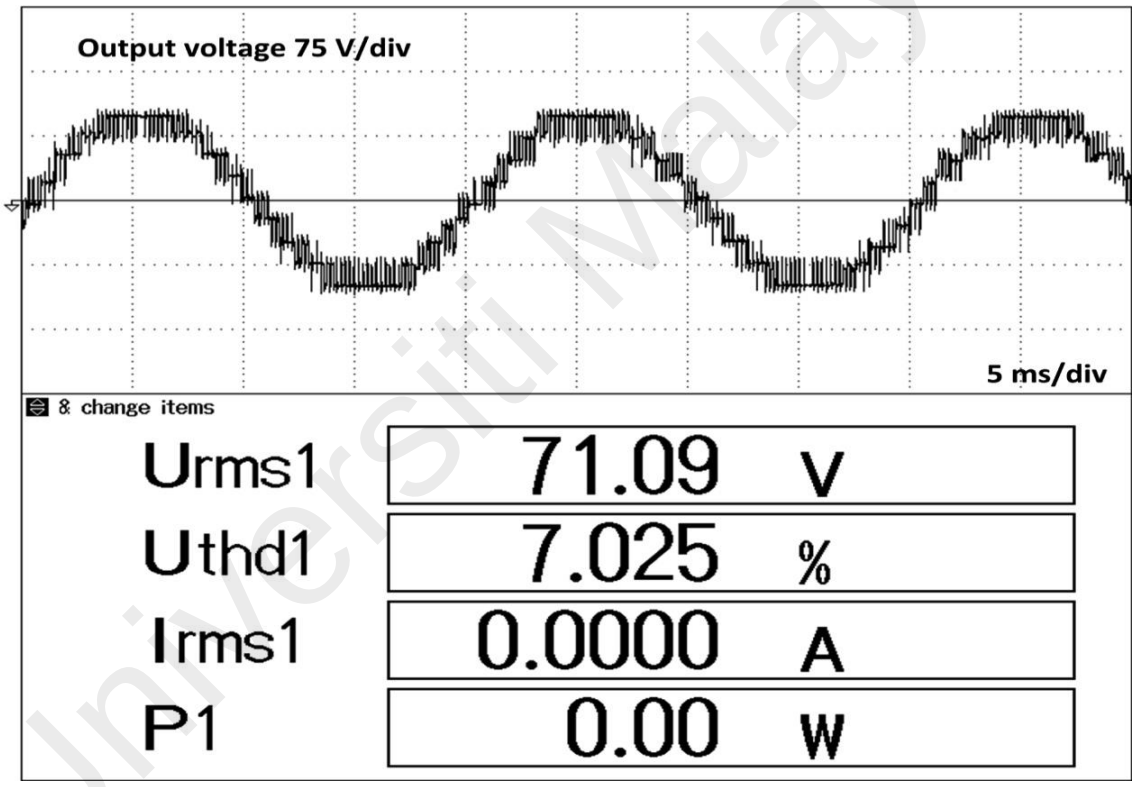



**Figure 5.24:** Output voltage of nine-level (2N +1 modulation) under normal state form measured by a power analyzer (75 V/div).

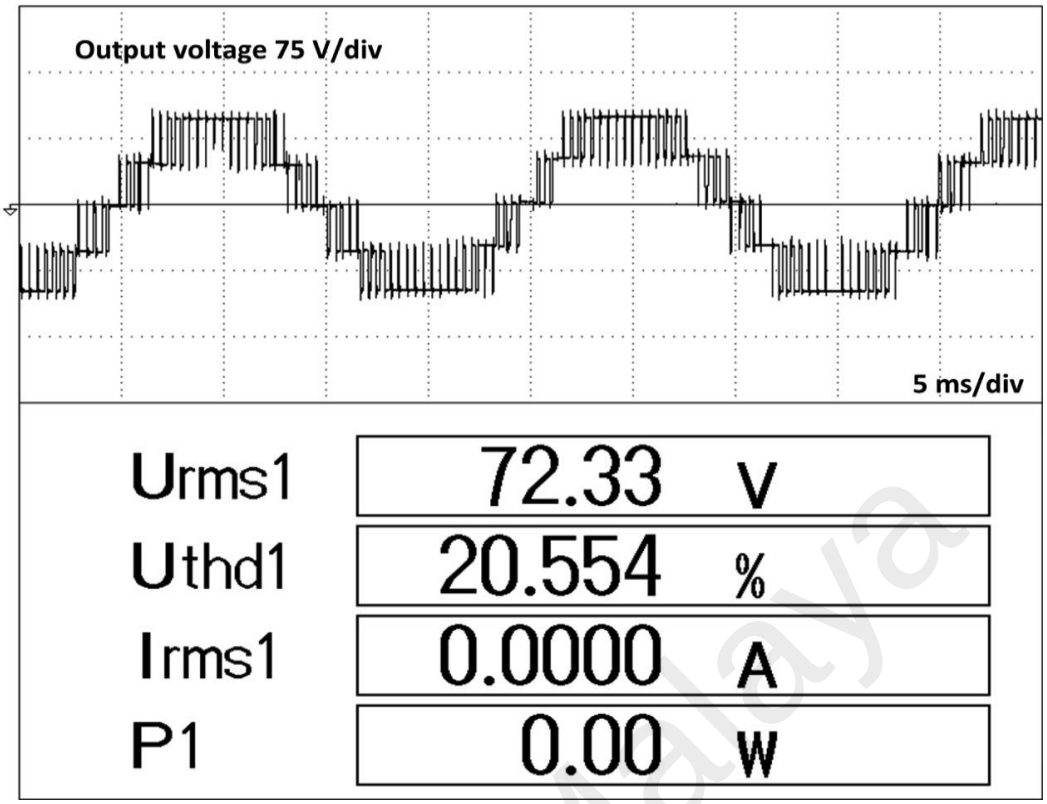



**Figure 5.25:** Voltage of five-level (N+1 modulation) under normal state form measured by a power analyzer (75 V/div).

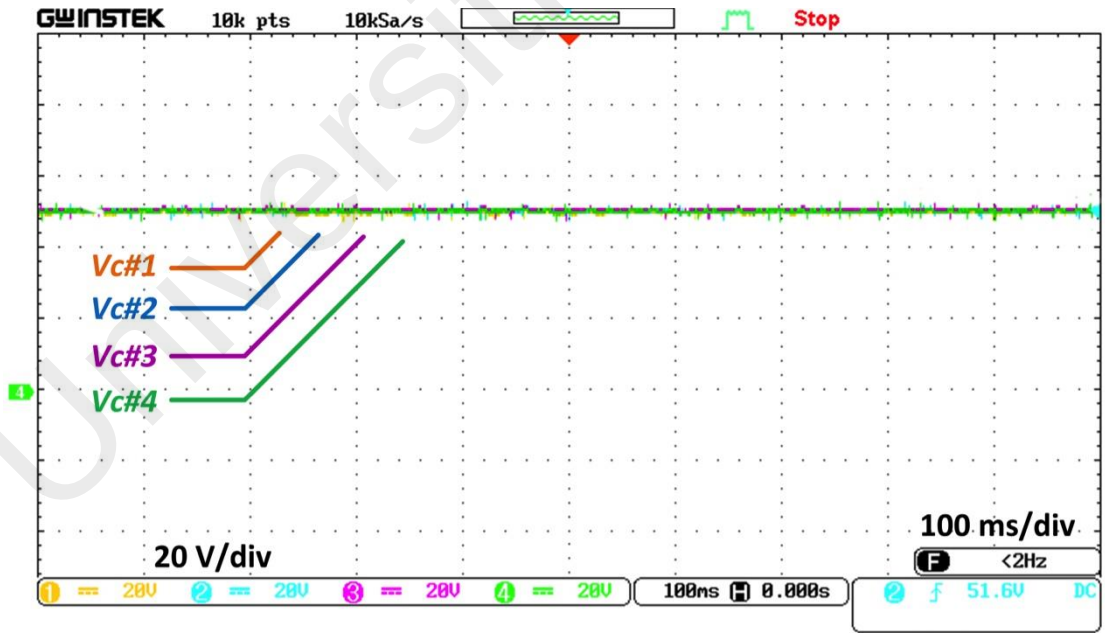



**Figure 5.26:** Lower arm capacitor voltages under normal state form measured by Gwinstek oscilloscope.

This study focuses more on 2N + 1 voltage level. Figure 5.27 and Figure 5.28 show the experimental steady-state waveforms of the output voltage and current when the resistive and inductive loads are connected, respectively. Once the resistive load is connected at terminal AC, the THD of the voltage significantly diminishes due to the influence of two arm inductors on the leg that work as internal current filters. Figure 5.29 and Figure 5.30 are experimental waveforms of the single-phase voltage and current during steps load change. The experimental results show the excellent performance of the MMC inverter control system.

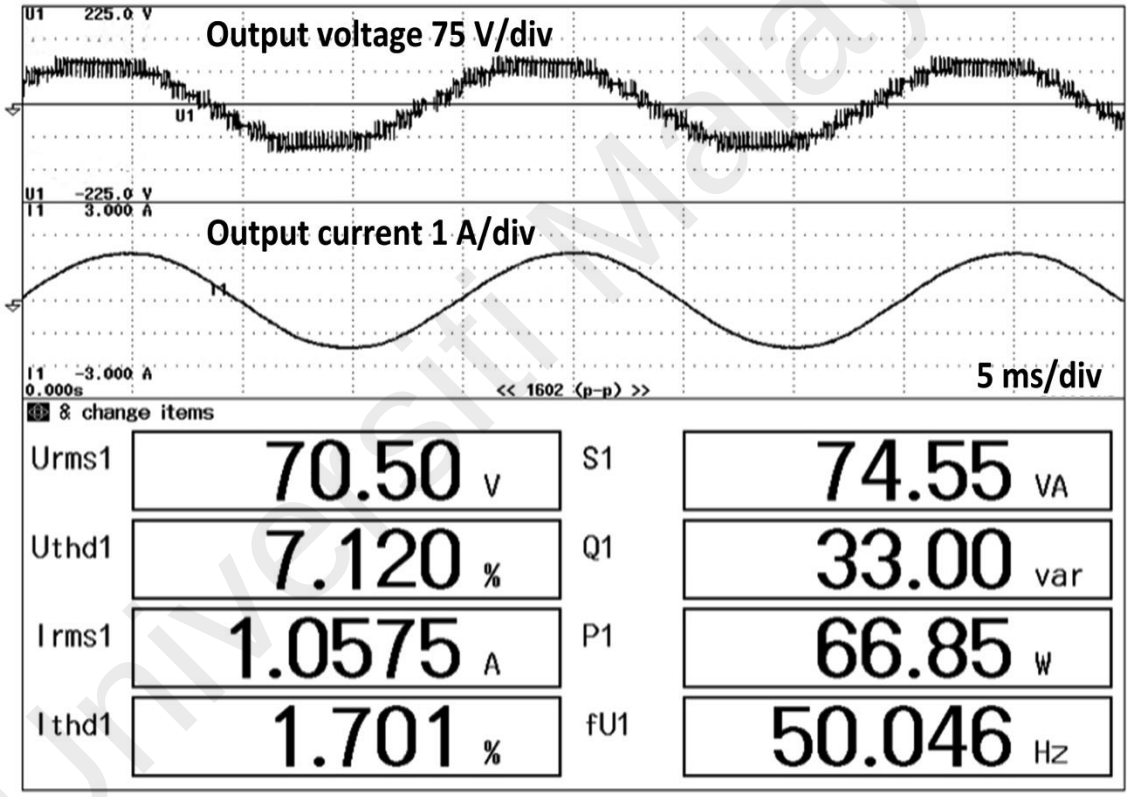



**Figure 5.27:** Output voltage and current using inductive load under normal state form measured by Power Analyzer (75 V/div and 1 A/div, respectively).

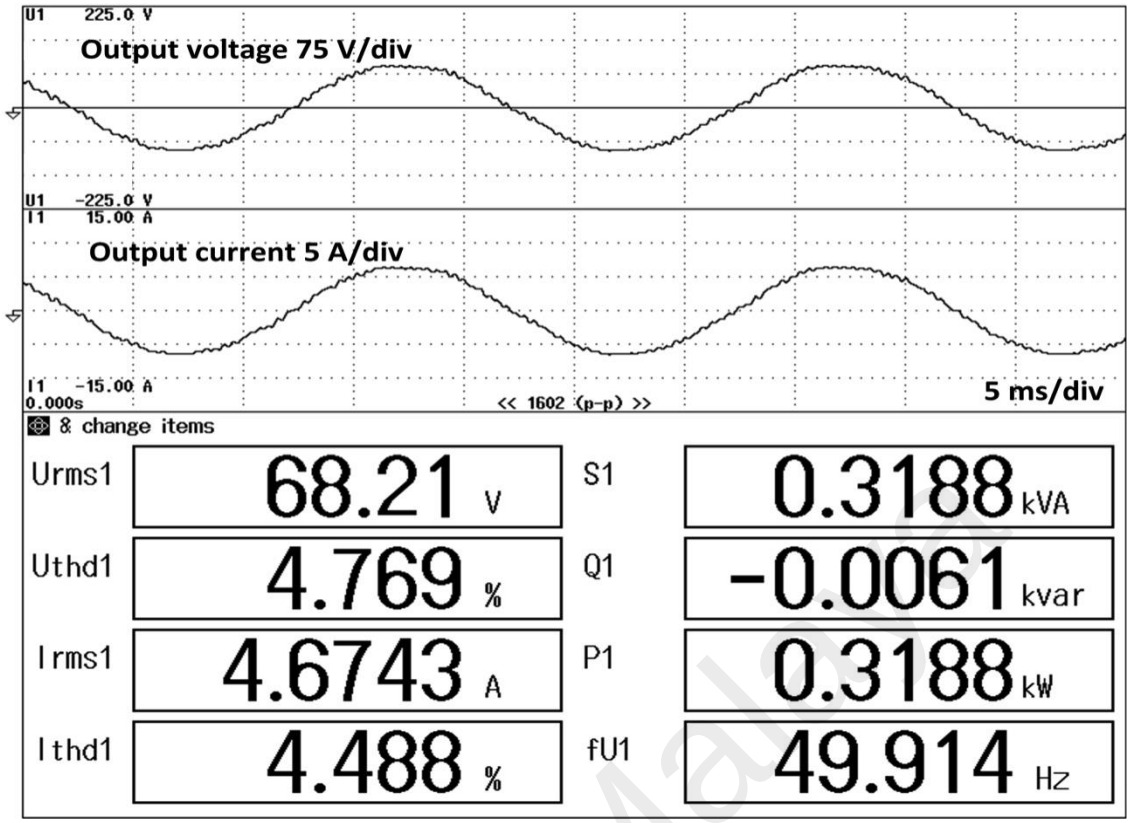



**Figure 5.28:** Output voltage and current using resistive load under normal state form measured by Power Analyzer (75 V/div and 5 A/div, respectively).

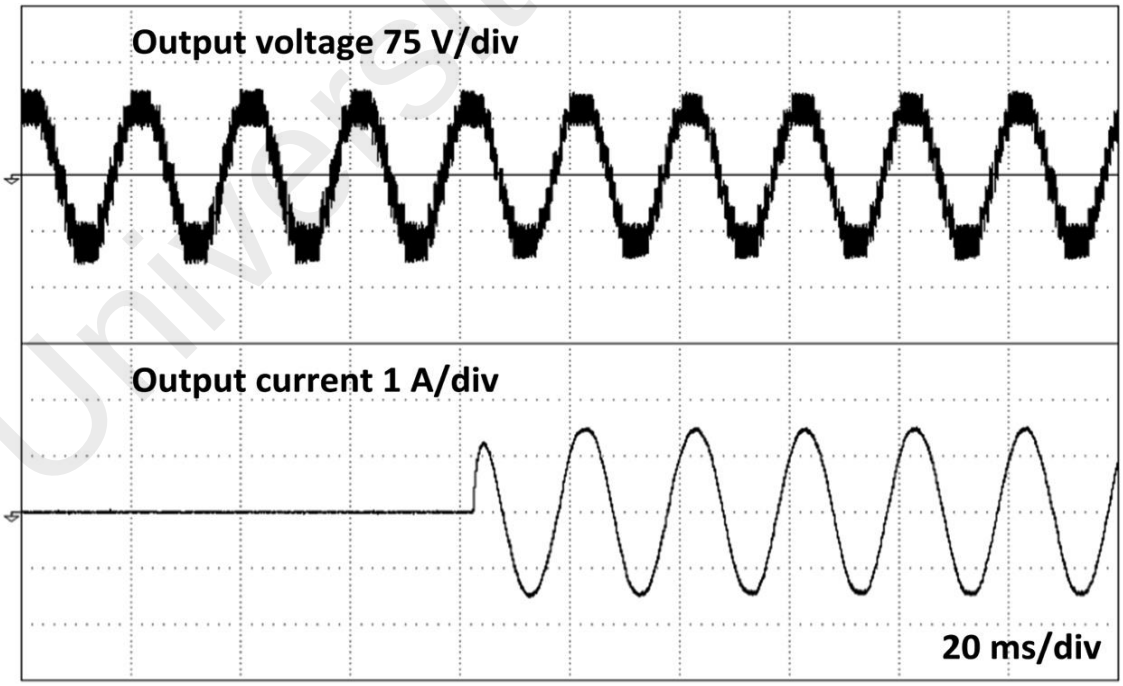



**Figure 5.29:** Output voltage and current with step increase of load measured by Power Analyzer (75 V/div and 1 A/div, respectively).

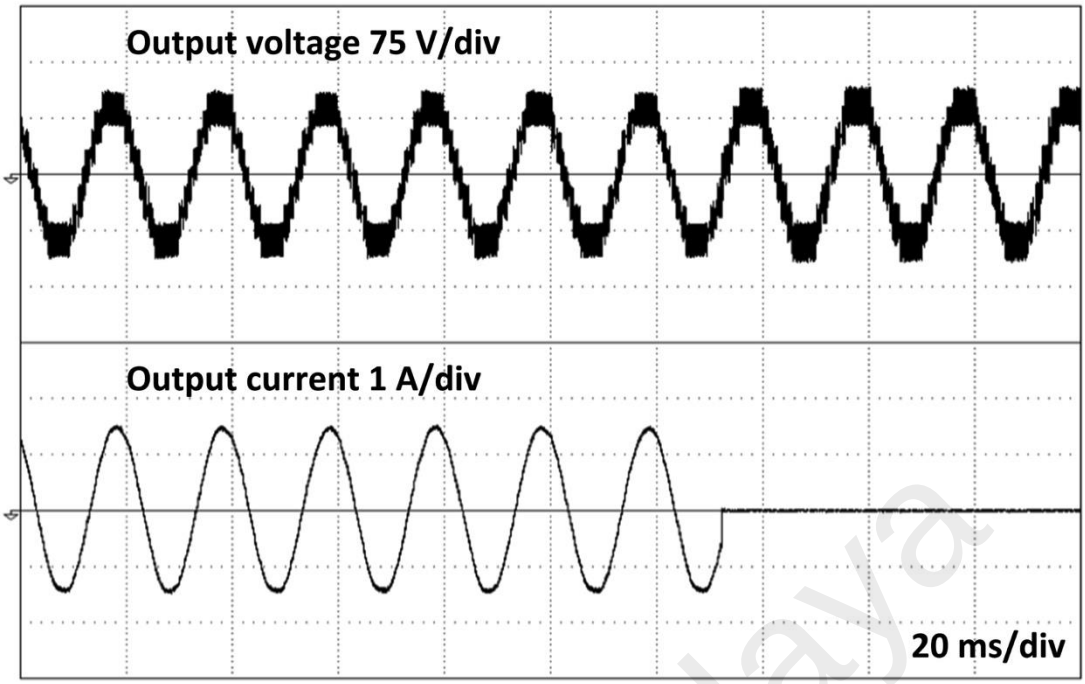



**Figure 5.30:** Output Voltage and current with step decrease of load measured by Power Analyzer (75 V/div and 1 A/div, respectively).

### 5.3.3 Fault State Operation

A fault signal from SM#4 at the lower arm is programmed in the system to highlight the balancing control and proposed internal fault tolerance. The system detects a fault signal from SM#4 at the lower arm, and the algorithm calculates the new number of SMs ($N$). Subsequently, the SM#4 at the lower arm and other SMs in the upper arm are bypassed. The new scale modulation signal is activated. Then, the remaining SMs are recharged at the new desired voltage ($V_{DC}/N; N = 3$). The output voltage, current, and recharge capacitor voltages during a fault are shown in Figure 5.31 and Figure 5.32. The voltage output waveform eventually becomes normal.

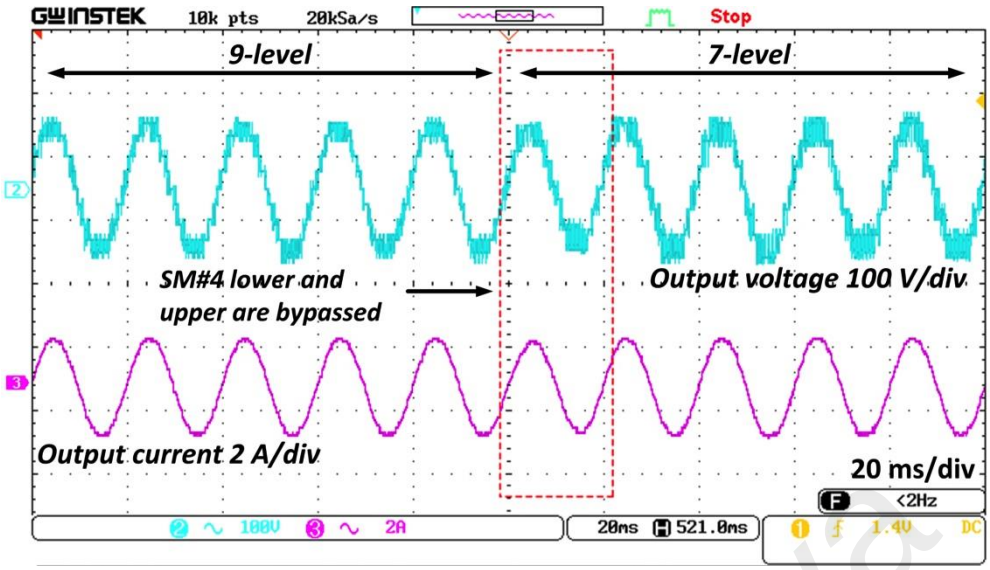



**Figure 5.31:** Output voltage and current before and during SM#4 failure (100 V/div and 2 A/div, respectively) measured by Gwinstek oscilloscope.

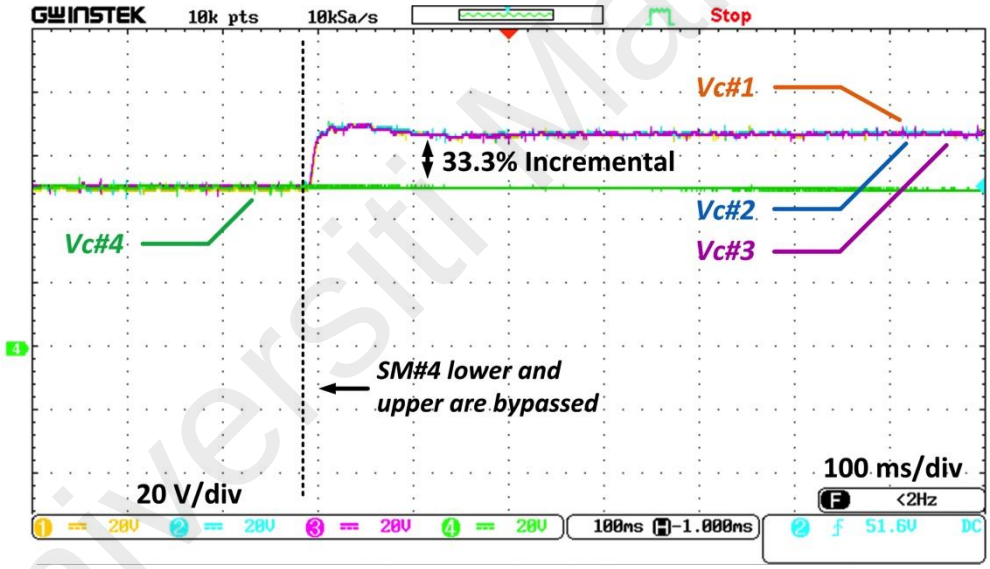



**Figure 5.32:** Bypassed waveform SM#4 at the lower arm (20 V/div) measured by Gwinstek oscilloscope.

From the simulation and experimental result shown in Figure 5.7 and Figure 5.32, the healthy SMs increase by 33.3% from the normal condition. This condition may cause a problem when designing the converter for selecting the tolerance of the capacitor and IGBT rating. The rest of healthy SMs can reach percentage of tolerance to 100%, if the used IGBT is not supported the margin of percentage, the converter is not pratical anymore to be operated. However, for a larger number of SM, this tolerance can be

decreased significantly. The percentage of tolerance for redundancy calculated by equation 4.6 is given in Table 5.2

**Table 5.2: Redundancy Tolerance**

| No of SM fault | Tolerance | | | |
|---|---|---|---|---|
| | N = 4 | N = 5 | N = 15 | N = 44, (Zhou et al., 2014) |
| 1 | 33.33% | 25% | 7.14% | 2.32% |
| 2 | 100% | 66.67% | 15.38% | 4.76% |

Figure 5.33 and Figure 5.34 show the performance after clearing the fault, wherein SM#4 is re-inserted to the converter. The SM#4 capacitor voltage is rebalanced, and the other capacitor voltages are automatically readjusted to the same voltages ($V_{DC}/N; N = 4$).

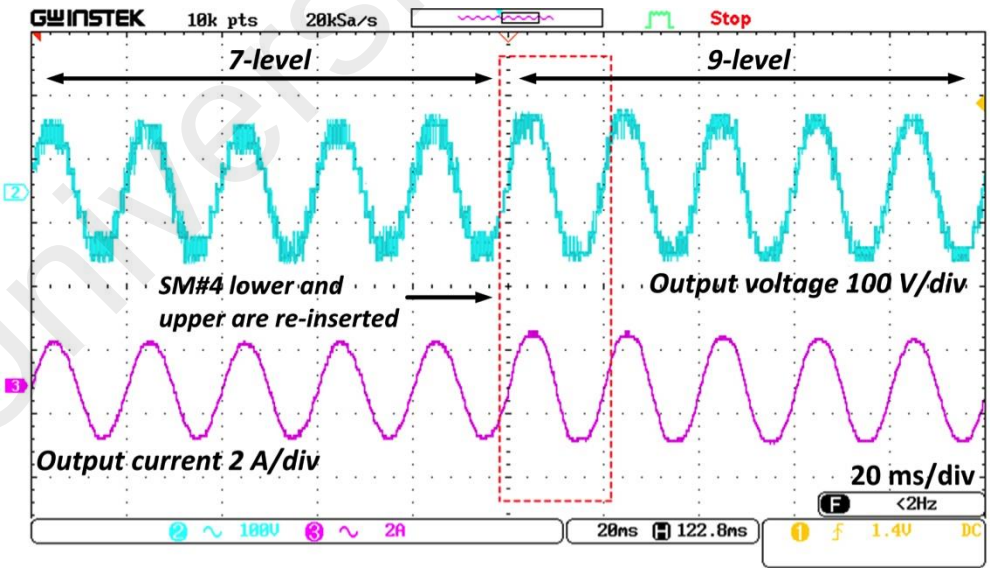



**Figure 5.33:** Output voltage and current during and after the failure of SM#4 at the lower arm (100 V/div and 2 A/div, respectively) measured by Gwinstek oscilloscope.

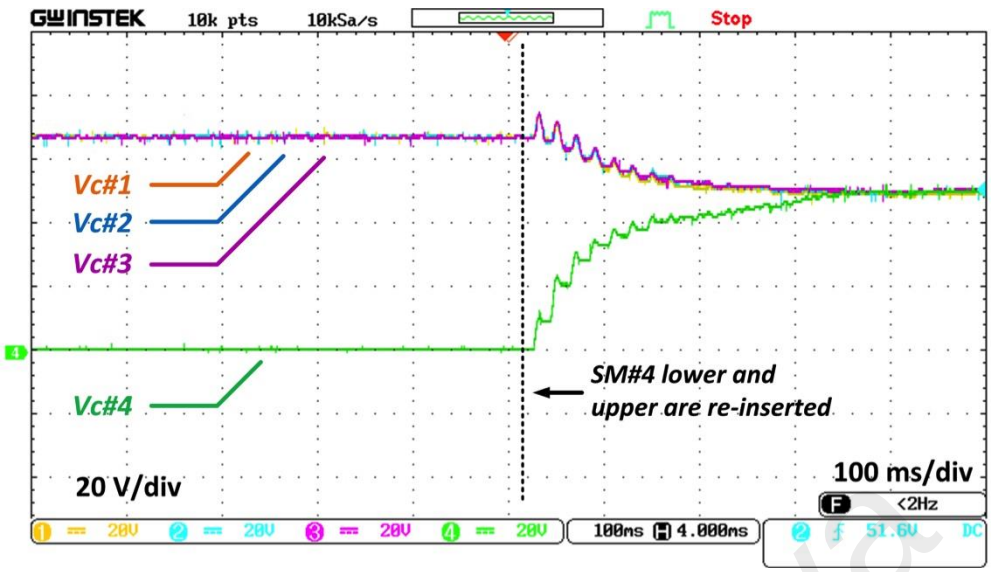



**Figure 5.34:** Waveform SM#4 of the lower arm is inserted again (20 V/div) measured by Gwinstek oscilloscope.

Figure 5.35 shows the influence of the recharge capacitor voltage to the new desired voltage on the circulating current. This phenomenon occurs because the DC-side needs to inject current to energyze the remaining capacitors that are controlled by the energy-based controller. As shown in Figure 5.36, when the fully discharged SM#4 at the lower arm is activated, the upper and lower currents start fluctuating due to the voltage difference between SM#4 at the lower arm and the other SMs. The energy-based controller is used to minimize the oscillation and regulate the imbalance condition among the SM voltages. This fluctuation can be reduced by externally charging the failure SM to the desired voltage before inserting to the arm. The upper and lower currents can be diminished by increasing the number of SMs in the MMC. This condition occurs because the input voltage is equally divided by the number of SMs.

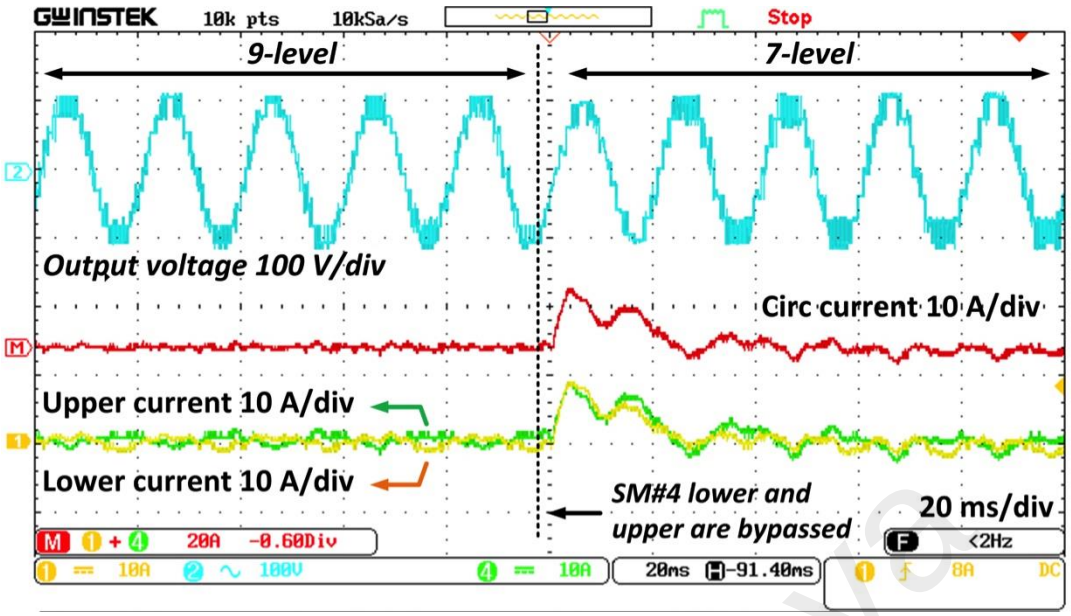



**Figure 5.35:** Output voltage, circulating current, and upper and lower arm current waveforms under lower SM#4 failure (100 V/Div, 10 A/Div, 10 A/Div And 10 A/Div, respectively) measured by Gwinstek oscilloscope.

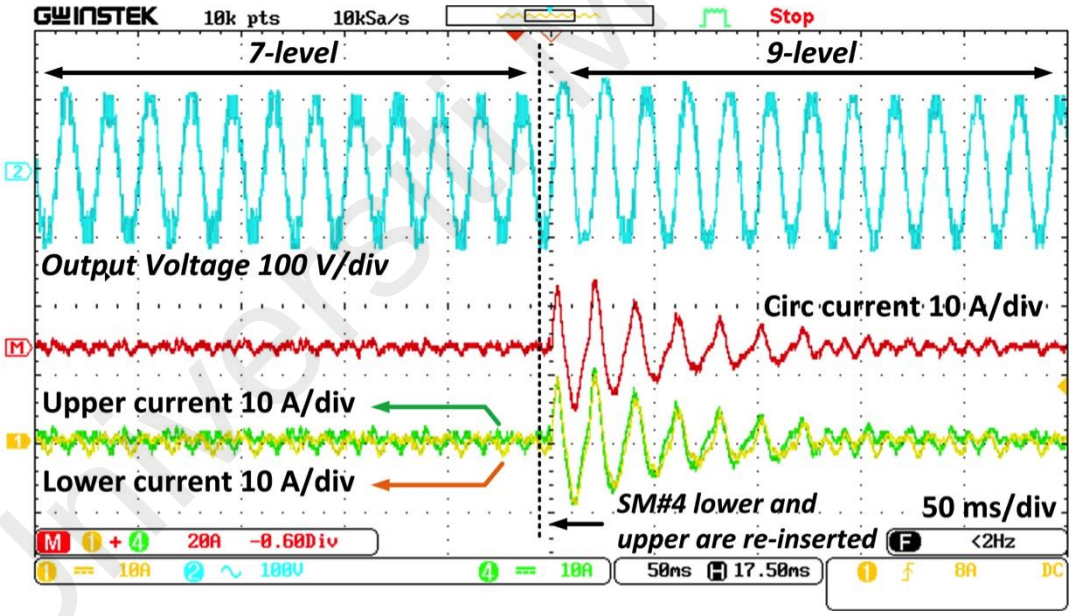



**Figure 5.36:** Output voltage, circulating current, and upper and lower arm current waveforms when SM#4 at the lower arm is re-inserted (100 V/Div, 10 A/Div, 10 A/Div And 10 A/Div, respectively) measured by Gwinstek oscilloscope.

## 5.4 Comparison of Fault-tolerant Method Under SM Failure

A comparison between the proposed method and the other methods presented in the literature, which involves a broad range of features, is presented in Table 5.3. There are three main strategies to overcome the failure of SM, which are reserved / spare redundant SM, redundancy tolerance on SM, and without redundant SMs. Reserved SMs require extra spare SM, which used when the fault happens. However, reserved SM will cause an increase in the volume, cost of the converter and taking time to recover the fault due to charging time on the spare SM capacitor. Redundancy tolerance on SM is suitable for large number of SMs where the increasing number of SM will reduce the tolerance percentage of redundancy. In (S. Kim et al., 2018), the authors proposed fault-tolerant without redundant SM, where it will not increase the cost and volume of the converter. However, this method negates the pulses for the failure SM by injecting zero-sequence or changing the direction of pulses in order to keep the capacitor voltages remain the same. Consequently, this method has low performance on the output side.

The proposed method has a low computational burden by using only one single carrier that can be adapted immediately with the new level-number when an SM is under a fault. This proposed method also practically reduces the complexity of the implementation of the PDPWM modulation technique. Since this method is implemented using symmetric operation to maintain the symmetry of arm voltage, it is suitable for a large number of SM. On the other hand, the conventional PDPWM and CPS-PWM use multiple carriers for the multilevel converters where the algorithm need to modified all the carriers. In MMC, one carrier deputizes one SM, which means a large number of carriers are required for a large number of SMs leading to an increase the computational burden as well as complexity to overcome the submodule failure. In CPS-PWM, the phase-shift between all the carriers need to be re-adjusted to isolate the faulty SM.

**Table 5.3: Comparison of Fault-tolerant Method Under SM Failure**

| Method | Reserved Redundant SM | Redundancy Tolerance (SM Tolerance) | Modulation Technique | Performance on the fault | | Computational burden | Hardware Cost |
|---|---|---|---|---|---|---|---|
| Proposed by (Choi et al., 2016; Farias et al., 2018a) | No | Yes | CPS-PWM | High | Recovery : Fast<br>Circulating current : Good<br>Out voltage: Good | High | Low (for large No. of SM) |
| Proposed by (D. H. Kim et al., 2015; Gaoren Liu et al., 2015) | Yes | No | NLM | High | Recovery : Slow<br>Circulating current : Good<br>Out voltage: Very good | High | High |
| Proposed by (Abdelsalam et al., 2017) | No | Yes | CPS-PWM | High | Recovery : Fast<br>Circulating current : Good<br>Out voltage: Good | High | Low (for large No. of SM) |
| Proposed by (S. Kim et al., 2018) | No | No | CPS-PWM | Low | Recovery : Fast<br>Circulating current : Good<br>Out voltage: Bad | High | Low |
| Proposed by (Mei et al., 2016) | No | No | CPDPWM | Medium | Recovery : Fast<br>Circulating current : Good<br>Out voltage: Bad | High | Low |
| Proposed by (Yin et al., 2019) | No | Yes | PDPWM | High | Recovery : Fast<br>Circulating current : Good<br>Out voltage: Good | High | Low (for large No. of SM) |
| **Proposed Method** | **No** | **Yes** | **Adaptive Carrier PDPWM** | **High** | Recovery : Fast<br>Circulating current : Good<br>Out voltage: Good | **Low** | **Low (for large No. of SM)** |

# CHAPTER 6: CONCLUSION AND FUTURE WORK

## 6.1 Conclusion

The developments of new technologies and power electronics devices in the 21th century have boosted the concentration in smart electric power systems. As a new technology conversion device, multilevel converters have features of lower frequency, less voltage $dV/dt$ rates, less harmonics and more reliability. These features make the multilevel converters more attractive and suitable for electrical machines, medium and high voltage applications. As part of multilevel converter topologies MMC topology can accommodate any possible power conversion functions, and capable of reaching any voltage, current and power levels using identically rated modules. Then, the hierarchical structure and energy storage capability based on the embedded capacitor within each module can make this topology superior to other topologies and a promising topology for HVDC. The model of MMC is designed and analyzed using MATLAB/Simulink.

Since the design of the MMC has floating capacitor in each of SMs, it requires a significant effort to understand the operation principles of the converter. The modeling approach should be chosen to provide an analysis of the converter's operation. The control structure of MMC is divided into two parts, which are DC side control and AC side control. DC side control is used to achieve stability of equivalent energy or voltage between the arms and all the SMs over time. As part of DC side control, the circulating current and energy based closed-loop control for MMC are tested in MATLAB/Simulink. The performance of the energy based and circulating control have worked effectively in experimental test in normal state by generating $2N + 1$ level at the output AC voltage.

Power switch and control in converter is needed to be safe, reliable, and accessible in order to achieve all the requirements and reduce the environmental impact. A redundant switching state is provided by some of the multilevel by allowing the converter to

maintain normal operation under internal fault conditions. The proposed method has a low computational burden by using only one single carrier that can be adapted immediately with the new level-number when an SM is under a fault. This proposed method also practically reduces the complexity in the implementation of the PDPWM modulation technique. The proposed control acts to change the scale of the staircase signal, which means it changes the scale of the adaptive carrier signal. The general energy-based control and circulating current control structures are well adapted to rebalance the remaining healthy SMs. Since this method is implemented using a symmetric operation to maintain the symmetry of arm voltage, it is suitable for a large number of SMs.

The simulation and experimental results have demonstrated that the proposed control method can effectively rebalance the remaining SM capacitors voltages at the desired new voltage. This proposed control method can also ensure that the converter works well to deliver good quality power without decreasing the performance of the converter. After clearing of the fault, the converter can return to normal nine-level immediately. Moreover, this method can also be used for adding more SMs into the arms without turning off the power supply.

## 6.2 Future Works

This thesis serves as a baseline for future studies on modular multilevel converter (MMC) based on balancing the SMs series using PDPWM technique and effect of a fault occurred internally (device fault). Referring to the evaluation and observation, the proposed method has some drawbacks in terms of the fast response on circulating current control and reducing the fluctuation of circulating current during a fault. The control algorithm can be improved by integrating with extra control to predict, accelerate and minimize the fluctuation such as fuzzy logic and predictive control algorithm.

In submodule (SM) failure, there are three scenarios that need to be considered to increase the reability of the proposed control to avoid the unbalanced voltage caused by faulty SM. First, if an SM of lower arm gets failure, the other SM from the lower is removed, so that it will maintain the phase voltage symmetric. Second, in the three-phase scheme, if the series of SMs of one phase fail, the other arms of the other phase continue operating normally as the result asymmetric in the synthesized voltage of an failed phase. Third, in the three-phase scheme, if an SM of lower arm gets fails, the other SMs at arms are removed in order to keep symmetric voltage of the MMC in all phases. Based on these scenarios, the future researches may focus on second and third scenario for three phase scheme. Additionally, grid connection is also considered as a future work. There are so many other faults can occur from grid, which give impacts to the converter.

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## LIST OF PUBLICATIONS AND PAPERS PRESENTED

- Adaptive Carrier Based PDPWM Control for Modular Multilevel Converter with Fault-tolerant Capability. IEEE Access. Status: Accepted on 29 January 2020.
- Modular Multilevel Converter Modulation Technique with Fault-Tolerant Capability. Conference IEEE PEDS July 2019, France. Status: Submitted on 28th February 2019; Accepted.