DUAL-BAND DOHERTY POWER AMPLIFIER WITH THE IMPROVEMENT OF REACTANCE COMPENSATION TECHNIQUE FOR LTE FREQUENCY OPERATIONS

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FACULTY OF ENGINEERING
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KUALA LUMPUR

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DISSERTATION SUBMITTED IN FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF MASTER OF ENGINEERING SCIENCE

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DUAL-BAND DOHERTY POWER AMPLIFIER WITH THE IMPROVEMENT OF REACTANCE COMPENSATION TECHNIQUE FOR LTE OPERATIONS

ABSTRACT

A dual-band selection of Doherty power amplifier employing a Reactance Compensation Technique (RCT) with Gallium Nitride High-Electron-Mobility-Transistor (GaN HEMT) technology is presented. In this dissertation, the focus has been given to the design power amplifier in Doherty configuration, where it can operate at dual-band frequency and enhanced performances at 6 dB back-off from saturation power. This project applied lossy matching circuit for the input matching network and incorporated the primary motivation of using RCT and third harmonic tuning for the output matching network.

The DPA designed can achieve satisfying results for the frequency of 0.8 and 2.1 GHz. The implementation is suitable for two-way radio application, particularly for LTE frequency operation. The results of the proposed concept are validated through simulation by using Advanced Design System (ADS). The measured results of the prototype board report accepted performance over the desired frequency. (ie. the maximum power level of 40.5 dBm, 6 dB back-off efficiency of 43% and 47% and gain of 10 dB approximately at 0.8 GHz and 2.1 GHz, respectively).

Keywords: Power Amplifier, Doherty Power Amplifier, dual-band.

PENGUAT KUASA DWI-BAND DOHERTY DENGAN PENAMBAHBAIKAN TEKNIK PAMPASAN REGANGAN UNTUK OPERASI FREKUENSI LTE

ABSTRAK

Penguat jalur dua pilihan untuk penguat kuasa Doherty menggunakan teknik pampasan regangan dengan Gallium Nitride High-Electron-Mobility-Transistor (GaN HEMT) teknologi dipersembahkan. Dalam tesis ini, tumpuan telah diberikan kepada penguat kuasa reka bentuk dalam konfigurasi Doherty di mana ia boleh beoperasi pada frekuensi dwi-band dan prestasi yang dipertingkatkan pada 6 dB dari back-off kuasa tepu. Motivasi projek ini adalah untuk menunjukkan bahawa dengan menggunakan idea litar padanan lossy untuk rangkaian padanan masukan dan pampasan regangan untuk rangkaian padanan keluaran, penguat kuasa Doherty yang direka dapat mencapai keputusan yang memuaskan untuk frekuensi 0.8 GHz dan 2.1 GHz. Pelaksanaan adalah sesuai untuk aplikasi radio dua hala terutamanya pada frekuansi pengendalian LTE. Keputusan cadangan konsep mengesahkan melalui simulasi dengan menggunakan Advanced Design System (ADS). Keputusan yang diukur daripada prototaip, menunjukan bahawa prestasi yang diterima pada frekuensi yang dikehendaki. (ie. Kuasa maksimum pada aras 40.5 dBm, 6 dB back-off kecekapan sebanyak 43% dan 47% dan gandaan hampir sebanyak 10 dB masing-masing pada 0.8 GHz dan 2.1 GHz.

Kata kunci: penguat kuasa, penguat kuasa Doherty, dwi-band.

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LIST OF SYMBOLS AND ABBREVIATIONS

ADS	:	Advance Design System
AI	:	Artificial Intelligent
ALGaN	:	Aluminium gallium nitride
dB	:	Decibels
DC	:	Direct current
DL	:	Deep Learning
DPA	:	Doherty power Amplifier
EER	:	Envelop elimination & restoration
ET	:	Envelope tracking
ESD	:	Electro-static discharge
FET	:	Field effect transistor
FR	:	Frequency ratio
GaN	:	Gallium nitride
GaAs	:	Gallium arsenide
HBT	:	Heterojunction bipolar transistor
Hz	:	Hertz
I_{MAX}	:	Maximum current saturation point
LINC	:	Linear amplification using non-linear components
MMIC	:	Monolithic microwave integrated circuit
MOSFET	:	Metal oxide semiconductor field effect transistor
PA	:	Power amplifier
PAE	:	Power added efficiency
PCB	:	Printed circuit board
PHEMT	:	Pseudomorphic-high-electron-mobility-transistor

P_{avail}	:	Power available from the source
P_{DC}	:	Power of direct current supply
P_{load}	:	Power deliver to load by the amplifier
P_{RFin}	:	Input power of RF
P_{RFout}	:	Output power of RF
RCT	:	Reactance compensation technique
RF_{in}	:	RF input
RF_{out}	:	RF output
Ri	:	Real input impedance
R_L	:	Load resistance
Rs	:	Real source impedance
S2P	:	2-port S-parameter component
TEM	:	Transverse electro-magnetic
VCVS	:	Voltage-controlled voltage source
VCCS	:	Voltage-controlled current source
VSWR	:	Voltage standing wave ratio
V_Q	:	Quiescent voltage point
Zi	:	Complex input impedance
Zs	:	Complex source impedance
Zo	:	Characteristic impedance
2DEG	:	Two-dimensional electron gas
Ω	:	Ohm

CHAPTER 1: INTRODUCTION

1.1 Research Background

Recently, there is a drastic improvement in Power Amplifier (PAs). As a result, the modern PAs for the telecommunication system has required a wide range of output power levels with high linearity and high efficiency. Generally, the PAs for two-way radio applications operate less efficiently at lower power levels and consume too much Direct Current (DC) power at lower power levels, even if it is designed for the highest power levels with maximum available efficiency. Therefore, it is a challenge to design a two-way radio with high efficiency not only at maximum output power but also at the 6 dB back-off from the maximum output levels with the consideration of lowering the design cost.

Moreover, to combat this problem, there is a newly proposed dual-band Doherty PA (DPA) circuit topology and methodology by implementing RCT to improve the efficiency performance compared to conventional DPA. The dual-band DPA design is based on the GaN HEMT n-type MOSFET (Metal Oxide Semiconductor Field Effect Transistor) packaged device with RF Coaxial Wilkinson splitter at the input of the DPA to improve output power, gain, and Power-Added Efficiency (PAE). A prototype of the dual-band DPA is designed based on the simulation result and desired output power of 40.5 dBm, a gain of 10 dB and the efficiency of 43% and 47% is achieved at 6 dBm back-off from the maximum output power level at 0.8 GHz and 2.1 GHz, respectively.

The overall simulation design and analysis is done using Advance Design System (ADS) software. The simulation of the large-signal model is executed using the transistor design kit acquired from Cree. Furthermore, measurements are carried out in Motorola Solutions laboratory at University of Malaya (UM) to test and rectify the fabricated amplifier.

This dissertation introduces the research background, theory, and DPA design for dual-band configuration The dissertation's main objective is to improve the back-off output power's efficiency across the specific frequency bandwidth. This dissertation introduces several chapters discussing the design methodology, fabrication, and the process of measurements. This work's topology interest is required to cover the dual-band frequency of 0.8 GHz and 2.1 GHz as per required in dual-band radio application's need. In terms of realization in the hardware level, the inductor has been converted to distributed elements such as microstrip for the smaller form factor. Moreover, the simulations and measurement results were demonstrated together with the discussion and conclusion at the end of the chapter. The results showed that the prototype is acceptable for two-way radio communication applications.

1.2 Problem Statement

Typically, PA is applied in the last stage of the transmitter, and it consumes the most energy in the transceiver. Since PA consumes the most power during the overall system's operation, PA's low efficiency will translate into more heat dissipation by the transistor, thus reducing the PA board's performance and reliability. Many approaches have been proposed to tackle the issue of the degradation of efficiency in the single-ended PAs, such as Load Modulation Method (known as Doherty), Linear Amplification using Non-linear Components (LINC), and Envelope Tracking (ET). Doherty Power Amplifier (DPA) stands out from other approaches as it has a simple implementation, maintains the linearity, and has broader potential fractional bandwidth compared to other approaches.

In recent years, there has been an increasing amount of research in multi-band DPAs. However, most of these works were focused on the building block approach where the single-band output matching network, phase offset lines, and dual-band impedance

inverters are pre-implemented, and their main focuses are on replacing each building block with its dual-band equivalent circuits. This has caused a large design complexity and significant bandwidth degradation and performance deterioration in at least one of the targeted frequency bands. Moreover, they have not demonstrated the capability of dual-band DPA for carrier aggregation scenarios.

For this dissertation, a novel technique of reactance compensation and third harmonic tuning at the output matching network is presented to design dual-band DPA. The proposed technique reduces the design complexity and extends the operational bandwidth of the existing dual-band DPA. This approach reduces the cost and complexity of the two-way radio design.

1.3 Research Objectives

The key to this work is to enhance the efficiency of the DPA for selected dual-band frequency. Therefore, this study embarks on the following objectives:

1. To design DPA based on reactance compensation technique and third harmonic tuning to meet the required efficiency, gain, and power using GaN HEMT technology.
2. To achieve high efficiency at 6 dB power back-off for the frequency of 0.8 GHz and 2.1 GHz.
3. To validate the fabricated prototype board experimentally to obtain decent dual-band performance.

1.4 Scope of Research

The work presented in this dissertation focuses on the system design of a dual-band PA. This system design aided by circuit design forms the first building block of the two-way radio. The other components, such as Wilkinson splitter and mixers amongst others that make up the rest of the two-way radio, fall outside this thesis's scope. (Note: Wilkinson splitter's presence is only used in simulation testing purposes as Wilkinson is out of this research scope, it is used only for testing purposes because we do not have two signal generator.)

1.5 Organization of Dissertation

This dissertation is divided into five chapters, as follows:

Chapter 1 describes the background, problem statement, and objectives for this research.

Chapter 2 describes the literature review of the power amplifier, whereby the power amplifier classification is discussed. Impedance matching, recent work of DPA, Figure-of-Merits, and the fundamental theory of GaN HEMT are presented.

Chapter 3 presents the methodology of DPA design, which includes the includes lossy matching, development of power splitter for simulation purpose, matching network with lumped inductors converted into microstrip, conversion of a capacitor with industrial realization, load modulation, PCB layout design, heat sink design, and PCB fabrication. Moreover, the enhanced DPA focusing on dual-band applications using RCT and third harmonic tuning for experimental setup are presented.

Chapter 4 presents the results of the simulation and the collected measurement data of the designed DPA. Discussion of the comparison between the simulation and measured are also presented.

Chapter 5 describes the conclusion and future work for the work in this dissertation.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction of Power Amplifier

In any discussion about RF PA techniques for modern applications, the central goal of maintaining efficiency over a wide range of signal dynamics is paramount important. Furthermore, the linearization goals which challenge the modern RF designer become relatively unimportant if efficiency is removed from the equation. In the case whereby efficiency is the sole criteria, backed-off Class-A amplifiers still take a lot of beating. It is quite surprising that numerous PA design techniques, especially the techniques that addressed the efficiency management issues which date from an earlier era, have been ignored by the modern RF design community. This chapter focuses on discussing the fundamental PA classification based on the conduction angle of the drain current and following some alternative ways of approaching a problem in pursuit of a PA design technique that emphasized the efficiency in the wide range of dynamic signal applications. The analyses lay the groundwork for understanding advanced circuit techniques presented in this chapter's subsection, such as the DPA, which uses two parallel devices.

2.2 Power Amplifier Classification

The PAs can be classified into two distinct amplifiers, known as the non-linear and the linear amplifiers. Both of the amplifiers can be differentiated by the efficiency, linearity, and topology of the circuit design. As for the non-linear amplifiers, the waveform can be identified by the presence of distortion of the signal. In comparison, linear amplifiers tend to have a waveform that is not distorted. The regular non-linear PAs are the Class-C, D, E, and F. On the other hand, the regular linear PAs are A, B, and AB.

2.2.1 Class-A

For Class-A PA, this needs to keep precise that the transistor conduct throughout the angle of 360˚ and preventing it from falling into saturation or cutoff region. The biasing of the transistor is set to the mid-point within the range of linearity. In comparison, other types of PAs; the Class-A PA will have a better performance, especially at a higher frequency due to lesser high-order harmonic. Class-A PA has very low distortion, and Figure 2.1 shows the quiescent point of this class, and it has clearly shown operation within the range of the linearity. Theoretically, the efficiency of Class-A PA is 50%. With this, it is usually applied in low power level applications, which require higher gain. The disadvantages of Class-A PA are the inefficiency at high power applications, requiring higher costs for the power supply to produce.

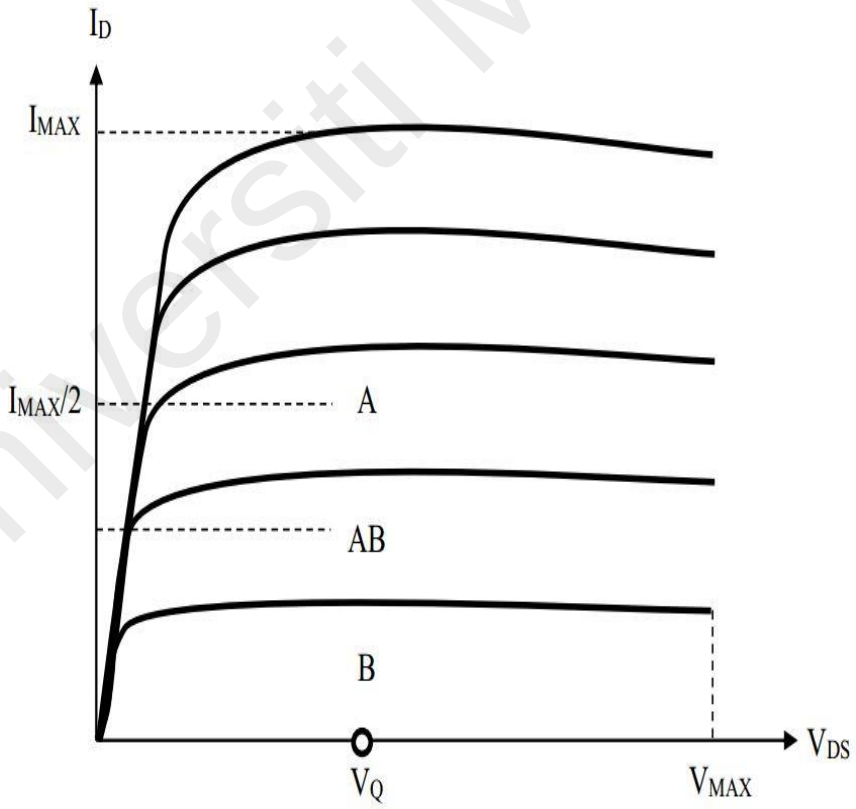


Figure 2.1: **Bias points for common PA Modes**

2.2.2 Class-B

For Class-B PA, the transistor has the conduction angle of 180˚, which is only half the Class-A PA's conduction angle. In other words, the transistor only conducts either half the negative or positive cycle of the signal from the input. The class of operation is determined by the DC bias. Figure 2.2 shows the cutoff for the quiescent point of Class-B. For the output, the harmonics are shorted, and above the threshold voltage, the device is considered linear. So the intrinsic load of the Class-B PA is considered as resistive. The efficiency of the Class-B PA has improved by 28.5% to 78.5% compared to the Class-A amplifier, but the weak point of Class-B PA is the lesser in linearity due to the presence of the harmonic signal after amplification.

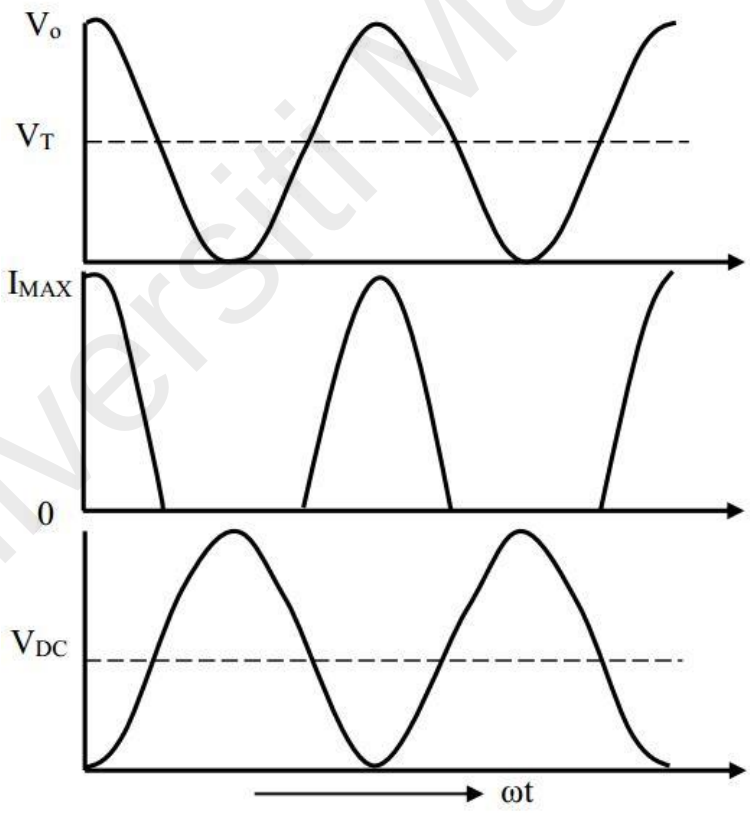


Figure 2.2: Class B Waveforms

2.2.3 Class-AB

In Class-AB PA shown in Figure 2.3, it consists of the combination between Class-A and Class-B PA. This means that the characteristic of the amplifier is non-linear. It is operated in the region between the two edges and exhibits the efficiency and linearity of the combination characteristic of the two different classes of PA. In the ideal case, the biasing of the Class-AB mode is in the region between the bias point and the cutoff point of Class-A, in which it is also known as the quiescent point. As a matter of fact, about the quiescent drain current, it is in the region between 0.1 and 0.2. Compared to Class-A PA, the Class-AB PA has improved; however, it is still not more than 78.5%, whereas the angle of conduction is between the range 180˚ and 360˚. Class-AB PA, as compared to Class-B PA, has distortion at the peak power level of the amplitude-modulated signals. As a result, Class-AB PA has a broader range considering dynamic as a factor compared to Class-A and Class-B PA, which is due to the multiplicity of the source, which leads to the compression of the gain in the PAs discussed above.

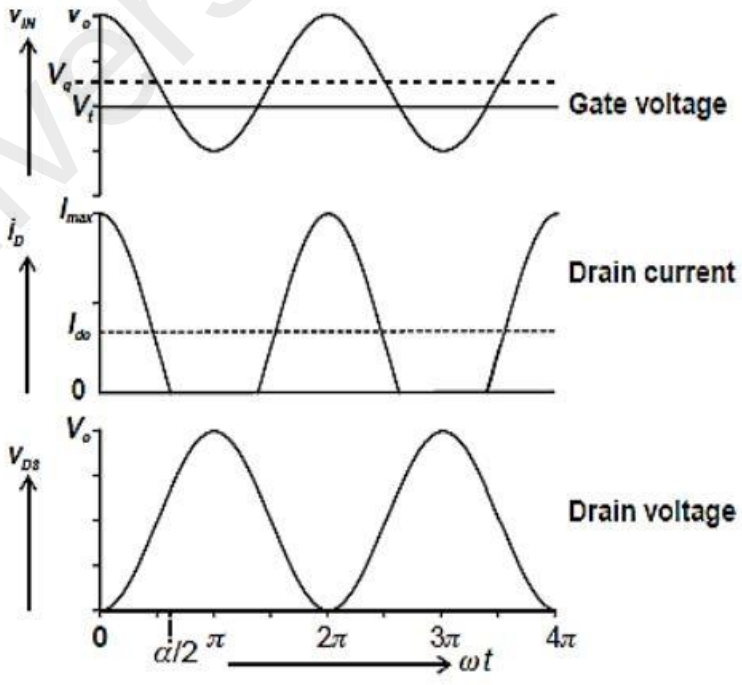


Figure 2.3: Class-AB Waveforms

Referred to the linearity of the Class-AB, Figure 2.4 below shows the gain compression for a variety of biasing classes for PA. Additionally, other different class of PA, which is not the Class-A, have the gain at the saturation region suffer from distortion, which leads to gain compression. The value of 0.05, 0.15, and 0.25 in Figure 2.4 indicate the biasing quiescent voltages for Class-AB PA. At lower power input levels, the presence of the distortion in Class-AB PA is of a different kind and required to be considered in detail.

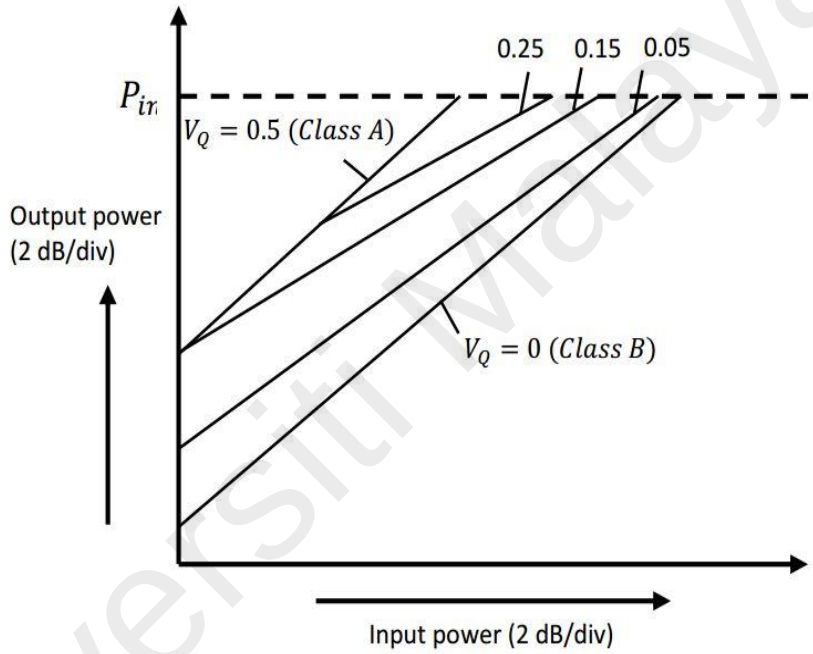


Figure 2.4: Class-AB gain characteristics

2.2.4 Analysis of Reduced Angle of Conduction

The terminology conduction angle means the PA is conducting at a fraction of the full-cycle sinusoidal waveform of 360˚. As for Class-A PA described before, the angle of conduction is at full-cycle 360˚. Fundamentally, Table 2.1 below shows the conduction angles for several classes of PA.

Next, Figure 2.5 shows the concept of improving efficiency by reducing the conduction angle. Refer to Table 2.1, which moves the biasing point of the Class-A PA toward cut-off, and results in a reduction of the conduction angle.

Table 2.1: Reduced Conduction Angle for some PA modes

Mode	Bias Point	Quiescent Point	Conduction Angle
A	0.5	0.5	2π
B	0	0	π
AB	0-0.5	0-0.5	$\pi - 2\pi$
C	<0	0	$0 - \pi$

Figure 2.5 has illustrated the quiescent voltage point at V_Q. By analyzing the figure, the input voltage will be falling below the threshold value as a result of a sufficient amount of RF drive, which causes the cut-off for current. This makes the current achieve the maximum saturation point (I_{MAX}). For the devices to be considered transconductive, the RF drive level relative to Class-A mode has to be increased.

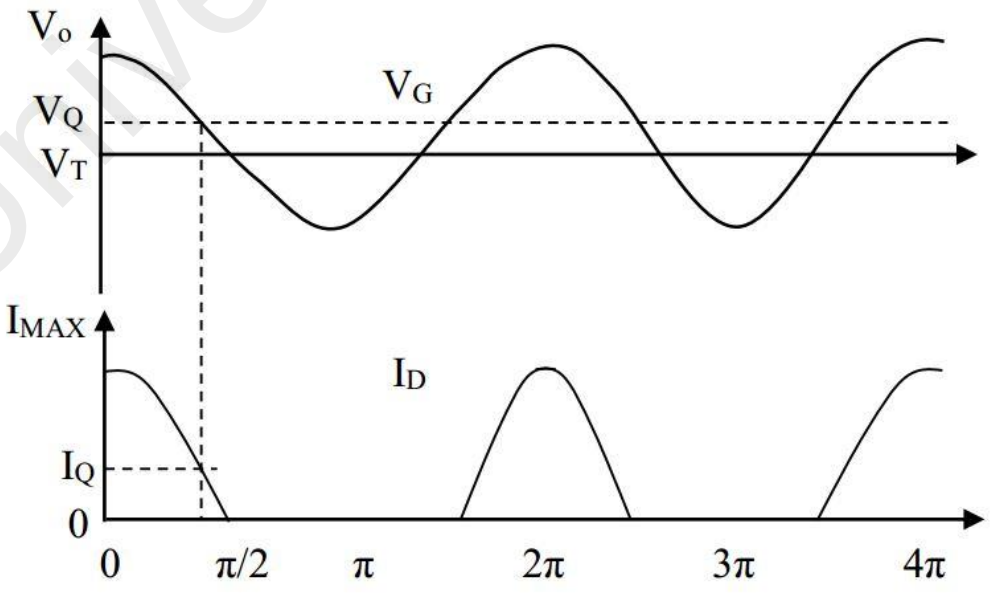


Figure 2.5: Reduced conduction angle waveforms

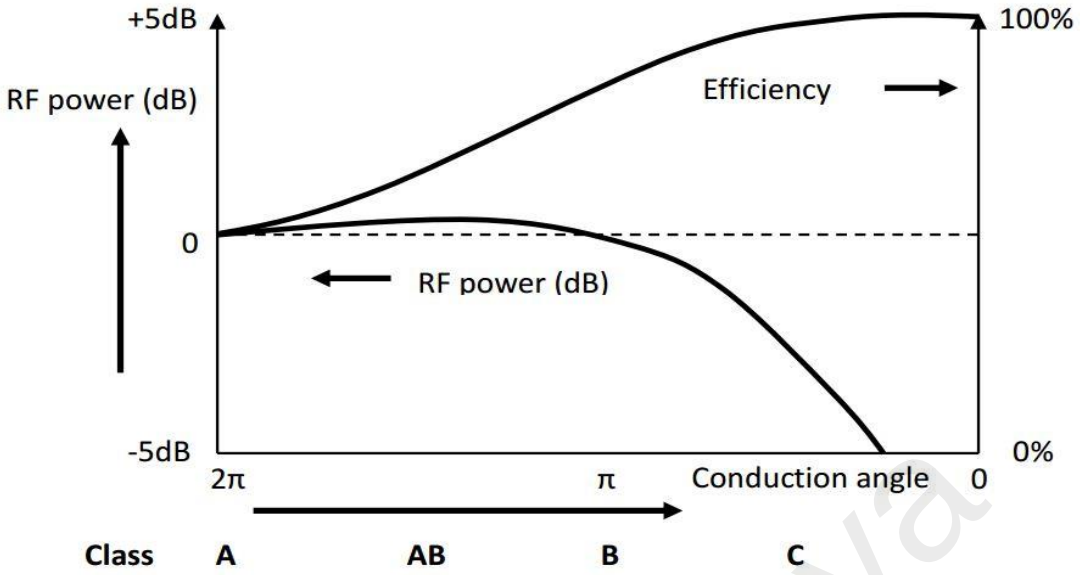


Figure 2.6: Efficiency as a function of the conduction angle

Referred to Figure 2.6 depicted above, the efficiency has improved while the conduction angle has reduced. In this case, the percentage of efficiency for Class-A mode is at 50%, whereas the conduction angle is reduced, the efficiency improves to Class-B mode territory of 78.5%.

2.2.5 Switch-Mode PA

To further improve the efficiencies of the PA, switch-mode PA is introduced to provide more efficiency as compared to the transconductance PA. In the case of switch-mode PA, it is driven into the region of compression where in this state, the transistor does not operate as a current source, but instead, it operates as a switch. Therefore, the switch-mode PA's efficiency is achievable by reducing the convergence between the non-zero drain voltage and current against time. Theoretically, achieving 100% efficiency is possible in switch mode configuration without the need to trade off the output power. However, practically several mechanisms reduced the efficiency of the switch-mode PA. As a matter of fact, the switch-mode PA's linearity can be improved

in the past by several proven methods such as EER (Envelop Elimination & Restoration) and LINC. The simple version of switch-mode PA is known as Class-E PA, which is operated on the principle of off-to-on switching or vice versa.

With the minimization of the overlapping between the voltage and current waveform for the drain current, the efficiency has improved, and the power loses has been kept low. (Grebennikov, O. Sokal, & J. Franco, 2012) Figure 2.7 showed the conventional design of the Class-E PA in which the capacitance of the output of the device is in a parallel configuration, whereas the series configuration of the device output consists of the Load Resistance (R_L), Reactive Component (jX), and resonator. The output signal of PA is sinusoidal due to the fact that the series resonator resonates at the fundamental frequency. The jX is responsible for the change of the phase shift of the output waveform between the drain and the load voltage.

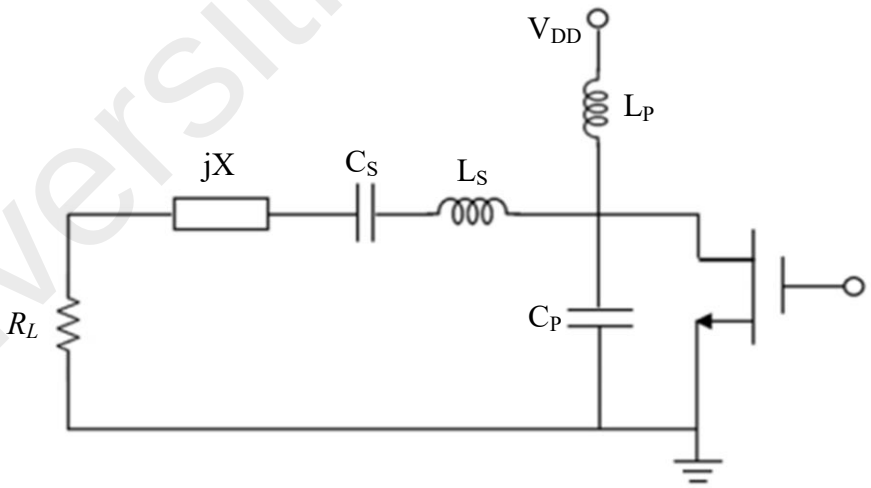


Figure 2.7: Basic circuit of Class-E PA

Furthermore, Class-F PAs applies the principle of trapping the odd and even harmonics and make it open and short, respectively. Therefore half sinusoidal waveform is produced for the drain current while generating a square wave for the drain voltage. As a result, the minimization of the overlapping between the drain current and the drain

voltage will lead to high efficiency. Class-F PA is usually designed using quarter-wave transmission lines. (Din, Geck, & Eul, 2009). Typically, the quarter-wave transmission line is similar to the series resonant circuit in an infinite number.

Figure 2.8 shows the Class-F schematics with the *LC* tank and *jX* as the transmission line of quarter-wave. The quarter-wave transmission is able to provide impedance transformation. The peak current and voltage of Class-F PA are low, which has an edge compared to the Class-E amplifier. However, the disadvantage of Class-F PA is the presence of a complex load network.

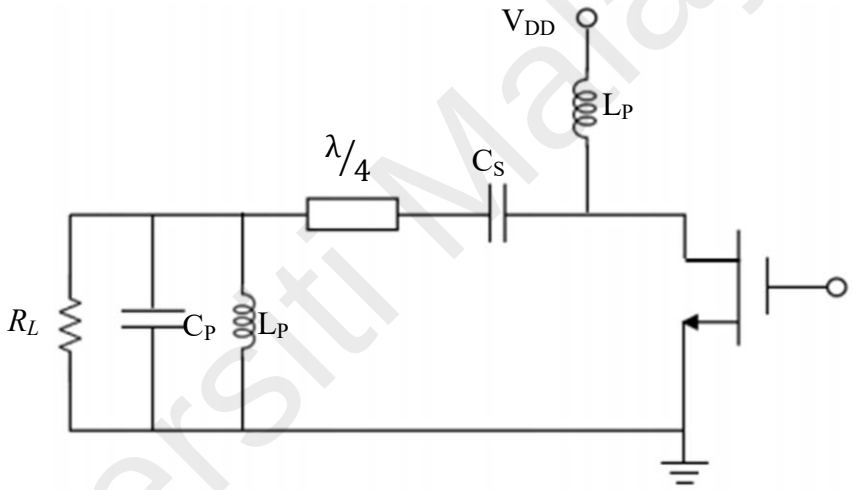


Figure 2.8: Class-F PA using a quarter-wave transmission line

To sum up, the transconductance PAs has a lower efficiency as compared to the switch-mode PAs. However, the downside is that the bandwidth is narrower due to the resonators' presence to tune the output to the fundamental frequency. For broadband amplifier design, the Class-A PA is the most favorable class. In terms of efficiency, the Class-AB PA is a good choice to be considered as it also can be used to design wideband PA.

2.3 Impedance Matching

For many decades, researchers have been working on impedance matching without finding a perfect technique for a solution. The approach to inserting metamaterial between the antenna and the ground plane has recently been very effective. However, this method's functional implementation is limited by exorbitant costs and other physical limitations, such as weight and material robustness.

The lack of an optimal solution to the broadband matching problem is the inspiration for this dissertation. It is possible to find an optimal impedance equalizer over a wide frequency band by inserting lossy components (i.e., resistors) into conventional matching networks.

2.3.1 The Problem with Impedance Matching

Early matching circuits were developed in the 1920s to couple the power from the amplifier output to a load antenna (Everitt, 1931). Some mathematical comprehension of impedances was addressed in the 1950s (Papoulis, 1953). Nevertheless, the issue was not well defined until then. Nor were the strategies and processes completely developed to solve this problem.

The topic of lossless networks with lumped L and C components was discussed by Fano (Fano, 1948) in 1948. Richards (Richards, 1948) adapted the lossless network outcomes into lossy impedance matching issues the same year. Ever since, the methods and procedures for impedance matching have evolved.

Nowadays, the problem of impedance matching has been defined as the need to optimize the signal power transmission or minimize the load reflection. In lossless networks, these two prime objectives are synonymous. However, in the lossy impedance

matching, there are two different targets, since a certain amount of power is consumed by the lossy components.

Impedance matching is fairly simple at a single frequency. However, in practical engineering problems, a load over a broader frequency range band is often needed to be matched. As the required bandwidth expands, designing becomes even more difficult. A network may consist of multiple lumped elements, distributed elements, a combination of both and/or ad hoc solutions instead of the fundamental lossless matching network with only two L and C components (Steer, 2013).

Resistors will be applied to matching networks in this dissertation to render "lossy", thus lowering the gain to a certain level and getting wider low VSWR bandwidth.

2.3.2 The Challenge of Broadband Impedance Matching

The problem of broadband matching is defined as the transmission of power from the source to load. Conjugate matching can be used to design a single frequency matching network, but over a finite frequency band is not physically feasible. However, by incorporating loss, more bandwidth can be gained at an expense to the transducer power gain of the matching networks.

2.3.3 Lossy Matching

In order to dissipate power into other materials besides the load, engineers should prevent lossy matching. However, in cases such as broadband matching issues, it is necessary to make a trade-off between power efficiency and bandwidth.

Lossy matching has its benefits. These benefits of lossy networks inspired researchers to continue to explore and made the following discoveries: lost networks without transformers were used (Gilbert, 1975); selected lossy lumped networks were optimized

to include sloped-gain passbands (Liu & Ku, 1984); the Pareto front was created showing the best trade-off between reflective equalizer power and dissipated power (Min & Allstot, 2005). Moreover, LaRosa (LaRosa & Carlin, 1954) identified three potential advantages of lossy matching networks:

(a) A dissipative network may have a simpler form than a lossless one.

(b) The return loss of input and the power transmitted to the load impedance cannot be independently controlled by a lossless matching network.

(c) The lossless network may not be able to provide the optimal low return loss over the passband.

Allen et al. (Allen, Arceo, & Hansen, 2008) used the H-infinity theory to show that the Pareto front is generated by a globally optimal lossless matching network followed by a resistive pad. They consider using dissipative network components instead of resistive pads to achieve optimum matching networks.

2.4 RCT and Third Harmonic Tuning

The RCT and third harmonic tuning has been developed for dual-band frequency to meet our requirements (Krishnamoorthy, Kumar, Grebennikov, & Ramiah, 2018) . Both of the resonant circuits are tuned to the fundamental frequency and R_L (Grebennikov, Kumar, & Yarman, 2015). If the frequency changes, it will affect the reactance of the series and shunt resonant circuits. In this case, the reactance increases in a series resonant circuit while reducing in the loaded parallel resonant circuit near the resonant frequency. Therefore, in near-resonant frequency, the positive slope of reactance in a series circuit is compensated by a proportional negative slope of reactance in the shunt circuit (Grebennikov et al., 2012), thus producing a zero total variation in reactance and a constant load angle over a wide frequency bandwidth (Kumar, Prakash, Grebennikov,

& Mediano, 2008). In addition, the third harmonic tuning is added to provide an open-circuit condition at the fundamental frequency whereas it is effective for narrow bandwidth. The implementation of the RCT and third harmonic tuning in circuit design will be shown in the Chapter 3, Section 3.10.

2.5 Recent works in DPA design

In telecommunication systems have numerous specifications and criteria that a certain frequency band may be used for each standard. One of the main targets for each generation is the data rate, in which complicated modulation and more bandwidth are needed for data rate growth (X. Chen et al., 2017; Kelly, Cao, & Zhu, 2017; Lin & Xie, 2018). The upcoming generation will use more frequency bands to meet the targeted requirements due to the crowded spectrum. In the past 20 years, Doherty power amplifiers (DPAs) was studied extensively to enhance the efficiency bandwidth (Aydin, Palamutcuogullari, & Yarman, 2016; Bertran & Yahyavi, 2015; Cheng, Li, Liu, & Gao, 2017; Jia, Yu, Yang, & Zhang, 2018; C. H. Kim & Park, 2016; J. Kim, Fehri, Boumaiza, & Wood, 2011; Sun & Jansen, 2012; Xia et al., 2018; Zhao et al., 2018). Carrier aggregation technology has been implemented to improve bandwidth efficiency, where emerging technologies for wireless communication systems are expected to use multi-band multi-standard implementations (Mingming et al., 2016).

Two power amplifiers can be used with each band to concurrently support the dual-band, but this increases the area of die and allows more circuitry to integrate their outputs. A reduction in the device size and cost can be achieved by the dual-band configuration, and Doherty will produce a decent efficiency (Shao et al., 2014). There are numerous successful implementations of either dual-band PAs (Dai, He, Pang, & Huang, 2015; Pang et al., 2016; Wu, Jiao, & Liu, 2015), or dual-band DPAs (W. Chen et al., 2014; Mingming et al., 2016; Pang et al., 2016). The work carried out by

Jingzhou Pang et al. shows that the concurrent dual-band DPA design is able to achieve 63% and 51% efficiency at 6 dB back-off point from the saturated power in the frequency of 1.8 GHz and 2.6 GHz (Pang et al., 2016). Also, the work presented by (Mingming et al., 2016) which proposed the feasibility of a dual-band DPA and obtained the drain efficiency exceeds 49% and 47% at 6 dB back-off point from the saturated power across the frequency bandwidth of 2.05-2.30 GHz and 3.2-3.62 GHz. The dual-band DPA presented by (W. Chen et al., 2014), applies frequency-dependent input power division and obtained power-added efficiency of 45% and 41% at 6 dB back-off from the saturation for the frequency of 0.85 GHz and 2.33 GHz.

The term dual-band can be applied in two ways. In the first one, the power amplifier is configured to operate in two frequency bands, one at a time, where depending on the target band, the circuit properties and configuration are modified. Next, the concurrent dual-band means that the amplifier will operate without any alteration or modification of the design on both frequency bands.

2.6 Dual-Band DPA Problems and Challenges

The key problem with multi-band features is the RF-front end-stage (Bathich, Gruner, & Boeck, 2011; Park, Yook, Kim, & Lee, 2011). In order to operate on the specified frequency bands, RF front-end components such as antennas, filters, switches, and power amplifiers should be designed. According to (Xiang et al., 2012), it is possible to build a multi-band DPA so long as there are dual-band components.

The power amplifier design sub-circuit involves the device cell, input, and output network matching. The device cell for each planned frequency band should be able to operate properly. It is usually the duty of the input matching network to control the gain over the appropriate band. In exchange, the output matching network selects the power

and quality of the output. The effect of the second harmonic on the PA input is negligible so that the matching input network can only be constructed for the fundamental frequency of each band (Saad et al., 2012). However, the contemporary design for matching networks does not rely solely on simple frequency matching; more harmonic effects may be used in order to achieve a certain efficiency.

The key disadvantages of the DPA are the 4-quarter wavelength (impedance inverter) and the offset lines that restrict the bandwidth due to their natural characteristics (Monzon, 2003; Saad et al., 2012; Wang, Zhao, & Szymanowski, 2010). In order to design a dual-band DPA, the quarter-wave impedance inverter and offset line should be replaced by more complex networks, which in split bands give equivalent functions.

2.7 Power Amplifier Figures-of-Merits

As a designer, the main concern when design the PAs is performance. Usually, the designer will take the cue based on a few parameters to validate the PAs' performances. In this section, we are focusing on several common parameters to validate the performances of the PA.

2.7.1 Efficiency

To measure how good the PA convert on energy in a device, efficiency is used as an indicator of measurement. The wasted energy or the energy that is unable to convert successfully in the process usually ends up as heat energy, which is detrimental to the PA's PCB. To know about the efficiency in microwave engineering, the main concern is about the conversion of RF power from DC power. This section will show several methods to calculate the PA's efficiency.

2.7.1.1 Drain Efficiency

Fundamentally, Field Effect Transistor (FET) is a device in which the drain efficiency acquires its name. The measurement of the transistor's drain terminal can be derived into drain efficiency. The drain efficiency of the transistor is expressed in the empirical calculation below:

$$\eta_{drain} = \frac{P_{RFout}}{P_{DC}} = \frac{P_{RFout}}{V_{DC} \times I_{DC}} \tag{2.1}$$

Where P_{RFout} = Output Power of RF

P_{DC} = Power of DC supply

Typically, the conversion of DC into RF power is known as drain efficiency. However, there is a big issue to benchmark drain efficiency as an indication of the performance because RF input power does not account for the drain efficiency calculation. RF input power can be significant because the gain for the device is low. Drain efficiency mostly uses in FET-based devices, such as pseudomorphic-High-Electron-Mobility-Transistor (pHEMT), but in the case of bipolar transistor devices such as Heterojunction Bipolar Transistor (HBT), this parameter can be referred to as ~~"c~~ollector efficiency".

2.7.1.2 Power Added Efficiency

For Power added efficiency (PAE), the differences compared to the drain efficiency include the parameters of RF power in the equation. Usually, when a designer designs a PA device, they will benchmark PAE for efficiency consideration. The PAE empirical expression is shown below:

$$\eta_{power-added} = \frac{P_{RFout} - P_{RFin}}{P_{DC}} = \frac{P_{RFout} - P_{RFin}}{V_{DC} \times I_{DC}} \tag{2.2}$$

Where P_{RFout} = Output Power of RF

$P_{RFin} =$ Input Power of RF

$P_{DC} =$ power of DC supply

Theoretically, PAE is quite similar to drain efficiency. But practically, PAE will always be lower than drain efficiency. In the calculation of the efficiency, the RF input power is included when the PA's gain is relatively lower than 30 dB. This is because the differences between the drain efficiency and PAE are significantly small as the input gain surpasses 30 dB. Moreover, when the frequency increases, the device's maximum PAE and maximum gain tends to decrease.

$$\eta_{power-added} = \eta_{drain} \frac{G-1}{G} \tag{2.3}$$

2.7.2 Gain

In RF PA design, the designer must contemplate which empirical method is relevant and essential; for this case, the power gain is much more important than the voltage gain. This is because reflections (both current and voltage) occur at this frequency range in the transmission lines. As a result, the circuit's characterization is done by s-parameter, and it is based on incoming and outgoing powers. (Zhang et al., 2016) The gain for the transducer is expressed as follow:

$$G = \frac{P_{load}}{P_{avail}} \tag{2.4}$$

Where $P_{load} =$ Power deliver to load by the amplifier

$P_{avail} =$ Power available from the source

With the input impedance and the source impedance are matched (In the case of real

impedances, Ri=Rs, and impedances in complex form, Zi=Zs), the availability of the power from the source to the input amplifier is similar.

If Rs=Ri, the available power (matched PA input) in empirical form can be expressed below:

$$P_{avail} = P_{input-matched} = \frac{V_i^2}{R_i} \tag{2.5}$$

The power received by the R_L by the amplifier's output is:

$$P_{load} = \frac{V_i^2}{R_L} \tag{2.6}$$

With the available expression of P_{avail} and P_{load}, these two equations are substituted into equation (2.4), and the gain for the transducer is defined based on Voltage (*V)* and Resistance (*R)*.

2.7.3 Output Power

In the design of RF microwave circuit, output power measurement is one of the crucial factors that we should focus on in order to obtain satisfactory performances of the design. In a system, the signal is passing from one component to the succeeding component. If the output power signal is too high, the performance will be non-linear, and distortion will occur or even damage the whole circuit. On the other hand, if the output power signal is too low, the signal can be obscured in noise.

When the DC is at low frequency, the current and voltage measurements are simple and straightforward. The power of the system can be easily computed by the following expression:

$$P = IV = \frac{V^2}{R} = I^2R \tag{2.7}$$

The measurement of current and voltage becomes more difficult when the frequency approaches 1 GHz; therefore, power measurement is preferable in most applications for high frequency. This is because power is maintained constant throughout the frequency bandwidth along the transmission line, but current and voltage may vary along the transmission line due to the reflected and incident waves produced by standing waves. Hence, in RF and microwave frequency, power is more easily measured and understood; it is also a very useful fundamental quantity compared to voltage and current for performance measurement.

A figure of merit that is often employed in the transmission theory is Voltage Standing Wave Ratio (VSWR). The impedance of the load has to be equal to the source's impedance to ensure power is transfer maximally. However, in almost every practical case, the incident signal is reflected back to the source by the load. Therefore, when the incident wave and reflected wave are present, a standing wave is produced. It is called a standing wave because the envelope of the wave does not change with time but remains stationary. The ratio refers to the ratio of maximum value and minimum value of the envelope, which is a measure of relative amounts of opposite traveling waves.

2.8 Basic Theory of GaN HEMT

GaN HEMT is chosen due to the presence of the high bandgap for a power device. For RF communication application, the suitable device is CGH40010F, which is from CREE Inc. with V_{bk} of ~120 V in 50-Ω condition. However, there is also another brand of GaN devices from other companies such as Triquint, NXP, etc. The fundamental configuration of the GaN HEMT device is shown in Figure 2.9. The layer of the AlGaN, also known as silicon-doped aluminum gallium nitride, is grown above of GaN. In comparison to the GaN, the energy gap for AlGaN is higher.

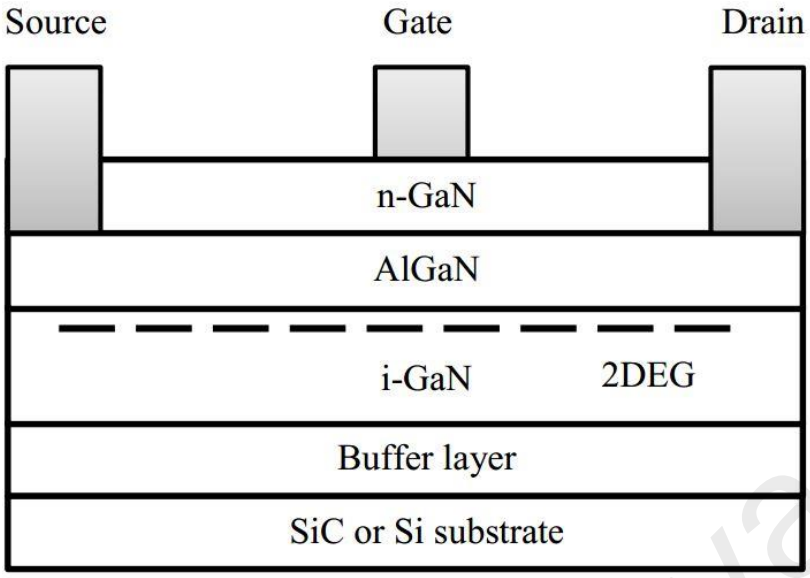


Figure 2.9: GaN HEMT basic configuration

In this case, the region with the lowest potential, known as the crystal, tends to receive the electrons donated by the silicon impurities—the presence of a layer of electrons, which has Two-Dimensional Electron Gas (2DEG). To realize the transistor's action, the drain and source metals and a gate contact are modulated with the depletion region and can be contacted to 2DEG. (Giorgi, 2008).

There are a few elements in which the high power GaN HEMT device can include in its enhanced equivalent circuit. First is the electrothermal elements; it is used to predict the rise of temperature during the dissipation of power. Second is the delay network, where it is used to expound the delay effect of high frequency. The third is the spreading resistance of the source, as it is used to explain the increase of the magnitude of S_{21} proportional to the frequency due to the influence of the device channel. However, this is essential for the device's equivalent circuit to be check and analyze for the main non-linear intrinsic elements. As for the extrinsic linear elements, although it has not much effect during lower frequencies, this can be considered and added to the distributed circuit parameters.

Table 2.2 shows the comparison between the properties of Gallium Nitride to other semiconductor materials. In addition, GaN-based HEMTs have specific unique properties that make them well suited for high frequency, high power applications (Santhakumar, 2010). These are:

1) **High breakdown voltage**. The wide bandgap of GaN, about 3.4 eV, results in a much higher breakdown field strength (>3.3 MV/cm) than other semiconductors. This, in turn, results in high breakdown voltages for GaN HEMTs. Hence, these transistors can be biased at higher drain-source voltages. For PAs, this usually results in an easier impedance match to 50 Ω.

2) **High electron sheet charge densities**. The ability of GaN to form a heterojunction with materials like AlxGa1-xN and the presence of strong polarization fields (spontaneous and piezoelectric) results in a 2DEG at the interface without the need for external doping. The sheet charge densities thus obtained are much larger than in hetero-junctions in other semiconductors. At the same time, due to the absence of dopants, high mobility can be maintained. The high sheet charge results in a high output current.

3) **High saturation/peak electron velocities**. The electron velocities in GaN are comparable to or better than other semiconductors. However, the electron mobility is not as high as in some other semiconductors like GaAs. This problem can be overcome by designing devices with short gate lengths to keep the electric field high. This should make the device performance more dependent on saturation velocity rather than mobility.

4) **High thermal conductivity**. Inherently, GaN exhibits better thermal conductivity than GaAs or InP. However, free-standing GaN substrates were not available at the time

of this work. The substrate of choice to grow the GaN epitaxial layers was 4H-SiC. In addition to having a good lattice match to GaN, SiC shows almost three times higher thermal conductivity than GaN. Hence, GaN-on-SiC offers a very high thermal conductivity material system and is well suited to build PAs.

Table 2.2: Comparison of Gallium Nitride to other semiconductor materials properties

Semiconductor Material	GaN	4H-SiC	GaAs	InP	Si
Bandgap (eV)	3.39	3.23	1.42	1.34	1.12
Breakdown Field Strength (MV/cm)	3.3-5.0	3.0-5.0	0.4	0.5	0.3
Saturated Electron Velocity (cm/s)	1.3	2.0	1.3	1.0	1.0
Peak Electron Velocity (cm/s)	2.5	2.0	2.1	2.5	1.0
Electron Mobility (cm^2/Vs)	1000	900	8500	5400	1400
Thermal Conductivity ($W/cm\ ^oC$)	1.3	3.7	0.55	0.68	1.3
Dielectric Constant	8.9	9.7	12.9	12.5	11.7

2.9 Summary

In this chapter, the literature review on the fundamental of PA concomitant with Doherty PA design work has been presented. By critically analyzing various works, several issues of concern regarding broadband amplification limitations for impedance matching and novelty in DPA design for two-way radio frequency communication applications have been raised. The lossy matching and its advantages have also been presented. The formulation of the empirical expression in theory base on previous research is discussed. Moreover, the performance discussion was also carried out on the stability, noise, and power. The simulation software known as Keysight's ADS 2012 software is used to obtain the data about the transistor's intrinsically parasitic effect and how it affects the design of the DPA when applying the reactance technique. The reactance compensation is expected to provide a good improvement as compared to the

conventional DPA design. Furthermore, GaN HEMT power transistor device has unique properties that will enable it to acts as an essence for the DPA design, which is well suited for high power and high-frequency RF communications applications.

CHAPTER 3: METHODOLOGY

3.1 Introduction

This chapter discussed the methods to design DPA, which includes the lossy matching, the power splitter, matching network with lumped inductors converted into microstrip, conversion of a capacitor with industrial realization, load modulation, PCB layout design, heat sink design, and PCB fabrication. Moreover, this chapter presents the enhanced DPA focusing on dual-band applications using RCT and third harmonic tuning, software simulations, theoretical analysis, and measurement setup.

3.2 Project Overview

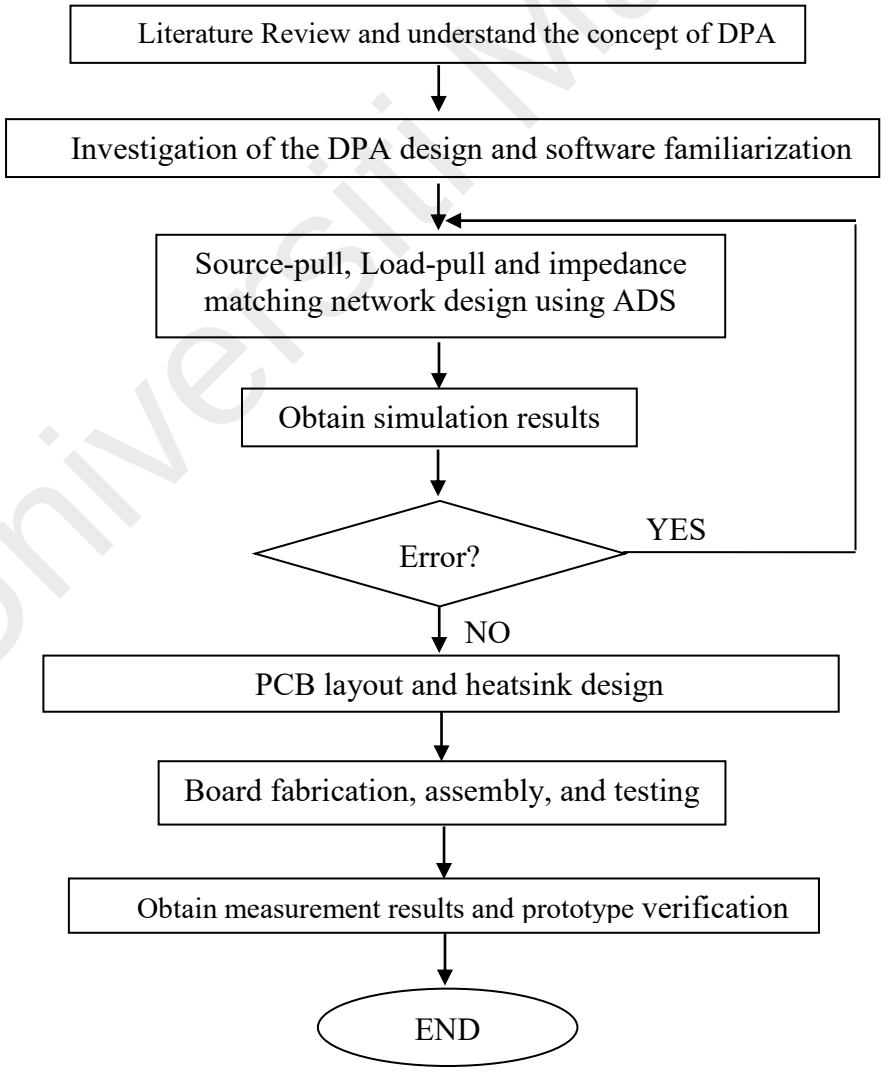


Figure 3.1: Project flow chart for DPA design

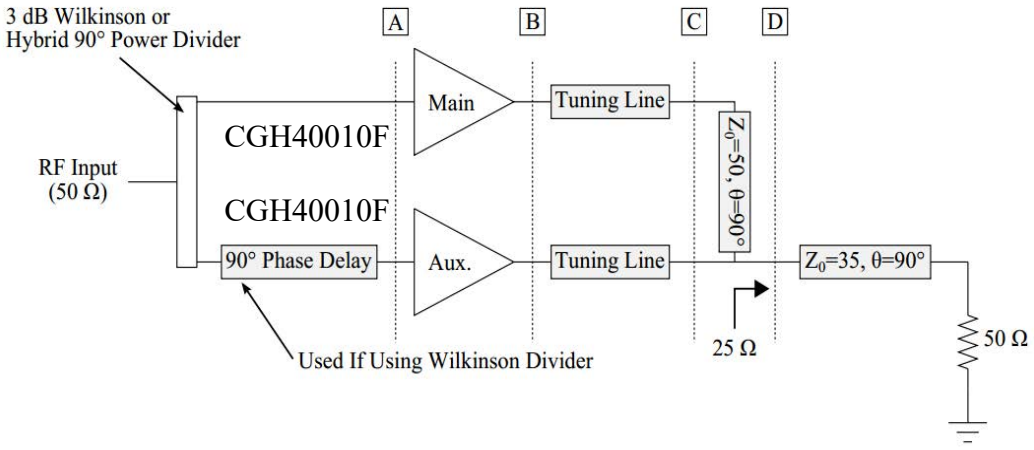


Figure 3.2: Overview diagram of the proposed circuit topology

3.3 GaN HEMT Bias Characteristics

As for the compromisation of the efficiency and linearity, the best operation to be choose was Class-AB. For CREE CGH40010F transistor gate bias voltage = -3 V and its value undergo sweeping from -3 V to 1.5 V with 100 mV step. The graph of the transistor's current versus voltage characteristic is plotted, and the test bench in ADS is carried out as below. For Class-AB operation, the best point for the transistor's bias was approximation VGS= -2.8 V to -3 V. The voltage swing and the drain current for the chosen bias point is 5 V to 28V and IDS=84 mA, while the maximum drain current was IDSmax=1049 mA.

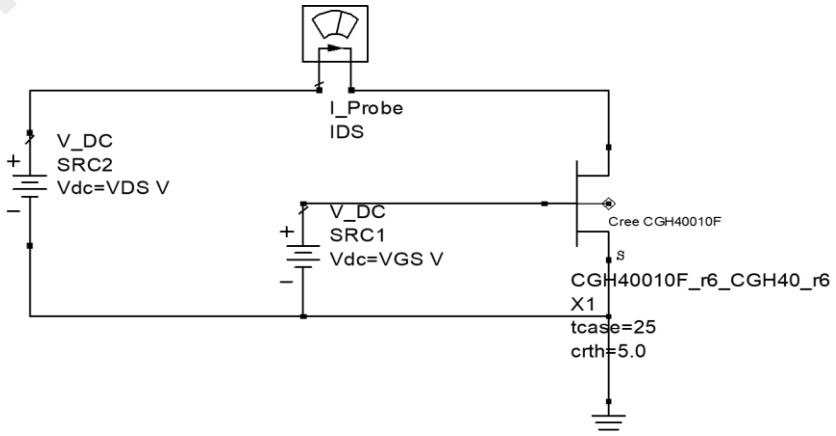


Figure 3.3: Schematic of GaN HEMT bias characteristic for bias point selection

Device I-V Curves

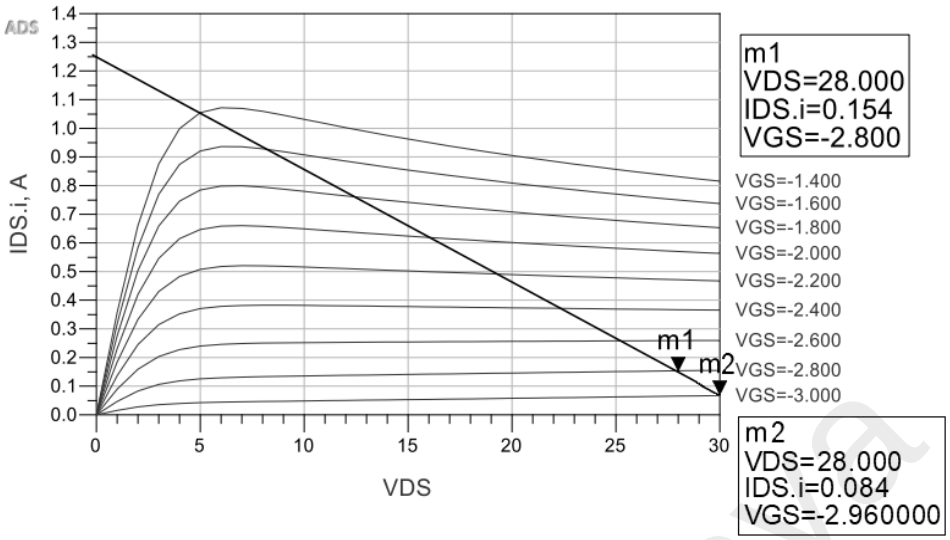
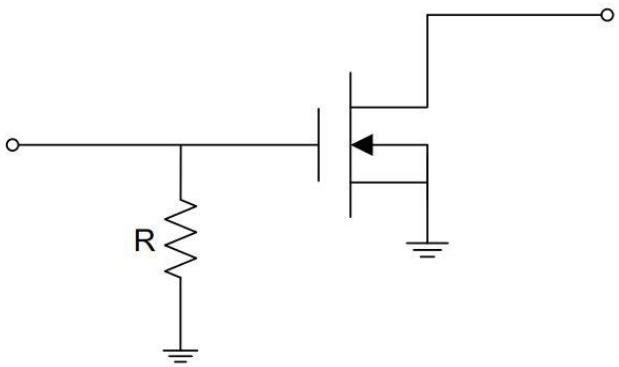


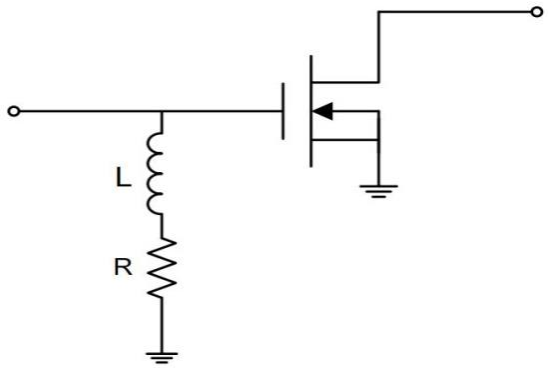
Figure 3.4: IV curves simulation results

3.4 Lossy Matching

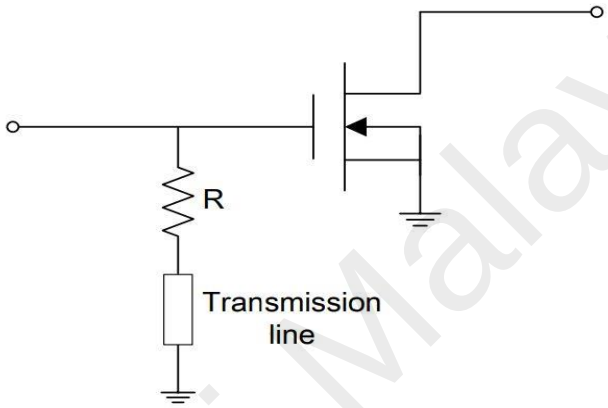
For lossy matching approach, the presences of resistors are designed to absorb the overhead in gain to achieve a flat gain over the whole frequency range. Furthermore, the stability of the amplifier also can be improved with resistors. Usually, lossy matching is much better as input impedance matching, and Figure 3.5 shows a few typical lossy matching networks:



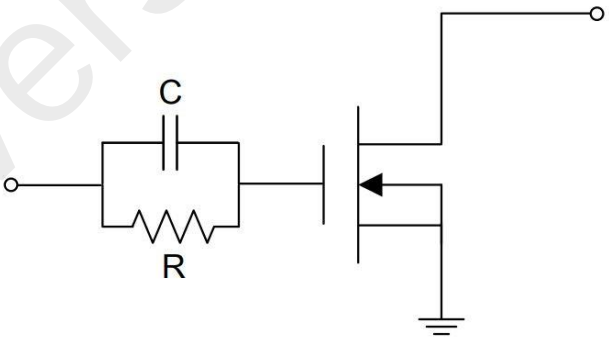
(a) R shunt network



(b) R-L shunt network



(c) R-transmission line shunt network



(d) R-C series network

Figure 3.5: Various types of lossy matching network for the input of device

Figure 3.5 (b) shows the series R-L shunt network; it is the common lossy matching network solution. The impedance of the inductor's is very small at low frequencies, therefore the gain is reduced by the resistor. But, as the frequencies arise to a higher

frequency, the impedance of the inductor also increases while the resistor has minimal effect on reducing the gain. Therefore, the roll-off of the gain is compensated by the positive slope of the gain of the R-L shunt network.

The reason for how the series R-L shunt network renders the gain flat has been quantitatively clarified. Here, it would be analysed in a particular manner. Figure 3.6 shows R-L shunt network as input. For this particular case, the circuit has been designed with multiple section networks of LC. Figure 3.7, and Figure 3.8 shows the equivalent circuit and the amplifier's input part. This implies that by incorporating R-L shunt network in the input matching, if R and L's values are selected correctly, lossy matching can be considered a decent matching network over the required bandwidth. Based on Figure 3.8, the virtual resistance ($R_{virtual}$) is equal to the gate node's impedance. Moreover, the multi-section network is lossless. Thus, the following equation (3.0) shows the V_g is constant across the frequencies.

$$Vg = (2Rvirtual * Pavs) \tag{3.0}$$

In this project, the R-L shunt network and R-C series network are analyzed, as for other networks, it can also be analyzed with this same method.

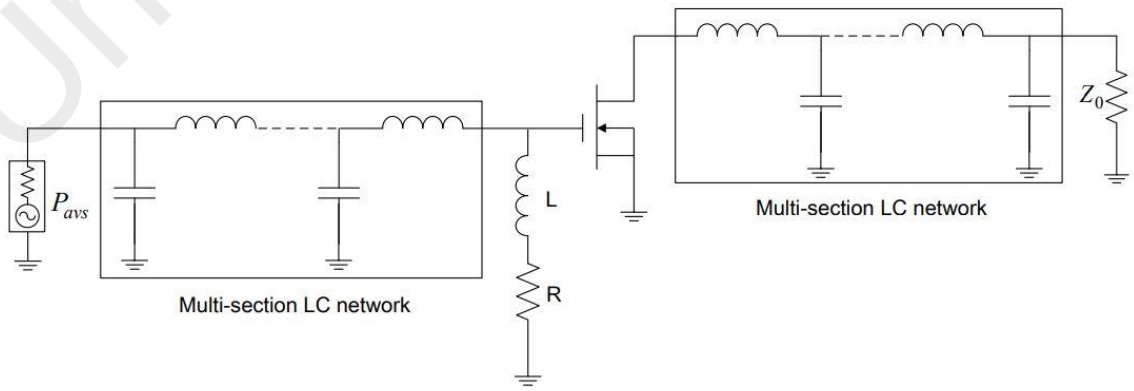


Figure 3.6: The schematic of a power amplifier with R-L shunt network as input

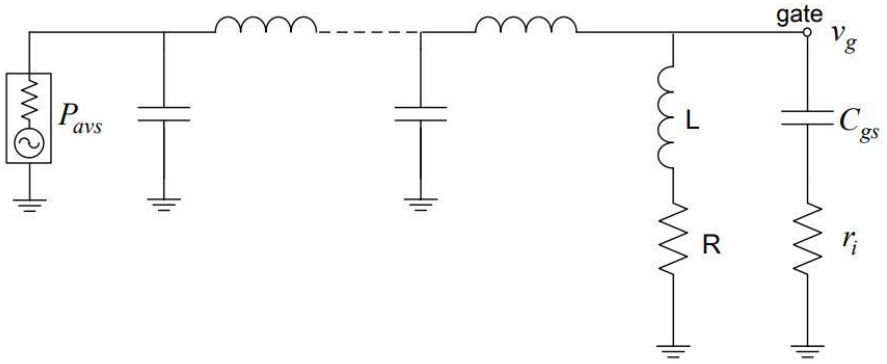


Figure 3.7: R-L shunt network as the input of power amplifier

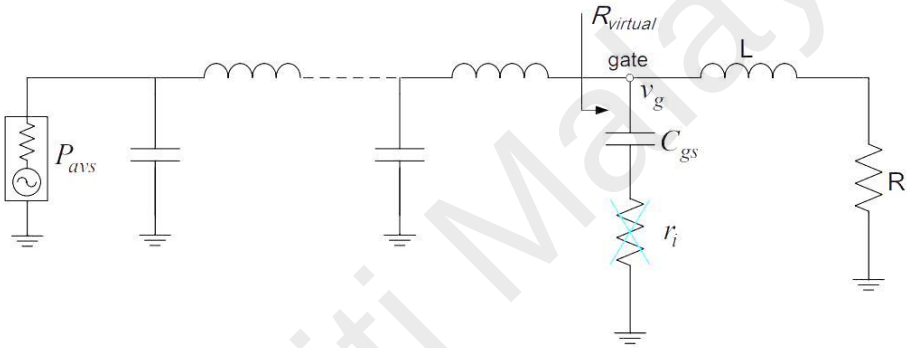


Figure 3.8: The equivalent circuit of: R-L shunt network as the input of power amplifier

3.4.1 Input Lossy Matching Network

The PA designed incorporated the R-L shunt and R-C series network as input matching. The topology of the circuit is shown in Figure 3.9. The matching for the input is to deliver maximum power transfer. To design the input matching, the source-pull result is required to obtain the best impedance matching points for the targeted frequencies of 0.8 GHz and 2.1 GHz, shown in Table 3.1, and the results are far from the ideal 50 Ω. Therefore the R-C series network is introduced as a stability network to the input matching network to make the resistance value not much deviate from 50 Ω and also to improve the lower frequency stability. During the low frequencies, the

capacitor behaves as an open circuit, whereas at high frequencies, the capacitor acts as a short circuit. When the frequency increases, the impedance of capacitors will decrease and vice versa. Thus, the optimum load impedance is transforming to the value shown in Table 3.2, seen at the transistor's input terminal. The values of all the relevant components in this design are shown in Table 3.3. The results of the simulation are shown in Figure 3.10. This lossy matching can be used to broaden and to achieve dual-band design as well. It shows decent return loss S11 in two distinct bands at 0.8GHz and 2.1 GHz. By decreasing the inductance and increasing the capacitance, the lossy match's bandwidth can be increased and will result in a decrease in the Q value. Moreover, by increasing the inductance and decreasing the capacitance, the Q value will be increased, and the bandwidth will be narrower.

Table 3.1: Input Impedance Matching

Frequency (GHz)	**Impedance (Ω)**
0.8	18.536 + j10.481
2.1	3.088 + j10.095

Table 3.2: Input Impedance Matching after factoring the Stability Network

Frequency (GHz)	**Impedance (Ω)**
0.8	56.91 + j8.48
2.1	48.38 + j18.78

Table 3.3: **The values of essential components in the schematic of R-L shunt and R-C series matching topology**

Component	Value
L1	10 nH
L2	1.8 nH
L3	1.0 nH
L4	220 nH
C1	5.6 pF
C2	1000 pF
C3	12 pF
C4	0.5 pF

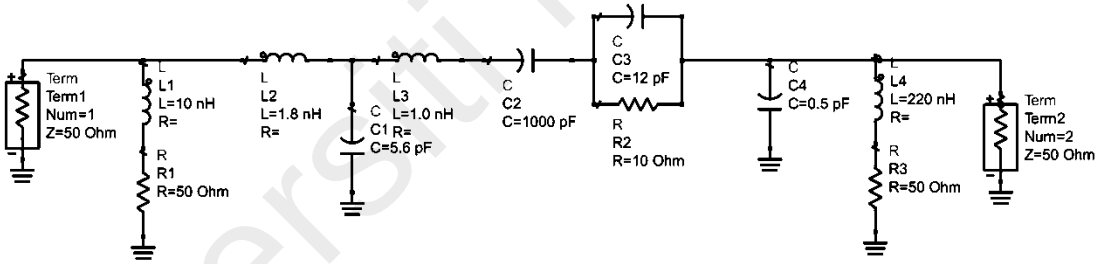


Figure 3.9: The simulation schematic for lossy match: R-L shunt and R-C series network

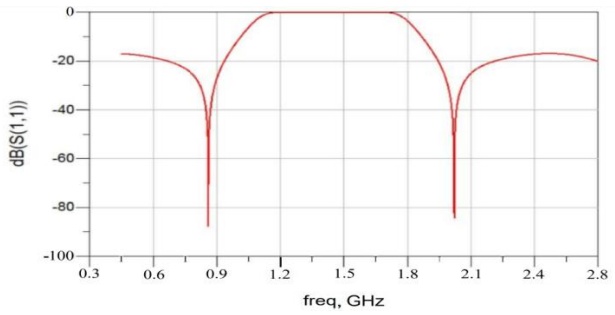


Figure 3.10: The simulation result for lossy match: R-L shunt and R-C series network

3.5 Transmission Line: Microstrip

The microstrip transmission line was applied to the DPA system. It consists of a grounded metallization surface covers at the bottom of the dielectric substrate, height between the trace and reference plane ~~"h~~", the dielectric constant ~~"ϵ_r~~" of the material used, the thickness of the trace, and the width of the conductive strip are ~~"t~~" and ~~"w~~" which is display in Figure 3.11. In the transmission line for microwave, specifically in Monolithic Microwave Integrated Circuits (MMICs) and microwave integrated circuits, the most frequent application is microstrip. This is because microstrip has advantages compared to the stripline as it will enable the majority of the active components to be soldered or integrated on top of the PCB.

However, it has a few down points in the context of disadvantages as the external shield is required when switch or filter is needed for high isolation. The spurious signals that arises during circuit response might lead to losses due to radiation. Considering that some signal travels at a relatively different speed from each other, it is considered dispersive, to which it is one of the microstrip minor issues. Due to the microstrip's filling factor, it is unable to support the mode of Transverse Electro-Magnetic (TEM).

However, the open structured microstrip has major fabrication advantages compared to stripline and coplanar waveguide because of the interconnection, adjustments, and simplicity of practical realization.

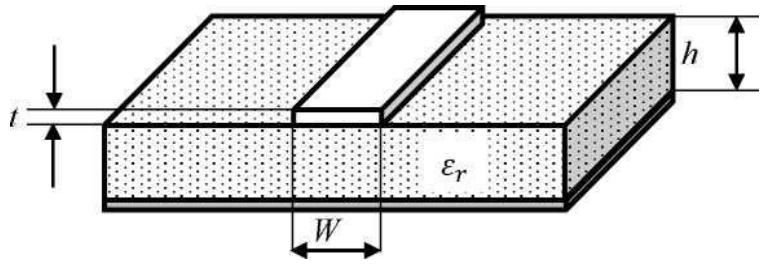


Figure 3.11: Structure of the microstrip line

During the design process of PCB, it is essential to calculate the impedance of the microstrip as a reference to the Characteristic Impedance (*Zo*). For a lossless microstrip, the characteristic impedance can be calculated using the equation below:

$$Z_O = \left[\left(\frac{120\pi}{\sqrt{\varepsilon_r}}\right)\left(\frac{h}{W}\right)\left(\frac{1}{1+1.735\varepsilon_r^{-0.0724}\left(\frac{W}{h}\right)^{-0.836}}\right)\right] \tag{3.6}$$

For this project, Figure 3.12 shows the characteristic impedance of Normalized Microstrip Width (W/h), with Relative Permittivity (ε_r) of 3.66 when the thickness is zero in the function. The empirical shows a decent approximation in terms of line impedances in the range of 50 to 166 Ω. Therefore, the thickness of the microstrip has to be taken into account during the design phase.

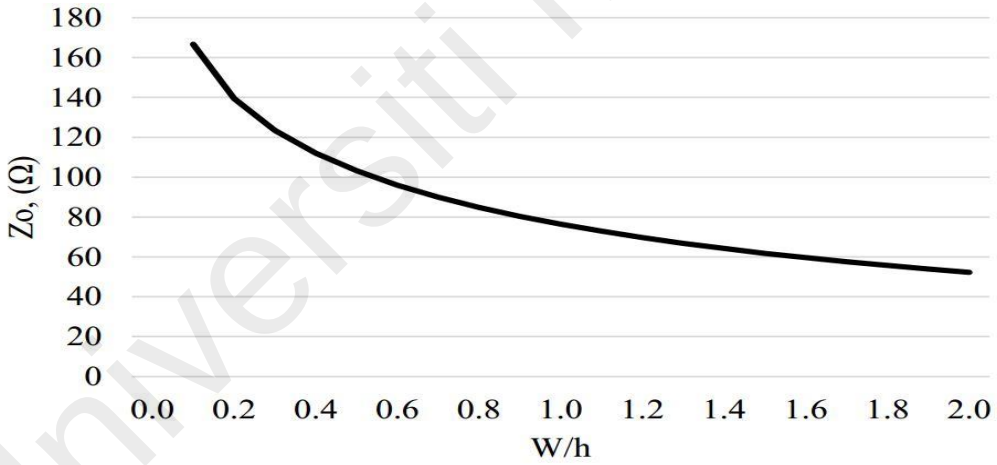


Figure 3.12: Characteristic impedance *Zo* versus *W/h*

Nonetheless, the Keysight ADS' LineCalc tool has alleviated the mathematical with more accurate calculation to get the microstrip's length and width. For the next topic, a method for the lumped inductor to microstrip conversion will be discussed.

3.6 Power Splitter Design

The power splitter chosen for this project is known as the Wilkinson power splitter. It has a three-port network with the ability to provide big isolation between these output ports. In this research, Wilkinson splitter is applied in the Doherty PA's input to provide symmetrical splitting of the input power before it is fed into the Class-AB and Class-C PA. (Note: Wilkinson splitter is only for simulation testing purpose only)

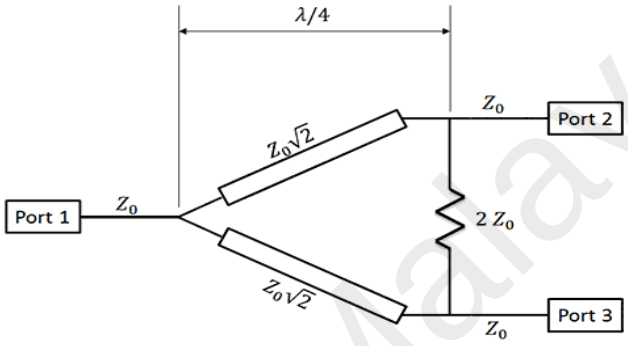


Figure 3.13: Schematic of basic Wilkinson splitter

Figure 3.13 shows the basic schematic diagram of the power splitter. It incorporated $\frac{\lambda}{4}$ quaterwave transmission line specifically at the center frequency. As for lower RF frequencies, the quaterwave may not be a wise choice as it can have unrealistic dimensions due to the presence of large wavelength. With the reason for the size constraints, the lumped element is preferable to replacing the $\frac{\lambda}{4}$ transmission line, as shown in Figure 3.14.

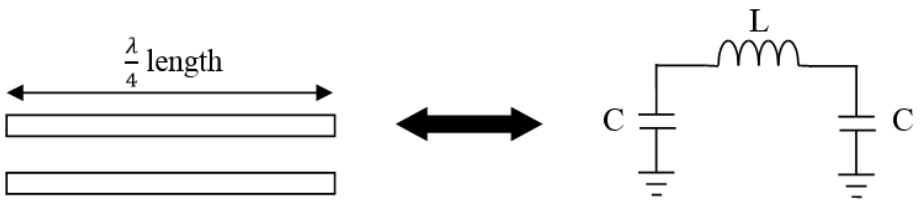


Figure 3.14: Lumped element π-section by using transmission line representation

The transmission line's conversion into the lumped element only has the effectiveness at the Center Frequency (f_c). As a result, the performance between the lumped element and transmission line should exhibit the same characteristic. The pi *LC* network is equivalent to a low-pass filter, which removes the high-frequency signal.

The basic power splitter circuit has been constructed using ADS software, as shown in Figure 3.15. The Wilkinson splitter has the characteristic impedance of 50 **Ω**, while for the value of f_o is determined by means of *L* and *C* elements of the Wilkinson splitter, there will be no electrical tuning require.

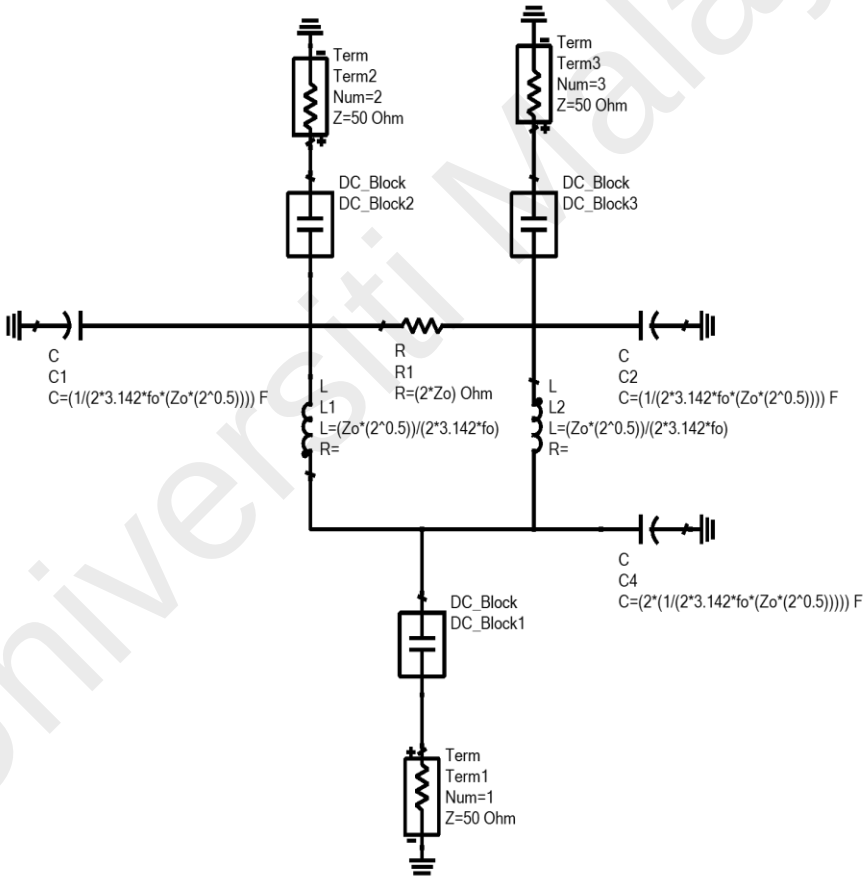


Figure 3.15: Circuit diagram of the Wilkinson network

Based on the theory of Wilkinson splitter, the analysis of lumped element's empirical formulation for Figure 3.15 is shown on the next page:

$$R = 2Z_o \tag{3.1}$$

$$Z_L = \sqrt{2}Z_o \tag{3.2}$$

$$L = \frac{Z_L}{\omega} \tag{3.3}$$

$$\omega = 2\pi f \tag{3.4}$$

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{3.5}$$

Based on the calculation, the value of the components is obtained, and the design was run in the simulation, shown in Figure 3.16. The purpose of the resistor to place in the middle of the splitter is to maintain high isolation.

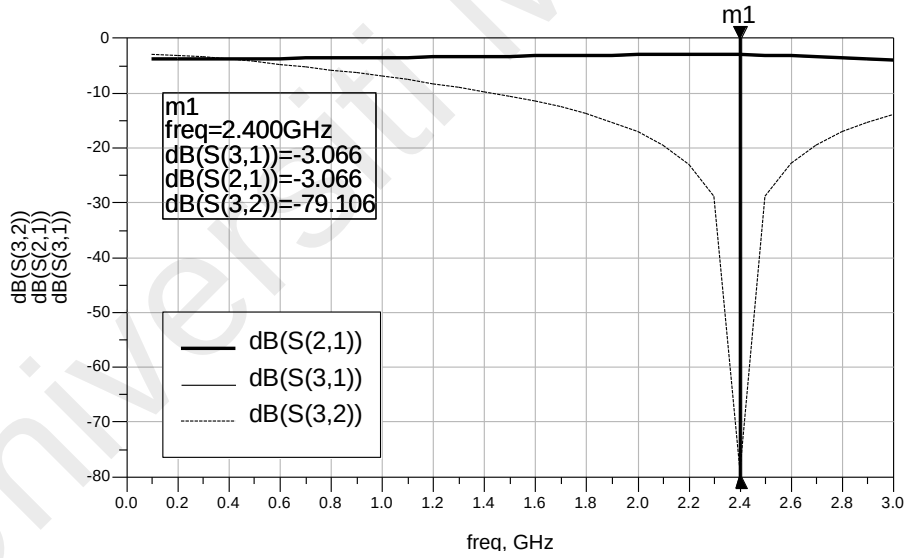


Figure 3.16: Simulation results of power splitter design

The coefficients of transmission at 2.4 GHz are represented by the coefficient of S(3,1) and S(2,1). The coefficient of isolation amid both of the ports is represented by S(3,2). Figure 3.8 indicates a decent and reliable design as per the calculated values. The maximum value of the insertion losses at 2.4 GHz is -3.066 dB.

Next, to determine the material of PCB used for the research. Rogers 4350B is selected, and substrate parameters in Table 3.4 need to identify based on its datasheet as input parameters in Figure 3.19 LineCalc tools in ADS software.

In the component parameters, the desired frequency is set to 2.4 GHz. The purpose of using the LineCalc tool is to synthesize the physical property such as length L and width W for the microstrip line.

Table 3.4: Parameters of ROGERS 4350B Laminate

Parameter	Value
Substrate thickness	0.508mm
Relative dielectric constant	3.66
Relative permeability	1
Conductor conductivity	4.1×10^7 Siemens/meter
Dielectric loss tangent	0.0034

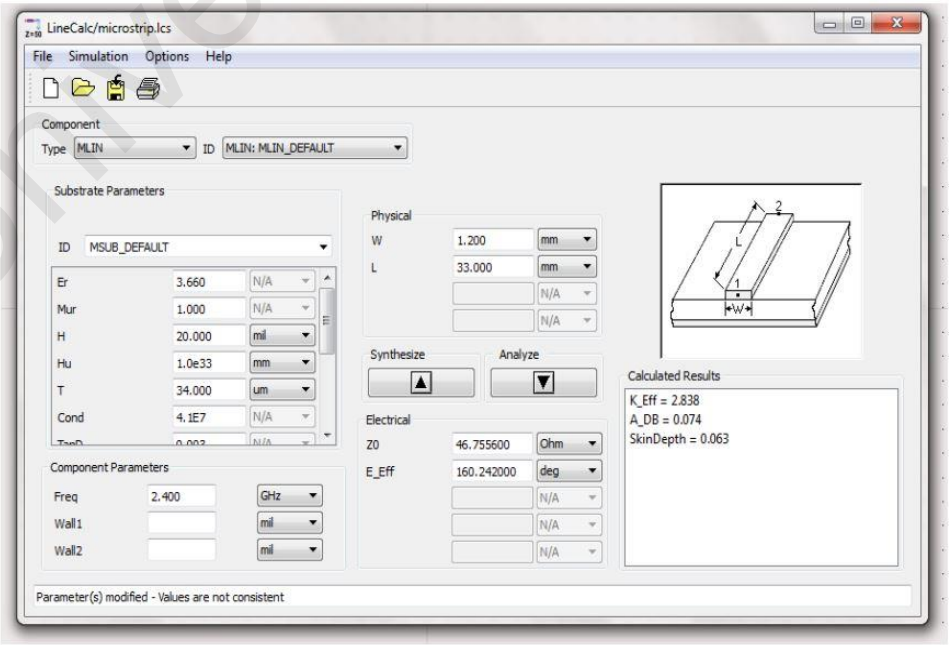


Figure 3.19: LineCalc tools interface in ADS

Therefore, the electrical parameters have to be determined with the aid of reactance of an inductor formula as followed:

$$X = 2\,\pi f L \tag{3.7}$$

Where f represents the design frequency, and L is the inductance in a network. Besides, the reactance of the inductor can also be expressed in terms of characteristic impedance Zo and electrical length θ,

$$X = Z_O = \sin\theta\,, \theta < 45^O \tag{3.8}$$

The lossless matched transmission line with an electrical length θ less than 45^O. Table 3.5, represents the calculations of lumped elements to microstrip line conversion at gate line input matching network according to equation (3.7) and (3.8), respectively. Whereas In Figure 3.20, the input matching network for the system is constructed in ADS. Circled in red represents the lumped inductors that need to be replaced with microstrip line.

Table 3.5: Electrical parameters determination

Inductance, *L* (nH)	1.0	1.800
Upper band Frequency, *f* (GHz)	2.40	2.40
Reactance, X_L (Ω)	15.08	27.14
Length, θ(°)	19.95	19.96
$\boldsymbol{sin\ \theta}$	0.891	0.896
$\boldsymbol{Z_o(n)}$	44.00	79.90

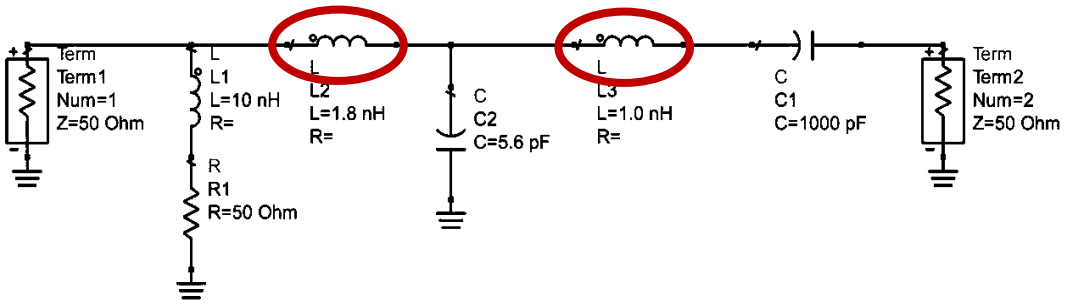


Figure 3.20: **Input matching network**

The value of characteristic impedance Z_O and electrical length θ is obtained and synthesize in the LineCalc tools in order to acquire the value of L and W of a microstrip line. The schematic is simulated with the input value of L and W to obtain inductance values that are close to the actual design value as shown in Figure 3.21. The deviation can be optimized by adjusting the variable of Z_O and θ.

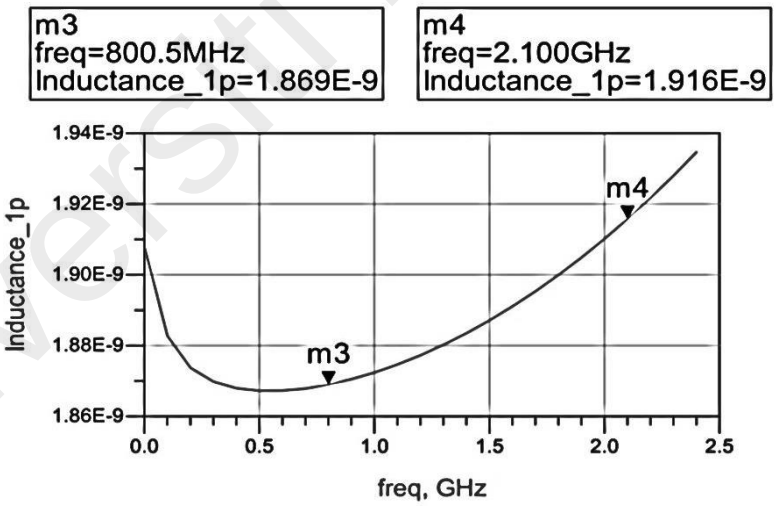


Figure 3.21: Microstrip conversion for actual inductor 1.80 nH

Figure 3.21 has delivered the least deviation for the actual value of inductor 1.80 nH from the simulation. The same procedure is repeated for other value of inductor conversion to the microstrip line. Ultimately, all the lumped inductor is replaced with the microstrip line, as shown in Figure 3.22.

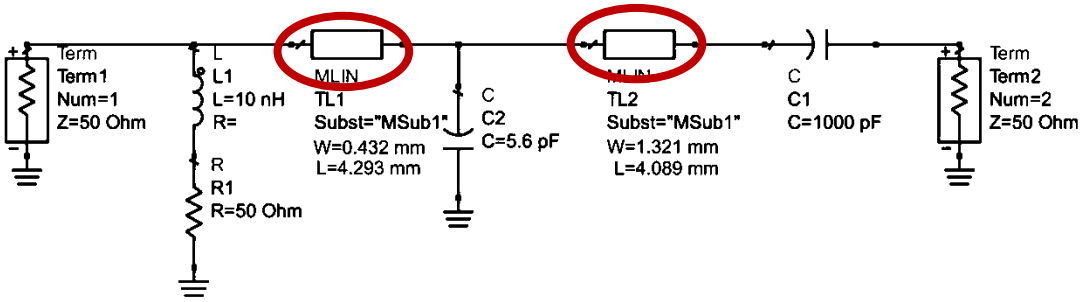


Figure 3.22: Lumped Inductor replaced with microstrip

3.8 Capacitor conversion with the industrial realization

Capacitors are lumped elements that store electrical energy in an electric field between two plates or electrodes when a voltage is applied across them. The circuit of an ideal value capacitor with the industrial capacitor model is constructed as in Figure 3.23, and there are both connected to a 50 Ω termination.

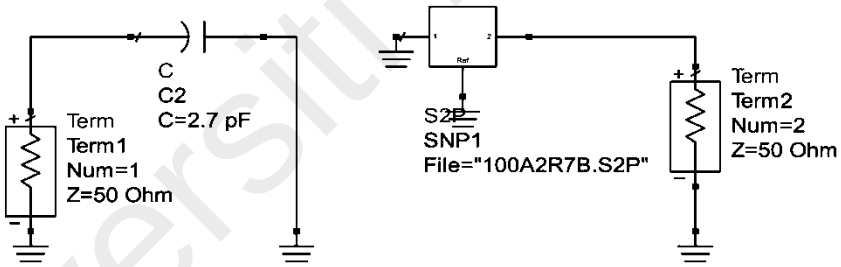


Figure 3.23: Circuit diagram of an ideal capacitor and an industrial capacitor ATC 100A model. (Corp., 1996)

The model of industrial capacitor that implement in this work is ATC 100A series capacitor from American Technical Ceramic Corp., which is a surface-mounted device that has the most versatile high Q, and high self-resonant multilayer capacitor. Typically function as bypass, coupling, tuning, feedback, impedance matching, and DC blocking. In order to run in ADS simulation, the source file of the capacitor model is required and inserts them according to the part number of the capacitor. The 2-port S-parameter component (S2P) is used as a function of data extraction from the industrial capacitor

model. Therefore, the value that is closed to the value of an ideal capacitor is chosen.

The capacitors constructed at the DPA matching network have to be replaced by the actual capacitor value, as shown in Figure 3.24. The simulation in Figure 3.25 represents the results of the actual ATC capacitor model with 2.7 pF in ADS.

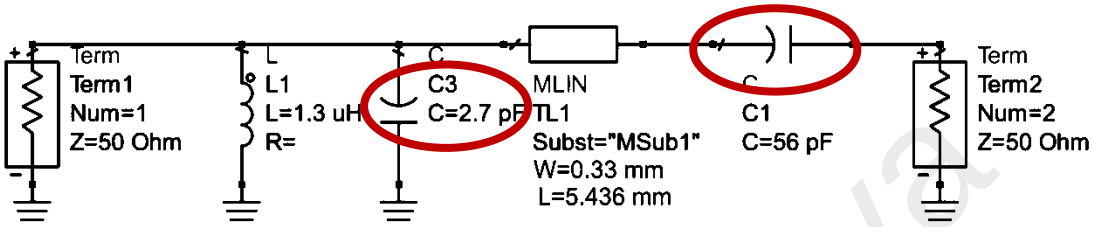


Figure 3.24: **Output Matching Network of lumped capacitors that needed to be replaced with industrial capacitors**

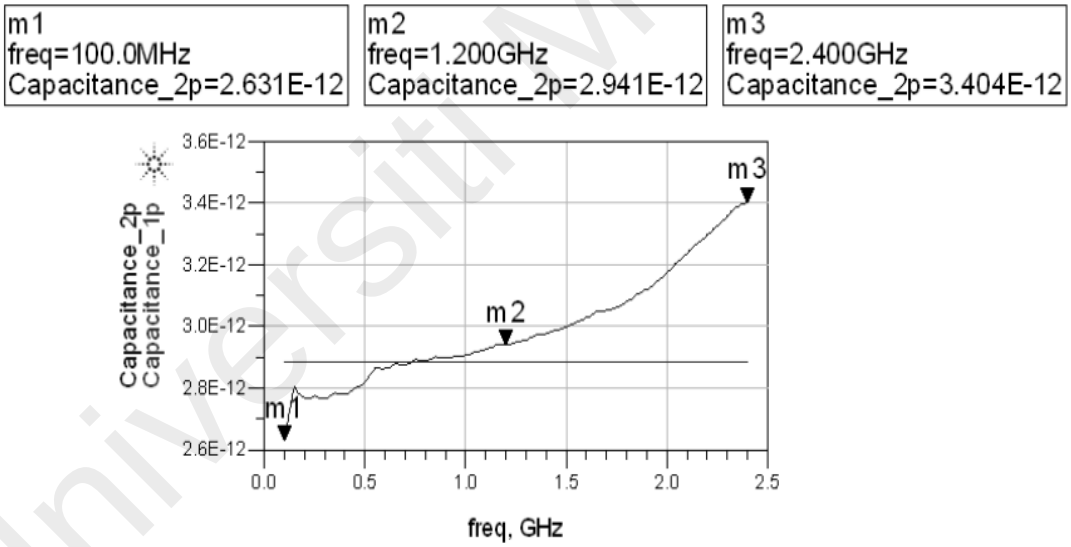


Figure 3.25: Simulation result for ATC capacitor 2.7 pF over the operating frequency

For instance, the real capacitor at 2.7 pF is chosen to replace the 2.886 pF ideal capacitor. According to the simulation result, the deviation between the real capacitor with the simulated value is significant. Therefore, it is crucial to select the suitable real capacitor closely matched with the ideal capacitor value to maintain the overall performance while implementing in prototype board.

This lumped inductor and capacitor conversion technique has been employed in the overall system of the DPA. In Figure 3.26, the capacitors in the input matching network have successfully converted to the ATC model capacitor to carry on DPA simulation.

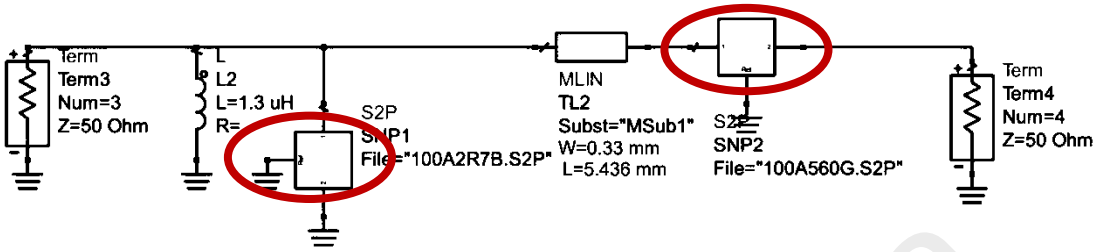


Figure 3.26: Ideal capacitor to industrial capacitor conversion

3.9 Load Modulation

The easiest way to describe the concept of load modulation is shown in Figure 3.27, as the Voltage-Controlled Voltage Source (VCVS) is designed in shunt configuration together with the Voltage-Controlled Current Source (VCCS) concomitant with the resistor acting as the load. The current **I2** able to affect the value of impedance **Z1** perceive by VCVS.

$$Z_1 = \frac{V_1}{I_1} = \frac{V_1}{I_R - I_2} \tag{3.9}$$

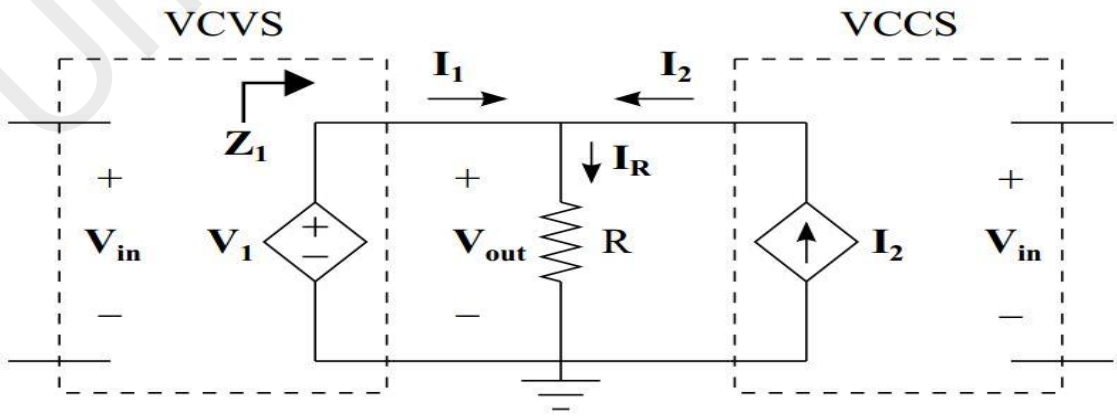


Figure 3.27: The load modulation concept illustrated using a VCVS and a VCCS

By changing the value of current I2 with respect to IR from 0 and corresponding to the variation of Z1 from R to infinity. In DPA, I2 is used to modulate Z1; as a result, it is used to locate the best impedances performance, which would able to ensure the amplifier operate at higher efficiency at 6 dB back-off from maximum saturated power. Figure 3.27 indicates about the linearity of the total DPA system; it shows the factor that affects the system is due to the VCVS linearity, as the V1 is equal to the output voltage Vout throughout the load *R*. As a result, in a condition where the Vin and V1 have proportional linearity, then the system will be linear despite different in the current I2.

The impedance Z1 is engineered to trace the profile of impedance versus Vin. This can be done by detailing I2 versus Vin profile, as it is a function used to improve efficiency at the back-off output power. In terms of empirically, there are difficulties in defining the function as more advanced methods are required in the typical DPA to fulfill the I2 versus Vin profile. Therefore, for the method of load modulation, the VCVS is used assures the amplifier's linearity, while the VCCS is represented as the device with load modulation, in which the I2 versus Vin profile shapes what VCVS sees at the impedance Z1.

3.9.1 Load Modulation with VCCSs only

For the load modulation method to be feasible, it is essential to note that a transistor's behavior does not act as a voltage source. Instead, it acts as a current source. Figure 3.28 shows the quarter-wave transmission line is used to convert VCCS into VCVS in the main amplifier, while in peaking, VCCS is applied for modulation of the impedance Zm seen by the main amplifier.

The differences between Figure 3.27 and Figure 3.28 is the lack of input phase alignment quarter-wave impedance transformer in Figure 3.27. Moreover, the quarter-

wave impedance transformer has a limitation as it causes restraint in bandwidth. As a result, Figure 3.28 require to consider the effect of changing in frequency θ and also the relationship of Ia and Im in terms of phase differences, or the relationship between Via and Vim.

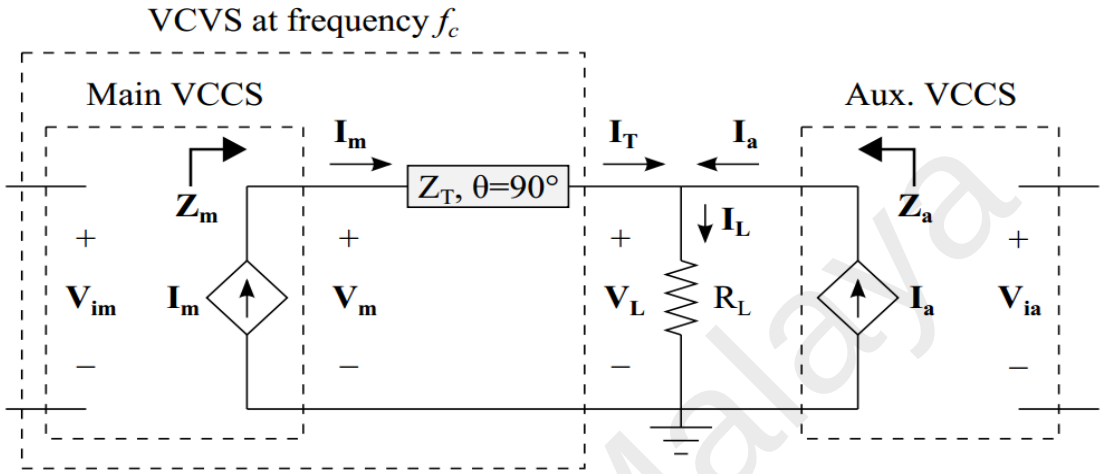


Figure 3.28: The DPA load modulation scheme with VCVSs only

For analysis of Figure 3.28, the transmission line is substituted by ABCD parameters, which are shown in the matrices below:

$$\begin{bmatrix} V_m \\ I_m \end{bmatrix} = \begin{bmatrix} \cos\theta & jZ_T \sin\theta \\ j(\frac{1}{Z_T}) \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_L \\ I_T \end{bmatrix} \tag{3.10}$$

The ZT and delta θ each indicate the characteristic impedance and electrical length of the transmission line. If the middle frequency *fc* equal to 90◦, the equation reduces to:

$$V_L = -jZ_T I_m \tag{3.11}$$

Assuming a linear relationship between Im and Vim, V_L is known as VCVS output, while Vim is the input voltage. This has satisfied the requirement for load modulation, notwithstanding it is specifically for middle-frequency *fc* only. The holistic explanation

regarding the parameters as in Figure 4.3 regardless of any types of angle θ, so the V_L is required for replacement in (3.10) to:

$$V_L = R_L I_L = R_L(I_a + I_T) \tag{3.12}$$

yielding

$$\begin{bmatrix} V_m \\ I_m \end{bmatrix} = \begin{bmatrix} \cos\theta & jZ_T \sin\theta \\ j(\frac{1}{Z_T})\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} R_L(I_a + I_T) \\ I_T \end{bmatrix} \tag{3.13}$$

Based on (3.13), there are two unknowns, which are Vim, the main device's voltage, and IT, the transmission line's current output. In contrast, Via and Vim are the control variables. With further derivation, IT can be determined as follows:

$$I_T = \frac{I_m - jI_a\left(\frac{R_L}{Z_T}\right)\sin\theta}{j\left(\frac{R_L}{Z_T}\right)\sin\theta + \cos\theta} \tag{3.14}$$

and Vm is given by

$$V_m = I_a R_L \cos\theta + I_T(R_L \cos\theta + jZ_T \sin\theta) \tag{3.15}$$

As for Zm and Za, the equation below shows the relationship for the impedances seen by the peaking and the main devices:

$$Z_m = \frac{V_m}{I_m} \tag{3.16}$$

and

$$Z_a = \frac{V_L}{I_a} \tag{3.17}$$

By further substitution of (3.14) into (3.12) and (3.15), the overall expression for V_L and Vm regardless of the θ are stated in terms of *RL*, Im, Ia, and *ZT*. It is also important to determine the right choices of *RL* and *ZT* when Zm is used to find the graph profile for impedance versus the input voltage. Next, the equation of the output power for peaking device and main devices *Pa* and *Pm* are shown as follows:

$$P_m = \frac{1}{2}\Re(V_m I_m^*) \tag{3.18}$$

and

$$P_m = \frac{1}{2}\Re(V_L I_a^*) \tag{3.19}$$

The efficiency of the main and peaking devices are given by

$$\eta_m = \frac{P_m}{P_{dcm}} \tag{3.20}$$

and

$$\eta_a = \frac{P_a}{P_{dca}} \tag{3.21}$$

where *Pdcm* and *Pdca* are the DC power consumption of the main and peaking devices, respectively. The efficiency of the overall DPA is given by

$$\eta = \frac{P_m + P_a}{P_{dcm} + P_{dca}} \tag{3.22}$$

3.10 Design dual-band DPA output matching

In this design, Figure 3.29 shows the schematic design for RCT with the third harmonic resonant circuit. In the output matching design, the application of the third harmonic resonant circuit $L_{t1}C_{t1}$ and $L_{t2}C_{t2}$ provides an open-circuit condition at the fundamental frequency for the carrier and peaking amplifier. Moreover, the presence of series $L_{t1}C_{t1}$ and $L_{t2}C_{t2}$ filters for third harmonic are effective for narrow bandwidth, specifically only for a high band of 2.1 GHz. Furthermore, the value of the matching elements presented through this method is optimized wherever necessary in order to obtain better performance. With the aid of simulation, the circuit is optimized for the improvement of the dual-band matching requirement. The RCT is applied to compensate for the reactance for the lower and upper bands individually as it is crucial to design it to match 50 Ω load to two arbitrary complex impedances seen by the device at both of the desired frequency bands.

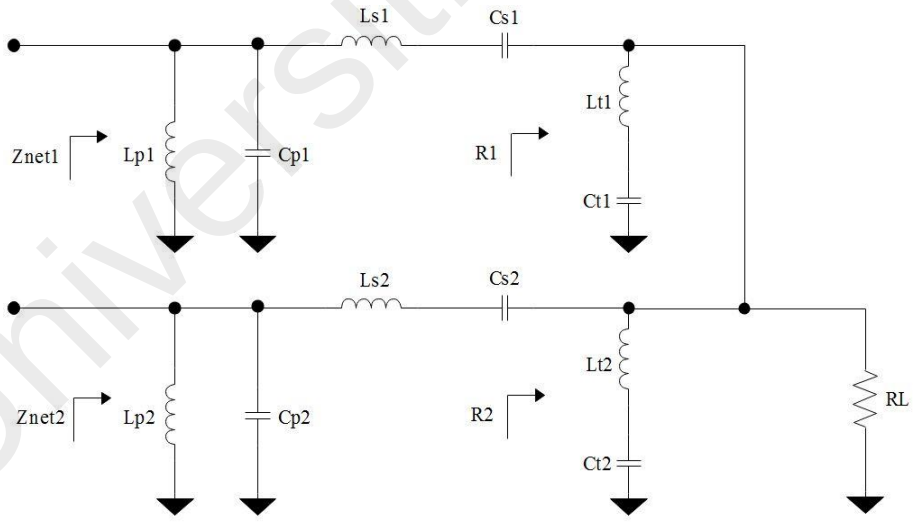


Figure 3.29: RCT with third harmonic resonant circuit

The circuit schematic of dual-band GaN HEMT DPA is shown in Figure 3.30, integrating two 10 W CREE devices CGH40010F with V_{dd}=28 V. The input lossy matching circuit includes a series *RC* circuit and a shunt *RL* circuit to provide dual-band

input matching with minimum input insertion loss. By using the input matching network shown in Figure 3.30 (including a 1000 pF capacitor in series with the parallel combination of a 10 Ω resistor and a 12 pF capacitor), stability is improved at low frequencies (because of the presence of resistor) and the power gain is improved at high frequencies (resistor is bypassed). Next, the output matching network has incorporated the RCT with the approach of optimizing it to match two arbitrary points for two different frequencies of 0.8 GHz and 2.1 GHz when the devices operate at 6 dB back-off. Therefore, the load-pull of output impedances has been extracted at 6 dB back-off region from the device saturation region.

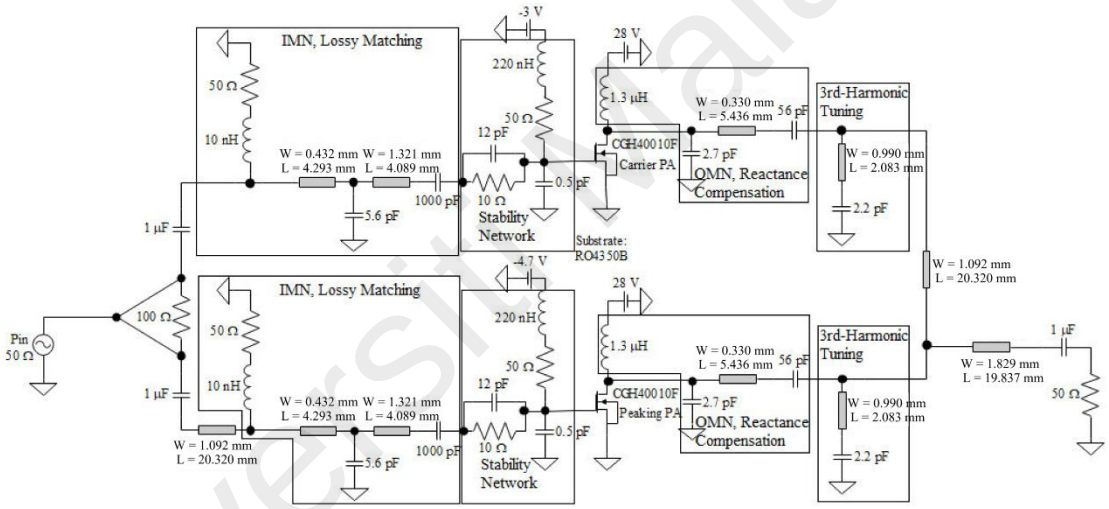


Figure 3.30: Simulated circuit schematic of dual-band GaN HEMT DPA

The result of the optimal output impedances obtained for each frequency will be shown in the result section in Chapter 4. From a practical implementation point of view, the third harmonic resonant circuit concept was optimized and implemented together with RCT at the output matching network. This is to make good optimization or tuning of the overall matching networks (with mixed lumped elements).

3.11 PCB Layout Design

The simulation is done to verify the performance of the dual-band DPA design. Subsequently, the layout for the PCB is designed for the fabrication of the prototype board. The software implemented in the PCB layout design is Multisim and Ultiboard from National Instrument. When the design's final layout is completed, the Gerber file is generated and is ready to send for board fabrication. The layout design of the PCB is shown in Figure 3.31.

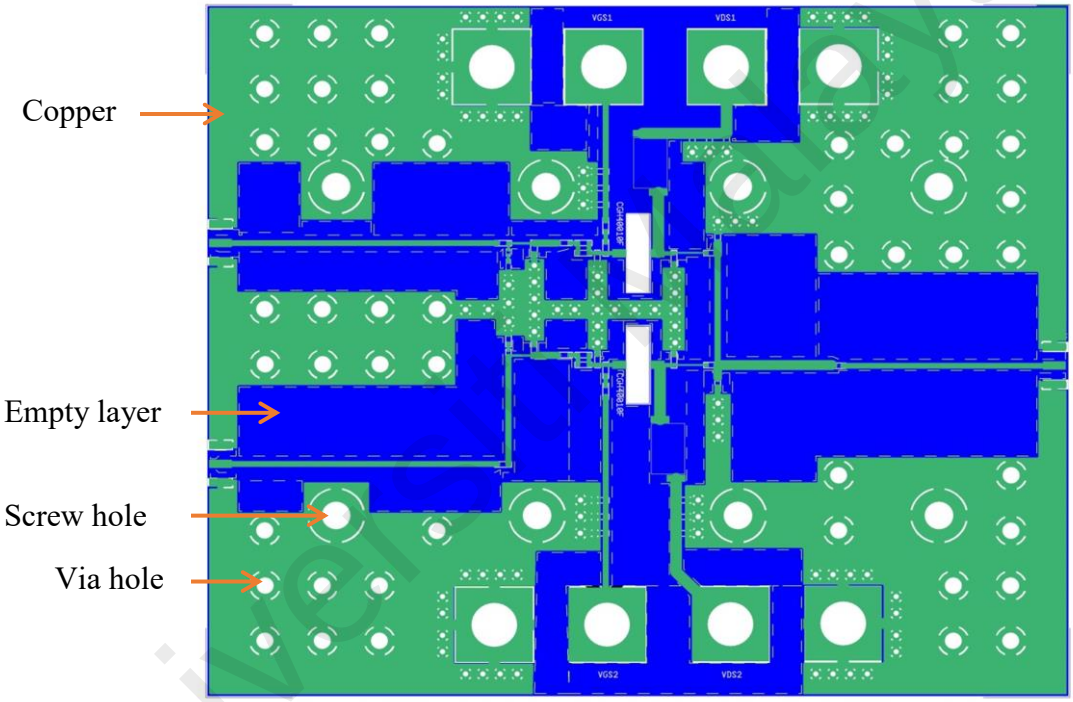


Figure 3.31: PCB layout design for DPA

The green color area is representing the copper, which indicates the conductive microstrip and ground layer. The blue area represents the empty layer. Eight big circles represent the screws hole for the mounting between the PCB and the heat sink in the middle of the layout design. Moreover, via holes are represented by the small circle scattered throughout the board.

3.12 Heat Sink Design

The heat sink is needed in the design of PA; this is because it is used to dissipate the heat away from the PCB. It is designed to be appended together with the PCB, specifically underneath it. Usually, copper will be used as a heat sink because it has one of the best heat conductivity. However, in this case, aluminum is chosen as it cost cheaper than copper, and the heat conductivity of aluminum is also suitable for this project. The heat sink was fabricated by using 7 mm thickness of aluminum. Figure 3.32 and Figure 3.33 shows the design of the heat sink in details.

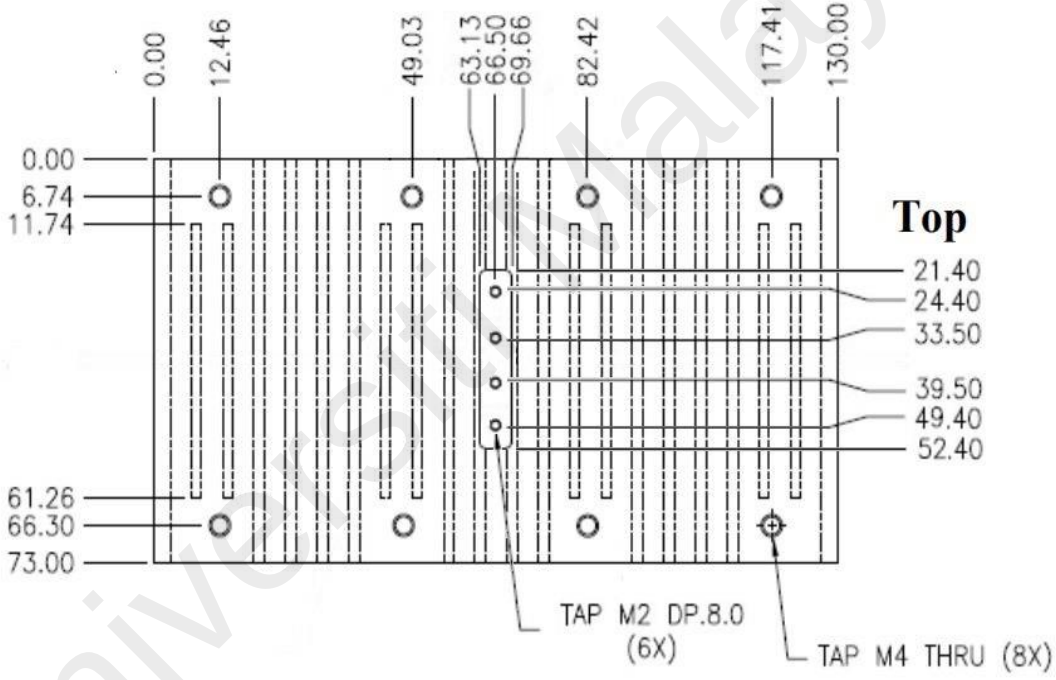


Figure 3.32: Heat sink blueprint (top view)

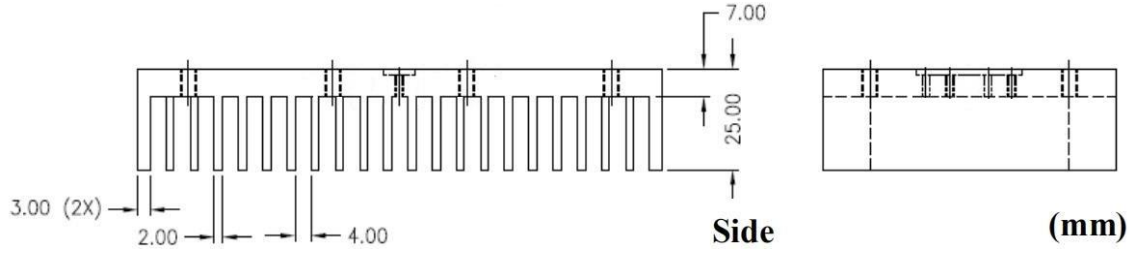


Figure 3.33: Heat sink blueprint (side view)

3.13 PCB Fabrication and Components Assembly

Upon completing the design of the PCB layout, Gerber file was generated and was sent to Circuit Image Sdn Bhd for fabrication. The material used for fabricating the PCB is two layers of Roger 4350B. It has a relative dielectric constant ε_r of 3.66 with a substrate thickness h of 0.508 mm. Moreover, it has an electrical conductivity of 4.1 x 10^7 S/m, the relative permeability of 1, and dielectric loss tangent of 0.0034. During the process of handling the CREE's CGH40010F GaN HEMT transistor, it should be handled with care by using a tweezer and not by bare hands because of the performance of the transistor will be affected by the Electro-Static Discharge (ESD) from bare hands. Next, in order to provide a strong connection between the PCB and the heat sink, a total of eight screws are used to mount under the PCB test board on the heat sink. Furthermore, indium foil is placed between the GaN transistor and the heat sink; this is to ensure good heat dissipation and maximum contact between the heat sink and the transistor. Figure 3.34 (top view) and Figure 3.35 (side view) show the PCB board being fabricated with complete components such as inductors, capacitors, RF inputs, and output ports, RF chokes being soldered onto the PCB together with a mounted heat sink. The board is connected to an external RF Coaxial Wilkinson splitter (380-2500 MHz) which is shown in Figure 3.36.

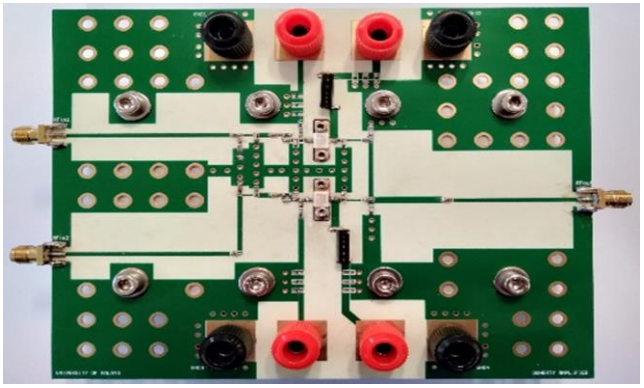


Figure 3.34: The actual prototype of dual-band DPA design board (top view)

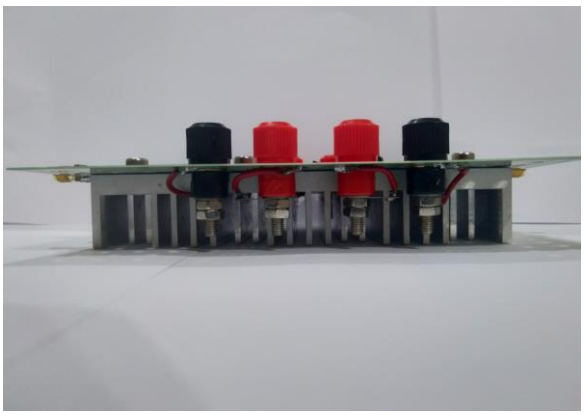


Figure 3.35: The actual prototype of dual-band DPA design board (side view)

Additionally, the board consists of four voltage supply feed for the gate and drain voltage, output, and input matching network, and the overall board size is 125x150 mm^2. Nevertheless, the effective size area occupied by the DPA is much smaller at 73x75 mm^2.

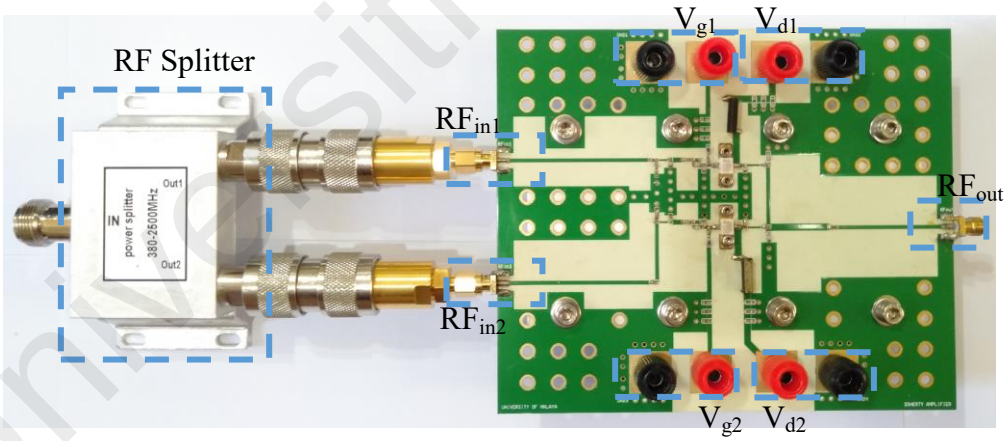


Figure 3.36: The actual prototype of dual-band DPA design board with RF Coaxial Wilkinson splitter (top view)

The open grounding area for the board is well designed with isolation and an adequate amount of via-holes. To minimize the coupling, the RF and DC signals have been cautiously routed. For the DC routing, the width has been carefully picked to provide a good DC current-carrying capacity. Next, to ensure a decent performance of the PA, via-holes are evenly distributed to enhance grounding.

3.14 Measurement Setup

In order to experimentally validate the simulation results of the proposed dual-band high-efficiency DPA, which incorporates the RCT and third harmonic tuning, a prototype board is developed by integrating CREE's CGH40010F GaN HEMT. As a result, to obtain the measurement results, the experimental setup is shown in Figure 3.37. There are several types of equipment being used, such as are Rohde and Schwarz SMA 200A signal generator, Rohde and Schwarz FSV signal analyzer, GW Instek GPS-4303 power supply, HP 6235A triple output power, HP 6205B dual DC power supply, attenuator, and cables.

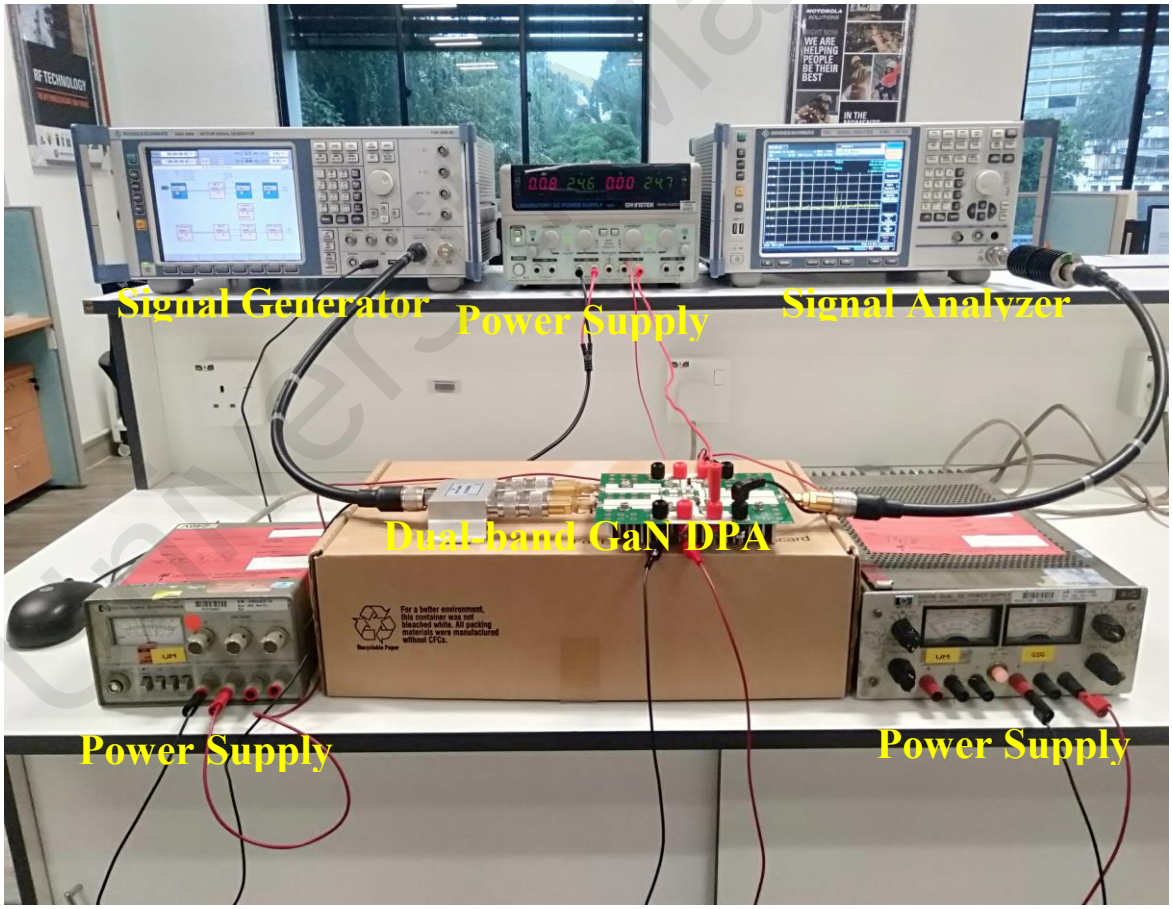


Figure 3.37: Experiment setup for data measurement

The cable used in the experiment setup is N-type cable. In order to protect the vector network analyzer from high RF signal entering, the Aeroflex/Weinschel -3dB attenuator is used. The signal generator provides the RF input power to the PA. The power supply provides the PA's DC power. Safety should be noted as a precaution is needed when operating the device power supply. The drain voltage needs to turn on after the gate voltage, as it is to prevent the circuit from current overflow.

Furthermore, the drain voltage and the quiescent current are 28 V and are in the range of 40-90 mA for both the carrier and peaking PA. For the gate, a bias of -3 V and -4.7 V was applied for the carrier and peaking PA. The measurement data is acquired and the performances of the designed DPA has been analyzed and compared with the simulation result.

3.15 Summary

In this chapter, the methodology of dual-band DPA design is discussed. The DPA's matching network is obtained through the lossy matching network for the input and RCT and third harmonic resonant circuit for the output matching network. The input lossy matching circuit provides us with the dual-band input matching with minimum input insertion loss, while the stability network improves stability at lower frequencies. The output matching network has incorporated the RCT to optimize it to match two arbitrary points for two different frequencies of 0.8 GHz and 2.1 GHz when the devices operate at 6 dB back-off.

The matching networks are realized with lumped inductors converted into microstrip. This method is used because it is more efficient in terms of prototype fabrication, and the performance of the designed device can be enhanced. The definition of a lumped element and distributed element are discussed in this section. The method of converting

the inductor to the microstrip transmission line is also presented in this section, along with the method to verify the equivalent of microstrip to the inductor. The approach of a selection of capacitor value by using ADS is discussed in this section. Also, PCB is fabricated, and the complete PCB with components soldered on it is presented. The measurement setup is presented to obtain experimental data of PAE, gain, and output power.

CHAPTER 4: RESULTS AND DISCUSSION

4.1 Dual-band Doherty Power Amplifier

4.1.1 Output Impedance Results

The results referring to Chapter 3, subsection 3.10, regarding the optimal output impedances obtained for the frequency of 0.8 GHz and 2.1 GHz is shown below.

Figure 4.1 shows the forward transmission S21 for the optimum impedance. Both the forward transmission values are in the range of higher than ~-1 dB, which is considered decent in terms of signal strength.

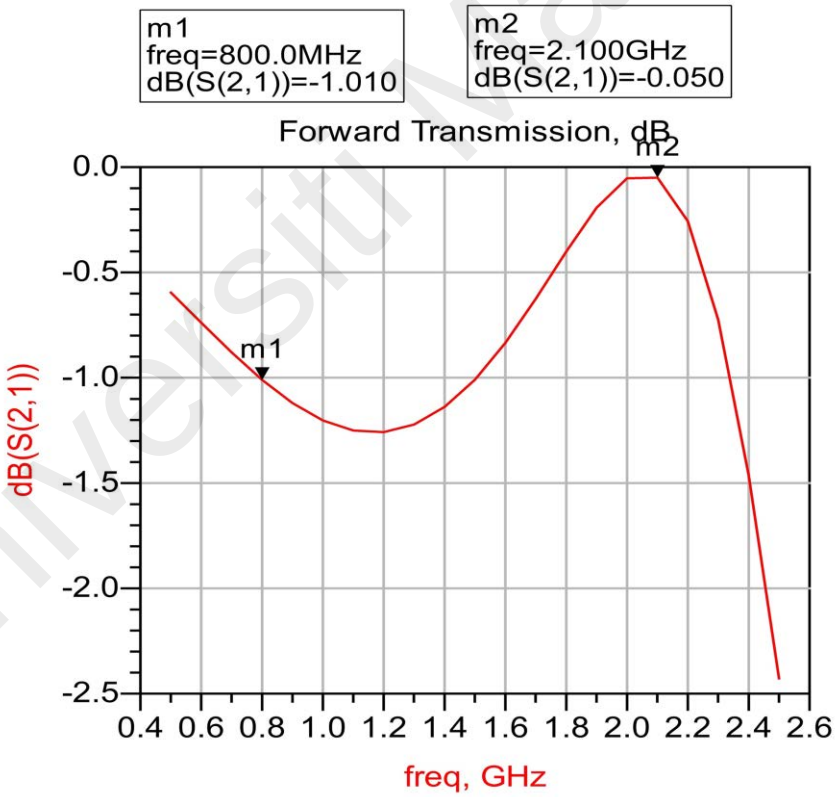


Figure 4.1: Simulated forward transmission S21 of the design DPA

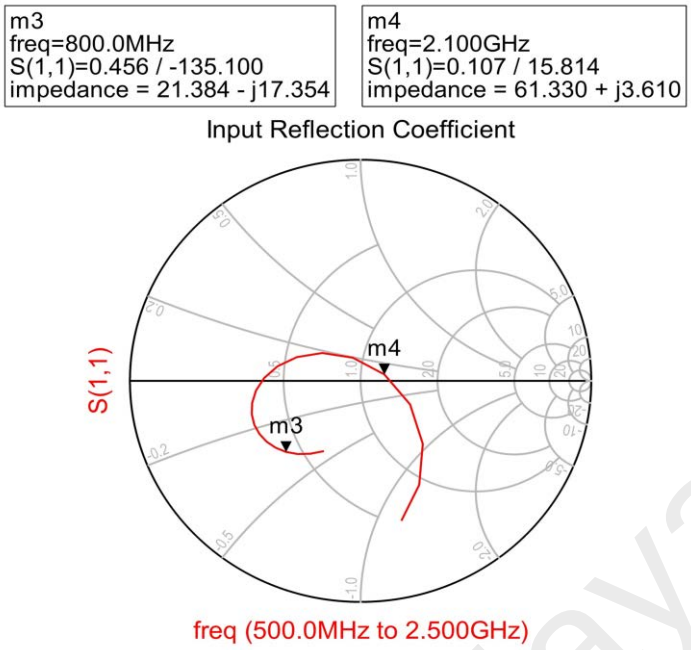


Figure 4.2: Simulated smith chart of S11 of the design DPA

Table 4.1: Optimal output impedances for dual-band DPA

Frequency (GHz)	Optimal output impedance (Ω)
0.8	21.384+j17.354
2.1	61.330-j3.610

Figure 4.2 above showed the simulated performance for the reflection coefficient S11. The load-pull of optimal output impedances for dual-band DPA was showed in Table 4.1. The output matching network was designed to match the optimal output impedances' value to achieve acceptable performance. The results of the overall performances will be shown in subsection 4.1.2.

4.1.2 Simulation and Measurement Results

The result of the measurement for simulated and experimental will be shown in this section. The simulation results were obtained from harmonic single tone PAE simulation, and the circuit schematic diagram referring to this simulation is shown in

Figure 3.30. Whereas the measured data were obtained based on the experimentally set up in Chapter 3, subsection 3.14.

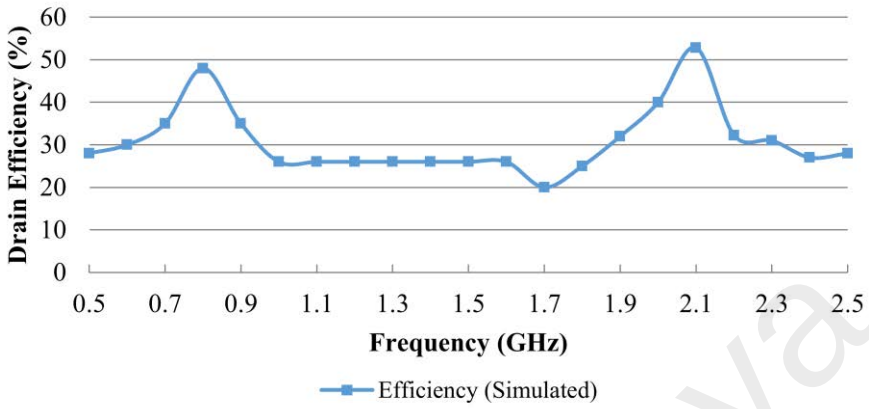


Figure 4.3: Simulated drain efficiency of the prototype board at 6 dB back-off from saturation power

Based on the simulated result in Figure 4.3 above, the drain efficiency against the frequency shows satisfactory performances of 48% and 52.8% at 0.8 GHz and 2.1 GHz, respectively.

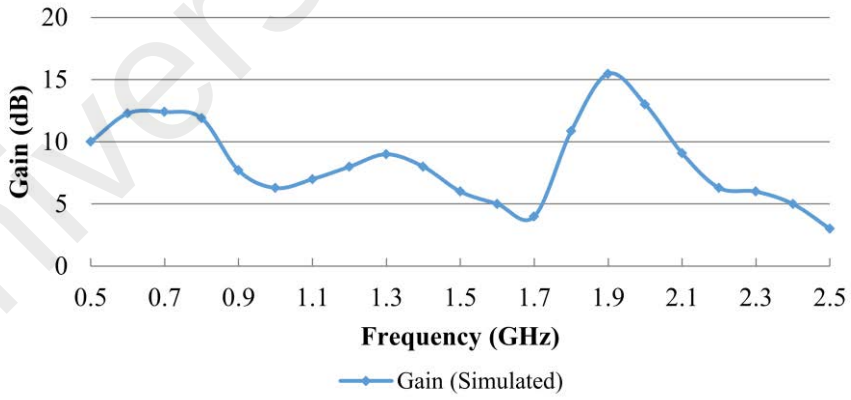


Figure 4.4: **Simulated gain performance of the prototype board at 6 dB back-off from saturation power**

In Figure 4.4, the simulation graph of gain against frequency shows a decent performance at the desired frequency of 0.8 GHz and 2.1 GHz, which is 11.9 dB and 9.1 dB.

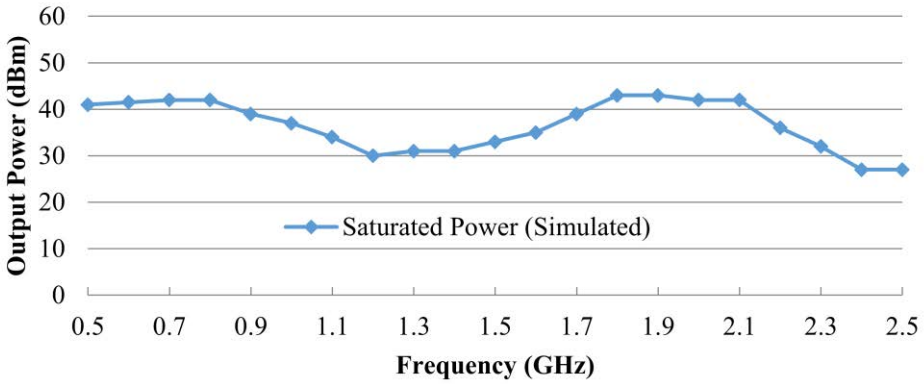


Figure 4.5: **Simulated saturated output power of the prototype board**

The simulated saturated output power against frequency is shown in Figure 4.5. The results show a good performance with the output power of 42 dBm for 0.8 GHz and 2.1 GHz.

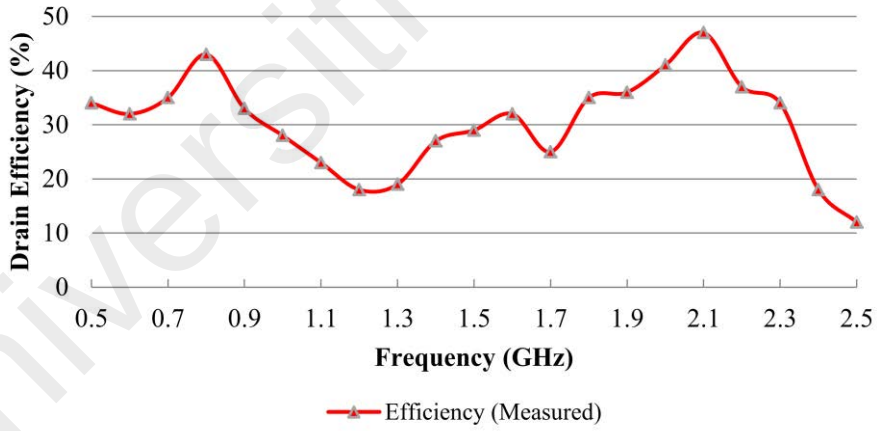


Figure 4.6: Measured drain efficiency of the prototype board at 6 dB back-off from saturation power

The measured drain efficiency against frequency is shown in Figure 4.6. The measured data shows the drain efficiency of 43% and 47% for 0.8 GHz and 2.1 GHz.

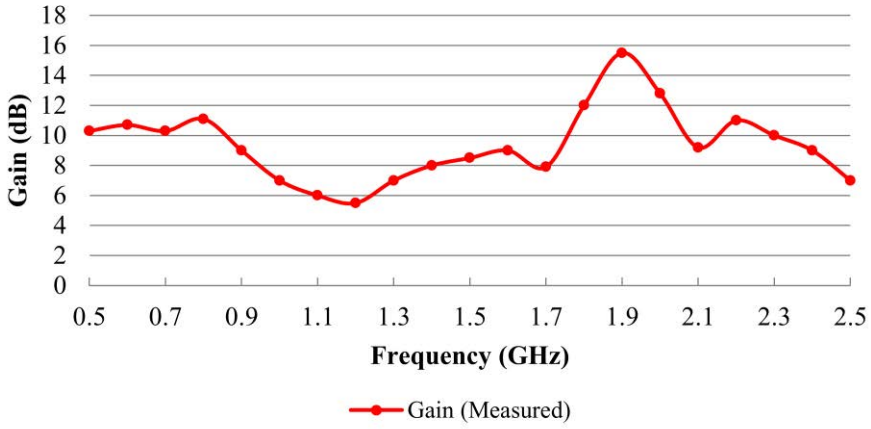


Figure 4.7: Measured gain performance of the prototype board at 6 dB back-off from saturation power

The measured gain performance against the frequency is shown in Figure 4.7. The gain obtained from the measured data demonstrated acceptable performances of 11.1 dB and 9.2 dB in the frequency of 0.8 GHz and 2.1 GHz.

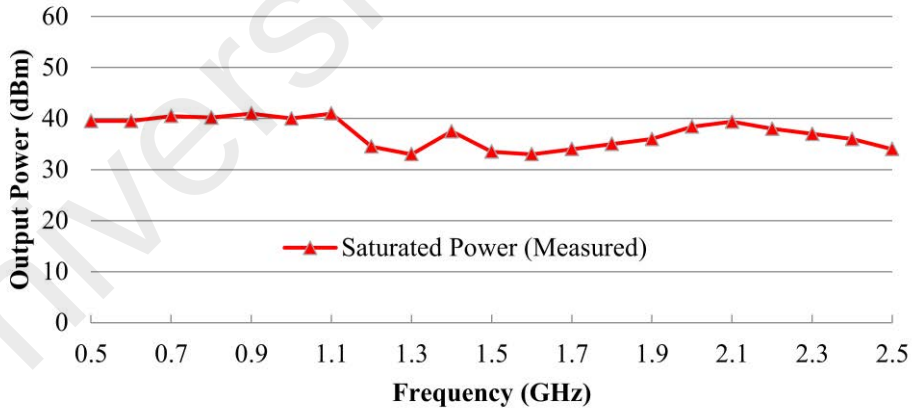


Figure 4.8: **Measured output power of the prototype board**

In Figure 4.8 above, the measured output power against frequency is shown. The results showed a saturated output power of 40.2 dBm and 39.4 dBm for the frequency of 0.8 GHz and 2.1 GHz.

4.1.3 Comparison of Simulation and Measurement Results

The comparison performance graphs between the proposed design's simulated and measured results are shown in Figure 4.9 and Fig. 4.10. Fig. 4.9 shows the simulated gain and the drain efficiency of the dual-band DPA for the frequency of 0.8 GHz and 2.1 GHz, respectively. The measured results show an efficiency of 43% at 0.8 GHz and 47% at 2.1 GHz as compared to the simulated results which shows 49% at 0.8 GHz and 53% at 2.1 GHz for 6 dB back-off points from power saturation. This work has achieved a good result in simulation. However, the simulated and measured results' performance deviate slightly due to the designed DPA in simulation is carried out under ideal condition. This means that in a real-life experiment, the DPA's performance is affected by the non-ideal device characteristics. From the perspective of efficiency, the real transistor's knee region limits the available voltage swing, reducing the efficiency by 9% to 14% compared to the ideal value. Moreover, the peaking amplifier, which is biased at Class-C shows slow turn-on due to the varying conduction angle of the current versus the power, leading to the reduction of power at 6 dB back-off power from saturation. From the linearity perspective, the voltage-dependent capacitance and the non-linear transconductance g_m also cause the DPA to be non-linear in the real-life experiment.

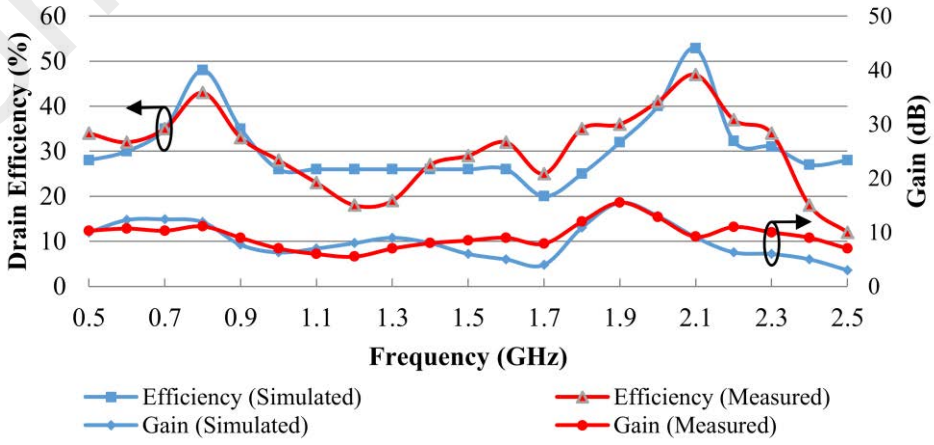


Figure 4.9: Simulated and measured drain efficiency and gain performance of the prototype board at 6 dB back-off from saturation power

The measured gain of the proposed design is in the range of 10 dB approximately. While the measured gain at 0.8 GHz is 9.8 dB, and 9.2 dB for 2.1 GHz, respectively. In a balanced power range mode, both of the bands achieve close to 50 Ω characteristic impedance. Nevertheless, the operation power over the bandwidth is acceptable.

Next, the simulated and measured results of the saturated output power in the frequency range of 0.5 GHz to 2.5 GHz are shown in Figure 4.10. For the desired frequency bandwidth, the saturated output power is achieved at 40.5 dBm. Both the simulated and the measured results agree and show a decent dual-band performance.

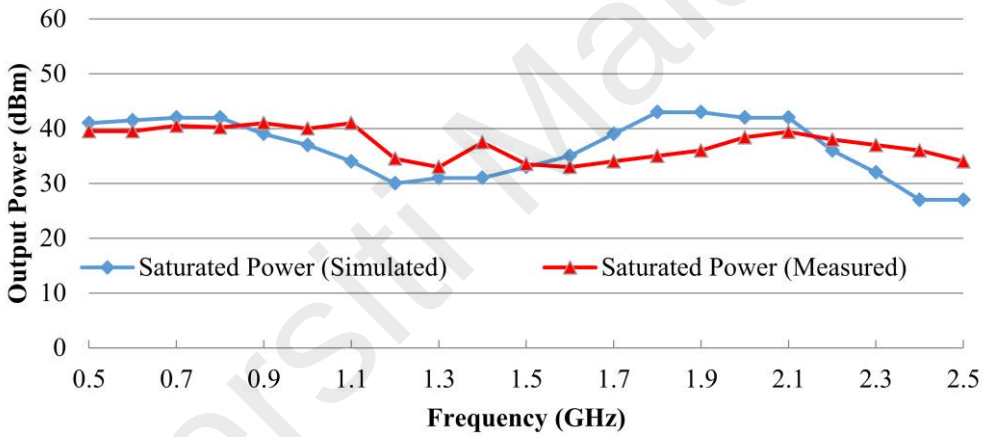


Figure 4.10: Simulated and measured output power of the prototype board

4.1.4 Comparison of DPA Performances with Several Papers

The performances of recent papers in the context of GaN dual-band PA are summarized in Table 4.2. This work shows high efficiency at 6 dB back-off from saturation and gains within the bandwidth of interest. Liu (Mingming et al., 2016) shows high efficiency at 6 dB back-off from the saturated efficiency for dual-band purposes. Nonetheless, their Frequency Ratio (FR) is 1.58, which is regarded as narrow for frequency spacing. For this work, the FR of 2.63 has been realized to satisfy the condition when broad frequency spacing is required. Moreover, this work attains a

much higher saturated efficiency of 60% at 2.1 GHz and retains a good 54% saturated efficiency at 0.8GHz compared to other methods. This work also shows good performances for efficiency at 6 dB back-off without sacrificing the saturated efficiency.

Table 4.2: **Comparison of performances of dual-band DPA in different methods**

Work	Topology	Device	Frequency (GHz)	Frequency Ratio (FR)	Saturated Efficiency (%)	Efficiency (%)	Saturated Power (dBm)	Saturated Gain (dB)
			f_1/f_2	f_2/f_1	f_1/f_2	f_1/f_2	f_1/f_2	f_1/f_2
(Zheng, Liu, Yu, Li, & Li, 2014)	Simplified phase offset-lines	GaN	0.9/2.14	2.38	67/57.3	51.2/39.9 @ 6.5 dB OBO	43.7/43.9	9.3/8.9
(Mingming, Golestaneh, & Boumaiza, 2016)	Modified Π-network	GaN	2.15/3.4	1.58	41.5/43.4	52/51 @ 6 dB OBO	47.3/47	7.5-9.5/9-11
(W. Chen, Zhang, Liu, Liu, & Ghannouchi, 2014)	Frequency dependent input power division	GaN	0.85/2.33	2.74	47.5/45	45/41 @ 6 dB OBO	44/42.5	10/8
This work	**RCT + 3rd Harmonic Resonant Circuit**	**GaN**	**0.80/2.10**	**2.63**	**54/60**	**43/47 @ 6 dB OBO**	**39.5/40.5**	**10/10.2**

4.2 Summary

In this chapter, the results of the output impedance were presented and discussed. The simulation for forward transmission S21 and smith chart S11 was presented to determine the optimum output matching required for dual-band DPA.

Next, the complete DPA simulation and measurement results were carried out to test and validate the DPA performances. The individual results of 6 dB back-off drain efficiency, gain, and saturated power were shown and observed to determine the DPA's performance.

Furthermore, to verify the results between the simulation and measurement, the performance of the simulated and measured drain efficiency and gain performance of the prototype board at 6 dB back-off from saturation power are compared in a single graph. Moreover, comparing the simulated and measured output power of the prototype board was shown in another graph. The comparison between the simulated and measured results shows acceptable performances within the bandwidth interest of 0.8 GHz and 2.1 GHz. Lastly, the comparison of DPA performances with several works with the different method is presented.

CHAPTER 5: CONCLUSION

5.1 Conclusion

In this thesis, a dual-band DPA with GaN HEMT is designed for two-way radio application. The DPA design methodology is discussed from the theory to the development of the dual-band DPA with RCT and third harmonic tuning and further towards the measurement of the fabricated prototype. In the input matching network, the lossy matching circuit is applied concomitant with a stability network to provide dual-band input matching with minimum insertion loss and improve the DPA's overall performances at the frequency of 0.8 GHz and 2.1 GHz. Whereas at the output matching network, the reactance compensation circuit is applied and optimized together with the third harmonic tuning circuit to match two arbitrary points for two different frequencies of 0.8 GHz and 2.1 GHz when the devices are operated at 6 dB back-off.

For the measurement data, the proposed dual-band DPA with GaN HEMT presents a satisfactory achievement with a maximum output power of 40.5 dBm, 6 dB back-off efficiency of 43% and 47%, and gain of 10 dB approximately at 0.8 GHz and 2.1 GHz, respectively, and have a decent agreement with the simulated data. As compared to other methods, this work attains a much higher saturated efficiency of 60% at 2.1 GHz and retaining a good 54% saturated efficiency at 0.8GHz. Moreover, this work shows decent performances for efficiency at 6 dB back-off without sacrificing the saturated efficiency. Likewise, this work achieves the FR of 2.63, which is considered wide as for frequency spacing and is suitable for the condition in which broad frequency spacing is required. Hence, this thesis's proposed methodology is practical with enhanced performances at 6 dB back-off for the desired dual-band DPA configuration, which fulfills the objectives of this research work.

5.2 Future work

This research work has developed a dual-band DPA employing reactance compensation, third harmonic tuning, and lossy matching circuit implementation. This design's key point is to employ the methodology mentioned to obtain dual-band DPA with enhanced performances at a specific dual-frequency of interest.

The measurement results of the designed DPA are presented in Chapter 4. As we can observe that although the measurement performances of designed DPA are in good agreement with the simulation data, the results at the higher frequency end (after 2.1 GHz) showed degradation due to loss, limitation of equipment, and errors on the circuit construction. This design can be further improved by adding figure-of-merits such as 9 dB back-off region, linearity, and 1 dB compression point to investigate the DPA design in-depth. Additionally, the proposed DPA can further be improved by introducing a structure like a balun to enable the designer to fine-tune the center frequency for both bands independently by addressing the second harmonic of the first band to prevent it from overlapping with the second band's fundamental frequency. Moreover, this design can be extended to the high-frequency application (up to 20 GHz), such as millimeter-wave application, an essential application in future 5G communications.

Furthermore, the DPA can be further improved to incorporate the gate biasing and the input RF power with a dynamic control mechanism to implement it with the Artificial Intelligent (AI), especially the Deep Learning (DL) algorithm. The learning ability of DL would enable the performance of the DPA to adapt to the changes in the load and improves the efficiency at the desired back-off point and bandwidth of the DPA continuously.

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