## DEVELOPMENT OF SOLUTION PROCESSABLE VERTICAL ORGANIC LIGHT-EMITTING TRANSISTORS

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## DEVELOPMENT OF SOLUTION PROCESSABLE VERTICAL ORGANIC LIGHT-EMITTING TRANSISTORS

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## DEVELOPMENT OF SOLUTION PROCESSABLE VERTICAL ORGANIC LIGHT-EMITTING TRANSISTORS

## ABSTRACT

Display technology is shifting from liquid crystal display (LCD) to active matrix organic light emitting diode (AMOLED) due to many advantages of AMOLED such as better image quality, high viewing angle and flexible in design. However, the backplane thin-film transistor (TFT) issue have hindered the AMOLED to offer a competitive price compare to that of the LCD. Because of this, the vertical organic light emitting transistor (VOLET) was introduced, in which the combination function of charge modulation and light emission can solve the backplane issue. Unfortunately, the suggested solution only focuses on using sophisticated and expensive equipment which will not reduce the fabrication cost of the device. This PhD thesis addresses this issue by developing solution processable VOLET. This PhD thesis begins with understanding the fabrication processes and device characteristics of two type of devices; the static induction transistor (SIT) and Schottky barrier (SB) based VOLET. The simple solution process technology was used to fabricate the organic active layer, which also acts as an emissive layer. In the initial work, both devices show transistor behavior in which current density and luminance brightness were modulated by varying the gate voltage. It is also found that the principle mechanism of the two devices is different between each other. In order to gain more understanding of device physics of the VOLET, a thermally evaporated silver-sourced device has been fabricated as the control. The theoretical study involving Fowler-Nordheim (FN) tunneling and space charge limited current (SCLC) models are used to quantitatively analyze the experimental results and explain the device physics of the VOLET. In addition, a simple approach has been introduced to measure the mobility of the VOLET. The main research work focuses on utilizing a solution processable silver nanowires (AgNWs) as source electrode in the VOLET fabrication. The analysis on this novel device showed similar behavior as the silversourced device. More interestingly, the efficiency of the device is 10 times higher compared to that of thermally evaporated Ag-soured VOLET, which is due to high exciton formation and recombination. The study is continued with a demonstration of SIT based VOLET by using AgNWs gate. This could be the simplest technique to fabricate the VOLET. The use of AgNW as source and gate electrode has never been investigated prior to this study reported and this study has shown to some extent an improvement in the performance of the VOLET. Therefore, the research indicates that if a similar source and gate are used in VOLET with other high-efficient emissive materials, it could further enhance the performance of the device. Thus, this study provides a great insight and fundamental study for future development of low-cost display panel.

Keywords: VOLET; AgNW; electrical; luminescence; solution-processed technique.

## PEMBANGUNAN TRANSISTOR PEMANCAR CAHAYA ORGANIK MENEGAK YANG DIPROSES SECARA LARUTAN

## ABSTRAK

Teknologi paparan sedang beralih dari paparan kristal cecair (LCD) ke matriks aktif diod pemancar cahaya organik (AMOLED) kerana banyak kelebihan AMOLED seperti kualiti imej yang lebih baik, sudut paparan yang tinggi dan reka bentuk yang fleksibel. Bagaimanapun, isu transistor filem nipis (TFT) pada satah-belakang telah menghalang AMOLED untuk menawarkan harga yang kompetitif berbanding dengan LCD. Kerana ini, transistor pemancar cahaya organik menegak (VOLET) diperkenalkan, di mana gabungan fungsi modulasi cas dan pemancaran cahaya telah menyelesaikan masalah satah-belakang ini. Malangnya, penyelesaian yang dicadangkan hanya memberi tumpuan kepada penggunaan peralatan canggih dan mahal yang tidak akan mengurangkan kos fabrikasi peranti. Penyelidikan ini menangani masalah ini dengan membangunkan VOLET yang boleh diproses daripada larutan. Kerja penyelidikan ini bermula dengan memahami proses fabrikasi dan ciri-ciri dua jenis peranti; transistor induksi statik dan capasitor VOLET. Teknologi larutan proses yang mudah digunakan untuk membentuk lapisan aktif organik yang juga bertindak sebagai lapisan pemancar. Di peringkat awal kerja, kedua-dua peranti menunjukkan sifat transistor di mana ketumpatan arus dan kecerahan cahaya termodulasi dengan mempelbagaikan voltan get. Juga didapati bahawa mekanisme asas kedua-dua peranti adalah berbeza di antara satu sama lain. Untuk mendapatkan lebih banyak kefahaman tentang fizik peranti VOLET, peranti bersumber elektrod perak yang disejat secara termal telah dihasilkan sebagai peranti kawalan. Kajian teoretikal melibatkan model penerowong Fowler-Nordheim (FN) dan model cas ruang arus terhad (SCLC) telah digunakan untuk menilai secara kuantitatif data eksperimen dan menerangkan fizik peranti VOLET. Di samping itu, satu pendekatan mudah telah diperkenalkan untuk mengukur mobiliti VOLET. Kerja penyelidikan utama adalah tertumpu kepada penggunaan nanowayar perak (AgNWs)

yang boleh diproses secara larutan sebagai elektrod sumber dalam fabrikasi VOLET. Analisis pada peranti novel ini menunjukkan tingkah laku yang sama seperti peranti bersumber elektrod perak. Lebih menarik lagi, kecekapan peranti itu adalah 10 kali ganda lebih tinggi berbanding VOLET yang dihasilkan dari penyejatan terma, yang disebabkan oleh pembentukan dan penggabungan semula eksiton yang tinggi. Penyelidikan diteruskan dengan demonstrasi SIT VOLET yang menggunakan get berasaskan AgNW. Penggunaan AgNW sebagai elektrod sumber dan get tidak pernah dibuat kajian sebelum kerja ini dilaporkan dan penyelidikan ini menunjukkan beberapa peningkatan dalam prestasi VOLET. Disebabkan itu, penyelidikan ini menunjukkan bahawa jika sumber yang sama dengan bahan pemancar yang lain digunakan dalam VOLET ini, ia dapat meningkatkan lagi prestasi peranti. Oleh itu, kajian ini menyumbang pandangan yang mendalam serta menyediakan kajian asas untuk pembangunan panel paparan kos rendah di masa hadapan.

Kata kunci: VOLET; AgNW; elektrikal; pendarkilau; kaedah larutan proses.

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## LIST OF SYMBOLS AND ABBREVIATIONS

$\phi$	:	Barrier height
$\eta_c$	:	Current efficiency
$J_d$	:	Drain current density
<i>m</i> *	:	Effective mass of electron
F	:	Electric field
q	:	Elementary charge
т	:	Mobility
εο	:	Permittivity of free space
h	:	Plank constant
$\eta_p$	:	Power efficiency
d	:	Thin film thickness
AFM	:	Atomic force microscope
Ag	:	Silver
AgNWs	:	Silver nanowires
Al	:	Aluminum
Alq <sub>3</sub>	:	Tris(8-hydroxyquinolinato) aluminium
AMOLED	:	Active matrix organic light-emitting diode
DMF	:	Dimethylformamide
EL	:	Electroluminescence
FESEM	:	Field emission scanning electron microscope
FN	:	Fowler-Nordheim
HIL	:	Hole injection layer
НОМО	:	Highest occupied molecular orbital
ITO	:	Indium tin oxide

LCD	:	Liquid crystal display
LiF	:	Lithium Fluoride
LUMO	:	Lowest unoccupied molecular orbital
MEH-PPV	:	Poly[2-methoxy-5-(2-ethylhexyloxy)-1,4-phenylenevinylene]
OFETs	:	Organic field-effect transistors
OLEDs	:	Organic light-emitting diodes
OLEFETs	:	Organic light-emitting field effect transistors
PEDOT:PSS	:	Poly(3,4-ethylenedioxythiophene) polystyrene sulfonate
PL	:	Photoluminescence
PPV	:	Polyphenylene vinylene
PVDF-TrFE	:	Poly[(vinylidenefluoride-co-trifluoroethylene]
R <sub>s</sub>	:	Sheet resistance
SCLC	:	Space charge limited current
SEM	:	Scanning electron microscope
SIT	:	Static induction transistor
TFT	:	Thin-film transistor
UV-VIS	:	Ultraviolet-visible
V <sub>bi</sub>	:	Built-in voltage
V <sub>ds</sub>	:	Drain-source voltage
V <sub>gs</sub>	:	Gate-source voltage
VOLET	:	Vertical organic light emitting transistor
Vr	:	Resistance voltage
$V_{th}$	:	Threshold voltage

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University

#### **CHAPTER 1: INTRODUCTION**

## 1.1 Overview

Since a profound discovery on the first semiconductor-based on polymer (Shirakawa et al., 1977), many reports on the development of organic electronics has been published (Burroughes et al., 1990; Hagfeldt et al., 2010; Horowitz, 1998; Park et al., 2009; Roncali, 1992; Sirringhaus et al., 1998; Tyler et al., 2000). The commercial value of the organic-based electronic devices has been recognized in various applications such as display, transistors and solar cell technologies. The major factor of the tremendous development of these technologies is driven by new and advanced functionalized materials synthesized by the chemist. The great example of a commercialized product of the organic electronic devices is the ultra-thin organic light-emitting diode (OLED) TVs and flexible smartphones that already available in the market. It is expected that the organic electronic devices could offer much energy-efficient and "eco-friendly" as compared to that of existing electronic technologies, to achieve a sustainable environment world. Taking this as consideration, scientists around the world establish and continues research on advancing the synthesis and analysis of organic materials for more energy-efficient electronic displays and lights, solar cells, transistors, and other electronic devices.

In general, OLEDs are formed by single or multilayer organic electronic structure of either small molecules or polymers that sandwiched between two electrodes, which one of them is transparent to allow light emitted through it. As for the display application, OLEDs be able to generate an individual emission by their own, which offer more pure color and do not require any backlight, as found in liquid crystal display (LCD) technologies. Samsung is one of the pioneer electronic players that takes a huge step by commercializing the OLEDs display, staring with their Samsung Galaxy model. On top of that, Samsung and LG Electronics have both announced newly launched of largescreen OLED TVs (refer Figure 1.1). It is a positive move towards more pure colors and sharper contrasts, but also lighter, thinner, and more energy-efficient



Figure 1.1: Commercialized OLED TV by Samsung (top) and LG (bottom).

Transistors are the well-known basic electronic component that can amplify signals and switching voltages. There are several types of transistors, including metal-oxide field-effect transistors (MOSFETs), bipolar junction transistors (BJTs) and junction field-effect transistors (JFETs). Basic transistors are built from a semiconductor layer, and three junctions electrodes named a source, drain and gate. Most organic transistors are organic field-effect transistors (OFETs). There are several advantages of OFETs as compared to that of the silicon-based transistors, including the high flexibility in shape and low-temperature fabrication. Based on organic molecules used, OFETs also highly sensitive to certain wavelengths of visible light, chemicals and gases, making them promising candidates for optical, chemical and gas sensor applications. In 2000, chargecarrier mobilities of small-molecules based OFETs were less than one cm<sup>2</sup>/V.s (Facchetti et al., 2000; Katz et al., 2000). But after three years, the mobilities are increases above ten times (Diao et al., 2013), resulting from the new development and synthesis of the organic materials. Although the small molecules based OFETs were fabricated in ultrahigh vacuum chambers, it is suggested that high-performance OFETs can also be fabricated using simple and relatively inexpensive techniques, such as solution processing (Lee & Park, 2014).

Interest in organic electronics does not only arise due to their functionality, but also the versatility of device fabrication and application. Great example is the innovative idea of integration OLED and OFET technologies to produce organic light-emitting field effect transistors (OLEFETs) or OLETs. OLETs is a device that generate light luminescence from organic emissive layer in which the intensity can be modulated by the transistor current (Cicoira & Santato, 2007). The OLETs can be fabricated from ambipolar and unipolar materials, but the ambipolar type is more favorable for radiative recombination. Materials selection and modification of source and drain electrodes are some of the keys to achieve balance charge injection and transportation in both ambipolar and unipolar type devices. Development of architecture of OLETs has been improved from conventional planar type of OFET design into vertical type. Vertical geometry of OLETs, so called VOLETs, give more flexibility in fabrication technique, and narrow channel length, which leads to high performance and efficacy.

### **1.2** Research Problems and Opportunities

Most of the VOLETs were fabricated by using physical method such as thermal evaporation techniques. This technique was used to deposit either the organic layer, dielectric layer as well as the electrodes. On top of that, more complicated methods, which involves Langmuir-Blodgett, sputtering, vacuum filtering and transfer techniques have been utilized, especially for fabricating the source electrode with nano-porous structure (Liu et al., 2008; McCarthy et al., 2011; Yu et al., 2016). All these techniques required a vacuum environment and multiple steps procedure that lead to high fabrication cost and complex processes. Concerning on this particular fabrication issue, this study implement a simple solution processing technique, a spin-coating technique, which is notable as a low cost technique. This technique also known as a lab-based method to fabricate and design a simple organic electronic device. This study used solution based organic emissive materials which are small molecule and polymer. Furthermore, a solution based silver nanowire (AgNW) was fabricated as the porous source and gate electrodes by using the spin-coating technique. From the literature review, there are no work reported on a complete solution processing technique to form electrode, organic emissive layer and dielectric layer in one single VOLET device.

Device physics of VOLET is governed by injection, transportation, accumulation and recombination mechanisms of charge carrier. Currently, theoretical study is only established for the planar structure OLET, which directly adopted from the OFET parameters analysis. Parameters such as threshold voltage ( $V_{th}$ ), and transistor mobility of the OLET can be obtained from formula that manipulates the transfer characteristic of the device in which the saturation region of the output characteristic was taken into account. However, there is no saturation region in the output characteristics of VOLET, as it is impossible to obtain the  $V_{th}$  and transistor mobility by using the similar approach as for the OLET. In order to figure out this matter, a quantitative analysis has been

proposed which is fitted nicely with the experimental data. Moreover, the quantitative theoretical analysis also has been performed in order to understand the charge carrier injection mechanism that cause the transistor tuning behavior of the VOLET.

## **1.3** Research Objectives

The main objective of the thesis is to introduce a simple technique to fabricate OLET devices and evaluate their performance. It can only be achieved by gaining a deep understanding in the fundamental device physics. The findings could be used as a platform to simplify the production process of existing devices such that cheaper commercial product can be proposed. The main objective can be divided into three specific objectives:

- To investigate the fundamentals and performance of two different types of VOLETs which are static induction transistor (SIT) and Schottky barrier (SB) based devices that are fabricated by using a simple spin-coating method,
- To characterize and evaluate the device physics of control VOLET device which was fabricated using thermally evaporated source and dielectric layer,
- To fabricate and characterized the solution-processable AgNW-sourced VOLET device and compare its performances with that of control VOLET device,
- To demonstrate the AgNW-gated SIT based VOLET as the simplest VOLET device fabricated.

## **1.4** Scope and Limitation of the Research

The scope of the research is specifically focused on proposing and demonstrating a new design of VOLET and simplify the fabrication technique. The analysis of the device performance is fundamentally evaluated in order to fully understand the concept of the proposed design, which is not aiming for a high efficiency device. For that reason, the VOLET has not gone any evaluation test on the device stability and reliability.

Although the spin-coating technique is the simple method to VOLET device, it has a limitation in terms of controlling the alignment and orientation of the AgNW. This technique is also not the best method to perform a pattern, since the thin layer deposited is all over the surface. The length of the nanowire might not be 100% the same as some nanowire may be broken during the synthesis and fabrication. It is also important to highlight that the brightness and color of the light emission of the VOLET device is totally depended on the emissive materials used. It is understandable that a single emissive layer will not be able to yield a high brightness and efficiency. The selected emissive materials were only meant for evaluating the proposed concept and design of the VOLET device. The theoretical analysis applied is totally based on the existing organic semiconductor theory, with some modification to fit with the experimental results.

## 1.5 Organization of the Thesis

In Chapter 1, a brief overview of the organic electronics and their development from research to commercialize product is presented. The motivation keys that inspired this research work are described by pointing out the importance of green-technology, the transition from traditional LCD to OLED display technology, advantages of OLEDs, introduction of OLET as well as the market projection demand for this technology. It is followed by the objectives of this thesis where the introduction of simple processing technique in OLET fabrication becomes the main focus.

In Chapter 2, details on materials properties and device physics of organic semiconductor are explained. It begins with basic structure of conjugated polymer, the electroluminescence mechanism in OLED and transport properties in OFET are subsequently described. Then, literature reviews on OLET device is presented by comparing two types of OLETs; ambipolar and unipolar. The review is continued with explaining the VOLET development and fundamental issue need to be solved. Then, research idea is presented, followed by the overview of solution process technique, where several types of solution fabrication method are explained.

In Chapter 3, all materials used in this study are introduced and their properties are briefly explained. Then, the fabrication technique of spin-coating and thermal evaporation methods are explained in detail including their theories and working principles. Subsequently, the instruments used for sample characterization are introduced and their working principles are briefly explained.

In Chapter 4, two type of VOLET were introduced; a SIT and Schottky barrier (SB) based device. The fabrication of SIT-based VOLET with emissive small molecules and characterization of the device were demonstrated. Output characteristics of the device is explained in details. Then, another type of VOLET based on Schottky barrier (SB) is demonstrated. The important of source electrode in the VOLET design is discussed.

In Chapter 5, silver-sourced VOLET is fabricated and characterized as a control device. Device mechanism related to injection, transportation and electroluminescence are explained. Several theories are introduced to simulate the electrical properties of the devices in order to obtain the value of injection barrier and transistor mobility of the device.

In Chapter 6, optimization of AgNW as a source electrode in the VOLET is presented. The device fabrication process was explained followed by the device characterization techniques used in this thesis. The chapter ends by comparing the characterization and performance of the AgNW based VOLET with that of control VOLET as described in Chapter 6.

In Chapter 7, utilization of AgNW as gate electrode in the SIT is demonstrated. This chapter reveal the multiple function of AgNW in VOLET fabrication by empowering the unique characteristics of the AgNW, which are optically transparent, morphologically porous, and electrically conducting.

Finally, Chapter 8 summarized the overall research work done in this thesis and the suggestion of future works to improve the performance of VOLET device.

#### **CHAPTER 2: LITERATURE REVIEW**

## 2.1 Introduction

Organic semiconductors are essentially consisted of  $\pi$ -conjugated of small molecules and polymers. The properties of organic semiconductors such as charge carrier transport, electronic density of state, band gap and luminescence depend on their chemical structure which can be altered by chemical synthesis. Organic semiconductors are also scalable, printable, roll to roll processable, bendable, light in weight, and require low energy fabrication process. Therefore, significant cost and energy savings can be achieved, which makes organic semiconductors suitable for a variety of applications. This includes a light emitting diode for display and lighting, photovoltaic cell, field effect transistors, sensors, photodetectors and memory devices.

The significant impact of organic optoelectronics has been discovered by the realization of the first organic light emitting field effect transistors (OLEFETs) (Muccini, 2006; Zaumseil & Sirringhaus, 2007). OLEFETs or also known as OLETs are multifunction devices that combine the current modulating behavior of transistor with light emission. OLETs offer for the development of optoelectronic devices especially for display such as active matrix full-color display and highly sensitive touchscreen display. Moreover, their technology can be directed to solid-state lighting for commercialize and residential building. The architecture of an OLET adopts from that of an organic FET (OFET) as shown in Figure 2.1(a). It is noted that an OFET has three electrodes; source (S), drain (D) and gate (G) electrodes. The organic semiconductor layer is placed to be in contact with S and D electrodes whereas it is isolated from the G electrode by the dielectric layer. The area of the organic semiconductor layer confined by S and D electrodes represents the transistor channel. The geometry of this channel is described by the interelectrode distance (L) and the electrode width (W) of S and D as

shown in Figure 2.1(b). Under a significant drain-source bias, ( $V_{ds}$ ), holes and electrons are injected from S and D electrodes into the organic semiconductor layer within the transistor channel. It is essentially important to select S and D to have appropriate work functions to enable efficient electron injection in the lowest unoccupied molecular orbital (LUMO) and hole injection in the highest occupied molecular orbital (HOMO) of the organic semiconductor. At constant  $V_{ds}$ , the current flowing between the S and D electrodes ( $I_d$ ) is modulated by the gate bias. In principle, when emissive materials are utilized as the organic semiconductor layer in OFET, the charge carriers will form excitons and radiatively recombine to generate light in the transistor channel. Ideally, OLETs are ambipolar devices, in which both holes and electrons are injected and transported before recombining to produce the emission. However, OLETs has been reported also as unipolar devices, where just one type of charge carrier (electron or hole) is transported and the emission occurs close to the opposite electrode.



Figure 2.1: Basic architecture of an OLET at (a) cross-section and (b) 3-D view.

The characterization of OLETs includes the measurement of electroluminescence with responding to gate modulation. From here, the external quantum efficiency, current and power efficiency and color spectrum as well as its CIE coordinate, can be obtained. Similar to that of FET, the electrical characteristics allow to determine the transistor mobility and the ON/OFF ratio of the device by analyzing the output and transfer characteristic. For the planar architecture, it is possible to reveal the position of the recombination region in the transistor channel. On the other hand, the vertical design offers bigger size of emission area which eases to capture the luminance spectra. Instead of using direct current (DC) voltage, some groups reported on EL performance under alternating current (AC) bias as well (Liu et al., 2010).

In materials perspective, emissive organic semiconductor, electrodes and dielectric gate are the important aspects to determine the performance as well as fabrication technique of the OLETs. Numbers of small molecules and polymeric semiconductor has been utilized to fabricate OLETs by using thermal evaporation and solution processing techniques. Depending on the electronic density of state and optical properties, the light emission is mostly in the visible spectrum.

In this Literature Review chapter, current research in OLETs is reviewed in terms of types of device with respect to the materials employed, the device architecture, and direction towards vertical OLETs (VOLETs). This chapter is organized as follows; in Section 2.2, materials science of organic semiconductor and device physics of OLED and OFET were discussed; in Section 2.3, the detailed review of ambipolar and unipolar OLETs are presented; Section 2.4 reports the performance of various OLETs device structures; and finally Section 2.5 describes briefly the constructive plan on VOLETs research.

#### 2.2 Organic Semiconductor: Material Properties and Device Physics

#### 2.2.1 Conjugated Bond and Molecular Orbital.

Interaction among molecules for organic semiconductor is relatively weaker compared to that of the inorganic semiconductor. Most of the organic semiconductor compound contain conjugated bonding structure which is made of an alternation of single and double chemical bonds in the organic structure. These conjugated bonds structure can be seen in either polymeric or small molecule semiconductors. A polymer is an organic compound that consists of repeating monomer while small molecule doesn't have repeating monomer structure. Repeating the set of monomers in polymer makes them larger in size as compared to small molecule compound so that they are also known as macromolecules.

The molecular energy level of organic semiconductor compound is controlled by their conjugated structure (Almeida et al., 2002). For example, in benzene (see in Figure 2.2.), the carbon atom has trigonal Sp<sup>2</sup> hybrid orbital which forms  $\sigma$ -bond and  $\pi$ -bond. The  $\sigma$ -bond is created from strong single covalent bonded of C-C and C-H. The electrons that occupied the  $\sigma$ -bonds ( $\sigma$  electron) are strongly localized, which is not easily removed from its orbital and need high energy, e.g. thermal energy to remove it. On the other side, the  $\pi$ -bond is created from the overlapping of the 2pz orbital as a result of C=C covalent bonds. The electrons that occupied the  $\pi$ -bond ( $\pi$  electrons) are delocalized, which easily moves over the neighbor's atoms under external electric filed so that shows semiconductor property of the compound.

The  $\pi$  molecular orbital is splitted into two energy levels due to their electrons spin. Half of the molecular orbital is occupied by electrons which is so-called the highest occupied molecular orbital (HOMO) which refers to the distribution of energy band of weak tightly held electron in the molecule. Another half of the molecular orbital is unoccupied by electron (or occupied by hole) which is so-called unoccupied molecular orbital (LUMO) which represent the easiest route to the excitation of electrons from the lower levels. In an inorganic semiconductor, HOMO and LUMO are refer as valance band (VB) and conduction band (CB), respectively. The gap between these two energy levels represents the energy gap of the compound and strongly depends on the size and configuration of the conjugated structure.



Figure 2.2: Molecular structure of benzene and its orbitals system.

#### 2.2.2 Electroluminescence (EL) Mechanism in OLED

Electroluminescence in OLED is governed by four major physical processes which are carrier injection from an electrode, carrier transportation in the organic semiconductor, exciton formation and radiative recombination in emission center. Figure 2.3 shows the schematic diagram of basic electroluminescence mechanism in organic solid.

When sufficient bias is applied across the OLED, electrons and holes are injected from cathode and anode into the organic material and transported towards the opposite electrode. The injected carriers are transported by hopping process due to the disordered nature of the organic semiconductor. The number of the injected charge carrier influenced by injection barriers at metal-organic interface and potential different across the device. At sufficient voltage, the charge carrier be able overcome the injection barrier, which the current density, *J*, behave as the Shockley diode (Sah, 1991):

$$J = J \circ \left( \exp\left[\frac{qV}{nkT}\right] - 1 \right)$$
(2.1)

where  $J_0$  is the saturation current density, q is the elementary charge, V is the applied voltage, n is the ideality factor, k is the Boltzmann constant, and T is the temperature. There are two types of injection models, which are the Richardson-Schottky (RS) (Dekker, 1957) and Fowler-Nordheim (FN) model (Lenzlinger & Snow, 1969), respectively. For the RS model, the RS current density,  $J_{RS}$  can be simplified as:

$$J_{RS} = A^* T^2 \exp\left(-\frac{\Phi_B}{kT}\right),\tag{2.2}$$

where, A<sup>\*</sup> is the Richardson constant, A<sup>\*</sup> =  $4\pi qm^*k^2/h^3$  (=120 A/(cm<sup>2</sup>K<sup>2</sup>) for  $m^*=m_o$ ) and  $\Phi_B$  is the injection barrier in eV. Nonetheless, the FN model neglect Columbic effects, and so that the FN current density,  $J_{\text{FN}}$  is written as:

$$J_{FN} = \frac{A^* q^2 F^2}{\Phi_B \alpha^2 k^2} \exp\left(-\frac{2\alpha \Phi_B^{3/2}}{3qF}\right),\tag{2.3}$$

with 
$$\alpha = \frac{4\pi\sqrt{2m^*}}{h}$$
 (2.4)

The FN tunneling injection of carriers can also be described mathematically by Equation (2.5) and which is simplified to (2.6)
$$J_{FN} \propto F^2 \exp\left(\frac{-K}{F}\right)$$
, where  $K = \frac{8\pi (2m^*)^{1/2} \phi^{3/2}}{3qh}$  (2.5)

$$\ln(\frac{J_{FN}}{F^2}) \propto -K \cdot \frac{1}{F}$$
(2.6)

After injected through the metal/organic interface, the charge carriers are transported along the organic layer by hopping process. At low applied voltage, movement of the charge carrier demonstrate a linear increase of the current, which govern by the Ohmic drift current:

$$j_{ohmic} = n_{\circ} q \mu \frac{V}{d}, \qquad (2.7)$$

where q is the elementary charge,  $n_o$  is the charge carrier density,  $\mu$  is the charge mobility, V is the applied voltage and d is the device thickness. However, at higher applied voltage, the transportation of charge carrier is limited by low free-carries density and low carrier mobility of the organic semiconductor. At this stage, the current is referred as space-charge limited current (SCLC) (Donovan & Wilson, 1981). The SCLC can be described by Mott-Gurney equation (Lampert & Mark, 1970):

$$j_{SCLC} = \frac{9}{8} \varepsilon_{\circ} \mu \frac{V^2}{d^3}$$
(2.8)

where  $\varepsilon$  is the dielectric constant and  $\varepsilon_0$  is the permittivity constant. This relation is derived for a trap-free SCLC where diffusion and boundary condition at injecting contact are neglected. This then result to an infinitely high carrier density at the metalorganic contact. These carriers can be trapped in trapping level created from dopant impurities and disorder structural traps, which lead to low mobilities (10<sup>-3</sup> to 10<sup>-7</sup> cm<sup>2</sup>/V.s) (Stallinga & Gomes, 2006). At a higher bias, more carriers have been injected across metal-organic (MO) contact. When the density of charge carriers becomes high enough to form space charges, it creates an internal field that is against the direction of applied bias resisting further charged carrier injection. In the space charge region, the electrons are excited to LUMO level, leaving holes in HOMO level. These electronhole pairs are called exciton. The exciton is in meta-stable state and can lose its energy by electronic vibration. Then, the excited electrons from LUMO is recombined back to the holes in HOMO, releasing energy in a form of emission. This radiative recombination is normally referred as Langevin type recombination, which the exciton are captured faster the carrier mobility. The electroluminescence spectrum depends on the energy gap between HOMO and LUMO. After all, in the real case, the excitons is not always decaying radiatively, but can be loss as photonvibration.



**Figure 2.3:** Schematic diagram of electroluminescence mechanism in the organic device where 1) injection, 2) transportation, 3) recombination, and 4) emission process.

#### 2.2.3 Electrical Properties of OFET

As mentioned in Section 2.1, basic OFET is constructed to have (shown in Figure 2.4(a)): a thin organic semiconducting layer, an insulator/dielectric layer and a gate electrode, which stacked together end-to-end; source and drain electrodes, which are in

contact with the semiconducting layer to form transistor channel. In many cases, voltage is biased only to the drain and the gate electrode, and grounded at the source electrode. The voltage across between the gate and the source is defined as gate-source voltage  $(V_{gs})$ , while the voltage across between the drain and the source is ascribed as drain-source voltage  $(V_{ds})$ .

Figure 2.4 also illustrates the basic operating regimes of OFET, together with their respective current-voltage characteristics. When positive or negative bias is applied to the gate, electrons or holes are injected, respectively, from the source and accumulated at the insulator/semiconductor interface. The magnitude of accumulated charges is proportional to  $V_{gs}$  and the capacitance  $C_i$  of the insulator. Due to the deep traps in the organic semiconductor layer, minimum threshold voltage,  $V_{th}$  is required before the additional charges can be mobile. Thus, the effective gate voltage is  $V_{gs} - V_{th}$ .

For the case  $V_{ds}=0$  V, the accumulated charge carrier is uniformly distributed in the channel. With a small amount of  $V_{ds}$  ( $V_{ds}$ << $V_{gs}$ ), charge density increases linearly proportional to  $V_{ds}$  as the carrier injected from the source to flow through the. Further increased in  $V_{ds}$  until a point  $V_{ds} = V_{gs} - V_{th}$ , the channel experienced "pinched off" (Figure 2.4(c)). In this case, the depletion region is formed near to the drain as the potential difference between the local potential V(x) and the gate voltage is lower as compared to the threshold voltage. Only a small amount of saturation current  $I_{d,sat}$  allows to flow through this narrow depletion region as carriers. This current is travel from the pinch-off point to the drain by the comparatively high electric field in the depletion region is expanded and formed a shorter channel. At this region, the current saturated at a level  $I_{d,sat}$  because ideally, there is no potential different between the pinch-off point and the source electrode (Figure 2.4(d)).



**Figure 2.4:** (a) Schematic structure of an OFET and illustrations of operating condition at (b) linear condition, (c) start of saturation condition at pinch-off, (d) saturation condition and corresponding current-voltage characteristics.

## 2.2.4 Comparison Between OLEDs, OFETs and OLETs

In term of device functionality, OLEDs is designed to generate light emission by converting electrical energy, while the OFETs is device that can modulate current by varying gate voltage. Whereas the OLETs exhibit both characteristics of producing light and modulate current (and light) at the same time. In general, the OLEDs is constructed to have three basic layers; organic emissive layer that sandwiched between transparent anode and reflecting metal cathode. For the OFETs, there are three junctions known as source, drain and gate. The construction of these junction is totally depending on the type of OFET. In the case of basic metal-oxide field effects transistors (MOSFET), the source and drain electrodes are in parallel manner with several micrometers distance between each other, attached on organic semiconductor layer, followed by insulator or dielectric layer and gate electrode. In some cases, the OFETs is structured without dielectric layer, in which all three electrodes are in contact with organic semiconductor layer. This OFETs is categories as metal-semiconductor field effect transistors (MESFET). On the other hands, the OLETs is commonly follows the design of OFETs, except the organic semiconductor layer is emissive materials.

# 2.3 Type of OLETs: Ambipolar and Unipolar.

#### 2.3.1 Ambipolar OLETs

Polyphenylene vinylene (PPV) derivative has been used in the first ambipolar OLETs fabricated by solution process. Electroluminescent PPV derivative is commonly employed in LEDs, exhibit appropriate hole and electron transistor mobility if the dielectric gate is passivated by an organic dielectric. This organic dielectric limits electron trapping at the semiconductor-dielectric interface, and thus lead to an ambipolar transportation even though it is noted that the organic semiconductor is acting more as p-type. "Super Yellow" PPV based polymer OLETs have been fabricated with a very narrow channel length of 1 µm where the source and drain electrodes are made of gold (Au) and aluminum (Al), respectively (Swensen, Moses, & Heeger, 2005). Another polymer used is OC<sub>1</sub>C<sub>10</sub>-PPV where the device was designed such that the electrons and holes which were injected from separate calcium and gold electrodes, recombine radiatively within the channel, as shown in Figure 2.5. Interestingly, the recombination zone can be moved with the applied gate and source-drain bias to any position within the channel. This provides a direct visualization and proof of the coexistence of electron and hole accumulation layers, in an ambipolar transport regime (Zaumseil, Friend, & Sirringhaus, 2005). Beside PPV derivatives, polymer F8BT has also been employed with a top gate configuration, where a polymeric gate has been utilized. F8BT can conduct both holes and electrons efficiently in either bottom-contact or top-gate OLETs using gold electrodes, even though the injection barriers for both charge carriers is high. Transistor mobility of holes and electrons for this device were  $7.5 \times 10^{-4}$  cm<sup>2</sup>/V.s and  $8.5 \times 10^{-4}$  cm<sup>2</sup>/V.s, respectively.



**Figure 2.5:** Schematic and characteristics of ambipolar  $OC_1C_{10}$ -PPV transistors. (Zaumseil et al., 2005).

Despite high hole mobility and thus known as a hole-conducting organic semiconductor, Tetracene can be used to fabricate ambipolar OLETs by a submicrometer channel length with interdigitated coplanar hole-injecting Au and electron-injecting Ca contacts (Reynaert et al., 2005). The short-channel effects dominate the transistor behavior, while for longer channels, I<sub>ds</sub> is limited to the electron current injected from the Ca contact. Electrode modification has also been employed by

Yamane et al. (2007) where Al/LiF and Au have been used to inject electron and hole, respectively into pentacene/  $\alpha,\omega$ -bisbiphenyl-4-yl-terthiophene (BP3T) heterojunction semiconductor.

Sakanoue et al. have applied a wide-band-gap blue emission molecule of 4,-4'bis(styryl)biphenyl (BSBP) as an active layer in light-emitting organic field-effect transistors (Sakanoue et al., 2007). The used of an aluminum contact and a PMMA insulator allowed ambipolar operation for this device.

Bilayer heterojunction-based ambipolar OLETs of a,x-dihexylsexithiophene (DH6T) and N,N0-ditridecylperylene-3,4,9,10-tetracarboxylic diimide (P13) has been fabricated by using neutral cluster beam deposition technique (NCBD) (Seo et al., 2009). This device is air stable with hole and electron transistor mobilities of  $2.22 \times 10^2$  and  $2.78 \times$ 10<sup>2</sup> cm<sup>2</sup>/V.s, respectively. In fact, P13 also has been combined as heterojunction structure with tetracene to form the OLETs with top-contact, multi digitated, long channel width geometry that demonstrated good field-effect characteristics, stress-free operational stability, and electroluminescence under ambient conditions (Seo et al., 2010). More complicated structure of ambipolar OLETs has been reported with "p-i-n" design which consisted of a 30 nm thick film of a highly conductive p-doped layer as a hole transporter, then a 20 nm thick 4,4-bis-N-1-napthyl-N-phenyl-amino biphenyl (NPB) active layer doped with a 2 wt. % concentration of 5,6,11,12-tetraphenylnaphthacene (rubrene) and finally, a 30 nm thick highly conductive n-doped layer as an electron transporter (Maiorano et al., 2010). This p-i-n OLETs (see Figure 2.6) heterostructure has overcomed intrinsic problems of conventional OLETs, such as a limited emissive area at low output currents and relatively high output voltages. Single crystals of an ambipolar thiophene/phenylene co-oligomer has been synthesized as the active layer in OLETs (Katagiri et al., 2011). The compound AC5-1CF3-12OMe exhibits the ambipolar carrier transport on the FETs and light emission can be detected under AC bias on the gate electrode with EQE reported of 0.16% under square-wave on the gate bias.



**Figure 2.6:** Transfer characteristics of p-i-n OLETs, the inset shows a picture of the device operating in the light-emitting voltage range and the configuration of the device (Maiorano et al., 2010).

# 2.3.2 Unipolar OLETs

Ideally, the ambipolar materials are more acceptable for OLETs due to balance charge injection and accumulation in the active layer which increases probability of exciton formation and radiative recombination. However, light emission also has been detected in unipolar OFET devices such as the spin-coated polv[9.9di(ethylhexyl)fluorene] (PF2/6) when the gate voltage is increased (Ahles et al., 2004). The device shows unipolar characteristic when the calculated transistor mobility of PF2/6 is  $4.4 \times 10^{-4}$  cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> which is comparable to hole mobilities of  $3-4 \times 10^{-4}$  cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> as reported from time of flight experiments on polyfluorene (Redecker et al.,

1998). Further analysis has revealed that at a high gate voltage, the electrons have been injected from the drain electrode and the injected holes are accumulated at the gate oxide due to under etched electrodes during the lithography process.

Oyamada et al. have reported emission on another *p*-type polymer of tetraphenylpyrene (TPPy) (Oyamada et al., 2005) and 2,4-biss4-s28-thiopheneyldphenyldthiophenes (TPTPT) in FET devices (Oyamada, et al., 2005) as shown in Figure 2.7. They suggest an unusually high electrical field must be generated between the organic layer and the drain electrode, which will promote electron injection. The light was detected near to the drain electrode where the "pinch off" occurred. EL efficiency has been improved by an optimum short channel length.



**Figure 2.7:** (a) Molecular structure of TPTPT, (b) structure of organic light emitting field-effect transistor (OLEFET) (Oyamada et al., 2005).

# 2.4 Alternative Device Structures: Vertical Organic Light-Emitting Transistor (VOLET)

#### 2.4.1 Static Induction Transistors (SITs)

The vertical integration between a static induction transistor (SIT) and an OLED has been introduced in order to increase the emission area and lowering the operation voltage. SIT based OLETs does not require insulator or dielectric layer where the gate electrode is deposited inside the organic semiconductor with a grid design. Initially, a simple grid type Al gate electrode was employed in Alg<sub>3</sub>/ $\alpha$ -NPD based OLED (Kudo et al., 2003) before fabrication was later advanced by varying the grid width using different shadow evaporation technique (Kudo, 2005). The Al gate is used to modulate the hole transportation in  $\alpha$ -NPD hole transport layer before the hole was recombined with the electron at Alq<sub>3</sub> emissive center. The luminance of the device was detected with gate voltages as low as 1 V and the dynamic operation was obtained at 60 Hz. The low frequency operational is possibly due to the vertical type transistor where the distance between the source, drain and gate electrodes are very short (less than 100 nm) as compared to that of conventional OLETs design (above 1 µm). Others have reported that the hole also can be modulated in the transport layer of TPD by SIT design (Yang et al., 2009). Another attractive design of SIT-based OLETs is where the grid type gate was placed out of the overlapped region between the source and drain electrodes to efficiently prevent shielding electric fields (Park & Takezoe, 2004). The turn-on voltage and luminance were significantly improved by increasing the gate voltage. Similar model has been reported by Lu et al. (2010) with 5 layers of organic materials to ensure balance charge carrier injection and transportation in the device.

The SIT was invented by Watanabe & Nishizawa in 1950, which based on junction field effect transistor (JFET) concept but in vertical structure (28-6077, 1950). It controls current flow by modulating the internal potential of a single channel using a surrounding gate structure. In 1975 experimental SITs were fabricated, and the sourcedrain current of this device was shown to follow a diode model that consists ohmic and space-charge limited current (SCLC) characteristics (Nishizawa et al., 1975). There are three main structure of SIT devices; surface-gate, buried-gate and recessed-gate SIT (Napoli & Strollo, 2015). Figure 2.8 shows the cross section of the SIT devices. As compared to ordinary OFETs presented in previous Section 2.2.3, this SIT exhibit a short channel FET structure without dielectric or insulator layer. A current flowing vertically between source and drain is controlled by the potential energy barrier at the gate, and both the gate (grid) voltage and the drain (anode) voltage affect the source drain current (Patrick et al., 2018). The SITs also has been associated with the permeable- base transistor (PBT) which explained by bipolar junction transistor (BJT) model (Lüssem et al., 2015). However, the SIT is more preferred as short-channel JFET rather than BJT, as only one type of semiconductor layer (either n- or p-type) was used as compared to BJT that consists of either combination of NPN or PNP.



Figure 2.8: Cross section structure of 3 type of SIT devices (Napoli & Strollo, 2015).

#### 2.4.2 Schottky Barrier (SB) Transistors

Instead of SIT, the vertical coupling between a capacitive cell and OLED cell has also been proposed, which is also known as Schottky barrier (SB) VOLETs (refer Figure 2.9). Both cells were connected to a common source which acts as a source electrode where a dielectric layer was deposited between the source and gate electrodes and the organic emissive layer was deposited between the source and drain electrodes. Current flow between source and drain is modulated by height of Schottky barrier at source/emissive layer interface when gate voltage is varied.



Figure 2.9: Structure of SB-VOLETs.

This idea was adopted from vertical OFET reported by (Ma & Yang, 2004). The deposited Al source electrode was very thin and rough to increase the possibility of partial oxidization, where a certain amount of negative charge can be generated. The same group has also fabricated the first OLETs device that used the same model with some modification. They have deposited OLED cell prior to depositing the capacitive cell (Xu et al., 2007). The dielectric material used is LiF and the transistor produces a near 0.4 mA output current and a 10<sup>2</sup> on/off ratio (the ratio of the source-drain current I<sub>SD</sub> with and without gate bias). The same approach has been used for MEH-PPV orange

emissive polymer by (Reshak et al., 2013), however, the luminescence response to the gate voltage is not discussed in details.

A remarkable VOLETs design has been invented and reported by Liu et al. where a single-walled carbon nanotube (SWCNT) transparent electrode has been employed (Liu et al., 2008). The SWCNT networks were formed on nanoporous mixed cellulose ester membranes before they were transferred onto aluminum-titanium oxide (AZO) dielectric layer to form a porous source electrode. The porous feature of SWCNT has allowed energy level contact between the organic active layer and the gate electrode, which plays an important role to accumulation of charge. Subsequently poly[(9,9dioctyl-fluorenyl-2,7-diyl)-alt-co-(9-hexyl-3,6-carbazole)] (PF-9HK) as hole-injecting layer, N,N'-di(1-naphthyl)-N,N'-diphenyl-1,1'-diphenyl-1,4'-diamine) NPD as the hole transport layer, tris(8-hydroxyquinoline) aluminum (Alq<sub>3</sub>) as the photoactive layer and Al/LiF drain electrode were deposited on top of the SWCNT networks by a thermal evaporation technique. This vertical architecture enables the use of low mobility semiconductor in OFETs and thereby widening the range of potential active materials that can be chosen. There is also a possibility to increase the device lifetime. Operating at a considerably low-voltage and low-power make this VOLETs a favorable candidate for active matrix displays (McCarthy et al., 2011). Recently, a new VOFET which integrate a VOFET and OLED has been reported (Yu et al., 2016). This work established the self-assembly of Langmuir-Blodgett nanospheres as a shadow mask to produce a close-packed nanopore array on top of an ITO film. The ITO was then undergoing lithography process to form a porous ITO and used as the source electrode in such VOLET. Table 2.1 list the summary of the progress in VOLET development as described in this section.



**Table 2.1:** Progress in VOLET development.



Table 2.1, continued.

# 2.5 Fundamental Issue: Fabrication Process of Source Electrode

Several techniques have been used to fabricate VOLETs. In particular, the main focus was given to the fabrication of the source electrode. This is because the source electrode requires a special features which are morphologically porous and electrically conductive. The source electrode has been fabricated by using a combination of vacuum filtering and transferring of the CNT network (Liu et al., 2008; McCarthy et al., 2011). The vacuum filtering setup is illustrated in Figure 2.10. The fabrication process involve

five major steps: (i) vacuum-filtering a dilute, surfactant-based suspension of purified nanotubes onto a filtration membrane; (ii) washing away the surfactant with purified water; (iii) cutting into the desired shape and size with a razor blade; (iv) dissolving the filtration membrane in solvent; and (v) transferring onto the top of the dielectric layer. This process was first introduced by (Wu et al., 2004).



Figure 2.10: Vacuum filtering setup for CNT film fabrication.

Recently, a porous ITO based source electrode have been fabricated by colloidal lithography where polystyrene spheres (PS) were deposited by Langmuir-Blodgett (LB) to form a monolayer (Yu et al., 2018). The fabrication steps is illustrated in Figure 2.11. A monolayer of the PS was initially form by LB technique. The size of close-packed polystyrene particle was controlled by a reactive ion etching. A 90 nm-thick ITO film was deposited by RF sputtering, before the PS was lift-off by a 3 M scotch tape, leaving the ITO with pore center to center distance of around  $1.1 \,\mu m$ .



Figure 2.11: Schematic diagram of fabrication steps of ITO porous electrode.

Those above mentioned methods have disadvantages. The CNT filtered technique is indirect deposition method, which involve transferring process. On the other hand, the ITO porous electrode involve very complex routine, expensive and sophisticated equipment, and not suitable for large-scale production. In order to simplify the fabrication of the source electrode, a new idea of utilizing silver nanowires (AgNWs) as the source electrode for VOLETs is introduced in this work. The AgNWs can be fabricated easily by simple solution process such as spin-coating method, and can be formed directly to the device without transferring process.

# 2.6 Research Idea: Solution Processable Silver Nanowires as Source Electrode

The new generation of VOLET structure consists of the combination of capacitor cell and OLED cell. The capacitor cell is used to modulate current of OLED cell by varying gate voltage. These cells combination were interconnected with the source electrode, or known as an intermediate electrode. The source of VOLET must fulfill two requirements before it can be employed as electrode, which includes:

- i. electrically conductive to allow current flow on it;
- ii. morphologically porous to allow energy band diagram alignment between the organic semiconductor layer and the gate electrode for current modulation

From literature, the development of source electrode of VOLET has evolved from the high roughness of metal electrode (Xu et al., 2007), to the used of carbon nanotube (Liu et al., 2008) and nanolithography of porous ITO (Yu et al., 2016). Among the three methods suggested, only the method that used carbon nanotube is using solution processing technique in the preparation process. However, the preparation process involves many steps which include vacuum filtration and transferring processes of the carbon nanotube network. The most complex process is the nanolithography of the ITO, which involves depositing and resizing the nanosphere by Langmuir-Blodgett (LB) technique and etching technique, deposition of ITO by e-beam technique and finally the lithography process. Thus, a new way of fabrication technique and a new type of material for the source electrode need to be studied in order to simplify the overall process of VOLET fabrication.

A silver nanowire (AgNW) was widely studied due to their fascinating electrical, thermal, and optical properties (Sun, 2010). Silver exhibit the highest electrical conductivity of  $6.3 \times 10^7$  Sm<sup>-1</sup> as compared to all metals, by merit of which AgNWs are considered as a favorable candidates in electronic devices. Lee et al. (2008) have first demonstrated that the solution processable AgNW can be used as a transparent electrode

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in solar cell with comparable performance to that of sputtered ITO electrode. Polyol synthesis method was utilized to produce high yield uniform AgNWs with a very low electrical resistivity of 0.091  $\Omega$ /sq (Zhang et al., 2011). However, the films suffer a low transparency of 14.2%, which shows great promise in the improvement of a conductive antireflection coating. A self-assemble AgNWs can be deposited on a bubble template to form a low sheet resistance of 6.2  $\Omega$ /sq with a transparency of 84% after heat treatment at 200 °C for 20 min (Tokuno et al., 2012). A foldable transparent electrode based on AgNWs and AgNPs was developed by using an all-solution-process roll-toroll ink-jet printing and spray coating technique for OLED application (Triambulo et al., 2014). Figure 2.12 shows the schematic diagram of AgNWs processing by the roll-toroll technique with the flexible OLED structure. The flexible AgNWs exhibit sheet resistance of 2.5  $\Omega$ /sq with high transparency around 90-95%.

Improvement on AgNWs conductivity was reported by incorporating a graphene sheet in which the sheet resistance reduced down the resistivity to  $6.05 \times 10^{-4} \Omega \text{cm}^{-1}$  (Liu et al., 2014). The graphene sheets embedded within the AgNW network fill the porous and enhance the junction contact between the AgNWs, resulting in a uniform electrical conductive network while the AgNW network can prevent the re-stacking of graphene sheets. Combination of mechanical pressing and annealing technique was discovered effectively reduce the sheet resistance of AgNW transparent electrodes (Jiang et al., 2015; Tokuno et al., 2011). Depending on the pressing load and annealing temperature, the sheet resistance and the transparency of the AgNW electrode can be 8.6 to 10  $\Omega$ /sq and 80 and 90%, respectively. A hybrid AgNW-polymer was also introduced as the transparent electrode which significantly reduces the surface roughness of the AgNW down to 1.27 nm (Zeng et al., 2010) and very suitable for flexible electronic application such as shape-memory polymer LED (Yu et al., 2011). PEDOT:PSS-AgNW

hybrid electrode with 7.7  $\Omega$ /sq of sheet resistance was fabricated in inverted OSC (Kim et al., 2015).



**Figure 2.12:** Schematic descriptions of (a) all-solution-based hybrid film roll-to-roll coating processes and the films fabricated at each processing step and (b) f-OLED structures on the AgNWs and hybrid films (Triambulo et al., 2014).

## 2.7 Overview of Solution Process Techniques

Solution process technique is a method that uses precursors from a liquid phase to form a sample, e.g. thin films. The precursors can be either organic material such as polymer and small molecule, or inorganic nanostructured materials including metallic nanoparticles, nanowires and quantum dot. The organic based materials, such as polymer are usually dissolved easily in organic solvent system depending on polarity of the materials and the solvents. On the other hands, the inorganic materials are dispersed in solvent to prevent agglomeration between their individual nanostructures. The fabricated sample can be in various form i.e. a thin film (Filho et al., 2018), distribution of nanoparticles (Ito et al., 2012), layers of nanowires networks (Lee et al., 2018) and stack of nanosheets (Alshrah et al., 2018). Following are the example of solution processing techniques including spin-coating, screen printing, inkjet printing and gravure printing.

# 2.7.1 Spin-Coating

The simplest solution technique is a spin-coating method. Spin-coating technique uses a centrifugal force at very high speed of rotation to spread the solution (mix of solvent and precursor) on the surface of a substrate (Emslie et al., 1958). The formation of the final product i.e. thin film is not only depended on the nature of the solution in term of viscosity, solid concentration, boiling point of solvent used and surface tension, but also spin speed, acceleration and duration time parameters. This is a well-established initial laboratory method to form sample from solution prior transferred into a large scale production (Filho et al., 2018).

# 2.7.2 Screen-Printing

Another solution method to produce thin film is screen printing. This is a stencil process in which solution is forced through a screen by resilient squeegee. The stencil on the screen defines the actual design of thin film. The process of screen printing is shown in Figure 2.13. The prepared solution (also refer as ink) is initially applied to the screen and flooded on the screen surface. The squeegee is pressed, allowing the ink through the mesh at the screen and touch the substrate. After the mesh is lifted, the ink left on the substrate is solidified to become a thin film.



Figure 2.13: Screen printing process.

Metal meshes are usually employed due to their chemical stability against solvents and better precision than synthetic meshes. The quality of the printed thin film depends on the mesh opening, fiber diameter and geometry. Since the overall thickness of the mesh is relatively in micrometer thick, this technique is possible to reach higher layer thicknesses than with any other printing method. On top of that, this technique requires high viscous ink with a viscosity above 500 mPa.s, depending on the size of the mesh opening. With 70  $\mu$ m of the mesh size, 20 to 100  $\mu$ m thick of film can be produced from 500 to 5000 mPa.s viscosity of the ink. A significant work done by (Liang et al., 2016) by utilizing the screen printing technique to produce a water-based silver-nanowires (AgNW) as stretchable electrode in the wearable transistors.

## 2.7.3 Inkjet-Printing

Compared to the screen printing method, an inkjet printing is a noncontact method, which the thin film shape follows the design set by computer. The thin film was produced on the substrate by generating drops of the solution. The inkjet printing technology can be divided into two; continuous inkjet (CIJ) and Drop on Demand (DOD) inkjet systems. However, CIJ technology suffer a low print resolution due to production of large diameter droplets. On the other hands, the DOD offer a fine ink droplet which makes resolution increased significantly. Figure 2.14 illustrates basic process of DOD piezo inkjet print head. The ink is filled into a cartridge and flowed to the printer head. The ink is then injected from the printer head via a nozzle onto a substrate surface. In this stage, volume of injected droplet is controlled by a piezoelectric actuator, while the size of the droplet depends on the nozzle aperture. The printed ink is dried to form a thin film on the substrate.

Recently, performance of inkjet-printed conducting polymer of PEDOT:PSS on paper has been reported (Morais et al., 2018). This is a basic study towards an application of the electronic paper in the future. This method also used to produce PVDF-TrFE based device for energy harvester, sensor and actuator applications (Thuau et al., 2017).



Figure 2.14: Inkjet printing process with piezoelectric actuator print head.

# 2.7.4 Gravure-Printing

Among the solution process techniques, the gravure printing is known as the most economic for the mass production in large area system. Figure 2.15 presents a printing process by the gravure technique. The system is consisted of two stainless steel cylinders; impression cylinder and gravure cylinder. The design was patterned on surface of the gravure cylinder known as the cell. The substrate is placed and moved in between these cylinders. The ink is filled in the pan and the gravure cylinder is immersed in the ink. As the gravure cylinder rotates, the ink covered on the cylinder surface and the nonprinting areas is removed by a doctor blade. The ink that evenly filled the cell is then transferred onto the substrate while the impression cylinder pressing the substrate towards the cell. The printed pattern is dried to form the thin film.



Figure 2.15: Process of gravure printing technique

This technique is able to yield of approximately 75% functional OFETs over 50000 unit of fabricated transistors (Hambsch et al., 2010). A high performance flexible polymer light-emitting diodes (PLEDs) have been fabricated by this method with maximum luminosity of 8.8 lmW<sup>-1</sup>, which is comparable with conventionally fabricated device (Chung et al., 2010).

## 2.7.5 Advantage of Solution Processing Method

Unlike other conventional physical deposition methods such as thermal evaporation, sputtering and chemical vapor deposition, the solution processing technique requires no vacuum system and can be performed in room or low temperature environment. This makes them less complex, time saving, and cost effective especially for the mass production. By optimizing the method of synthesis and usage materials, this method can be a green and an environmentally friendly technology. Solution process also enable the layer to form on any type of substrate including paper, plastic, glass, fabric or metal. The limitless of type of substrate allows versatility in design and expand functionally of application such as in wearable electronics.

#### 2.8 Summary

Properties of organic semiconductor materials depends much on their electronic structure. Electroluminescence mechanism in OLED involves charged carrier injection, and transportation, exciton recombination, and light emission processes. The electrical properties of the OFET are controlled by depletion formation due to the gate voltage modulation. The OLET is basically the OFET device with an ability to produce a light, which has both OFET and OLED functions in one device. Depending on the organic semiconductor and electrode used, the OLET can be classified as ambipolar and unipolar. The light emission of ambipolar OLET occurred at the center of the transistor channel, however, for the unipolar OLET, the emission observed is near the electrode of the channel. The VOFET offers the solution of the high channel length and small light emission area of the planar OLET. The VOLET with a combination of the capacitor and OLED cells are believed to be the best VOLET so far. The source electrode that connected both the capacitor and OLED cells must possess a high electrical conductivity and reasonable morphological porosity. The AgNW is elected as the suitable candidate to be the source electrode, which not only fulfills the expected criteria but also offers cheaper and easier fabrication technique. The overview of solution processing techniques has been described. It is anticipated that the solution processing method has various advantages on cost, equipment, procedure and selection of substrates.

#### **CHAPTER 3: METHODOLOGY**

#### 3.1 Introduction

This chapter focuses on the experimental methods and procedures for solution and substrate preparation, thin films deposition and devices fabrication. Chapter 3 begins with brief introduction of materials used in this thesis. The sample preparation is then described, which involves the explanation on solution and substrate preparation, spin-coating and thermal evaporation techniques, and details in device fabrication procedure. Subsequently, the characterization method used for the prepared thin films and devices are presented. The thin films are characterized for thickness, optical, photoluminescence (PL), and morphological properties. The VOLET devices, are characterized for current-voltage-luminance (J-V-L) and electroluminescence behavior.

It is important to highlight that there are five types of VOLETs device fabricated in this thesis. These devices were categorized into 2 major groups; thermally evaporated source or gate electrode (TESG) and solution processable source or gate electrode (SPSG). In the TESG, threes device were fabricated, which are Tris(8hydroxyquinolinato) aluminium (Alq<sub>3</sub>) based static induction transistor (SIT) VOLET with aluminium, Poly[2-methoxy-5-(2-ethylhexyloxy)-1,4-phenylenevinylene] (MEH-PPV) based VOLET with aluminium and silver source electrode. On the other hand, in the SPSG group, MEH-PPV based VOLET and SIT-VOLET were fabricated with silver nanowires (AgNW) source and gate electrode, respectively. Devices fabrications involve two major deposition techniques; spin-coating and thermal evaporation methods, which will be explained in this Chapter. Details on fabrication process of each devices are explained in Chapter 4, 5, 6 and 7. All devices were characterized to investigate their electrical and luminance properties. Besides the device, material preparations and characterizations were also performed in order to justify the analysis of the device performances. These includes fabrication of AgNW on glass substrate by spin-coating technique. The samples were then characterized to study their optical, structural and electrical properties. Figure 3.1 shows schematic diagram of research flow chart for this work.



Figure 3.1: Schematic diagram of research flow chart in this work.

# 3.2 Materials

There are several types of materials used in this thesis, depending on their function especially for each layers of VOLET devices. The materials can be under the category of transparent conducting electrode, organic conducting polymer, organic semiconducting, ferroelectric polymer, conducting nanowires, dielectric, and conducting metal electrode. Table 3.1 shows the materials used in this study together with their details of functions in the VOLET system.

Category	Name of material	Function in VOLET
		system
Transparent	Pre-patterned indium tin	• Anode electrode in
conducting electrode	oxide (ITO)	static induce
		transistor organic
		light-emitting
		device (SIT-OLED)
		• Drain electrode in
		VOLETs
Organic conducting	Poly(3,4-	• Hole injection layer
polymer	ethylenedioxythiophene)	(HIL) for anode and
	polystyrene sulfonate	drain electrode
	(PEDOT:PSS)	
Organic emissive	Tris(8-hydroxyquinolinato)	Emissive layer to
	aluminium (Alq <sub>3</sub> )	produce green light
	Poly[2-methoxy-5-(2-	• Emissive layer to
	ethylhexyloxy)-1,4-	produce orange
	phenylenevinylene] (MEH-	light
	PPV)	
Conducting	Silver nanowires (AgNWs)	• Source electrode in
nanowires		the new VOLETs
Ferroelectric polymer	Poly[(vinylidenefluoride-	• Dielectric layer in
	co-trifluoroethylene]	new VOLETs
	(PVDF-TrFE)	
Dielectric	Lithium Fluoride (LiF)	• Dielectric layer in
		controlled VOLETs
Conducting metal	Aluminum (Al) and Silver	• Source electrode in
electrode	(Ag)	the controlled
		VOLETs
		• Gate electrode in
		the VOLET

Table 3.1: List of materials used in this thesis and their functions in VOLETs system.

**Pre-patterned ITO** used in this study was purchased from Ossila Ltd. The ITO is consisted of a 1.1 mm thick of a polished soda lime float glass with 100 nm thick of fully oxidized ITO deposited by electron-beam technique. The sheet resistance for the ITO is 20  $\Omega$ /sq with roughness of less than 1 nm RMS measured by AFM.

**PEDOT:PSS** used in this study was purchased from Heraeus Clevios. The PEDOT:PSS is a composition of 0.5 and 0.8 wt. % of PEDOT and PSS dispersed in water with 1.3 wt. % of concentration. The conductivity of the PEDOT:PSS is 1 S/cm and possess high transparency within the visible light spectrum and even into near infrared and near UV regions, with no absorption maximum from 400-800 nm.

Alq<sub>3</sub> used in this study was purchased from Sigma Aldrich. The Alq<sub>3</sub> is a small molecule with 99.9995% trace metal basis and 0.5 wt. % loss on heating with a typical glass transition temperature of 175 °C (Mayr & Brütting, 2015). The melting point of this material is between 300 to 411 °C. The material can absorb high UV light of 259 nm and emit a green light at 519 nm and usually used as a control device for many OLED study (Mohd Sarjidan et al., 2013; Za'Aba et al., 2013).

**MEH-PPV** used in this study was purchased from Sigma Aldrich. The average molecular weight of the MEH-PPV are between 70,000 and 100,000. The excitation and emission of the polymer are at 495 and 554 nm, respectively in toluene. This orange emissive polymer is also widely used as a control in OLED study (Rahman et al., 2013; Sarjidan et al., 2010).

AgNWs used is this study was purchased from Novarials Corp. The average diameter and length of the AgNWs are about 20 nm and 20  $\mu$ m, respectively. The AgNWs was dispered in isopropanol solvent with concentration of 5 mg/ml. Many research work has used this AgNWs from Novarials, which indicates the reliability of

the materials (Deignan & Goldthorpe, 2017; Dong & Goldthorpe, 2018; Kim & Park, 2018; Mohd Halizan et al., 2017).

**PVDF-TrFE** used in this study was purchased from Kureha. This material is wellknown to exhibit ferroelectric behavior and also can be used as a dielectric layer in the transistor (Lu et al., 2016; Thuau et al., 2016).

**LiF** used in this study was purchased from Sigma Aldrich. The LiF is in a powder form with a melting point of 845 °C and it is used as a dielectric layer in OFET devices (Kumar & Dhar, 2016; Luo et al., 2015).

Al and Ag used in this study were purchased from Sigma Aldrich. They are graded as 99.999% metal in a form of 1 mm diameter of wire. The melting point of the Al and Ag are 660 and 960 °C, respectively with boiling point temperatures of 2460 and 2212 °C, respectively.

The molecular structures of organic materials used were presented in Figure 3.2. All these materials are soluble in solvent for solution processing technique.



Figure 3.2: Molecular structure of organic based materials used in this study.

# **3.3** Solution Preparation

The materials presented in Figure 3.1 are solution processable. Some of them are purchased in solution form and some are diluted or dissolved in solution prior before used. As previously mention, PEDOT:PSS was purchased in aqueous form with concentration of 1.3 wt. % dispersion in water and AgNW was purchased as dispersion with concentration of 5 mg/mL in isopropanol. Thus, in this work, the Alq<sub>3</sub>, MEH-PPV and PVDF-TrFE materials were prepared using solution processing technique only.

Alq<sub>3</sub> was diluted in chloroform with concentration of 15 mg/ml, and stirred in room temperature for at least 1 hour to ensure full dissolution of Alq<sub>3</sub> powder. The MEH-PPV was diluted in toluene with concentration of 4 mg/ml and the stirring process was performed inside a glove-box for at least 48 hours, before it can be used. The PVDF- TrFE was diluted in methyl ethyl ketone solvent with concentration of 40 mg/ml and stirred at 90 °C on a hot plate for at least 24 hours.

# 3.4 Substrate Preparation

Glass and the pre-patterned ITO were used as substrate for the thin films and the VOLET devices, respectively. Both substrates undergone a cleaning process to avoid contamination that can affect the experimental results. The glass substrates were initially prepared by cutting a microscope glass slide into a size of 1.5 cm  $\times$  2.0 cm, which is similar as the size of the pre-patterned ITO. The pre-patterned ITO substrate was purchased from Ossila Ltd., came in with a set of a pair of connector legs and an encapsulation glass slide (see Figure 3.3(a)). The pattern design of the ITO is shown in Figure 3.3 (b). This is the standard ITO design from Ossila, specially made for fabrication organic light-emitting diodes (OLEDs) and organic photovoltaics (OPVs).



Figure 3.3: (a) A complete set and (b) specific design and dimension of the prepatterned ITO substrate.

The glass and ITO substrates were cleaned through the cleaning procedure in the following order:

- The substrates were put in a beaker containing Decon<sup>TM</sup> diluted in water with ratio 1:10. The whole beaker is immersed into an ultrasonic bath for 15 minutes to remove dust and small particle contamination,
- The substrates were then rinsed with distilled water to remove soap water from their surfaces,
- 3) The substrates were rinsed with acetone to remove non-polar type contamination,
- The substrates were quickly rinsed with isopropanol in order to remove polar type contamination,
- 5) The substrates were rinsed with deionized water to remove ethanol solvent,
- 6) The cleaned substrates were purged with nitrogen gas for drying proposes,
- The substrates were kept in an oven at 60 °C overnight to ensure no water or moisture left.

#### 3.5 Thin Film and Device Fabrication

#### 3.5.1 Spin-Coating Technique

The thin film layers which based on solution such as hole injection polymer, organic semiconducting, AgNWs and ferroelectric polymer in this study were prepared by using a spin-coating technique. Two spin-coaters were used in this study. One of the spin-coater was placed inside a 10k cleanroom and the other one was placed inside a glovebox. Figure 3.3 shows the spin-coaters. The one which was placed inside the cleanroom (Figure 3.4(a)) is meant to spin-coat water based PEDOT:PSS and the other one inside the glovebox (Figure 3.4(b)) was used to spin-coat the solution based materials.



Figure 3.4: Spin-coater used in this study which placed (a) outside and (b) inside the glove-box.

Spin-coating is a simple process to deposit thin film from solution form. The deposition procedure is illustrated in Figure 3.5. The cleaned substrate was placed on top of the coater platform. The substrate was vacuumed in order to ensure it sticked well on the platform during the spinning process. A small volume of solution was taken using a micro-syringe and dispensed on top of the substrate. The spinning process is
then executed according to the spin parameter including spin speed, time and acceleration. During the rotation of the substrate, the solution experienced a centrifugal force which allowed it to spread on the substrate. The solvent of the solution was evaporated and leaving a film as the final product. The produced film also undergo a soft-bake process where the substrate was baked on a hot-plate at a temperature around the boiling point of the solvent used for a short period of time, e.g. 15 minutes, in order to enhance the solvent evaporation rate and also to ensure there was no solvent left in the film.



Figure 3.5: Spin-coating process.

# 3.5.2 Thermal Evaporation Technique

The fabrication of the device also involves another process called thermal evaporation technique. This technique was used to deposit Al and Ag metals, and LiF dielectric layers. There are two thermal evaporator systems used in this study. The first system is Edward Auto 306 system which is located in the cleanroom environment as shown in Figure 3.6(a). This system has a capability to vacuum down the evaporation

chamber until the pressure of 10<sup>-5</sup> mbar using a diffusion vacuum pump. The filament coil is used as the heating medium for this machine since the power supply can only produce a low current with a maximum value of 25 A. The other evaporation system is placed in a glove-box system as shown in Figure 3.6(b). This system is equipped with a turbo molecular vacuum pump system, which can easily achieved 10<sup>-7</sup> mbar of chamber pressure within 2 hours. This system is connected with a high current power supply, and thus a tungsten boat can be used as the heating medium.



Figure 3.6: Thermal evaporation system.

The schematic diagram of a thermal evaporator system is illustrated in Figure 3.7(a). The sample was placed on the patterned mask as shown in Figure 3.7(b). The sample was positioned to face-down so that the evaporated materials can be deposited on it. The mask was placed on the sample holder inside the evaporation chamber. The heating medium was connected to the heating electrodes and the selected materials were then

placed in the heating medium (tungsten boat). The chamber were closed and vacuumed until the desired low pressure was achieved. After the high vacuum had been achieved, the current was slowly increased using the transformer power supply. The current that passed through the electrodes was heating up the tungsten boat as well as the materials inside it. At the high temperature equivalent to the evaporation temperature of the materials, the materials would be evaporated. The shuttle was opened and the thickness monitor started to take the thickness reading. Until the chosen thickness of the materials was deposited, the shuttle was closed and the current was slowly reduced.



Figure 3.7: (a) thermal evaporator system and (b) mask for electrode deposition.

### 3.5.3 Encapsulation Process

The device fabrication was completed by encapsulation process. The UV-cured epoxy was dropped on the deposited device, followed by covering with a piece of glass. The device was then placed inside the UV-box system and exposed with UV light for 15 minutes.

Figure 3.8 illustrates the detail fabrication process for one of the device. The solution processed layers were patterned by a simple wipe technique with cotton bud containing

suitable solvent that can etch the layers. This diagram also shows how the device fabrication was divided into VOLET fabrication with metal evaporated source and solution process AgNW source.



Figure 3.8: Fabrication process for the MEH-PPV based VOLET with thermal evaporated (left) and spin-coated (right) source electrode.

# 3.6 Thin Films and Devices Characterization

# 3.6.1 Thickness Measurement

The picture of KLA Tencor P-6 profilometer that has been used to determine the thickness of the prepared thin films is presented in Figure 3.9(a). The P-6 profiler analysis system is a powerful apparatus for surface topography analysis. The system uses a contact mode in which the stylus tip is moved on the thin film surface and

profiling the surface physical variation. This machine is capable to measure the medium size of sample with maximum scan length of 150 mm. The thickness of the thin film was measured from the steps height different between the substrate (base) and the surface of the thin film layer. This patterned was formed by scratching carefully the sample with a knife, but not to scratch the substrate, prior to measurement. Figure 3.9(b) shows a typical scanning process to determine the thickness of the thin film using this machine. The stylus tip is moving in the given direction and generate force analog signal which is converted to a step digital signal. The surface profile of the sample was placed on top of the sample stage. The stylus tip was then move downward to approach the sample. Once the tip has reached the sample surface, the sample stage was moved to find the scratched mark on the sample. After the scratched mark was found, scanning was performed with an applied force of 2 mg and scanning length of 200 µm.



Figure 3.9: A typical measurement of thickness using the step height difference method.

### 3.6.2 UV-Vis Characterization

Optical properties of the thin films were performed by using UV-vis spectrometer brand Jasco model Lambda 750 as shown in Figure 3.10(a). The equipment was used to analyze transmission and absorption properties of the AgNWs and the MEH-PPV films, respectively. The optical path of the system is presented in Figure 3.10(b). The system was sourced with a deuterium discharge tube and a tungsten iodine lamp that allow the optical measurement from UV to visible and near infra-red region. The beam from the source is spreaded by grating in the monochromator and splitted into two light paths by a sector mirror, entering the thin film and a reference glass substrate. These lights are then incident on the photomultiplier tube, which convert the photon energy count into an electrical signal. The signal is then amplified and processed by software to come out with an optical spectrum of the film. The optical data of the sample was collected from 250 to 800 nm, as the visible range was the region of interest in this work. The cleaned substrate was used as the reference to get an absolute value of optical properties. The background scan was performed using the reference substrate prior to the measurement of the samples.



**Figure 3.10:** (a) Lambda 750 UV-VIS-NIR Spectrometer and (b) the optical path of the UV-VIS-NIR system.

# 3.6.3 Photoluminescence Characterization

The photoluminescence (PL) spectroscopy is another type of optical analysis. The Perkin Elmer LS 50B Luminescence spectrometer is used to perform PL analysis in this study (see Figure 3.11(a)). The optical path of the system is illustrated in Figure 3.11(b). This machine is equipped with a Xenon light source which allow excitation wavelength to be set from 200 to 700 nm. The excitation light is transmitted through a slit to confined the size, and then hit a grating monochromator. This is where the excitation wavelength is selected. The selected excitation light is then passed through a filter and polarizer wheel for stabilizing the light polarity. The polarized and stabled excitation light is then reached the thin film sample that placed inside the sample compartment. The excited sample is then emit the photoluminescence emission, which then goes into polarization and grating process, and then finally detected by the photomultiplier. All the experimental setups including selecting the excitation wavelength, beam slit size, and scan speed is performed and monitored by a FL WinLab interface software. PL analysis was performed on MEH-PPV thin film with excitation wavelength of 480 nm, 10 nm slit size and 800 nm min<sup>-1</sup> of scan speed.



**Figure 3.11:** (a) LS 50B Luminescence meter and (b) the optical path of photoluminescence spectrometer.

### 3.6.4 Scanning Electron Microscope (SEM) Analysis

Nanoscale surface image of the sample was obtained by using the scanning electron microscope (SEM) model Hitachi SU1510 (see Figure 3.12(a)). This equipment is built with 4 high sensitive semiconductor back scattering electron (BSE) detectors, which allow an observation of sample topography from four different orientations without the need to rotate the sample. Schematic diagram of the working principal of SEM imaging was presented in Figure 3.12(b). The image from SEM is obtained when the focused beam electron interact with atoms in the sample surface, producing secondary electron that emitted from very close to the sample surface. This process is known as secondary electron imaging. SEM characterization parameters used in this study was tabulated in Table 3.2.



Figure 3.12: (a) Hitachi SU1510 AFM and (b) the basic working principal of AFM.

Accelerating	Working Distance	Emission	Magnification
Voltage (V)	(μ <b>m</b> )	current (nA)	( <b>x1000</b> )
5000	5400	86000	5, 10 and 30

Table 3.2: Parameters of SEM characterization.

### 3.6.5 Atomic Force Microscope (AFM) Analysis

Topological analysis allows determining the surface roughness of the thin film. In this work, this kind of analysis was performed by using an atomic force microscope (AFM) model NTEGRA Prima as shown in Figure 3.13(a). The system is built with the new generation electronics that provides operations in high-frequency (up to 5 MHz) modes. This AFM also has very low noise level which increases the sensitivity of measurement. Basic working principle of AFM is illustrated in Figure 3.13(b). AFM operates by measuring a force between a probe and the surface of the film. The probe is a sharp pyramid tip with 15 to 40 nm end radius, which is attached on a cantilever. To obtain the sample morphology, AFM measures the vertical and lateral deflections of the cantilever by using the optical lever. A laser beam is shone on the cantilever where the stylus tip is allocated at the bottom. The optical lever operates by reflecting this laser beam off the cantilever. The reflected laser beam strikes a position-sensitive photodetector consisting of four-segment photo-detector. The differences between the segments of photo-detector of signals indicate the position of the laser spot on the detector and thus the angular deflections of the cantilever. The signal is then processed by using lock-in amplifier before the phase and the topography of the film is obtained. The AFM image in this study was taken at 10 µm x 10 µm of scan size.



Figure 3.13: (a) NTEGRA Prima and (b) the working principal of AFM.

# **3.6.6 4-Point Probe Analysis**

The electrical resistivity of the AgNW sample was determined by using a 4-point probe model Jandel Universal Probe, which connected with Keithley 2012B source meter as shown in Figure 3.14. The system is consisted of four working tungsten wires, which connected to a source measure unit (SMU), where the current is sourced at probe 1 and 4, and the voltage reading is collected from probe 2 and 3. From the output data, the resistivity, R, is obtained from the gradient of the voltage-current graph, while the sheet resistance,  $R_s$ , and bulk resistance,  $R_b$ , can be calculated by:

$$R_s = 4.532 \times R \tag{3.1}$$

$$R_b = R_s \times t \tag{3.2}$$

where t is the thickness of the film. The samples were placed on the sample stage and the probes were lowered to touch the sample surface. The current was sourced from 0 to 10 mA and the measurement was repeated to get 6 sets of readings at different spot on the sample.



Figure 3.14: Jandel Universal Probe and Keithley 2612B.

The 4-point probe setup is shown in Figure 3.15. It consists of four tungsten carbide probes that equally separated by 1 mm of probe spacing, *s*. Under a spherical protrusion of current emanating from the outer probe tips, the resistance for thin film where the film thickness t  $\ll$  s, the probe spacing is derived as:

$$R = \int_{x1}^{x2} \rho \, \frac{dx}{2\pi xt} = \int_{s}^{2s} \frac{\rho}{2\pi t} \frac{dx}{x} = \frac{\rho}{2\pi t} \ln 2 \tag{3.3}$$

where  $\rho$  is the sheet resistivity for a thin film. Consequently, R=V/2I, then the sheet resistivity can be expressed as:

$$\rho = \frac{\pi t}{\ln 2} \left( \frac{V}{I} \right) \tag{3.4}$$

and the inverse of this equation give the conductivity value (Schroder, 2006):

$$\sigma = \frac{\ln 2}{\pi t} \cdot \left(\frac{l}{V}\right) \tag{3.5}$$

however, in general, the sheet resistivity  $R_s = \rho/t$  can be expressed as:

$$R_s = k\left(\frac{v}{I}\right) \tag{3.6}$$

where V/I can is obtained from the slope of I-V characteristic of the 4-point probe.



Figure 3.15: Setup for resistivity measurement.

### 3.6.7 Current-Voltage-Luminance Measurement

The current-voltage-luminance (*J-V-L*) characteristics of the devices are measured using a Konica Minolta CS-200 chroma meter as shown in Figure 3.16. This unit is also connected to the dual channel Keithley 2612B source meter. The CS-200 is a high-precision measurement for luminance and chromaticity, which measure the spectral emittance of the light device and performs calculations using the spectral sensitivity characteristics (color-matching functions) corresponding to the sensitivity of human eye. Customized software is used to control the parameters measured for the VOLETs. The device was placed on the sample holder as shown in the insert of Figure 3.15. Electrical cables from the source meter were connected to the connector leg at the device. Each connector legs represents the different electrodes such as the gate, the drain and the source points of the device. The sample holder was then fixed inside the dark box to avoid light distraction during device characterization. The characterization parameters such as range and step size for both gate and drain voltage, and current limit

of the measurement were setup prior analysis execution. For the VOLET analysis, the current and luminance data was collected simultaneously during the measurement. Two set of analysis were performed for VOLET device, which are output and transfer characterizations.



Figure 3.16: CS-200 Konica Minolta and sample holder of VOLET device.

From the device characterization, the current-voltage (I-V) and luminance-voltage (L-V) data were obtained. In order to change the unit of current to current density, *J*, the current value obtained is divided with the size of an active area of the device,

current density, 
$$J = \frac{I}{A}$$
 (3.7)

where I the is current in Ampere and A is an active area in meter. Then, according to the formula of power efficiency,

$$\eta_p = \frac{\pi L}{VJ} = \pi \frac{1}{V} \left( \frac{L}{J} \right) = \pi \frac{\eta_c}{V}$$
(3.8)

where  $\eta_p$  is the power efficiency and  $\eta_c$  is the current efficiency of the device.

#### 3.6.8 Electroluminescence Spectroscopy

Electroluminescence (EL) spectra of the device was obtained by using a luminescence meter model SM442 spectrometer (Spectral Products) as shown in Figure 3.17. The system was built with a Toshiba TCD1304 detector and connected with a SMA905 fiber optic cable. The other end of the fiber optic cable is pointed to the pixel of the fabricated device. When the desired voltage was applied to the device, light is emitted from the pixel and entered the fiber optic cable and reaching a monochromator and the detector of the spectrometer. The signal is processed and the EL spectrum of the device is produced.



Figure 3.17: SM442 Spectrometer connected to fiber optic cable.

# 3.7 Summary

Materials used including organic semiconductor, dielectric, metal and substrates have been introduced. Substrate cleaning processes have been described in details and it is very important to avoid any contamination on the sample. The spin-coating and thermal evaporator techniques have been explained. These techniques have been used to fabricate thin films and devices in this thesis. Characterization techniques for sample analysis also have been described. The apparatus used were research-class equipment, thus the outcomes of this study were reliable and meet high-quality research standard.

# CHAPTER 4: PRELIMINARY STUDY ON VERTICAL ORGANIC LIGHT-EMITTING TRANSISTORS (VOLETS)

#### 4.1 Introduction

This research was initially starts with the fabrication of two types of VOLETs, which are static-induced transistor (SIT), and nano-porous intermediate source electrode. Both VOLETs have a unique device structure and different types of emissive materials was used for each devices. The only similarity of these devices are both of them were fabricated by using a spin-coating technique. In this Chapter, the fabrication process of the different types of VOLETs design is introduced. The basic device physics of these VOLETs was explained. This chapter is divided into two parts according to the types of VOLETs structure. This initial study was performed to understand different method to produce the solution processable VOLETs and to analyze the properties so that the electrical and luminesce mechanism of the device can be understood. The study presented in Chapter 4 has been published in Nanoscience and Nanotechnology Letters (Mohd Sarjidan et al., 2014) and Journal of Optoelectronics and Advanced Materials (Mohd Sarjidan & Abd. Majid, 2018).

### 4.2 Static Induction Transistors (SIT) based VOLETs

Several designs of VOLETs have been reported to date. K. Kudo et. al. has utilized a combination of combining static induction transistor (SIT) (Kudo et al., 1998) with OLED to fabricate the VOLET and investigate the static and dynamic characteristics of the device (Kudo et al., 2003). Multilayer SIT type of OLET has been reported by Lee et al. (2012). Recently, it has been reported that the lithium fluoride (LiF) layer was deposited in between the gate and source electrodes of MEH-PPV based OLET (Reshak et al., 2013). Other groups fabricate the OLET with dielectric or insulator layer to form a depletion region in order to control the amount of charge carrier by varying the gate

voltage (Katagiri et al., 2011; Ohtsuka et al., 2012; Seo et al., 2009; Yamao et al., 2009; Yumusak et al., 2013). In 2004, Park et. al (Park & Takezoe, 2004) have reported the characteristic of a top-gate-type OLET. The OLET is consisted of patterned indium thin oxide (ITO) as drain and source planar electrodes, followed by organic transporting and emissive layers and top aluminium (Al) electrode which acts as a gate. The fabrication process is similar to the normal single-layer OLED fabrication (Mohd Sarjidan et al., 2013), except the ITO was patterned to form drain and source electrode, separated with a gap size of 30 µm. The device reported by Park et. al (Park & Takezoe, 2004) was prepared in a glove-box, and the organic layers are deposited using a thermal evaporation method.

In this thesis, the VOLET has been fabricated by patterning the Al metal layer to form source and gate electrodes with a gap of 50  $\mu$ m. Simple solution process has been employed to form the emissive layer. The device was prepared outside the glove-box. Current and EL characteristics, and light switching for both source and gate channels were investigated with respect to the gate biases.

### 4.2.1 VOLET Fabrication

ITO substrates were patterned by covering a part of the surface with Kapton® tape and etching with diluted hydrochloric acid (HCl:deionized, 1:1) at temperature of 100 °C. PEDOT:PSS solution was then spun coated on top of the cleaned patterned ITO substrates at the spin rate of 7000 rpm for 20 s. Alq<sub>3</sub> in chloroform solution of concentration 15 mg/ml was then spun coated on the PEDOT:PSS layer at the spin rate of 1500 rpm for 40 s. The devices were soft-baked using a hot plate at 100 °C temperature for 60 s after each of spin-coating step to remove the remaining solvent. Thickness of the PEDOT:PSS and the Alq<sub>3</sub> layers measured, was 20 and 63 nm, respectively. Finally, a top electrode of Al metal was evaporated through a special mask in vacuum condition of 2 x  $10^{-5}$  mbar. A copper wire of 50 µm diameter, has been use to form a gap between cathode and the gate. Although the architecture is seem like a two pixels OLED, this SIT structure is design to prevent shielding electric fields between the source and the drain. This is known as surface-gate SIT. Figure 4.2 shows a schematic diagram of the evaporation process. Current-voltage-luminance (*J-V-L*) characteristics of the OLET devices were performed by using a Konica Minolta CS-200 chroma meter. The cathode electrode was grounded while the gate electrode was negatively and positively biased. The voltage was swept from 0 to 20 V between cathode and anode for each gate bias. Measurement was performed was room temperature, and the fabricated device is not encapsulated.



Figure 4.1: Evaporation process of Al as a cathode and gate electrode.

#### 4.2.2 Output Characteristics and Device Mechanism

Figure 4.2 shows output current characteristic of the VOLET device for gate biased from +5 to -15 V. Current density increases when the gate sweeps from positive to negative bias. The threshold voltage ( $V_{th}$ ) of the device is reduced from 17.5 to 17 V for

gate biased from +5 to -5 V, respectively. Rapid increase in the current density can be observed when the magnitude of negative bias is increased up to -15 V. When the bias gate is set to -15 V, the  $V_{th}$  is reduced to 12 V.



Figure 4.2: Output current characteristic of VOLET for gate biased from +5 V to -15 V.

Figure 4.3 shows the output luminance characteristic of the device. A unique luminescence-voltage (*L-V*) characteristic can be observed where the luminance is obtained from the drain channel and compared to that of gate channel. The luminance intensity pattern of the drain channel was observed to reduce when the gate bias was varied from +5 to -5 V. The turn on voltage ( $V_{on}$ , when L=1 cd/m<sup>2</sup>) of the device was increased from 18 to 19.5 V. On the other hand, the light output intensity of the gate channel was observed to reduce rapidly until no emission was detected (for L=1 cd/m<sup>2</sup>) when the gate electrode was set at 0 to 5 V. The  $V_{on}$  at this channel is 18 V for -5V gate bias.



Figure 4.3: L-V characteristic of OLET at (a) drain channel and (b) gate channel.

Figure 4.4 shows a schematic diagram of the EL mechanism of the VOLETs for both, positive and negative bias on the gate. When the gate was positively biased, holes are injected from anode and transported into the Alq<sub>3</sub> layer. However, the holes are not injected from the gate due to the large potential barrier high of about 1.6 eV (energy differences between LUMO level of the Alq<sub>3</sub> (-5.8 eV) and work-function level of the aluminum gate electrode (-4.2 eV) (see Figure 4.5)). The injected electrons were then travelled and attracted into drain channel as the applied bias for this channel was increased. At the same time, holes and electrons are injected from cathode and anode, respectively. Accumulation of the exciton in drain channel becomes high as  $V_{sd}$ increased followed by a recombination process which leads to a high EL emission. No recombination occurred at gate channel because no electron enters this path to recombine with holes from the anode.



**Figure 4.4:** Schematic diagram of EL mechanism of the VOLET at (a) positive and (b) negative gate bias, where the ( $\bullet$ ) and ( $\circ$ ) are representing electron and hole, respectively, and the black, light-green and dark-green arrows are representing the non-, low, and high output emission intensity, respectively.

When the gate was negatively biased, electron and hole are injected from gate and anode, respectively, into the gate channel. An initial electric field has been created in the gate channel. When the  $V_{sd}$  bias is increased, electrons was injected from cathode and divert into the gate channel due to the initial field. Thus, more recombination of exciton was occurred at gate channel as compared to the drain channel. A significant increase in luminescence intensity and reduction of  $V_{on}$  can be observed in Figure 4.6.



Figure 4.5: Energy band diagram of OLET.



Figure 4.6: L-V characteristic at gate channel at various gate biases.

It is noted that the Alq<sub>3</sub> is also known as an electron transporting material. The mobility of electron is higher than the hole. However, from the energy diagram of the device, the holes are easier to be injected into the Alq<sub>3</sub> as compared to the electrons because the barrier height of the hole is lower compared to the barrier height of electron. Assuming that the density of the holes injected from the anode is similar for both gate and drain channels, negative biased gate resulted in more electrons injected into the Alq<sub>3</sub> layer. The density of electron in the gate channel was higher compared to that in the drain channel because the electron from the drain channel is attracted to the gate channel due to the initial electric field. Thus, more recombination of an electron-hole pair occurs at the gate channel resulting in high luminance compared to the drain channel. This can be observed by plotting the ratio of  $L_g/L_d$  (see Figure 4.7). The ratio obtained increases when higher negative bias was applied at the gate.



Figure 4.7: Luminescence ratio of gate over drain channels.

Drain current density,  $J_d$ , of the device increases rapidly with an increase in magnitude of negative bias at the gate electrode. Electron is a dominant charge carrier of the Alq<sub>3</sub> molecule. Thus, the electron transportation is the major contribution for the current density reading. More electrons will be injected into the Alq<sub>3</sub> layer when the gate is negatively biased. However, a slight reduction in current density is observed when the gate is positively biased due to more holes being injected compared to electron into the Alq<sub>3</sub> layer.

# 4.3 Nano-Porous Intermediate Sourced Schottky Barrier based VOLETs

Even though the previous SIT-based VOFET exhibit a very simple fabrication technique, the device suffer a low luminescence intensity and a high operating voltage above 10 V for  $V_{gs}$ = 0 V which due to the used of single layer Alq<sub>3</sub> as an emissive layer. Moreover, the previous design of the VOLET produced a secondary light emission at gate-drain channel, which is not suitable in display application. In order to consolidate these issues, another polymer emissive material and VOLET design have been introduced.

Since the first conjugated polymer has been reported by H. Shirakawa et. al. (Shirakawa et al., 1977) was a breakthrough in polymer science field, interest in the conjugated polymer research was rapidly expanded to a wide category including conducting, semiconducting, and smart materials. Poly(p-phenylenevinylene) (PPV) has shown a great potential as a multifunction semiconducting polymer material since it can be utilized in OFET (Chen et al., 2014; Muratsubaki et al., 2004), OLEDs (Hewidy et al., 2017; Sarjidan et al., 2010; Suo et al., 2007) and OPVs (Chen et al., 2011; Chen et al., 2010), depending on its derivatives. One of its derivative named MEH-PPV has been used in OLEDs research due to its ability to emit a pure orange light output (Suo et al., 2007). MEH-PPV is highly soluble in common organic solvent and its glass

transition temperature is also high which makes it easily deposited in such device by solution processing technique (Prajongtat et al., 2013; Zheng et al., 1998). In order to show the potential of MEH-PPV in both OLEDs and OFETs, Reshak et al. has reported an electrical behavior of MEH-PPV polymer based VOLETs (Reshak et al., 2013). The paper only focuses on the electrical properties of VOLET with different thickness of MEH-PPV. No result on electroluminescence was presented and the device physics on the current modulation by gate voltage was also not clearly explained.

This study will demonstrate an electroluminescence property of MEH-PPV based VOLETs. Current and luminance of the VOLETs were analyzed in terms of output and transfer characteristics. Physical mechanisms such as injection, transportation and recombination of charged carries were discussed in detail in Section 4.3.2.

#### 4.3.1 VOLET Fabrication

PEDOT:PSS was spin-coated onto the cleaned ITO substrate at 2500 rpm for 40 s, and baked at 120 °C for 30 minutes to removes residual water. For emissive layer, 4 mg/ml of MEH-PPV from chlorobenzene solution was spin-coated at 800 rpm onto the PEDOT:PSS layer to obtain ~47 nm thick film and baked on a hot plate at 100 °C for 30 mins. A 20 nm thick of aluminum (Al) source electrode was thermally evaporated followed by 150 nm lithium fluoride (LiF) as a dielectric layer. Finally, 100 nm thick of Al was thermally evaporated as the top gate electrode. VOFETs construction is presented in Figure 4.8. The devices were encapsulated to avoid degradation and stability.



Figure 4.8: Device architecture of VOLETs.

# 4.3.2 Output Characteristics and Device Mechanism

Figure 4.9 (a) shows output current characteristics of the fabricated VOLETs. Potential different between drain and source  $(V_{ds})$  was fixed to be from 0 to 10 V for all samples. Gate to source voltage  $(V_{gs})$  was varied from +3 V to -1 V for each  $V_{ds}$  swept. The current density of  $V_{ds}$  increases as the negative value of  $V_{gs}$  increases. Threshold voltage for the VOLETs observed reduces towards lower voltage when  $V_{gs}$  is more negative. A similar trend was observed for the luminance graph as shown in Figure 4.9 (b) where the light intensity increases with the increment of negative value of  $V_{gs}$ . This modulation behavior of current density and luminance is known as transistor effects since  $V_{gs}$  was used to control the intensity and the characteristics of the device.



Figure 4.9: Output (a) current and (b) luminance of VOLETs.

The important key to this modulation behavior is the special porous features of the aluminum source electrode. Figure 4.10 shows the SEM image of the 20 nm thin aluminum electrode. From the SEM image, several holes were observed within the size of 500 to 900 nm in diameter. These holes are relatively bigger than the thickness of the aluminum. The large size of the hole as compared to the thickness of the aluminum result in discontinued porous structure (Xu et al., 2007). The function of these holes and

the ultra-thin layer of aluminum is to allow energy band contact between emissive materials and the gate electrode. Upon an appropriate  $V_{gs}$ , the energy band of the emissive materials can be tuned and spontaneously modulate the current density as well as the luminance intensity.



Figure 4.10: SEM image of 20 nm aluminum source electrode. Insert is the higher magnification image of the selected area.

Figure 4.11 shows the schematic diagram of injection mechanism of the electron at MEH-PPV/Al interface at a different condition of  $V_{gs}$ . These schematic diagrams are presented to illustrate the charged carrier behavior in the VOLETs. At  $V_{gs}$ =0, the VOLETs acts as ordinary OLED. Under a significant voltage across drain and source, the current will exponentially increase after entering the space-charge limited-current (SCLC) region and light will start to be emitted and the light will become brighter for higher  $V_{ds}$ . At  $V_{gs} > 0$ , the positive charge will be accumulated at the MEH-PPV/Al interface and increased the potential barrier height, which results in a reduction of injection of electron from the source into MEH-PPV layer. The other situation is when

the  $V_{gs} < 0$ , since the gate was biased with the negative potential, the electron will be accumulated at the MEH-PPV/Al interface and lower the potential barrier height, which significantly improved the injection of the electron into the emissive MEH-PPV layer. The light emission intensity is directly proportional to the amount of charged carrier accumulated in the MEH-PPV layer. High exciton formation from the high population of charged carrier accumulation will produce the high intensity of light.



**Figure 4.11:** Schematic diagram of energy band alignment at MEH-PPV/source/dielectric/gate of VOLETs at different gate voltage.

The efficiencies of the VOLETs can be divided into 2 types that are, current ( $\eta_c$ ) and power efficiencies ( $\eta_p$ ), which are adopted from OLED analysis by considering the output characteristics as a basis of the calculation. Figure 4.12 (a) and (b) shows the current and power efficiencies of the VOLETs at different V<sub>gs</sub>, in linear and logarithm scale, respectively. It is found that the efficiency of the VOLETs is increases when V<sub>gs</sub> is becoming more negative, especially when the V<sub>gs</sub> increases from -1 to -3 V. At these V<sub>gs</sub>, the value of current and power efficiency increases from 0.0032 to 0.0034 cd/A, and from 0.0010 to 0.0015 lm/W, respectively. It is postulated that the amount of exciton radiative recombination is higher when V<sub>gs</sub> was biased with the negative voltage, which finally results in brighter luminance with relatively low current density. It is also suggested that the improvement of electron injection by negative V<sub>gs</sub> facilitates more balance hole-electron accumulation in the emissive layer since the nature of MEH-PPV is known as p-type materials in which dominated by hole carrier mobility.



Figure 4.12: Efficiencies of VOLETs at different gate voltage in (a) linear and (a) logarithm scale.

### 4.4 Conclusions

Alq<sub>3</sub> VOLET has been fabricated using solution processed, and the EL properties of the device have been characterized. The current characteristic of the device depends on electron transportation in emissive layer. The initial internal electric field plays an important role to attract the electron flow into the respective channel. The luminescence characteristic shows an opposite pattern between gate and cathode channels. The ratio of light intensity also depends on exciton accumulation as a respond to the gate bias.

The EL properties of MEH-PPV based VOLETs have been also demonstrated. The current and luminance properties of the VOLETs have been analyzed in terms of output and transfer characteristics. The porous structure is an important feature for source electrode in VOLETs fabrication. The fabricated VOLETs can be modulated with a minimum  $V_{gs}$  of 1 V. Modulation of current by  $V_{gs}$  in the VOLETs was related to the change in magnitude of potential barrier height at the MEH-PPV/Al interface. Efficiencies of the VOLETs were higher at stronger negative  $V_{gs}$  due to more balance exciton formation and recombination.

Since the Alq<sub>3</sub> based SIT-VOLET has a poor performance due to high turn-on voltage and secondary luminance output at gate electrode, MEH-PPV based VOLET were selected to proceed to the next work, in which a porous silver electrode was deposited to replace the aluminum as the source electrode. Details analysis were also explained in the next Chapter 5.

# CHAPTER 5: VOLETS WITH THERMALLY EVAPORATED POROUS SILVER INTERMEDIATE SOURCE ELECTRODE

### 5.1 Introduction

The technology of the thin-film transistors (TFT) has been developed in the past years was motivated by the increased attraction in various applications such as wearable electronics and the Internet of thing. The present single crystalline transistors have several disadvantages such as high in cost, complex to integrate and fragile in structure, which are unsuitable for flexible field-effect electronic. One promising solution that can address these issues for TFT is by using organic field effect transistors (OFETs) (Bao & Chen, 2016; Someya et al., 2016). Unfortunately, the relatively low motilities of organic semiconductor compared to that of inorganic silicon has become a big challenge that hinders commercialization of OFETs. The ordinary OFETs is designed as a planar structure in which source and drain electrodes are deposited side-by-side with a distant (known as channel length) of micrometre. Since the mobility of organic semiconductor materials is low, the output current of the OFETs is relatively low due to the wide distant between these two electrodes. The channel length can be reduced from micrometre to nanometre size to counter the low mobility of the organic semiconductor materials. As a result, a new structure of OFETs, known as vertical OFETs (VOFETs) has been introduced (Li et al., 2008; Ma & Yang, 2004). The structure of OFETs has been modified from planar into vertical. Another virtue of the vertical structure is that an organic emissive material can be deposited as an active layer to multiply the function of the device, as a transistor and also a light emitter. This design allows a large emission area which is favourable for active matrix OLED (AMOLED) displays.

According to established device physics of VOLETs, the gate bias from the capacitor cell is operated to change the injection barrier at the source/organic semiconductor interface. By applying voltage across the diode cell, current can drift from the source to the drain electrode. Thus, the modulation of current from source to drain in the diode cell is highly depended on the change of the injection barrier by the gate voltage. Similar to conventional planar OLETs, the current profile with respect to drain and gate voltage can also be interpreted as output and transfer characteristic, respectively for the VOLETs. However, the pattern of the current profile is not identical between OLETs and VOFETs due to different mechanisms that may take place in both devices. The saturation current in OLETs can be easily observed from their output characteristic, which is related to the pinch-off phenomenon as a result of depletion of charge. On the other hand, current profile for VOLETs usually follows a diode curve characteristic, whereby the current increases exponentially with the increase in drain voltage without the occurrence of saturation.

In Chapter 4, MEH-PPV VOLET with ultra-thin layer of aluminum has been successfully fabricated and analyzed. Unfortunately, the used of ultra-thin aluminum (Al) as an intermediate source electrode might be the reason of the low light emission intensity. The ultra-thin aluminum exhibits a low optical reflectivity and transparency, which has absorbed the light emission from the MEH-PPV while the device is operated. Thus, in this chapter, a porous silver (Ag) has been adopted as the intermediate source electrode in the VOFET fabrication. The device physics of the VOLET was also explained in details, not only in the output characteristic, but also in the transfer characteristic of the VOLET. This chapter is divided into two parts, which begins with electrical analysis and followed by luminescence study of the VOLET. This study has been published in Current Applied Physics (Mohd Sarjidan et al., 2018).

### 5.2 Device Fabrication

The architecture of the VOLET device in this study was fabricated based on the combination of diode and capacitor cells as illustrated in Figure 5.1. The basic design is similar with the VOLET fabricated in the Chapter 4. The only difference is that the source and gate are fabricated by silver Ag.



Figure 5.1: Device architecture of the VOLET fabricated in this work.

The PEDOT:PSS (Heraeus Clevios GmbH) was spin-coated onto the cleaned ITO substrate at 2500 rpm for 40 s to form ~40 nm thick film. The buffer layer was then baked at 120 °C for 30 mins to remove any residual water. MEH-PPV with concentration of 4 mg/ml in chlorobenzene solution was spin-coated at 800 rpm onto the PEDOT:PSS layer to obtain ~50 nm thick film. The thick film was then baked on a hot plate at 100 °C for 30 mins. The Ag source electrode of thickness of 100 nm was thermally evaporated to form the intermediate layer with porous morphology. The presence of porous morphology (represented by the black dot) can be observed by scanning electron microscope (SEM) as shown by images in Figure 5.2. It can be seen

that the porous structure are well distributed all over the Ag surface. Diameter of the porous structure is between 200 to 400 nm, which is relatively larger than the thickness of the Ag. This morphology creates a discontinued structure that allows current modulation by the gate voltage in the fabricated VOFET (Xu et al., 2007). Lithium fluoride (LiF) of 150 nm thick and another layer of Ag of 100 nm thick were then thermally evaporated as the dielectric layer and gate electrode, respectively. In order to have a better insight on formation of the porous structure, field emission scanning electron microscope (FESEM) analysis of the Ag metal deposited at different deposition rate of 0.5, 2 and 5 Å/s were performed. Figure 5.3(a)-(c) show the FESEM images of Ag metal at different deposition rate. It was found that surface morphological of Ag depends on the deposition rate. For low deposition rate (~0.5 Å/s), the Ag was formed with almost homogenous medium size particle with some cracks in between them. For medium deposition rate ( $\sim 2$  Å/s), the Ag was grown with mix of fine and large particles with porous features. For the high deposition rate, the Ag also was grown with mix of fine and large, but without porous structure. Figure 5.3(d)-(e) show the FESEM images at different magnification of the Ag electrode deposited at  $\sim 2$  Å/s. The porous structures have numerous sizes and shapes, distributed on the Ag surface. The devices were then encapsulated prior to the performance of several characterization procedures.


Figure 5.2: SEM image of Ag source electrode at low and high magnification (insert).



**Figure 5.3:** FESEM images of Ag source electrode deposited at (a) ~0.5, (b) ~2, and (c) ~5 Å/s at 50k magnification, and different magnification of (d) x10k, (e) x30k, and (f) x100k of ~2 Å/s deposited Ag.

#### 5.3 Output Characteristic of VOLET

Output characteristic represents a current response with respect to drain-source voltage (V<sub>ds</sub>), at different gate-source voltage (V<sub>gs</sub>), thus denoted as drain current density (J<sub>d</sub>). Figure 5.4 shows the output characteristic of the fabricated VOLET. The  $V_{ds}$  was swept from 0 to 10 V and  $V_g$  was varied from +3 to -3 V. Since the output characteristic probes the current profile at the diode cell in such a VOLET, a diode curve property was clearly observed for all values of V<sub>gs</sub>. It is noticed that when the bias polarity and magnitude of V<sub>gs</sub> was increased toward negative value, the magnitude of J<sub>d</sub> was observed to increase. The opposite behaviour was observed when  $V_{gs}$  was positively biased, J<sub>d</sub> value was reduced significantly. This modulation of current density by V<sub>gs</sub> can be referred as a transistor effect. On the other hands, it is noticed that a knee voltage of the VOLET is shifted to a lower value when V<sub>gs</sub> was biased from positive to negative voltage. It is hypothesised that the reduction of the knee voltage in the diode is associated to a reduction of an injection barrier at metal/organic semiconductor interface. This has certainly improved the injection process of charge carrier from metal electrode into the organic semiconductor layer. In this case, the injection barrier is reduced with respect to the negative of V<sub>gs</sub> value.



Figure 5.4: Output current characteristic of the fabricated VOLET.

In order to clarify the dependency of the injection barrier with respect to the  $V_{gs}$ , carrier, tunneling mechanism was further analyzed using Fowler-Nordheim (FN) theory. In FN theory, the charge carrier needs to experience a sufficient electric field, in order to overcome the injection barrier height,  $\phi$ , before it passes through the metal-organic interface. The FN tunneling can be described mathematically by Equation 5.1 and simplified by Equation 5.2

$$J \propto F^2 \exp\left(\frac{-K}{F}\right)$$
, where  $K = \frac{8\pi (2m*)^{\frac{1}{2}\phi^{\frac{3}{2}}}}{3qh}$  (5.1)

$$\ln\left(\frac{J}{F^2}\right) \propto -K\left(\frac{1}{F}\right) \tag{5.2}$$

where F is an electric field (F=V/d, d is thickness of the organic thin films),  $m^*$  is the effective mass of electron, q is the elementary charge, h is the Planck constant and K is the gradient obtained from the plot of  $ln(J/F^2)$  vs 1/F (see Figure 5.5(a)). Figure 5.5(b) shows the relationship between V<sub>gs</sub> and the value of injection barrier height of the

VOLET. The injection barrier is reduced when the  $V_{gs}$  was biased towards negative value. This analysis has justified the role of  $V_{gs}$  in tuning the injection barrier as well as the threshold voltage. Improvement on the injection mechanism has induced more charge carriers to be injected from metal electrode into the MEH-PPV layer. As a result, an increment in the current density was observed in the VOLET.



Figure 5.5: (a) FN plot and (b) injection barrier height profile at different  $V_{gs}$ .

#### 5.4 Device Physics of the VOLET

The physics of the VOLET device was further investigated with respect to the energy band diagram of diode cell of VOLET and the overall VOLET as illustrated in Figure 5.6(a) and (b), respectively. From cyclic voltammetry and optical absorption analyses (see Appendix A), the energy value of high occupied molecular orbital (HOMO), and the lowest unoccupied molecular orbital (LUMO) were obtained to be 5.2 and 3.0 eV, which are similarly as reported in (Davids et al., 1997). From Figure 5.6(a), the energy value of high occupied molecular orbital (HOMO), and the lowest unoccupied molecular orbital (LUMO) are 5.2 and 3.0 eV, respectively (Davids et al., 1997). The work function of ITO/PEDOT:PSS (drain) and Ag (source) are 5.1 eV (Kim et al., 2018) and 4.4 eV (Ford & Pritchard, 1971), respectively. These energy work functions were aligned with the fermi energy of MEH-PPV ( $E_F$ =-4.8 eV) (Davids et al., 1997), forcing the energy band to bend, after all layers were connected with each other. The value of an injection barrier of hole (at PEDOT:PSS/MEH-PPV interface) and electron (at Ag/MEH-PPV interface) obtained are 0.1 and 1.4 eV, respectively. Based on the previous FN analysis, the injection barrier value obtained is assumed to be the value of hole injection barrier of the VOFET. This assumption is based on a consideration that an initial value of injection barrier may equal to 0.1 eV (when  $V_{gs} = 0$  V), which fall in between the value of the injection barrier when  $V_{gs}$  was biased between -1 and +1 V. This value also indicates that the diode cell can be considered as a hole-only device (Sun & Dalton, 2008). An ideal VOFETs operation requires a positive  $V_{gs}$  in order to reduce the injection barrier. When Vgs is positively biased, a negatively charged carrier is drifted towards the gate, while the positively charged carrier is moved to the opposite direction towards the source (Ag), as shown in Figure 5(b). Since the dielectric is acting as an insulating layer, ideally there is no current (or very small amount of current) flows from source to gate. The positively charged carrier that has accumulated at the LiF/Ag source interface attracts electrons from the MEH-PPV to accumulate at the MEH-PPV/Ag source interface, which consequently has decreased the injection barrier at the interface. This has induced a strong band bending in the MEH-PPV layer near the Ag source porous region. The Schottky barrier width in the vicinity of the LiF/MEH-PPV interface becomes significantly narrow, facilitating electron injection from the Ag source to the MEH-PPV layer. At the same time, the injection barrier of hole is also reduced due to band bending at the PEDOT:PSS drain/MEH-PPV interface.



Figure 5.6: (a) Band energy diagram of MEH-PPV diode cell and (b) transistor mechanism for an ideal MEH-PPV based VOLET.

However, an unusual result was obtained from the fabricated VOLET in this work. The present study shows that the reduction of injection barrier is achieved by a negative bias at V<sub>gs</sub>, and not at a positive bias as has been explained theoretically. In order to explain the unusual data, leakage current analysis was performed on the VOLET. Figure 5.7(a) shows the leakage current characteristics under gate bias from -5 to +5 V. Surprisingly, the leakage current is quite large with a maximum value of  $\sim 2A/cm^2$  at  $V_{gs}$ =5 V. Resistant value of this current-voltage profile was obtained as 35.71  $\Omega$ . The experiment has been repeated several times and similar results were obtained. This may cause by low capacitance value of LiF as shown in Figure 5.7(b). It is believed that the high leakage current might influence the unexpected result. Thus, a new possible mechanism is proposed to explain the device physics of the VOFET. Since the leakage current is high, the LiF is behaving like a resistor, as salt doping can occur due to diffusion of LiF into the MEH-PPV (Wang et al., 2013), rather than as an insulator or a capacitor. When the gate was negatively biased, the electrons were injected and transported from the gate into the MEH-PPV layer through the porous Ag source and they were expected to accumulate at MEH-PPV/Ag source interface as shown in Figure 5.7(c). The rest of mechanism is then followed the usual device physics of the ideal VOFETs where the injection barrier is reduced. Some may argue that this result can simply be obtained by probing the source and the gate at the same terminal (short circuit) and the drain at the opposite electron in the diode cell. However, from our analysis on the two terminals diode (anode (drain) and cathode (source-gate short circuited), the output current density obtained was the same, even when the polarity and magnitude of V<sub>gs</sub> were varied as presented in Figure 5.7(d). The similar result was obtained for the device with non-porous Ag source electrode (deposited at ~5 Å/s), indicating that the porosity in the source electrode is an important features to achieve the transistor effect for the device.



Figure 5.7: (a) Leakage current plot, (b) capacitance plot of LiF, (c) suggested mechanism of the fabricated VOLET and (d) current-voltage characteristic of MEH-PPV diode.

### 5.5 Determination of Carrier Mobility of the VOLET

Carrier mobility of planar structured organic field effect transistors (OFETs) is usually obtained by manipulating a saturation region of transfer characteristic. However, there is no clear method to calculate the mobility for either VOFET or VOLET. Since  $J_d$ output characteristic is directly representing the current property of the MEH-PPV diode cell, a mobility of the VOLET can be estimated by using space charge limited current model. By assuming that the MEH-PPV is a perfect insulator without an intrinsic carrier, the SCLC can be explained by Mott-Gurney equation (Lampert & Mark, 1970):

$$J_{SCLC} = \frac{9}{8} \varepsilon_o \varepsilon_r \mu \frac{v^2}{d^3}$$
(5.3)

where  $\varepsilon_o$  is the permittivity of free space,  $\varepsilon_r$  is the dielectric constant of MEH-PPV (assumed as 3),  $\mu$  is the carrier mobility, V is the applied voltage. In a real device, V is influenced by the voltage drop due to contact resistance and series resistance across the electrodes  $V_r$ , and the built-in voltage,  $V_{bi}$  (Liu et al., 2016). Thus, Equation 5.3 become:

$$J_{SCLC} = \frac{9}{8} \varepsilon_o \varepsilon_r \mu \frac{(V - V_r - V_{bi})^2}{d^3}$$
(5.4)

In a transistor, the  $V_r$ - $V_{bi}$  can be referred as a threshold voltage,  $V_{th}$ , thus Equation 5.4 can be simplified as:

$$J_{SCLC} = J_d = \frac{9}{8} \varepsilon_o \varepsilon_r \mu \frac{(V_d - V_{th})^2}{d^3}$$
(5.5)

Figure 5.8(a) shows the fitted plot by using Equation 5.5 in a log scale of drain current at different gate voltage. As the SCLC model shows a square relationship of voltage with respect to the current, a plot of square root of drain current is also presented in Figure 5.8(b). It is observed that the calculated values of drain current from SCLC model are perfectly fitted to the experimental data. From the fitting, the threshold voltage, V<sub>th</sub> and mobility,  $\mu$  of the VOLET are obtained. Both values decreased when V<sub>gs</sub> was biased from positive to negative value as shown in Figure 5.8(c). The decreased in V<sub>th</sub> can be attributed to the reduction in the injection of barrier height. The calculated value of mobility,  $\mu$  is in the range between  $1.35 \times 10^{-5}$  to  $1.50 \times 10^{-5}$  cm<sup>2</sup>/V.s, which is similar to that reported for hole mobility of MEH-PPV (Inigo et al., 2005) and transistor mobility of conventional planar MEH-PPV-based OFET at high V<sub>ds</sub>=V<sub>gs</sub>= -40 V (Amorim et al., 2012). A slight reduction in the mobility can also be related to an improvement in the electron injection and transportation of charge carriers in the MEH-PPV layer (Shi et al., 2007) as the electron injection barrier at the MEH-PPV/Ag source interface may also be reduced by negative V<sub>gs</sub>.



**Figure 5.8:** Experimental and fitted data of drain current in (a) log scale and (b) square root form, and (c) threshold voltage,  $V_{th}$  and mobility,  $\mu$  calculated at different gate voltage.

#### 5.6 Transfer Characteristic of VOLET

Figure 5.9(a) shows the transfer current characteristic of the fabricated VOFET measured for  $V_{gs}$  from -10 to + 10 V and  $V_{ds}$  from 0 to 5 V. In general, the magnitude of J<sub>d</sub> is observed to increase with respect to the increase in V<sub>ds</sub>. For each V<sub>ds</sub>, J<sub>d</sub> starts to increase exponentially when  $V_{gs}$  is biased from +4 to -4 V. J<sub>d</sub> reaches a clear saturation current when a higher negative biased is applied to V<sub>gs</sub>, especially when V<sub>ds</sub> is biased from 2 to 5 V. As discussed earlier, when  $V_{gs}$  magnitude is becoming more negative, the injection barrier is reduced. At Vgs>5 V, the injection barrier is too high, and thus the charge carrier is prevented from being injected from source/drain and transported in the MEH-PPV layer. There will be no current collected. However, when Vgs<5 V, the injection barrier becomes narrow, hence allowing the charge carrier to be transported in the MEH-PPV. The increase in  $J_d$  depends on  $V_{gs}$  as the reduction of injection barrier is proportional to  $V_{gs}$  as evident in the previous Figure 5.5(b). It is observed that  $J_d$  is not equal to zero when V<sub>gs</sub>=0 (known as off-state). This is actually a minimum current that flow in the device and is known as the off-state current, Joff. In real application, Joff should be very small especially in a low power device. However, the optimization of Joff is not in the scope of this work. When  $V_{gs} < -5V$ , the injection barrier is very small (almost zero) (Xu et al., 2007), thus the current flow is saturated at a maximum value, known as saturation current ( $J_{sat}$ ). The saturation region of a VOFET is also referred as an on-state. At this state, the value of J<sub>sat</sub> is exponential dependent on the magnitude of  $V_{ds}$ , as shown in Figure 5.8(b). It is noticed that  $J_d = 0.064 \text{ mA/cm}^2$  at the on-state, even though the value of  $V_{ds}=0$  V. It is expected that, there is no current (or very small current) can flow in the diode cell when V<sub>ds</sub>=0 V. This indicates that J<sub>d</sub> was contributed by a high leakage current coming from the gate as previously described. The maximum current of the VOLET is above 280 mA/cm<sup>2</sup>, which is considered as very high compared to other solution processed VOFETs (Ben-Sasson et al., 2012; Mohd Halizan

et al., 2017). Further improvement is required since it still suffer from a low on/off ratio ( $\sim$ 5.08) as J<sub>off</sub> is quite high for the VOLET.



Figure 5.9: (a) Output characteristic and (b) on/off state current of the VOLET.

### 5.7 Luminescence Properties of VOLETs

Figure 5.10(a) and (b) present luminance plot from output and transfer characteristics, respectively. Both plots show identical pattern with respect to their current characteristics. This is expected because the exciton formation and the brightness of emission are highly dependent on current density in typical OLEDs. From Figure 5.10(a), the maximum luminance obtained is ~77 cd/m<sup>2</sup> when  $V_{gs}$ = -3 V and  $V_{ds}$ = 10V. The saturation region (on-state) is also observed in the transport characteristic as presented in Figure 5.10(b).

Figure 5.11 shows the luminance profile at on/off state of the VOLET. The luminance characteristic increases exponentially when  $V_{ds}$  increases from 0 to 5 V. The maximum brightness of an on-state recorded is ~10 cd/m<sup>2</sup> at  $V_{ds}$ =5 V. Although this value is still considered low as compared to the other reported VOLET (McCarthy et al., 2011; Yu et al., 2016), the value is still acceptable since the VOLET fabricated in this study only consisted of a single emissive layer without any transport layers.



Figure 5.10: (a) Output and (b) transfer luminescence characteristics of the VOLET.



Figure 5.11: On/off state luminance of the VOLET.

Figure 5.12 shows the relationship between drain current and luminance output of the VOLET. This figure indicates that luminance intensity is linearly proportional to the increment of  $J_d$ , which is a common relation in OLEDs characteristic. Efficiency of the OLEDs can be obtained from the slope of the graph. Efficiency can be defined as a ratio of output/input. In this case, the output and input are the luminance and drain current, respectively. Behaviour of charge carrier (injection and transportation) can also be investigated from the slope of the graph (Braun & Heeger, 1991). It is well-established that light is generated from radiative recombination of exciton (electron-hole pair). A balance exciton formation induces high efficient device. It can be observed that the slope increases when  $V_{gs}$  was negatively biased, indicating a more balance exciton formation in the VOLET by negative  $V_{gs}$ . This result can be related to a significant reduction in electron injection barrier at MEH-PPV/Ag source interface, which has caused a high injection of electron into the MEH-PPV. This analysis to some extent has verified the mechanism of reduction in the electron injection barrier, as previously proposed.



Figure 5.12: Relationship of luminance brightness and drain current.

## 5.8 Conclusions

MEH-PPV based VOLET has been fabricated by a simple spin-coating method. The porous structure of the intermediate Ag source electrode allows current to be modulated by  $V_{gs}$ . The output characteristic of the VOLET represents the electrical property of the diode, while the transfer characteristic of the VOLET shows transistor behaviour. The VOLET can produce a clear saturation region as the device reaches the on-state condition. The current modulation is related to the change in injection barrier which can be achieved by altering a small magnitude of  $V_{gs}$ . New device physics has been proposed to include the significant role plays by the high leakage current from the gate. The potential of VOLET for display device has been evaluated. Further research is required to improve the on/off ratio and luminance brightness of the VOLET. This concept of device can be utilized with other high performance organic electronic materials which may enhance the performance and fulfil the commercialization requirement.

## CHAPTER 6: VOLETS WITH SOLUTION PROCESSABLE SILVER NANOWIRES INTERMEDIATE SOURCE ELECTRODE

#### 6.1 Introduction

A remarkable contribution has been made by McCarthy et. al. when they introduce VOLETs with a coupling of an aluminum zinc oxide (AZO) capacitor (server as a dielectric gate) with small molecules based OLEDs, interconnected with a single-walled carbon nanotube (SWCNT) as a source electrode (Liu et al., 2008). The idea is that the porous structure of the SWCNT networks allows a connection of energy alignment between the organic layer of OLEDs and the gate electrode which plays an important role for charge accumulation. The concept of porous structure was also applied to ITO source electrode with an average pore size of hundreds nanometer for VOLETs application (Yu et al., 2016). However, both VOLETs suffer a complex fabrication, especially for the source electrode. The SWCNT networks were initially formed on nanoporous mixed cellulose ester membranes using a vacuum filter system before they were transferred to the VOLET, while preparation of the porous ITO was performed using Langmuir-Blodgett (LB) deposition technique, oxygen plasma etching, and sputtering processes.

AgNWs have been attracting more and more attention as a suitable candidate for replacing ITO as a transparent conducting electrode because of their intriguing electrical, thermal, and optical properties (Duan et al., 2016). Ag exhibits an electrical conductivity of  $6.3 \times 10^7$  S/m, which is the highest among all metals, by virtue of which Ag NWs are recognized as very suitable material in flexible electronics which is favorable for the wearable smart sensor for healthcare applications (Jang et al., 2017; Kim et al., 2017; Park et al., 2016; Yan et al., 2014). AgNWs are also easily deposited by solution processing techniques such as spray-coating (Bobinger et al., 2016; Choe et

al., 2017; Ding et al., 2016; Lagrange et al., 2017; Lee et al., 2016), spin-coating (Altin et al., 2016; Han et al., 2017; Lin et al., 2017; Shin et al., 2017; Yu et al., 2017; Zhao et al., 2017) and printing (Araki et al., 2016; Chen et al., 2017; Falco et al., 2016; Hemmati et al., 2016; Liang et al., 2016; Maisch et al., 2016; Maisch et al., 2016; Nian et al., 2016; Zhao et al., 2017), which simplify and reduce the cost of production in future. It is noticeable that the AgNWs networks exhibit porous features and reasonable sheet resistance which made them possible to be the source electrode in VOLETs. Recently, there is some work that reported the use of AgNWs as the source electrode, however, they are only utilized on the vertical organic field-effect transistor (VOFET) (Albano et al., 2017; Mohd Halizan et al., 2017).

In this chapter, a top-gated solution processed VOLETs with AgNWs as an intermediate source electrode is demonstrated. The main objective of this study is to fabricate a solution processable VOLET and to understand the physical mechanism of charge carrier in such device. Deposition parameter of AgNWs was initially optimized before the VOLET was fabricated. Properties and suitability of AgNWs as the source electrode in top-gated type VOLETs were evaluated. Electrical and luminescence properties of output and transfer characteristics of the fabricated VOLETs were analyzed and discussed in detail. This study has been accepted for publication in Journal of Nanoscience and Nanotechnology.

#### 6.2 VOLET Architecture

VOLET fabricated in this study is based on top-gated design as illustrated in Figure 6.1. This configuration consisted of an indium tin oxide (ITO)/PEDOT:PSS bulk layer as a bottom drain electrode, a MEH-PPV as active an organic semiconductor and emissive layer, AgNW as source electrode, a poly(vinylidene fluoride-trifluoroethylene) (PVDF-TrFE) as dielectric layer and finally a silver (Ag) metal as a top gate electrode.



Figure 6.1: VOLETs architecture fabricated in this work.

### 6.3 Optimization of AgNW as the Source Electrode

Prior device fabrication, optimization of the AgNW has been performed. The AgNW was spin-coated on the cleaned glass substrate at three different numbers of layers. The possibility of MEH-PPV/AgNW bilayer formation has been evaluated. This has been performed by spin-coating the IPA (solvent of the AgNW) on the MEH-PPV to evaluate the etching effect of MEH-PPV by the IPA.

### 6.4 **Optical Properties of AgNW**

Figure 6.2 shows optical transmission spectra of the AgNW spin-coated at different number of layer. The spectra were obtained in a visible range from 400 to 800 nm of wavelength. It is observed that the single layer AgNW exhibit the highest transparency in all range of visible. The intensity of the transmission spectra reduces as the number of AgNW layer was increased. As the number of layers increased, the AgNW network formation becomes denser and thus, reduce an optical path through the sample. This characteristic also can be achieved by varying the concentration of AgNW (Coskun et al., 2013). The maximum transparency of the AgNW is 94% from the single layer and the lowest is 77% for the 3 layers sample, as obtained at 500 nm of wavelength.



Figure 6.2: Transmission spectra of AgNW spin-coated at the different number of layer.

Based on the VOLET structure proposed in this work, light is generated in the MEH-PPV layer. The light path of the emission in such a device is illustrated in Figure 6.3. There are three (3) most possible optical paths in this device, where the light 1) passes through the transparent drain and glass (brown arrow), 2) passes through the AgNW (indigo arrow) and 3) then reflects back to pass-through the dielectric, AgNW source, MEH-PPV, drain and come out through the glass. Thus, the AgNW need to be optically transparent in order to allow light to emit out from the second and third path, efficiently. Reflection by the AgNW is very minimum and can be ignored as AgNW exhibit an optical haze due to diffuse reflection in nature (Kim et al., 2014).



Figure 6.3: The possible optical path emission of the VOLET.

### 6.5 Electrical Properties of AgNW

Figure 6.4 shows the sheet resistant and percentage of optical transmission at 500 nm of wavelength for the AgNW thin films. The sheet resistant of AgNW films reduces when the number of the layer was increased. A similar trend is observed for the optical data where the transmission is reduced. The relationship between optical transmission and sheet resistance can be quantitatively described as:

$$T = \left[1 + \frac{1}{\Pi} \left(\frac{Z_0}{R_s}\right)^{1/(n+1)}\right]^{-2}$$
(6.1)

where the T and  $R_s$  are the transmissions and sheet resistant,  $Z_o$  is the impedance of free space (377  $\Omega$ ).  $\Pi$  is a figure of merit which describes the optoelectrical quality of a twodimension network made of percolating conductor and n is the percolation coefficient (De et al., 2010). Equation 6.1 originates from the percolation scaling law  $1/R_s \propto (N-N_c)^n$ , where N is the number of conductive rods per area unit. N<sub>c</sub> as the critical rod number required for percolation, which is also known as a threshold point. Reduction in sheet resistance is an interpretation of improvement in electrical conductivity. The conductivity of the AgNW is highly depending on the interconnection among individual nanowire. Ideally, number of AgNW induces more electrical junction, leading to higher conductivity, however, suffering poor transparency.



Figure 6.4: Sheet resistant and transmission at 500 nm of AgNW spin-coated at the different number of layer.

# 6.6 Morphological Properties of AgNW

Figure 6.5 shows the SEM images of the AgNW with the different number of layers. As previously mentioned, the conductivity depends on the interconnection among the individual nanowires. In a single layer AgNW film, the sheet resistance is so high (97.96  $\Omega$ /sq) due to poor connectivity among the wire as evident in the SEM image. Increasing the number of layer has improved the conductivity and reduces the sheet resistivity of the AgNW. As shown for 2 layers AgNW film, the formation of denser nanowire improves an overlapping nanowire network and creates a better electrical pathway for electron mobility. The 2 layers AgNW exhibit sheet resistant of 27.66  $\Omega/sq$ , which is comparable with the value of the commercially available ITO. As the number of layers increased to 3 layers, the conductivity obtained reduces down to 12.50  $\Omega/sq$ . The 3 layers AgNW show uneven nanowire network, where some part is denser than the other part. This may occur due to an irregular surface energy of the AgNW after 2 layers of deposition. However, this features does not hinder the reduction trend of the sheet resistant as the value declines almost two times from the 2 layers AgNW sample. The conductivity only depends on the connected junction among the AgNW. Thus, the uneven surface density is not the major issue in conductivity as long as the electrical pathways are well-connected (Ackermann et al., 2016).



Figure 6.5: SEM images of AgNW spin-coated at the different number of layer.

The surface profile of the AgNW layers was further investigated by analyzing surface roughness using AFM. Figure 6.6 shows three- and two-dimensional images of AFM for the different number of AgNW layers. The density of the AgNW networks was observed to increases when the number of the layer was increased, which is in the same agreement with the previous FESEM analysis. A brighter tone color of the AFM images represents a higher surface profile while the darker side is referred to lower or deeper surface profile. Thus, unlike FESEM, the AFM allows surface roughness analysis to be performed. Figure 6.7 shows the roughness profile of the AgNW samples taken from cross-section analysis at the middle of the 2-D AFM images. Here, five roughness parameters have been plotted which are Arithmetical mean deviation of the profile  $(R_a)$ , Root-mean-square deviation of the profile  $(R_a)$ , Maximum profile peak height  $(R_p)$ , Maximum profile valley depth  $(R_v)$  and ten point height of irregularities (R<sub>z</sub>). In general, the roughness of the AgWN films increased by the increase in the number of AgNW layers. The roughness was significantly increased when the 1 layer AgNW was added with another layer to become 2 layered AgNW. However, the roughness is then just increased slightly when another layer of AgNW was spin-coated to form 3 layers AgNW. For example, the value of R<sub>a</sub> and R<sub>q</sub> are increased from 9.041 and 12.095 nm to 22.075 and 26.819 nm, respectively when the second layer of AgNW was deposited. The increment in the roughness is more than 100% from the initial value. On the other hand, the increment of the value of  $R_a$  and  $R_q$  is only about 4 and 8%, respectively, when another layer of AgNW was deposited to form 3 layers AgNW sample.



Figure 6.6: AFM images of AgNW spin-coated at the different number of layer.



Figure 6.7: Roughness profile of AgNW spin-coated at the different number of layer.

## 6.7 Orthogonal Solvent Test

The solution processable VOLET in this study requires the AgNW source to be spincoated on top of the MEH-PPV organic layer. Thus, the solvent used for dispersing the AgNW must be orthogonal with that of MEH-PPV layer. On the other words, the solvent must not etch, damage or remove the MEH-PPV layer when the spin-coating process is performed. To verify this, MEH-PPV thin film was spin-coated with IPA which is the solvent for the AgNW in this work. Figure 6.8 shows absorption spectra of MEH-PPV layer before and after spin-coated with the IPA solvent. The MEH-PPV exhibits a broad absorption peak centered at 500 nm of visible wavelength, which is attributed to  $\pi \rightarrow \pi^*$  transition (Kim et al., 2007). The absorption peak before and after IPA washing are observed perfectly overlapped on each other, indicating that the IPA does not wash out the MEH-PPV layer. This result is expected because IPA is a polar protic solvent and thus not capable to dissolve high molecular weight MEH-PPV polymer.

In this work, the 2 layered AgNW thin film has been chosen as the source electrode for the VOLET due to good optical transparency, reasonably low sheet resistant and acceptable surface morphology.



Figure 6.8: Absorption spectra of MEH-PPV before and after IPA spin-coated.

# 6.8 VOLET Fabrication

The PEDOT:PSS was spin-coated on top of the ITO substrate with a spin speed of 3000 rpm within 40 s to form 40 nm thick layer. The substrate was then baked at 120 °C for 30 mins to remove residual water. The MEH-PPV was prior dissolved in toluene solvent to obtain 0.4 wt. % of solution concentration. The solution was then spin-coated on top of PEDOT:PSS layer with two steps spin speed of 800 followed by 1000 rpm within 40 and 20 s, respectively to form a 47 nm thick film layer. The sample was baked on a hot plate at 100 °C for 15 mins to fully evaporate the toluene solvent. The AgNWs dispersion was then spin-coated onto the MEH-PPV layer at 1000 rpm for 40 s and baked at 100 °C for 15 mins to remove residual solvent and to improve conductivity. This process is repeated to form the optimized 2 layered AgNW thin film. The PVDF-TrFE was dissolved in dimethylformamide (DMF) solvent with a concentration of 40 mg/mL. The dielectric solution was spin-coated onto the AgNW source layer to obtain ~150 nm thick film. The sample was annealed at 100 °C for 1 hour to remove the DMF

solvent and to improve contact resistant among layers. Finally, 100 nm thick of Ag was thermally evaporated as the top gate electrode.

## 6.9 Output Characteristics of VOLET

Figure 6.9(a) and (b) present output current and luminance characteristics, respectively, of the VOLET. Drain-source voltage, V<sub>ds</sub> was biased from 0 to 10 V while gate voltage, V<sub>gs</sub> was varied from 0 to -3 V. The VOLET exhibits a diode curve characteristics where the drain current, J<sub>d</sub> is increased exponentially when the V<sub>ds</sub> was increased. This characteristic was expected since channel of the VOLET is behaving as the OLED cell. The luminescence of the VOLET also observed to increase when the Vds was increased. When V<sub>ds</sub> was increased, electron and hole are injected from the source and drain electrode, respectively. The charged carriers were then transported in the MEH-PPV layer, causing the J<sub>d</sub> to increase. They were then accumulated in the emission region in the MEH-PPV layer to create a space charge. Exciton was then formed in this space charge, and recombined to release a light. This can be referred as electroluminescence process of an OLED. From Figure 6.9(a), it can be observed that knee voltage of the device is shifted to a lower voltage when the gate voltage, Vgs was biased from 0 to -3 V. On the other hand, turn on voltage also reduces as shown in Figure 6.9 (b). The current and brightness of the VOLET also increase significantly after negative V<sub>gs</sub> was applied. At V<sub>gs</sub>=0 V, value of maximum current and luminance are 600 mA/cm<sup>2</sup> and 19 cd/m<sup>2</sup>, respectively. When  $V_{gs}$ = -3 V, the maximum value are increases up to  $1200 \text{ mA/cm}^2$  and 50 cd/m<sup>2</sup>. These modulations of the current density and luminance are known as transistor effects.



Figure 6.9: Output (a) current and (b) luminance of the VOLET.

The transistor effect in such device is related to the reduction of injection barrier by negative  $V_{gs}$ . In order to evaluate this hypothesis, a Fowler-Nordheim (F-N) analysis was performed as shown in Figure 6.10. From this Figure 6.10, the injection barrier observed reduces when the  $V_{gs}$  was negatively biased, which is in the same agreement with the initial hypothesis. When the  $V_{gs}$ =0V, the device act as the ordinary VOLET

device. However, when the  $V_{gs}$  was negatively biased, the electrons from MEH-PPV accumulate at the MEH-PPV/AgNW source interface, which consequently has cause the injection barrier to decrease at the interface. This has induced a strong band bending in the MEH-PPV layer near the AgNW source porous region. The Schottky barrier width in the vicinity of the PVDF-TrFE/MEH-PPV interface becomes significantly narrow, facilitating electron injection from the AgNW source to the MEH-PPV layer.



Figure 6.10: FN plot of the VOLET.

### 6.10 Determination of VOLET Mobility

By using similar approach as mentioned in previous Chapter 5, mobility of VOLET was determined. Figure 6.11(a) shows the fitted SCLC plot in a log scale of drain current at different gate voltage. As the SCLC model shows a square relationship of voltage with respect to current, a plot of the square root of drain current is also presented in Figure 6.11(b). It is observed that the calculated values of drain current from SCLC model are perfectly fitted to the experimental data. From the fitting, the threshold voltage,  $V_{th}$ , and mobility,  $\mu$  of the VOLET are obtained. The carrier mobility of the device obtained from this method are within range of 4.1 to  $4.5 \times 10^{-7}$  cm<sup>2</sup>/V.s,

which is lowered than the reported value of hole for MEH-PPV based transistor (Amorim et al., 2012). The low mobility carrier is probably due to a carrier trapping process by traps that were created during device fabrication (Antoniadis et al., 1994). Both values decreased when  $V_{gs}$  was biased from positive to the negative value as shown in Figure 6.11(c). The decreased in  $V_{th}$  can be attributed to the reduction in the injection of barrier height.



Figure 6.11: (a)  $J_d$  and (b)  $J_d^{0.5}$  plots fitted with SCLC model and (c) plot of  $V_{th}$  and  $\mu$  at different  $V_{gs}$ .

#### 6.11 Transfer Characteristics of VOLET

Figure 6.12 presents output current and luminance characteristics of the VOLET. The  $V_{gs}$  was biased from 0 to -5 V at  $V_{ds}$  fixed at 5 and 10 V. It is found that the current density and luminance intensity of the VOLET are linearly increased when the  $V_{gs}$  was biased from 0 to -3 V, before being saturated at higher negative  $V_{gs}$ . As mentioned earlier, the injection barrier is reduced when the  $V_{gs}$  was biased from 0 to -3 V. As the injection barrier reduces, the charge carrier is allowed to flow when there is potential different at  $V_{ds}$ , rendering the current density and luminance intensity to increase. Above -3 V of  $V_{gs}$ , the injection barrier is nearly zero, thus current flow at its maximum value for the specific  $V_{ds}$ , where the 'saturation' occurred. The luminance intensity is also constant at this stage as the current density was saturated. In ordinary planar OFETs, the saturation is usually observed at the output characteristic due to a creation of depletion region that induces a pinch-off phenomenon. However, the saturation of VOLET which occur in transfer characteristic is mainly due to reduction in injection barrier. The on/off ratio of this device is 5.36, which is almost similar as the previously reported in Chapter 5.



Figure 6.12: Output current and luminance properties of the VOLET.

### 6.12 Electroluminescence Properties of VOLET

Electroluminescence (EL) spectra of the VOLET and photoluminescence (PL) spectrum of the MEH-PPV thin film were presented in Figure 6.13. The EL was taken by varying the  $V_{gs}$  from 0 to -5 V, at a constant  $V_{ds}$ =10 V. The EL peak of the VOLET is centered at 576 nm, attributed to a yellowish-orange emission as evident in the photographic picture in the insert Figure 6.13. The EL intensity increased when the  $V_{gs}$  was biased with the negative voltage, which is in agreement with the output characteristics of the VOLET. The PL was taken by exciting the MEH-PPV thin film at 480 nm. The PL peak is centered at 605 nm, indicating an orange emission was emitted from the MEH-PPV thin film. The shift in value between EL and PL was reported due to the micro-cavity effects in which produces a strong emission zone near the PEDOT/emissive layer interface (Aydemir et al., 2016). It is known that MEH-PPV is a hole transport semiconducting material which has a strong hole trapping property that would trap a large population of holes near the PEDOT/MEH-PPV interface where the majority of excitons are formed.



Figure 6.13: EL and PL spectra of VOLET and MEH-PPV thin film. Insert are pixel image of the VOLET at  $V_{ds}$  =10 V,  $V_{gs}$ =0 and -5V.

### 6.13 Comparison Between Physical- and Solution-Processed VOLETs

The output performances of the solution processed AgNW-sourced VOLET (labelled as AgNW-VOLET) were further evaluated by comparing with that of thermal evaporated Ag-sourced VOLET (labelled as Ag-VOLET) which was presented in the previous Chapter 5. Figure 6.14 shows the output current, luminance, efficiencies of both VOLETs at V<sub>gs</sub>=-3V. It is observed that the Ag-VOLET exhibit more than 20 times higher current density as compared to that of the AgNW-VOLET. This was expected due to the high conductivity of thermally evaporated Ag compared to spincoated AgNW as the source electrode, which significantly lower the contact resistance between the source electrode and the MEH-PPV layer (Bae et al., 2007; Woo et al., 2014). The measured sheet resistivity for Ag and AgNW are 0.28 and 27.66  $\Omega/sq$ , respectively. However, it is found that the luminance of Ag-VOLET is not really significant high (only 1.5 times higher) as compared to that of AgNW-VOLET as shown in Figure 6.14(b). This results then significantly affect the value of current and luminance efficiencies (see Figure 6.14(c) and (d)), where the AgNW-VOLET performed 10 times efficient as compared to the Ag-VOLET. This indicates that exciton formation is higher for the AgNW-VOLET than that of Ag-VOLET. The work function of AgNW and Ag are 4.1 eV (Woo et al., 2014) and 4.4 eV (De Boer et al., 2005), respectively. Thus, the rate of electron injection is higher for the AgNW-VOLET since the electron injection barrier is less as compared to that of the Ag-VOLET. Since MEH-PPV is known as hole transport materials, the high injection of electron may increase the formation of exciton, which subsequently increase the efficiencies of the device.



**Figure 6.14:** Comparison of output (a) current, (b) luminance, (c) current efficiency and (d) power efficiency between AgNW and Ag sourced VOLET.

# 6.14 Conclusions

MEH-PPV based VOLETs with AgNW source electrode have been fabricated by the spin-coating technique. The 2 layer AgNW is the optimum thin film to form source electrode due to reasonably high optical transparency, low resistivity, and better surface morphology. A high molecular weight of MEH-PPV and the used of IPA as the solvent for AgNW has made possible the formation of heterostructure of MEH-PPV/AgNW by using spin-coating method. The current and emission brightness of the VOLETs were easily modulated by a small bias at a gate electrode (e.g.  $V_{gs}$ =-1V). This modulation was explained by FN model due to the reduction of the injection barrier. The maximum current and luminance obtained are ~1200 mA/cm<sup>2</sup> and ~50 cd/cm<sup>2</sup>, respectively, at
$V_{ds}$ =10 V,  $V_{gs}$ = -3 V. The mobility of the VOLET obtained by using SCLC method is in the magnitude of 10<sup>-7</sup> cm<sup>2</sup>/V.s. The saturation region was observed in the current and luminance transfer characteristics. The VOLET produces a yellowish-orange light emission as evident by the EL spectra. The efficiency of the AgNW-VOLET is 10 times higher as compared to that of the Ag-VOLET, which can be attributed to the high exciton formation. The overall device performance is not fully optimized yet. It is suggested that other high luminance polymer with high molecular weight and resist to IPA solvent can be used to replace MEH-PPV for better device performance in the future.

# CHAPTER 7: VOLETS WITH SOLUTION PROCESSABLE SILVER NANOWIRE GATE

# 7.1 Introduction

It is understood that the simplest VOLET design is based on static induction transistor (SIT) architecture. However, the SIT-based VOLET that was fabricated in Chapter 4 suffered the secondary light emission. Another type of SIT-based VOLET is designed with the formation of gate electrode at an overlapped area between source and drain electrode (Yang et al., 2009). This gate electrode is typically made from a patterned metal (Kudo, 2005) or an ultra-thin metal (Ma & Yang, 2004), which use vacuum technique such as thermal evaporation technique. In the process, the organic semiconductor layers were also fabricated using similar method. In this chapter, a novel and simple approach to fabricate the SIT-based VOLET was introduced. In this work, silver nanowire (AgNW) was used as the gate electrode. AgNW is a well-known material with high optical transparency and low electrical resistivity (Chen et al., 2017; Duan et al., 2015; Lee et al., 2013; Liang et al., 2016; Tokuno et al., 2011; Wu et al., 2016) which is a suitable candidate to be used as electrode in organic optoelectronic devices such as organic light-emitting diode (OLED) (Xu et al., 2017) and organic photovoltaic (OPV) (Maisch et al., 2016; Song et al., 2013). AgNW also exhibits a high porosity in nature (Yang et al., 2015) which is very important for the gate electrode to allow charge carriers passing through the gate electrode in the VOLET device. Unlike the VOLET in Chapter 6, the AgNW is not served as the source electrode, but was formed as gate electrode. This VOLET has a simple layered structure of ITO (drain)/ PEDOT:PSS/MEH-PPV/AgNW(gate)/MEH-PPV/A1 (source). This chapter evaluates the properties of the AgNW prior to investigation of the MEH-PPV based VOLET device performance. The implementation of simple solution processing technique for this device shows a great promise in the low-cost display manufacturing in the future.

#### 7.2 VOLET Fabrication

The PEDOT:PSS was spin-coated on top of the ITO substrate with a spin speed of 3000 rpm within 40 s to form 40 nm thick layer. The substrate was then baked at 120 °C for 30 mins to remove residual water. The MEH-PPV was prior dissolved in toluene solvent to obtain 0.4 wt. % of solution concentration. The solution was spin-coated on top of PEDOT:PSS layer with two steps spin speed of 800 followed by 1000 rpm within 40 and 20 s, respectively. The sample was baked on a hot plate at 100 °C for 15 mins to fully evaporate the toluene solvent. Another two layers of MEH-PPV was spin-coated to form a 90 nm thick film layer. The AgNWs dispersion was then spin-coated onto the MEH-PPV layer at 1000 rpm in 40 s and bake at 100 °C for 15 mins to remove residual solvent and to improve conductivity. This process is repeated to form a 2 layered AgNW gate electrode. IPA is a polar and orthogonal solvent for the MEH-PPV polymer which enables this MEH-PPV/AgNW heterojunction to be separately formed. Another three MEH-PPV layers were then fabricated on top of the AgNW gate according to the previous steps, to form a 160 nm thick film layer. Finally, 100 nm thick of aluminium (Al) metal was thermally evaporated as the top source electrode. Figure 7.1 shows the architecture of the SIT-VOLET device fabricated in this work.



Figure 7.1: Schematic structure of VOLET device with AgNW source electrode.

### 7.3 Optoelectronic Properties of AgNW

Figure 7.2 shows transmission spectra of the AgNW film. The film exhibits high optical transparency with average of 80% in visible range from 400 to 800 nm. The highest transparency obtained at 550 nm of visible wavelength with 83% of transmission. High transparency gate electrode is necessary in order to gain high yield of emission from a reflected light at Al source electrode. SEM image of the AgNW is presented in the insert of Figure 7.2 It is noticed that the AgNW film exhibit porous structure which resulted from a random orientation of individual nanowires. This morphology features enable the charge carrier in the organic layer flow across the gate electrode during device operation. From four-point probe measurement, the sheet resistance,  $R_s$ , of the AgNW is about 27  $\Omega$ /sq, which is favorable to form the static effect in such device.



**Figure 7.2:** Transmission spectra of AgNW film. Insert is the SEM image of AgNW with the value of sheet resistance.

#### 7.4 Output Characteristics of VOLET

Figure 7.3(a) and (b) show the output current and luminance characteristics, of the SIT device, respectively. Under drain voltage,  $V_{ds}$  of 0 to 10 V, drain current density,  $J_d$  and the luminescence, L, are controlled by the gate voltage,  $V_{gs}$ . When  $V_{gs}=0$ , the SIT device acts as ordinary OLED device, in which the  $J_d$  and L totally depend on the  $V_{ds}$  across the organic emissive layer. This result has proven that the charge carriers are transported across the AgNW gate through the porous region. With appropriate  $V_{ds}$ , electron and hole are injected from source and drain electrodes, respectively, into the MEH-PPV layer. They were then accumulated and form excitons. When the  $V_{gs}>0$  V, holes are injected from the AgNW gate which causes potential barrier at source interface increases. This increased potential barrier hinder the electrons transporting from the source to the drain and result in the decreased J<sub>d</sub> and L. On the other hand

when  $V_{gs}$ <0 V, the electrons are injected from the AgWN gate and reduce the potential barrier which allows a higher flow of electron and increases the light brightness significantly.



Figure 7.3: Output (a) current and (b) luminance characteristics of the VOLET.

### 7.5 Device Mechanism of the VOLET.

The basic mechanism of the VOLET can be explained by the schematic energy band diagram as shown in Figure 7.4(a) and (b). Without any bias at  $V_{gs}$  (off-state), the MEH-PPV makes the Schottky contact with the Al source and the AgNW gate. When the AgNW was negatively biased, electron is injected and accumulated at the MEH-PPV/AgNW/MEH-PPV interface. This electron alters the energy band and narrows the Schottky barrier at the interface. Reduction of the Schottky barrier will facilitate more electron to travel from the Al source into the MEH-PPV layer through the porous region of the AgNW gate. Thus, current density of the device increases accordingly. This electron accumulates with the injected hole from the drain to form exciton which, finally recombine to release light emission.



Figure 7.4: Schematic energy band diagram of the VOLET at (a) off-state and (b) on-state.

Figure 7.5 shows the Fowler-Nordheim plot of the VOLET at different  $V_{gs}$ . It was found that the slope of the plot are almost the same, only the magnitude increases when negative  $V_{gs}$  was applied. This result indicates that the potential barrier of hole at ITO/PEDOT:PSS drain/MEH-PPV interface does not change so much (from 0.11 to 0.10 eV) by the  $V_{gs}$  from +2 to -2 V. The significant change may only occur at the MEH-PPV/AgNW gate/MEH-PPV, which the energy diagram of the MEH-PPV is bended to facilitate charge carrier transportation in the device when the negative voltage was applied on the gate electrode. The turn-on voltage for this device is around 6 V, which is slightly higher as compared to that of the previously reported at around 4 V, for the Schottky barrier (SB) based VOLET. It is suggested that a thicker emissive layer in this device (160 nm) as compared to in the previous one (47 nm), result in a high turn-on voltage (Yap et al., 2008).



Figure 7.5: FN plot at different Vgs.

Carrier mobility of the device was also calculated by the space charge limited current (SCLC) technique reported in previous Chapter 5 and 6. Figure 7.6(a) and (b) show the fitted SCLC plot of drain current in log and square root scales, respectively. From the fitting, the threshold voltage,  $V_{th}$  and mobility,  $\mu$  of the VOLET are obtained. The  $V_{th}$  value obtained reduces from 5.3 to 4.4 V when the  $V_{gs}$  was biased from +2 to -2 V. However, the carrier mobility of the device remained at the value of  $1.6 \times 10^{-5}$  cm<sup>2</sup>/V.s, which are within the range of reported value of hole mobility for MEH-PPV based planar transistor (Amorim et al., 2012). This result is differ with the previous reported in Chapter 5 and 6, where there is a slight reduction of hole mobility when the  $V_{gs}$  is negatively increased. However, this result is expected since the potential barrier of hole

is almost unchanged with respect to the change of  $V_{gs}$ , as verified by FN plot in previous Figure 7.5.



Figure 7.6: Experimental and fitted data of drain current in (a) log scale and (b) square root form at different  $V_{gs}$ .

#### 7.6 Transfer Characteristics of VOLET

Transfer current and luminance characteristics of the device are presented in Figure 7.7(a) and (b). The transfer characteristics are referred as a respond of J<sub>d</sub> and L with the swept of  $V_{gs}$  from -10 to 0 V, at various  $V_{ds}$  from 0 to 5 V. The negative range of  $V_{gs}$  is selected in this study because it results in the increment of J<sub>d</sub> and L in the previous output characteristics, which is very interesting to focus on. It is found that the J<sub>d</sub> and L increased when the  $V_{ds}$  is increased. On the other hand, the value of J<sub>d</sub> and L are exponentially reduced when  $V_{gs}$  was increased from -10 to 0 V. It is worthy to mention that the selected range of  $V_{ds}$  is the region where the value of J<sub>d</sub> and L were the lowest in the previous Figure 7.3. This is also known as an ohmic region where normally the light will not be emitted at this region in the ordinary OLED since there is no exciton formation at this stage. This current result indicates that with significant low  $V_{gs}$  ( $V_{gs}$ <<0 V), the potential barrier can be reduced very low which allow exciton to form at low  $V_{ds}$  range. The on/off ratio for this device is 6.94, which is slightly higher as compared to the previously reported VOLET in Chapter 5 and 6.



Figure 7.7: Transfer (a) current and (b) luminance characteristics of the SIT-VOLET.

The current and power efficiencies ( $\eta_c$  and  $\eta_p$ ) of the VOLET is presented in Figure 7.8. It is observed that the efficiencies of the device do not depends on the V<sub>gs</sub> which is contrary to that of Schottky barrier (SB) based VOLET as reported in Chapter 4. This indicates that the ratio of light emission over the exciton formation is almost the same for this SIT-based VOLET even at different V<sub>gs</sub> biased. Biasing negative voltage at the gate electrode not only alter the injection barrier, but also promoting more injection of hole from the drain due to the high potential different between drain and gate. Interestingly, the value of efficiencies of this device is significantly higher than that of other VOLET fabricated in this work. The value of current and power efficiencies obtained are about 0.1 cd/A and 0.03 lm/W, respectively. These efficiencies value are 50 times higher than AgNW-sourced VOLET presented in Chapter 6. It can be suggested that the thicker MEH-PPV layer in this SIT VOLET induces more exciton accumulation as compared to that of thin layers of MEH-PPV in the AgNW-sourced VOLET.



Figure 7.8: Efficiencies of the device.

Unlike organic field effect transistor, the typical SIT operation without current saturation was observed in this device. The current saturation is attributed to pinch-off phenomenon that limits the drain current at its maximum value. It is observed that the square-law characteristic was dominant in the high- and low-voltage region in output and transfer plots, respectively. This indicates the behavior of the space charge limited current (SCLC), where normally the exciton formation and radiative recombination occurs. It is reported that the dimension of porosity of the gate electrode can affect the modulation of current and luminance (Kudo, 2005). However, in this current work, the AgNW was formed in a random orientation since the spin-coating fabrication method is used. Thus, fabricating a well-oriented AgNW can be the next challenge for this device. It is suggested that this issue may be addressed by employing a capillary-assisted fluidic assembly technique (Wu et al., 2016) to form a well-aligned AgNW gate electrode. It is also important to highlight that the used of MEH-PPV as the emissive polymer is this study is only for a reference device of this solution processable AgNW-gated concept. Hence, other suitable emissive polymer that resist to IPA solvent can also be implemented by using a similar approach to produce high performance display.

### 7.7 Conclusions

The proposed solution processable VOLET with AgNW gate was fabricated and the static characteristics of the device were investigated. High transparency, surface porosity, and low resistivity of AgNW made it a suitable candidate for gate electrode in SIT of a display application. A typical SIT device operation with non-saturation  $J_d$  and L was observed in both output and transfer characteristics. In addition, the VOLET display was fabricated totally by solution processing technique, which demonstrates a great approach for low-cost display production in the future.

#### 8.1 Summary

In this thesis, several design and a step-by-step approach have been demonstrated and developed in producing the solution processed VOLET. The fabrications steps, device architecture and physical mechanisms of the VOLET were systematically described and investigated. The main findings are summarized in the following paragraphs.

Initially, a small molecule Alq<sub>3</sub> based static induction transistors VOLETs have been fabricated by using a simple solution process. A special feature about this VOLETs is the structure is simple and almost similar to the single layer OLED design. The VOLETs consists of a bulk layer of ITO and hole injection layer of PEDOT:PSS as a source, organic electroluminescent layer of Alq<sub>3</sub> and two strip of Al as drain and gate electrodes. These Al drain and gate electrodes were thermally evaporated Al through a 50 micrometers diameter of copper wire mask. The output current and luminance characteristics of the VOLETs show that the current density and light intensity depends on polarity of gate bias. It is also revealed that an initial internal electric field contributes to the charge diffusion between gate and drain channel. An inverse characteristic observed for luminance at drain-source and gate-source channels. Even though the VOLET exhibit a simple fabrication technique, it suffers low light output intensity and secondary light emitted from the gate-source channel. Thus, this device is not suitable for a practical device application.

Addressing the weakness of the VOLET demonstrated earlier, a second design of VOLET has been studied. Not only has the design been modified, materials used have also been replaced with another materials. The emissive polymer MEH-PPV has been

chosen as the active layer. The design of VOLET is based on combination of capacitor and OLED device that are connected by an ultra-thin intermediate common Al source electrode, which is also known as Schottky barrier (SB) based VOLET. The VOLET consist of ITO/PEDOT:PSS as drain electrode, MEH-PPV as emissive layer, ultra-thin Al (~20 nm), LiF as capacitor and Al top gate electrode. It is found that the negative bias on the gate electrode has induced a high current density and brighter luminescence in the VOLET output characteristics. The major factor that contributes to this transistor behavior is the special porous features of the ultra-thin Al source electrode. From SEM image, several holes were observed which is relatively bigger that the thickness of the electrode, which result in, discontinued porous structure. This feature allows energy band contact between the MEH-PPV and the gate electrode, which demonstrate the transistor modulation when gate electrode biased appropriately.

Instead of using Al as the source electrode, a Silver (Ag) metal is utilized in the subsequent VOLET fabrication. This study shows that the structure morphology of the Ag surface depends on the deposition rate. At 2 Å/s, porous structure can be formed even at thickness of Ag at about 100 nm. Using the similar architecture as in the previous VOLET, the ultra-thin Al has been replaced with a porous Ag. The VOLET exhibits a high leakage current that induces an inversion polarity of its transistor behavior. Interestingly, a well-defined saturation current observed in the linear scale of transfer characteristic. The energy band banding by the gate voltage was explained related to the reduction of potential barrier at drain and source electrodes which is supported by Fowler-Nordheim (FN) tunneling theory. The study also proposed a simple method to measure transistor mobility of VOLET, which use space charge limited current (SCLC) theory.

In order to extend the VOLET fabrication towards all-solution process technique, a silver nanowire (AgNW) and ferroelectric polymer PVDF-TrFE have been used as the source electrode and the dielectric layers. The optical, electrical and morphological properties of the AgNW formation were initially optimized, prior to VOLET fabrication. It was found that the two layers of AgNW is the optimum condition to be the source electrode due to high optical transparency, relatively low electrical resistivity and reasonably low surface roughness. A high molecular weight of MEH-PPV has an advantage in order to form a multilayer structure by solution process. Similar as the Agporous sourced VOLET, the current density and luminance intensity of the VOLET modulated by a small magnitude of gate voltage. The transistor modulation process induced by changing an injection barrier via gate voltage bias. As comparison, the efficiency of the AgNW-sourced VOLET is 10 times higher as compared to that of the Ag-VOLET, which is attributed by the high exciton formation in the AgNW-sourced VOLET.

Since the AgNW and MEH-PPV can form a heterojunction structure, a new solution processable SIT-based VOLET using AgNW as a gate electrode was fabricated. The characteristics of this device were investigated. The electroluminescence characteristics showed that the drain-source current and emission brightness were modulated by the bias voltage that applied to the AgNW gate electrode. The SIT-based VOLET operates with non-saturation property in both output and transfer characteristics. The porous structure, optically transparency and low resistivity of AgNW is a key factor in the success of the device. Furthermore, compared with the traditional devices, this concept of VOLET was fabricated by simple spin-coating technique, showing its high potential for low-cost display production in the future. In overall, this study has achieved a significant increment in term of device performances. Current and power efficiencies of the device increase 10 times higher from  $1.8 \times 10^{-4}$  cd/A and  $1.1 \times 10^{-4}$  lm/W to  $2.6 \times 10^{-3}$  cd/A and  $1.1 \times 10^{-3}$  lm/W, respectively, when the VOLET used AgNW as source electrode instead of Ag. A greater current and power efficiencies were established when the AgNW was utilized as the gate electrode in SIT-based VOLET, with the value of  $1.1 \times 10^{-1}$  cd/A and  $3.1 \times 10^{-2}$  lm/W, respectively. The on/off ratio of the devices also improves from 5.08 to 5.36 and 6.94 when the device evolved from Ag-sourced to AgNW-sourced VOLET and SIT-based AgNW-gated VOLET, respectively.

#### 8.2 Suggestion for Future Works

Based on the preliminary studies demonstrated in this thesis, there are still issues that can be addressed in the future including:

- The efficiency is not sufficient in order to meet the consumer product requirement (above 20 cd/A). The emissive materials should be replaced with other high efficiency materials, but must exhibit similar physical properties that can orthogonal with IPA solvent in order to form a multilayer structure with AgNW.
- The fabrication method is not fully solution technique yet. Thus, it would be better if the all layers in the device can be fabricated with solution technique, especially the electrodes, without compromising the performance of the devices. Moreover, it is quite difficult to form a pattern of the pixel by the spin-coating technique, which the ink-jet printing technique can be considered as the perfect solution. This also can venture into a new concept of wearable electronics when the flexible substrates are exploited.
- The stability and reliability test of the devices are important to be performed in order commercialize the final product. This can be done by evaluating the

environmental stability, effects of bias stress and influence of photo-induced on the performance of the devices.

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# LIST OF PUBLICATIONS

# **Publications related to the thesis:**

- 1. Mohd Sarjidan, M. A., Shuhaimi, A., & Abd. Majid, W. H. (2019). Solution-Processable Vertical Organic Light-Emitting Transistors (VOLETs) with Directly Deposited Silver Nanowires Intermediate Source Electrode. *Journal of Nanoscience and Nanotechnology*, 19(11), 6995-7003
- Mohd Sarjidan, M. A., Shuhaimi, A., & Majid, W. H. A. (2018). Observation of saturation transfer characteristics in solution processed vertical organic field-effect transistors (VOFETs) with high leakage current. *Current Applied Physics*, 18(11), 1415–1421.
- 3. Mohd Sarjidan, M. A., & Abd. Majid, W. H. (2018a). Electrical and luminescence properties of MEH-PPV vertical organic light-emitting transistors with an ultra-thin aluminum source electrode. *Journal of Optoelectronics and Advanced Materials*, 20(5–6), 285–289.
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### **Other publications:**

- 1. Basri, S. H., Majid, W. H. A., Talik, N. A., & **Sarjidan, M. A. M.** (2018). Tailoring electronics structure, electrical and magnetic properties of synthesized transition metal (Ni)-doped ZnO thin film. *Journal of Alloys and Compounds*, 769, 640-648.
- 2. Zaini, M. S., **Sarjidan, M. A. M.**, & Majid, W. H. A. (2016). Determination of Traps' Density of State in OLEDs from Current-Voltage Analysis. *Chinese Physics Letters*, 33(1) Article#018101.
- 3. Mohd Sarjidan, M. A., Mohd Mokhtar, H. A., & Abd. Majid, W. H. (2015). Determination of energy band diagram and charge carrier mobility of white emitting polymer from optical, electrical and impedance spectroscopy. *Journal of Luminescence*, 159, 134-138.
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- 5. Basri, S. H., **Mohd Sarjidan, M. A.**, & Abd Majid, W. H. (2014). Structural and optical properties of nickel-doped and undoped zinc oxide thin films deposited by sol-gel method. *Advanced Materials Research*, *895*, 250-253.
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- 8. Mohd Sarjidan, M. A., Basri, S. H., & Abd Majid, W. H. (2013). Fabrication and characterization of organic light-emitting diodes containing small molecules blends as emissive layer. *Advanced Materials Research*, *795*, 106-109.
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- 12. Za'Aba, N. K., **Mohd Sarjidan, M. A.**, Basri, S. H., & Abd. Majid, W. H. (2013). Electronic device characteristics and charge conduction mechanisms of single-layer organic light emitting devices based on Alq<sub>3</sub>, TPD:Alq<sub>3</sub> and TPD:PBD:Alq<sub>3</sub> blend system. *Journal of Nanoelectronics and Optoelectronics*, 8(5), 437–445.
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