ONLINE TUNING CONTROL FOR A SWITCH-SHARING-BASED MULTILEVEL INVERTER USING CAPACITOR VOLTAGE BALANCING

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KUALA LUMPUR

2022

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DISSERTATION SUBMITTED IN FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF MASTER OF PHILOSOPHY

INSTITUTE FOR ADVANCED STUDIES
UNIVERSITI MALAYA
KUALA LUMPUR

2022

UNIVERSITY OF MALAYA

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Matric No: **17050543/1 / HGF 150007**

Name of Degree: **Master**

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ONLINE TUNING CONTROL FOR A SWITCH-SHARING-BASED MULTILEVEL INVERTER USING CAPACITOR VOLTAGE BALANCING

ABSTRACT

In these modern days, energy sustainability has gained increasing attention, bringing about the reinforcement of numerous attempts to utilize renewable energy and improve energy efficiency. In relation to this, multilevel inverters, which come from a family of power electronic converters, have a great potential to play an important role in contributing to this field. One type of multilevel inverter which has the potential to perform the task is the switch-sharing-based multilevel inverter. The switch-sharing-based multilevel inverter offers several benefits, such as decreasing the complexity of a circuit, minimizing power losses and contributing to smaller filter size. However, just like diode-clamped multilevel inverter, the switch-sharing-based multilevel inverter also suffers from the unbalanced capacitor voltage issue. This phenomenon degrades the voltage waveforms for the AC-side, which results in an unfavorable operation of the inverter. Therefore, this research adopts the approach of implementing a capacitor voltage balancing circuit based on a buck-boost converter in a five-level switch-sharing-based multilevel inverter topology. For this approach, a performance-based online tuning control based on proportional-integral (PI) configuration is proposed to balance and maintain the capacitor voltages at the desired levels and improve the dynamic performance. Through MATLAB/SIMULINK simulation, a detailed analysis of the results for the buck-boost converter with the proposed online controller with performance-based tuning has been made. For validation purposes, the buck-boost converter has been constructed in the laboratory, and the controller has been implemented on a digital signal processor (DSP). The test conducted with an experimental five-level switch-sharing-based multilevel inverter reveals that satisfactory results have been

achieved. Simulation and experimental results reveal that the capacitor voltages can be balanced at high modulation indexes with improved current harmonic performance able to be acquired at the inverter's output.

Keywords: Buck-boost converter, capacitor voltage balancing, online-tuning, Switch-Sharing-Based-Multilevel-Inverter.

ABSTRAK

Pada masa kini, kemampanan tenaga telah menarik perhatian sehingga membawa kepada pelbagai usaha untuk menggunakan tenaga yang boleh diperbaharui dan menambah baik kecekapan tenaga. Dalam hal ini, penyongsang bertingkat yang berasal dari penukar kuasa elektronik, mempunyai potensi yang besar dalam memainkan peranan penting dalam bidang kemampanan tenaga ini. Salah satu penyongsang bertingkat itu adalah penyongsang bertingkat berdasarkan perkongsian suis. Kelebihan penyongsang bertingkat ini adalah seperti mengurangkan kerumitan litar, mengurangkan kehilangan kuasa dan menawarkan saiz penapis yang lebih kecil. Walaubagaimanapun, penyongsang bertingkat berdasarkan perkongsian suis ini juga mengalami masalah voltan kapasitor yang tidak seimbang. Fenomena ini akan merendahkan kualiti gelombang voltan di sisi AC hingga menyebabkan penyongsang bertingkat tidak dapat beroperasi dengan baik. Oleh itu, penyelidikan ini menggunakan pendekatan pelaksanaan litar pengimbang voltan kapasitor yang berdasarkan penukar buck-boost untuk lima aras penyongsang bertingkat yang berdasarkan perkongsian suis. Bagi pendekatan ini, kawalan penalaan online berasaskan prestasi yang bersandarkan konfigurasi berkadar kamiran dicadangkan untuk mengimbangi and mengekalkan voltan kapasitor pada tahap yang dikehendaki serta untuk meningkatkan prestasi dinamik. Melalui simulasi MATLAB/SIMULINK, analisis terperinci dibuat keatas penukar dan pengawal online berasaskan prestasi yang dicadangkan. Pengesahan lanjut telah dijalankan dengan membina prototaip makmal dan pengawal telah dilaksanakan pada pemproses isyarat digital (DSP). Ujian makmal mengesahkan bahawa keputusan yang memuaskan telah dicapai. Keputusan simulasi dan eksperimen menunjukkan voltan kapasitor yang boleh seimbang pada modulasi yang tinggi berserta prestasi arus harmonik (THD) yang bertambahbaik di output penyongsang.

ACKNOWLEDGEMENTS

Alhamdulillah. Praise be to Allah the Almighty, with His will, I am able to complete my thesis for my Master's degree. First and foremost, I would like to express my gratitude to my supervisor, **Ts**. **Dr. Jafferi Jamaludin** for his continuous support and assistance towards the development and completion of my MPhil thesis. It is a norm to have plenty of blank moments in research field hence, his valuable experience as a researcher along with friendly approach helped me a lot to be consistent until I have successfully reached this far. Next, my deepest appreciation goes to **Prof. Ir. Dr. Nasrudin Bin Abd Rahim** for his endless motivation throughout my thesis work.

Not to forget, many thanks to my friends and fellow researchers from my laboratory and UMPEDAC members, Hasanah, Radin, Ahmad Rivai, Nur Athirah and Farhana for their all-time positivity and support. I shall take this opportunity to express my appreciation to UMPEDAC for the research funding and thanks to that, my research has advanced to this stage without any financial problem.

I would also like to express my gratitude to all UMPEDAC staff for directly or indirectly assist me to complete my research works. I am grateful and it is a privilege to experience as a Master's student in University of Malaya.

My sincere thanks to my family members especially my husband, mother and daughters for their endless prayers, understanding and moral support. Last but not least, thank you to everyone who has played a part towards completing my research work and thesis.

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LIST OF SYMBOLS

C_1 - C_4	:	Capacitor
D_1 - D_4	:	Diode
$e_1(t)$,$e_2(t)$	:	Voltage Error
HB	:	Hysteresis Band
i_1 - i_5	:	Circulating Current
$I_{chlimit}$	:	Current Limit
I_A	:	Output Current at Phase A
F_1 - F_5	:	Fuse
K_{iU}	:	Integral Gain for the Upper Part of Converter (Proposed PI Control)
K_{iL}	:	Integral Gain for the Lower Part of Converter (Proposed PI Control)
K_{pU}	:	Proportional Gain for the Upper Part of Converter (Proposed PI Controller
$K_{pU,max}$	:	Maximum Limit of Proportional Gain for the Upper Part of Converter (Proposed PI Converter)
$K_{pU,min}$	:	Minimum Limit of Proportional Gain for the Upper Part of Converter (Proposed PI Controller)
$K_{pU,prev}$	:	Previous Value of Proportional Gain for the Upper Part of Converter (Proposed PI Controller)
K_{pL}	:	Proportional Gain for the Lower Part of Converter (Proposed PI Controller)
$K_{pL,max}$	:	Maximum Limit of Proportional Gain for the Lower Part of Converter (Proposed PI Controller)
$K_{pL,min}$	:	Minimum Limit of Proportional Gain for the Lower Part of Converter

		(Proposed PI Controller)
$K_{pL,prev}$	:	Previous Value of Proportional Gain for the Lower Part of Converter (Proposed PI Controller)
L_1 - L_2	:	Inductor of Buck-Boost Converter
m_a	:	Modulation Index
S_1 – S_4	:	Switches
T	:	Time
V_{c1} - V_{c4}	:	Capacitor Voltage
V_{AB}	:	Line-to-Line Voltage waveform
V_{AN}	:	Inverter Phase Voltage
V_{dc}	:	Input Voltage
$V_{dc,prev}$	:	Previous Value of Input Voltage
V_{ref}	:	Reference Voltage
$y_1(t)$-$y_2(t)$	:	PI Controller Output

LIST OF ABBREVIATIONS

PV	:	Photovoltaics
DC	:	Direct Current
DSP	:	Digital Signal Processor
PWM	:	Pulse Signal Modulation
MATLAB	:	Matrix Laboratory
AC	:	Alternating Current
ADC	:	Analog-to-Digital Conversion
DCMI	:	Diode Clamped Multilevel Inverter
EMI	:	Electromagnetic Interference
IGBT	:	Insulated Gate Bipolar Transistors
GPIO	:	General-Purpose Input/Output
HVDC	:	High Voltage Direct Current
PI	:	Proportional-Integral
RC	:	Resistance-Capacitance
RSCC	:	Resonant Switched Capacitor Converter
STATCOM	:	Static Compensator
SVM	:	Space-Vector-Modulation
THD	:	Total Harmonic Distortion
VBC	:	Voltage Balance Circuit

CHAPTER 1: INTRODUCTION

1.1 Introduction

This chapter explains the main idea and overview of the project in this thesis. The importance of energy sustainability is presented, along with the reasons which lead to this project. It is then followed by the objectives and methodology of the research work. Lastly, summary for this chapter is presented.

1.2 Study Motivation

The global energy demand is increasing rapidly and this is a worldwide worrisome issue to meet future demands. Currently, conventional energy sources such as fossil fuels and natural gas are widely utilized and have been the primary choice for ages. However, despite being affordable and efficient with a large amount of energy produced per unit weight, conventional energy sources are getting depleted over time. These energy sources are non-renewable and cannot comply with the increasing energy demand, leading to a serious problem in the future. Furthermore, these conventional energy sources release greenhouse gasses that affect the environment, causing climate change and global warming (Ünal, Ercan, & Kayakutlu, 2015; Islam, Hasanuzzaman, Rahim, Nahar, & Hosenuzzaman, 2014). With the environmental issue, through the implementation of the Eleventh Malaysia Plan 2016 – 2020, Malaysia has supported the green growth, which was outlined as a development and advancement of socio-economic conditions, promoting the quality of life to be in harmony with environmental and natural resources sustainability (People, 2020). Numerous strategies have been explored to support green growth, and one of them is by increasing renewable resources shares in the energy mix (People, 2020). It is found that only 1% (243.4W) of the total generation capacity in Peninsular Malaysia and Sabah was from renewable energy sources in 2014, and 66% of the contributed renewable energy was from solar photovoltaics (PV) (Goals, 2017). Every

solar PV system contains an inverter that converts DC power generation from the PV modules into AC power. From the literature review, it is revealed that an inverter helps to achieve high efficiency of a system with reduced power loss.

A multilevel inverter is one inverters that can achieve high output quality and very efficient (Siva et al., 2011). Among many topologies of multilevel inverter circuits, the cascaded H-bridge and diode-clamped topologies have gained better attention in PV systems (Song, Kang, & Park, 2009; Boora, Nami, Zare, Ghosh, & Blaabjerg, 2010; Sarebanzadeh et al., 2021; Qanbari & Tousi, 2021). Several PV systems issues are to be addressed based on the previous research on DC voltage balancing solutions for these two topologies. The power imbalance is one of the hurdles in the cascaded H-bridge multilevel inverters. This occurs as every H-bridge cell contains different maximum power that is extracted from the PV modules leading to an unbalanced current injected into the grid. Hence, to respond to this issue, a two-pronged feedforward compensation method that implements a DC voltage balancing scheme was introduced (Cheng et al., 2006). A modulation compensation scheme is another method to address the same issue by making use of a zero-sequence voltage (Raj et al., 2018). This scheme produces a balanced injected current by ensuring the unbalanced phase output voltages of the inverter based on the degree proportional to their respective unbalanced phase powers. In another method (Song et al., 2009), a model predictive control was employed in controlling the DC link voltages for the H-bridge cells.

In diode-clamped multilevel inverters, the DC voltage balancing solution contributes to increased the amount of power transferred. Busquets-Monge et al (Busquets-Monge et al., 2008) suggests an investigation on a three-phase four-level diode-clamped inverter whereby the adopted control scheme consists of an unbalanced control block and a total DC link voltage control block which ensure that every PV

module voltage is at the maximum power point independently without degrading the output quality. Tian et al. (Tian et al., 2015) studied the function of a three-phase three-level neutral-point-clamped inverter for grid-connected application based on a multivariable linear quadratic regulator control scheme. This type of control scheme manages to supply a DC link neutral-point voltage balance and regulates the DC link voltage for the highest power transfer at almost unity power factor.

Jamaludin et al (Jamaludin et al., 2015) show that switch-sharing-based multilevel inverter can give out outputs as good as the cascaded H-bridge and diode-clamped inverters along with other attractive benefits including improved efficiency and smaller filter size. Therefore, overcoming the existing shortcoming is crucial as it can be the root of the possibility for the DC voltage to be not equally divided, leading to an unbalanced voltage problem. However, there are two different methods to solve this issue. The first one implements the modification of the switching pattern to consider voltage balancing criterion, and this can avoid the use of additional circuits to maintain the implementation cost (Choi & Saeedifard, 2011; Lai, Chou, & Pai, 2007; Hotait, Massoud, Finney, & Williams, 2007; Narimani et al., 2013; Grigoletto & Pinheiro, 2009). Nevertheless, this increases the control complexity, and at some points, it reduces the magnitude of the output voltage. The second method uses auxiliary circuits to divide the total DC voltage to balance across the voltage each capacitor used (Akagi, Fujita, Yonetani, & Kondo, 2008; Mishra, Joshi, & Ghosh, 2001). Despite the need for additional components, the performance of voltage balancing is better without any degrading effects on the inverter's output.

This work studies on auxiliary circuit method to explore the best solution in solving the voltage balancing issue for a switch-sharing-based multilevel inverters. A laboratory prototype has been made, and it has been tested with a digital signal processor

(DSP) which is used for implementing the PWM and control algorithm. To assess the impact of the capacitor voltage balancing on the inverter's output, a careful analysis from the simulation and experimental results has been carried out.

1.3 Research Objectives

The study's main objective is to develop a suitable voltage balancing scheme for the switch-sharing-based multilevel inverter. To achieve the main objective, it is necessary,

1. To investigate the different types of voltage balancing strategies for multilevel inverters.
2. To propose and enhance a suitable voltage balancing strategy for the switch-sharing-based multilevel inverter by considering variable DC inputs.
3. To analyze the proposed controller with the suggested online tuning mechanism using MATLAB/Simulink simulation.
4. To conduct hardware implementation of the proposed voltage balancing circuit based on buck-boost converter for the switch-sharing-based multilevel inverter.

1.4 Research Methodology

The research is conducted based on the methodology as shown in Figure 1.1 and the explanation for each step. This work highlights the strategy to respond to the DC voltage balancing issue, which becomes the subject of this thesis. There are three stages of the investigation. The first one is the design stage according to the theoretical analysis. This stage includes the literature review, configuration design of the inverter with DC voltage balancing solution, preliminary analysis of the operational principles and the analysis of the control scheme. The second stage involves verification by computer simulation with the utilization of MATLAB/Simulink software tools. This simulation is

to study the effectiveness of the voltage balancing solution. The third stage, or known as the validation stage, is the practical experimentation in the laboratory. This involves constructing of the experimental buck-boost converter whereby the DSP controller is used to execute the algorithms for voltage balancing solution and control. The experiments are carried out in steady state and transient response conditions. The data recorded are analyzed in detail, and suitable modification is made to achieve the target performance.

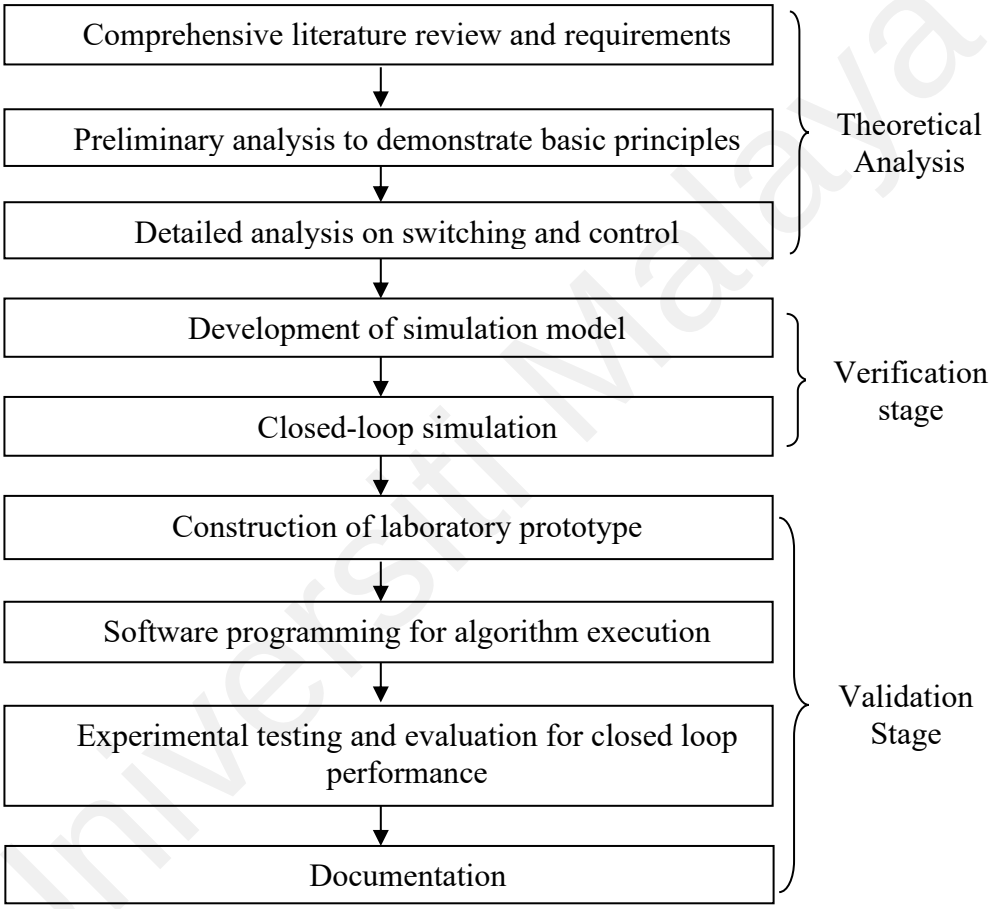


Figure 1.1: Research methodology.

1.5 Chapter Overview

The thesis consists of six chapters, and the description of each chapter is given as follows.

Chapter two presents the literature review of the chosen inverter and existing methods used to balance the capacitor voltages in the classical multilevel inverter. The

chapter ends by discussing the existing controllers used for the capacitor voltage balancing solution in the inverter.

Chapter three presents the capacitor voltage balancing method based on the buck-boost converter. The analysis and operational principle of the converter are explained. Finally, the proposed PI controller with the performance-based online tuning mechanism controller is discussed.

Chapter four explains the simulation studies by using MATLAB/SIMULINK software. Firstly, step responses are investigated in the simulation study due to a change in the input voltage. Secondly, the analysis of power loss and efficiency among switches are conducted. Some comparative analysis between the conventional PI controller and the proposed PI controller with the online tuning mechanism is also included. The results of power loss and efficiency have been analyzed for both controllers.

Chapter five presents the important features for hardware implementation of the capacitor voltage balancing circuit. The development of the laboratory prototype of the circuit for the five-level switch-sharing-based multilevel inverter is explained. Related results from the experiment are presented along with their analysis.

Chapter six is the conclusion that summarizes the overall study, which is explained in previous chapters, together with some suggestions and recommendations.

1.6 Summary

The global energy demand is increasing at a fast pace, and this has posed a great challenge to meet the future demands, which have led to the progress in renewable energy technologies. With this, multilevel inverters, which come from a family of power electronic converters, have great potential to play an important role in contributing to this

progress. Nonetheless, these inverters have a major setback whereby there is a potential unbalanced capacitor voltage issue at their DC-link that affects the output of the inverters. Therefore, this work presents the work conducted to solve the unbalanced capacitor voltage issue in one type of multilevel inverters known as the switch-sharing-based multilevel inverter.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

This chapter is focused on reviews of capacitor voltage balancing strategies and then control mechanisms. At the beginning of this chapter, a brief overview of switch-sharing-based multilevel inverter is presented, followed by a discussion of the methods for capacitor voltage balancing namely PWM modifications and balancing circuit implementation. In addition, controller algorithms, which are commonly used in the capacitor voltage balancing scheme, are also given.

2.2 Switch-Sharing-Based Multilevel Inverter

The inverter is a device that converts DC power into AC form. A type of inverter that has taken the interest of many researchers is the multilevel inverter. It can generate voltage waveforms with many voltage levels. Thus, the waveforms are closer to a pure sinusoid compared with those of the two-level inverter. Diode-clamped multilevel inverters (DCMI) (Nabae, Takahashi, & Akagi, 1981; Pou, Pindado, & Boroyevich, 2005), cascaded multilevel inverters (Song et al., 2009; Zhang, 2021), and flying capacitor multilevel inverter (Song et al., 2009; Fard et al., 2020) are the three well-known classical multilevel inverters. The static compensators (STATCOM) (Shu, Ding, et al., 2013; Neyshabouri et al., 2020), variable-speed motor drives (R et al., 2018; Okazaki et al., 2017) and unified power flow controllers (R et al., 2018) are examples of medium-voltage and high-power applications using multilevel inverters. The multilevel inverter offers great advantages in comparison with the two-level inverter such as low electromagnetic interference (EMI), low total harmonic distortion (THD), low switching loss, and high quality of waveforms (Yuan & Barbi, 2000; Cheng et al., 2006; Marchesoni & Tenca, 2002). Despite their advantages, classical inverter suffers from disadvantages that reduce the inverter's reliability and efficiency. This happens when the number of

levels increases as the circuit of the inverter becomes complex. Moreover, the cost to buy circuit components used in the inverter also increases as the number of levels increases.

These three classical multilevel inverters become the benchmarks for the new topologies. One of them is the switch-sharing-based multilevel inverter. This inverter can perform almost the same as the diode-clamped inverter along with some other benefits such as reduced power losses and reduced circuit complexity and a smaller filter size compared to the diode-clamped counterpart (Ping et al., 2013). Basically, the inverter creates a hybrid type that combines both advantages of the two-level full-bridge inverter and the diode-clamped inverter. With these benefits, the inverter can be utilized in full capacity for low-power applications. One advantage that it has over the diode-clamped inverter is enhancing the output quality without a very high switching frequency usage. The circuit topology of the three-phase five-level switch-sharing-based inverter is presented in Figure 2.1 (Jamaludin et al., 2015).

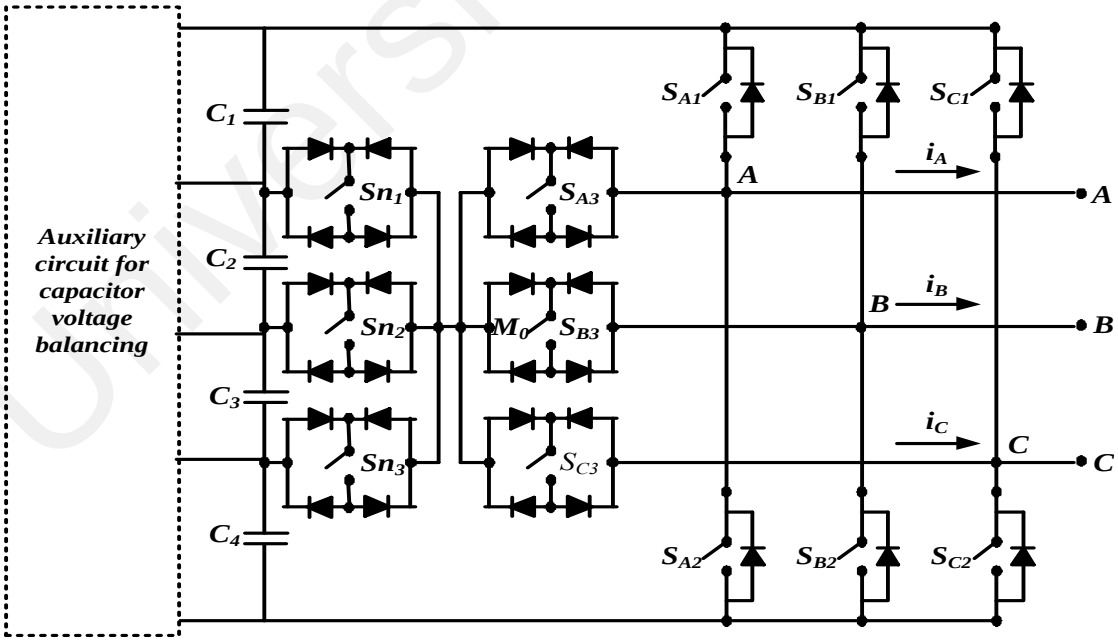


Figure 2.1: Five-level switch-sharing-based multilevel inverter (Jamaludin et al., 2015).

To overcome the circuit's complexity, the switch-sharing-based inverter uses more power diodes instead of using power switches. There are 12 power switches, including six bidirectional switches which are connected to four DC-link capacitors, namely C_1, C_2, C_3 and C_4. For the optimization of bidirectional switches operation, every switch is shared among the three phases. This is done to prevent a short circuit across the DC sources by allowing only one switch to be turned on when the others are turned off. As a result, line-to-line voltage waveform (V_{AB}) produces nine voltage steps at the inverter output, as shown in Figure 2.2.

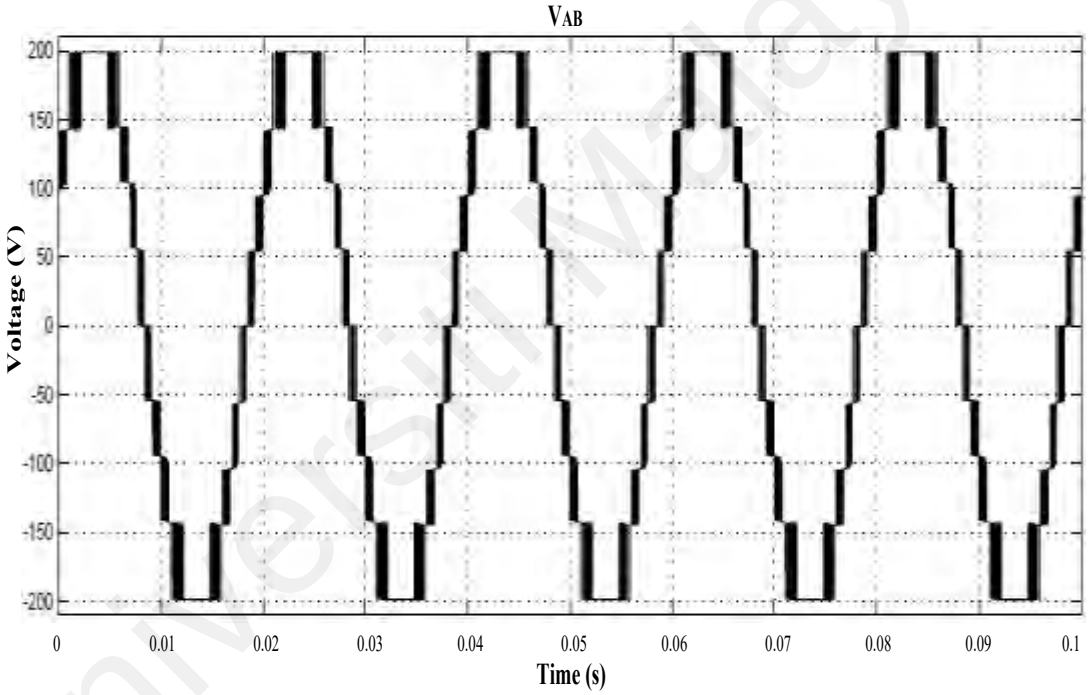


Figure 2.2: Line-to-line voltage waveform (V_{AB}) for the five-level switch-sharing-based multilevel inverter.

2.3 Review on Capacitor Voltage Balancing Methods

Like the classical multilevel inverters, switch-sharing-based multilevel inverter also has shortcomings that can affect the inverter output voltage quality. Several factors, such as unequal capacitance leakage currents and unequal delays in semiconductor

devices, lead to the capacitor voltage imbalance issue for the inverters (Srikanthan & Mishra, 2010). The voltage-drift phenomenon degrades the AC-side voltage waveforms, and this results in an unfavorable outcome. There are two methods to overcome the unbalanced capacitor voltages in the inverter; by improving the PWM strategies (Wang, Xu, Zheng, & Li, 2016; Saeedifard, Iravani, & Pou, 2009; Hotait et al., 2007) and by implementing a balancing circuit (Abdullah, Rahim, Sheikh Raihan, & Ahmad, 2014; Srikanthan & Mishra, 2010; Cui & Ge, 2018; Qin, Zhu, Gao, Shu, & Gao, 2014; He, Shu, Ding, Zhu, & Jing, 2013; Newton & Sumner, 1999).

2.3.1 PWM Modification

The first method is the modification of the pulse-width modulation (PWM) switching pattern. The switching pattern will be selected from the redundant states to regulate the capacitor voltages at their reference value (Choi & Saeedifard, 2012). Many researchers prefer this method since no additional hardware is needed. However, this technique leads to the complexity of the control system. Gao et al (Gao et al., 2013) proposed a novel diode-clamped modular multilevel converter with a power feedback control method. It is claimed that the control strategy can also control the capacitor voltages in the diode-clamped circuit and improve the overall performance. The drawback of this method lies in the limitation of the modulation index and the control system complexity. Modification of the switching strategy can only balance the capacitor voltage at low modulation indexes. Saeedifard et al, (Saeedifard et al., 2007) proposed a space-vector-modulation (SVM)-based switching strategy to balance the capacitor voltages. The results showed that it worked at low modulation indexes only.

2.3.2 Voltage Balancing Circuits

The second method for the capacitor voltage balancing is implementing an auxiliary circuit connected to the DC-link capacitors and the multilevel inverter. This method requires extra circuits, which can increase the cost for components and the complexity of the circuit. Despite the drawback, the circuit offers a satisfactory balancing performance without negatively affecting the inverter's output since the control method and auxiliary circuit are separated from the inverter circuit. Many balancing circuits are proposed by researchers to be used in classical multilevel inverters, especially DCMI.

2.3.2.1 Buck-boost Converter

A buck-boost converter is one of the well-known auxiliary circuits for the capacitor voltage balancing solution. The buck-boost circuit is used for preventing the imbalance of a DC capacitor voltage in a three-phase five-level DCMI, as portrayed in Figure 2.3 (Shukla, Ghosh, & Joshi, 2012). The converter inductor is used to store energy transferred from the overcharge capacitor to the undercharge capacitor to control the capacitor voltages. There are two types of buck-boost converter, a single-quadrant circuit and a two-quadrant circuit. The two single-quadrant buck-boost converter circuits shown in Figure 2.3(a), only work under steady-state conditions. This is because the charging process happens in one direction only from capacitor C_{d1} to C_{d2} by using inductor $L_1$and switch Sc_1 and from capacitor C_{d3} to C_{d4} by using L_2 and Sc_2.

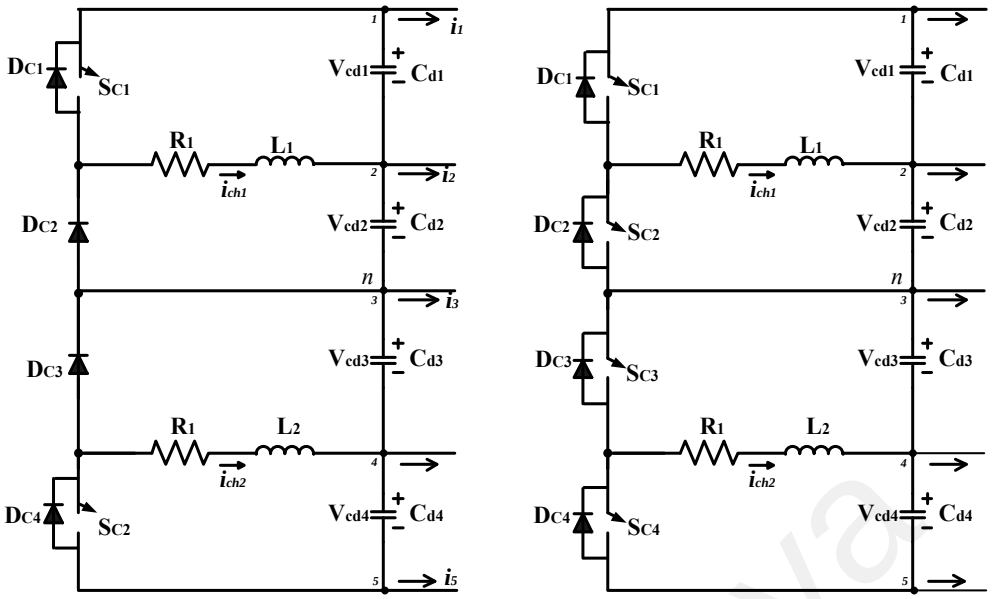


Figure 2.3: (a) Single quadrant buck-boost converter circuit

(b)Two-quadrant buck-boost converter circuit.

Many researchers prefer to use the two-quadrant buck-boost converter because the circuit can balance the capacitor voltage under transient conditions. Moreover, they can save cost as most of the power semiconductor switching modules have been built with anti-parallel diodes. The two-quadrant buck-boost converter circuit is used to control the capacitor voltages in a three-phase five-level DCMLI, as shown in Figure 2.3(b) (Shukla et al., 2012). It consists of four power switches, two inductors and four diodes. For the experimental setup, the buck-boost converter is connected to a single-phase five-level IGBT based DCMI. The DC voltage is supplied at V_{dc} = 80 V with V_{ref} = 20 V and modulation index, m_a of 0.85. Using a single-pulse control, the result shows that capacitor voltages can be equally balanced at the reference voltage of 20 V with a five-level waveform line-to-line voltage produced at the inverter output.

Akagi et al. (Akagi & al., 2008) applies two bidirectional buck-boost converter circuit for the capacitor voltage balancing in 6-6 kV transformerless static synchronous

compensator (STATCOM) based on the five-level diode clamped PWM converter. From Figure 2.4, the authors proposed combining a PWM method with the ability for voltage balancing at the mid-point node M with a voltage balancing circuit for positive, P1 and negative, N1 nodes. The experimental outcome which is obtained from a 200-V, 10-kVA laboratory model, confirms the viability and effectiveness of the voltage-balancing circuit and control.

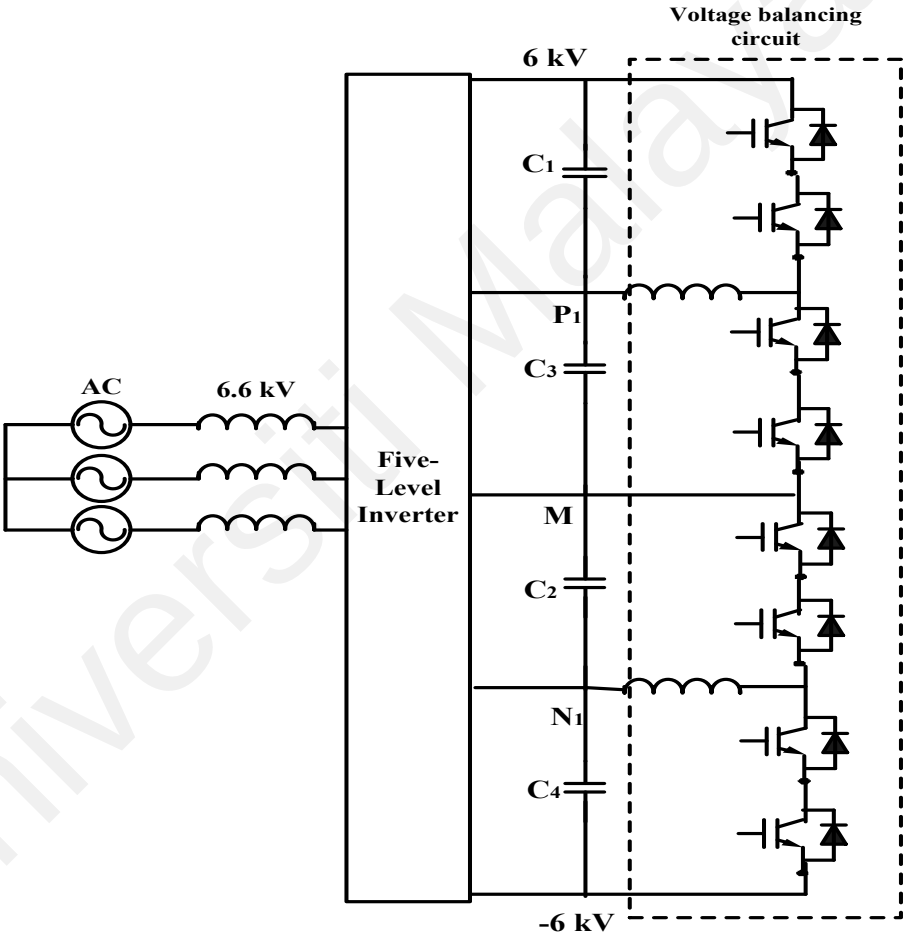


Figure 2.4: Buck-boost converter circuit for voltage balancing in 6-6 kV transformerless STATCOM based on a five-level diode-clamped PWM converter.

A two-bidirectional buck-boost converter circuit is also used to balance the four capacitor voltages in five-level diode-clamped PWM converters connected back-to-back for motor drives (Hatti et al., 2008). A 6.6-kV, 1-MW transformerless motor drive system

where the five-level rectifier is connected directly to the 6.6-kV grid is shown in Figure 2.5 along and five-level inverter connected to the 6.6-kV motor without a transformer. A 200-V 5.5-kW laboratory model for experimental setup is built. A common 3-kHz triangle-carrier signal is utilized to generate gate signals for the two converters. The outcomes from the experiment have confirmed the effectiveness of the voltage-balancing circuit and the validity of the theoretical analysis. It is found that the capacitor voltages are in balance mode at their reference values, and the inverter produces a nine-level waveform. On top of that, the line current THD value is less than 5%, and each harmonic current is found to be less than 3%.

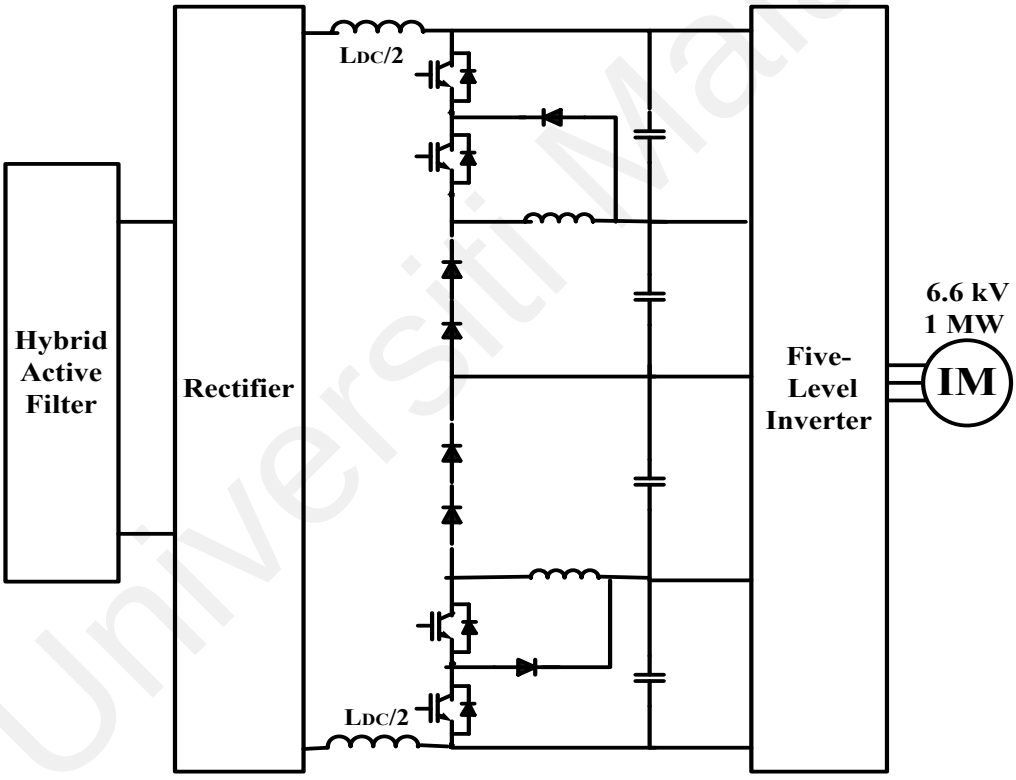


Figure 2.5: Buck-boost converter circuit for voltage balancing in 6.6-kV transformerless motor drive equipped with the hybrid active filter (Akagi et al., 2008).

2.3.2.2 Flying Capacitor Based Converter

Another auxiliary circuit for a three-phase DCMI is the three-level flying capacitor-based converter circuit (Shukla, Ghosh, & Joshi, 2010). This circuit is well-recognized for reducing voltage stress across converter switches and improving its reliability. Compared to the buck-boost converter, this type needs an additional power semiconductor device with a lesser rating and capacitors. Figure 2.6 indicates that the number of switches used for this converter circuit is twice as many as that of the buck-boost converter circuit. This is an undesirable case as when the converter levels are increased, and this would lead to higher costs and other losses. Moreover, when three switches are turned on simultaneously, the short circuit is bound to happen, causing the voltage imbalance for the capacitors. Besides, the control philosophy of the converter could be complicated and tedious since the number of switches required will be increased.

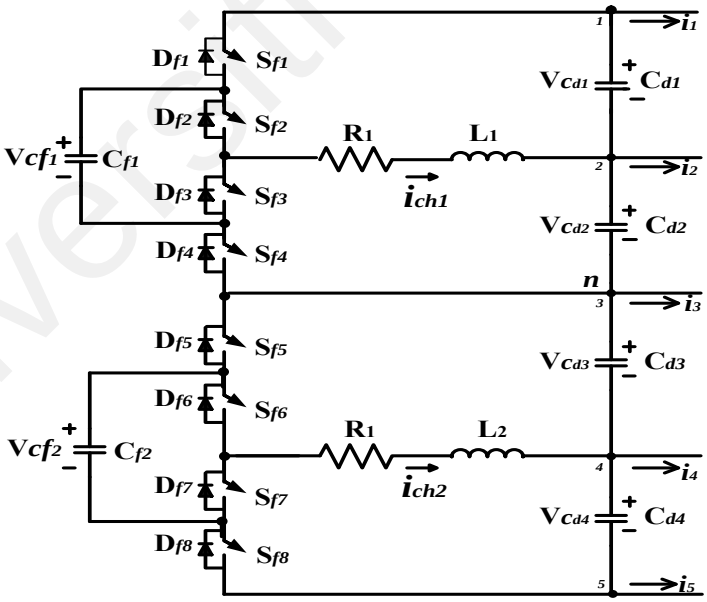


Figure 2.6: Flying capacitor-based converter circuit for voltage balancing in single-phase DCMI.

2.3.2.3 Resonant Switched-Capacitor Converter

Sano et al. (Sano & Fujita, 2008) have introduced a resonant switched-capacitor converter (RSCC) for a new voltage balancing circuit with a new phase shift control to enhance the performance of voltage balancing. RSCC manages to reduce the inductor to one-tenth of the volume compared to the buck-boost converter. Figure 2.7 illustrates the configuration of the RSCC circuit with a five-level DCMI. The RSCC contains the two half bridge inverters and four switching devices which are named S_1, S_2, S_3, and S_4, and a series of resonant circuits L_{r1} and C_{r1}. The resonant capacitor, C_r, is used to store the transferred energy instead of an inductor L_r. On top of that, a small inductor, L_r is the sole difference compared to the conventional switched capacitor converter in the circuit configuration, leading to great suppression of spike currents, power losses EMI. Nonetheless, another problem arises as to the number of switches increase, whereby the switching losses will in return, change the control system into a more complicated capacitor voltage balancing scheme. The results obtained from the experiment have verified the validity of the theoretical analysis and the proposed control method. The proposed method shows a voltage error of 0.5%.

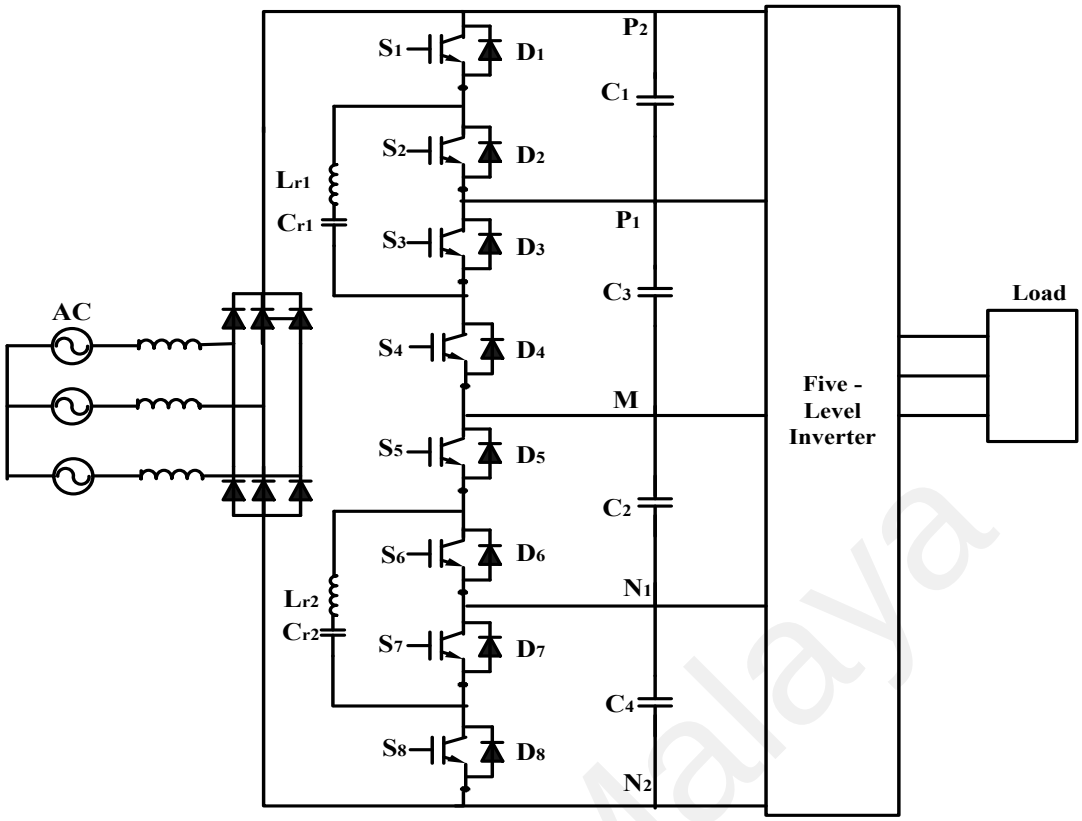


Figure 2.7: Voltage-balancing circuit based on an RSCC for multilevel inverters.

2.3.2.4 Parallel Switch-Based Chopper

Ajami et al. (Ajami et al., 2014) have introduced a new auxiliary circuit to overcome the disadvantages of RSCC. A parallel switch-based chopper circuit is proposed to solve the unbalanced capacitor voltage in DCMI, as shown in Figure 2.8. It is mentioned that the circuit has the lowest number of switches in comparison with other auxiliary circuits. The proposed chopper circuit consists of three power switches compared to the buck-boost converter, which consists of four power switches. Hence, this implies the switching losses are lesser, and the control system becomes simpler. In this research, the authors perform the simulation study on the three-phase five-level DCMI with the proposed balancing circuit using MATLAB/SIMULINK. The input voltage, V_{dc} is supplied at 200 V, and the parameters for the DC-link capacitors are $C_1 = C_2 = C_3 = C_4 = 330$ μF and $L_1 = L_2 = L_3 = 2$ mH. As a result, all the capacitor voltages are found to balance at their reference value of 50 V. A nine-level line-to-line voltage is

generated at the output voltage waveform without any distortion, and the steps are the same.

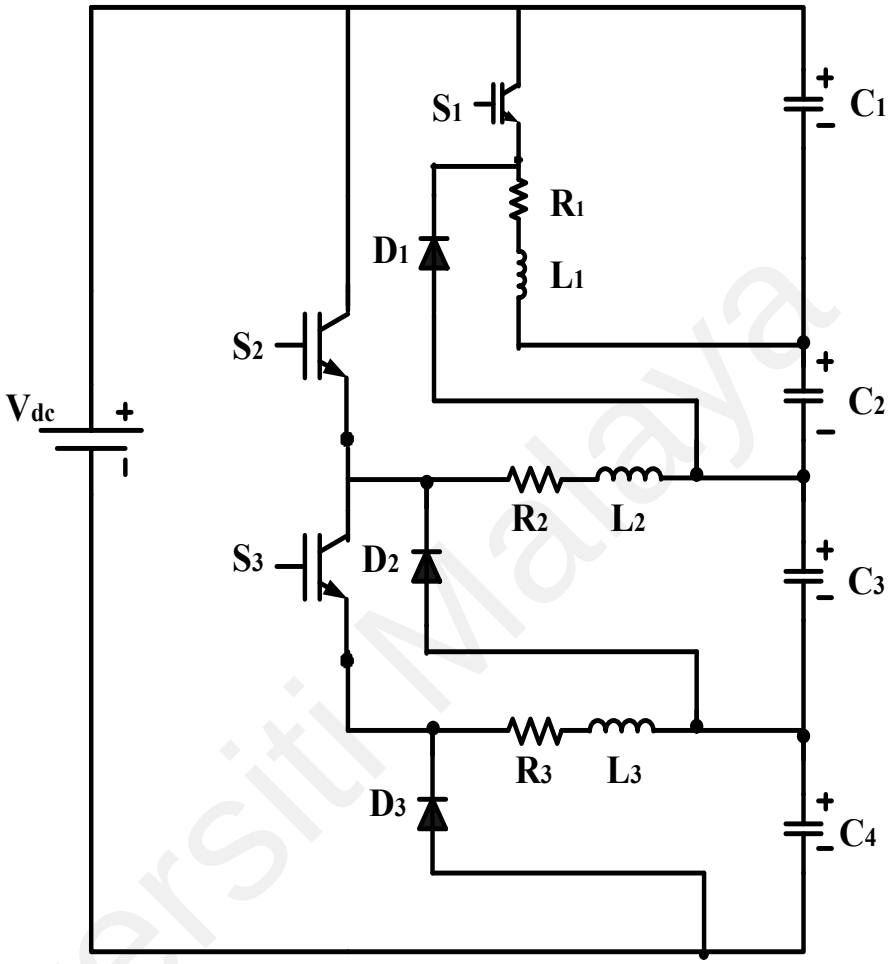


Figure 2.8: Voltage-balancing circuit based on parallel-switch based chopper circuit.

However, for the switch-sharing-based multilevel inverter's case, the simulation result shows that the parallel-switch based chopper circuit cannot balance the capacitor voltage at high modulation indexes, $m_a = 0.9$, as shown in Figure 2.9. Capacitor C_1 and C_4 tend to charge while capacitor C_2 and C_3 tend to discharge. As a result, this type of circuit is not suitable for the switch-sharing-based multilevel inverter, which requires a high modulation index to achieve the best performance.

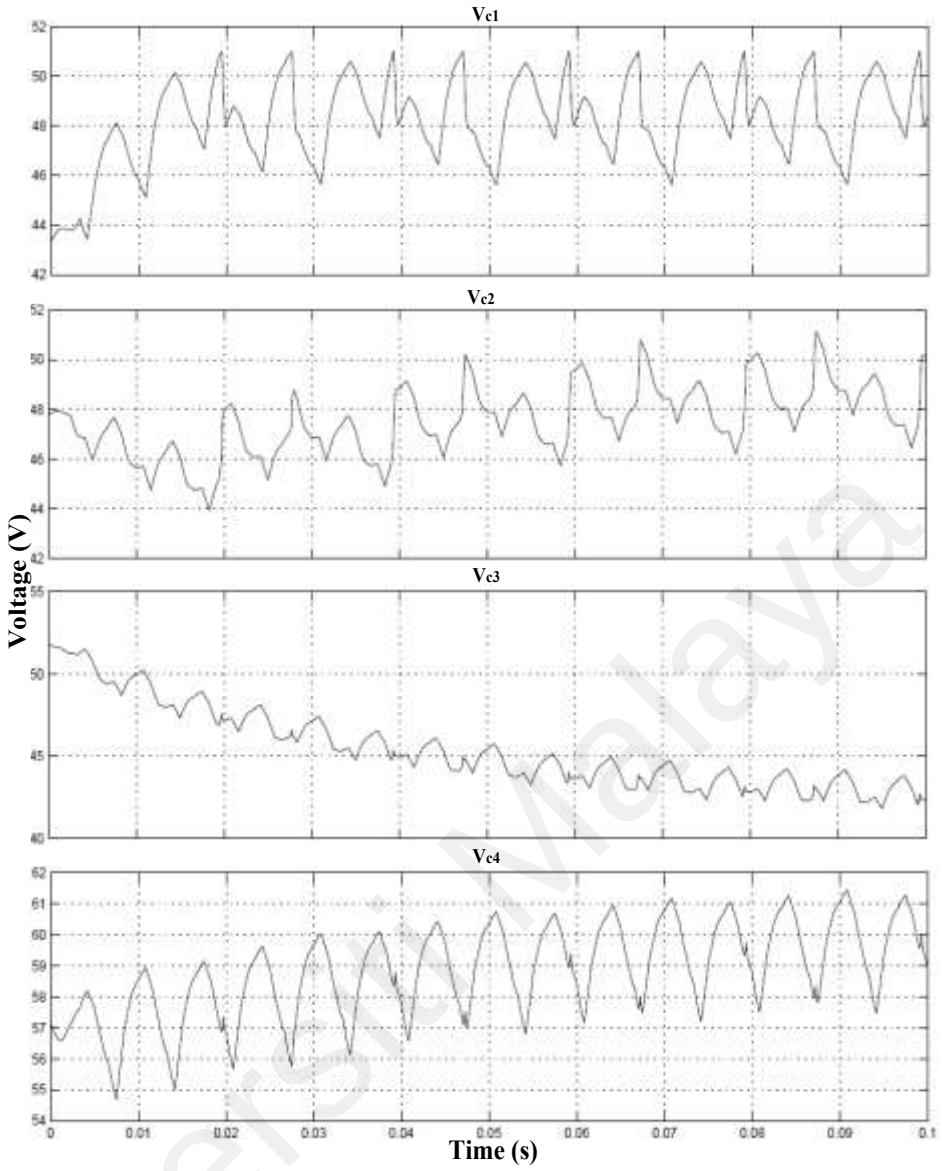


Figure 2.9: Simulation result of capacitor voltages (V_{c1}, V_{c2}, V_{c3}, V_{c4}) in switch-sharing-based inverter by implementing parallel-switch based chopper.

2.3.2.5 Novel Flying-Capacitor-Based Voltage Balance Circuit (VBC)

Cui et al (Cui & Ge, 2018), has introduced a novel hybrid voltage balance technique (VBC) for five-level DCMIs, where flying-capacitor-based auxiliary circuits are used to keep the balance for the top part or the bottom part of the two capacitors, along with a zero-sequence injection to keep the midpoint voltage in balance. The voltage stresses of the power devices are made to be equal, and the current ripples of inductors

can also be suppressed with the flying capacitors working as energy-storage elements. Figure 2.10 presents the configuration of a system consisting of a five-level DCMI with VBC. The DC-link of five-level DCMI contains four series-connected capacitors. The proposed VBC is divided into two parts which are upper and lower parts. Every part of the VBC consists of a flying capacitor, an inductor and four insulated gate bipolar transistors (IGBTs) with free-wheeling diodes. The proposed VBC can allow a bidirectional power flow between the DC-capacitors so that it can be applied for back-to-back applications, such as adjustable motor drives and HVDC transmissions.

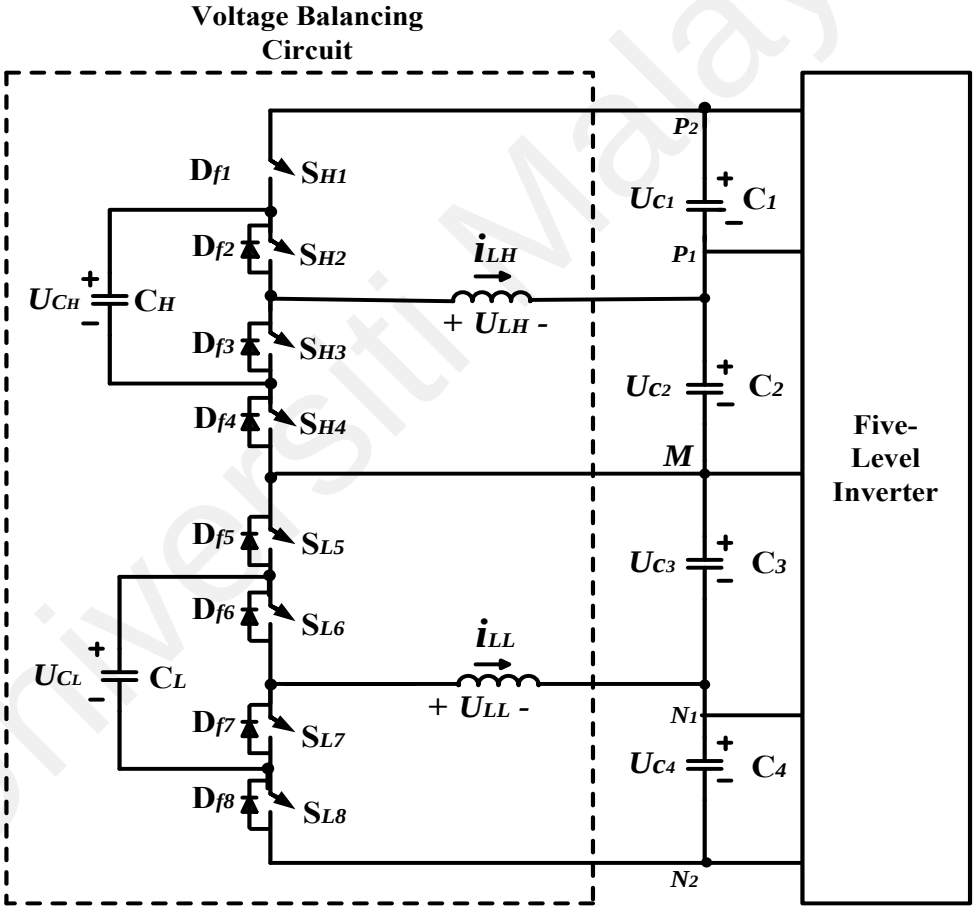


Figure 2.10: Voltage balancing circuit based on VBC in DCMI (Cui & Ge, 2018).

As mentioned in (A. Shukla et al., 2010), the flying capacitors are quite different from the auxiliary circuits as shown in Figure 2.10. The mentioned capacitors used to

transfer the energy between two adjacent DC-capacitors, and introduce the inductors to limit discharging currents. The inductors of the proposed VBCs are much smaller than the buck-boost converter owing to (Hatti et al., 2008) the use flying capacitors as energy-storage elements, leading to the reduced volume and weight (Sano & Fujita, 2008). The discharging current spikes can be removed efficiently by changing the current-limiting resistors (Shukla et al., 2010) and inductors (Shu, He, et al., 2013), which results in fewer losses and electromagnetic noises (Sano & Fujita, 2008). However, the number of the components in the circuit increases compared to the buck-boost converter circuit, leading to the complexity of the control algorithm.

2.4 Control Techniques

Control techniques play an important role in controlling switching signals for capacitor voltage balancing in an inverter. A system with certain criteria such as high dynamic response, low harmonic distortion of the output current, small current ripple, good DC voltage utilization and the limited or constant switching frequency is ideal for a safe operation of power devices (Kazmierkowski & Malesani, 1998). Various control algorithms are utilized in the capacitor voltage balancing, such as hysteresis voltage control, proportional-integral (PI) control, single-pulse control, multi-pulse control, hysteresis band current control, fuzzy control, model predictive control and proportional-resonant control.

2.4.1 Hysteresis Voltage Control

The hysteresis control is a method that can be implemented to control a capacitor voltage whereby a comparison of the reference voltage and the actual voltage are made on an instantaneous basis to create switching pulses for the converter. Hysteresis comparators are used in this type of controller to process voltage errors, followed by direct

generation of the switching signals for the power switches. The technique controls the switches asynchronously for ramping up and down the voltage through a capacitor to ensure it tracks the reference voltage signal. Figure 2.11 shows a configuration of hysteresis voltage control whereby the error signal, *e* is the difference between the reference voltage and the actual capacitor voltage. The lower and upper limits related to minimum and maximum values of the error signals, are e_{min} and e_{max}, respectively.

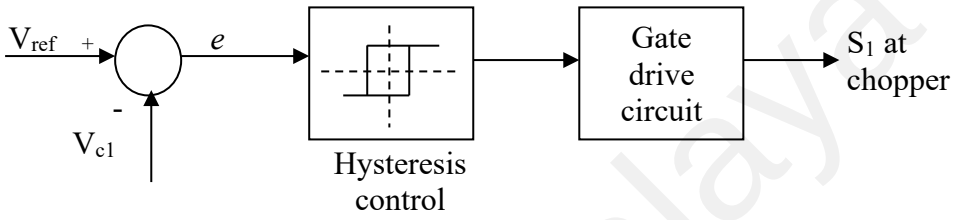


Figure 2.11: Block diagram of hysteresis voltage control.

The hysteresis band is the range of error signals (e_{min} - e_{max}) where the converter's output voltage is controlled so that the voltage can be maintained within the upper and the lower hysteresis band limits, as seen in Figure 2.12. The dynamic performance is considered excellent as the switching signals are created from the direct comparison in the hysteresis comparators, which results in fast responses. It is easy to practice this scheme practically as it is only based on a simple concept that is robust and has low tracking errors (Kazmierkowski & Malesani, 1998). However, the hysteresis control scheme is generally characterized by a variable switching frequency of the converter during the foundation period (Brod & Novotny, 1985). As a result, occasional irregular operations of the converter occur, leading to the increase in the switching losses (Azizur Rahman, Radwan, Osheiba, & Lashine, 1997). Hence, to prevent undesirable effects of variable switching frequency, constant switching frequency hysteresis controllers are introduced. An adaptive hysteresis controller is suggested by varying the hysteresis band based on the variations in motor speed, load current and neutral-point voltage for holding

switching frequency constant at any operating condition (Tae-Won & Meong-Kyu, 1996). To enhance the transient response and stabilize the switching frequency (Zare, Zabihi, & Ledwich, 2007), the multiband hysteresis concept has been studied (Loh, Bode, Holmes, & Lipo, 2002). A finding has introduced a new space-vector-based hysteresis current controller for the multilevel inverter-fed induction motor drive (Dey, Rajeevan, Ramchand, Mathew, & Gopakumar, 2013) whereby the control scheme utilizes a varying parabolic hysteresis band for controlling the switching frequency variation and employing a specific voltage vector selection procedure to make sure that an optimal switching of the inverter is achieved.

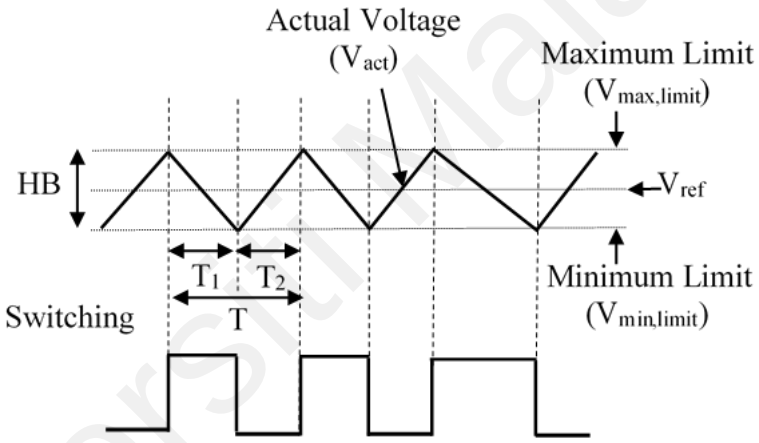


Figure 2.12: Hysteresis switching method.

2.4.2 PI Control

PI controller is one famous controller among researchers, most studied and developed for many applications as presented in a lot of past literature (Visioli, 2001; Vrančić, Petrovčič, & Peng, 1997; Sayed, Gharghory, & Kamal, 2015; Yu Jin, Ryu, Sung, Lee, & Lee, 2014). It also produces good performance in a wide range of operating conditions. A PI transfer function can be written as

$$G_c(s) = K_p + \frac{K_I}{s} \tag{2.1}$$

The controller provides a proportional gain, K_P and an integration term, K_I. The equation for the output in the time domain is:

$$u(t) = K_p e(t) + K_I \int e(t)dt \tag{2.2}$$

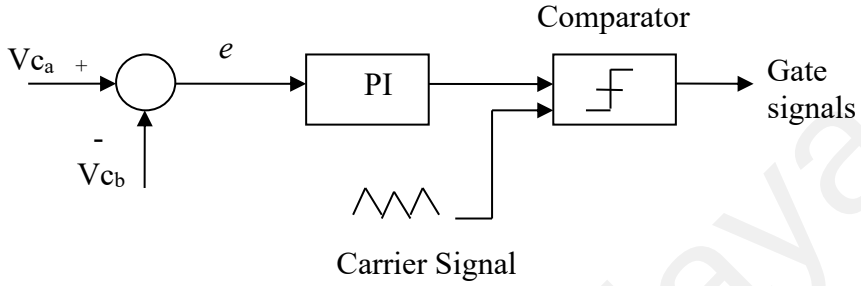


Figure 2.13: Basic PI control scheme.

Figure 2.13 shows the basic Pl control scheme used in DCMI to control switches for the capacitor voltage balancing solution. In this control scheme, PI controllers are used to minimizing the voltage error between two capacitor voltages, *e* and then generate the control signals for switches in the converter. This control signal acts as modulating signal, which is next used to compare with triangular carrier signals (Abdullah et al., 2014; Akagi et al., 2008). The results of the comparison provide the switching signals for switches in the converter. Several considerations are taken into account when designing a PI controller since it plays a crucial role in minimizing errors through an integral part and controlling the amount of ripple via the proportional gain and zero placement (Kazmierkowski & Malesani, 1998). To avoid multiple crossings, PI gain should be limited so that the slope of the modulating signals does not exceed the triangular signal slope. This is because multiple crossings contribute to an increase in switching frequency and switching losses. Besides, to ensure the tracking error does not become large, it can be avoided by not providing overly low PI gain values.

2.4.3 Single-Pulse Control Using State-Space Model

This type of controller is specially designed to balance capacitor voltage in a buck-boost converter. The advantage of this control is it does not involve faster-switching actions. According to Shukla et al (Shukla et al., 2012), the mathematical expressions for this control involve converter currents and capacitor voltages of the converter circuit. Figure 2.3 (a) shows the circulating currents ($i_1 – i_5$) in the inverter-capacitor loops which are also present in the mentioned mathematical expressions. These complicated mathematical equations are derived to calculate the time durations for switches to be ON and OFF so that the energy can be exchanged between the capacitors. However, this control method requires a large current rating of the converter which is one of its drawbacks. Furthermore, a single-pulse control does not ensure robust and reliable performance.

2.4.4 Multi-Pulse Control

Multi-pulse control is proposed to overcome the limitation which is found in single-pulse control. It can be realized by reducing the converter current rating below a certain defined current limit, $I_{chlimit}$. Figure 2.14 shows the multi-pulse control for a buck-boost converter whereby the switch is maintained to be closed until the chopper achieves the pre-defined current limit, $I_{chlimit}$. From that point, the switch is opened and is kept that way until the current from the converter decreases to zero by energy transfer to the undercharged capacitor through an anti-parallel diode. Nonetheless, this control to switch multiple times to equalize capacitor voltages depending on the current limit. As a result, a response using this control is much slower than the single-pulse control method.

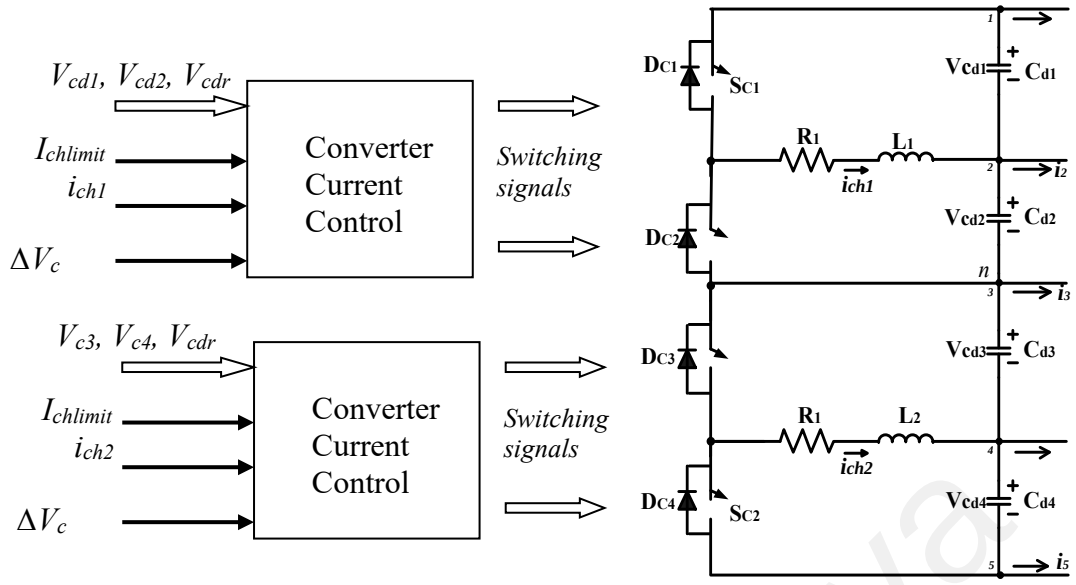


Figure 2.14: Block diagram of multi-pulse control for buck-boost converter circuit.

2.4.5 Hysteresis Band Current Control

Hysteresis band current control is proposed to overcome the problem with the single-pulse and multi-pulse control methods. This control method offers a faster dynamic performance due to the inclusion of the converter current feedback. Figure 2.15 shows a block diagram of the proposed hysteresis band converter current control. The current is controlled by this scheme in a manner to determine the average value of the difference of the two corresponding capacitor currents. Hence, the rate of charging and discharging for the capacitors become equal, and they achieve equalization. The initial voltage imbalance can be nullified since this involves a proportional voltage controller. However, the limitation of this control depends on the hysteresis band size, whereby the switching losses in the converter circuit increase as the hysteresis band size decreases. Moreover, the hysteresis band current control needs converter switches for a faster operation than the single-pulse and multi-pulse control. Therefore, this control method is not economically viable for some applications, specifically those with higher power levels.

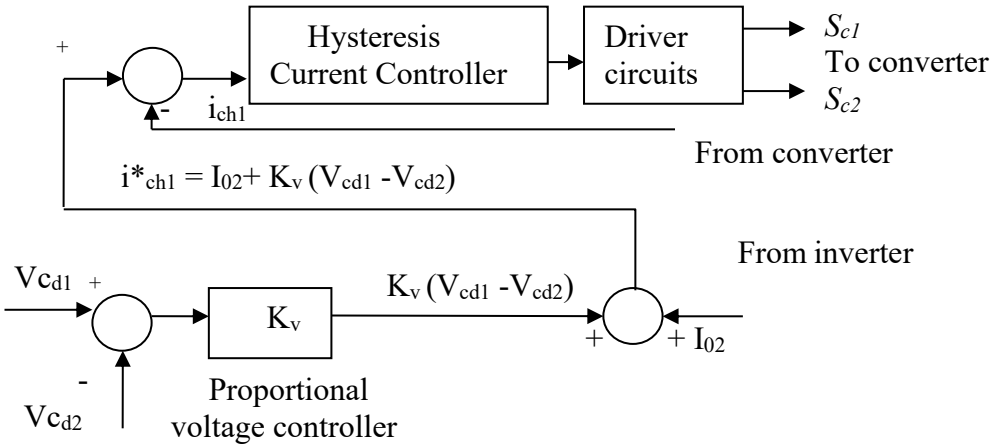


Figure 2.15: Block diagram of hysteresis band current control for buck-boost converter circuit.

2.4.6 Fuzzy Control

Fuzzy control is a control strategy that is widely used for dc-dc converters. The advantages of fuzzy control are well known because it has a simple control scheme and robustness (Guo et al., 2011). With the development of adaptive-fuzzy logic control (FLCs), improvements can be seen in the performance of fuzzy logic controllers (FLC). Adaptive-FLCs has been implemented in various industrial processes to achieve the desired control requirements. It is also known as a self-tuning fuzzy (STF) controller since it combines of PI controller and fuzzy logic. The PI controller parameter values of proportional K_P and/or K_i can be changed online when the tuning mechanism based on fuzzy logic is applied.

In dealing with the nonlinear nature of a three-level boost converter (TLBC), a new fuzzy controller application with a self-tuning PI controller (STF-PI) has been proposed (Nouri et al., 2017). It can be used to balance the capacitor voltage and to control the DC bus voltage in TLBC. This can be achieved using a STF-PI controller that has been designed for each operating point. The transfer function of the duty cycle for the

proposed controller has been derived from TLBC small-signal model. As a result, the capacitor voltages of TLBC are balanced at their reference voltage with lower quadratic error.

2.4.7 Model Predictive Control

The predictive controller is attractive since it can handle a nonlinear system and offers low harmonic distortion and noise to achieve precise current control. Nevertheless, it is usually harder to be implemented and needs an exact load to be matched to it (Gálvez-Carrillo et al., 2009). In an input series output series (ISOS) modular DC-DC converter, a modified model predictive control (MPC) known as the duty cycle-based MPC (DC-MPC) has been proposed to address the capacitor voltage imbalance issue (Wei et al., 2017). The proposed DC-MPC differs from the conventional MPC, whereby it can optimize duty cycles with a fixed switching frequency rather than a variable switching frequency. By predicting the effects on input voltage sharing (IVS) and output voltage sharing (OVS) of the fundamental modules, the optimized duty cycles can be determined. With the optimized duty cycles, the proposed DC-MPC can rapidly attain IVS and OVS when there is a voltage imbalance of the ISOS converter between the input capacitor and output capacitor.

2.4.8 Proportional-Resonant Control

PR controller has been increasingly attractive for the grid-connected and stand-alone system (Hassaine et al., 2014). The use of the quasi-proportional-resonant controller to control the voltage balancing of a capacitor in a single-phase AC/AC modular multilevel converter has been presented in (Liu et al., 2016). In this research, the controller has been applied in an inter-arm balancing method to assure the capacitor voltages have an even distribution without affecting the input/output power quality.

Equation (2.3) shows the transfer function of an ideal PR controller, which can achieve a zero-phase shift, and around the resonance frequency spectrum, it has a large gain.

$$G_{PR}(s) = K_p + K_i \frac{s}{s^2 + \omega_0^2} \tag{2.3}$$

where, ω_0 is the resonance frequency, K_p is the proportional gain, and K_i is the integral gain of the controller. Meanwhile, equation (2.4) below is derived for a PR controller that is not ideal so that stability problems related to a large gain can be avoided.

$$G_{PR}(s) = K_p + K_i \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{2.4}$$

Where ω_c is the cutoff frequency that widens the controller's passband. This is to ensure that during practical applications, the system is more robust. Moreover, Blaabjerg et al, (Blaabjerg et al., 2006) have proposed a PR regulator design method based on the theory of root locus analysis and feedback of capacitor's current so that the system stability and dynamic response are guaranteed.

Table 2.1 gives a meta-analysis of the related works being referred to for this research.

2.5 Summary

This chapter has summarized the voltage balancing methods in detail and the control methods used for balancing in general for multilevel inverters, especially DCMI. The switch-sharing-based multilevel inverter becomes the focus area in this work for improved characteristics and performance via the enhancement of capacitor voltage balancing solution.

Table 2.1: Meta-analysis of the related works

Title	Author(s)	Year	Work	Strength	Limitations/Future work
Control of dc capacitor voltages in diode-clamped multilevel inverter using bidirectional buck-boost choppers	A.Shukla, A.Ghosh, A.Joshi	2012	The buck-boost circuit is used for preventing the imbalance of a DC capacitor voltage in a three-phase five-level DCMI. The converter inductor is used to store energy transferred from the overcharge capacitor to the undercharge capacitor to control the capacitor voltages.	The two-quadrant buck-boost converter circuit can balance the capacitor voltage under transient conditions. The circuit can save cost as most of the power semiconductor switching modules have been built with anti-parallel diodes.	-
Flying-capacitor-based chopper circuit for dc capacitor voltage balancing in diode-clamped multilevel inverter.	A.Shukla, A.Ghosh, A.Joshi	2010	The three-level flying capacitor-based converter circuit is an auxiliary circuit used for a three-phase DCMI. The number of switches used for this converter circuit is twice as many as that of the buck-boost converter circuit. This is an undesirable case as when the converter levels are increased, and this would lead to higher costs and other losses.	This circuit is well-recognized for reducing voltage stress across converter switches and improving its reliability.	The control philosophy of the converter could be complicated and tedious since the number of switches required will be increased.

Voltage-Balancing Circuit Based on a Resonant Switched-Capacitor Converter for Multilevel Inverters	Kenichiro Sano, Hideaki Fujita	2008	A resonant switched-capacitor converter (RSCC) is introduced to enhance the performance of voltage balancing. The RSCC contains the two half bridge inverters and four switching devices which are named S_1, S_2, S_3, and S_4, and a series of resonant circuits L_{r1} and C_{r1}. The resonant capacitor, C_r, is used to store the transferred energy instead of an inductor L_r.	RSCC manages to reduce the inductor to one-tenth of the volume compared to the buck-boost converter.	As to the number of switches increase, whereby the switching losses will in return, change the control system into a more complicated capacitor voltage balancing scheme.
Parallel switch-based chopper circuit for DC capacitor voltage balancing in diode-clamped multilevel inverter	Ali Ajami, Hossein Shokri, Ataollah Mokhberdoran	2014	Parallel chopper circuit is a new auxiliary circuit to overcome the disadvantages of RSCC. It is mentioned that the circuit has the lowest number of switches in comparison with other auxiliary circuits.	The proposed chopper circuit consists of three power switches compared to the buck-boost converter, which consists of four power switches. Hence, this implies the switching losses are lesser, and the control system becomes simpler.	The simulation result shows that the parallel-switch based chopper circuit cannot balance the capacitor voltage at high modulation indexes, $m_a = 0.9$, for the switch-sharing-based multilevel inverter's case.
A Novel Hybrid Voltage Balance Method for	Dongdong Cui, Qiongxuan Ge	2018	A novel hybrid voltage balance technique (VBC) is introduced for five-level DCMIs, where flying-capacitor-based auxiliary circuits are used to keep the	The inductors of the proposed VBCs are much smaller than the buck-boost converter owing to the use flying capacitors as energy-	The number of the components in the circuit increases compared to the buck-boost converter circuit, leading to the

Five-Level Diode-Clamped Converters			balance for the top part or the bottom part of the two capacitors, along with a zero-sequence injection to keep the midpoint voltage in balance. The proposed VBC can allow a bidirectional power flow between the DC-capacitors so that it can be applied for back-to-back applications, such as adjustable motor drives and HVDC transmissions.	storage elements, leading to the reduced volume and weight. The discharging current spikes can be removed efficiently by changing the current-limiting resistors and inductors, which results in fewer losses and electromagnetic noises.	complexity of the control algorithm.
Hysteresis Voltage Control	A.Shukla, A.Ghosh, A.Joshi	2012	Hysteresis comparators are used in this type of controller to process voltage errors, followed by direct generation of the switching signals for the power switches. The technique controls the switches asynchronously for ramping up and down the voltage through a capacitor to ensure it tracks the reference voltage signal.	The dynamic performance is considered excellent as the switching signals are created from the direct comparison in the hysteresis comparators, which results in fast responses. It is easy to practice this scheme practically as it is only based on a simple concept that is robust and has low tracking errors.	The hysteresis control scheme is generally characterized by a variable switching frequency of the converter during the foundation period. As a result, occasional irregular operations of the converter occur, leading to the increase in the switching losses

PI Control	Rosmadi Abdullah, Nasrudin Abd.Rahim, Siti Rohani Sheikh Raihan, Abu Zaharin Ahmad	2014	PI controllers are used to minimizing the voltage error between two capacitor voltages, *e* and then generate the control signals for switches in the converter. This control signal acts as modulating signal, which is next used to compare with triangular carrier signals.	It produces good performance in a wide range of operating conditions	To avoid multiple crossings, PI gain should be limited so that the slope of the modulating signals does not exceed the triangular signal slope. This is because multiple crossings contribute to an increase in switching frequency and switching losses.
Single-Pulse Control Using State-Space Model	A.Shukla, A.Ghosh, A.Joshi	2012	This type of controller is specially designed to balance capacitor voltage in a buck-boost converter. The mathematical expressions for this control involve converter currents and capacitor voltages of the converter circuit. These complicated mathematical equations are derived to calculate the time durations for switches to be ON and OFF so that the energy can be exchanged between the capacitors.	This control is it does not involve faster-switching actions.	This control method requires a large current rating of the converter which is one of its drawbacks. Furthermore, a single-pulse control does not ensure robust and reliable performance.

Multi-Pulse Control	A.Shukla, A.Ghosh, A.Joshi	2012	Multi-pulse control is proposed to overcome the limitation which is found in single-pulse control. The switch is maintained to be closed until the chopper achieves the pre-defined current limit, $I_{chlimit}$. From that point, the switch is opened and is kept that way until the current from the converter decreases to zero by energy transfer to the undercharged capacitor through an anti-parallel diode.	The control can reduce the converter current rating below a certain defined current limit, $I_{chlimit}$.	This control to switch multiple times to equalize capacitor voltages depending on the current limit. As a result, a response using this control is much slower than the single-pulse control method.
Hysteresis Band Current Control	A.Shukla, A.Ghosh, A.Joshi	2012	Hysteresis band current control is proposed to overcome the problem with the single-pulse and multi-pulse control methods. The current is controlled by this scheme in a manner to determine the average value of the difference of the two corresponding capacitor currents. Hence, the rate of charging and discharging for the capacitors become equal, and they achieve equalization.	This control method offers a faster dynamic performance due to the inclusion of the converter current feedback.	However, the limitation of this control depends on the hysteresis band size, whereby the switching losses in the converter circuit increase as the hysteresis band size decreases.

DSP-based implementation of a self-tuning fuzzy controller for three-level boost converter	Abdellatif Nouri, Issam Salhi, Said Elbeid, Najib Essounbouli	2017	Self-tuning PI controller (STF-PI) has been proposed to deal with the nonlinear nature of a three-level boost converter (TLBC). The transfer function of the duty cycle for the proposed controller has been derived from TLBC small-signal model. As a result, the capacitor voltages of TLBC are balanced at their reference voltage with lower quadratic error.	This control has a simple control scheme and robustness	-
Model Predictive Control of Capacitor Voltage Balancing for Cascaded Modular DC-DC Converters	Qiang Wei, Bin Wu, Dewei Xu, Navid Reza Zargari	2017	A modified model predictive control (MPC) known as the duty cycle-based MPC (DC-MPC) can optimize duty cycles with a fixed switching frequency rather than a variable switching frequency.	The control can handle a nonlinear system and offers low harmonic distortion and noise to achieve precise current control.	It is usually harder to be implemented and needs an exact load to be matched to it.

Simplified model and submodule capacitor voltage balancing of single-phase AC/AC modular multilevel converter for railway traction purpose.	Wanxun Liu, Kai Zhang, Xiaosen Chen, J. Xiong	2016	The controller has been applied in an inter-arm balancing method to assure the capacitor voltages have an even distribution without affecting the input/output power quality.		

CHAPTER 3: VOLTAGE BALANCING METHOD BASED ON BUCK-BOOST CONVERTER

3.1 Introduction

This chapter describes the voltage balancing method based on the implementation of the auxiliary circuit. Since the switch-sharing-based multilevel inverter shares common characteristics with DCMI, similar solutions used for capacitor voltage balancing in DCMI are chosen for the application in the switch-sharing-based multilevel inverter topology. Modifying the PWM strategy is not applicable as redundant switching states are unavailable in this type of inverter, leading to the proposed buck-boost converter for balancing the DC-link voltage. Section 3.2 explains the details on the operational principle of the buck-boost converter used as the auxiliary circuit. Two PI controllers will control switches for the ON and OFF operations so that the four DC-link capacitor voltages will be equally balanced. In this work, the proposed controller with a performance-based online tuning mechanism is suggested to enhance their responses. In addition, the performance of the capacitor voltages and inverter's outputs are also improved compared to using the conventional PI controller.

3.2 Buck-Boost Converter

In this work, the buck-boost converter is selected for DC-link capacitor voltage balancing in the switch-sharing-based multilevel. The advantages of the buck-boost converter as the best solution for capacitor voltage balancing circuits are described in Section 2.3.2. Figure 3.1 shows the circuit configuration of the buck-boost converter to balance the voltages of the four capacitors in the five-level switch-sharing-based multilevel inverter. The buck-boost circuit is considered as the simplest configuration since it only consists of four power switches (S_1, S_2, S_3, S_4) and two inductors (L_1, L_2) and they are connected to four DC-link capacitors (C_1, C_2, C_3, C_4). The inverter is

supplying an RL-load of R = 120 Ω and L = 69 mH while modulation index is 0.9. The dc capacitors are C_1= C_2= C_3= C_4= 2200 μF, buck-boost converter are L1=L2= 12 mH (a Shukla et al., 2012).

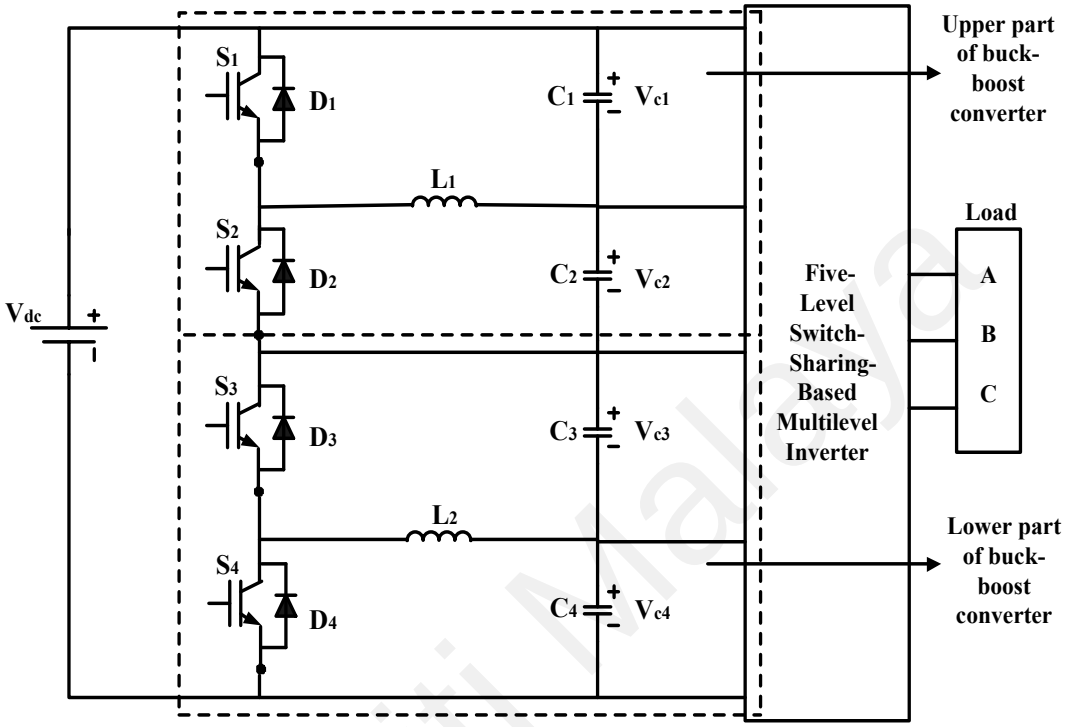
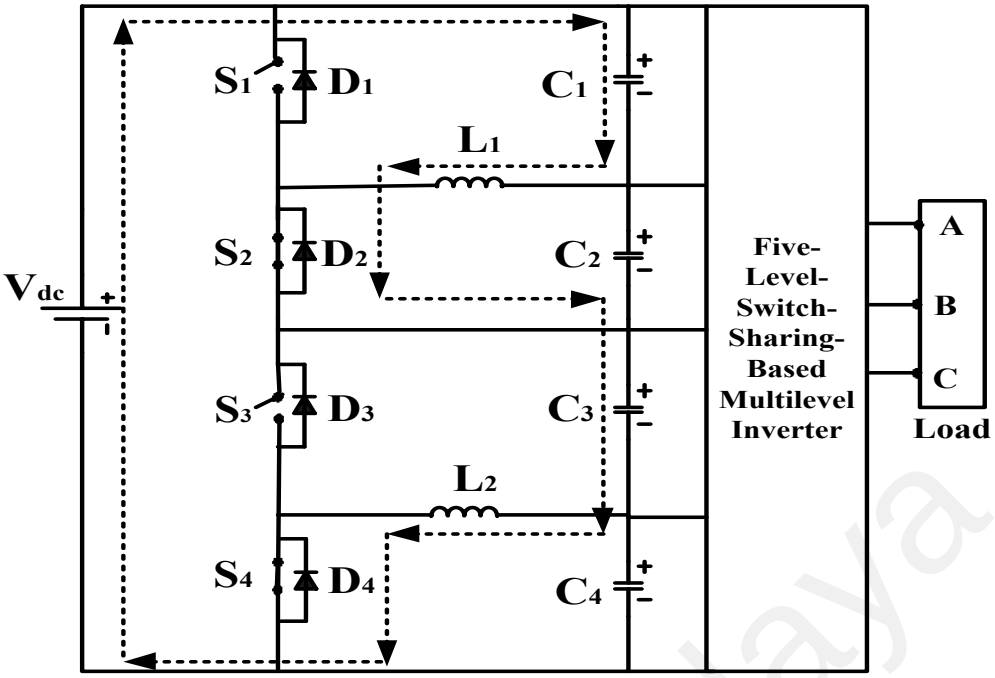


Figure 3.1: Circuit configuration of the buck-boost converter for DC-link capacitor voltage balancing in a five-level switch-sharing-based multilevel inverter.

There are two separate parts of the buck-boost converter known as the upper and lower parts. The upper part consists of one inductor (L_1) and two power switches (S_1 and S_2), while the lower part consists of one inductor (L_2) and two power switches (S_3 and S_4). These parts are connected to four DC-link capacitors (C_1, C_2, C_3, C_4) of the five-level three-phase switch-sharing-based multilevel inverter. In this work the precaution steps are taken into account since a short circuit might happen when all power switches (S_1, S_2, S_3, S_4) are turned ON simultaneously. Therefore, for each part of the buck-boost converter, the power switches are designed to switch ON and OFF in complementary mode to avoid the short circuit.

The elements of inductors, diodes and switches are used to transfer energy between capacitors in the circuit. Energy in the upper part of the circuit is transferred between C_1 and C_2 through inductor L_1 and diodes D_1 and D_2. Meanwhile, S_3 and S_4 are complementary switches in the lower part of the circuit since the energy can be transferred between C_3 and C_4 through inductor L_2 and diodes D_3 and D_4.

The conditions of switches S_1, S_2, S_3 and S_4 are determined by using pulse-width modulation (PWM) signals to balance all DC-link capacitor voltages at their reference values. The operations of charging and discharging for the capacitors in both parts of the buck-boost converter circuit are presented in Figure 3.2. There are four different operating modes of charging and discharging for the capacitors, current flow paths in all modes. The charging process for capacitors C_1 and C_3 occurs as switches S_2 and S_4 are switched ON during mode 1. On the other hand, capacitors C_2 and C_4 are discharged as switches S_1, and S_3 are switched OFF. During mode 2, S_1 and S_3 are switched ON to allow the charging of capacitors C_2 and C_4. As for the complementary switches, S_2 and S_4 are automatically switched OFF to allow capacitors C_1 and C_3 to be discharged. Capacitors C_1 and C_4 will start to charge when S_2 and S_3 are turned ON during mode 3, and S_1 and S_4 are consequently turned OFF. As a result, capacitors C_2 and C_3 will start to discharge. The related switching signals will turn S_1 and S_4 switches ON for the last mode to allow capacitors C_2 and C_3 to be charged. Automatically, capacitors C_1 and C_4 will start to discharge as S_2 and S_3 are turned OFF. Capacitors will continue to charge and discharge until they reach the respective reference values.



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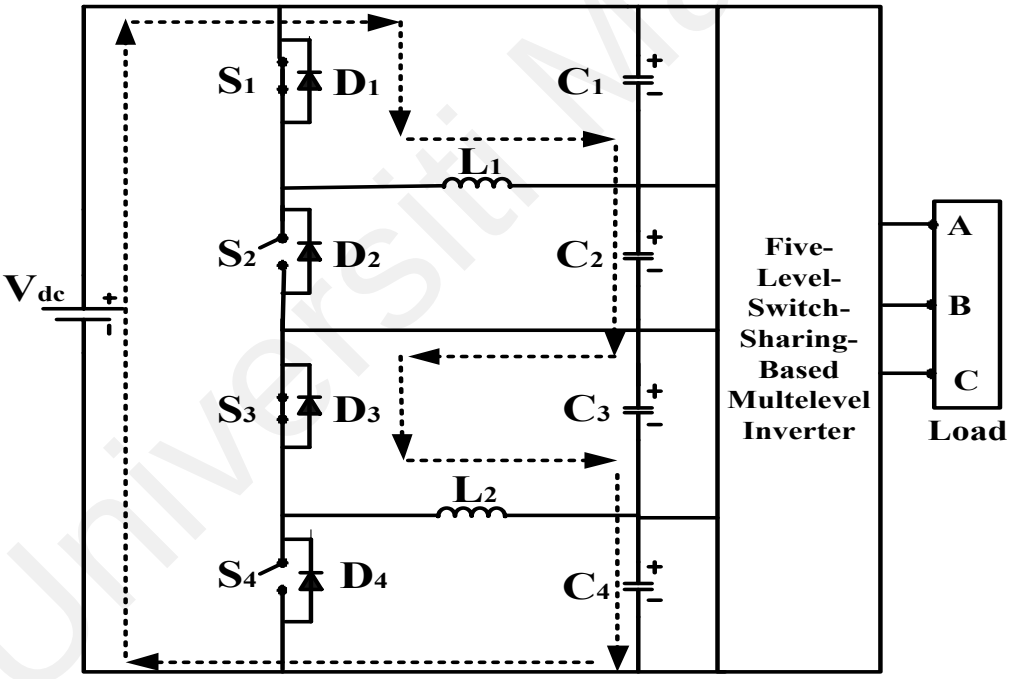

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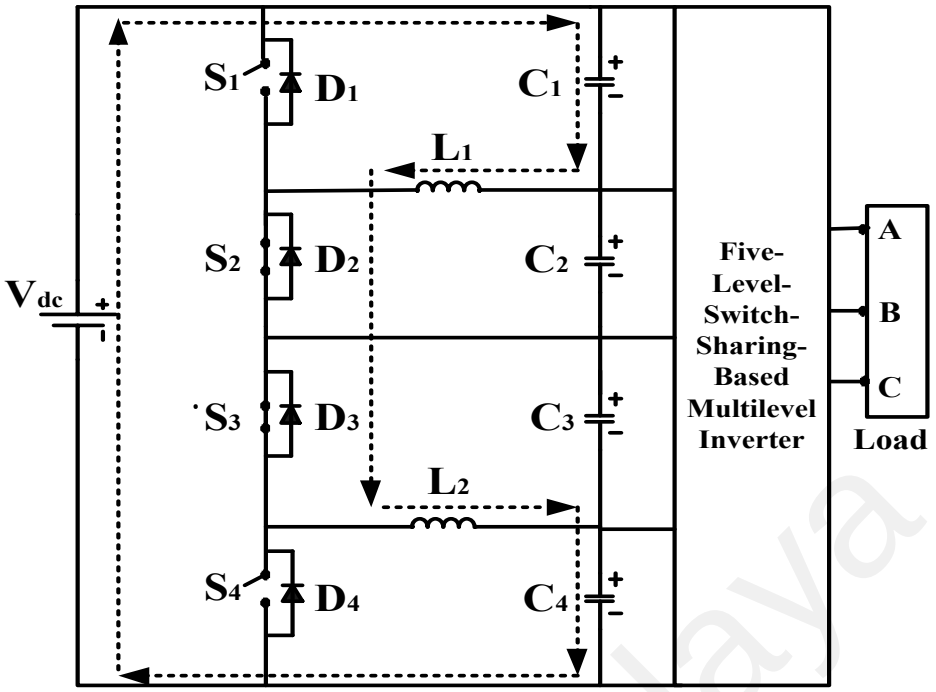

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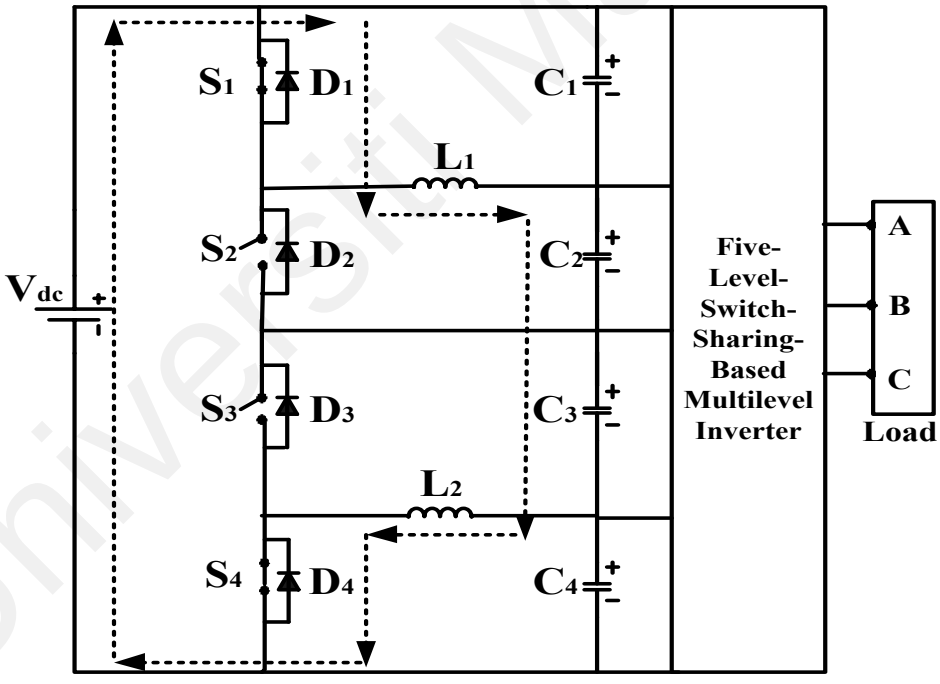


d

Figure 3.2: Different operating modes of the buck-boost converter.

(a) Mode 1: (S_2 and S_4 ON, S_1 and S_3 OFF).
(b) Mode 2: (S_1 and S_3 ON, S_2 and S_4 OFF).
(c) Mode 3: (S_2 and S_3 ON, S_1 and S_4 OFF).
(d) Mode 4: (S_1 and S_4 ON, S_2 and S_3 OFF).

3.3 Control Scheme

A controller is very important to a system. It is a component in a system that monitors certain input variables and adjusts output variables to achieve the desired operation. This section highlights the use of conventional PI controller and proposed PI controller with the performance-based online tuning mechanism to control the switching signals at the buck-boost converter.

3.3.1 PI Controller

Owing to its uncomplicated structure that comes with a powerful performance in various operating conditions, the PI controller is widely chosen to be used in many applications (Abdullah et al., 2014; Hatti et al., 2008). One attractive benefit offered by this type of controller is eliminating or reducing steady state errors. Figure 3.3 presents the block diagram of the PI controller to produce the switching signals. C_1, C_2, C_3, and C_4, are connected between the converter and the inverter circuits. Therefore, every capacitor will be at a reference voltage, whereby $V_{ref} = V_{dc}/4$. Two controllers are used as there are two parts in the converter circuit. Voltage errors e(t) can be minimized by using the PI controller, leading to the controller output y(t) derivation. Generally, the voltage error is a voltage difference between the two-split DC-link capacitor voltages whereby $e_1(t)$ is the error between two capacitor voltages by subtracting Vc_2 from Vc_1 and e_2 (t) is the error between two capacitor voltages Vc_4 and Vc_3. Proportional gain K_{pU} and integral gain K_{iU} are used to reduce $e_1(t)$ for the upper part of the circuit and proportional gain K_{pL} and integral gain K_{iL} are used to reduce $e_2(t)$ for the lower part of the circuit. Equation (3.1) and Equation (3.2) show the proportional and integral terms which are added up to produce the outputs; $y_U(t)$ and $y_L(t)$.

$$y_U(t) = K_{pU}e_1(t) + K_{iU}\int e_1(t)dt \tag{3.1}$$

$$y_L(t) = K_{pL}e_2(t) + K_{iL}\int e_2(t)dt \quad (3.2)$$

The power switches are turned ON or OFF according to the applied switching signals. The outputs of the PI controllers, $y_U(t)$ and $y_L(t)$ are compared with the carrier signals to produce the switching signals. The ON and OFF switching operation of switches S_1, S_2, S_3, and S_4 rely on either charging or discharging the capacitors. Nonetheless, it is crucial to consider that the charging and discharging processes would be kept repeating until the capacitors are fully charged.

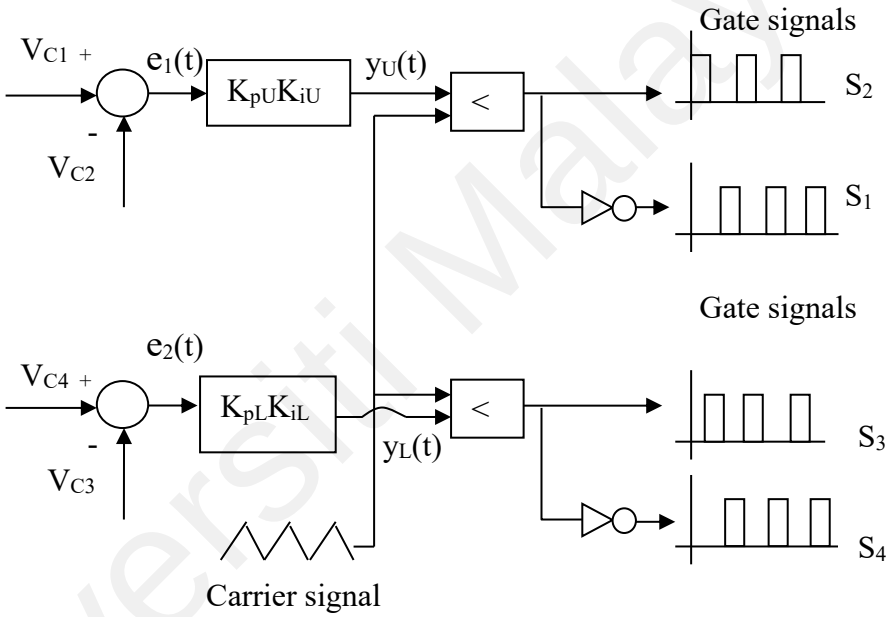


Figure 3.3: Block diagram of PI controllers for the upper and lower part of the converter.

3.3.2 Proposed PI Controller with Performance-Based Online Tuning Mechanism

The conventional PI controller may not achieve satisfactory dynamic performance at all times. To overcome this shortcoming, performance-based online tuning mechanisms have been introduced. Tuning mechanisms have been implemented in many studies with various tuning methods as reviewed in (Reynoso-Meza, Sanchis, Blasco, & Freire, 2016; Alagoz, Ates, & Yeroglu, 2013; Mobin, Mousavi, Komaki, & Tavana, 2018). A new

tuning algorithm is proposed to add a performance-based online tuning mechanism feature to the PI controller in this work.

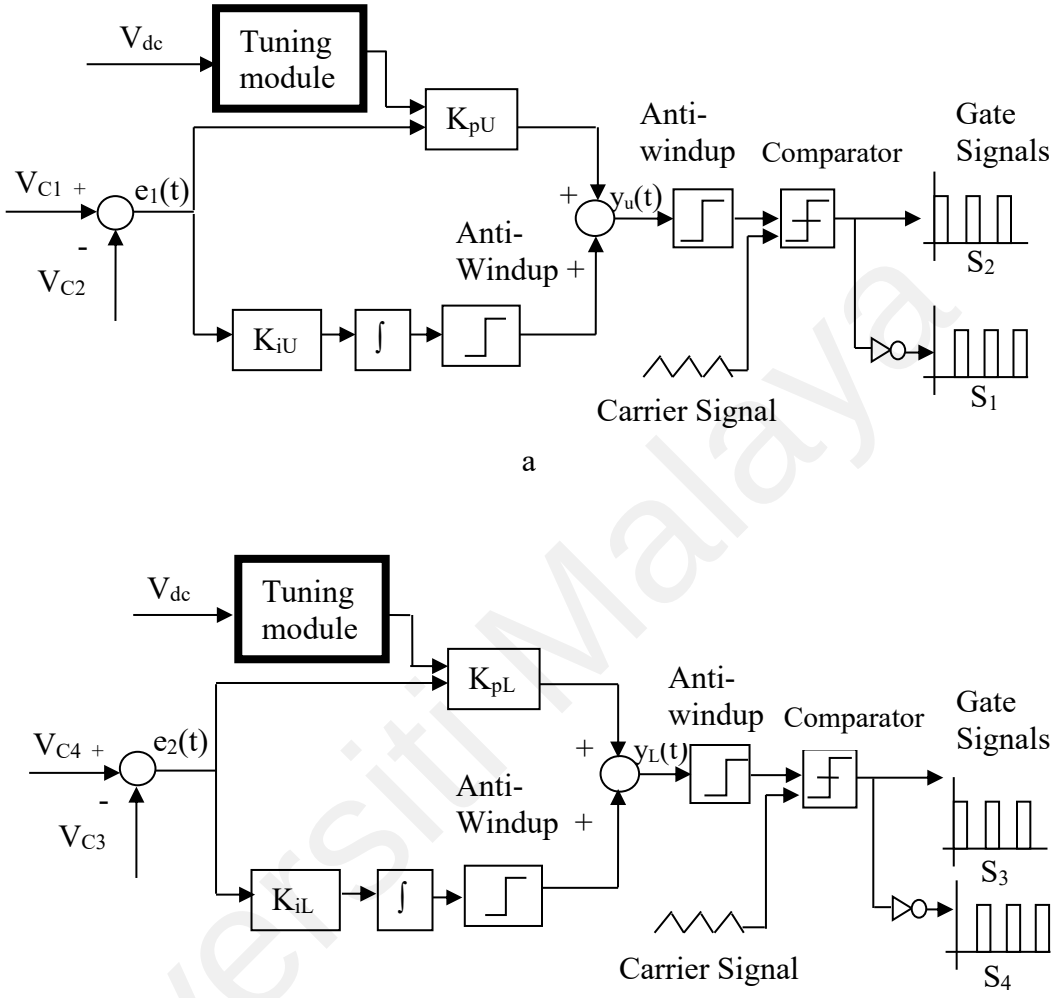


Figure 3.4: Block diagram of the proposed PI controller with online tuning module. (a) Upper part of buck-boost converter (b) Lower part of buck-boost converter

The proposed PI controller is based on the conventional PI controller as presented in Section 3.3.1. Here, the online tuning algorithm is designed to tune the value of the proportional gains (K_{pU}, K_{pL}) in both parts of the circuit. Meanwhile, the integral gains (K_{iU}, K_{iL}) for both parts remain unchanged.

The proposed PI controller contains an additional component in its structure compared with the conventional PI controller, which is the online tuning module. Figure 3.4 illustrates the block diagram of proposed PI controllers with online tuning modules for the upper and lower parts of the converter. The two proposed PI controllers are used to control $Vc_{1,}$ Vc_2, Vc_3 and Vc_4. The prime purpose of the online tuning module is for the fine-tuning of the proportional gain according to the DC input voltage while preventing the controller from reaching the state of saturation simultaneously. An input voltage V_{dc} signal is needed in the tuning module. Therefore, the right adjustment can be made according to the input voltage change. After that, comparing the outputs of the proposed PI controllers (y_U, y_L) with the carrier signals is carried out to generate the switching signals for the switches. From Figure 3.4, it is observed that the switching signals for S_1 and S_2 are complementary to each other, and the same case occurs for switches S_3 and S_4. Two anti-windup modules are applied whereby one module limits the output of integral K_{iU} and K_{iL}. Another one is to limit the controller's output $y_U(t)$ and $y_L(t)$ to prevent the controller from becoming saturated.

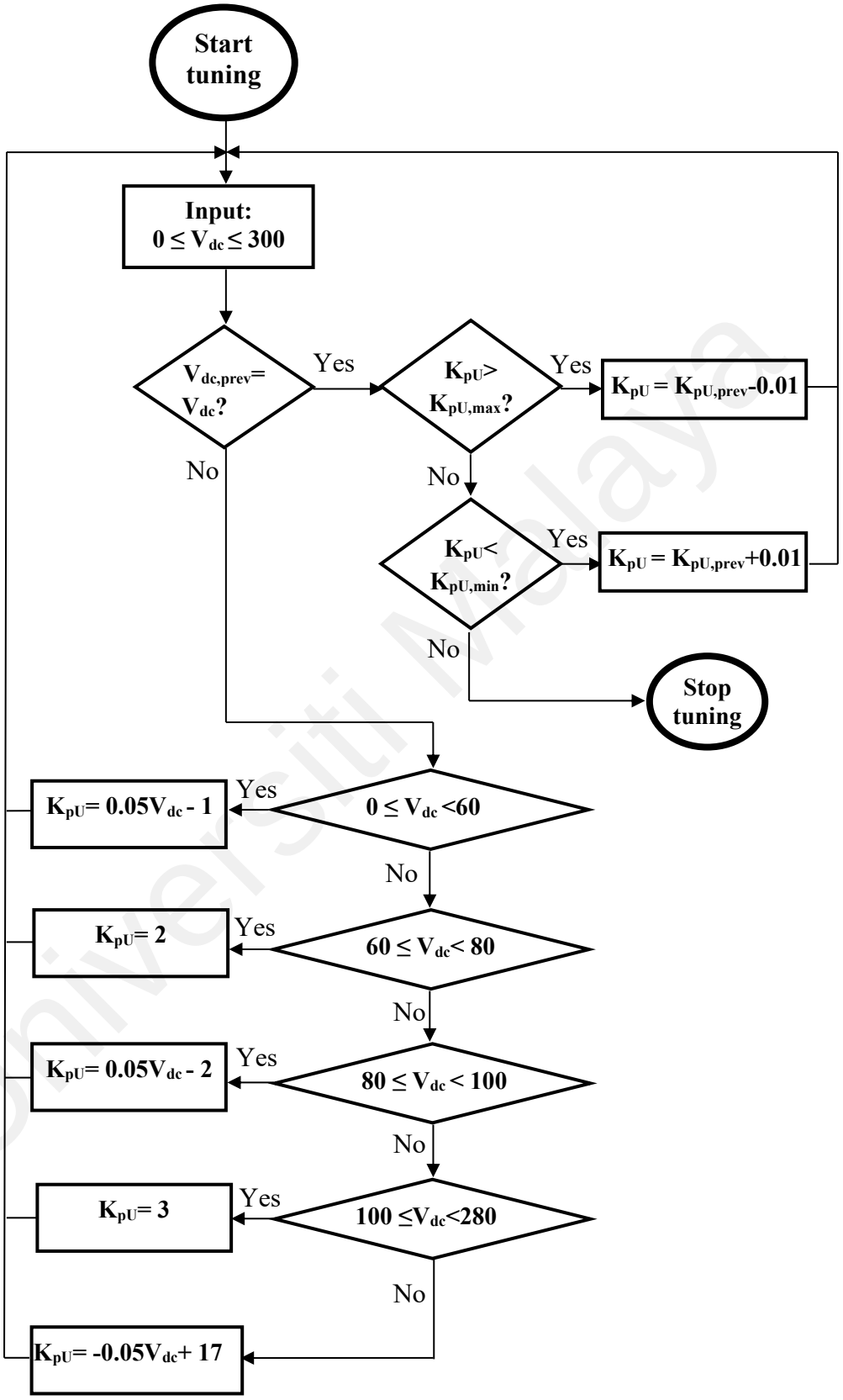


Figure 3.5: Flow of online tuning algorithm for the upper part of the buck-boost converter.

The process flow of the tuning algorithm for the upper part of the buck-boost chopper is displayed in Figure 3.5. To generate a new $K_{pU,}$ five equations are derived. The derivation is based on the correlation between K_{pU} and V_{in} that is established from a preliminary test. During the test, to minimize the tuning error due to the ideal-condition assumption, the actual measurement of the output current THD of the inverter is used to build the correlation above. Hence, the online tuning is carried out based on the actual performance of the inverter reflected by the measured output current THD. Further details of the preliminary test are provided in Section 5.

Firstly, the present value of V_{dc} is checked to ensure its similarity to its previous value, which is stored in $V_{dc,prev}$. $V_{dc,prev}$ is updated to the present value if it is different from the previous value. The new K_{pU} is then calculated according to the present value of V_{dc}. Consequently, the previous value of $K_{pU,prev}$ is updated to the new value of K_{pU}. If the value of V_{dc} is found to be in between the range of 0 V and 60 V, the new K_{pU} will be calculated as follows:

$$K_{pU} = 0.05V_{dc} - 1 \tag{3.3}$$

A new K_{pU} is constant at 2 if the present value V_{dc} is between 60 V and 80 V. If V_{dc} is between 80 V and 100 V, the new K_{pU} is given by the equation below:

$$K_{pU} = 0.05V_{dc} - 2 \tag{3.4}$$

If V_{dc} is between 100 V and 280 V, the new K_{pU} is constant at 3. The new K_{pU} is calculated as below if the present value V_{dc} is between 280 V and 300 V:

$$K_{pU} = - 0.05V_{dc} + 17 \tag{3.5}$$

If the present value of V_{dc} is the same as the previous value, then K_{pU} is checked whether it is within the allowable K_{pU} band. K_{pU} band is the maximum and minimum limits of K_{pU}.

K_{pU} should be in the limitation range to retain the balanced capacitor voltages at the lowest output current THD. In case the value of K_{pU} is more than the maximum limit of $K_{pU,max}$, the new K_{pU} will be evaluated by the equation below:

$$K_{pU} = K_{pU,prev} - 0.01 \tag{3.6}$$

Then, $K_{pU,prev}$ is updated to a new value of K_{pU}. The same procedure applies for the situation where K_{pU} is less than the minimum limit of $K_{pU,min}$. The new K_{pU} is calculated by increasing the previous value of $K_{pU,min}$ as stated by the equation below:

$$K_{pU} = K_{pU,prev} + 0.01 \tag{3.7}$$

These procedures are repeated in the following iterations until K_{pU} falls within the K_{pU} band. When the value of V_{dc} is the same as the previous value $V_{dc,prev}$ and K_{pU} is within the limited range, the tuning of the controller will be stopped.

The online tuning algorithm for the lower part of the buck-boost converter is presented in Figure 3.6. It is found that the process flow of the online tuning algorithm for the lower part is identical to the upper part except for their distinct equations of K_{pL}. There are five different equations for the new value of K_{pL} to be calculated when the present value of V_{dc} is not the same as the previous value of $V_{dc,prev}$. When V_{dc} is between 0 V and 60 V, the new K_{pL} is calculated based on the equation as follows:

$$K_{pL} = 0.05V_{dc} - 1 \tag{3.8}$$

If V_{dc} is between 60 V and 80 V, the new K_{pL} is updated at 2. The new K_{pL} is given by the equation below if the value of V_{dc} is between 80 V and 100 V.

$$K_{pL} = -0.05V_{dc} + 6 \tag{3.9}$$

K_{pL} is constant at 1 if the value of V_{dc} is between 100 V and 280 V. For the input voltage, V_{dc} between 280 V and 300 V, new K_{pL} is calculated based on the equation as follows:

$$K_{pL} = 0.05V_{dc} - 13 \quad (3.10)$$

Consequently, the value of $K_{pL,prev}$ is updated to the new value of K_{pL}. For the case where the present value of V_{dc} is almost the same as the previous value of $V_{dc,prev}$, the value of K_{pL} is checked to ensure it is located within the allowable value of the K_{pL} band. When the value of K_{pL} is higher than that value of $K_{pL,max}$, the calculation of the value of K_{pL} is done by lowering the previous value of $K_{pL,prev}$ by 0.01. The same step is used when the value of K_{pL} is lower than the value of $K_{pL,max}$, whereby the new value of K_{pL} is determined by increasing the previous value of $K_{pL,prev}$ by 0.01. The value of $K_{pL,prev}$ is then updated to the new value of K_{pL}. These steps will continue until the proportional gain, K_{pL} falls within the acceptable range.

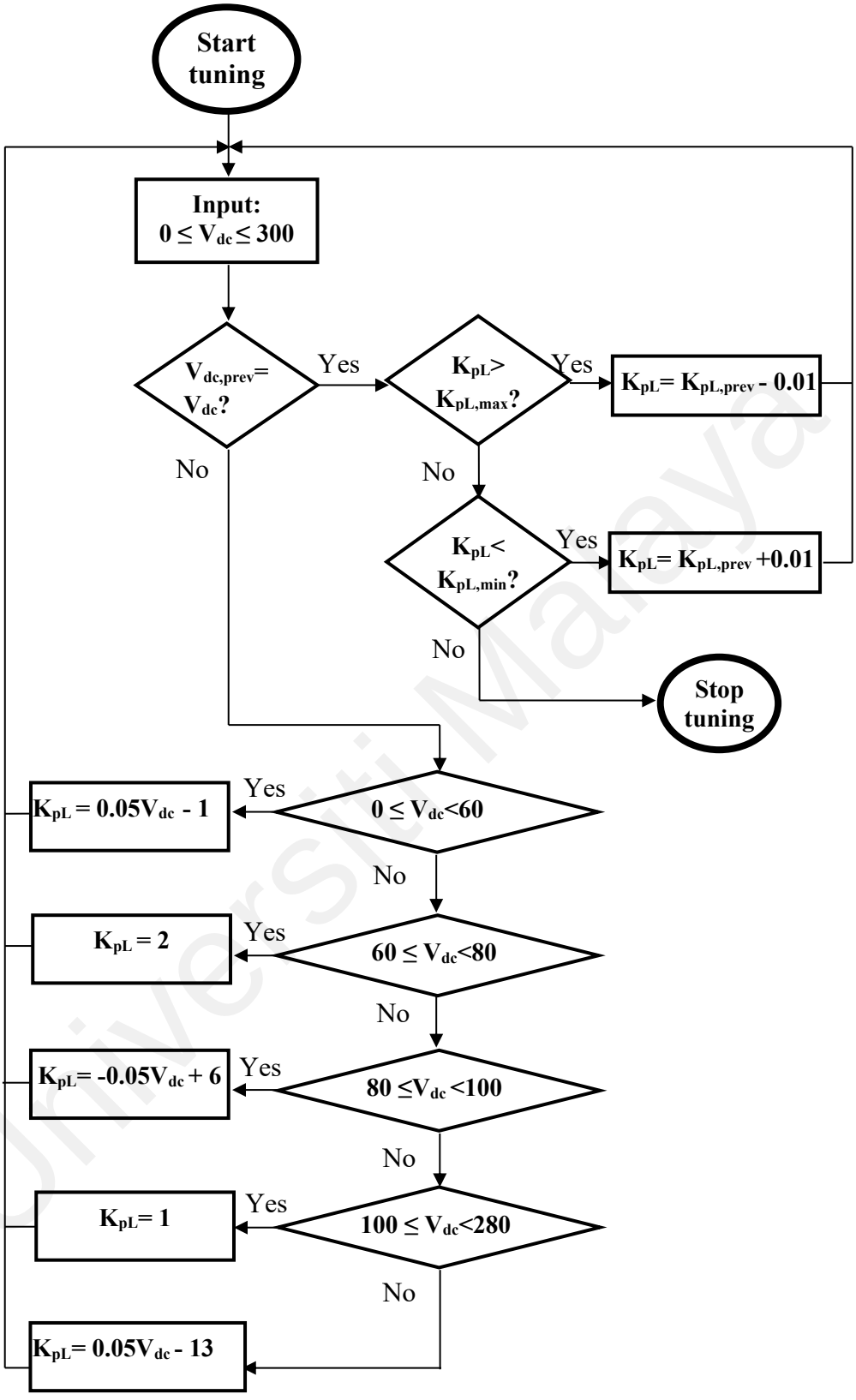


Figure 3.6: Flow of online tuning algorithm for the lower part of the buck-boost converter.

3.4 Summary

In this chapter, the capacitor voltage balancing method based on the buck-boost converter has been discussed. With the motivation to balance capacitor voltages in the five-level switch-sharing-based multilevel inverter, the balancing solution is adapted from the solution applied in DCMI topology since there are some similarities between the two inverters topologies. The design and operating principle of the buck-boost converter have been described. In this section, a new proposed performance-based online tuning algorithm is presented to tune the proportional gains of the upper and lower parts of the buck-boost converter so that a good quality of output current is maintained after a change in the input DC voltage. Basically, new proposed controller is introduced to improve the performance of the conventional PI controller. A conventional PI controller can be basically adequate to balance capacitor voltages at a given V_{dc}. However, when V_{dc} changes especially when the change is big enough, a conventional PI controller may not be running at its optimum operating point anymore, thus may cause some negative impacts on the inverter's performance. The proposed approach with the online tuning mechanism comes into the picture as a potential solution to rectify this situation. The online tuning mechanism provides a means to change the PI controller's operating point to the new optimum one when V_{dc} changes. By doing so, not only the capacitor voltages remain balanced, but also the good output quality of the inverter are kept intact, in addition to the satisfactory dynamic and steady state performances of the controller. This is owing to the fact that the online tuning algorithm treats the lowest THD of the output current as the main criterion for adapting to the change in V_{in}. The fact that tuning mechanism is simple, is a great advantage for real-time implementation. Ease of implementation is an important factor for practical application. In this aspect, the proposed approach offers an additional benefit that most other controllers encounter

difficulty to achieve. In addition, control simplicity also allows for the proposed method to be easily extended when the range of V_{dc} expands.

CHAPTER 4: SIMULATION RESULTS AND ANALYSIS

4.1 Introduction

In this chapter, the results of the simulation studies and analysis are explained in detail. The controller is designed and simulated using MATLAB/SIMULINK software to carry out preliminary analysis before real experiments are conducted. The simulation studies are performed to investigate the performance of the controllers. The conventional PI controller and the proposed PI controller with the performance-based online tuning mechanism are used in this investigation. In the beginning, the simulation study of the conventional PI controller is presented in Section 4.2 and followed by the simulation study of the proposed PI controller with an online tuning mechanism in Section 4.3. Figure 4.1 shows the circuit configuration of the three-phase five-level switch-sharing based multilevel inverter developed using MATLAB/SIMULINK. A Y-connected RL load with R = 120 Ω and L = 69 mH is connected to the inverter. The DC-link voltage is fixed at 200 V, thus $V_{ref} = V_{dc}/4 = 50$ V. The inductors are set as $L_1 = L_2 = 12$ mH, capacitors are 2200 μF each and the modulation index used is 0.9. The same parameters are applied to both simulation studies. Table 4.1 shows the parameters used for the simulation. The simulation is conducted in two conditions; with fixed input voltage and with variable input voltage. Step responses are investigated in the simulation study as a result of a change in the input voltage. The fixed DC voltage is set at 200 V and the variable DC voltage changes between 60 V and 200 V with a step response that's occurs at t = 0.03 s. The time duration for simulation is 0.1 s. Meanwhile, the simulation study of power loss and efficiency is carried out in Section 4.5. The purpose here is to study the impact of the online tuning mechanism in reducing power loss, improving efficiency and contributing to a uniform distribution of power loss among switches. A comparison is made between the proposed PI controller and the conventional PI controller to evaluate the effectiveness of the tuning scheme.

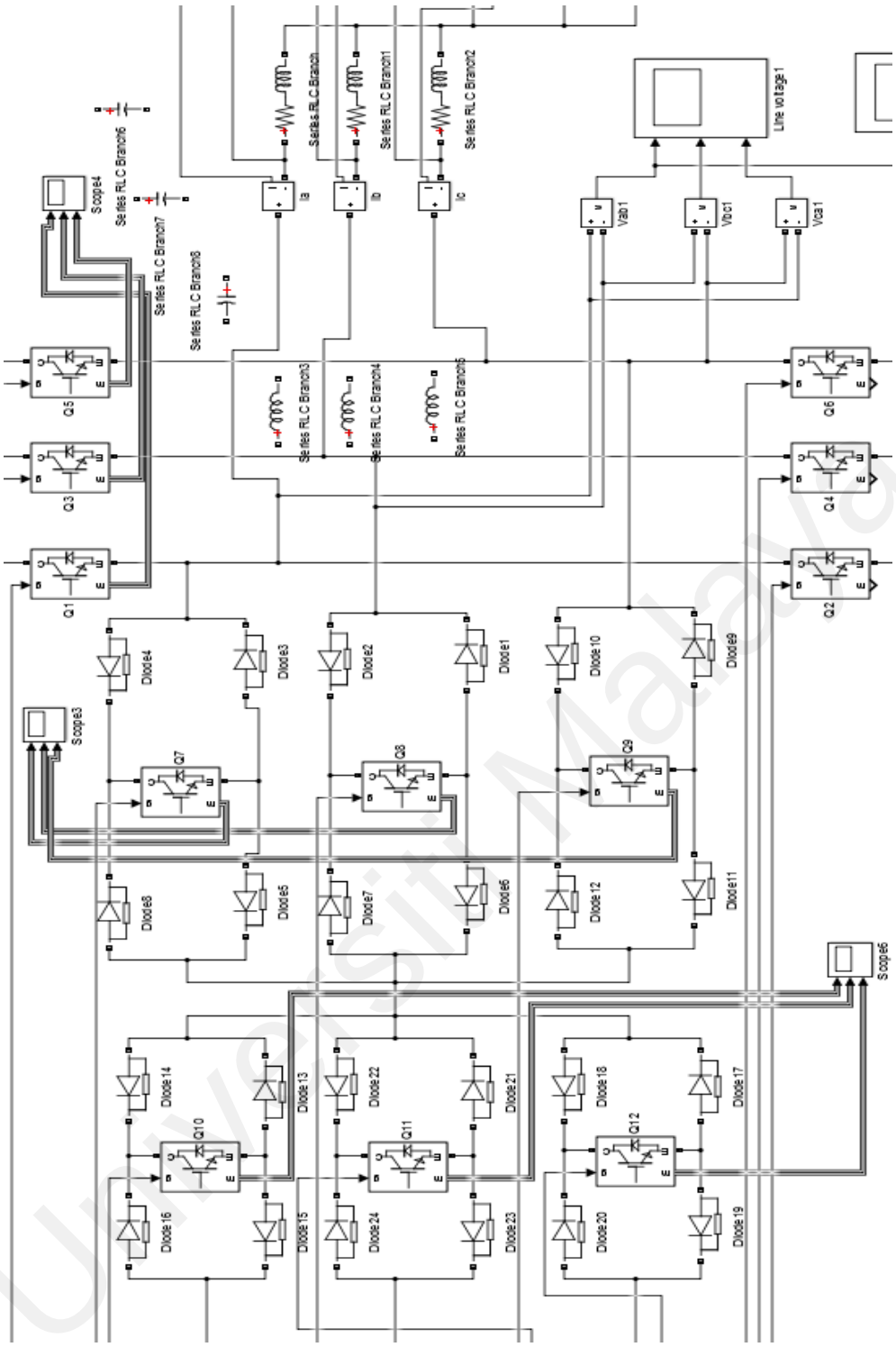


Figure 4.1: Circuit configuration of three-phase five-level switch-sharing-based multilevel inverter developed using MATLAB/SIMULINK.

Table 4.1: Parameters of the components use

Component	Values
DC capacitor	2200 µF
Inductance of buck-boost converter	12 mH
R load	120 Ohm
L load	69 mH
Five-level inverter modulation index, m_a	0.9

4.2 Conventional PI Controller

In this investigation, the gains are made constant at $K_{pU} = K_{pL} = 2$ and $K_{iU} = K_{iL} = 0.001$. Then, the output from the controller is compared with the carrier signal to generate the switching signals for the buck-boost converter. The operation modes of switches S_1 and S_2 are determined by the results of the comparison. Consequently, depending on S_1 and S_2 switching signals, C_1 and C_2 will start charging and discharging. In this simulation study, the carrier signal is set at 5 kHz. The results for the capacitor voltages and the dynamic performance of the controller and the impact on the inverter's output are analyzed.

4.2.1 Fixed Input Voltage

The fixed DC source, V_{dc} is set at 200 V. All capacitor voltages are kept the same to balance at the reference value of 50 V as shown in Figure 4.2. Figure 4.3 shows the line-to-line output voltage of phase A (V_{AB}) which generates nine voltage levels whereby the inverter phase voltage and output current also indicate satisfactory results. Meanwhile, THD of output current at phase A (I_A) is 3.77%, as portrayed in Figure 4.4. Figure 4.5 which shows the switching signals, indicates that switches S_1 and S_2 and S_3 and S_4 are complementary to each other.

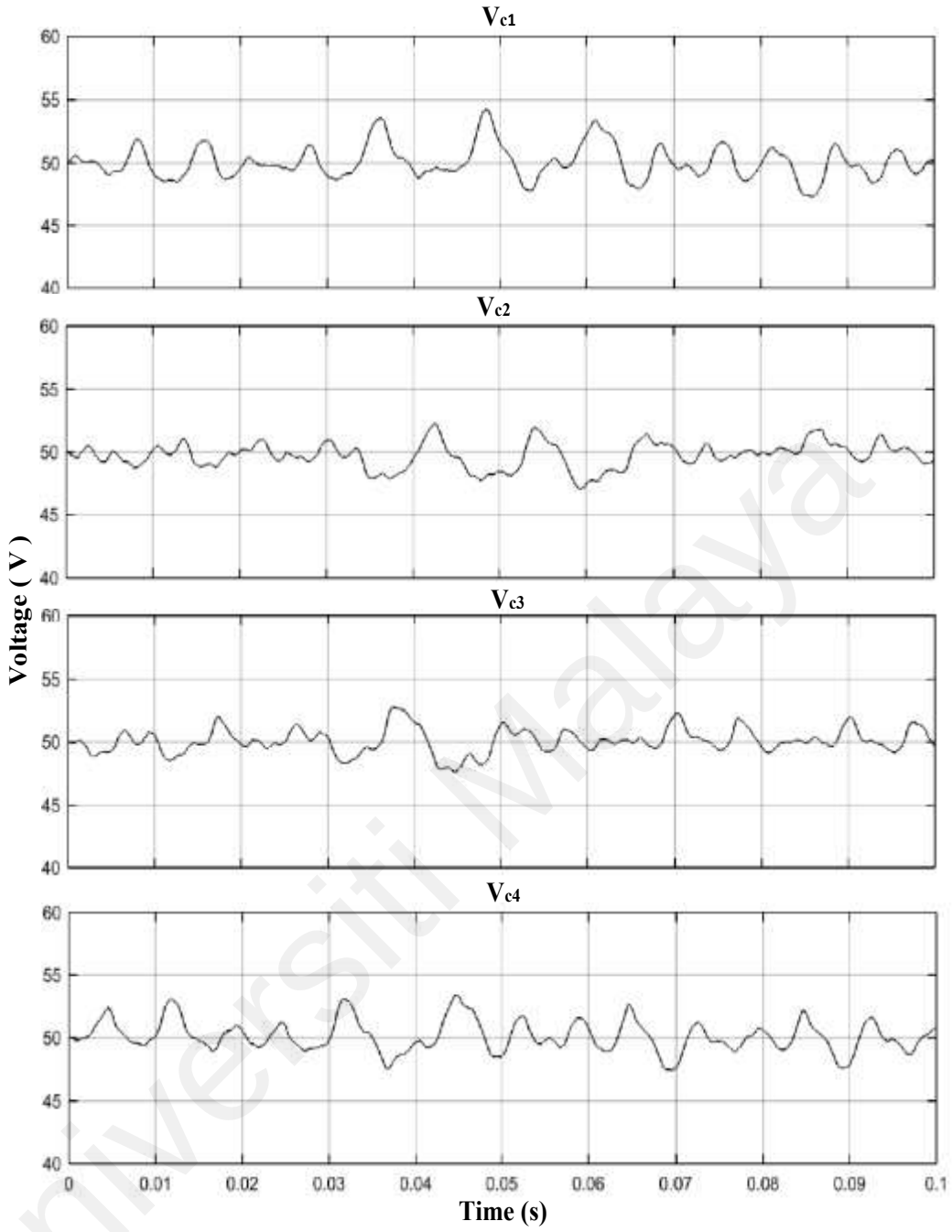


Figure 4.2: Simulation results of capacitor voltages (V_{c1}, V_{c2}, V_{c3}, V_{c4}) for a fixed input voltage (200 V) by using the conventional PI controller.

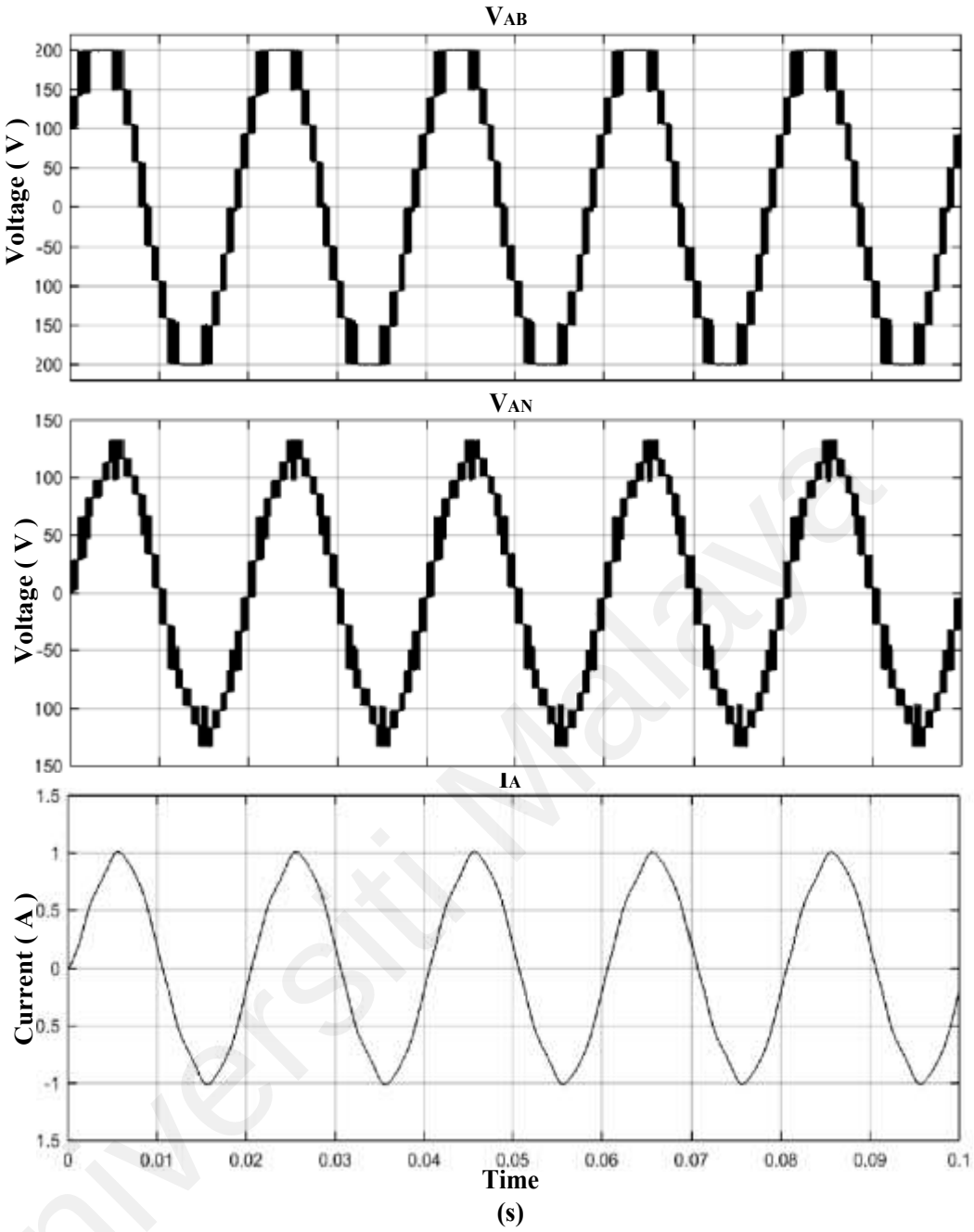


Figure 4.3: Simulation results of line-to-line output voltage (V_{AB}), phase voltage (V_{AN}) and output current (I_A) for a fixed input voltage (200 V) by using the conventional PI controller.

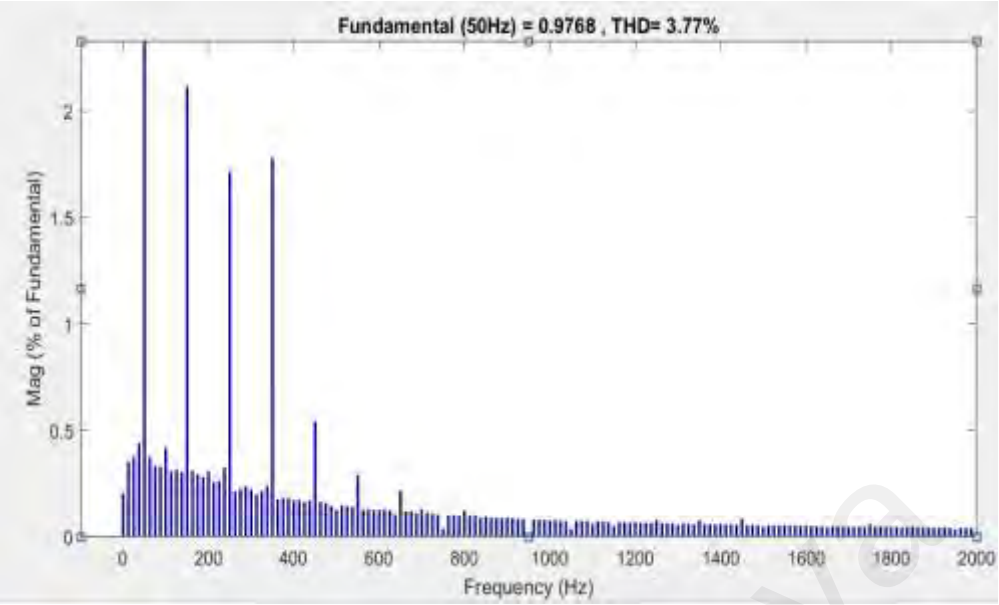


Figure 4.4: Simulation results of output current THD (I_A) for a fixed input voltage (200 V) by conventional using the PI controller.

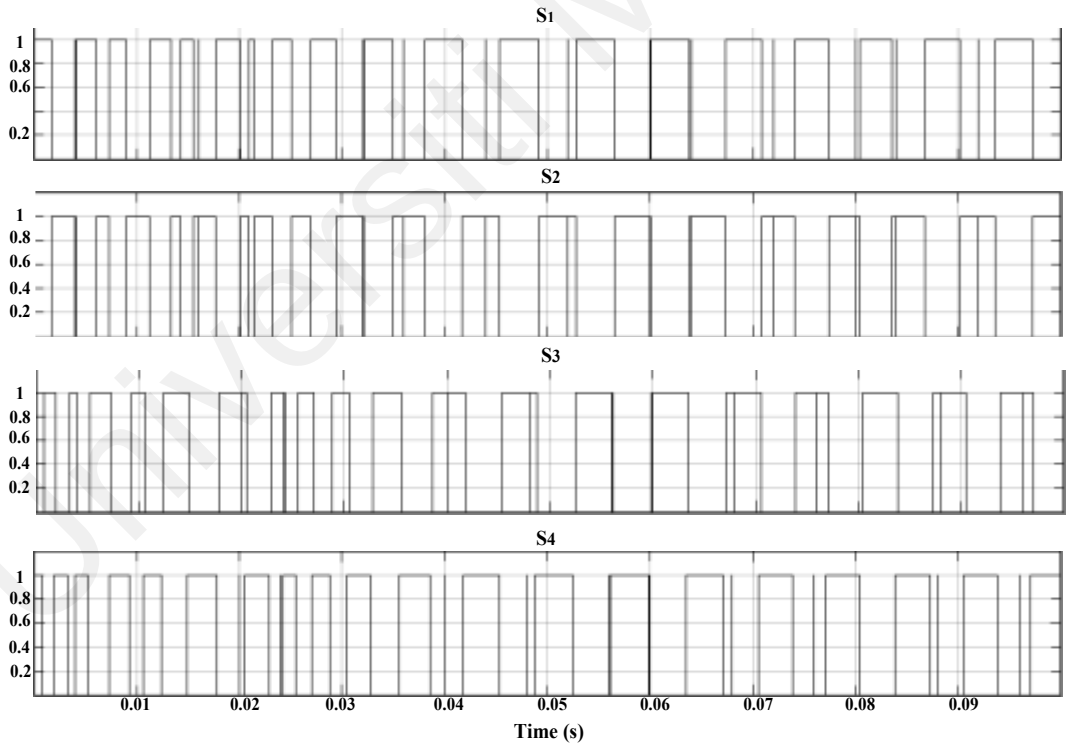


Figure 4.5: Simulation results of switching signals (S_1, S_2, S_3, S_4) for a fixed input voltage (200 V) by using conventional PI controller.

4.2.2 Variable Input Voltage

Simulation to study the performance of step response is carried out for further investigation on the ability of the capacitor's voltages to stabilize in dynamic conditions. The simulation is conducted for two conditions; the step-up and the step-down modes.

4.2.2.1 Step-Up Response

The step-up response is set to occur at t = 0.03 s as the variable DC source, V_{dc} changes from 60 V to 200 V. The change of input from the 60 V to 200 V at t = 0.03s has led all capacitor voltages to balance at the reference value from 15 V to 50 V as seen in Figure 4.6. Figure 4.7, shows that nine-level waveform is generated in the line-to-line output voltage which indicates that the buck-boost converter can perform at a high modulation index (0.9) for capacitor voltage balancing. Satisfactory performance during the step response is also observed for output line current (I_A) and inverter's output phase voltage (V_{AN}). The output current THD (I_A) is recorded as 3.51%, as shown in Figure 4.8. Figure 4.9 portrays the switching signals for variable input voltage for conditions. It shows that, switches S_1 and S_2 are complementary to each other and also S_3 and S_4 being complementary to each other.

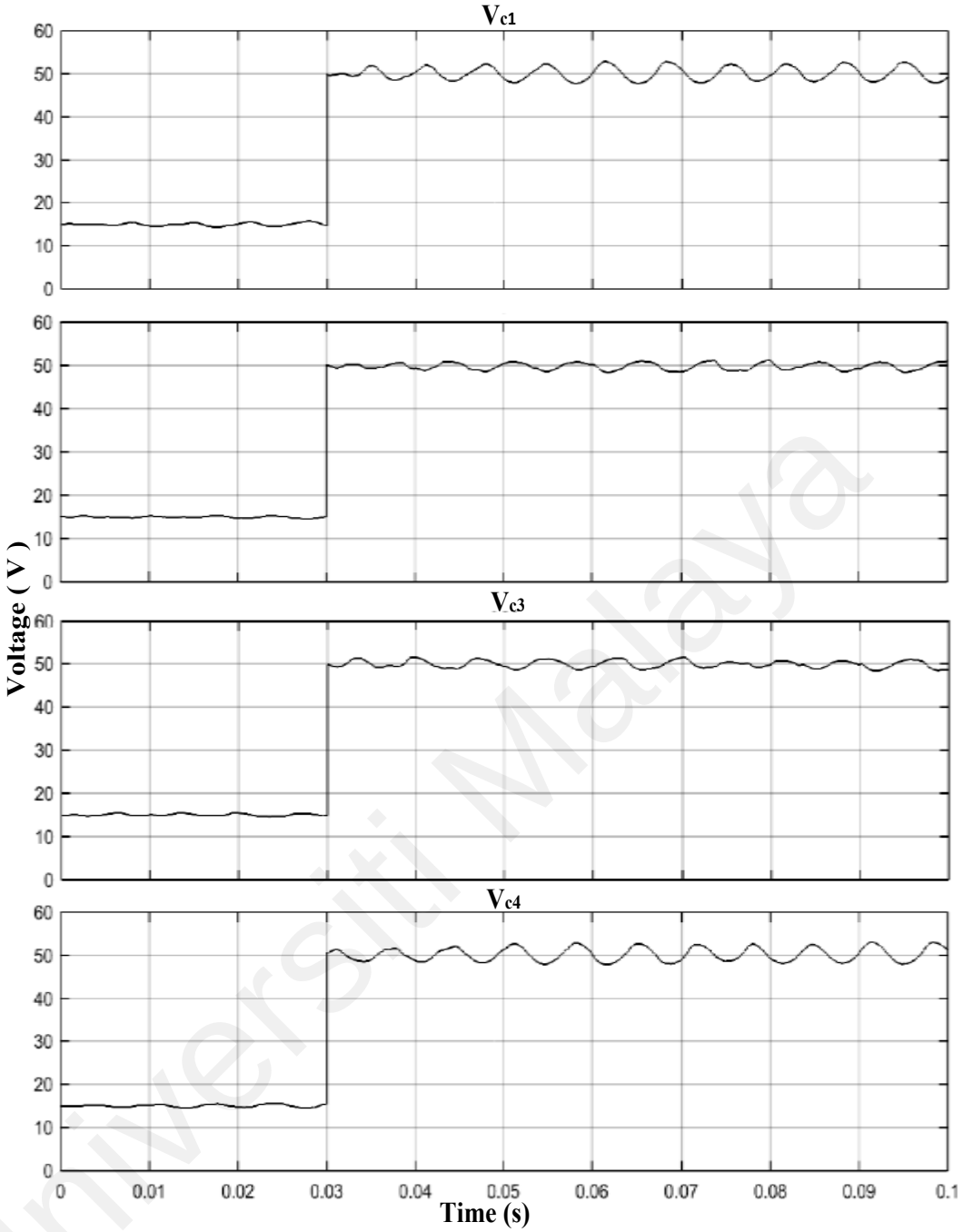


Figure 4.6: Simulation results of capacitor voltages (V_{c1}, V_{c2}, V_{c3}, V_{c4}) for step-up response (60 V - 200 V) by conventional using PI controller.

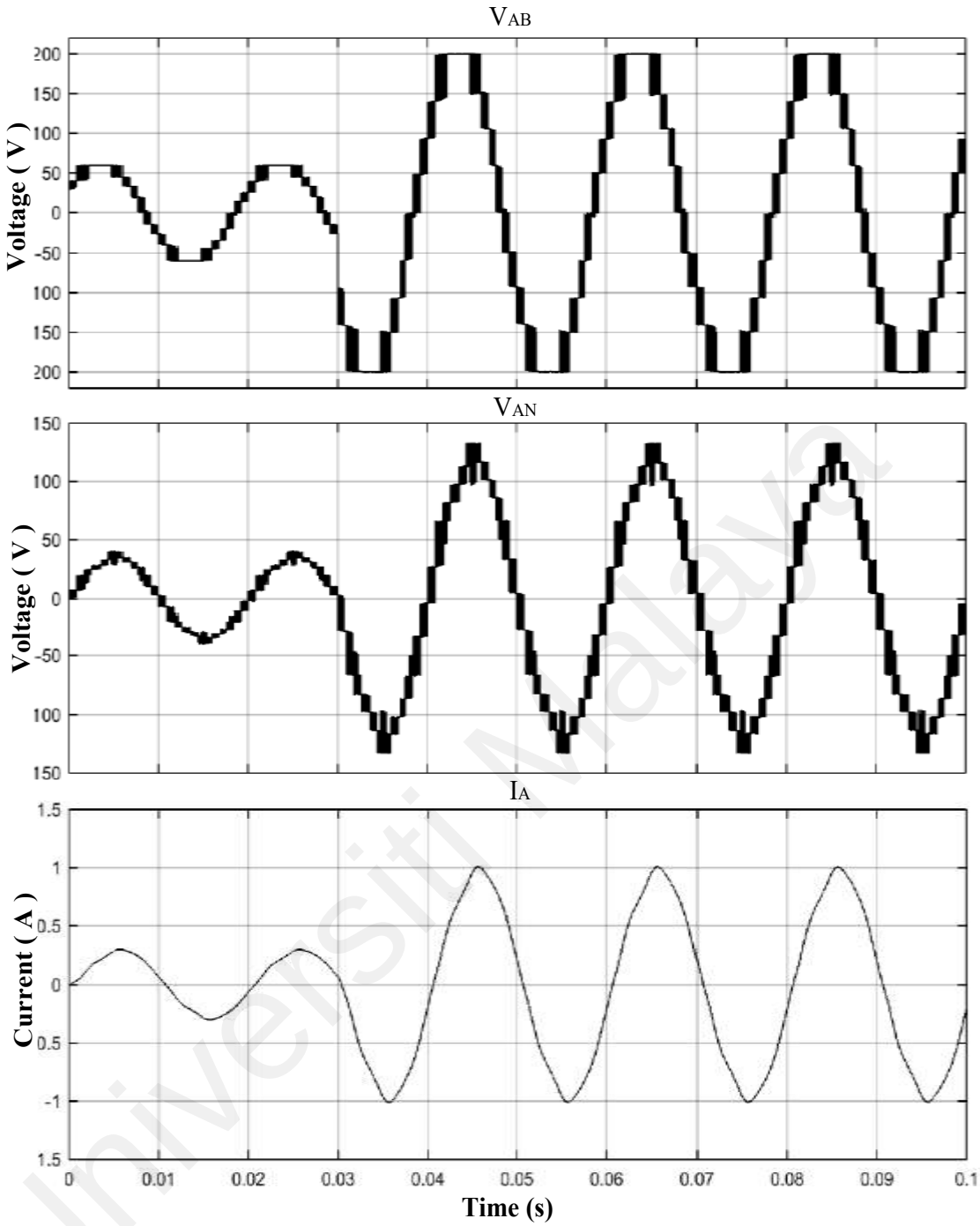


Figure 4.7: Simulation results of line-to-line output voltage (V_{AB}), phase voltage (V_{AN}) and output current (I_A) for step-up response (60 V - 200 V) by using the conventional PI controller.

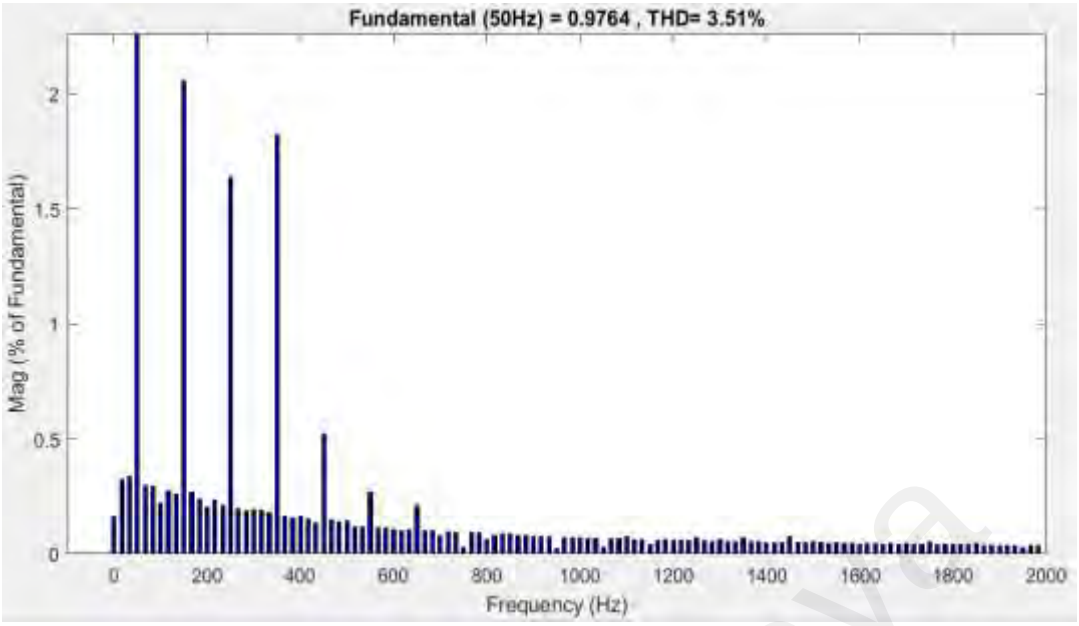


Figure 4.8: Simulation result of output current THD (I_A) after the step-up response (60 V - 200 V) by using the conventional PI controller.

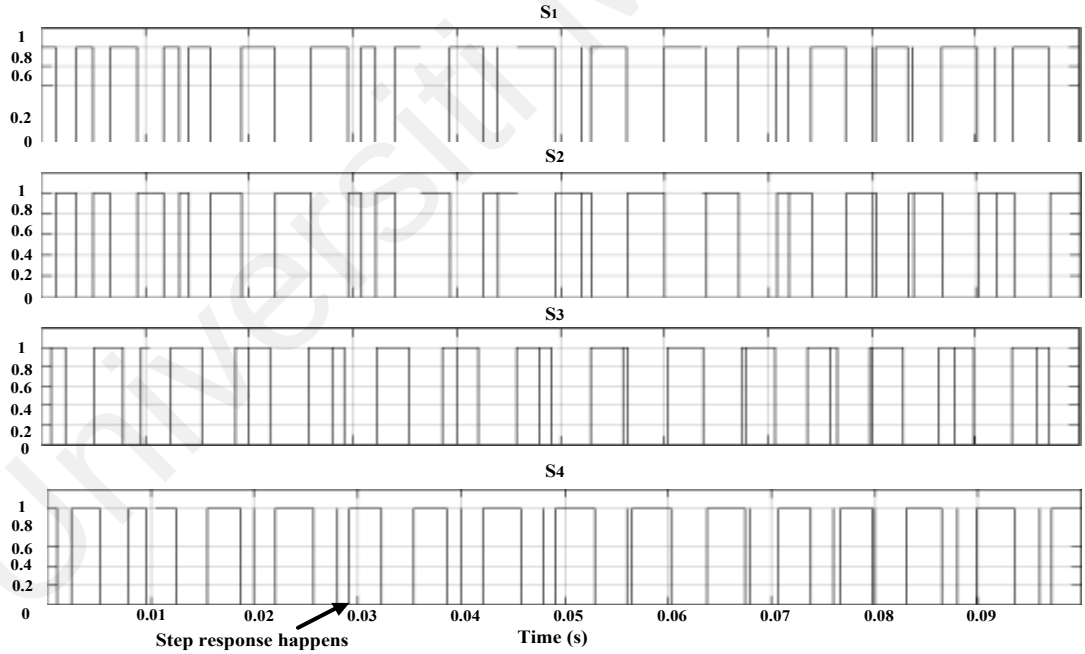


Figure 4.9: Simulation result of switching signal (S_1, S_2, S_3, S_4) for step-up response (60 V - 200 V) by using the conventional PI controller.

4.2.2.2 Step-Down Response

The DC source, V_{dc}, is set to vary from 200 V to 60 V with a step-down response that happens at t = 0.03 s. It can be observed from Figure 4.10 that when the input changes from 200 V to 60 V, all capacitor voltages can be balanced at the reference value from 50 V to 15 V.

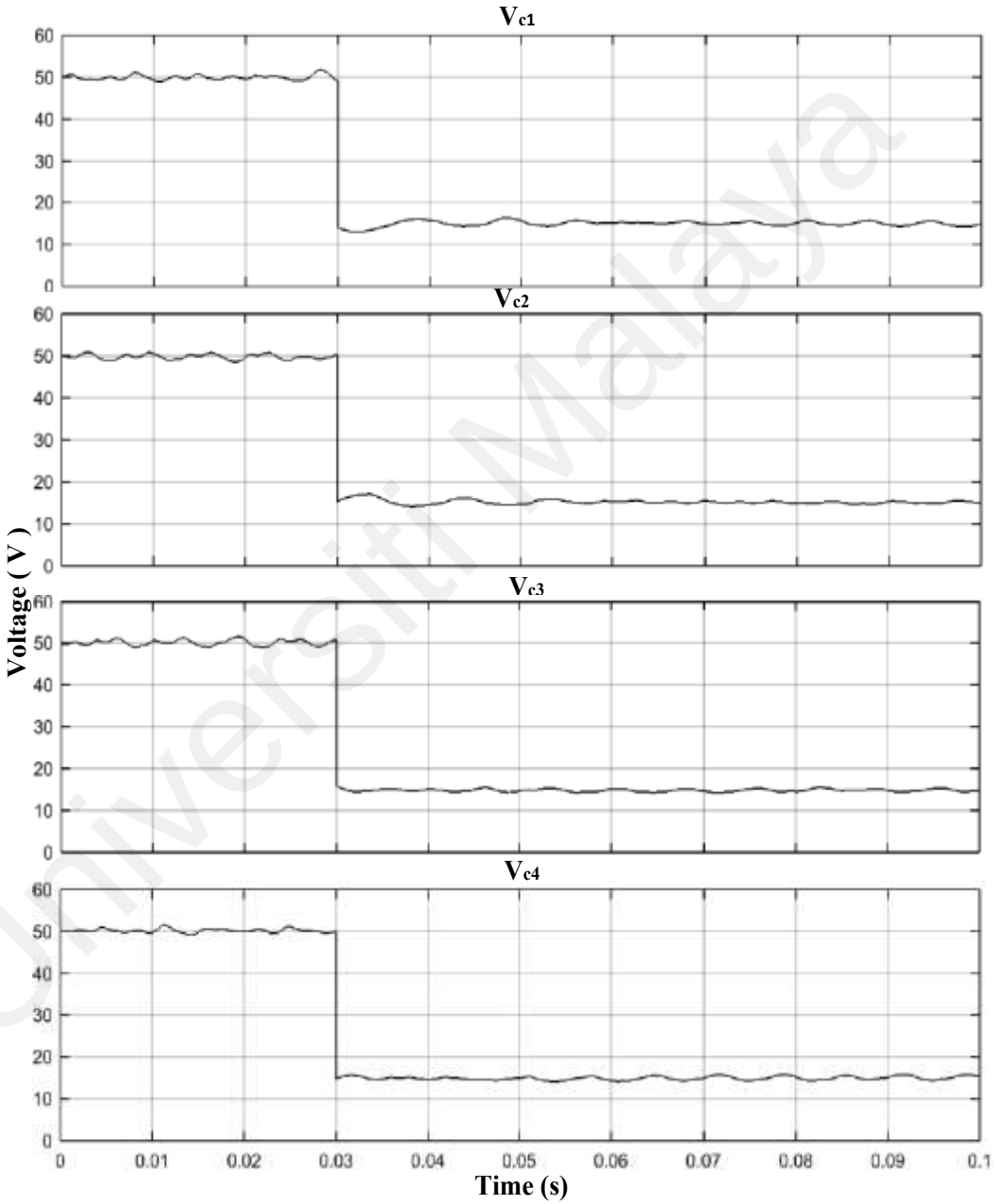


Figure 4.10: Simulation results of capacitor voltages (V_{c1}, V_{c2}, V_{c3}, V_{c4}) for step-down response (200 V - 60 V) by using the conventional PI controller.

The line-to-line output voltage (V_{AB}) portrays a satisfactory result since the nine-level waveform is successfully produced, as shown in Figure 4.11. Also, the inverter output phase voltage (V_{AN}) and output line current (I_A) show acceptable performance during the step response. After the step response, the output current THD is measured as 3.21%, as shown in Figure 4.12. Meanwhile, Figure 4.13 displays the switching signals (S_1 and S_2) that complement each other and switch signals (S_3 and S_4).

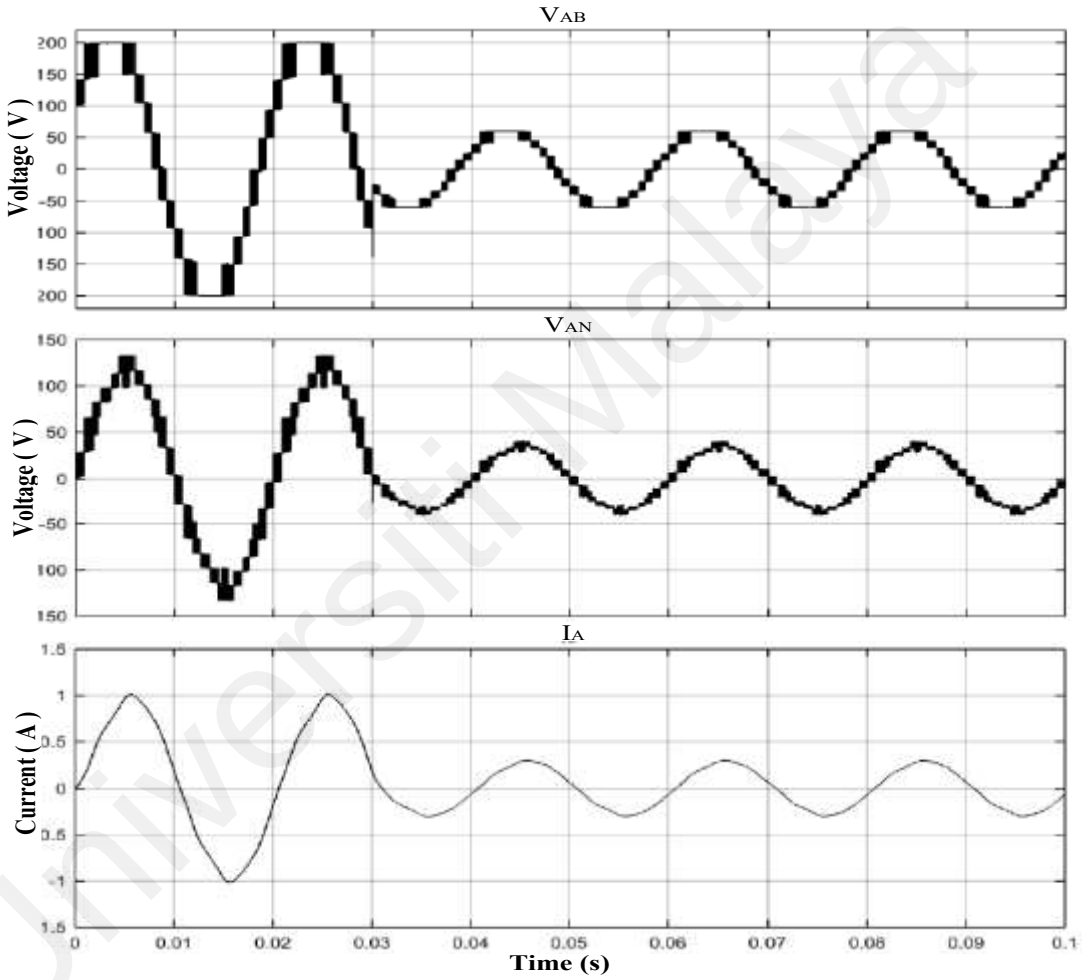


Figure 4.11: Simulation results of line-to-line output voltage (V_{AB}), phase voltage (V_{AN}) and output current (I_A) for step-down response (200 V - 60 V) by the using conventional PI controller.

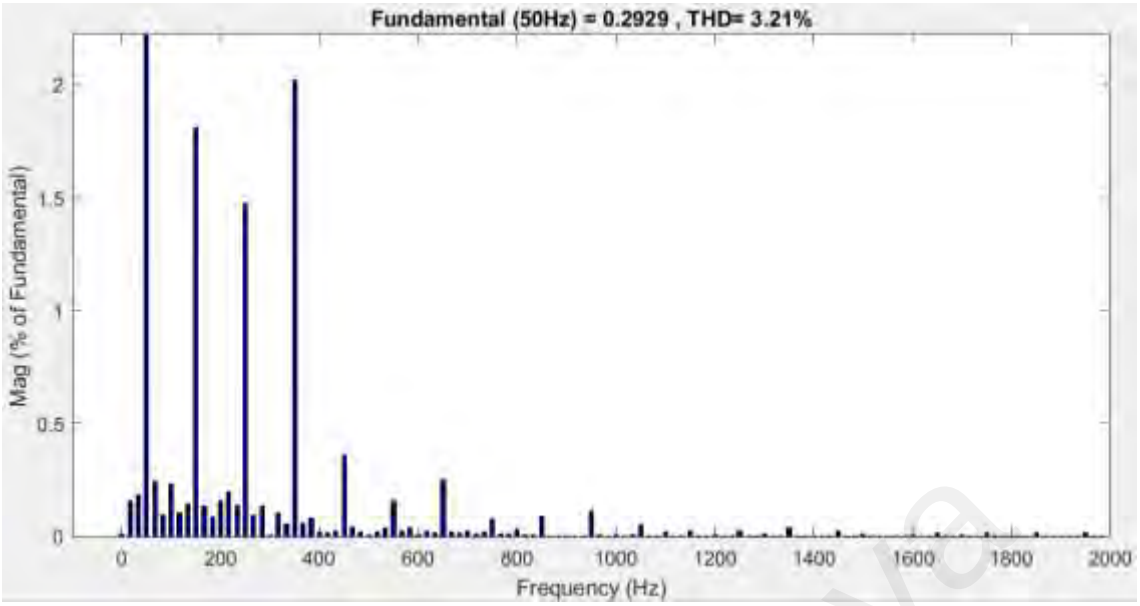


Figure 4.12: Simulation result of output current THD (I_A) after the step-down response (200 V - 60 V) by using the conventional PI controller.

Figure 4.13: Simulation results of switching signals (S_1, S_2, S_3, S_4) for step-down response (200 V - 60 V) by using conventional PI controller.

4.3 Proposed PI Controller with Performance-Based Online Tuning Mechanism

In this work, to explore the controller's response, a proposed PI controller with the performance-based online tuning mechanism is developed. Furthermore, an additional MATLAB program code is prepared via a new "embedded MATLAB function" block. The additional MATLAB program code refers to a program code for the additional online tuning module in the controller's structure. It is used to calculate the proportional gains (K_{pU} and K_{pL}) of the controllers at both parts of the circuits when the input voltage changes while K_{iU} and K_{iL} are kept at 0.001, as described in Section 3.3.2. Like the conventional PI controller, the performance of the proposed PI controller is also investigated under a steady-state and dynamic conditions. Therefore, simulation is conducted for both fixed input voltage and variable input voltage situations.

4.3.1 Fixed Input Voltage

The fixed DC source, V_{dc}, is fixed at 200 V. The time duration for the simulation is 0.1 s. All capacitor voltages are kept to maintain the balance at the reference value of 50 V, as indicated in Figure 4.14. From Figure 4.15, it is observed that the line-to-line output voltage shows nine voltage levels (V_{AB}), and a satisfying result is also obtained for the inverter phase voltage (V_{AN}) and output current (I_A). Figure 4.16 shows that the output current THD is recorded as 3.77%. Meanwhile, Figure 4.17 shows the switching signals for all power switches at both parts of the circuit.

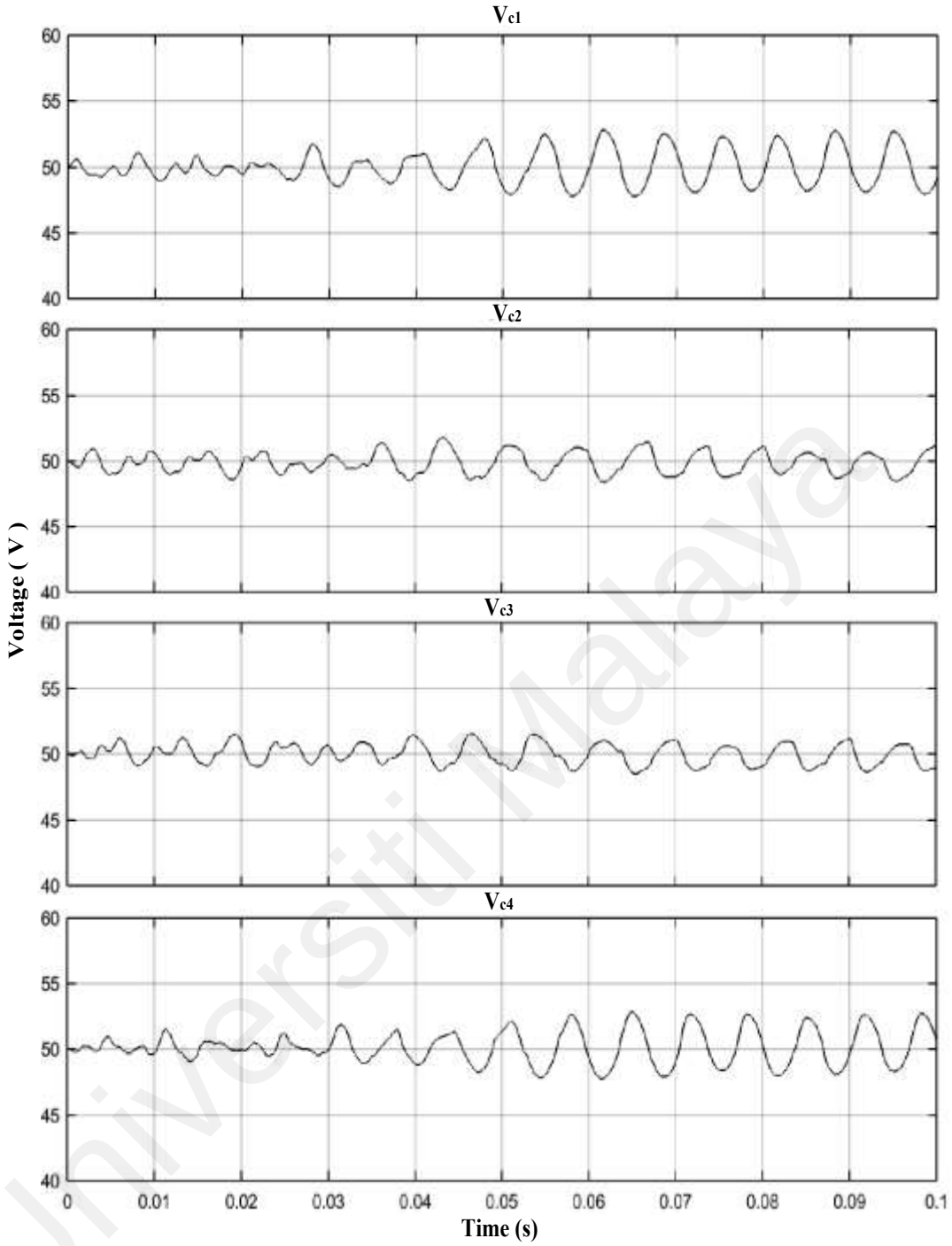


Figure 4.14: Simulation results of capacitor voltages (V_{c1}, V_{c2}, V_{c3}, V_{c4}) for a fixed input voltage (200 V) by using proposed PI controller.

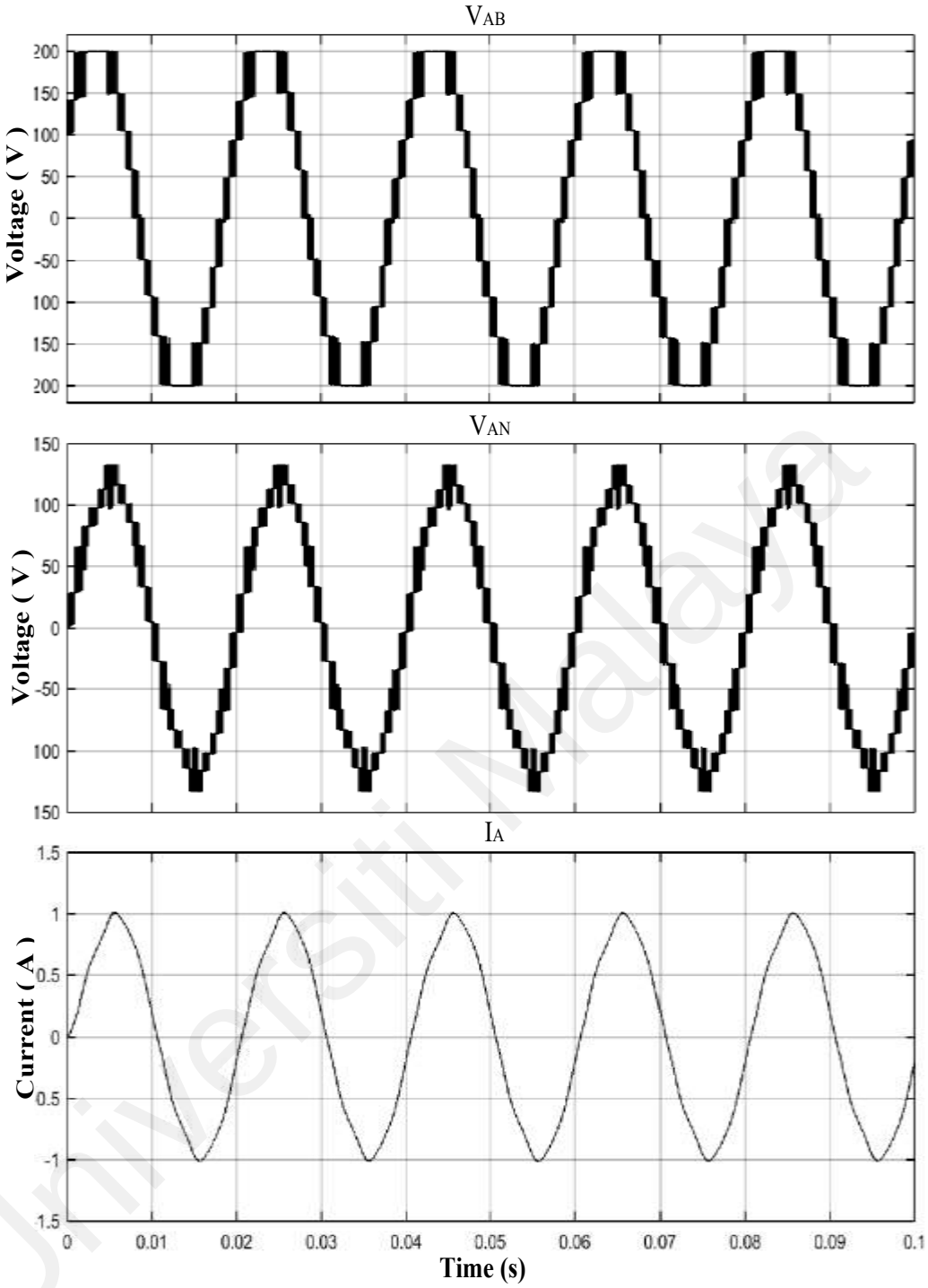


Figure 4.15: Simulation results of line-to-line output voltage (V_{AB}), phase voltage (V_{AN}) and output current (I_A) for a fixed input voltage (200 V) by using proposed PI controller.

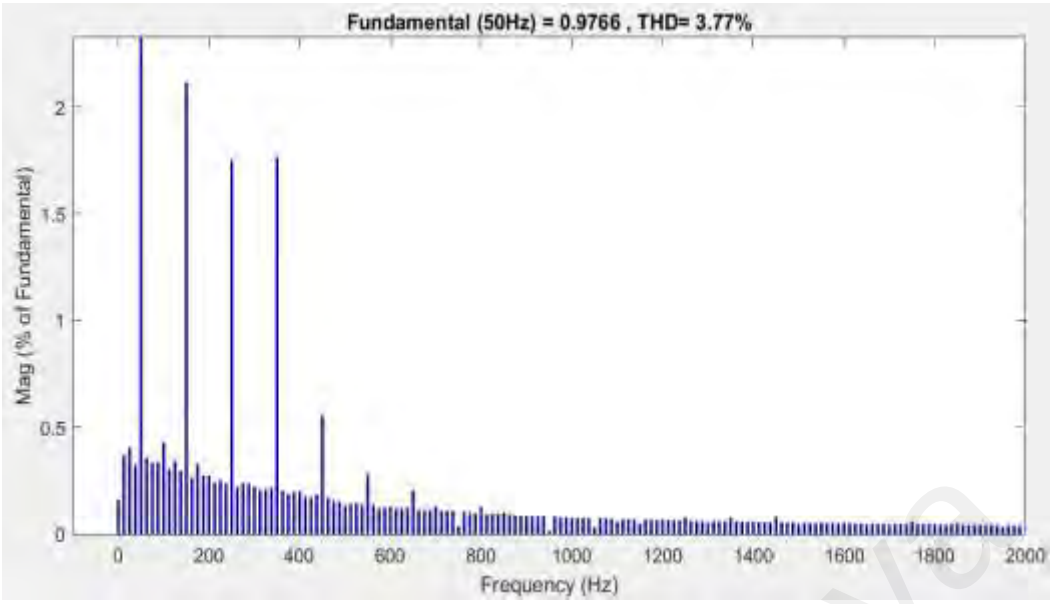


Figure 4.16: Simulation result of output current THD (I_A) for a fixed input voltage (200 V) by using the proposed PI controller.

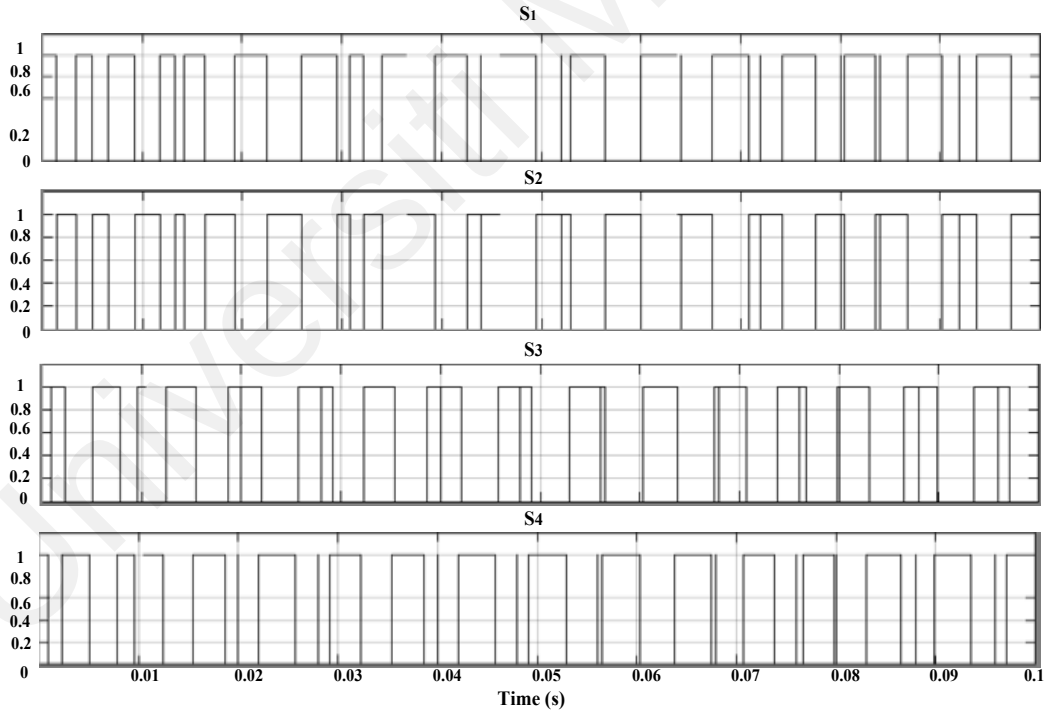


Figure 4.17: Simulation results of switching signals (S_1, S_2, S_3, S_4) for a fixed input voltage (200 V) by using the proposed PI controller.

4.3.2 Variable Input Voltage

A simulation study for step response is conducted for two conditions, the step-up and the step-down modes to validate the effectiveness of proposed PI controller.

4.3.2.1 Step-Up Response

The variable DC source, V_{dc}, changes from 60 V to 200 V, in which step-up response occurs at t = 0.03 s. Figure 4.18 proved that the proposed PI controller also could balance all capacitor voltages at the reference value from 15 V to 50 V. The line-to-line output voltage (V_{AB}) can produce nine-level voltage waveform as well as inverter phase output (V_{AN}) and output current (I_A) give the desired result as shown in Figure 4.19. Meanwhile, output current THD (I_A) is recorded as 3.14% as shown in Figure 4.20. Figure 4.21 indicates that the switching signals (S_1 and S_2) and (S_3 and S_4) complement each other.

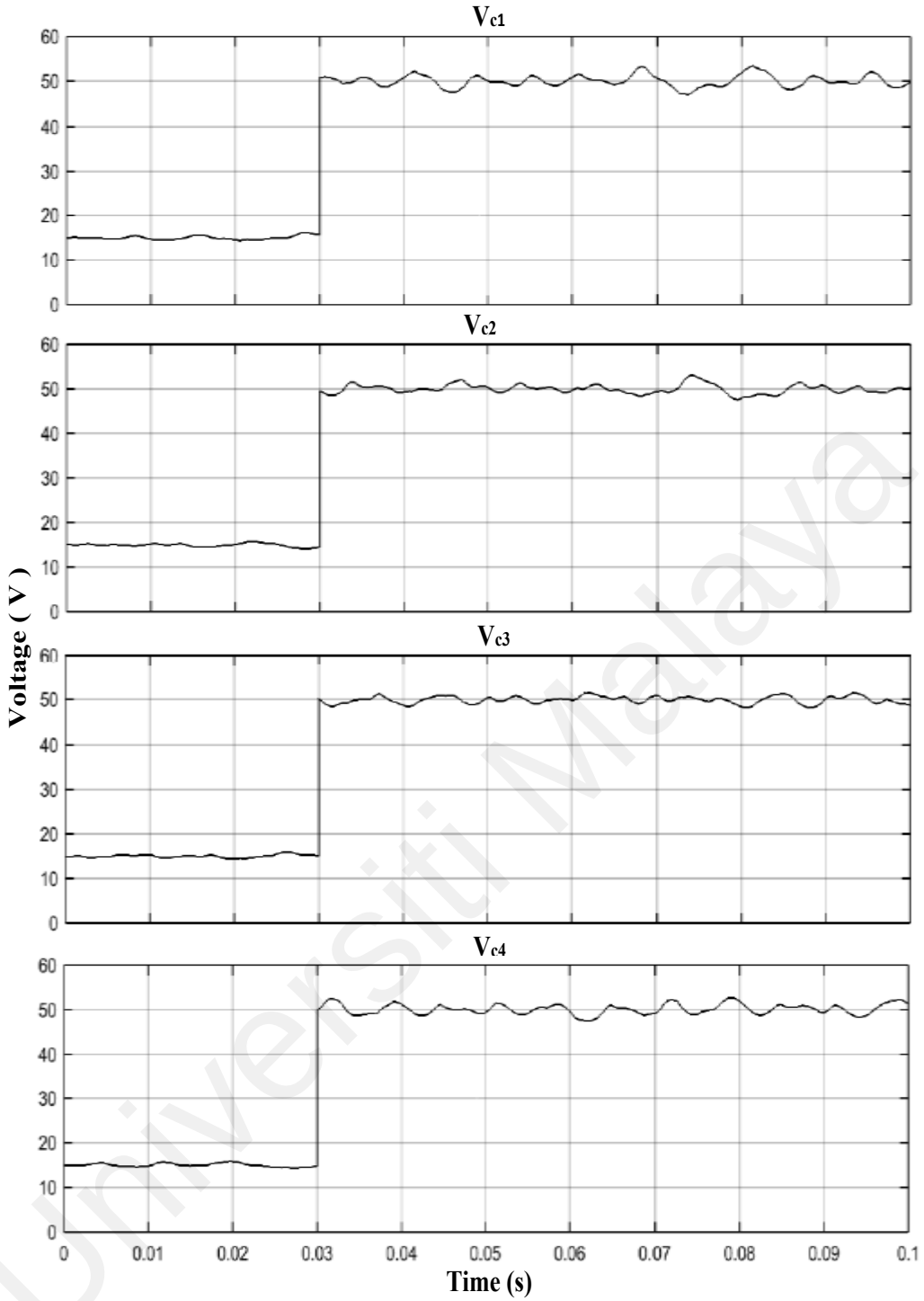


Figure 4.18: Simulation results of capacitor voltages (V_{c1}, V_{c2}, V_{c3}, V_{c4}) for step-up response (60 V - 200 V) by the using proposed PI controller.

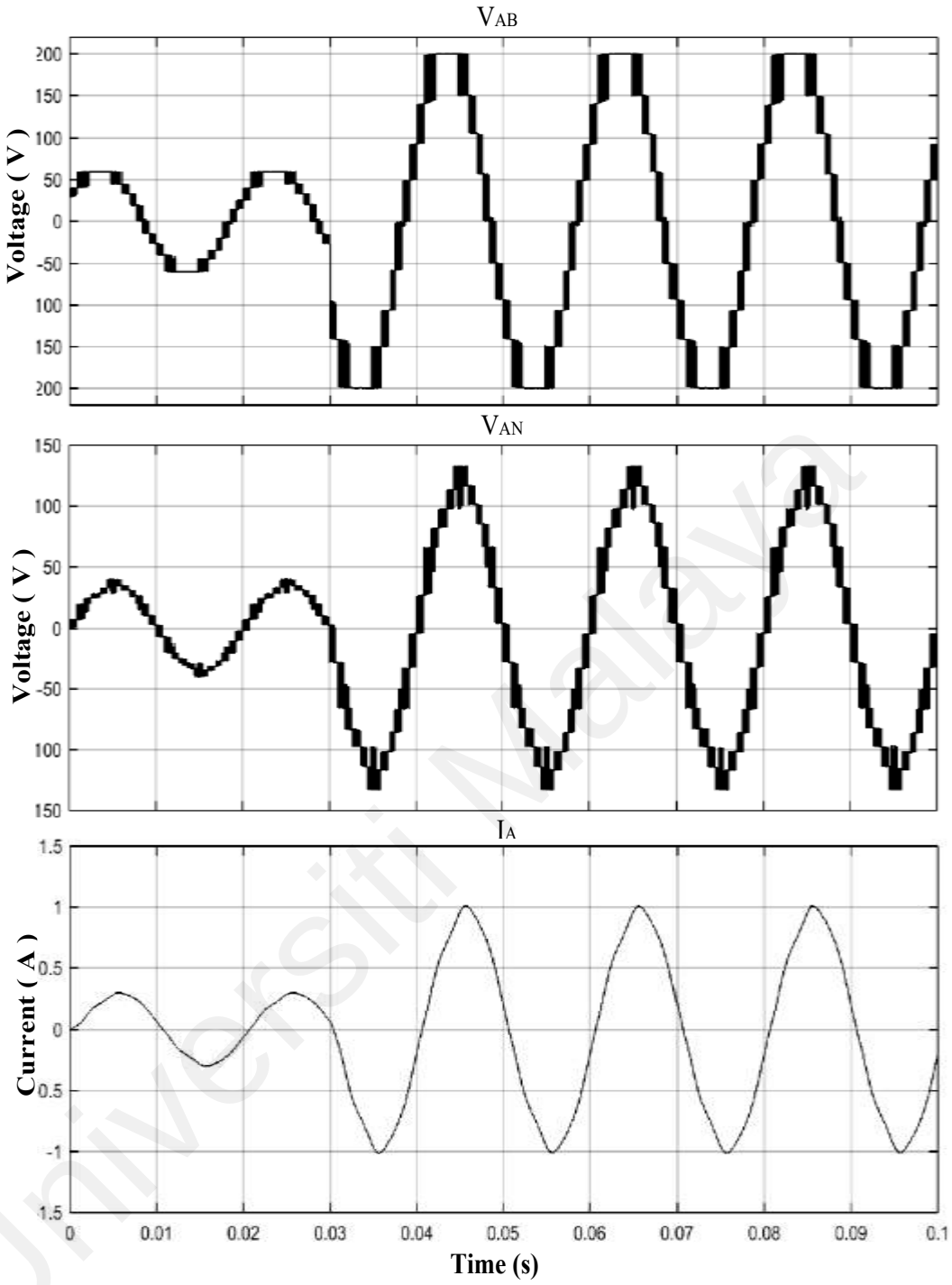


Figure 4.19: Simulation results of line-to-line output voltage (V_{AB}), phase voltage (V_{AN}) and output current (I_A) for step-up response (60 V - 200 V) by using proposed PI controller.

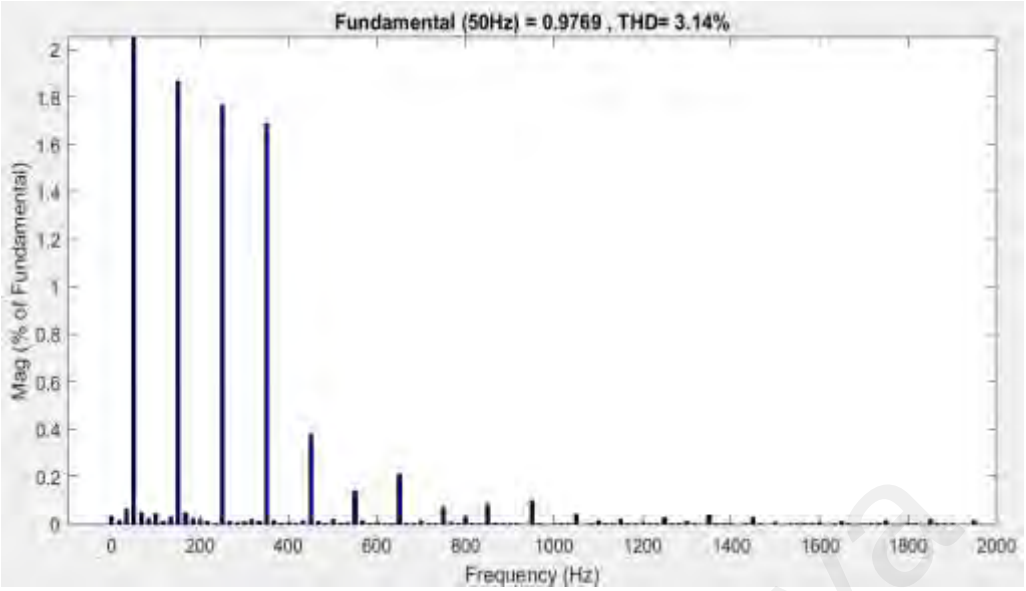


Figure 4.20: Simulation result of output current THD (I_A) after step-up response (60 V - 200 V) by using proposed PI controller.

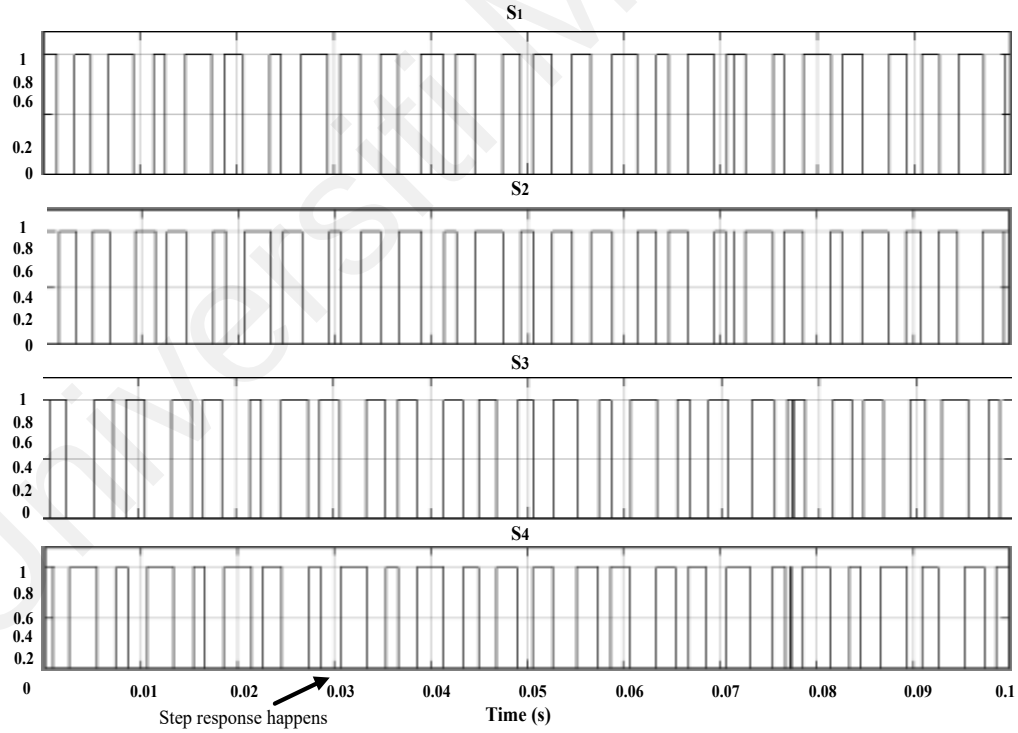


Figure 4.21: Simulation results of switching signals (S_1, S_2, S_3, S_4) for step-up response (60 V - 200 V) by using the proposed PI controller.

4.3.2.2 Step-Down Response

Figure 4.22 shows all capacitor voltages can be balanced at the reference value from 50 V to 15 V when the input changes from 200 V to 60 V at t = 0.03 s. A nine-level waveform is successfully produced at the line-to-line output voltage (V_{AB}), as portrayed in Figure 4.23. Besides, the inverter output phase voltage (V_{AN}) and output line current (I_A) also depict satisfactory performance during the step response. The output current THD (I_A) is recorded as 3.19%, as shown in Figure 4.24. The switches at both parts of the circuit are recorded to be complementary between S_1 and S_2 and S_3 and S_4 as shown in Figure 4.25.

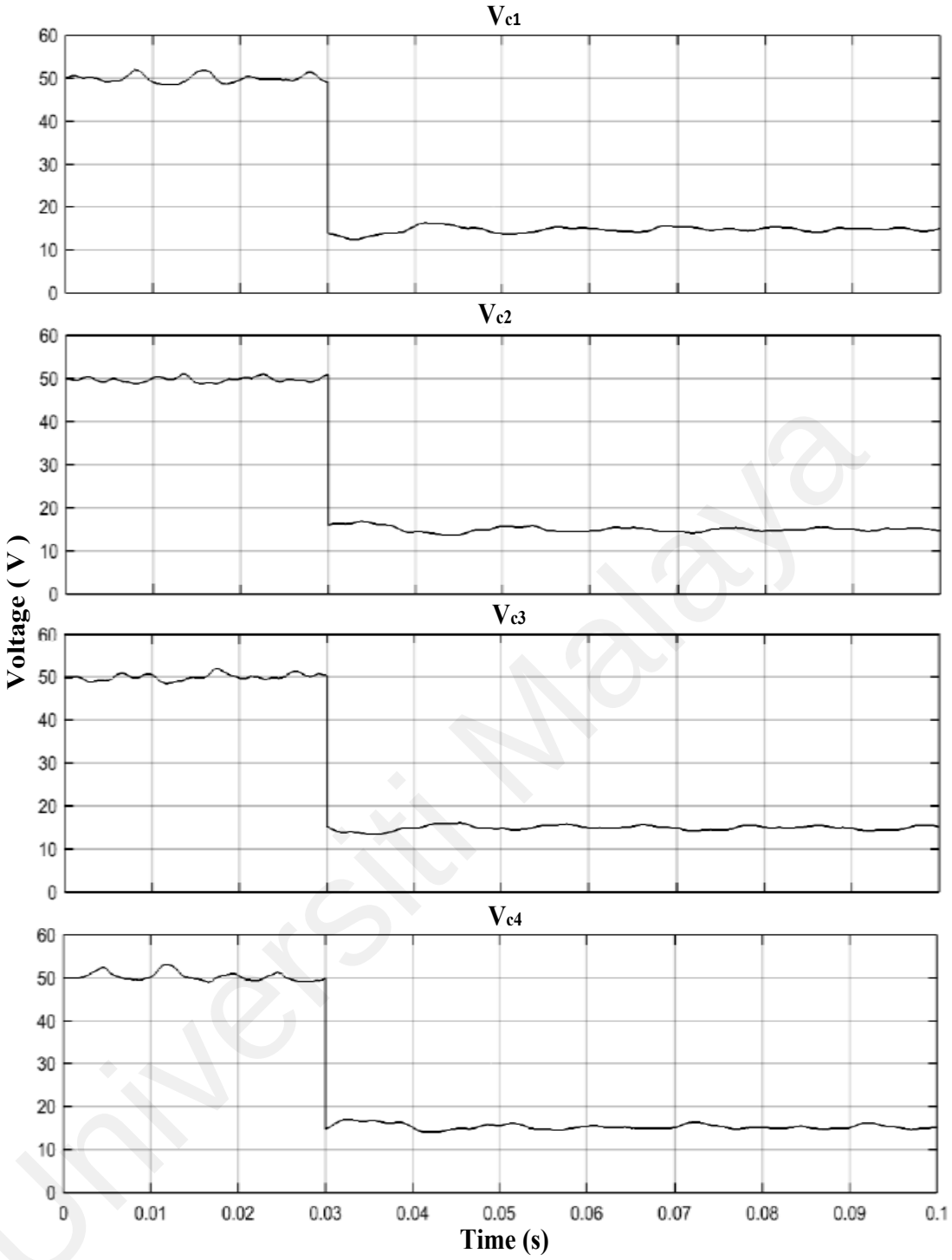


Figure 4.22: Simulation result of capacitor voltages (V_{c1}, V_{c2}, V_{c3}, V_{c4}) for step-down response (200 V - 60 V) by using proposed PI controller.

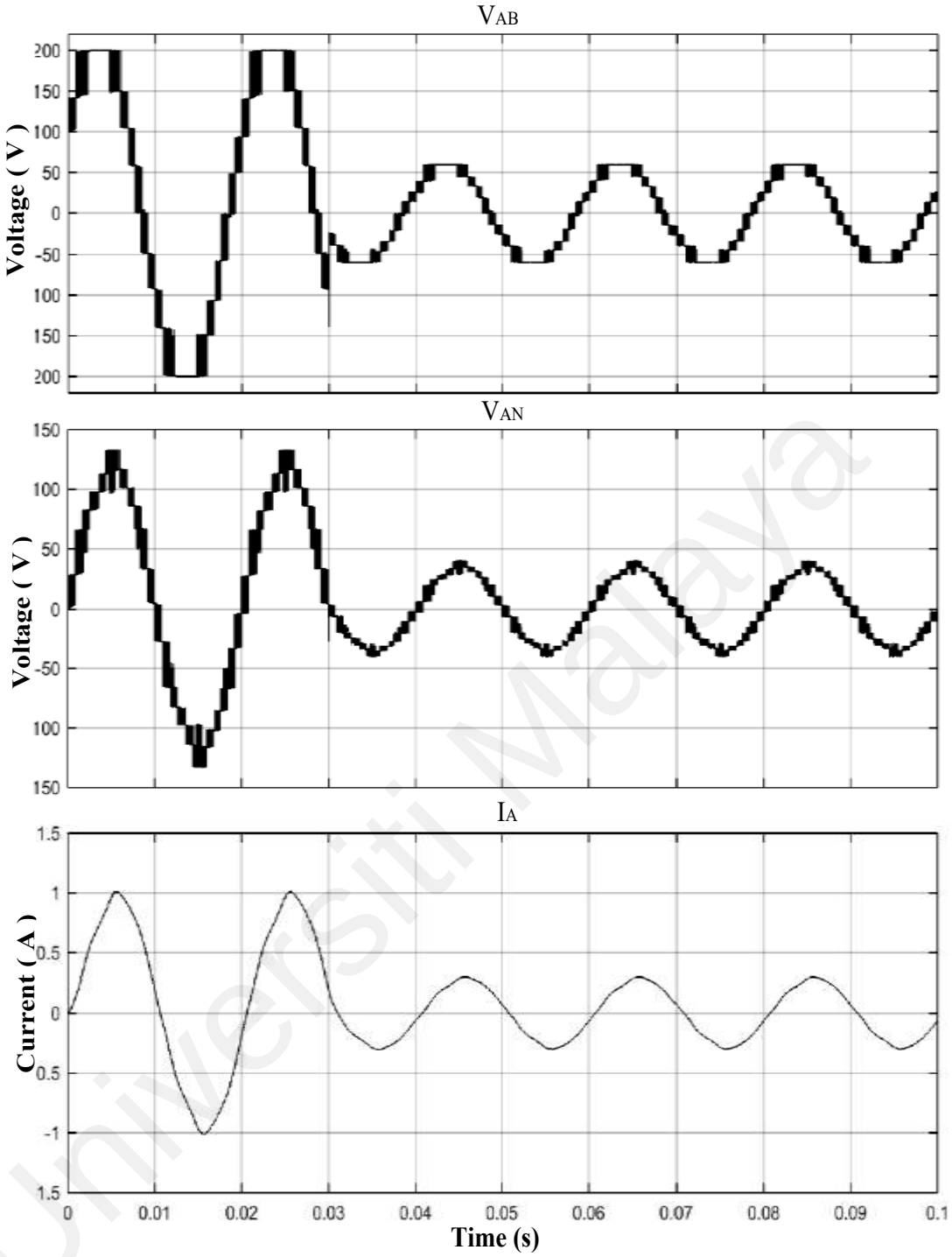


Figure 4.23: Simulation results of line-to-line output voltage (V_{AB}), phase voltage (V_{AN}) and output current (I_A) for step-down response (200 V - 60 V) by using proposed PI controller.

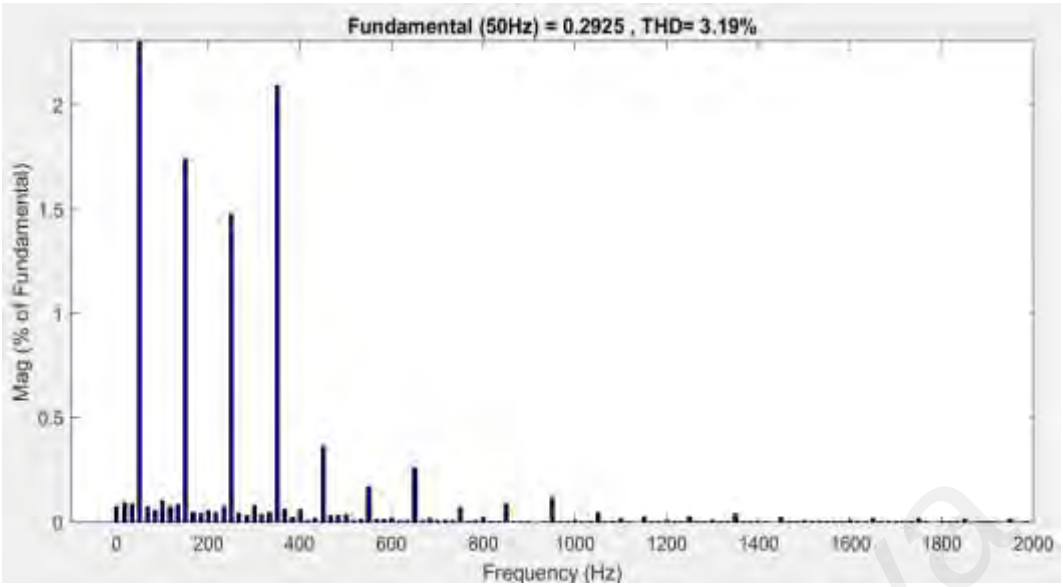


Figure 4.24: Simulation result of output current THD (I_A) after the step-down response (200 V - 60 V) by using the proposed PI controller.

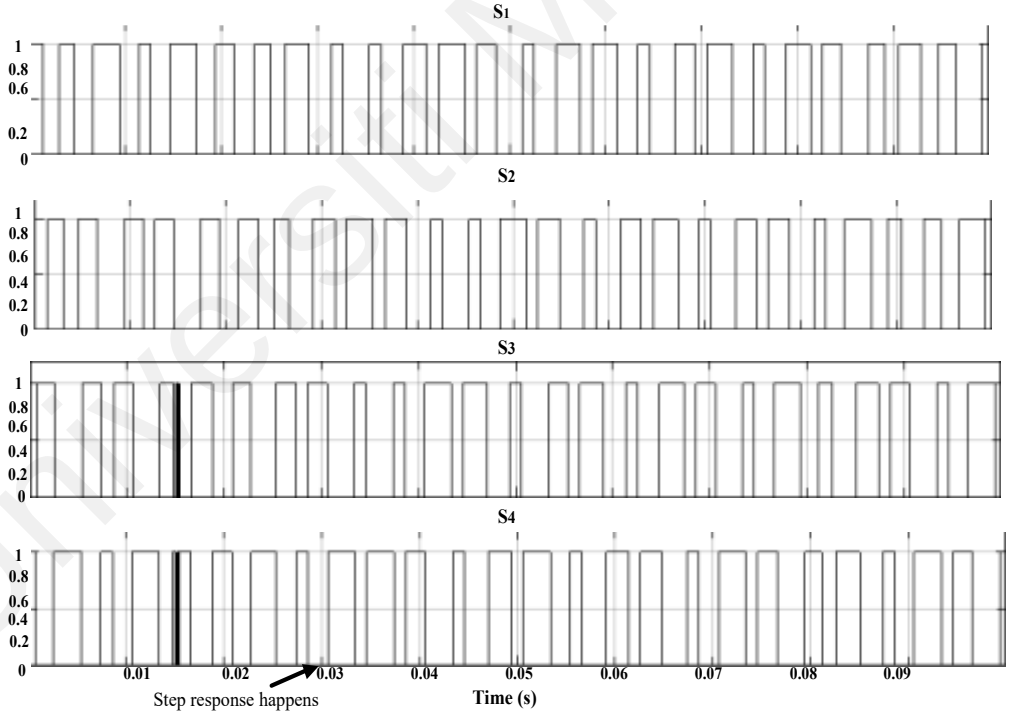


Figure 4.25: Simulation results of switching signals (S_1, S_2, S_3, S_4) for the step-down response (200 V - 60 V) by using the proposed PI controller.

4.4 Comparative Analysis

The simulation results show that all capacitor voltages can be balanced even after a change in input voltage. The inverter's output shows satisfactory results as the line-to-line voltage can produce nine voltage levels in the waveform and the phase output voltage (V_{AN}) and output current (I_A) indicate a good result. It is observed that the capacitor voltage ripple with the use of proposed online tuning mechanism is estimated at 2 V in terms of magnitude whereas the capacitor voltage ripple without online tuning mechanism is around 4 V. In addition, after the input voltage change, the output current THD is recorded to be lower than that when there is no application of the online tuning algorithm. The results show only 3.14% (with online tuning algorithm) compared to without online tuning, which is recorded as 3.51%. This indicates that the online tuning algorithm is an advantageous mechanism to enhance the THD of the output current, especially in a dynamic environment. The significance of the online tuning mechanism is verified by the simulation results, showing improved quality of the output current. Table 4.1 summarize the comparison between the two controllers.

Table 4.2: Comparative analysis between two controllers.

	Conventional PI controller	Proposed PI controller
Ripple voltage (V)	4	2
THD of output current (%)	3.51	3.14

4.5 Simulation for Power Loss and Efficiency

Power loss is emphasized in calculating conduction loss and switching loss because of the small off-state loss (Patra et al., 2018). Therefore, the off-state loss is assumed negligible in this analysis. By analyzing the characteristic curves found in the individual power device's datasheet, the respective power losses can be approximated. Mathematical equations reflecting the curves can be acquired from the appropriate characteristic curves obtained from the datasheet (Baskar, 2014). To calculate the conduction loss, an equation relating the conducted current to the forward voltage drop across the device is used. From the energy loss curve versus current, the switching loss of the power switching device has been estimated. This is due to the turn-on and turn-off commutation along with the freewheeling diode's reverse recovery. This analysis uses the power switch as the IGBT model IRG4PC40UDPbF from International Rectifier. Relevant points are extracted from the IGBT datasheet to obtain several curves for the calculation of the losses. The mathematical models for the IGBT have been derived from a MATLAB curve-fitting tool as given below:

$$V_{CE} = 3.141e^{0.003496i(t)} - 2.296e^{-0.01392i(t)} \quad (4.1)$$

$$V_{FW} = 1.396e^{0.009157i(t)} - 0.5844e^{-0.1733i(t)} \quad (4.2)$$

$$E_{SL,IGBT} = 15.62(e^{0.009769i(t)} - e^{0.009764i(t)}) \quad (4.3)$$

Here, V_{FW} is the forward voltage drop, V_{CE} is the collector-to-emitter voltage, $E_{SL,IGBT}$ is the sum of the IGBT switching energy loss, and i(t) is the current flowing via the IGBT. To determine the conduction loss of the IGBT, the equations are used as follows:

$$P_{CL,Diode} = \frac{1}{T_{PO}} \int V_{FW}\, i(t)\, dt \quad (4.4)$$

$$P_{CL,IGBT} = \frac{1}{T_{PO}} \int V_{CE}\, i(t)\, dt \quad (4.5)$$

Here, $P_{CL,Diode}$ and $P_{CL,IGBT}$ are the diodes and IGBTs conduction losses, and T_{PO} is the period for one cycle. The overall IGBTs switching power loss, $P_{SL,IGBT}$ is given as follows:

$$P_{SL,IGBT} = \frac{1}{T_{PO}} \sum E_{SL,IGBT} \tag{4.6}$$

By multiplying the reverse recovery time with the reverse recovery current as well as the reverse voltage drop, the switching loss of diode, $E_{SL,DIODE}$ can be estimated, which results in:

$$E_{SL,DIODE} = (16.2e^{0.003252i(t)} - 10.4e^{-0.076497i(t)} - 1.815e^{-0.076441i(t)} + 1.166e^{-0.1562i(t)}) \, x \, 10^{-6} \tag{4.7}$$

Subsequently, the total switching power loss of diodes, $P_{SL,DIODE}$ is determined as follows:

$$P_{SL,DIODE} = \frac{1}{T_{PO}} \sum E_{SL,DIODE} \tag{4.8}$$

The sum of conduction and switching losses is known as the total power loss, P_L and is represented as follows:

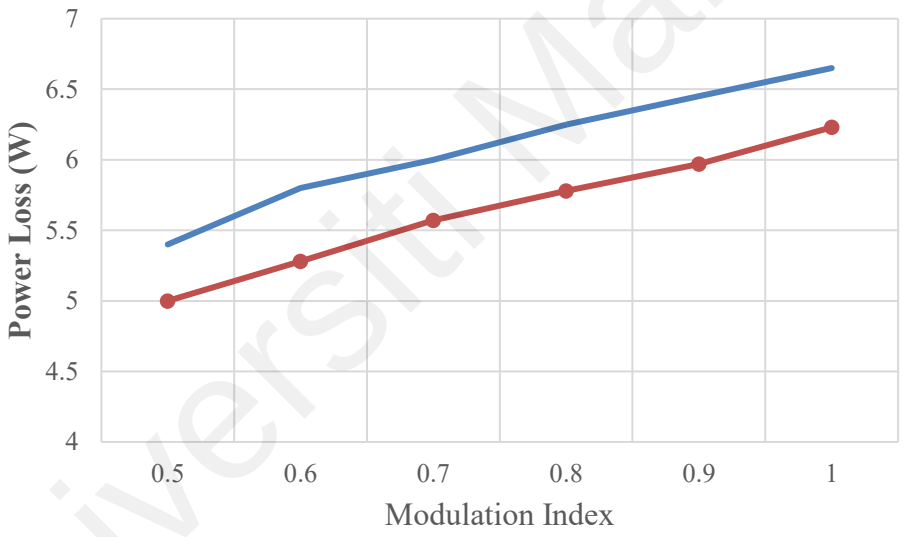
$$P_L = P_{CL,DIODE} + P_{CL,IGBT} + P_{SL,DIODE} + P_{SL,IGBT} \tag{4.9}$$

To calculate the efficiency, η of the converter, the following equation is used, in which P_O stands for the output power of the converter:

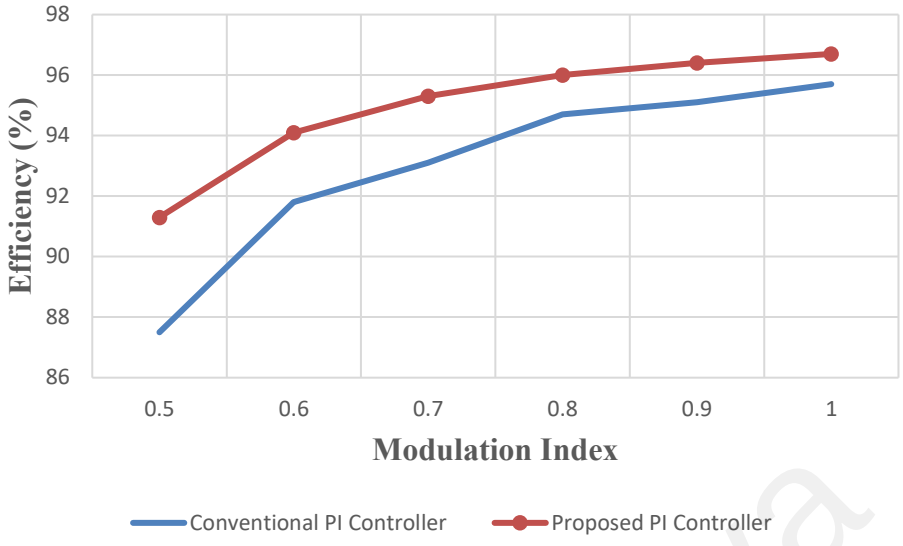
$$\eta = \frac{P_O}{P_O + P_L} \text{ x } 100\% \tag{4.10}$$

With the same condition presented in Section 4.2, simulation of power loss was conducted using MATLAB/SIMULINK. The simulation results are shown in Figure 4.26 (a) and (b) indicates that the higher the modulation index, the higher the total power loss and efficiency. A rise in the power output is found to be more than the increase in power loss. This has been contributed by improvement in the efficiency. The highest power loss

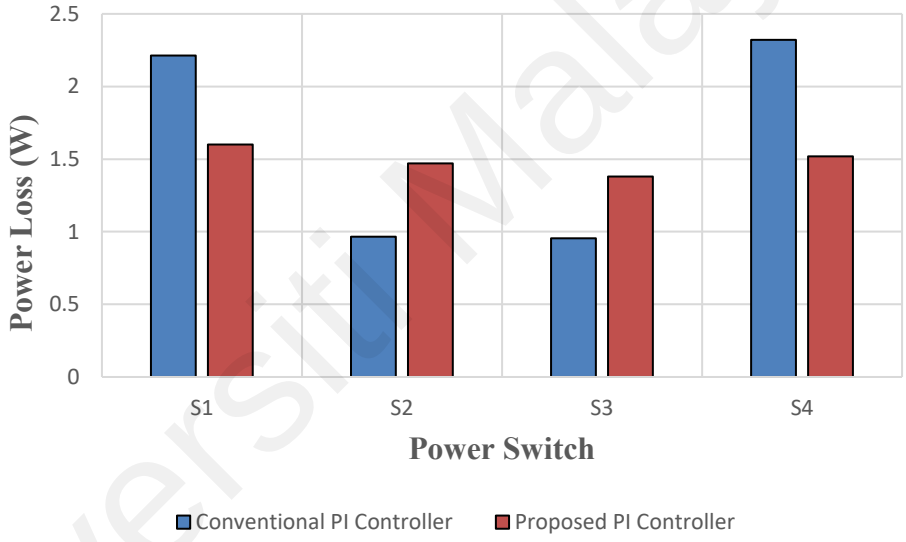
recorded for the proposed controller is 6.23 W at a modulation index of 1.0. This power loss is lower than the one using a conventional controller, which is 6.65 W and occurs at a 1.0 modulation index. For the proposed controller, the highest efficiency achieved is 96.7% at a 1.0 modulation index. This is slightly higher as compared to employing the conventional controller. Figure 4.26(c) shows power loss distribution among the power switches observed at a modulation index of 0.9. For every power switch, the power loss accounts for both conduction and switching losses of the IGBTs. Using the conventional controller, each switch records almost identical power loss as compared to varying power loss. In other words, by using the proposed controller, a uniform distribution of power loss among the switches can be accomplished.



(a)



(b)



(c)

Figure 4.26: Simulation results of power loss and efficiency for modulation index. (a) Total power loss (b) Efficiency (c) Power distribution among the power switches at 0.9 modulation index

4.6 Summary

Overall, this chapter presents the simulation results obtained and the analysis made for the PI controller with and without an online tuning mechanism. In this study,

MATLAB/SIMULINK has been utilized to complete all simulations. An observation on the capacitor voltage performance and the inverter's output have been made, and the analysis of output current THD has been carried out. The simulation of power loss and efficiency analysis among switches for both controllers are also covered in this chapter. Detailed analysis of the distribution of power dissipation among the semiconductor devices has been included. To assess the performance of the proposed controller, a comparison with the conventional PI controller has been comprehensively made. The proposed controller recorded a better performance in terms of efficiency. Thus, it can have higher efficiency. Additionally, compared to the conventional PI controllers, the proposed controller has shown to reduce power loss among switches.

CHAPTER 5: HARDWARE IMPLEMENTATION AND EXPERIMENTAL INVESTIGATIONS

5.1 Introduction

This chapter describes the hardware development and experimental setup of a buck-boost converter connected to the three-phase five-level switch-sharing-based multilevel inverter. The experimental setup is divided into two parts; the hardware and the software part. The hardware part refers to the construction of a power circuit of the buck-boost converter. Section 5.2 presents the development of the buck-boost converter circuit for capacitor voltage balancing. This part also describes the additional auxiliary circuits and components needed to complete the construction. Meanwhile, the software part refers to the control unit which is represented by the controller board eZdsp TMF2812 for real-time implementation. The control unit is discussed in Section 5.3, followed by an explanation for the experimental setup in Section 5.4. Two types of controllers that are considered for the experimental testing, namely conventional PI controller and proposed PI controller with the performance-based online tuning mechanism. Finally, the experimental results associated with the two controllers are analyzed and compared as presented in Sections 5.5 and 5.6.

5.2 Hardware Development

Hardware development refers to constructing a power circuit consisting of a buck-boost converter and additional auxiliary circuits required for DC-link capacitor voltage balancing for the inverter under study.

5.2.1 Buck-Boost Converter

The buck-boost converter circuit is shown in Figure 5.1. The converter consists of four power switches (IGBT), two inductors (L_1 and L_2), which are connected to four

capacitors (C_1, C_2, C_3, C_4). Five fuses (F_1, F_2, F_3, F_4, F_5) are installed to provide overcurrent protection for the converter. Electromagnetic interference can be reduced by using RC snubber which is connected across each IGBT used in the buck-boost converter. When the IGBT is turned off, the RC snubber will function to prevent voltage surges. The value of the RC snubber that used in this experiment is 10 Ω and 1 nF.

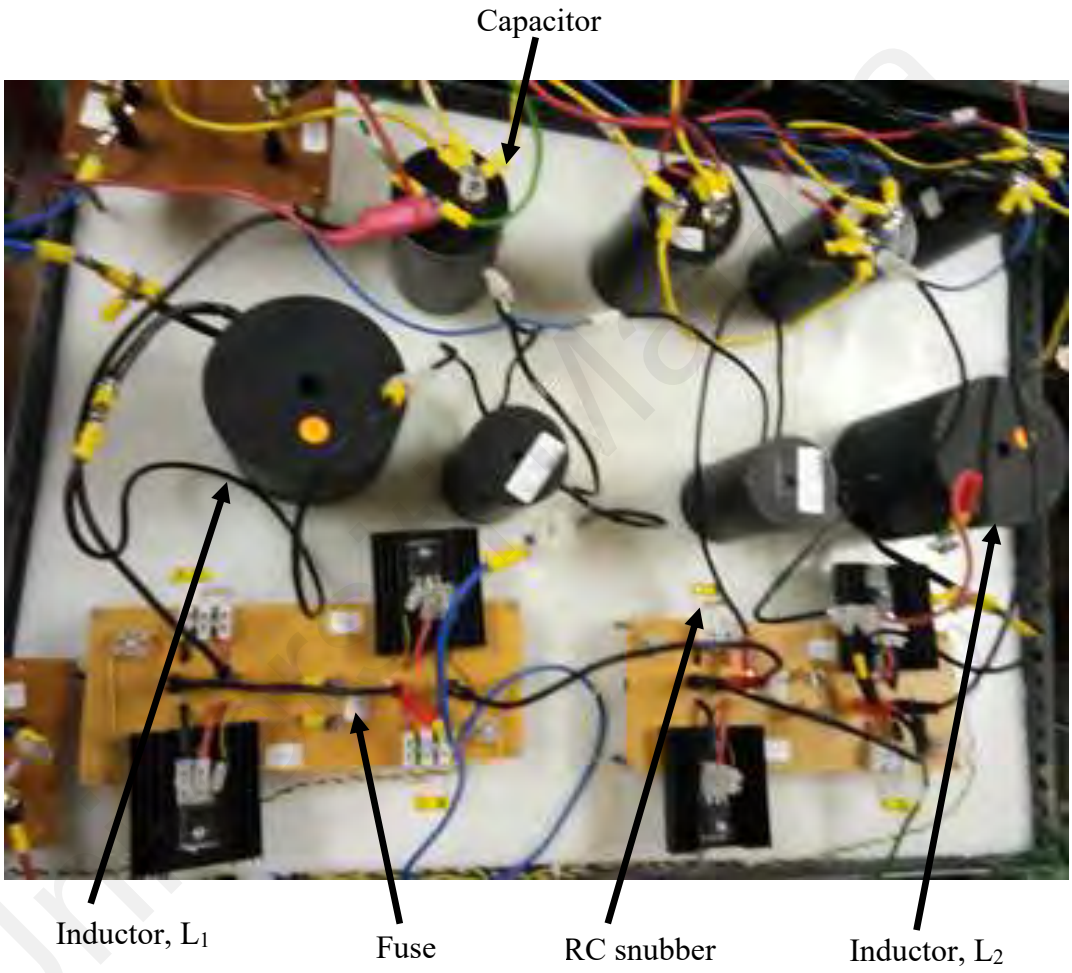


Figure 5.1: Experimental hardware of the buck-boost converter.

5.2.2 Gate Drive Circuit

A gate drive is one of the auxiliary circuits which is used, as portrayed in Figure 5.2. IGBT switches start to operate when the switching signal's voltage level increases to +15 V. This is made possible by using the gate drive in the buck-boost converter circuit.

Moreover, power circuit is isolated from the control unit by using the gate drive for protection purposes at the control unit.

Figure 5.2: Gate drives as one of the additional auxiliary circuits.

5.2.3 Dead Band Generation Circuit

Another auxiliary circuit used is the dead band generation circuit, as shown in Figure 5.3. The dead band generation circuit ensures that the complementary power switches will not be switched on simultaneously by generating a blanking time of 1 μs. This helps to avoid a short circuit across the DC sources as well.

Figure 5.3: Dead band generation circuit as another additional auxiliary circuits used.

5.2.4 Voltage Sensors

Figure 5.4 shows the circuit of the voltage sensor for the buck-boost converter. The levels of voltage across each capacitor of the buck-boost converter can be measured by using a voltage sensor. The measured capacitor voltages are used as input for the controller. The LEM model LV25P, is used as the voltage sensor.

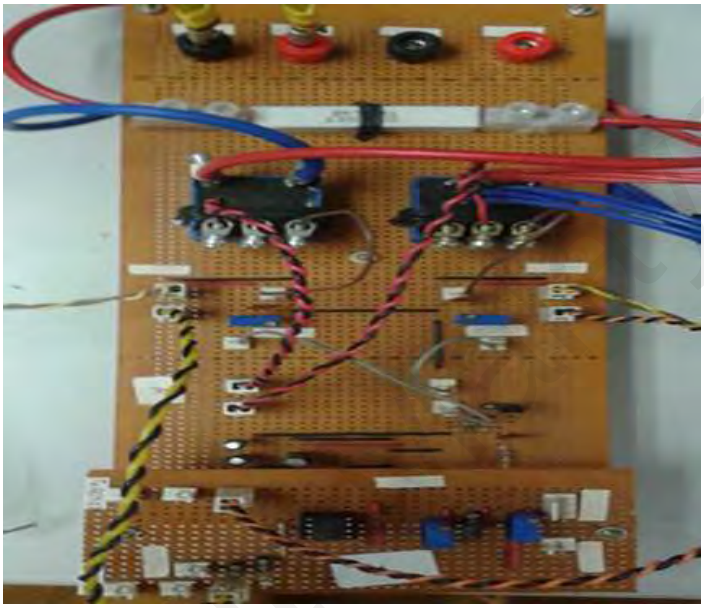


Figure 5.4: Voltage sensor circuit as an additional auxiliary circuit.

5.2.5 Auxiliary circuit for Power Supply

Figure 5.5 shows the circuit that makes the power supply regenerative. It is needed because the Sorensen power supply that we currently have in the lab is not regenerative. Therefore, regenerative power supply can reduce the fall time during the dynamic performance. In this work, an auxiliary circuit in the power supply can help to reduce the fall time from 200 ms to 6 ms. It is important since without an auxiliary circuit at the power supply, the rise time is 6 ms. So, to make a result of fall time within 6 ms, an auxiliary circuit for the power supply to become regenerative is developed.

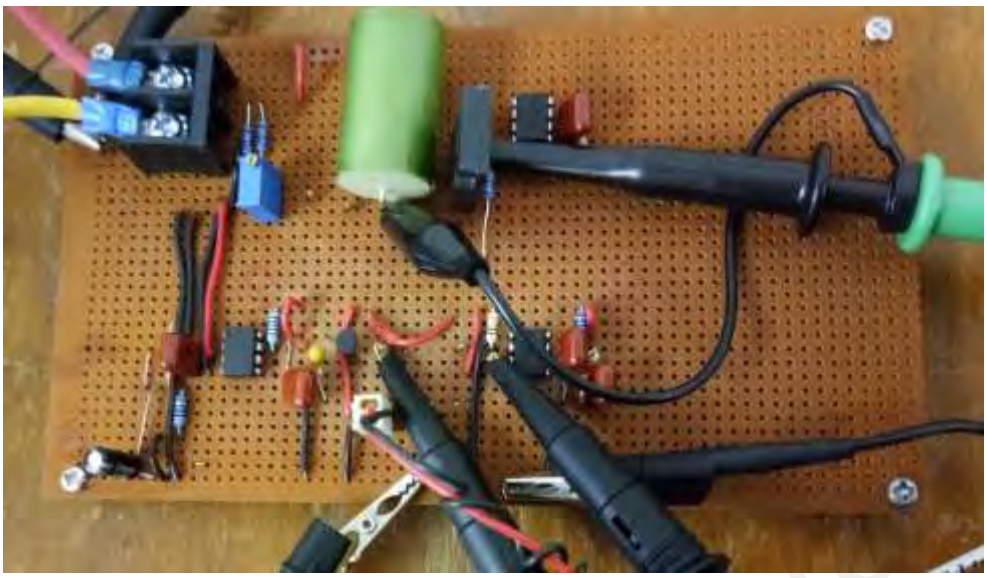


Figure 5.5: Photo of an auxiliary circuit for power supply.

5.2.6 Switch-Sharing-Based Multilevel Inverter

Figure 5.6 shows a three-phase five-level switch-sharing-based inverter (Jamaludin et al., 2015). The experimental inverter is readily available in the laboratory and is used to investigate capacitor voltage balancing. The buck-boost converter circuit is connected to the switch-sharing-based multilevel inverter via four DC-link capacitors.

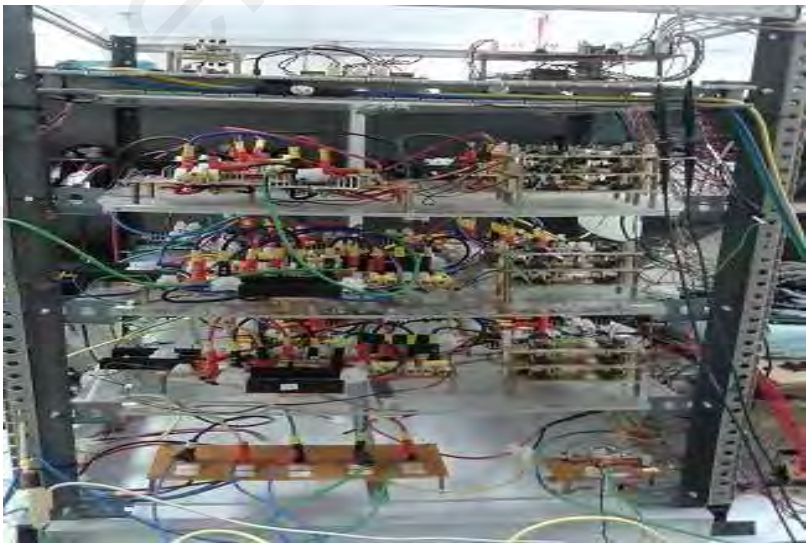


Figure 5.6: Experimental hardware of three-phase five-level switch-sharing-base multilevel inverter.

5.3 Software Part

For the control unit, the DSP controller board from Texas Instruments, TMS320F2812 eZdsp is used to implement the control algorithm of the converter and generate the switching signals physically. DSP from Texas Instruments is used for building and debugging the C source codes of the control algorithm. The operating speed of the DSP is 150 MIPS with a high performance of 32-bit fixed-point processor. Analogue-to-digital conversion (ADC), event manager, and general-purpose input/output (GPIO) ports are the special features of the DSP suitable for the real-time application. An analogue signal which is sensed from the voltage sensor is converted into small electrical voltages so that the ADC module can receive it. Another useful function of the ADC module is supplying an interface between the controller board and the real signal. There are six ports of GPIO, which are labelled as A, B, C, D, E, F and G. The function of the GPIO is to act as the digital inputs/output by cutting off specific bits in the respective multiplex registers. Program code is developed and debugged in Code Composer Studio by using a host computer. Then, the program code is uploaded onto DSP via a parallel port to the host computer. In this work, the program code involves mathematical operations using floating-point numbers. Thus, it has been optimized by using the IQ math library.

5.4 Experimental Setup

To verify the effectiveness of the proposed controller with the tuning mechanism, an experimental investigation is conducted, as shown in Figure 5.7. Once all circuits and instruments are ready, the experimental setup is built. A flow diagram of the experimental setup is shown in Figure 5.8. Four DC-link capacitors are connected between the buck-boost converter and the switch-sharing-based multilevel inverter. A single DC power supply powers the buck-boost converter. Additional power circuits such as the dead band

generation circuit and the gate drives are connected to the buck-boost converter to complete the experimental setup. The results of the inverter output and capacitor voltages are captured using an oscilloscope. Table 5.1 shows the parameters used for the experiment. To obtain nine voltage levels in the line-to-line output waveform, a modulation index of 0.9 is set during the experiment, and a switching frequency of 5 kHz is applied.

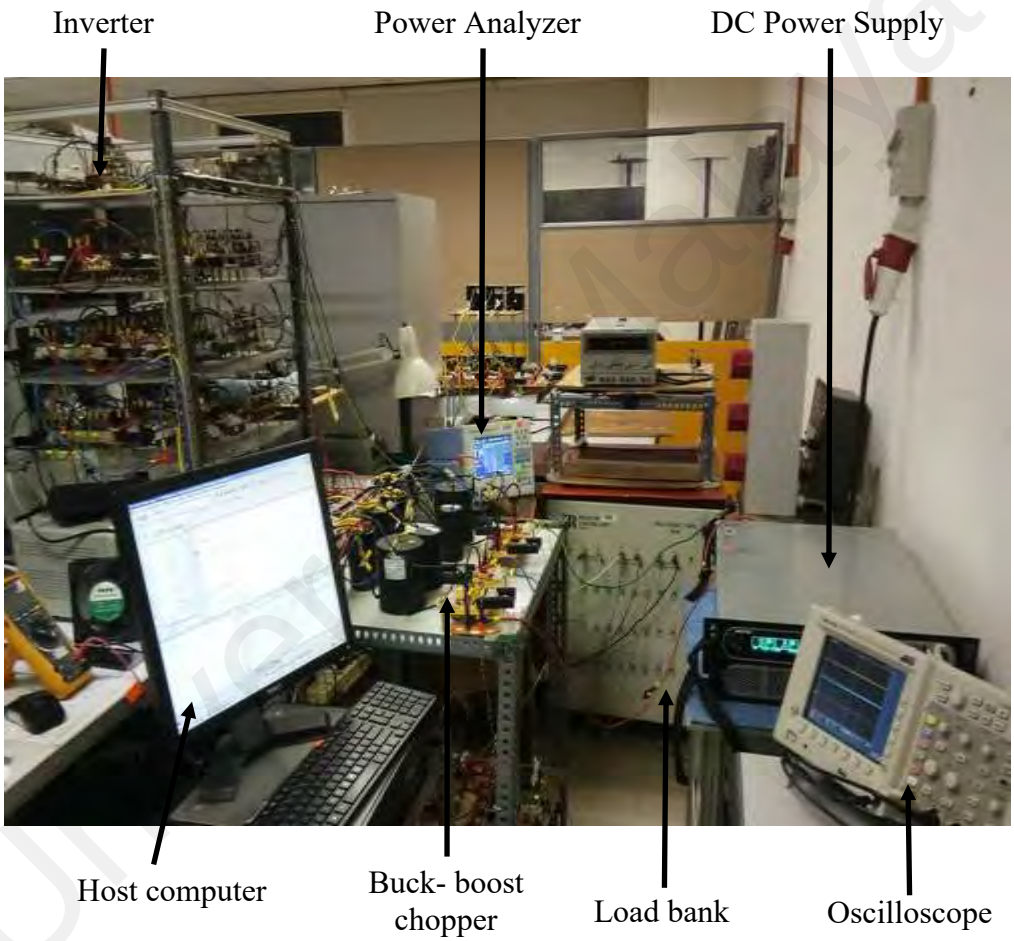


Figure 5.7: Photo of experimental setup to assess capacitor voltage balancing performance.

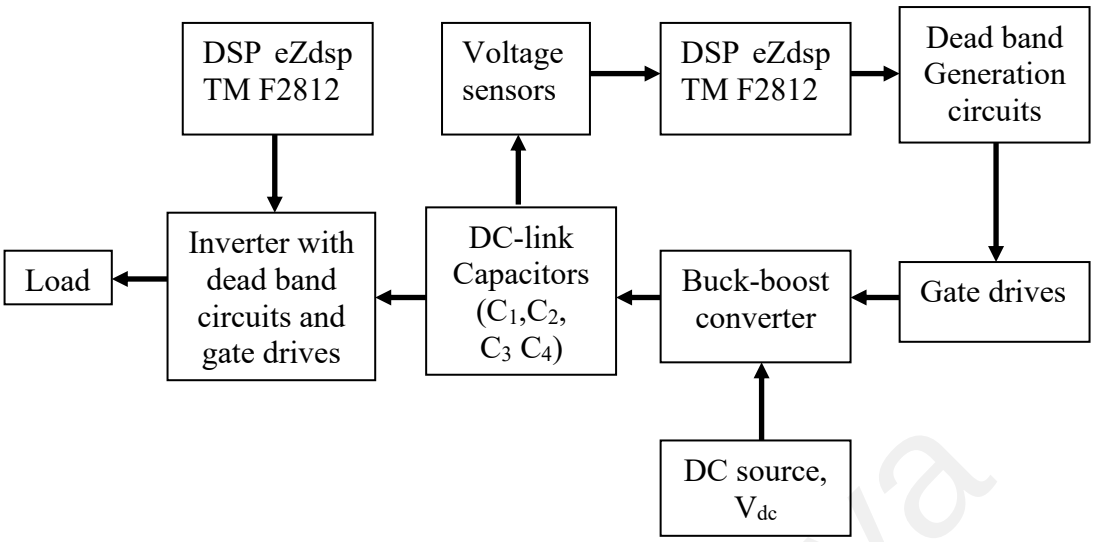


Figure 5.8: Flow diagram to represent experimental setup.

Table 5.1: Parameters of the components used.

Component	**Values**
DC capacitor	2200 µF
Inductance of buck-boost converter	12 mH
R load	120 Ohm
L load	69 mH
Five-level inverter modulation index, m_a	0.9

There are procedures that must be followed to run the experiments. Those procedures are described as below:

i. Complete Experimental setup as shown in Figure 5.7.

ii. Run the DSP programming for the switch-sharing-based multilevel inverter.

iii. Run the DSP programming for the buck-boost converter.

iv. Before connecting the DC source (power supply Ametek) to the converter, set V_{dc} to 0 V to ensure safety at the beginning. Then, turn ON the power supply. Firstly, set the DC source to be V_{dc} = 10 V (low voltage).

v. Turn ON the power supply (+5 V) of gate drives which are connected to the switch-sharing-based multilevel inverter.

vi. Then, set V_{dc} to 60 V.

vii. For step-up response, the main power supply is set between 60 V and 200 V. Adjust the oscilloscope to capture relevant waveforms during the step-up response.

viii. Start the button sequence at the power supply to run the step-up response.

ix. Set the power supply for a step-down response. The V_{dc} is between 200 V and 60 V.

x. Adjust the oscilloscope for the step-down mode.

xi. Start the button sequence at the power supply to run the step-down response.

xii. Capture waveforms from the oscilloscope.

xiii. Then, set power supply at V_{dc} = 10 V.

xiv. Turn OFF the power supply for the gate drives in the switch-sharing-based inverter.

xv. Turn OFF the power supply.

xvi. Exit the DSP programming for the inverter and the buck-boost converter.

5.5 Experimental Results

There are two parts of the experiments; preliminary testing and comparative testing. For the preliminary testing stage, the experiments are carried out to derive the relationships between K_{pU} and V_{dc} as well as K_{pL} and V_{dc} for the online tuning module, as explained in Section 3.3.2. As a start, the chosen values of proportional (K_{pU}, K_{pL}) and integral (K_{iU}, K_{iL}) gains have to balance the capacitor voltages at each input voltage, V_{dc}, which is regulated between 0 V and 300 V. This is completed by using a trial-and-error method.

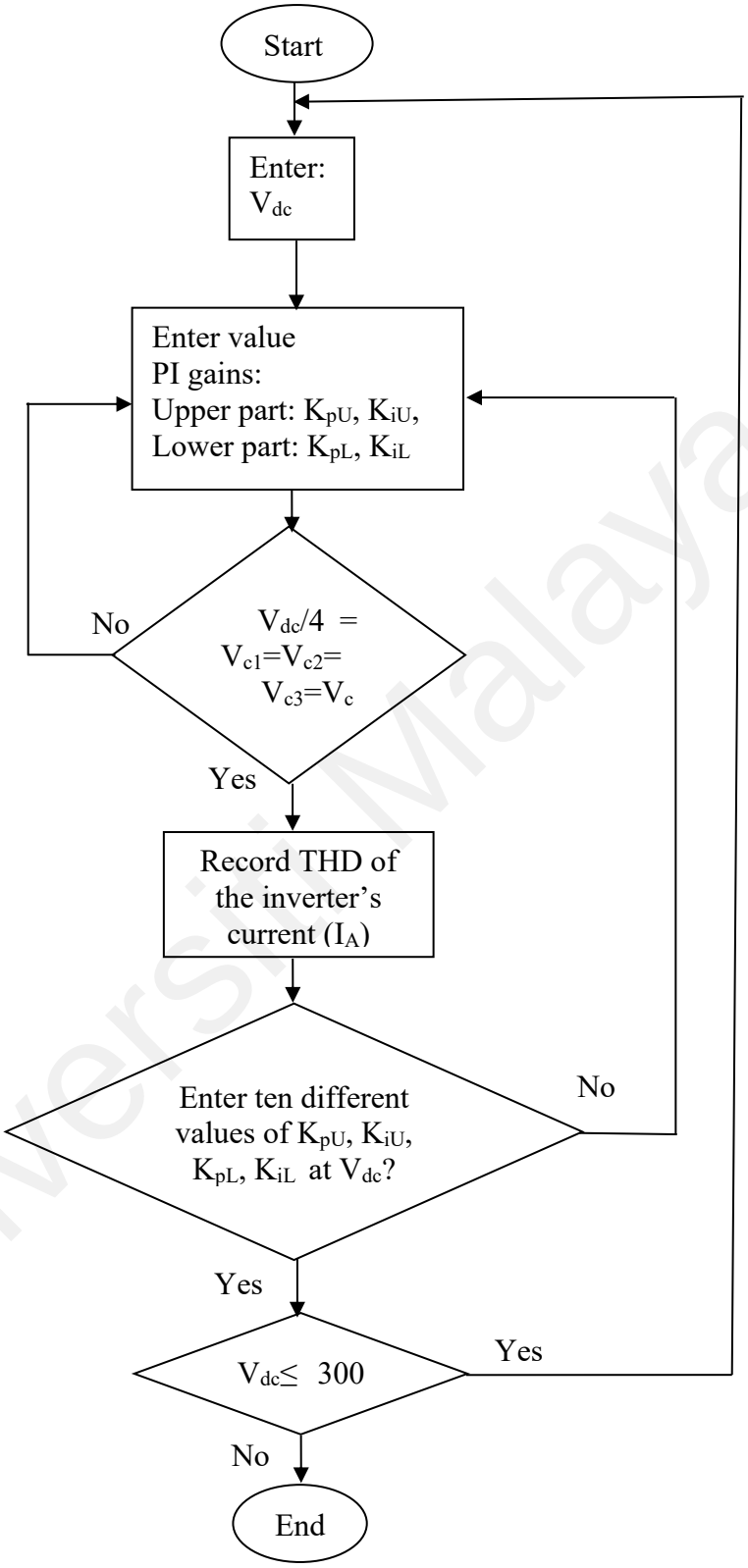


Figure 5.9: Flowchart of the preliminary experiment with the proposed PI controller.

Figure 5.9 displays the flowchart for the preliminary experiment with the proposed PI controller. The steps of the preliminary experiments are explained as follows:

i. Enter DC source or input voltage, V_{dc}.

ii. Enter the value of PI gains (K_{pU}, K_{iU}, K_{pL}, K_{iL}) in DSP programming.

iii. Using oscilloscope, check either capacitor voltages (V_{c1}, V_{c2}, V_{c3}, V_{c4}) at a balance state at reference voltage, $V_{dc}/4$ or not.

iv. If all capacitor voltages balance at their reference voltage, then measure the THD of the inverter's current, I_A, by using a power analyser. Continue with step (ii) until step (iv) with ten different values of PI gains (K_{pU}, K_{iU}, K_{pL}, K_{iL}) at V_{dc}.

v. If the capacitor voltages are not at a balanced state at their reference voltage, enter another value of PI gain. Continue step (ii) until step (iv).

iv. Continue the experiments for every 20 V of V_{dc} until V_{dc} at 300 V.

v. Stop the experiments until V_{dc} is 300 V.

According to the flowchart as shown in Figure 5.9, ten preliminary experiments are conducted to find the lowest output current THD for every input voltage change between 0 V and 300 V. Then, the collected data are used to design the proposed PI controller with the online tuning mechanism. The optimum values are determined based on the selected $K_{pU,}$ K_{iU}, K_{pL} and K_{iL} with the lowest output current THD. The THD for the inverter's output current is obtained using a power analyser for each gain value. Simultaneously, the values of the integral gain, K_{iU} and K_{iL} remain the same for each input voltage change.

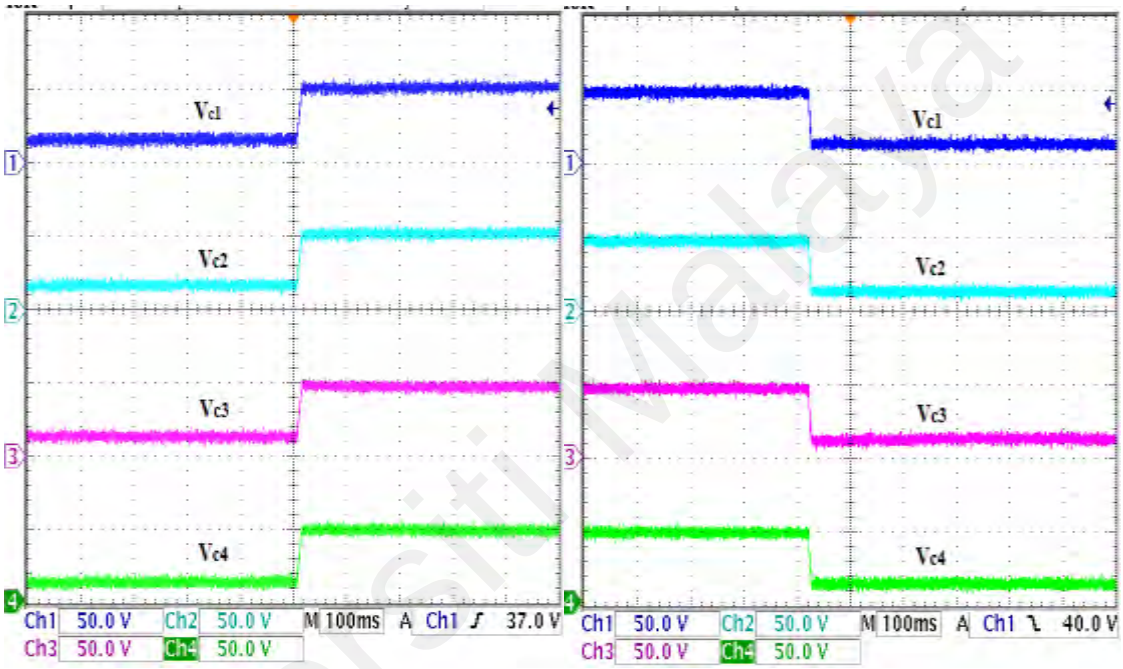
The accuracy and credibility of the selected K_{pU} and K_{pL} have been improved using actual measurement that represents real performance. The error due to the assumptions and estimation made in an ideal condition is minimized since no ideal condition is assumed. Furthermore, by using the optimum K_{pU} and K_{pL}, the controller can run at the optimum operating point. This will then retain the best output performance of the inverter. In most cases, this is critical because, as V_{in} changes, the reference voltages for the capacitors also change. This will most likely cause the optimum operating point

of the controller to deviate, resulting in the deterioration of the performance of the multilevel inverter. To reduce the complexity in the proposed tuning scheme, the values of K_{iU} and K_{iL} are not required to be changed, even though the values of K_{pU} and K_{pL} are varied. Therefore, when the online tuning mechanism is applied, attempts are made by the proposed PI controller to balance V_1, V_2, V_3 and V_4 by adjusting the proportional gain only. The integral gain and the anti-windup parameters are left unmodified.

The relationship between K_{pU} and V_{dc} as well as K_{pL} and V_{dc} are established by utilizing the MATLAB curve-fitting tool. The graphs are plotted by using the MATLAB curve-fitting tool. At the input voltage between 0 V and 300 V, five equations are derived for K_{pU} and K_{pL} in both parts of the converter. As described in Section 3.3.2, five equations are derived for K_{pU} in the upper part of the buck-boost converter at each input voltage V_{dc} change between 0 V and 300 V based on the relationships established via the preliminary experiments. In the lower part of the converter, five equations also are derived for K_{pL}. All equations are given in Section 3.3.2. On the other hand, for comparative testing, an analysis of the performance of the proposed controller (with online tuning) and the conventional controller (without online tuning) are made. It is then followed by a comparison, whereby two experimental situations have been assessed.

For the first scenario, experiments with the proposed controller are conducted, whereas the conventional controller is applied for the second situation. This work presents the investigation of the capacitor voltage balancing performance during the step-up and step-down conditions. Both experiments use similar parameters, which are portrayed in Table 5.1. Figure 5.10 shows the step responses when the online tuning mechanism is used, proving that the proposed controller can keep all capacitor voltages around their reference values between 15 V and 50 V as the input changes from 60 V to 200 V or otherwise. For the step-up case, Figure 5.11 illustrates a more detailed evaluation during a transient and steady-state conditions. The rise time, peak time and settling time are noted

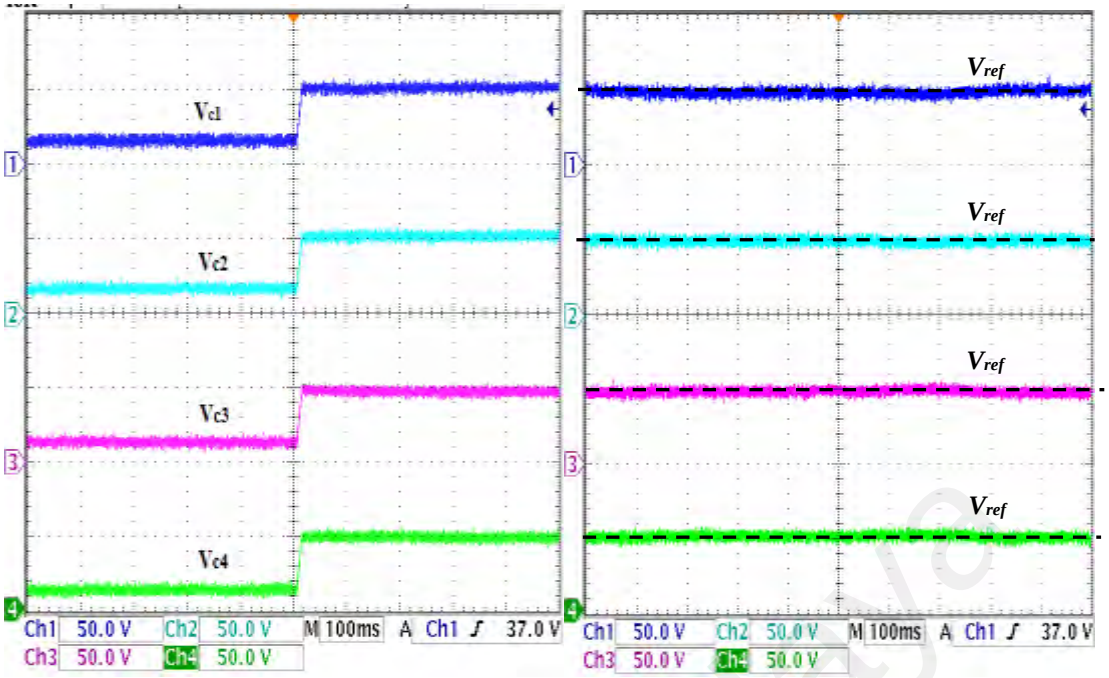
as 6, 8 and 12 ms, respectively and the percentage of the overshoot is 6%. Meanwhile, Figure 5.10 (b) shows the fall time is 6 ms. Figure 5.11 (c) displays the harmonic content of the output current with 4.46% THD. Figure 5.12 presents the line-to-line output voltage (V_{AB}) result as it can produce a nine-level waveform at modulation index of 0.9. The inverter output phase voltage (V_{AN}) and output line current (I_A) also reveal satisfactory performance.



a b

Figure 5.10: Experimental results of the capacitor voltages (Vc_1, Vc_2, Vc_3, Vc_4) with online tuning for step response with input voltage changes between 60 V and 200 V.

(a) Step-up response, (b) Step-down response.



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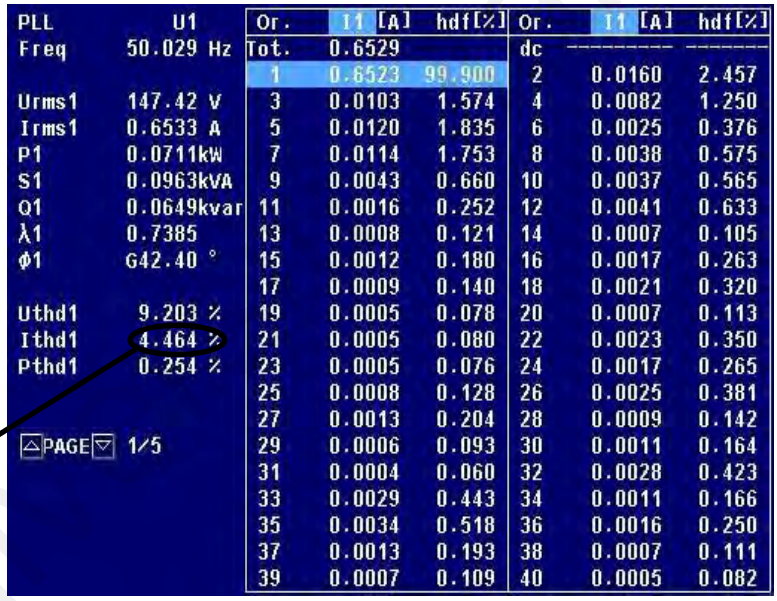


PLL	U1
Freq	50.029 Hz
Urms1	147.42 V
Irms1	0.6533 A
P1	0.0711kW
S1	0.0963kVA
Q1	0.0649kvar
λ1	0.7385
ϕ1	G42.40 °
Uthd1	9.203 %
Ithd1	4.464 %
Pthd1	0.254 %
PAGE	1/5

Or.	I1 [A]	hdf[%]	Or.	I1 [A]	hdf[%]
Tot.	0.6529		dc		
1	0.6523	99.900	2	0.0160	2.457
3	0.0103	1.574	4	0.0082	1.250
5	0.0120	1.835	6	0.0025	0.376
7	0.0114	1.753	8	0.0038	0.575
9	0.0043	0.660	10	0.0037	0.565
11	0.0016	0.252	12	0.0041	0.633
13	0.0008	0.121	14	0.0007	0.105
15	0.0012	0.180	16	0.0017	0.263
17	0.0009	0.140	18	0.0021	0.320
19	0.0005	0.078	20	0.0007	0.113
21	0.0005	0.080	22	0.0023	0.350
23	0.0005	0.076	24	0.0017	0.265
25	0.0008	0.128	26	0.0025	0.381
27	0.0013	0.204	28	0.0009	0.142
29	0.0006	0.093	30	0.0011	0.164
31	0.0004	0.060	32	0.0028	0.423
33	0.0029	0.443	34	0.0011	0.166
35	0.0034	0.518	36	0.0016	0.250
37	0.0013	0.193	38	0.0007	0.111
39	0.0007	0.109	40	0.0005	0.082

THD of the output current (%)

c

Figure 5.11: Experimental results of the capacitor voltages (Vc_1, Vc_2, Vc_3, Vc_4) with online tuning for step-up response with input voltage changes from 60 V to 200 V (a) Transient response, (b) Steady-state response, (c) Output current harmonics.

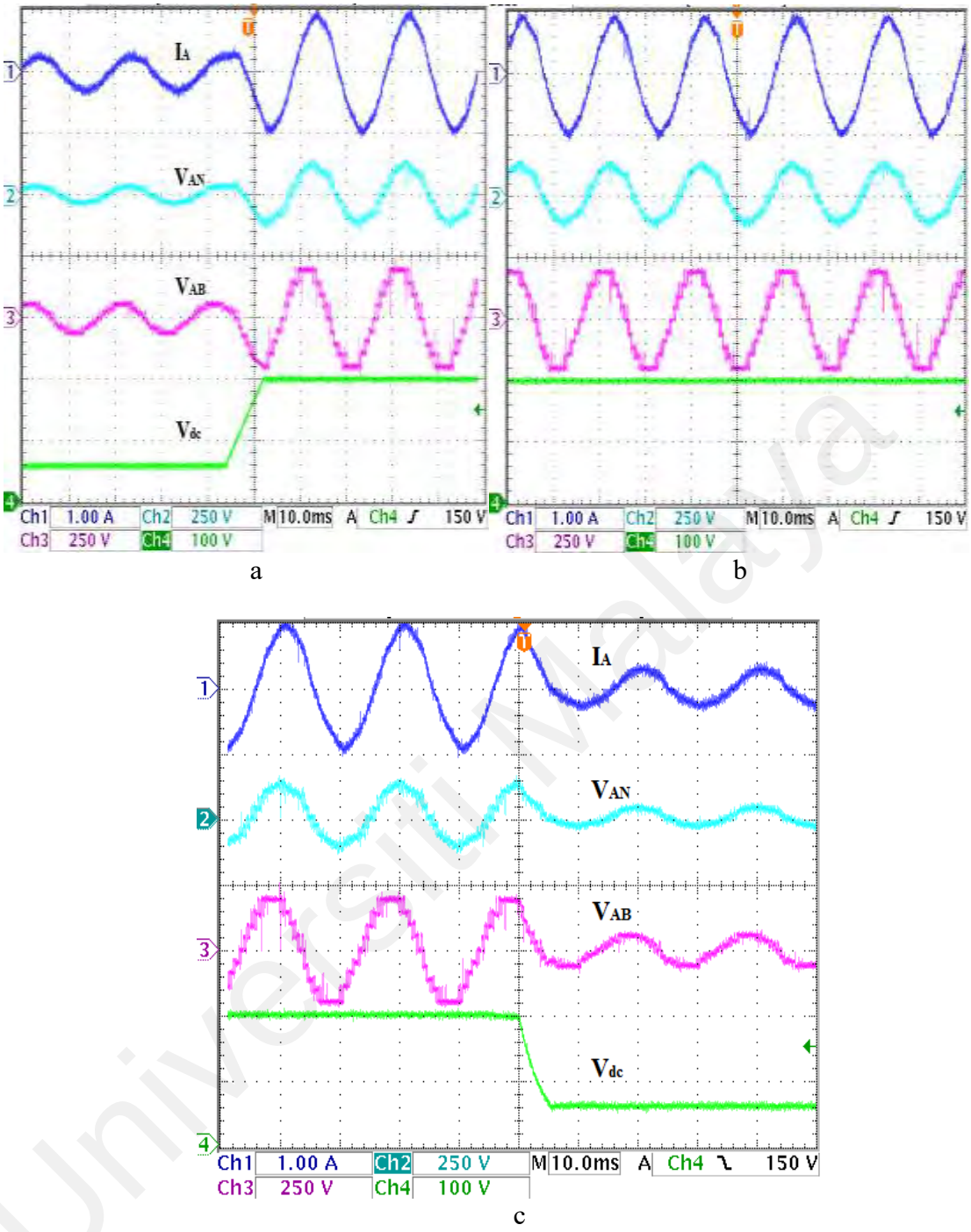
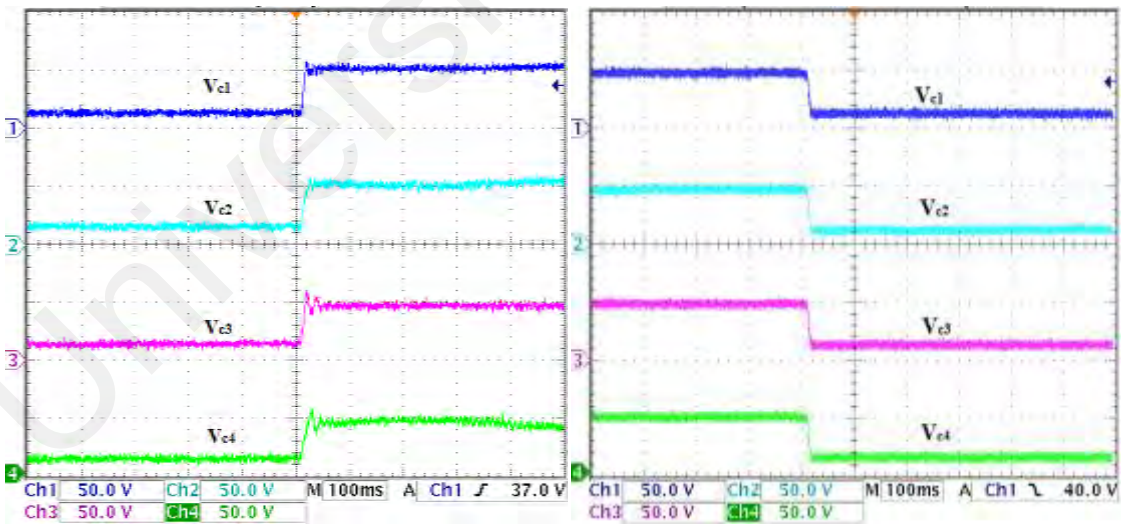


Figure 5.12: Experimental results of inverter's output with online tuning for step response with input voltage changes between 60 V and 200 V.

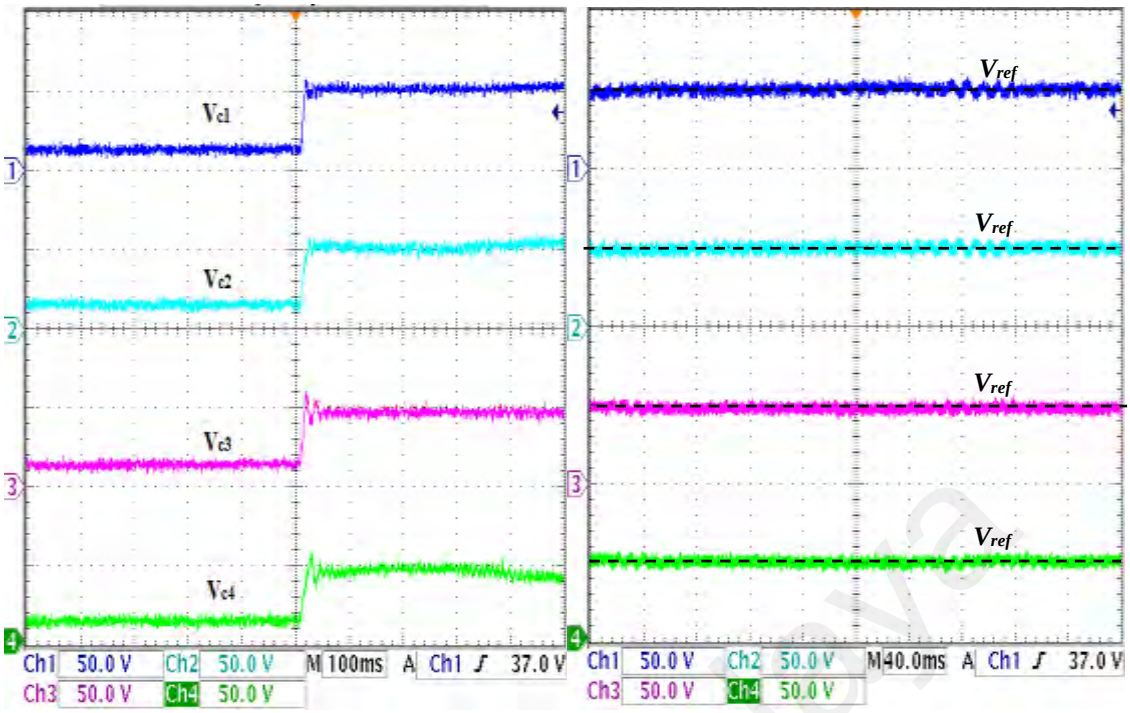
(a) Step-up response, (b) Steady-state response, (c) Step-down response.

For the second scenario, an experiment without the online tuning scheme is carried out whereby the PI controller is set with constant values of proportional gain and integral gain of 2 and 0.001, respectively, for both parts of the converter at each change of input voltage. The step responses without the online tuning scheme are shown in Figure 5.13. Figure 5.14 shows an example for the extended examination of the controller's performance during transient and steady state conditions for the step-up case. The results prove that all capacitor voltages can be kept around their respective references. The rise time, peak time and settling time are noted as 9, 12 and 200 ms, respectively. The calculated percentage of overshoot is approximately 20%. The THD of the output current was 4.92%, as shown in Figure 5.14 (c). From Figure 5.15, it is observed that without an online tuning mechanism, the line-to-line output voltage (V_{AB}) can produce a nine-level waveform for the inverter. The inverter output line current (I_A) and output phase voltage (V_{AN}) also showed satisfactory performance.



a b

Figure 5.13: Experimental results of the capacitor voltages (Vc_1, Vc_2, Vc_3, Vc_4) without online tuning for step response with input voltage changes between 60 V and 200 V. (a) Step-up response, (b) Step-down response.



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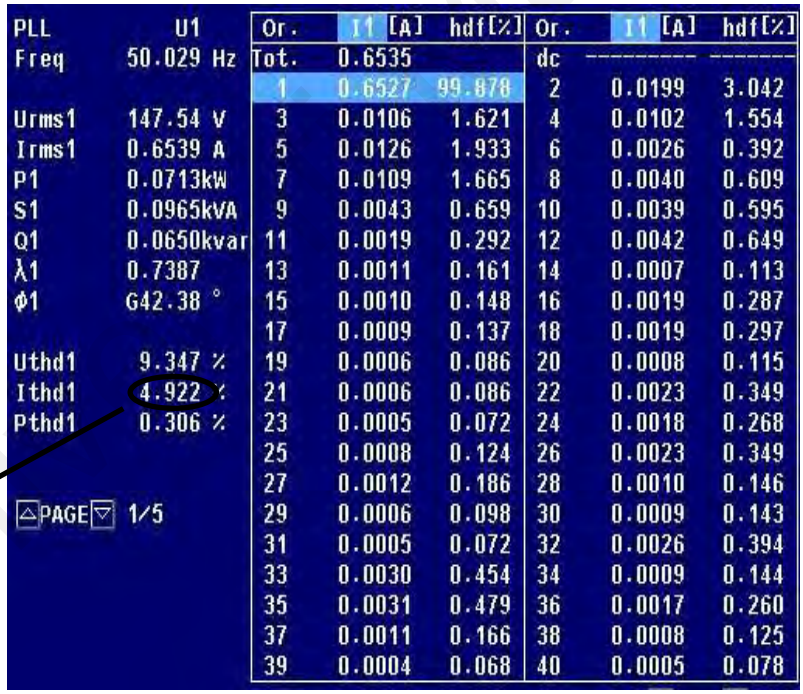
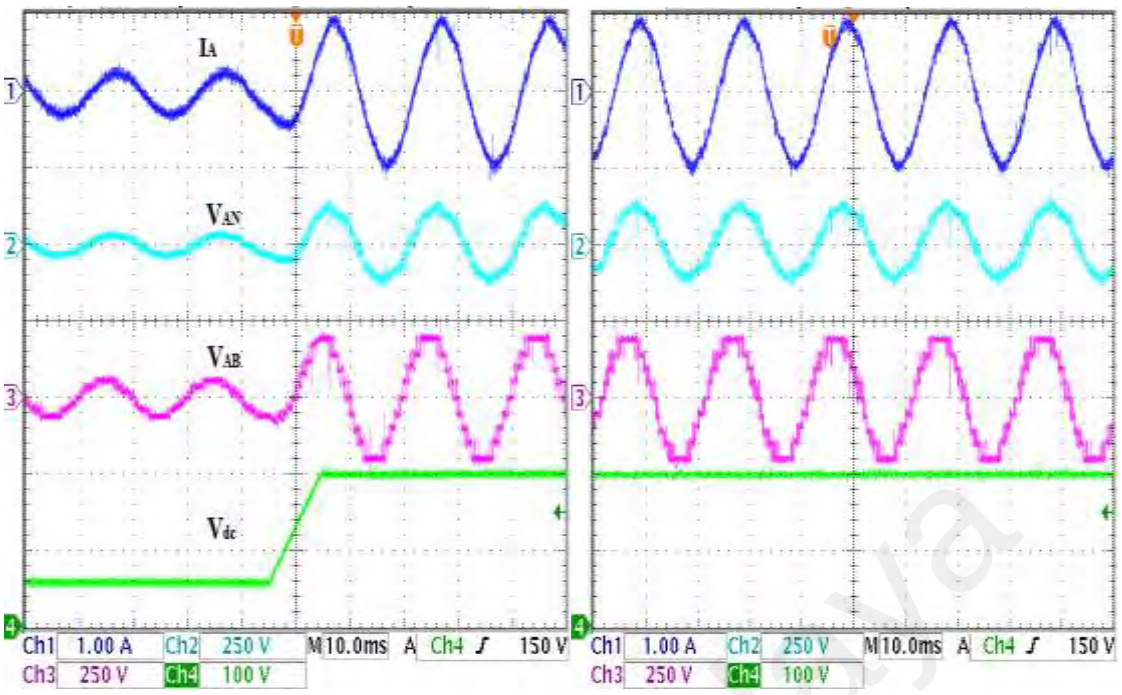


c

Figure 5.14: Experimental results of the capacitor's voltage (Vc_1, Vc_2, Vc_3, Vc_4) without online tuning for step-up response with input voltage changes from 60 V to 200 V. (a) Transient response, (b) Steady-state response, (c) Output current harmonics.



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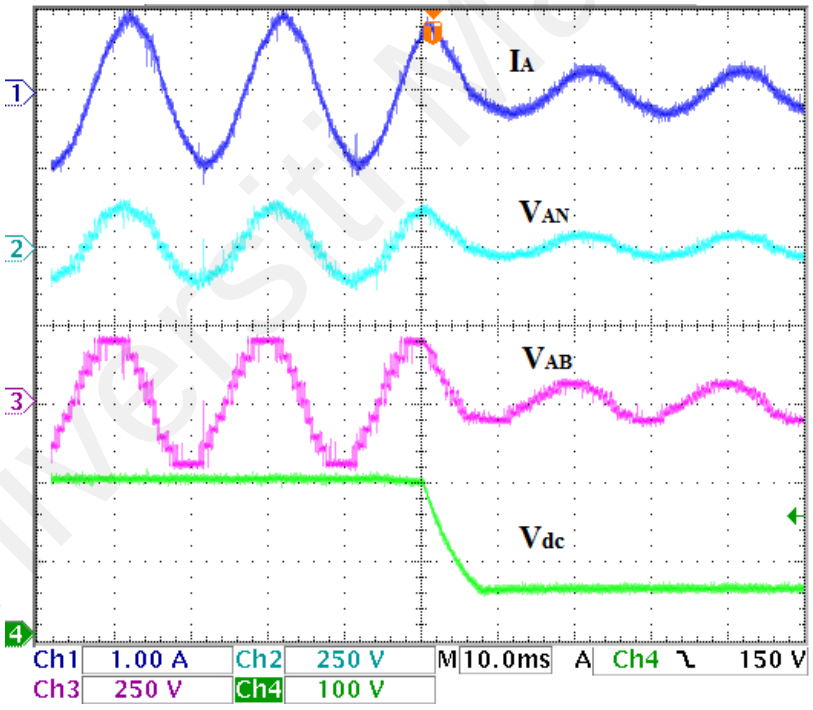

c

Figure 5.15: Experimental results of inverter's output for step response without online tuning (Input voltage, 60 V – 200 V). (a) Step-up response, (b) Steady-state response, (c) Step down response.

5.6 Discussion of Main Results and Comparison with Other Control Strategies

Using the proposed performance-based online tuning mechanism, an analysis is done to compare the simulation results and the experimental results. The peak-to-peak capacitor voltage ripples, output current THD and rise time for both results are compared. The simulation result shows a value of 2 V for the peak-to-peak capacitor voltage ripples, while a value of 3 V is shown for the experimental result. The simulation result for the output current THD is 3.09%, whereas the experimental result is 4.46%. It has also been revealed that when V_{in} is changed from 60 V to 200 V, the experimental result has a higher rise time of 6 ms, than the simulation result, which is 0.1 ms. In general, for the peak-to-peak capacitor voltage ripples, output current THD and rise time, it has been observed that the experimental results have higher readings compared to the simulation results. However, since the experimental condition considers various factors in a real environment, such as external disturbances, instrument limitations and hardware constraints, while the simulation condition assumes an ideal case, this difference is expected.

During the steady-state condition, it has been shown that the capacitor voltage ripples are quite significant when the experiment is done without the online tuning scheme. The peak-to-peak capacitor voltage ripples reach up to 15 V, as shown in Figure 5.14. In Figure 5.11, the peak-to-peak capacitor voltage ripples are reduced to 3 V when the proposed online tuning method is applied. Without the online tuning mechanism, V_{AB} is also seen to take the form of a nine-level waveform, as displayed in Figure 5.15. I_A and V_{AN} also indicate satisfactory performances. It has been shown that the results of the dynamic performance with the online tuning mechanism have been improved compared to the results without tuning. Through the improved performance achieved, the effectiveness of the proposed PI controller with the proposed online tuning method has

been validated. Meanwhile, satisfactory results have been shown by the inverter output, and fewer ripples are observed since the capacitor voltages can be balanced at the reference values.

Analysis of the conventional PI controller used in DCMI and switch-sharing-based multilevel have been compared in term of rise time, peak time and settling time. By using conventional PI controller, three level boost converter is proposed to balance the capacitor in DCMI (Abdullah et al., 2014). Table 5.2 show the performance result of the conventioal PI controller that used in both inverters. The results show that conventional PI controller give a better results for switch-sharing-based multlevel inverter as compared to DCMI. The inverter's output show satisfactory results as the line-to-line voltage can produce nine voltage levels in the waveform for both inverters.

Various control approaches have been proposed for capacitor voltage balancing, as mentioned in Section 2. These include those that apply a fuzzy controller, model predictive controller and proportional-resonant controller. Even though these control approaches offer desirable solutions, however there are concerns regarding the issue of real-time implementation. The fuzzy controller and model predictive controller may suffer from high computational costs. To perform well, the proportional-resonant controller will need an infinite gain. This will lead to difficulty for practical implementation. On the other hand, the proposed controller is based on PI configuration. PI controller is widely used in industrial applications due to its simplicity. Although the proposed controller's structure has an online tuning module, this will not result in high computation since the tuning mechanism is simple. Consequently, for potential real-time implementation in industry, the proposed control strategy that employs the proposed controller is attractive and practical.

Table 5.2: Comparative analysis of PI controller that use in DCMI and Switch-Sharing-Based Multilevel Inverter

	DCMI	Switch-sharing- based multilevel inverter
Rise time (ms)	20	9
Peak time (ms)	40	12
Settling time (ms)	600	200

5.7 Summary

Hardware development and the experimental setup are presented in this chapter. The components and equipment which are used to complete hardware development, including sensor, dead band generation circuit, gate drive circuit and a DSP, have also been explained in detail. Experiments have been performed to verify the effectiveness of the controllers. The results for both controllers have been compared and analyzed. It is shown in the results that compared to the conventional PI controller, proposed PI controller with the performance-based online tuning mechanism provides better performance in balancing DC-link capacitor voltages with less ripple, lower output current THD and enhanced dynamic characteristics.

CHAPTER 6: CONCLUSION AND FUTURE WORK

6.1 Conclusion

The switch-sharing-based multilevel inverter offers several advantages compared to classical multilevel inverters in the manner that it can reduce power losses and reduce circuit complexity. However, switch-sharing-based multilevel inverter suffers from voltage balancing problems at the DC-link. A three-phase five-level switch-sharing-based multilevel inverter, without a proper capacitor voltage balancing algorithm, C_1 and C_4 tend to charge more while C_2 and C_3 tend to discharge more. This is undesirable since the performance of the inverter in terms of its output quality can be deteriorated.

Considering this fact, a solution for the unbalanced capacitor voltages is investigated in detail. Furthermore, the method of capacitor voltage balancing used in DCMI is studied since the switch-sharing-based multilevel inverter has similarities with DCMI. After taking some considerations, the balancing circuit approach based on buck-boost converter has been selected for capacitor voltage balancing solution in the switch-sharing-based multilevel inverter. In this work, the buck-boost converter is connected to four capacitors and a five-level switch-sharing-based inverter.

The simulation study is performed to verify the effectiveness of the controller with buck-boost converter and switch-sharing-based multilevel inverter before the real experiment is conducted. Using MATLAB/SIMULINK, PI controllers have been designed, and proper simulation work has been carried out. A prototype of a buck-boost converter for switch-sharing-based multilevel inverter has been built in the lab. DSP board TMS320F2812 is used to implement the PI control scheme with experimental hardware. The experiment is conducted in two states which are steady-state and dynamic response performance.

To enhance the performance of the system, the proposed PI controller with performance-based online tuning mechanism is suggested. This online tuning mechanism tunes the values of the proportional gains (K_{pU}, K_{pL}), in both parts of the circuit while integral gains (K_{iU}, K_{iL}) remain unchanged. Simulation and experimental setup are conducted to verify the effectiveness of the proposed online tuning mechanism. The comparison between the proposed PI and the conventional PI controller is made in steady-state response, transient response and output current THD. The results of both experiments show that the performance of the proposed PI controller is better than the conventional PI controller. Furthermore, with online tuning mechanism, the voltage ripple of capacitors also reduces compared to without an online tuning mechanism. In conclusion, the research objectives have been satisfactorily achieved. The contribution made through this work has provided a promising solution to the DC-link capacitor voltage imbalance issue in a five-level switch-sharing-based multilevel inverter towards promoting inverters with improved output quality.

6.2 Recommendations for Future Work

Several issues have been highlighted below which need further study:

1. In this work, a proposed PI controller with a performance-based online tuning mechanism has been utilized. AI-based methods such as genetic algorithms and neural networks can be added to the proposed online tuning algorithm. Other types of controllers for the capacitor voltage balancing, such as fuzzy logic controllers, predictive controllers and emotional controllers, are also possible to be used in the future. Further study on this subject is recommended as option that can be explored.

2. Current control strategy can be added to the proposed control scheme with the performance-based online tuning method. Moreover, it could offer better dynamic performance since there is feedback from converter current.
3. The work presented in this thesis focuses on the five-level structure of the switch-sharing-based multilevel inverter. Moreover, the proposed performance-based online tuning scheme can be extended to structures other than five levels. Further investigation is therefore recommended.
4. This research scope is to study dynamic response resulting from the DC input change at the voltage balancing circuit side. Load disturbance is at the inverter side and is not within the scope. Therefore, analysis of load disturbance at the inverter side can be added for transient response as part of future work.

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