DEVELOPMENT OF HOLMIUM OXIDE THIN FILM AS HIGH-K GATE DIELECTRIC BASED ON SILICON CARBIDE SUBSTRATE

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FACULTY OF ENGINEERING
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2022

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THESIS SUBMITTED IN FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

FACULTY OF ENGINEERING
UNIVERSITI MALAYA
KUALA LUMPUR,
MALAYSIA

2022

UNIVERSITI MALAYA

ORIGINAL LITERARY WORK DECLARATION

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Matric No: **(17036133/1/ KVA170022)**

Name of Degree: **DOCTOR OF PHILISOPHY**

Title of Project Paper/Research Report/Dissertation/Thesis ("this Work"):

DEVELOPMENT OF HOLMIUM OXIDE THIN FILM AS HIGH-K GATE DIELECTRIC BASED ON SILICON CARBIDE SUBSTRATE

Field of Study:

ELECTRONIC MATERIALS/ THIN FILM/ NANOTECTHNOLOGY

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DEVELOPMENT OF HOLMIUM OXIDE THIN FILM AS HIGH-K GATE DIELECTRIC BASED ON SILICON CARBIDE SUBSTRATE

ABSTRACT

This thesis investigates the formation of holmium oxide (Ho_2O_3) thin film on silicon carbide (SiC) substrate by sputtering and thermal oxidation. The effects of thermal oxidation on the physical, chemical and electrical features of the resulting Ho_2O_3 layers were evaluated experimentally at various temperatures from (800 – 1100 °C). The crystallinity of the Ho_2O_3 films was detected by X-ray diffraction (XRD), while Fourier transform infrared (FTIR), High-Resolution Transmission electron microscopy (HRTEM), and X-ray photoelectron spectroscopy (XPS) analysis were used to investigate the chemical working atoms, atomic structures, and the elemental composition of the samples, respectively. The results of electrical characterization showed that thermally oxidized samples at 900 °C have the best electrical properties, which could be attributed to the thinnest oxide and absence of interfacial layer that was recorded at that temperature. For the oxynitridated samples, the impact of flow concentration of oxynitridation gas on the structural and electrical performance of the high-κ Ho_2O_3 dielectric on the SiC substrate was studied. The Ho_2O_3 films were grown using the PVD RF magnetron sputtering at various O_2 and N_2 gas flow concentrations from (25 – 100 %), and at a constant temperature and period of 900 °C and 15 mins, respectively. The results of FTIR and XRD analysis showed that cubic c-Ho_2O_3 and monoclinic-(b) SiO_2 crystal structures were formed in between the SiC substrate and the Ho_2O_3 thin films during thermal oxynitridation. The microstrain and crystallite size were obtained by Williamson-Hall (W-H) plot. The electrical measurements from the MOS capacitor revealed that 50 % oxynitridation exhibited the most encouraging electrical results, with the smallest leakage current density of 6.05×10^{-2} A/cm^2 at a breakdown field of 7.52 MV/cm and barrier height

value of 18.5 eV. These results provide potential and important implications for using Ho_2O_3/SiC gate stack, validating the usefulness of leakage current density–breakdown electric field measurement in understanding the operation of the gate dielectric in MOS-based devices. Owing to variation in temperature during thermal applications, the thin film layers and substrates in complementary metal oxide semiconductor (CMOS) structures undergo high thermal stresses, which can result in large deformation and failure. Consequently, thermal characterization and stress analysis are necessary for the reliability and durability of the electronic structures. Furthermore, the distribution of heat and thermal stress between the Ho_2O_3 thin film and the SiC substrate was simulated numerically using finite element modelling and analysis software (ANSYS). This is necessary to emulate the thermal behaviour of the structure under different thermal loadings, and for each temperature loading, the effects of thermal stress and deformation on the structure were also investigated. Based on the results of the simulation, an optimum temperature was suggested. The thermal stability and characteristics of the thin film layer/SiC structure were evaluated and validated for better electrical performance.

Keywords: Holmium oxide, silicon carbide, thermal oxidation, oxynitridation, sputtering.

PEMBANGUNAN FILEM NIPIS HOLMIUM OKSIDA SEBAGAI DIELEKTRIK GET-K TINGGI PADA SUBSTRAT SILIKON KARBIDA

ABSTRAK

Tesis ini menyiasat pembentukan filem nipis holmium oksida (Ho_2O_3) pada substrat silikon karbida (SiC) secara pemercitan dan pengoksidaan terma. Kesan pengoksidaan terma terhadap ciri fizikal, kimia dan elektrik bagi lapisan Ho_2O_3 yang terhasil dinilai secara eksperimen pada pelbagai suhu (800 – 1100 °C). Kehabluran filem Ho_2O_3 telah dikesan oleh pembelauan sinar-X (XRD), inframerah transformasi Fourier (FTIR), Mikroskopi elektron penghantaran (TEM), dan analisis spektroskopi fotoelektron sinar-X (XPS). Keputusan pencirian elektrik menunjukkan bahawa sampel teroksida terma pada 900 °C mempunyai sifat elektrik terbaik, yang boleh dikaitkan dengan oksida paling nipis dan ketiadaan lapisan antara muka yang direkodkan pada suhu tersebut. Bagi sampel oksinitridasi, kesan kepekatan aliran gas oksinitridasi ke atas prestasi struktur dan elektrik lapisan dielektrik Ho_2O_3 pada substrat SiC telah dikaji. Filem Ho_2O_3 telah ditanam menggunakan pemercitan PVD RF magnetron pada pelbagai kepekatan aliran gas O_2 dan N_2 daripada 25 – 100 %, dan pada suhu malar dan tempoh 900°C dan 15 min, masing-masing. Keputusan analisis FTIR dan XRD menunjukkan struktur hablur kubik c-Ho_2O_3 dan monoklinik-(b) SiO_2 telah terbentuk di antara substrat SiC dan filem nipis Ho_2O_3 semasa oksinitridasi terma. Saiz mikrostrain dan kristal telah diperolehi oleh plot Williamson-Hall (W-H). Pengukuran elektrik daripada kapasitor MOS mendedahkan bahawa 50% oksinitridasi mempamerkan hasil elektrik yang paling menggalakkan, dengan ketumpatan arus bocor terkecil 6.05×10^{-2} A/cm^2 pada medan pecahan 7.52 MV/cm dan nilai ketinggian penghalang 18.5 eV. Keputusan ini memberikan

implikasi yang berpotensi dan penting dalam menggunakan timbunan get Ho_2O_3/SiC, mengesahkan kegunaan pengukuran medan elektrik pecahan ketumpatan arus bocor dalam memahami operasi dielektrik get dalam peranti berasaskan MOS. Disebabkan oleh variasi suhu semasa aplikasi terma, lapisan filem nipis dan substrat dalam struktur semikonduktor oksida logam (CMOS) pelengkap mengalami tegasan haba yang tinggi, yang boleh mengakibatkan ubah bentuk dan kegagalan yang besar. Akibatnya, pencirian haba dan analisis tegasan adalah perlu untuk kebolehpercayaan dan ketahanan struktur elektronik. Tambahan pula, pengagihan haba dan tegasan haba antara filem nipis Ho_2O_3 dan substrat SiC telah disimulasikan secara berangka menggunakan perisian pemodelan dan analisis unsur terhingga (ANSYS). Ini adalah perlu untuk mencontohi kelakuan terma struktur di bawah beban terma yang berbeza, dan untuk setiap beban suhu, kesan tegasan terma dan ubah bentuk pada struktur juga disiasat. Berdasarkan keputusan simulasi, suhu optimum dicadangkan. Kestabilan terma dan ciri-ciri struktur lapisan filem nipis/SiC telah dinilai dan disahkan untuk prestasi elektrik yang lebih baik.

Kata kunci: Holmium oksida, silikon karbida, pengoksidaan terma, oksinitridasi, sputtering.

DEDICATION

This thesis is dedicated to my late mother; Alhaja Ramota Aduke Odesanya, who died during this research. May the Almighty Allah forgive her soul and count her among the inmates of paradise (Amen!).

ACKNOWLEDGEMENTS

First and foremost; all thanks, praises and adoration are due to the almighty Allah, the Lord of the world, the creator of heaven and the earth, the giver and the sustainer of life for seeing me through this programme.

My most profound gratitude goes to my loving and caring parents; Alhaji Shamsideen Tolani Odesanya and late Alhaja Ramota Aduke Odesanya, who have toiled day and night to ensure that I am successful in life. May the Almighty Allah spare the life of my father to enable him eat the fruits of his labour! Amen. May He also grant the soul of my mother the entrance into Al-Janah Firdaus.

I want to sincerely appreciate the immeasurable and immense contributions of my able supervisor, Assoc. Prof. Yew Hoong Wong for imparting knowledge to me willingly and freely without any reservation. I appreciate his patient supervision, constructive criticisms, suggestions and the unending support he displayed throughout the period of this study.

I also wish to appreciate the immense contributions of my co-supervisors, Assoc. Prof. Roslina Binti Ahmad and Assoc. Prof. Andri Andriyana for their assistance, advice and words of encouragement from time to time. Special thanks to Mrs Hartini Binti Bharum of the thin film characterization lab for her kind assistance in the preparation of samples. I also thank the Engineers and technicians of the Malaysian Institute of Microelectronic System (MIMOS) for some of the physical characterization analysis. I will be most ungrateful, if I fail to mention the valuable assistance of Dr Lei Zhence, Tahsin Ahmed Mozaffor, and Ding Zhou for their contribution, especially in the area of analysis and characterization of this thesis.

Many thanks to the Dean, Prof. Ir. Dr Kaharudin bin Dimyati, Mrs Halijah Ramlan and all the academic and administrative members of staff of the Faculty of Engineering, University of Malaya. In addition, I will like to express my special gratitude to Prof. Sedat Bingol, Assoc. Prof. Farouk Gokce, Mr Serkan Ekmem, Mr Jihad and other members of staff of Yabanci Diller, Dicle University, Diyarbakir, Turkey for hosting me during the Erasmus international mobility internship programme.

I wish to also express my appreciation to Dr Isiaka Ola-gbadamosi and his wife, both of Lagos state university, Ojo, Lagos, Nigeria for their financial and moral support. Special appreciation to Dr Segun Olanrele for his valuable advice and encouragement throughout the programme. My profound gratitude also goes to the Dean and immediate dean of faculty, Prof. Nurudeen Raji and Prof. Elkanah Oyetunji of the Faculty of Engineering, Lagos State University Epe campus, Epe, Lagos, and all the academic and non-academic members of the Faculty for giving me the opportunity to embark on this study. I want to thank most sincerely, everyone who had contributed meaningfully in one way or the other to the success of this work, but whose name could not be mentioned due to one reason or the other, may the Lord almighty reward you abundantly! (Amen).

I am so much indeed indebted to my siblings; Kaosarat, Afeez, Olubukola, and Dr Mojeed Odesanya for their social, moral and financial support in making this project a success. Finally, I want to express my profound gratitude to my dear wife, Ganiyat and my lovely children: Ridwanullahi, Al-Ameen and Faaiz Odesanya for their tolerance and the wonderful support provided throughout my programme. May the Almighty Allah be with you all.

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LIST OF SYMBOLS AND ABBREVIATIONS

AC	:	Alternating current
AFM	:	Atomic force microscopy
AI	:	Artificial Intelligence
Al	:	Aluminum
ALCVD	:	Atomic layer chemical vapour deposition
ALD	:	Atomic layer deposition
ALE	:	Atomic layer epitaxy
AlN	:	Aluminum Nitride
Al_2O_3	:	Aluminum oxide
Ar	:	Argon gas
B	:	Boron
B	:	Bulk modulus
BPD	:	Basal plane dislocation
CAS	:	Chemical abstracts service
$(CH_3)_2CO$	:	Acetone
CMOS	:	Complementary metal-oxide-semiconductor
C-V	:	Capacitance-voltage
DC	:	Direct current
DFT	:	Density functional theory
dcMS	:	Direct current magnetron sputter
DI	:	De-ionized
D_{it}	:	Interface density

E	:	Young modulus (Pa; N/m^2)
EBE	:	Electron beam evaporation
EELS	:	Electron energy loss spectroscopy
EOT	:	Equivalent oxide thickness
ESR	:	Equivalent series resistance
EV	:	Electric vehicle
FACTS	:	Flexible alternating current transmission system
FBSOA	:	Forward biased safe operating area
FEM	:	Finite element modelling
FET	:	Field effect transistor
FIB	:	Focused ion beam
FinFET	:	Fin field effect transistor
F-N	:	Fowler-Nordheim
G	:	Shear modulus (Pa; N/m^2)
GaAs	:	Gallium arsenide
GaN	:	Gallium nitride
H	:	Hydrogen
HCL	:	Hydrochloric acid
HF	:	Hydrogen fluoride
HfO_2	:	Hafnium oxide
HiPIMS	:	High power impulse magnetron sputtering
H_2O_2	:	Hydrogen peroxide
Ho	:	Holmium
HoTiOx	:	Holmium titanium oxide

Ho_2O_3	:	Holmium Oxide
HRTEM	:	High resolution transmission electron microscopy
HVDC	:	High voltage direct current
IC	:	Integrated circuit
ICSD	:	Inorganic crystal structure database
IGBT	:	Insulated gate bi-polar transistor
IL	:	Interfacial layer
IoT	:	Internet of things
ITRS	:	International roadmap of semiconductor
JBS	:	Junction barrier Schottky
J–E	:	Leakage current density-breakdown electric field
JVD	:	Jet vapour deposition
κ	:	Dielectric constant
LAGB	:	Low-angle grain boundaries
LED	:	Light emitting diode
LPCVD	:	Low pressure chemical vapour deposition
MEMS	:	Micro-electromechanical systems
Mn	:	Manganese
MSM	:	Metal-semiconductor-metal
MOD	:	Metal organic decomposition
MOS	:	Metal oxide semiconductor
MOSFET	:	Metal oxide semiconductor field effect transistor
MPS	:	Merged p-n Schottky
N	:	Nitrogen

N_2	:	Nitrogen gas
Nd_2O_3	:	Neodymium oxide
NH_4OH	:	Ammonium hydroxide
N_2O	:	Nitrous oxide
NO	:	Nitric oxide
O	:	Oxygen
O_2	:	Oxygen gas
OP-ROA	:	Oxygen plasma-oxidation annealing
P	:	Phosphorous
PEALD	:	Plasma-enhanced ALD
PD	:	Photo-detector
PDA	:	Post deposition annealing
PON	:	Passive optical network
PSG	:	Phosphosilicate glass
P-N diode	:	Positive-Negative junction diode
PVD	:	Physical vapour deposition
PVT	:	Physical vapour transport
Pt	:	Platinum
RCA	:	Radio corporation of America
RBS	:	Rutherford backscattering
REO	:	Rare earth oxide
RF	:	Radio frequency
RTA	:	Rapid thermal annealing
SCS	:	Semiconductor characterization system

SE	:	Spectroscopic ellipsometry
SEM	:	Scanning electron microscope
Si	:	Silicon
SiC	:	Silicon carbide
WBG	:	Wide band gap
VLSI	:	Very large scale integrated
SiO_2	:	Silicon dioxide
SI_3N_4	:	Silicon Nitride
SiOCH	:	Hydrogenated silicon oxycarbides
Sm_2O_3	:	Samarium oxide
Ta_2O_5	:	Tantalum pentoxide
TEOS	:	Tetra-ethyl-ortho-silicate
TEM	:	Transmission electron microscopy
TSD	:	Threading screw dislocation
TiN	:	Titanium nitride
TiO_2	:	Titanium dioxide
t_{ox}	:	Oxide thickness (nm)
ULSI	:	Ultra large scale integrated devices
VBO	:	Valence band offset (eV)
V_{fb}	:	Flat band voltage (V)
V_g	:	Gate voltage (V)
XRD	:	X-ray diffraction
XPS	:	X-ray photoelectron spectroscopy
Y_2O_3	:	Yttrium (III) oxide

ZrO_2	:	Zirconium dioxide
ρ	:	Density (g/cm^3)
σ	:	Stress (N/m^2)
$\Delta\alpha$	:	Change in coefficient
ΔT	:	Change in temperature
v	:	Poisson ratio
ε	:	Microstrain
2H-SiC	:	Two hexagonal silicon carbide
3C-SiC	:	Three cubic silicon carbide
3D	:	Three-dimensional
4H-SiC	:	Four hexagonal silicon carbide
6H-SiC	:	Six hexagonal silicon carbide

CHAPTER 1: INTRODUCTION

1.1 Preamble

The future development of power electronic systems and structures is being enabled by the present technology of electronic devices. These devices are responsible specifically for regulating the source of energy based on their load requirement, by performing with great reliability and better efficiency. The possibility of systems to operate at higher switching frequencies, power density and efficiency at a new level above that of Si-based devices is predicated on the availability of semiconductor devices that utilizes SiC-based technology (Lorenz, Erlbacher, & Hilt, 2018). Semiconductors are playing increasingly significant role in addressing challenges in the modern society in respect of energy, information, catalysis, environment, and so on.

The improved and continuous demand for electrical energy as the main driver for industrial production, automation and comfortability for human movement and living is hinged at the progress and development recorded in modern systems. Power electronic devices with great reliability and efficiency that have the capacity to transform electrical energy from one form to another are very significant for the production of renewable energy and smart grid systems. These devices play very important roles in the determination of system efficiency, cost and size thereby making them the cornerstone of technology in a power electronics system. Dated back to 60 years ago, the invention and production of silicon-based bipolar junction was started with arrays of silicon power semiconductor devices being manufactured in commercial quantity. In order to attain super high efficiency and power capacity required for various renewable energy systems and applications such as wind,

flexible AC transmission system (FACTS), transmission of high DC voltage (HVDC) and electric vehicle (EV) are enabled by power electronic devices.

The latest group of power semiconductor systems that depends largely on wide bandgap (WBG) components, such as GaN and SiC were invented and manufactured to move their power further to higher temperatures, frequencies and voltages in the last two decades (A. Q. Huang, 2019). The Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) form the bedrock of the present day electronics and automation industry. They are the pillars of very large scale integrated (VLSI) circuits in telecommunications, microelectronics, memory chips and microprocessors. A recently developed microprocessor may consist of above 2 billion MOSFETs. These MOSFETs are basically used in logic control circuits as switches. The scaling down or continuous miniaturization of silicon-based MOSFETs is attributed to the successes recorded so far in recent times on microelectronic systems which has also resulted in development of cheaper, faster and smaller devices.

According to Moore's law (Bondyopadhyay, 1998; Mack, 2011), the quantity of transistors that are used on a chip will be doubled within two years, and this has been characterized by the scaling down of silicon-based integrated circuits (ICs) over the past few years. So far, the number of transistors that are mounted on every generation of microprocessor has been a good way of describing the improvement on ICs that was predicted by Moore's law. However, the continuous miniaturization of the transistors into the organization of nanometer are faced with performance and physical restrictions that inspires the semiconductor industry to search for another set of technological devices. In order to improve on the miniaturization and speed of MOSFET devices, new electronic materials and structures need to be investigated. This will generate a novel structure for future design of

nano-electronic device. In addition, one of the problems that is being faced by the industry which was pointed out by the International Roadmap of Semiconductor (ITRS) is the method of reducing the size of semiconductors, while the efficiency is also being improved to meet the demands of the society with the aim of adhering to the geometrical growth of Moore's theory. Therefore, 'Beyond Moore's plan, there is a need to identify other options for the production of the regular MOSFET device.

The Moore's arrangement takes into account the novel structures such as the FinFET, dual gate FET and vertical MOSFET as feasible substitutes to the current planar transistor. Furthermore, there is a relationship between the utilization of substitute materials, such as graphene, carbon nanotube, silicon nanowire and strained silicon to substitute the active channel area (Ismail, 2015).

1.1 Problem Statement

The most significant microelectronic component is the complementary metal oxide semiconductor (CMOS) field effect transistor (FET) which is produced from silicon. Due to its low consuming power and improved performance, this production has increased for more than two decades. Based on Moore's law of miniaturization, which states that the amount of components mounted on ICs will increase geometrically resulting in twice its number within a period of 2 to 3 years. The lowest characteristic size of a transistor decreases yearly in a significant rate. Before now, the components used in the production of CMOS are very few. They include N, Si, Al, O, H, P and B.

Currently, the situation has changed, and new components are now introduced in various fields, such as; silicides in place of contact metals, SiOCH for low dielectric inter-

metals, TiN as barrier in diffusion materials, and copper as interconnecting material in aluminum. The SiO_2 layer which is used as interfacial layer has been reduced to approximately 1.2 nm such that the leakage current from the SiO_2 layer becomes extremely high beyond 1 A cm^{-2} at 1V, and the dissipation power becomes undesirable (B. Lee, Choi, Hande, Kim, & Wallace, 2009; J Robertson, 2011). Furthermore, it becomes very challenging and highly unreliable to develop and measure such thin films. Thus, there is a need to find a replacement for the existing SiO_2. An exponential increasing distance will result in decreasing tunneling currents. Therefore, the idea is to tackle the challenge of tunneling by replacing the native SiO_2 with a thicker material that possesses higher dielectric constant, and at the same time maintain the same capacitance as that of the native oxide.

Although, the specific material does not matter to a device designer, it is better to state the thickness of the new gate oxide in terms of its 'equivalent oxide thickness' (EOT). This is meant to develop a gate oxide with high dielectric constant that will allow scaling down to much lower EOT values. The challenges of gate leakage has been in existence since the 1990s (H.-f. Li, Dimitrijev, Harrison, & Sweatman, 1997), but the requirement for the selection of oxides were not clear. Around year 2001, the option of oxide has been reduced to HfO_2 with a huge challenge of conversion into an effective component. The growing significance of the low-power electronics in computer and telecommunication requires that the challenges should be tackled. CMOS which possesses low stand-by power requires a leakage current of approximately 1.5×10^{-2} A cm^{-2} instead of 1 A cm^{-2}. Production of high-κ oxides/metal-gate stacks entails some challenges, but they were gradually surmounted.

For an effective and successful introduction of high gate dielectric oxide, three main challenges have been identified (Gusev, Cabral, Under, Kim, & Maitra, 2004) namely;

improper gate threshold voltage, which led to the demand for metal gates, ability to continue with miniaturization for reduction of EOTs, and high defect densities that resulted in unstable gate threshold. In other to improve systems performance, the size of the system has been reduced constantly in the last few decades. Research for continuous miniaturization and search for alternative components for devices were studied extensively (Thompson & Parthasarathy, 2006; Mack, 2011; J Robertson, 2011). In order to overcome the challenges of downscaling, high gate dielectric constant materials were utilized to permit higher thickness, and therefore decrease the direct tunneling current while maintaining a low EOT (N. P. Maity, Thapa, & Baishya, 2013; N. Maity, Maity, Thapa, & Baishya, 2014). Therefore, finding an alternative high-κ material to replace the native gate oxide is the main issue.

Recently, there has been an increasing attention on metal oxides as dielectric materials in gate oxides of MOSFETs and steady capacitors in ultra-large-scale integrated devices (ULSI). New combinations of dielectric material should be set for the work function and the optimum thermo-chemical stability of the layer stacks. Therefore, a lot has been done to search for new combinations of conductive films and dielectric materials so that the scaling down of MOS-based electronics can be sustained after Moore's theory (Hlali, Hizem, & Kalboussi, 2016). Since modern CMOS technology is aggressively scaling down, states of interface in the oxide-semiconductor can be formed by low quality boundary (Mahapatra, Kumar, & Alam, 2004). The oxide trapped charge of MOS devices and the generation of interface trap states at the oxide/semiconductor interface have been demonstrated as the main reasons behind the poor performance of MOS structures (Blat, Nicollian, & Poindexter, 1991; J. Zhang & Eccleston, 1998). The interface traps characterization is significant for the assessment of the system reliability of MOS components (Militaru, Poncet, & Leroux, 2005). It is important for the development and the production of speedy Schottky, long-lasting, good

quality MOS device like ICs, transistors, diodes capacitors (Hlali et al., 2016). Various high-κ materials have been investigated as gate oxide materials. For instance, hafnium dioxide (HfO_2) (H. Liu, 2018), zirconium dioxide (ZrO_2) (Wong & Cheong, 2010; Lei, Goh, Abidin, & Wong, 2017; Lei, Abidin, & Wong, 2018), samarium oxide (Sm_2O_3) (Goh, Haseeb, & Wong, 2016a, 2016b), neodymium oxide (Nd_2O_3) (Hetherin, Ramesh, & Wong, 2017a, 2017b), titanium dioxide (TiO_2) (Maiti, Samanta, Dalapati, Nandi, & Chatterjee, 2004; Dang et al., 2014; Kibasomba, Dhlamini, Maaza, & Liu, 2018; Razera, Boudinov, Rodrigues, Ferreira, & Feil, 2018), tantalum pentoxide (Ta_2O_5) (Ťapajna et al., 2010; Cheng, Sang, Liao, Liu, Imura, et al., 2012; Sekhar, Reddy, Akkera, & Reddy, 2017), aluminum oxide (Al_2O_3) (Taube, Guziewicz, Kosiel, Gołaszewska-Malec, & Piotrowska, 2016; Damianos et al., 2018; L. Huang, Liu, Xiao, Ding, & Peng, 2021), yttrium (III) oxide (Y_2O_3) (T. E. Lee et al., 2019; D. G. Kim, Kim, Kwon, Lim, & Seo, 2021). HfO_2 and ZrO_2 are some of the most popular materials for studies on gate material due to several characteristics such as; high-κ value, large bandgap, thermodynamic and chemical stability that make them desirable (Lei et al., 2018). The advantage of using Ge channel over silicon is that the activation temperature of dopants are lower in Ge, which is around 400 to 500 °C (Kamata, 2008). Since the introduction of the first commercial silicon-based electronics in 1954 (Łukasiak & Jakubowski, 2010), silicon technology has been dominating the field of semiconductor technology. Its properties have been employed for a wide range of applications. Developed Si-based systems may attain temperatures around 200 ºC at 1000 V (Buttay et al., 2011), with a bandgap energy of 1.1 eV (Baliga, 2010). Even at that, inverse relation and the breakdown voltage is preceded by the critical junction temperature. It was found that silicon is the prime restraining factor when fabricating devices for high voltage (greater than 600 V) and high temperature (greater than 200 ºC). Various applications, including harsh environment,

requires more performing semiconductor systems and stronger devices. As a result of this, the semiconductor industry has shifted its interest towards wide bandgap materials (Salvado, Morel, Buttay, Labrousse, & Lefebvre, 2018). Therefore, SiC is an appropriate semiconductor for the replacement of Si in systems and structures that demand harsh environmental conditions (JB Casady & Johnson, 1996; Dhar, Wang, Williams, Pantelides, & Feldman, 2005; Presser & Nickel, 2008). Similar to the oxidation in SiC/SiO_2, a substrate/silicon dioxide is provided as a technology that is crucial to the Si-based MOS. A persistent approach is however significant to the method of reduction and the quality of interface density of the SiC/SiO_2 of the deposited films, which is also vital to the improvement of the performance of SiC-based MOSFETs.

1.3 Research Objectives

The main aim of this study is to develop a metal oxide semiconductor by growing Ho_2O_3 on silicon carbide (SiC) wafer, through thermal oxidation/oxynitridation in oxygen (O_2) environment, subsequent upon sputtering with Holmium (Ho) thin film target. In order to achieve this, the following objectives are to be followed:

1. To investigate the impact of oxidation temperature in O_2 ambient on the physical, chemical and electrical properties of Ho_2O_3 sputtered on 4H-SiC substrate.

2. To investigate the impact of oxidation time on the physical and electrical properties of Ho_2O_3 sputtered on 4H-SiC substrate.

3. To investigate the impact of O_2 and N_2 gas flow concentration on the physical and electrical properties of Ho_2O_3 gate oxide on 4H-SiC Substrate.

4. To develop a mechanism model of oxidation for the formation of oxidized holmium thin films on SiC substrate.

5. To investigate the thermodynamic stability and thermal stress of the Ho_2O_3 thin film on SiC substrate.

1.4 Scope of Study

In this study, Ho_2O_3 thin film was grown on SiC substrate by thermal oxidation/oxynitridation. Prior to the oxidation, pure Ho metal was first sputtered on the substrate through physical vapour deposition (PVD). The sputtering process is followed by thermal process which involves oxidation of the specimens under high temperature. This process was conducted in a horizontal tubular furnace, with the combination of controlled temperature, duration and gas flow concentration in a simultaneous manner. The characterization of the physical and chemical properties was carried out, using, x-ray diffraction (XRD) analysis, Fourier transformed infra-red (FTIR) spectroscopy, x-ray photoelectron spectroscopy (XPS), Transmission electron microscopy (TEM) and microscopic imaging. Also, the electrical properties were analyzed by using semiconductor characterization system (SCS). The thermal reliability and stress analysis of the Ho_2O_3/SiC structure were performed using a three-dimensional (3D) finite element model (FEM) thermal simulation with ANSYS 2020 R1 software.

1.5 Outline of the Thesis

This thesis was presented in an organized and orderly manner. There are five chapters in the thesis. A brief introduction and background of this research is provided in Chapter 1.

In this chapter, a general introduction of silicion carbide is presented, while providing an overview of its characteristics as a wide bandgap semiconductor for microelectronics and power devices. The need to find a suitable replacement for the existing SiO_2 native oxide, the challenges of direct tunneling and gate leakage current associated with downscaling of dielectric gate of a new gate oxide were also mentioned. Chapter 2 focusses on the literature review of previous researches, studies on gate oxides and other rare earth oxides that have been deposited on SiC substrates. The crystal growth formation and features of different polytypes were discussed alongside the crystal structure. The recent development in the CMOS technology with the application of SiC in power electronic devices were clearly mentioned. The experimental design, implementation, equipment, tools and the flow processes were discussed in Chapter 3. The experiment regarding the fabrication of the SiC MOS device, the structural, morphological and electrical properties using several characterization techniques were all discussed. Chapter 4 presents the experimental results, investigation of samples, its analysis and discussion with reference to results of previous researches. Finally, the summary of the whole study with some recommendations that were made and future challenges were presented in Chapter 5.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

Currently, the semiconductor industry is among the largest providers of the world's technological advancement, with a great expectation for continuous and steady growth in years to come. It is majorly driven by various developments such as the Internet of Things (IoT), Artificial Intelligence (AI), 5G communication, and autonomous cars. They are now widely adopted in various sectors, especially communications, power electronics, defence, automotive and aerospace. With the rate at which technology is advancing; and the continuous demand from consumers, the world semiconductor industry is projected to record a more promising future. Although, it plays a significant role in creating the modern life technology that led to the information age; each generation has its challenges; such as the implementation of low-κ material for semiconductor processes, and the replacement of SiO_2 with Al_2O_3 using plasma enhanced atomic layer deposition technique (E Schilirò et al., 2017). Hence, the emergence of a rapid increase in technological innovations has spurred the utilization of WBG semiconductors as a substitute for the replacement of silicon substrates in applications of high-radiation, high-temperature and high-power dielectric switching devices (W. Lim, Cheong, & Lockman, 2010).

The growing rate at which smartphones are acquired and that of which semiconductor integrated circuits are employed in automobiles cannot be over-emphasized. The increase in industrial automation in smart cities is also one of the trends that will gain traction in the compound semiconductor market in the coming years. Due to the commercial availability of silicon carbide and its ability to grow SiO_2, it has advanced technologically into one of the

topmost competitors among several WBG semiconductors (Roccaforte, Fiorenza, Greco, & Nigro, 2018). SiC is available in various polytypes (Sereni, 2016). One of the polytypes that offer good physical properties is 4H-SiC; which has WBG of 3.26 eV, a thermal conductivity of ~3.7 W/cm ºC, electron saturation drift velocity of ~ 2×10^7 cm/s, and a high breakdown field strength of ~3 MV/cm (W. Lim et al., 2010; G. Choi, Yoon, Jung, Jeon, & Lee, 2015). The display of these characteristics makes SiC-built electronics potentially suitable for applications under extreme environmental conditions (Soo, Cheong, & Noor, 2010; E Schilirò et al., 2017). In order to address some of the challenges being confronted by SiC-based devices, a reliable and high-κ dielectric material of thicker gate oxide is required. The development of components of this nature requires that an excellent gate oxide be formed between a target and the substrate for the attainment of a low gate leakage current and high transverse electric field in the MOS-based devices (Dushaq, Rasras, & Nayfeh, 2017).

Continuous reduction in the size of silicon-based semiconductors has necessitated the compaction of more transistors in a chip (Hourdakis & Nassiopoulou, 2020; Shah & Dhavse, 2021). Consequently, the size of the MOS structure has to be reduced accordingly, in a manner that its electrical design will not be negatively affected (E Schilirò et al., 2017). Therefore, SiO_2 dielectric gate oxide which has dominated the industry for a long period in MOSFETs and other semiconductors has to be reduced. As the oxide thickness is scaled down below 1.2 nm, there is a possibility of passage of quite a huge amount of leakage current through the dielectric, owing to the direct channelling of carriers (Kurniawan, Wong, Cheong, Moon, & Bahng, 2011; Samanta & Mandal, 2016). In a bid to surmount the aforementioned challenges, Al_2O_3 gate oxide with a good dielectric constant (κ) acting as a substitute to replace SiO_2 was developed. The oxide thickness of the dielectric is required to demonstrate better or similar features of MOS as that of SiO_2 (Khosa et al., 2019).

Micro-electromechanical systems (MEMS) and semiconductor devices play significant roles in the daily life of people, and in recent times, these technologies have become the major instruments for them to carry out their daily activities. The semiconductor technologies and other systems are required by portable devices like tablets, smartphones, detectors, photonics and other electronic gadgets to perform more efficiently. In order to have a more efficient electronic device; there is great attention by researchers towards its downscaling, with a view to improving its performance, low cost (Loncarski, Monopoli, Leuzzi, Ristic, & Cupertino, 2019), high speed (J. Chen et al., 2020; Cougo et al., 2020), low power consumption, and energy efficiency per year. These are fundamental considerations for designing an integrated circuit (IC) for higher performance. Moore's law states that the density of some electronic parts and the performance of the ICs will become twice their value every two years. This implies that the size of the components should be small enough so that the IC can accommodate more components.

Presently, complementary metal oxide semiconductor (CMOS) transistors have been reduced to a nanoscale size of less than 30 nm as compared to the previous one which was around 100 nm (Levisse, Giraud, Noël, Moreau, & Portal, 2017). This shows that, as time goes on, there will be a geometric reduction in the size of transistors. However, there is a limit to which the size can be reduced. Considering a transistor, its dimension is largely dependent on the size of the dielectric layer, most especially the thickness. The ultimate reduction in the size of the layer has almost gotten to an end, due to extreme leakage of current in ultra-thin gate oxide ($\leq$ 1 nm) (Bohr & Young, 2017). Through the ultra-thin film oxide; electrons can penetrate by tunnelling effect, and also cause current leakage. As a native gate oxide grown on Si wafer, SiO_2 was commonly used in the semiconductor sector, owing to its capacity to grow naturally on the Si substrate, hence a dense interface with little flaw

can be developed. Aside from that, there is a possibility of producing SiO_2 gate oxide in mass quantity at a low manufacturing cost. Several studies have been reported on the continuous reduction of gate oxides' thickness and downscaling of leakage current (Sharma & Rana, 2015; J.-G. Lee, Kim, Seo, Cho, & Cha, 2016; Matsumoto et al., 2017).

Another great challenge confronting producers in the semiconductor industry is the selection of high-κ materials. The integration of good dielectrics on Si is to find a solution to the problem of downscaling, while that of SiC is to reduce the leakage current that penetrates through the oxide film. Recent studies showed that Al_2O_3 as a high-κ material has a large fixed charge and interface trap density (Khosa et al., 2019). The band offset passage of Al_2O_3 or AlN to ~1.7 eV bandgap of 4H-SiC will be appropriate for an n-tunnel device (E Schilirò et al., 2017; Khosa et al., 2019). A good grade single AlN structure can be deposited on SiC because, it has only 1 % structural difference from SiC (Khosa et al., 2019). However, a non-crystalline Al_2O_3 offers better features as a gate dielectric than poly-crystalline α-Al_2O_3 on 4H-SiC due to the passage of leakage current through the microstructure. Therefore, different deposition methods have been employed to regulate the composition and thickness of the interfacial layer (IL) between the substrate and the gate oxide. In this way, a satisfactory amount of interface-trap density can be achieved.

The progress recorded so far in the semiconductor industry has focused majorly on four areas, namely; downscaling of electronic components on a tremendous scale, reduced power usage, increasing speed of operation, and increasing tolerance in the range of operational temperature (Moshrefi, Aghababa, & Shoaei, 2017). Despite these recorded successes, the current study shows that SiC-based devices are still confronted with a few challenges which include degradation of gate oxides, high leakage current density, low resistance owing to

trap-assisted tunnelling of gate oxide when subjected to continuous stress, and stress-induced current (S. Liu et al., 2016; X. Jiang, Zhai, Chen, Yuan, & Wang, 2018; Wei, Liu, Yang, Li, & Sun, 2018). Therefore, there is a need to address these challenges with a view to providing solutions and improving the reliability of SiC-based electronics under extreme environmental conditions.

2.2 SiC-Based Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

In our present-day life, the demand for the use of electronic equipment is greatly increasing, especially in the area of electrical energy. This equipment depends largely on various semiconductor devices and the cost of their components. Therefore, the power utilization of semiconductor systems becomes one of the main concerns for the environment. In order to avoid the indiscriminate building of several power generation stations that are consuming much of the available natural and renewable energy, power drops of semiconductor systems have to be largely minimized. Presently, the semiconductor industry is dominated by Si technology due to scaling down. Using this technology in power devices, most especially for electronic systems reduces power losses within the range of 4 – 5 % (Ballestín-Fuertes, Muñoz-Cruzado-Alba, Sanz-Osorio, & Laporta-Puyal, 2021). The slight reduction in the losses can be attributed to improvements in their design, but this may not eventually lead to a decrease in the total amount of energy wasted within the environment. In an effort to achieve a power-saving mode, the power drops in the electronic devices are required to be scaled down to about 2 % (Ballestín-Fuertes et al., 2021).

Creative ideas and the utilization of more appropriate components are also required to improve the performance of power systems that will later lead to a reduction in the energy consumption of electronic devices. With a more promising component such as SiC, the growth of semiconductor technology has been greatly improved. The SiC materials are readily available in commercial quantities in grades such as 100 mm, to enhance the fabrication of power devices at cost-effective rates. During the developmental stages of SiC, there were speculations that SiC-based devices can be utilized and manipulated in a similar manner as Si-based systems. However, it was not long before it was realized that the 50 % carbon content in the material combination of SiC makes it very challenging to be utilized as the regular Si technology. Various processes must be modified and /or new creative ideas have to be developed.

SiC is usually used as base components in MOSFETs and other semiconductor devices, especially for power electronics purposes. Currently, UMOSFET, VMOSFET and DMOSFETs are the various designs that exist in MOSFETs, depending on the mode of formation of the MOS structure. MOSFET-based devices have some specific advantages, such as; (1.) decreased consumption of current, owing to voltage-driven control circuits, (2.) absence of currents with reverse recovery associated with re-combined minority transporter that leads to high capacity switching frequency (about 1 MHz in Si technology), and (3.) utilization of epilayers and substrates as the physical transistor that results in a high capacity of current handling and breakdown voltage (about 10 A and 1500 V in Si technology). Intensive study on the development of SiC MOSFET has begun in the last two decades (Esteve, 2011).

In 1992, the development of the first SiC power semiconductors that are vertical U-shape trench MOSFETs (UMOSFETs) was reported by Cree Research (Palmour, Carter, Edmund, & Kong, 1993). Since then, various kinds of SiC MOSFETS including planar double-implanted MOSFETs have been fabricated (Shenoy, Cooper, & Melloch, 1997). Reports from early studies showed that carbon remnants exist near the interface of MOS during its development. To surmount the challenges that were encountered during the fabrication, alternative solutions were sought. Regardless of renewed interests in SiC MOSFETs from various researchers and the continuous awareness from the side of manufacturers, the devices are now available in commercial quantities (Esteve, 2011). Despite encouraging results obtained from research and developments, the appropriate process technology for commercial production of a MOSFET has not been established. The potential of a 4H-SiC as a promising substrate and the challenges for commercial production in a MOSFET device will be investigated.

2.3 History of Silicon Carbide

Silicon carbide is one of the most promising candidates that has emerged in the search for a viable semiconductor material, owing to its superior high temperature, frequency, voltage performance and low ON resistance when compared to silicon. It is a wide bandgap semiconductor material that possesses distinct electrical, mechanical and thermal properties making it appropriate for numerous uses in harsh conditions of operation; such as high radiation exposure, power, and situations where thermal management is desired (X. Zhang, Li, Wang, Zhang, & Akhmadaliev, 2018). Currently, SiC is available in commercial quantity and at high microelectronic grade quality. Apart from the large-scale wafers, there is an

increasing demand for SiC-based components, especially the ones that are built with SiC thin film on a substrate (J.-H. Lee, Bargatin, Park, & Milaninia, 2012; M. Kim, Seo, Singisetti, & Ma, 2017; Q. Jia, Huang, You, Yi, & Lin, 2018).

SiC is comprised of carbon and silicon at 50 % proportion, each. A SiC that occurs naturally is also referred to as "moissanite", which was named after Dr Henri Moissan, a French researcher who first discovered the material in 1905 (Pensl et al., 2008). It was found only in little quantities and in geographical locations where they are extremely rare to be found, like kimberlitic volcanic openings and in some kinds of meteorites. Almost all the SiC that are commercially available around the world are synthetic in nature. The synthetization of this material was first done by Jons Jacob Berzelius, a Swedish researcher at the University of Linkoping in 1824 (Schöner, Krieger, Pensl, Abe, & Nagasawa, 2006). However, the characteristics of SiC were not well comprehended at that time. There was little or no interest in SiC, until the electric smelting furnace was invented by the duo of Eugene and Alfred Cowles (Lelis, Habersat, Olaniran, Simons, & McGarrity, 2006), and adopted by Acheson (Matocha, Dunne, Soloviev, & Beaupre, 2008). This adoption was meant to produce a carbon-based material for the replacement of diamond as a coarse and cutting disc.

The crystalline material was formed after the process was characterized by infusibility, refractability and hardness. Shortly after that, the study on the electronic properties of SiC was started, and in 1907, the first light emitting diode (LED) was developed using SiC material (Afanas' ev, Stesmans, Bassler, Pensl, & Schulz, 2000). A new concept of developing high-quality crystals was presented in 1955, and the study on SiC was intensified such that the first conference on SiC was held in Boston in 1958. However, the interest in SiC was reduced due to its scarcity, fast-growing technology of silicon and its

accomplishment. In 1978, the invention of the seeded growth of sublimation came as a big break from the duo of Yu Tairov and V.F Tsvetkov which led to the creation of SiC wafer growth (Fung & Kopanski, 1984). The rate of growth could be improved and, bigger diameter seeds may also be created with that of its lengths by inserting a crystal and pushing substance to the seed from the source through a temperature gradient. The resultant material may be cut and packaged into wafers.

A "step-controlled epitaxy" on off-axis substrates was recorded in 1987 as a breakthrough (Esteve, Schöner, Reshanov, Zetterling, & Nagasawa, 2009), this implies that epitaxy of good quality could be achieved at low temperatures. In view of this achievement, Cree research, the first organization to market SiC wafers was established in 1989, and the organization has continued to be the largest player till now, as far as SiC substrate is concerned (Palmour et al., 1993). Since then, the interest in this area has continued to be of great significance to researchers. In the year 2001; Infineon, one of the leading manufacturers of semiconductor devices introduced a SiC-based Schottky diode line. Cree also launched a Schottky diode and MESFET of high frequency into the market. In 2009, this market has a value of about $ 29 million with an average income of about 25 % larger than the preceding year. In August 2010, Cree later introduced the 6" 4H-SiC wafers into the market. It has better material quality and enhanced epitaxy which results in the milestone recorded in components, and also ensures the growing interest in SiC devices remains continuous.

Owing to the latest availability of SiC substrates, especially in commercial quantities, the current and continued interest in SiC technology has greatly increased due to the quest for solutions to the limitations of Si-based devices (Eriksson, 2011). The chronological order of the development of the 4H-SiC component and its related devices is presented in a

schematic form (Figure 2.1). Although significant commercialization was noticeable only after 2005 when merged p-n Schottky (MPS) devices were almost eliminated (Shenai, 2019), the prospects of WBG devices has been identified since the mid-1980s (Shenai, Scott, & Baliga, 1989). Since then; densities in the defects, particularly the Basal plane dislocations (BPDs) have been shortened.

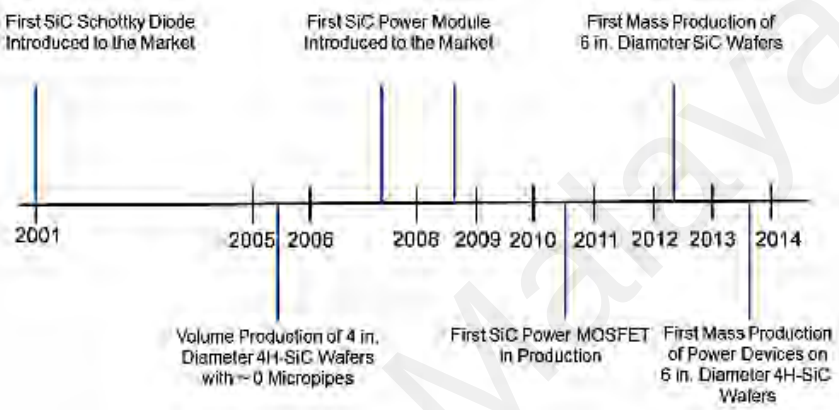


Figure 2.1: Schematic representation of the chronological order of development of 4H-SiC devices (Shenai, 2019).

The size of wafers has risen from 4 to 6 inches in diameter, and their cost has also reduced with growing numbers of manufacturers springing up all over the globe in the year 2012. However, the basic issues with the material regarding the crystal seed with the use of threading screw dislocations (TSDs) are still in existence. There have been fruitless efforts to seed large crystals individually; such as WBG electronic devices, and conversion in high-density power systems (Nakamura et al., 2004; Powell, Neudeck, Trunek, & Spry, 2008). There are indications that 4H-SiC power MOSFETs are prone to issues of reliability on gate oxides and also possess a MOS interface of high density (Lelis et al., 2006; A. Agarwal, Fatima, Haney, & Ryu, 2007; Kimoto & Cooper, 2014; Sakai et al., 2015). A report from a previous study indicates that the high density in the interface of MOS is attributed to the

intensity of the defects of the bulk crystal (Son et al., 2012). A 4H-SiC power device which is comprised of high voltage (less than 3 kV) is illustrated in Figure 2.2 (Yamamoto et al., 2012). An acceptor level of one carbon vacancy, referred to as $Z^{1/2}$ centre which is contained in n-type 4H-SiC is attributed to the main cause of the decrease in carrier lifetime. This has led to high intensity of passive optical network (PON) in low-carrier devices (Danno, Nakamura, & Kimoto, 2007; Son et al., 2012).

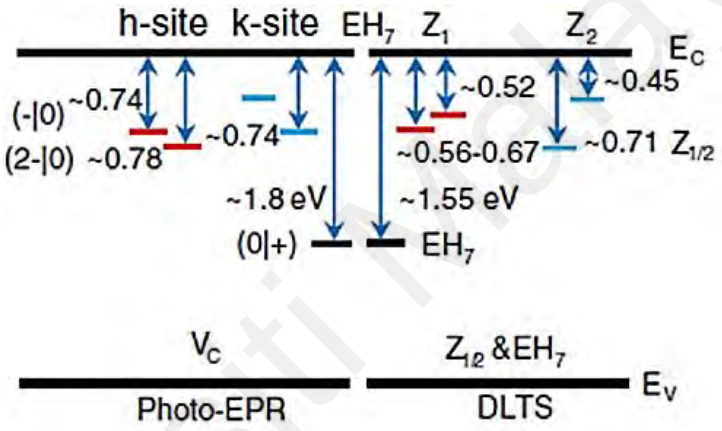


Figure 2.2: Representation of different kinds of energy states in a fully operated 4H-SiC power semiconductor device (Danno et al., 2007; Shenai, 2019).

In the last few years, the various energy states present in high-voltage processed SiC devices have almost been eradicated by thermal oxidation at 1300 – 1400 ˚C or implantation of carbon ion followed by annealing at 1600 – 1700 ˚C (Storasta & Tsuchida, 2007). However, difficulties of mounting additional devices and a rise in the temperature budget are caused by stages of additional fabrication. Presently, diode chips that are contained in 4H-SiC power devices are rated up to 1700 V and 50 A. Chips of GaN/Si power transistors are also rated up to 650 V and 120 A, and they are all commercially available (Shenai, 2019). The production cost of low voltage GaN/Si can compete favourably with silicon-based

devices that will have comparable current and voltage ratings in years to come. Presently, the cost of producing 4H-SiC power devices is about 3 to 5 times bigger than similar devices that are based on silicon. It was previously mentioned that the high cost of production of chips is mainly due to the elevated cost of a wafer, which is also caused by high temperature and slow growth of the physical vapour transport (PVT) process. The bad yield of the wafer is also attributed to the high intensity of defect crystals. But, the major concern presently, is the reliability of WBG in power devices.

In a bid to solve the overwhelming challenges, there is a need to employ optimization, design of technology-driven systems and manufacturing in a top-down manner. There is also the need for a full basic understanding of the significance of crystal imperfections on the cost, performance and reliability of application level of microelectronic structures for the purpose of advancement in technology. In the current society; where we have a non-unified industry, such a task is enormously challenging, if not impossible (Shenai, 2019).

2.4 The Structure of Silicon Carbide

The unit cell of a SiC has a tetrahedron shape, and it comprises of a central silicon atom with four carbon atoms surrounding it (Figure 2.3). Generally, there are nearly 200 polytypes of SiC in existence worldwide (Lohrmann, Johnson, McCallum, & Castelletto, 2017). The three most typical polytypes of SiC are shown in Figure 2.4, they consist of various stacking orders of SiC layers. They are hexagonal (H, α-SiC) and cubic (3C, β-SiC) with the number of SiC double layer compacts denoted by the figure (Parish, Koyanagi, Kondo, & Katoh, 2017). There are lattice sites in SiC that are surrounded by laminates in cubic, and others

with hexagonal form due to possible layering order of components represented by cubic and hexagonal sites, respectively (Lien, 2013). 6H-SiC shows two cubic and one hexagonal site, 2H-SiC contains only one hexagonal, while 3C-SiC possesses one cubic site. All these are shown in Figure 2.5. In addition, 4H-SiC has one cubic and hexagonal site. The 3C-SiC is the only polytype that can be developed on a Si substrate hetero-epitaxially, while 6H-SiC and 4H-SiC polytypes already possessed epitaxy and wafers in commercial quantity. The basic electrical and mechanical properties of the three SiC polytypes, and those for AlN, GaN, Si and diamond are presented in Tables 2.1 and 2.2.

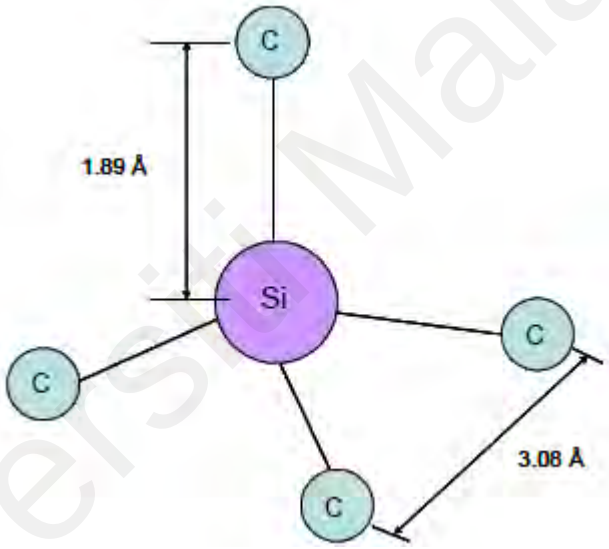


Figure 2.3: The crystal structure of silicon carbide (Lien, 2013)

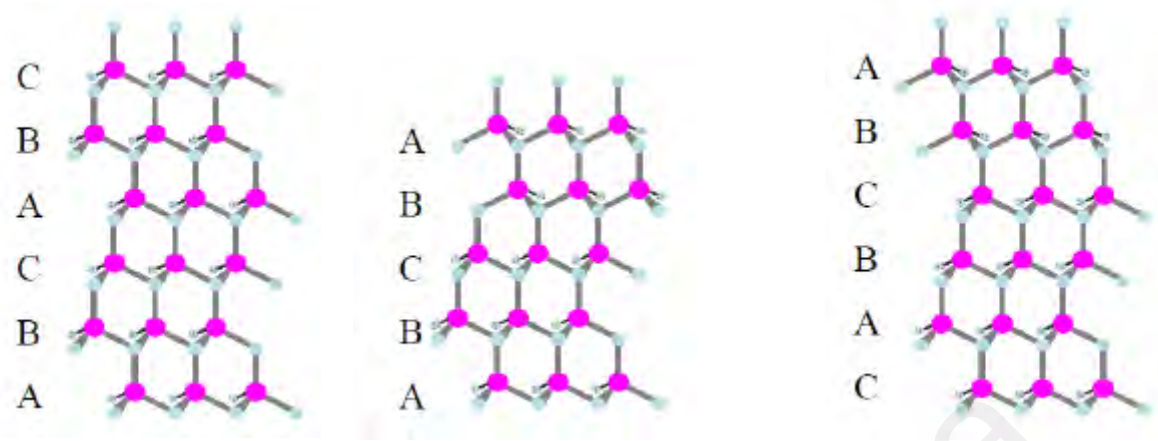


Figure 2.4: Different Polytypes of SiC. (a) hexagonal (H, α-SiC) (b) cubic (3C, β-SiC) (c) rhombohedral (R-SiC) (Lien, 2013)

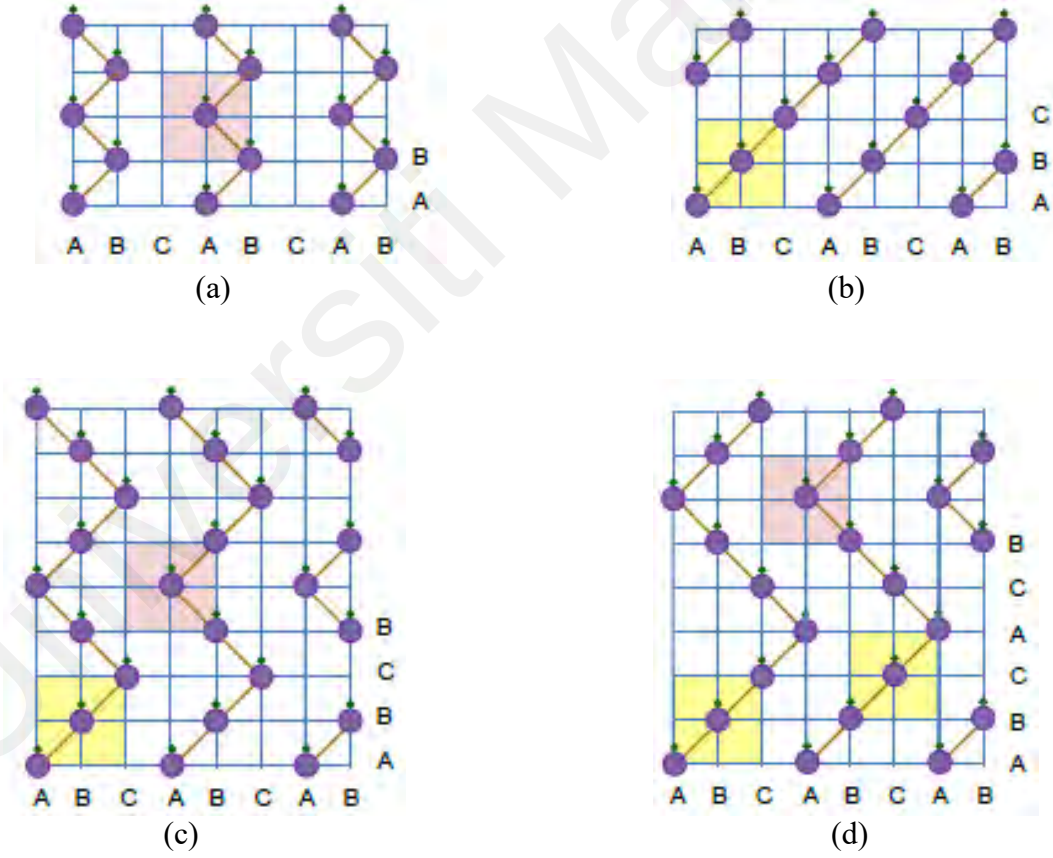


Figure 2.5: Piling of the main polytypes of SiC in bi-layer. (a) 2H-SiC (b) 3C-SiC (c) 4H-SiC (d) 6H-SiC (Lien, 2013).

Table 2.1: Mechanical properties of Si and wide bandgap semiconductors (Ballestín-Fuertes et al., 2021)

Property	3C-SiC	4H-SiC	6H-SiC	Si	2H-AIN	2H-GaN	Diamond
Thermal Conductivity (W/cm K)	3.6	4.9	4.9	1.5	2.85	1.3	20
Melting Point (°C)	2830	2830	2830	1420	3000	2500	4000
Density (g/cm^3)	3.21	3.21	3.21	2.33	3.23	6.15	3.5
Coefficient of Thermal expansion (10^{-6}/K)	3.28	3.3/3.16	3.35/3.25	2.6	5.27/4.15	5.59/3.17	0.8
Mohs Hardness	9	9	9	7	7	-	10
Lattice a (A)	4.36	3.08	3.08	5.43	3.112	3.189	3.567
Lattice c (A)	-	10.08	15.12	-	4.982	5.185	-

*Note: If the coefficient of thermal expansion has two numbers, one is meant for the a-axis and the other for the c-axis.

SiC is very suitable for micro-electromechanical systems (MEMS) due to its excellent mechanical properties. MEMS that are based on SiC have been employed in pressure and temperature sensors, especially in an environment of elevated temperatures (Marsi, Majlis, Hamzah, & Mohd-Yasin, 2015), such as strain sensors (Senesky, Jamshidi, Cheng, & Pisano, 2009), biomedical sensors (Phan, Dao, Nakamura, Dimitrijev, & Nguyen, 2015), and high-g accelerometers (L. Jiang & Cheung, 2009). They may also be used for resonators of high frequency as filters and micro-mechanical oscillators owing to their high E/ρ ratio. The frequency of resonant of a micro-machined system can be written as

$$F = C\upsilon\sqrt{\frac{E}{\rho}} \tag{2.1}$$

where υ is a function of Poisson's ratio, ρ is the density of the material, E is the Young's modulus and C is constant. SiC can be employed for high frequency, high temperature, high power and applications for radiation resistance devices. For instance, its wide bandgap properties make SiC more suitable for use in high thermal applications (Östling, Ghandi, & Zetterling, 2011). In addition, the strength of the breakdown electric field is perhaps the most significant feature for high power systems: the maximum E of SiC is ten times that of silicon.

The saturated electron drift velocity of SiC is about double the amount of silicon, which has allowed microwave devices to attain high channel currents as high-frequency systems (Pengelly, Wood, Milligan, Sheppard, & Pribble, 2012; Lien, 2013).

2.5 Physical and Electrical Properties of SiC

SiC displays higher thermal conductivity that is (3 times), saturated carrier velocity (2 times) and critical electric field (7 times) in comparison with the common semiconductor materials, such as GaN and silicon (S. K. Lee, 2002). The main electrical properties of these materials showing their comparison are presented in (Table 2.2). From the table, it was observed that silicon is significantly larger in concentration of intrinsic carrier when compared to other wide bandgap semiconductors. The operation temperature of Si-based devices is limited to about 150 ˚C by the aforementioned property (Sze, Li, & Ng, 2021). Owing to the deliberate doping of the material, the number of free carriers is exceeded by the amount of thermally produced electron-hole pairs at this temperature, and at this stage, the component becomes more intrinsic leading to a system failure. In comparison, the wide bandgap and smaller intrinsic density of SiC carrier permit it to attain a temperature of about 700 ˚C before functioning in the intrinsic area.

Table 2.2: The electrical properties of some wide bandgap semiconductors at room temperature (She, Huang, Lucía, & Ozpineci, 2017).

	SiC				
Properties	**3C-SiC**	**4H-SiC**	**6H-SiC**	**Si**	**GaAs**
Energy Bandgap (eV)	2.2	3.2	3	1.12	1.43
Breakdown field strength (V/cm)	20×10^5	22×10^5	25×10^5	3×10^5	4×10^5
Maximum electron saturation velocity (cm/s)	25×10^6	20×10^6	20×10^6	10×10^6	10×10^6
Maximum operation temperature (°C)	1580	1580	1580	600	400
Hole mobility	40	120	80	480	400
Electron Mobility ($cm^2/s.V$)	1000	980	370	1350	8500
Critical Field, E_C (MV/cm)	1.2	2.2	-	0.3	3.3
Interior Carrier Concentration, n_i (cm^{-3})	$\sim 10^0$	$\sim 10^{-8}$	-	$\sim 10^{10}$	$\sim 10^{-10}$
Dielectric Constant, κ	-	-	-	9.7	9.9

From the above relationship, it was observed that the critical electric field for Si is almost ten times lower than that of 4H-SiC. This value has a relationship with the bandgap energy of a semiconductor material; a property which indicates that it will support higher electric fields when used for the breakdown of the avalanche. The lower strength of the critical electric field of Si compared to 4H-SiC implies that, for an equivalent thickness of drift area, 4H-SiC can sustain around ten times the voltage prior to breaking down. The comparison between the breakdown voltage, and the theoretical limit of specific on-resistance against breakdown voltage for Si, GaN and 4H-SiC are shown in Figure 2.6. From the figure, it can be observed that for an equivalent level of breakdown voltage, 4H-SiC devices provide extremely lower specific on-resistance (around 350 times) than their Si counterparts. In addition, the thinner area of drift of 4H-SiC indicates that they can be operated at smaller switching losses and larger frequencies. The thermal conductivity of Si is approximately three times lower than 4H-SiC, which gives it the ability to be able to reduce

the criteria for big, large heat sinks and cooling devices. This is another great benefit for applications in power electronic systems.

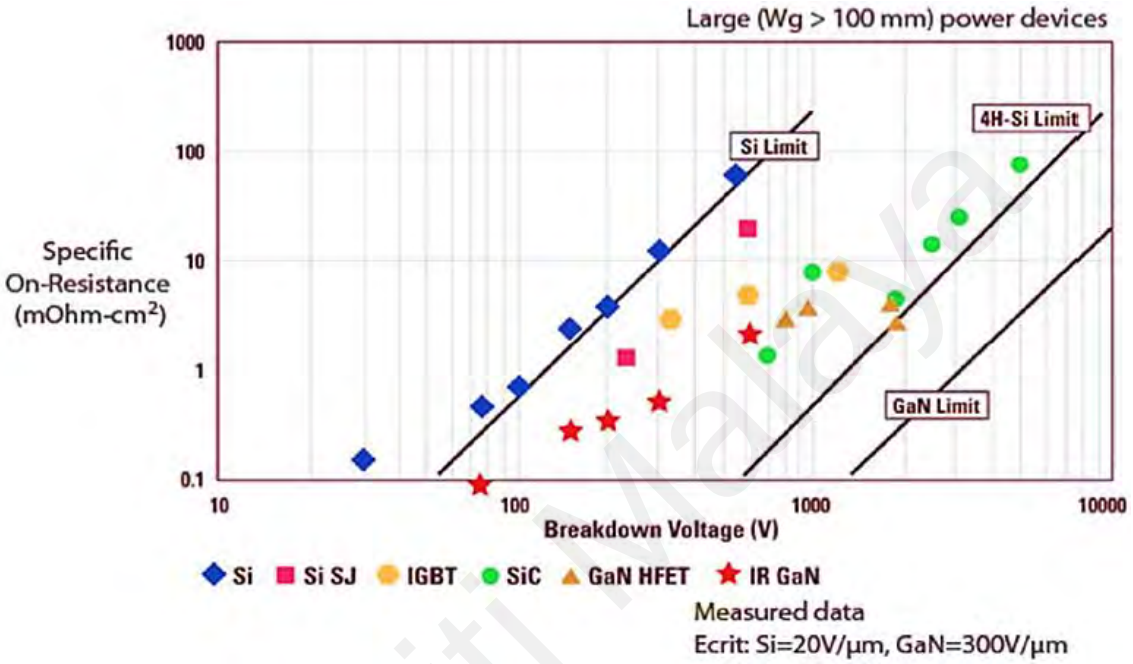


Figure 2.6: Specific on-resistance against breakdown voltage for 4H-SiC, Si and GaN (Ikeda et al., 2008).

According to Table 2.2, where the comparison between Si, 4H-SiC and other semiconductor materials with respect to their demerits was presented. It was observed that 4H-SiC material has a lower mobility carrier of both holes and electrons. A lower mobility implies a higher on-state losses and even a larger on-resistance. Although, the 4H-SiC may possess a thinner and more largely doped drift area than that of Si which can reduce this demerit. It is worthy of note, that the mobility values stated in the table were meant for large materials. However, the surface mobility of 4H-SiC-based semiconductor systems is considerably smaller than that of the bulk material, owing to the low quality of the interface

between SiO_2 and 4H-SiC. The low mobility of interface channel results in large on-state losses and even a great resistance to the channel (Rong, 2015).

2.6 Metal Oxide Semiconductor (MOS) Structure and Device Fundamentals

Due to the increasing demand for power conversion devices, there is great attention towards the use of SiC-based metal oxide semiconductor field effect power transistors (MOSFETs) for applications in high-performance power switching devices, such as motor control, electric power transmission, electric hybrid vehicles and power traction (Kimoto, 2015; Kodigala, Chattopadhyay, Overton, Ardoin, & Gordon, 2015; Yifan Jia, Lv, Song, Tang, & Xiao, 2017; Ballestín-Fuertes et al., 2021). The electrical features of SiC-based power devices are inexhaustible, even though they have been in commercial existence for some time (Nawaz, 2015). The growth of SiC bulk crystals was characterized by some challenges, and one of the solutions in terms of cheap and bulk wafers is hetero-epitaxy on silicon substrates (La Via et al., 2018). However, the difference in coefficients of thermal expansion, and that of lattice mismatch have become challenges to contend with, so as to obtain excellent grade silicon carbide films (Anzalone, Litrico, Piluso, Reitano, & Alberti, 2017). The large gaps created at the interface is as a result of a high concentration of imperfections, such as stacking-faults, twins and misfit dislocations at the interfacial layer.

In a bid to enhance the quality of the oxide layer, a carbonized silicon carbide layer which is derived from the reaction of the carbon precursor and the silicon surface is introduced. This process has been studied extensively in previous researches. Although, it was originally introduced by (Nishino, Powell, & Will, 1983). The method has been

influential largely on the properties and quality of oxide films. Normally, the thin film layer on Silicon carbide was developed by injecting propane under low-temperature hydrogen flux. Then, the temperature was raised to the temperature of growth and the silicon precursor was inserted to form a thick layer of SiC (Anzalone et al., 2017; Dushaq et al., 2017).

A typical MOS structure is shown in Figure 2.7. It is comprised of three layers, namely; a conducting metal electrode as the upper layer, a gate oxide as the interface, and a substrate as the bottom layer. The arrangement is one of the most essential and widely used systems in electronics, especially in ICs. In MOS structures, the two-point semiconductor is the simplest, and is usually manufactured and used for electrical performance analysis. In particular, the electric field and the charge of the semiconductor under various static biasing situations can be measured numerically.

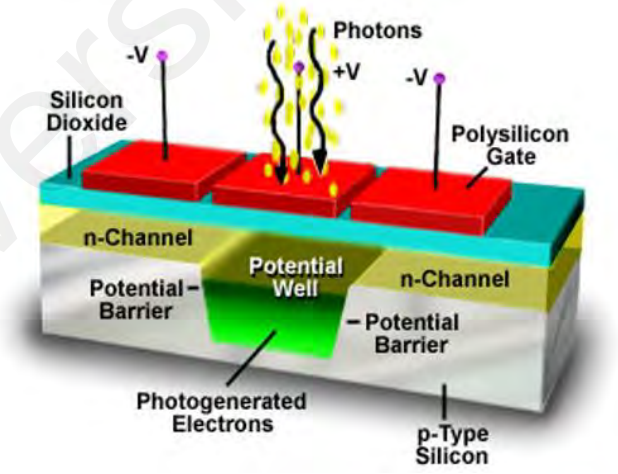


Figure 2.7: Structural diagram of a Metal-Oxide-Semiconductor capacitor (Abramowitz & Davidson, 2019).

2.7 Wide Bandgap Semiconductor

Wide bandgap materials possess several characteristics that make them suitable compared to materials that are made of narrower bandgap. These characteristics include higher energy gap which gives semiconductor devices the ability to operate at harsh and extreme environmental conditions. They were basically developed due to necessity for extension of the semiconductor industry concerning light management, high-frequency and high-power components. Even though, the properties and structure of the majority of the WBG semiconductors have been in the public domain, the development of different techniques of growth has led to the combination of components with outstanding properties, good control of stoichiometry, and low defect concentration.

The viability of SiC as a candidate for high-power and thermal applications has been discussed emphatically in this section, owing to its radiation hardness and its attraction to nuclear and aerospace industries. Its property as a WBG semiconductor permits it to function at temperatures of about 900 ^{o}C due to its ability to generate low heat, and also allows processes to be performed at high switching frequencies. Another material that has potentials for applications in high-power devices but requires high processing temperatures is diamond. GaN is also a good candidate for a WBG semiconductor, which has the potentials for use in radio frequency and high-power structures. It is used for light production and non-luminescent sources owing to its affinity for cool lighting devices and its direct band gap, such as light-emitting diodes (LEDs).

Despite the fact that SiC was used in the development of the first blue LED, there is very low efficiency recorded owing to the indirect feature of the energy gap. Therefore, a more conscientious effort was deployed towards the study of SiC for the development of

high-efficiency LEDs, GaN and its alloys, and laser diodes that offers visibility up to the range of ultraviolet (Ashutosh Sharma, Lee, Jang, & Jung, 2014; Katsikini, 2015). Ultra-wide band-gap (UWBG) β-gallium oxide (β-Ga_2O_3) has displayed some superior electronic properties for developing power and radio frequency (RF) structures with enhanced size, weight, and power (SWaP), and better performance over newly acquired wide bandgap structures that are SiC and GaN-based. However, the β-Ga_2O_3 device is characterized by self-heating, and that is seen as a major challenge that the technology will encounter. Normally, one would have expected that β-Ga_2O_3 structures possess higher power densities than WBG counterparts. However, the thermal conductivity of β-Ga_2O_3 is about 10 - 20 W/m K, which is considerably lesser than the thermal properties of GaN or SiC. It is therefore concluded that thermo-mechanical reliability issues could be caused by large temperature gradients formed in β-Ga_2O_3 devices during operation (Chatterjee, Leach, Dhar, & Choi, 2018).

WBG has been applied extensively in many sectors such as automotive, avionics, nuclear plant, etc. Their materials demonstrate a higher electrical breakdown field, which allows devices to be operated at a higher voltage. For instance, the Si Schottky barrier diode has a blocking voltage of 100 V. However, it has attained the peak blocking voltage of 1700 V. Consequently, SiC material is much easier to be used in high voltage applications such as junction barrier Schottky (JBS) and MOSFETs. The thermal conductivity of SiC material is 4.9 W/cm ^oC, which is approximately 3 times higher than Si material. Its implementation in an integrated circuit can eliminate or decrease the cooling system, which successfully lessens the weight and volume of a system thereby enhancing its integration. In addition, SiC material has a large maximum electron saturation velocity, which indicates that it has a faster switching speed and higher current density which makes it more appropriate for devices that require high frequency and high power (She et al., 2017).

2.8 Features of SiC-Based Power Device

SiC is a semiconductor material that offers numerous benefits over silicon in terms of its bandgap, breakdown energy, and a broad range of p- and n-type features meant for the compound. The high breakdown energy of SiC has been attributed to the realization of higher voltage (600 V to thousands of V) structures configured by a higher impurity concentration and thinner drift layer. It can also withstand greater voltages that have very low ON-resistance, since the majority of the high-voltage devices with resistance components are located in the drift layer. The newly developed semiconductor materials are gaining attention as an alternative for applications in thermal and power devices. With the progress made so far in semiconductor technologies, various forms of silicon (Si)-based devices have been developed for specific functions, and in the process, a balance has to be struck between efficiency, cost, robustness and complexity. Figure 2.8 presents the relationship between the capacity of various silicon-based devices and their frequency of operation. It was shown in the figure that the selection of different devices is determined by one trade-off.

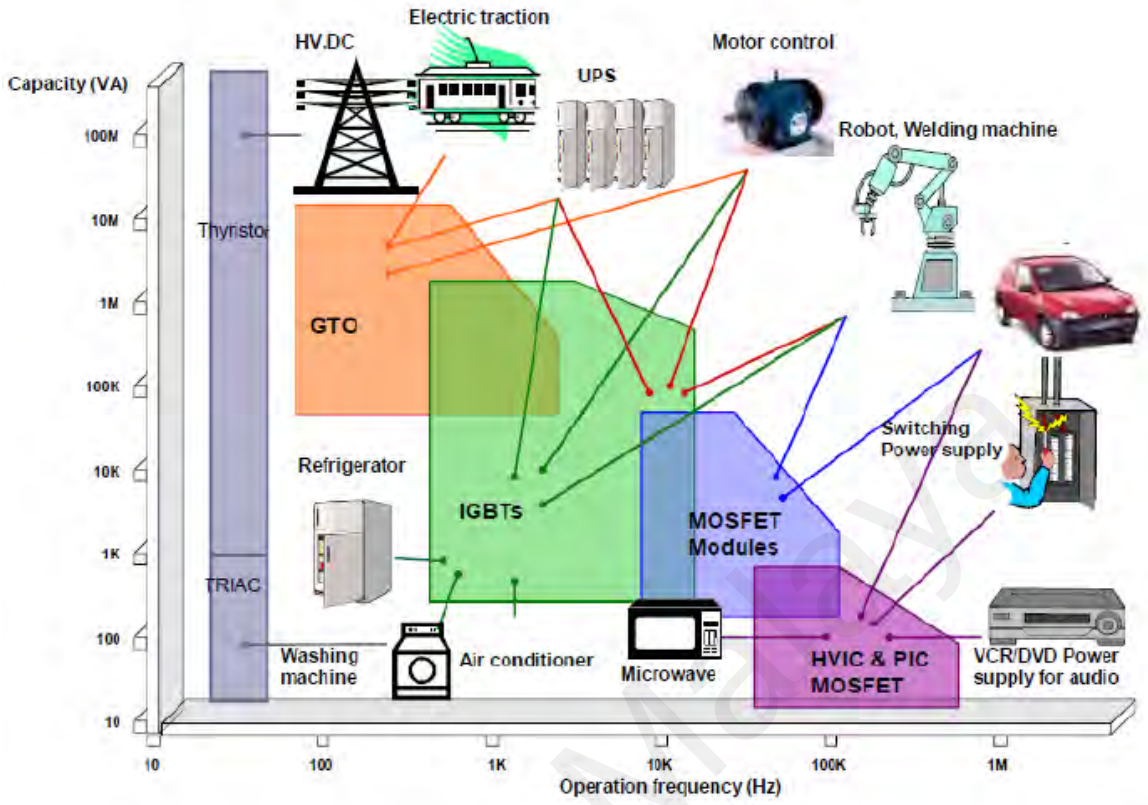


Figure 2.8: Different Si-based devices and their applications (Chan, 2018)

The fundamental limitations of Si devices have negatively affected the frequency of their applications, and this has caused significant attention to be paid to wide bandgap materials such as SiC-based MOSFETs and GaN, owing to their excellent properties, such as high electron mobility, high saturation velocity and critical field. These materials are now being considered frontiers in the semiconductor industries. Figure 2.9 presents the current application of Si-based devices and that of the new frontiers.

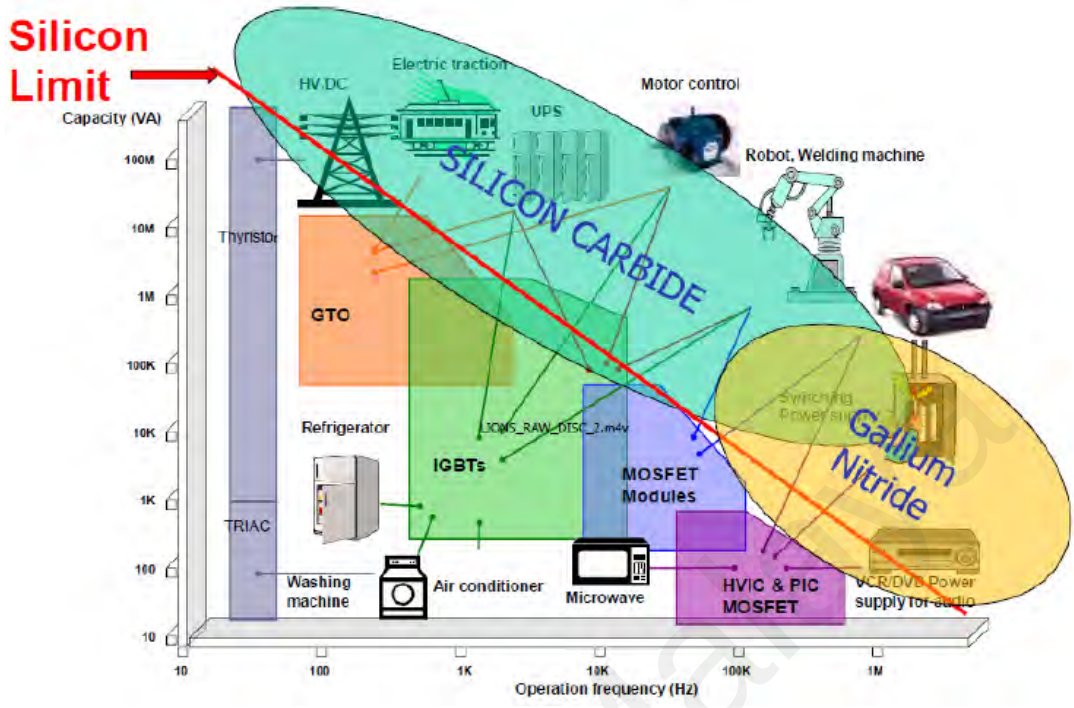


Figure 2.9: Present situation of Si devices with the new frontiers powered by SiC and GaN (Chan, 2018)

SiC-based structures offer various benefits in different applications, such that it permits extremely high voltage and a wide range of temperatures. However, the capacity of most components for thermal applications, especially Si-based devices have not attained the same height of development. The peak temperature obtained at the junction in a Si-device is 150 °C. This limitation as well as poor switching frequency makes it inappropriate for use in several applications. In order to make provision for tolerance in terms of low temperature, the silicon IGBT design was made from a complex hot reservoir with a peak switching frequency of about 30 kHz. The resultant effect was that the structure becomes cumbersome passive components with poor dynamic performance and low power density. However, it is difficult to record significant progress in systems with power conversion by using Si semiconductor devices or simple technological production. The drawbacks of Si-based

devices are apparent and thus reduce their uses in power electronics and industrial components (Hazra, De, Cheng, Palmour, & Bhattacharya, 2015; X. Guo, Xun, Li, & Du, 2019).

2.9 SiC as Alternative Substrate for Silicon

One of the most commonly used semiconductor components for power applications is silicon. However, structures that are based on silicon materials are reaching their usage limits, and that has necessitated a lot of effort to search for substitutes for enhanced efficiency. Considering the rate of technological advancements and progress in the semiconductor industry, high-performance and high-power density devices are sustainable replacements for silicon-based structures that were transformed from developed models in the laboratories. Even though, the cost of silicon is much cheaper than SiC, applications and uses of SiC-based devices are becoming more prominent where the benefits of the technology can provide far-reaching advantages that are capable of clearing the rising cost of the devices. In spite of the availability of numerous SiC-based devices in commercial quantities, the market has not attained its peak and most of the designers that are considered potential users are still struggling to familiarize themselves with the new development (H. Choi, 2016; Chan, 2018).

As a replacement for silicon-based technology, SiC is now considered a choice material for the future. The composition of silicon carbide is done in such a way that it combines an equal amount of the two components via covalent bonding. Although, a mono-crystalline SiC structure is very difficult to get because the process of manufacture will lead to a highly structured arrangement; it is even considered the third hardest material in existence. The bandgap of SiC is between 2.2 and 3.3 eV depending on the configuration.

2.10 Similarities between Si-Based and SiC-Based MOSFET

SiC-based electronics are similar in vertical structures to that of Si. Si-based MOSFETs usually offer a better balance between switching losses and conduction (She et al., 2017) owing to their charge and low ON resistance. The theoretical reduction in power loss may be attained when Si-IGBTs are replaced by the ones based on SiC with equivalent specifications (Figure 2.10).

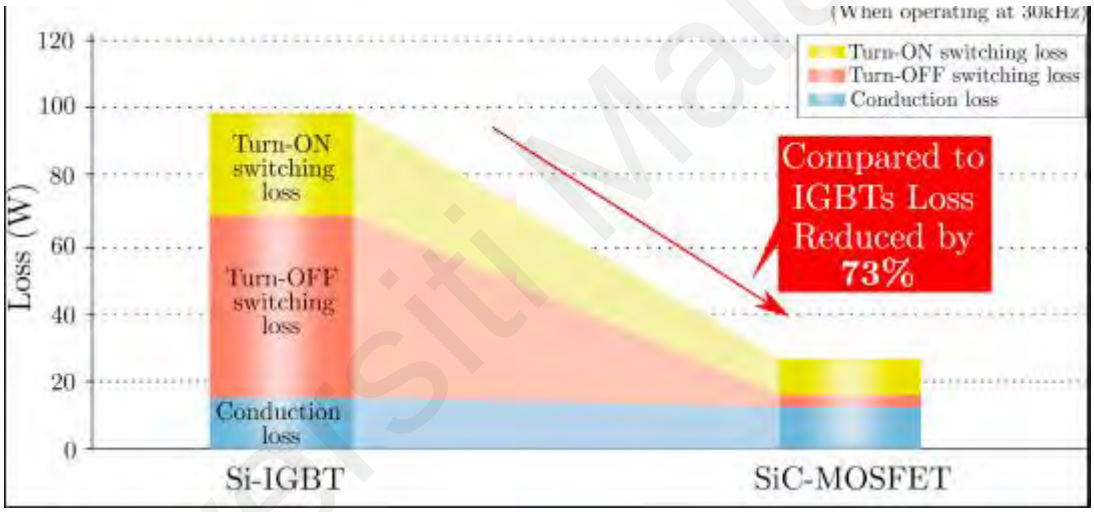


Figure 2.10: Reduction in Power loss attained using SiC MOSFET in comparison with Si-based IGBT (She et al., 2017).

Another significant characteristic of SiC is that, it can be powered by the circuitry of a similar driver as that of Si-based IGBTs (the reference for energy converters in HEV/EV propulsion devices), making the conversion between both systems easier. In addition, they can be operated in the absence of anti-parallel outside diode, due to the ones contained in the architecture of the transistor (Pala, Van Brunt, Ryu, Hull, & Hefner, 2016; She et al., 2017; Soler et al., 2017). Owing to a good result that can be obtained from optimized and outside

diodes of JBS, there is a need for analysis of the solution for every application. Values of Charge (Q_{rr}) are the same as the charge (Q_g) of the gate MOSFET. Generally, SiC MOSFETs are currently receiving the most attention in terms of research on the application of high-power electronic devices. For instance, the enhancement of the long-term stability of the threshold voltage and important developments are constantly reported (Östling et al., 2011; Green, Lelis, & Habersat, 2016; Pala et al., 2016). Also, a significant landmark was the inclusion of the super low R_{on} SiC-based semiconductors that depend on the structure of the trench gate.

Concerning current and voltage ratings of some components (ranging between 2.6 and 100 A, and 400 – 1700 V), their application in HEV/EV propulsion is made possible by the use of devices that have a larger range of current. Numerous manufacturers are developing complete modules of SiC-based MOSFET in that manner (Menghal & Laxmi, 2010). HEV/EV propulsion inverters may be developed using a cheaper parallel of modules, dies or digital devices. It can be deduced from available literature, and all the advantages of SiC-based semiconductors that have been mentioned above, that they offer superior properties for applications in HEV/EV among other WBG semiconductors (Matallana, Ibarra, López, Andreu, & Rebollo, 2019).

2.11 Application of SiC-Based Electronic Devices

2.11.1 SiC Power Electronics

The performance of devices that are based on SiC has been improved over the past few years i.e, there has been a considerable drop in voltage, superior stability of parameters and

higher operating temperature. All of these have been made possible due to enhancement of the growth process in the bulk material, design and fabrication technique of the device (Biela, Schweizer, Waffler, & Kolar, 2010; Millan, Godignon, Perpiñà, Pérez-Tomás, & Rebollo, 2013). Consequently, the solution for applications in high power and voltage devices was proffered, since the physical parameters of SiC permit the fabrication of tiny chips with smaller sizes depending on the capacitance and capabilities of high changing speed (She et al., 2017). Introduction of this new technology is supported by the power electronics sector, and this can be confirmed by the available commercial data and its future prospects (Figure 2.11). The summary of various traction inverters of Si and SiC, and different highlights is presented in Table 2.3.

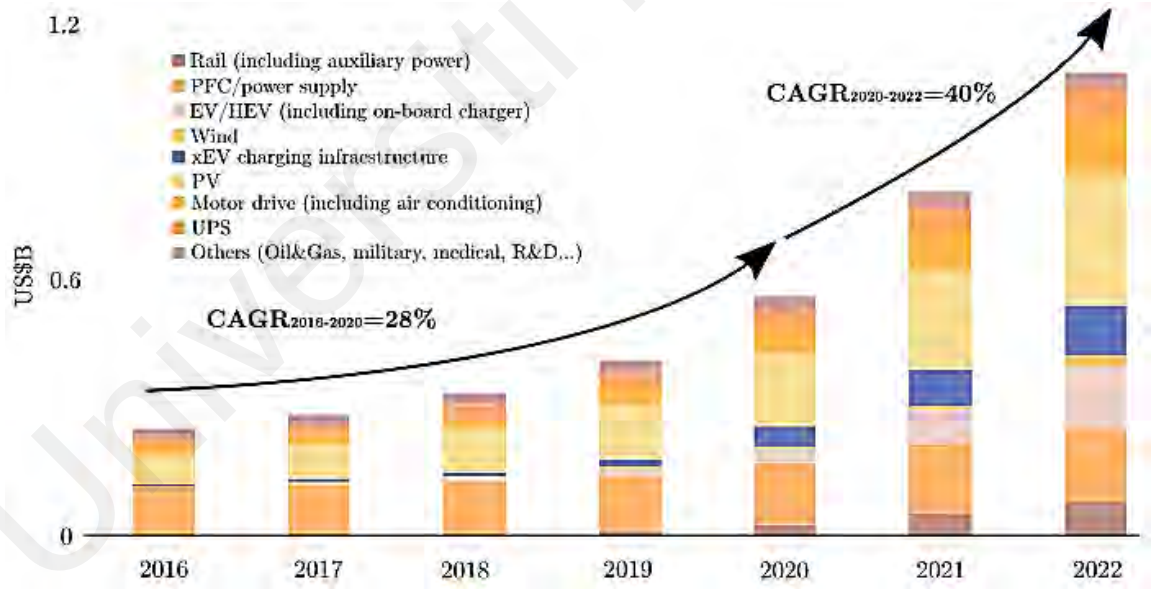


Figure 2.11: Current status of the SiC market and future prospects (Matallana et al., 2019).

Table 2.3: Different Si and SiC-based inverters with their relevant operating data.

Full SiC inverter	**Power (kW)**	**Power density (kW/l)**	**DC bus voltage (V)**	**Efficiency (%)**	**Refs**
Ev Inverter	88	21.5	900	-	(Jeffrey Casady et al., 2017)
Ev Inverter	60	160	800	92.3 - 99.1	(Matallana et al., 2019)
Ev Inverter	80	-	800	99.50	(H. Kim, Chen, Zhu, Maksimović, & Erickson, 2016)
Ev Inverter	30	15	250 – 800	99.50	(J. Zhu, Kim, Chen, Erickson, & Maksimović, 2018)
Ev Inverter	100 peak	34	400	-	(C. Zhang et al., 2018)
Ev Inverter	60	34	400	-	(Morya, Gardner, Anvari, Liu, & Toliyat, 2019)
Ev Inverter 1200 V half bridge modules	110	17	200 - 450	Mean 96.3 & Peak 98.9	(Morya et al., 2019)
Ev Inverter	120	160	800	96.8 - 99.3	(Matallana et al., 2019)
Commercial Si inverter	**Power (kW)**	**Power density (kW/l)**	**DC bus voltage (V)**	**Specific Power (kW/kg)**	**Refs**
Motor inverter for Nissan leaf 2012	80	5.7	380	4.9	(Burress, 2014)
Motor inverter for 2004 Prius	50	5.75	200	5.68	(Sarlioglu, Morris, Han, & Li, 2016)
Motor Inverter for 2010 Prius	60	11.11	200	16.67	(Sarlioglu et al., 2016)
Motor Inverter for 2007 Camry	70	11.67	250	9.33	(Sarlioglu et al., 2016)
Motor inverter for 2008 LS 600h	110	17.19	288	14.86	(Sarlioglu et al., 2016)

Most of the devices that were analyzed are enclosed in D3PACK or TO-247 packages, with comparable values of temperature resistance. They are; the highest blocking voltage of the power structure during the OFF state, V_{block} (V), maximum repetitive drain to source voltage, which is denoted by VDS_{max} for BJTs, JFETs and MOSFETs and the highest repetitive reverse voltage, V_{RRM} for diodes. The highest HEV/EV voltage of the battery must be lower than the V_{RRM}, which includes a security margin that has been provided (usually

around 1.5× or 2× factor), owing to the peaks of voltage that were developed along the systems during commutations (Matallana et al., 2019).

Another parameter that is denoted by (continuous ON-state DC drain current), I_D is I_{max} (A), the highest current of the device during the transmission state, which is provided for I_S/I_F diodes, BJTs, JFETs and MOSFETs by manufacturers. The number of power electronic systems to be arranged in parallel for each switch will be determined by the variables and the total current for each phase of the system converter. Mainly, I_{max} is limited thermally, which relies on the junction-to-case temperature resistance of the system. The parameter that determines the highest permissible thermal junction of the system is T_{jmax} (°C), which also depends on the reliability of manufacturers' data. The reduction in nominal device lifetime is surpassed extremely by the temperature (Lutz, Schlangenotto, Scheuermann, & De Doncker, 2011). The device must be designed thermally and electrically in a manner that the highest thermal application is smaller than the highest temperature of the semiconductor under which condition it switches.

The parameter that denotes an indication for unit polar JFETs and MOSFETs devices, drain to source ON-state resistance by the manufacturer is called R_{DSon} (mΩ). Some manufacturers of BJT abandon the collector-to-emitter offset drop in voltage and also offer the same value of R_{DSon} as a major parameter of conduction. This parameter defines the losses in power conduction along with the current of the instantaneous conduction of the device. In order to achieve a balanced distribution of current for every parallel semiconductor, the temperature coefficient of R_{DSon} must be positive. The manufacturers of BJTs, JFETs and MOSFETs offer R_g (Ω), known as internal gate resistance, as R_{gint}. It relies on the size of the semiconductor, where a larger size is equal to a larger value of resistance. The area of a SiC-

based semiconductor is less than that of Si if the same current is applied. But, for the avoidance of disruption of dielectric gates, they must have the lowest value of gate resistance. Therefore, an external resistance (R_{gext}) is generally incorporated to act as a solution to this problem. Both $R_g$ext and $R_g$int resistances have a straight effect on other parameters such as switching losses and speed.

V_f(V) employed in diodes and double polar devices is called the forward voltage drop. This parameter is provided at fixed values of temperature and current in spreadsheets, depending on both parameters. The parameter that identifies the charge stored in the dependent input capacitance between the terminals source and the gate, which also affects the dynamic performance of the system is called total gate charge, Q_g (nC). More so, this parameter defines the design aspects of a driver, because it must offer adequate switching power. This technology is more stable for SiC devices that are not temperature-dependent than that of Si during switching.

2.11.2 SiC-Based Sensors for High Thermal Uses

There has been significant improvement in the processing technology and development of SiC sensor material in the last few years (Wright & Horsfall, 2007). Numerous stages of SiC have been improved upon for applications in high thermal environments, such as pressure, gas and ultraviolet sensor. Some of the SiC-based sensors and their performances are discussed in the following sub-sections.

2.11.3 Ultra-Violet (UV) Sensor

An ultra-violet sensor that is made of SiC is the first WBG photo-detector that was available in the market, and was based on P-N diode (Lien, 2013; Monroy, Omnès, & Calle, 2003). Its major benefit is the low reverse current, which is approximately 2×10^{-7} A/cm^2 at 350 °C and -10 V, 10^{-9} A/cm^2 at 200 °C, and 10^{-13} A/cm^2 at room temperature for 6H-SiC photo-diode (Lien, 2013). The responsivity of the peak usually drops to a range of 0.15 – 0.175 A/W at 270 nm and 25 °C, which corresponds to a considerable efficiency of between 70 – 85 %. The long wavelength responsivity rises and the peak response shifts towards the red, when the temperature increases from -50 to 450 °C. The corresponding significant efficiency ranges between 82 and 96 % (Lien, 2013). Another type of semiconductor photo-detector (PD) has also been fabricated using SiC-based nanocrystalline for applications at temperatures up to 200 °C assisted by ion-beam deposition (Waye, 2016). The metal-semiconductor-metal (MSM) photo-detector works at high speed and can be integrated easily with MEMS and optoelectronics for the detection of signals.

2.11.4 Pressure Sensor

A typical Si-based pressure sensor requires a cooling system, and is also limited in temperature, while the ones that are SiC-based can function at elevated thermal environment (Bose, 2010; Aranzabal, de Alegria, Garate, Andreu, & Delmonte, 2017). Both thin film and bulk SiC are used as support for SiC-based pressure sensors. Micromachining of bulk SiC diaphragms has been used for the design of pressure sensors. A capacitive SiC pressure sensor of the polycrystalline structure was packaged and fabricated in high-thermal ceramic by (Schneider-Ramelow, Baumann, & Hoene, 2008). It can detect approximately 0.7 MPa

with a sensitivity of 7.2 μV/psi at 574 °C, and ~ 5.17 MPa with a sensitivity of 251 μV/psi at 300 °C. A piezo-resistive pressure sensor was created from a 6H-SiC diaphragm using an epitaxially deposited n-type and photo-electrochemically etching device (Neeb, Teichrib, De Doncker, Boettcher, & Ostmann, 2014). It can detect almost 6.9 MPa at 600 °C with the least junction leakage, and without permanent deformation.

A pressure sensor can also be made from other thin films deposited on SiC substrate with prospective bulk manufacture. Another capacitive SiC pressure sensor that was deposited on Si was proposed by Wen et al., (2012). The range of linear change of capacitance with pressure applied is between 22.2 and 31.2 per inch of absolute pressure (psi) at 500 °C. The sensitivity decreases to 0.53 pF/psi at 500 °C from 0.62 pF/psi (Lien, 2013).

2.12 Power MOSFETs in SiC

Power switches are regarded as the control unit of virtually all power electronic devices. Its affordability in a considerable amount of applications has been made possible due to the low cost of power, easy control, and high power capabilities. Bipolar and thyristors are the first set of power switches that were developed in the 1950's. Thyristors were employed in large power devices due to their specifications that are increased to a higher speed than that of bipolar transistors. The latter were preferred for their applications in medium and low-power devices due to their rapid switching capabilities. The specifications of these electronics improved gradually until the mid-1970s, when the first power MOSFET was introduced.

Si-based MOSFETs have been greatly improved and have become the leading power system since the discovery of the first power MOSFETs for various applications in the 1980s.

Their use in many devices was for several reasons. First, MOSFET possesses an extremely large input of impedance owing to its metal oxide gate arrangement, which also offers the easiest requirements in gate structure. The development of either accumulation or inversion layers under the channel of the metal oxide semiconductor can be determined with the use of integrated circuits (ICs) due to the low gate current that is meant to discharge and charge the large input oxide of the capacitance. Secondly, MOSFET is a large device carrier, which means there is no low storage of charge that is required in its activity. The ability to discharge and charge the input capacitance is controlled by the switching time of MOSFET.

Thirdly, MOSFETs have forward biased safe operating area (FBSOA) and better strength compared to bipolar transistors which permit the removal of snubbed circuits for guarding the switch during activity in a normal application of hard-switching. Fourth, the thermal runaway performance is avoided in MOSFETs as the bulk carriers in silicon displays an increasing temperature and resistivity. In order to benefit from the thermal performance of MOSFET cells, the devices are made as parallel arrangements of collections of individual MOSFET components. Any excess current carrying device will be heated up at an increase in resistance with the current diverted into parallel tracks. If the dependent BJT does not perform, the temperature failure can generate excessive loss without an unstable runaway influence.

Owing to its superior electrical features, it is appropriate to use power-based MOSFETs for large power/voltage system devices. However, the MOSFETs blocking voltage capacity depends on the ratings of the opposite body diode at the drift area. The blocking voltage is

obtained partially by the displacement between the source and the drain. Large blocking voltage capacity indicates large resistance due to the size, so there is an exchange between the device voltage capacity, values, R_{on}-drift and resistance at the low drift area. The exchange between the voltage capacity of the device and the low on-state resistance prevents the large power/voltage devices from their benefits (Linewih, 2003).

2.13 4H-SiC MOSFETs

Carrier mobilities can be significantly reduced in the major part of the insulator, owing to its scattering on the surfaces and interfaces of semiconductors. For years, the progress in SiC-MOS devices has been hampered by challenges due to the high concentration of interfacial traps in the power gap, indicating unsatisfactory mobility of channel-carrier (Ueno, Asai, & Tsuji, 1998; Cabello et al., 2018) and reliability oxide (H.-F. Li, Dimitrijev, & Harrison, 1998; Jamet, Dimitrijev, & Tanner, 2001). However, significant developments on nitrided SiO_2/SiC interfaces have been reported by (Yoshioka, Nakamura, & Kimoto, 2012; Kimoto, 2015), which resulted in the recently developed 4H-SiC MOSFET with improved reliability and high values of inversion-layer mobility. The 4H-SiC MOSFETs planar N-Channel with a diameter of 800 μm and nominal length which ranges between 5 and 50 μm were manufactured using a parallel method. A P^+ 4H-SiC wafer was used as the base component, on which a P-epitaxial layer with a little doping of 5×10^{15} cm^{-3} was grown.

The deposition of thin oxide film was done at Griffith University using the conventional method; i.e oxidation of the gate in nitric oxide (NO) for 1 hour, at 1150 °C. The main oxidation was done in dry oxygen for 5 hours at 1150 °C, and nitridation of the interface by

annealing in nitric oxide for 1 hour at the same temperature. The thickness of the oxide formed was 43 nm as identified by the bulk capacitance of the C-V curves taken at 1 MHz. After oxidation, the samples were placed in a nitrogen-filled plastic container. The container was then covered and air-tightened, which was later shipped to a company called SiCED Electronics Development GmbH & Company in Germany for further processing (Linewih, 2003; Singh, Jain, & Kumar, 2019).

2.13.1 The SiO_2/SiC Interface

The layer between the semiconductor and the oxide film depends strongly on the substrate and its orientation. Unlike the features of the large SiO_2 concentration, the interface quality is directly shown in the channel mobility of MOSFETs, which is an important characteristic for components as explained earlier.

2.13.1.1 Scattering Mechanisms

The true (Hall) mobility μ is defined as

$$\mu = q\tau m \tag{2.2}$$

where τ is the average scattering time in charge of the finite speed $v = \mu\xi$ of the carrier in a solid. q is the charge in coulombs, while m denotes the mass. Since different processes can cause scattering, τ can be broken down into Equation (2.3)

$$\frac{1}{\tau} = \sum_i^0 \frac{1}{\tau i} = \frac{1}{\tau ph} + \frac{1}{\tau Cb} + \frac{1}{\tau lt} + \frac{1}{\tau rg} + \cdots \tag{2.3}$$

Here, the contributing processes are coulomb scattering by charged centres, carrier trapping or recombination, surface roughness-induced scattering and carrier-phonon connections,

respectively. Combining Equations (2.2) and (2.3), the true mobility can also be expressed as

$$\frac{1}{\mu} = \sum_i \frac{1}{\mu i} \quad (2.4)$$

The dominant process can be obtained from the dependence on the thermal mobility of the electric field (Bandaru, 2020).

At the oxide/semiconductor interface, defects and surface-induced states can result in limited levels of energy contained in the band gap. For n-channel devices, the formation of an electron inversion layer is done when the amplitude of the positive gate bias is big enough for the Fermi level to surround the conduction of the device band edge near the interface. In that case, most levels around the bandgap are occupied with electrons which decreases free carriers' density and produces negatively charged centres. In the long run, it results in a reduced carrier lifetime and enhanced Coulomb scattering. Therefore, the mobility in the channel will be smaller than in the larger area (e.g. the drift region). In the case of SiO_2 grown on 6H-SiC and 4H-SiC of lightly doped n-channel devices, the oxides are deposited on the (0001) Si-face of the SiC (Choyke, Matsunami, & Pensl, 2013). A good interface, like H-passivated SiO_2 on Si, can yield mobilities that are approximately 50 % lower than the bulk.

2.13.2 Interface Defects

The poor quality of the interface of as-grown SiO_2/SiC possesses two origins, namely; the presence of carbon and the wide bandgap of the SiC. The energy gap of SiC makes it sensitive to a broader range of defects than Si. At SiO_2/Si interfaces, defects that are electrically active include Si-dangling bonds on the substrate (Rozen, 2008; Bhattacharya, Fornari, & Kamimura, 2011) and oxygen vacancies in the movement area of the oxide (sub-

oxide bonds) (Fleetwood, 2013). The Si-hanging bonds may be passivated by hydrogen (Stockmeier, 2008; Schulz, 2017). Furthermore, a bulk concentration of levels sited beneath the SiO_2 was observed at band edge conduction of around 2.8 eV (Barrero & Duran, 2015; Duran & Barrero, 2015; Y. Wang, Dai, Liu, Li, & Jones, 2016). Once they are located within the passage of the Si band, the channel mobility is not affected at the SiO_2/Si interfaces. In the case of SiC, electron spin resonance (ESR) measurements have not yet identified Si-dangling bonds at the interface (Zheng et al., 2014). Moreover, hydrogen passivation alone may not be effective (Junping, Jingang, & Lei, 2009; Fischer & Dorn, 2013; Subotic, Bodo, Levi, Jones, & Levi, 2015; C. Jung, 2017). Since they cannot be ignored, it implies that at the SiO_2/SiC interfaces, Si-dangling bonds are not considered a dominant defect. On the other hand, sub-oxide bonds could contribute to the concentration of defects that are electrically active.

The bonding and de-bonding splitting depend on the length of the Si-Si bonds. Usually, only bonds longer than 2.35 nm, which is the normal length in a Si crystal, can contribute to levels within the Si band-gap. They are also passivated by hydrogen, effectively. But, due to the relative positions of the band edges in SiC, the short bonds even result in active interface states (Figure 2.12). The theory suggests that these short bonds cannot readily be passivated by hydrogen (Subotic et al., 2015).

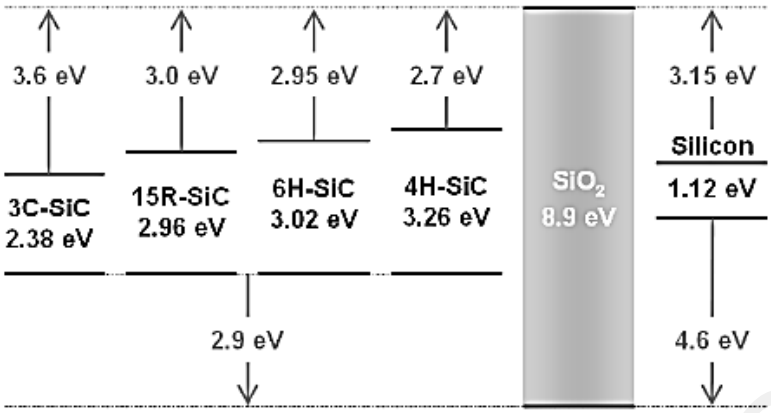


Figure 2.12 Energy gaps of Si, SiO_2, Relative band-offsets and common polytypes of SiC (Subotic et al., 2015).

In a similar manner, the fact that the n-channel mobility in 6H-SiC devices (≤ 100 cm^2 $V^{-1}s^{-1}$) is higher than in 4H-SiC devices (≤ 10 cm^2 $V^{-1}s^{-1}$), can be ascribed to levels situated above the band edge passage of 6H-SiC, and beneath that of 4H-SiC. These levels will trap carriers only at the interface of 4H-SiC/SiO_2. This position is in agreement with measurements of Hall mobility that show a tremendous decrease (approximately 90 %) of the concentration of free electrons at SiO_2/4H-SiC interfaces when compared to that of SiO_2/6H-SiC (approximately 10 %) (Wen et al., 2012). Those values also indicate that the concentration is high around the band edge passage of 4H-SiC. This contributes to the qualitative picture at the distribution levels shown in Figure 2.13. The relative positions of conduction (E_c) and the valence band edges (E_v) are also shown in the figure. 6H-SiC and Si are less sensitive to a larger extent of states interface than 4H-SiC.

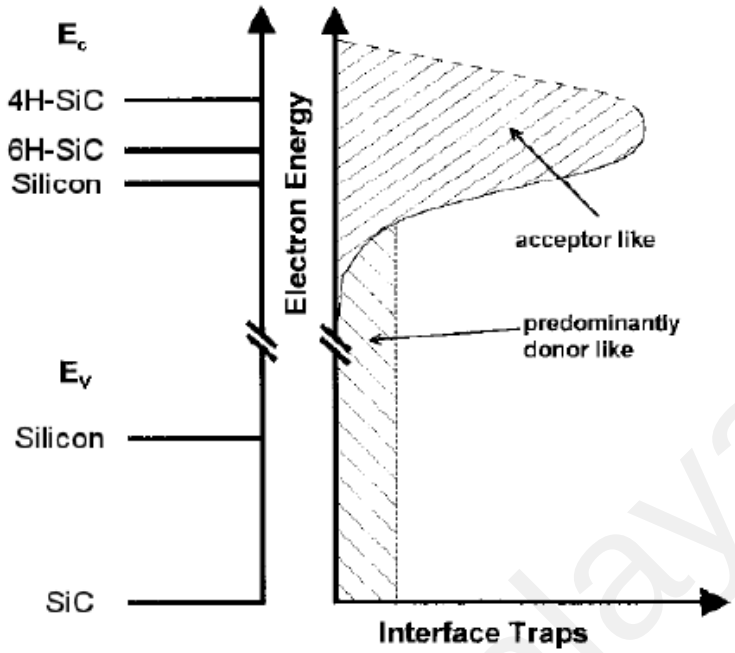


Figure 2.13: Schematic representation of the trap concentration at the interface between the semiconductor and the oxide (Matallana et al., 2019).

The measurements of conductance and capacitance-voltage (CV), which can resolve the power scattering of the traps, indicate that the states interface density (D_{it}) is actually increasing at the larger area of the SiC bandgap and its magnitude is also in order higher than the band edge passage of 6H-SiC and 4H-SiC, which is approximately $\times 10^{12}$ and $\times 10^{13}$ $cm^{-2}eV^{-1}$, respectively for as-deposited oxides (Figure 2.14). Since it was noticed that the n-channel mobility of 4H-SiC improved with temperature (from 200 to 475 K), it can also be concluded that Coulomb scattering, which is the main instrument for regulating the charge movement of the remaining free carriers prompted by the negatively charged centres. On the other hand, the n-channel mobility of the 6H-SiC reduces when temperature increases (from 200 to 500 K), showing a limited photon mobility, less affected by interface traps. It is important to state that the high concentration of states located between the 4H- and 6H-SiC conduction band edges were not allocated to any particular defect (sub-oxide bonds are a

possibility). In any case, they are the same up to the points that were previously identified at the interfaces of Si, located at 2.8 eV below the band edge passage of SiO_2 which is actually 0.1 eV below the band edge passage of 4H-SiC, and eventually within the bandgap of that polytype. Since they have a wide energy distribution and a slow time of response, it was inferred that the points are due to near-interface defects within the oxide (Z.-Q. Zhu & Howe, 2007; S.-Y. Jung, Hong, & Nam, 2013; Kerler, Burda, Baumann, & Lienkamp, 2014; Sridhar, 2017). If they are related to SiO_2, it could indicate the reason for their presence on both SiC and Si.

Due to the high concentration of inter-state density that corresponds to slow border traps-fall within its bandgap, and its higher bulk mobility which produces a lower inversion transportation, the 6H-SiC is less preferred to 4H-SiC for a larger channel resistance at the oxidized interfaces. Another reason for the high defect density at the interfacial layer of SiC /SiO_2 is the complex method of oxidation which involves carbon diffusion. The interface state density at the oxide layer formed on the Si-face of the two polytypes is similar throughout the gap, and increases sharply between their conduction band edges. It turns out that; the oxide appears free of carbon; it is not ideally removed from the interface during oxidation. Indeed, several techniques like Rutherford backscattering (RBS) (Boldea, Tutelea, Parsa, & Dorrell, 2014; Morimoto, Ooi, Inoue, & Sanada, 2014; Q. K. Nguyen, Petrich, & Roth-Stielow, 2014; Trancho et al., 2017), x-ray photoelectron spectroscopy (XPS) (Finken, Hombitzer, & Hameyer, 2010; Inoue, Morimoto, & Sanada, 2013; Ooi, Morimoto, Sanada, & Inoue, 2013; Bojoi, Cavagnino, Tenconi, Tessarolo, & Vaschetto, 2015; B.-H. Nguyen, Do, & Minh, 2015; Trancho, Ibarra, Arias, Salazar, & Peña, 2016), transmission electron microscopy (TEM) and electron energy loss spectroscopy (EELS) (Z. Liang, 2012; Bazzi, 2013; Reimers, Dorn-Gomba, Mak, & Emadi, 2019), surface-enhanced Raman spectroscopy

(Reimann, 2015), and spectroscopic ellipsometry (Uhlemann & Hymon, 2018), all have shown excess carbon present at the interface in a Si*x*C*y*O transition layer which was found to extend about 1 nm into the oxide. Accordingly, some C-related defects are expected to contribute to the D_{it}. Equivalent series resistance (ESR), the preferred tool for the identification of atomic configurations has led to the detection of unsaturated and three-fold coordinated carbon, which might be referred to as C-dangling bonds (Franquelo et al., 2008; Zheng et al., 2014). In addition, XPS suggests the presence of C-C and Si-O-C bonds.

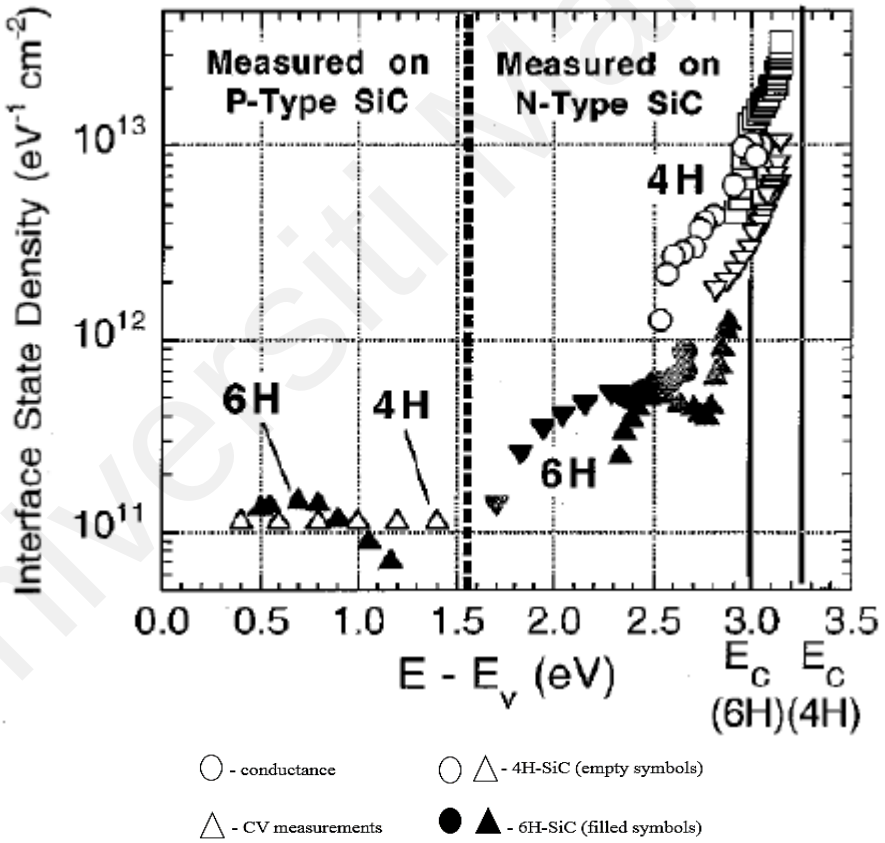


Figure 2.14: Interface state density obtained through CV measurements and conductance as a function of the bandgap energy of 4H- and 6H-SiC within the band-gap (Morimoto, Takeda, Hirasa, & Taniguchi, 1990; Matallana et al., 2019).

If slow near-interface defects are considered to be accountable for the large concentration of shallow states that are near the passage of band edge of 4H-SiC, C-related

defects may explain the trap levels within the rest of the band gap. In particular; such defects would also explain the larger *Dit* observed deep in the gap when the oxide is grown on C-containing faces, such as the a-face (50 % C atoms) and the C-face (100 % C atoms) when compared to the Si-face (0 % C atoms) (Rodríguez, Bernet, Wu, Pontt, & Kouro, 2007). As these lower energies correspond to the ones of graphitic inclusions in diamond, a carbon cluster model was proposed (Y. Wang et al., 2016). Excess carbon atoms could aggregate at the SiO_2/SiC interface, forming graphitic groupings of various geometries. The π orbital of *sp*2-bonded carbon may give levels whose energy depends on the cluster size. Small C-clusters would have energies in the lower part of the gap and large ones would have a graphite-like energy distribution spanning the gap. A third C-related level in the upper part of the gap has been attributed to 3C-SiC inclusions at the SiO_2/4H-SiC surface.

As the combined contributions of small C-aggregates, graphitic regions and 3C-inclusions could explain the shape of the D_{it}, the C-cluster model constitutes an interesting framework for the understanding of the interface. Therefore, carbon clusters have not been seen at SiO_2/SiC interfaces. In any case, results of previous studies show that they may not likely surpass a few atoms, and if such aggregates exist, their respective energy levels would depend largely on their surrounding which was not taken into consideration in the isolated C-cluster model. Theoretical simulations of the detailed SiO_2/SiC interface are therefore considered a useful complementary tool for the consideration of specific defects. The theory offers corresponding trap levels, charge-exchange parameters and their equilibrium atomic configurations. Also, the interface of a SiO_2/SiC layer largely depends on its environment and its relationship to the energy of a given defect, while the theoretical results provide general information on the possible defects and their impact on the states interface density.

In order to make some theoretical predictions, careful consideration is necessary for the computations, because the calculated values must be referred to specific cases for each stable configuration. The report of some studies in the field indicates that the technique relies strongly on the density-functional theory (DFT), which makes it difficult to reproduce the bandgap values of semiconductor devices (Subotic et al., 2015). Therefore, the calculated energy bandgaps of atomic configurations may not have 100 % accuracy. More so, the theoretical data depends on the identification of configuration defects equilibrium at the interface, and to a certain extent on the oxidation kinetics. Some of the predicted defects and their respective energy levels within the 4H-SiC bandgap are presented in Figure 2.15. A comprehensive list of defects was reported in the studies of Marchesoni et al. (1990); Meynard & Foch (1992); Rodriguez et al. (2009); López et al. (2013); Subotic et al. (2015); Matallana et al. (2019).

At the interface, the stability of carbon was observed in different configurations. For instance, a single carbon can be inserted in a Si-O-Si bridge in two ways: by forming Si-C-Si with an oxygen protrusion or by forming Si-O-C-Si with the carbon fairly connected to a Si atom on another ring close by. These defects were observed to be stable in the neutral and negatively charged states respectively. Split carbon interstitials sharing a Si-site on the substrate side could also occur. This can produce a ‘‘C-cluster” of not more than 6 atoms. In fact, simulations of the oxidation process have shown that their size is restricted by C-removal and DFT has also proven that big aggregates are not stable at the interface (Pou, Zaragoza, Rodríguez, Ceballos, & Boroyevich, 2007). In another proposed site for correlated carbons on the side of the substrate, it was predicted that this defect is so stable that it can occur in the oxide and form a C-C bond connecting two adjacent Si-C-O-Si bridges. The stated defects consist of three-fold coordinated C atoms and could describe the ESR signal.

In these stable configurations, the unsaturated carbon produces a platform in the upper part of the 4H-SiC bandgap and the valence band edge. These special defects are unique to the SiO_2/SiC interface, and correlate with the occurrence of excess carbon that was noticed at the interface which could describe the measured inter-state density, D_{it}.

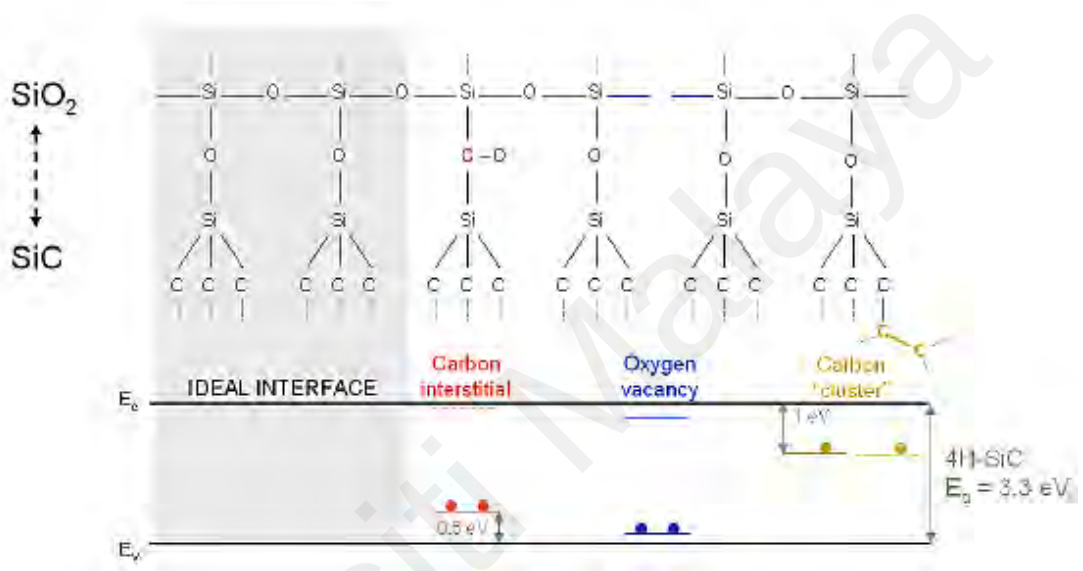


Figure 2. 15: Various defects that occur in SiO_2/SiC interface and their corresponding levels in the 4H-SiC energy bandgap (Rozen, 2008; Subotic et al., 2015).

2.13.3 Defects in SiC Substrates and SiO_2 Interlayer

Although, great improvements have been recorded in the past few years to lessen the concentration of defects in SiC substrates. This has been observed to be the most challenging part of the development of the SiC wafer processing technology, which has continued to hamper the growth of devices that require increased voltage and regions of large current. Defects in SiC is comprised of micropipes, also known as open-core dislocations, conventional dislocations and low-angle grain boundaries. Micropipe defects are observed to

be hindering the commercialization of various types of SiC-based devices, most especially the ones that require larger current (Kimoto, 2015). A typical micropipe defect that exists in SiC material is described in Figure 2.16. It is the large screw dislocation of a hollow part, which succeeds the direction of SiC (c-axis) growth and spreading into the epitaxial layer(s) of the device. This imperfection is prevented in a SiC-based system from obstructing a backward current, making it practically inactive.

The high concentration of micropipes that exist in a wafer can cause some losses during the processing of the device. The low-angle grain boundaries (LAGBs) around the periphery of the crystal will combine with the development of large-diameter structures grown under non-optimized processing conditions. These LAGBs are described as the borders between parts of SiC material that are not aligned. This could either be a rotation of the planes or a relative tilt of the (0001) planes with respect to each other, which normally comprises of screw dislocations and threading edge. These LAGBs can perform as stress concentrators and improve the likeliness of cracking the wafer at the locations of defects during the process of epitaxial development. It is then imperative to lessen the concentration of grain boundaries of low angle crystals. The LAGBs close to the surrounding of the wafer have been mainly removed from the present component of commercial SiC (Calusine, Politi, & Awschalom, 2016). SiC is the only compound element that can be oxidized chemically and thermally to create stable layers of SiO_2. These layers are very important for insulation in various electronics applications.

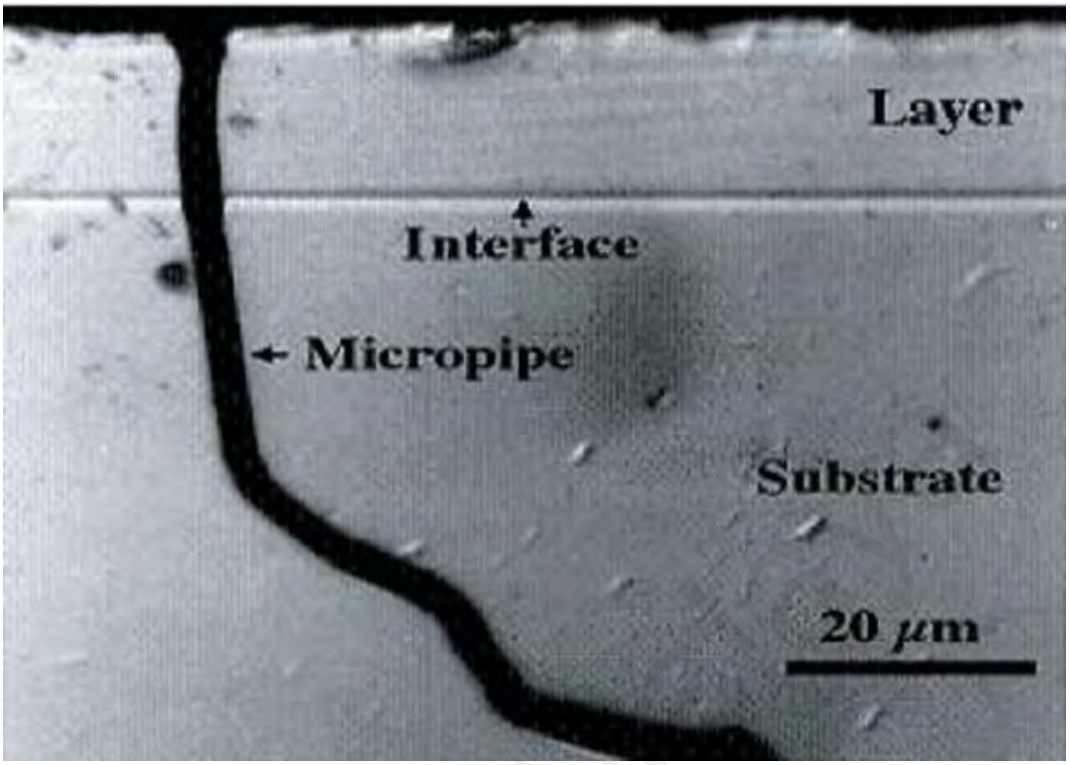


Figure 2.16: Cross-sectional view of a micropipe starting from the wafer and spreading to the epitaxial layer (Yakimova, 2006; Rong, 2015).

However, the major challenge in the fabrication of SiC semiconductors is the high interface trap density of the SiO_2/SiC structure. A high-density trap will influence the performance of the device since it will enclose the carriers from the passage, thereby reducing the conduction current. Although, the factors that differentiate the interface between the SiC and the gate oxides from the highly successful interface of Si/SiO_2 and the classic interface are still not clear. It is strongly believed that they are related to oxygen vacancies in the oxide, carbon dimmers in the SiC, carbon clusters, silicon, and carbon dangling bonds near the interface (Yogesh Sharma, 2012). These traps can be positively or negatively charged based on the potentials of the surface. A typical example of the dangling bonds at the interface between semiconductor (SiC or Si) and SiO_2 after thermal oxidation is illustrated in Figure 2.17.

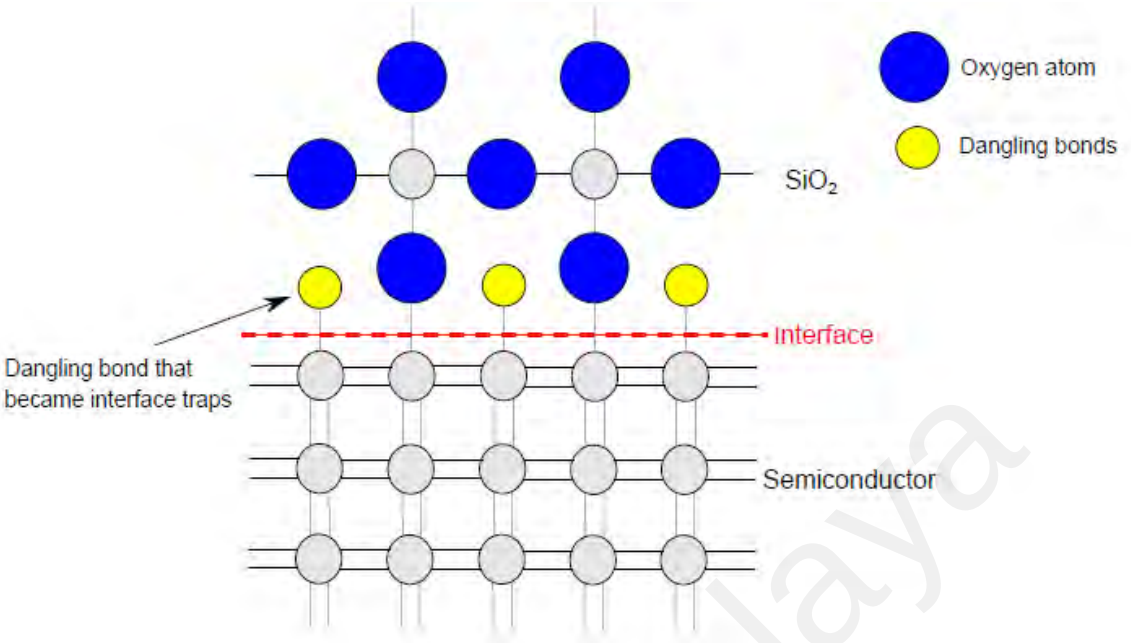


Figure 2.17: Creation of dangling bonds at the interface between SiC and SiO_2 after thermal oxidation (Rong, 2015).

In an effort to maximize the potentials of SiC, the quality of the interface of SiC/SiO_2 can be improved by creating more processes that will efficiently and effectively passivate the defects created during the oxidation process. As mentioned earlier in this section, the standard process of passivation depends on post-oxidation annealing in nitrous oxide (N_2O) or nitric oxide (NO) followed by annealing in hydrogen (NO + H_2) (Yogesh Sharma, 2012). On the other hand, NO is very toxic and for safety concerns, N_2O is now widely used for nitridation of thermally deposited oxide. The channel mobility of a SiC MOSFET from (~1 $cm^2/V.s$) single digit is increased to around 30 $cm^2/V.s$ by these passivation that have enabled the bulk production of SiC MOSFETs.

However, the value of this channel mobility is approximately 4 % of that of commercial SiC, whereas, the mobility of channel inversion can be as high as 50 % of bulk mobility in the case of Si. There are other processes that have been described in previous studies that can

further enhance the mobility of the channel; such as, deposition of oxide in the presence of sodium, which has high value of about 150 cm^2/V.s mobility. But, power electronics are very unsteady because, there is no real-time usage, since there is mobility of sodium under stress (Sveinbjörnsson, Allerstam, Ólafsson, Rödle, & Jos, 2007). Another passivation technique is the passivation of phosphorous which was observed to be more efficient in decreasing the density of interface trap compared to passivation of NO that has about 80 cm^2/V.s peak field effect mobility (YK Sharma et al., 2013). However, the SiO_2 was converted to phosphosilicate glass (PSG) by phosphorous passivation, which results in instability of threshold voltage because of polar material that they are made from. Both the passivation and N_2O have been studied with a view to compare both MOSFET and MOS capacitor that are fabricated from 4H-SiC.

Recently, a phosphorous passivation method that uses a thin layer of PSG, covered with grown oxide was reported by (YK Sharma et al., 2013). This method enhances the stability of the threshold voltage compared to the thick process of PSG passivation that has peak mobility field effect of (about 70 cm^2/V.s). High thermal oxidation temperature, above 1500 ˚C with a low rate of oxygen flow was also observed for a reduction in the concentration of interface trap to about 2×10^{11} cm^2eV^{-1}, and mobility field effect of almost 40 cm^2/V.s (SM Thomas, Sharma, Crouch, Fisher, & Mawby, 2014; S. M. Thomas, Jennings, Sharma, Fisher, & Mawby, 2014). An investigation on high thermal nitridation by annealing of thermally deposited oxides, and direct growth in N_2O on 4H-SiC (0001) semiconductors with p-body implanted area was carried out by (Rong, 2015). Results from the study shows that there is a significant improvement in the mobility field effect channel, approximately (20 cm^2V.s) and density of interface trap (~1.5×10^{11} $cm^{-2}eV^{-1}$) at high thermal nitridation above (1200 ˚C) compared to those at lower thermal values and interface trap density, i.e (4 cm^2/V.s) and (1

$\times 10^{12}$ $cm^{-2}eV^{-1}$), respectively. In terms of reduction of threshold voltage and improving the mobility of the field effect channel, 1300 ˚C was observed to be most effective among the nitridation temperatures (Rong, 2015).

2.13.3.1 Point Defects

Defects in point can be described as interstitials atoms which occupy a site in the crystal structure where there is absence of atom or vacancies that are not occupied in the crystal lattice. An interstitial and surrounding vacancy formed when an atom migrates into an interstitial site and develops a vacancy, is known as a pair of Frenkel (F. Gao & Weber, 2003; Crawford & Slifkin, 2013). When an impurity atom of a lattice site is occupied in a lattice where it is not required, it is referred to as substitutional defect. Figure 2.18 presents the various point defects available.

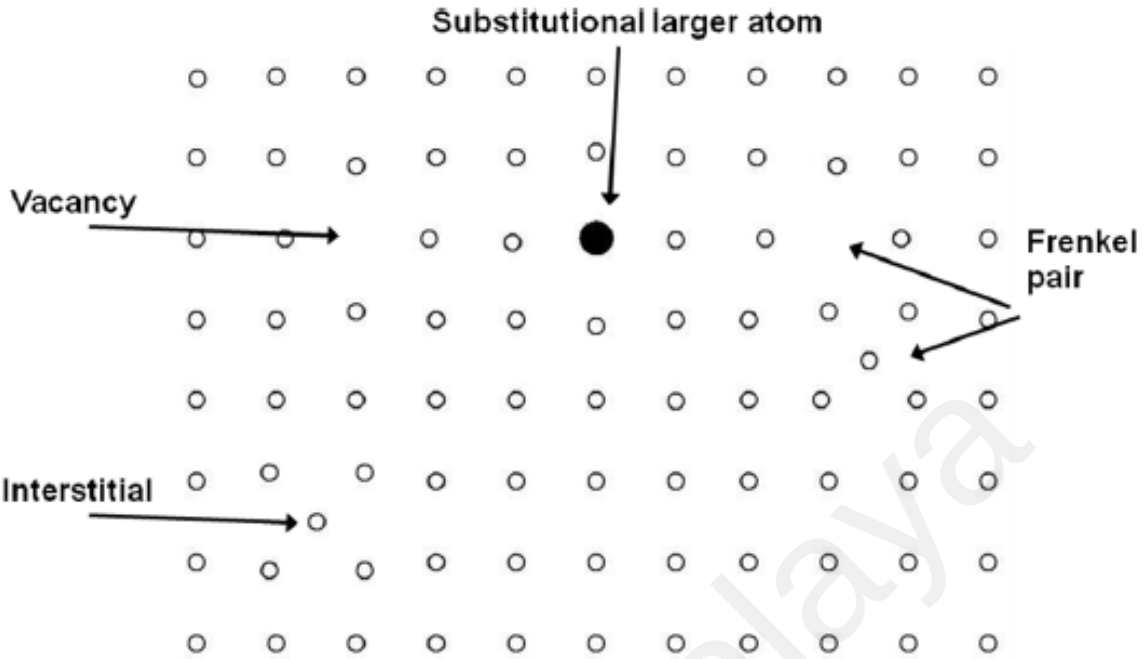


Figure 2.18: Different kinds of point defects in a crystal lattice (F. Gao & Weber, 2003; Eriksson, 2011).

2.13.3.2 Line Defects

Line defects are divided into two primary types; namely, the screw and edge dislocation. They are referred to as void in lattice that are spread in a single line direction, only. The termination of a plane of atoms in the centre of a crystal usually results in edge dislocations. In that case, the edge of the terminating plane is bent around the adjacent planes, so that the structure of the crystal is perfectly arranged on both sides (Figure 2.19 (a)). Owing to crystal stress, a screw dislocation happens when atomic planes slides over one another (Figure 2.19 (b)). The magnitude and direction of the crystal distortion is expressed as Burgers vector. A screw dislocation is parallel to the line direction, and it is perpendicular to the Burgers vector in an edge dislocation. Also, there is a mixed method of dislocations, which has the features of both. If the atoms from the nearby planes disintegrate and re-

assemble with the atoms at the terminal edge then, there is possibility of dislocation to occur (Anderson, Hirth, & Lothe, 2017).

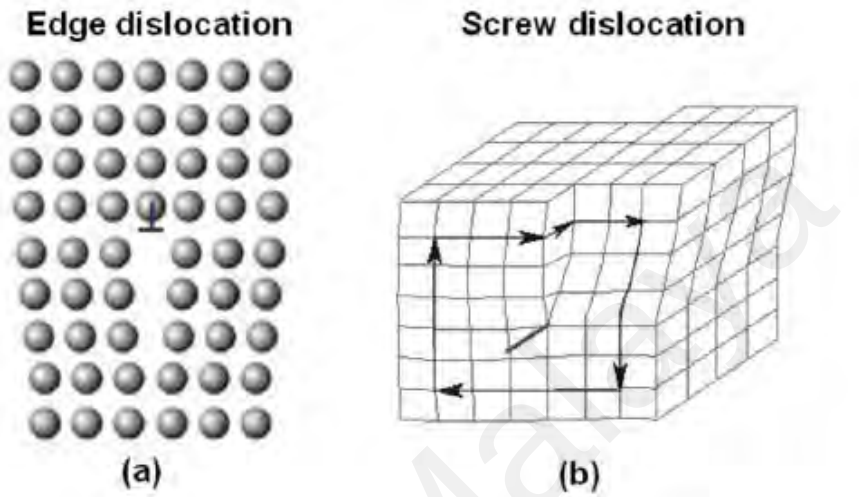


Figure 2.19 (a) Edge dislocation formed by atomic planes that are bent around a terminating crystal plane (b) Screw dislocation formed by planes sliding over each other. The arrows indicate the Burgers vectors (Eriksson, 2011; Anderson et al., 2017).

2.14 Gate Oxides on SiC

The difference in the properties of the bulk of gate oxides deposited on SiC as compared to those grown on Si has not been proven. Although, it has been demonstrated that oxidation process on SiC produces stoichiometric SiO_2 whose breakdown strength, density, refractive index and dielectric constant are very similar to the ones in thermal oxidation of Si (Raynaud, 2001). Since C removal occurs specifically in oxidation period, a major part of the oxide is basically free of carbon, as measured by the most sensitive analytical techniques. However, as the growth kinetics are different, the temperature budget necessary for the growth of a thermal oxide for a given thickness on SiC is around ten times more than in the case of Si. Therefore, CVD oxides can be grown to lessen the processing time, but a thermal SiO_2 layer

is still necessary to ascertain the quality of the interface. As explained earlier, thermal growth can be accelerated by using high oxygen pressures. This permits the oxidation of quality gate oxides in shorter times and/or at lower temperatures.

During the operation of an oxide-based device, charge build-up in SiO_2 can occur from carrier injection. This causes instabilities in threshold voltage to transport degradation and eventually oxide breakdown (device failure). Therefore, it is important to identify the conditions in which charge build-up occurs, and how it can influence the characteristics of a device. An electric field is generated in the gate oxide of a DMOSFET in OFF state, and this can restrict the attainment of the maximum blocking voltages. This is related to the breakdown field of SiO_2, which is approximately 10 MV/cm and the gate leakage currents which may exist through tunneling or emission of carriers from the gate contact. In addition, even if the oxide field is insignificant around the base area, tunneling of most carriers can occur and can be potentially trapped in the dielectric within a short wavelength of the interface.

In the ON state, a bias is utilized on the gate to create an inversion layer in the base area. This can cause minority carrier injection in the presence of high fields from the semiconductor device into the oxide through Fowler-Nordheim tunneling. During tunneling, the distance x_t, a carrier has to pass through in order to leak from the dielectric gate can be determined from φ_{bo}/ξ_{ox}, where φ_{bo} is the appropriate band-offset (in Volts) between the SiO_2 and semiconductor. The probability of tunneling depends exponentially on x_t. and the band-offsets of 4H-SiC relative to SiO_2 are less than those of Si (Rozen et al., 2008). For a given oxide field, this produces a larger current leakage in SiO_2 on 4H-SiC than in Si. This raises particular concerns for n-channel devices as the offset between the conduction bands of SiO_2

and 4H-SiC is only about 2.7 eV, improving the channeling of electron from the semiconductor towards the positively biased gate contact.

The introduction of carriers in the ON and OFF states causes charge trapping in the oxide, to degradation of interface, and to remote Coulomb scattering. The concentration of electron and hole traps is therefore a major factor that determines reliability and stability of a device. It was discovered that the NO annealing required for improvement of interface also suppresses trap-assisted tunneling and prevents negative charge trapping. The blocking voltage can be increased in devices at both the n and p of their channel as the tolerance on electron leakage current is increased. Also, the gate bias can be increased in the ON state of n-channel devices. Therefore, NO annealing can result in reduced energy dissipation and/or increased mean time to failure. However, it was discovered that NO treatments greatly improve hole trapping. This, of course, is a major concern for the p-channel devices in the ON state, but it can also affect the preferred n-channel devices in the OFF state as a hole accumulation layer is formed at the base/dielectric interface where most trapping occur. Therefore, the understanding of the SiO_2/SiC interface is required for further enhancement of the features of oxide-based SiC devices (Rozen, 2008).

2.14.1 Holmium (Ho) Oxide as a Rare Earth Oxide and Alternative Gate Oxide

Some rare earth oxides (REOs) have been studied recently for some properties; such as high chemical and thermal stability, low mismatch of lattice with silicon, surface smoothness, low density of interface trap, high conduction offset, high resistivity (between 10^{12} and 10^{15} Ω cm), high breakdown electric field, large bandgap (between 4 and 6 eV), and high-κ (between 7 and 30) (F.-H. Chen, Hung, Yang, Kuo, & Pan, 2013; John Robertson & Wallace,

2015; J. Gao, He, Sun, Chen, & Liu, 2016; Goh et al., 2016b;). These oxides have been broadly used in power electronics such as, transistors, capacitors, integrated circuits, varicaps and frequency switches (Pan & Yen, 2010; Constantinescu, Ion, Galca, & Dinescu, 2012; Kaya, Yilmaz, Kahraman, & Karacali, 2015). Table 2.4 presents the elements contained in the lanthanide metal group of rare earth.

Table 2.4: Group of rare earth elements (Lanthanide metals)(Goh, 2017)

Lanthanide														
La	Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu

The elements that belong to the group of lanthanide REOs possess higher dielectric constant, than that of SiO_2. High-κ values permit the reduction of EOT for the purpose of downscaling (Schamm, Scarel, & Fanciulli, 2007; Gillen & Robertson, 2013). Owing to direct channeling of electron through thermal oxides, which may result in unwanted leakage current, larger κ values can be replaced by using ultrathin gate oxides (Engström et al., 2007). A large bandgap is also required for the purpose of insulation (Chin, Cheong, & Hassan, 2010; Goh, 2017).

There is great attraction of holmium oxide (Ho_2O_3) for applications in pH sensing films, memory devices, logic and optoelectronics because of its large dielectric constant, κ which is approximately (13), its thermal and chemical stability, and large energy band gap with Si substrates (Pan, Chang, & Chiu, 2010; Pan & Huang, 2011; Kukli, Kemell, Dimri, Puukilainen, & Leskelä, 2014; Castan et al., 2015). Furthermore, Ho_2O_3 possesses largest magnetic period, largest lattice energy among the REO, and easy susceptibility to crystallization before the process of annealing (Pan et al., 2010; Heiba & Mohamed, 2015). According to previous researches, Ho_2O_3 films were grown by reactive RF sputtering (Pan

et al., 2010; Pan & Huang, 2011), ALD method (Castan et al., 2015) and sol-gel method (Heiba & Mohamed, 2015).

In the study of Pan et al., (2010) and Pan & Huang (2011), Ho_2O_3 films were grown with low crystallinity through reactive sputtering before the process of RTA. There is a great improvement in the binding energy and crystallinity after the RTA process. However, a decrease in the degree of crystallinity was observed when the RTA attain a temperature of 900 ºC as a result of amorphous silica layers formed between the interface of Si substrates and Ho_2O_3 films. This pattern was followed, indicating a sudden reduction in binding energy of Ho-O bonds. Interestingly, that of Si-O bonds increased when it was subjected to annealing temperature of 900 ºC. There was also an increase in surface roughness when the temperature of RTA increased, while the RMS value decreased at that temperature. This may be attributed to the migration of Ho and O_2 atoms to the interfacial layers and creating layers of amorphous silica with reduced surface roughness at larger temperatures of RTA (Pan et al., 2010; Pan & Huang, 2011). In the case of Mn-doped Ho_2O_3 films grown by sol-gel process, the sizes of the crystals decrease with the contents of Mn while the contents increased with increasing strain (Heiba & Mohamed, 2015). In the study of Castan et al., (2015), the HoTiOx films were deposited by the process of ALD. The larger the contents of Ho in the HoTiOx films, the lower the value of the capacitance, and a lower concentration of current leakage (Castan et al., 2015; Goh, 2017).

2.14.2 Growth of Gate Oxides on SiC

One of the best properties of Si that has made a landmark contribution to the development of a semiconductor is the growth of SiO_2 gate oxide. In order to form an

interfacial layer in a MOSFET gate structure, the oxide can be developed thermally. Similarly, it can be grown on a SiC which may be used for various applications when it is joined with the bulk properties of very low intrinsic, free carrier concentration, high thermal conductivity and wide bandgap. In other words, the application of gate oxide on both Si and SiC are the same, just that the latter requires higher processing temperatures. Table 2.5 presents the various gate oxides grown on SiC substrates. One of the major challenges being encountered during the development of a good gate oxide on SiC is the inclusion of carbon. The grade of gate oxides on Silicon carbide, and its positive influence on the major properties have been improving gradually, this is evident by the discovery of more ways on the system of growth and reactions with the interface.

Several studies have shown that hardening of gate oxides in nitric oxide improves oxide reliability with a considerable reduction of interface traps, while annealing in N_2O displayed a damaging effect (Pande et al., 2020). In the study of Houston Dycus et al., (2016), direct oxide growth in NO yielded a good result on the quality of the interface and the reliability of the oxide, this is because there is enough time for the removal of excess carbon by the nitrogen.

Table 2.5: Various gate oxides deposited on SiC substrates

No.	Deposition Method	Gate Oxide	Ref.
1	MOD	CeO_2	(W. Lim et al., 2010)
2	PEALD	Al_2O3	(E Schilirò et al., 2017)
3	MOD	ZrO_2	(Kurniawan, Wong, et al., 2011)
4	MOCVD	AlN	(Khosa et al., 2019)
5	ALD	HfO_2	(Taube, Gierałtowska, Gutt, Małachowski, Pasternak, et al., 2011)
6	LPCVD	TEOS	(Moon et al., 2020)

*MOD (Metal-Organic Decomposition Method), ALD (Atomic Layer Deposition), PEALD (Plasma-enhanced ALD), LPCVD (Low pressure Chemical Vapour Deposition), PVD (Physical Vapour Deposition), TEOS (Tetra-ethyl-ortho-silicate).

In conventional thermal growth, numerous methods have offered effective gates on SiC. Improved interfacial properties were observed when layers of oxide-nitride-oxide formed from jet vapour deposition (JVD) were stacked on an ultra-thin nitride. Within the interfacial area, the presence of nitrogen was observed with the potentials for strong adhesion between it and carbon (X. W. Wang, Bu, Laube, Caragianis-Broadbridge, & Ma, 2002; Dimitrijev, Han, Moghadam, & Aminbeidokhti, 2015). The densities of the interface around the transmission passage were decreased to a value less than 10^{12} $cm^{-2}eV^{-1}$. In the study of Sometani et al., (2016), dry oxides were opened to strong nitrogen that is created from remote plasma, and the MOSFETs produced exhibit great improvement in the mobility channel. In order to surmount the challenges of inadequate development of nitrided gate oxide, charge trapping with regulated high and low de-trapping time is used in the inner depth and the near-interface area of the SiO_2, respectively. A device with small field mobility electron (48 cm^2/Vs), breakdown field strength of 9 MV/cm and a low density of interface was eventually produced (Abe, Yamagishi, & Cho, 2018; Chanana, 2019; Nicholls, Vidarsson, Haasmann, Sveinbjörnsson, & Dimitrijev, 2020; Tsui, Huang, Wu, & Chien, 2021). Several studies have been conducted on the replacement of SiO_2 as a gate oxide, nitride or oxynitride. These studies include Sm_2O_3 (Goh et al., 2016b), Nd_2O_3 (Hetherin et al., 2017a), ZrO_2 (Lei et al., 2017), Al_2O_3 (P. Chang & Hwu, 2018), Ta_2O_5 (Cheng, Sang, Liao, Liu, Imura, et al., 2012), Y_2O_3 (Quah & Cheong, 2013). A graph of dielectric constant versus band gap is shown in Figure 2.20. Each of them has its limitations when compared with SiO_2 layers.

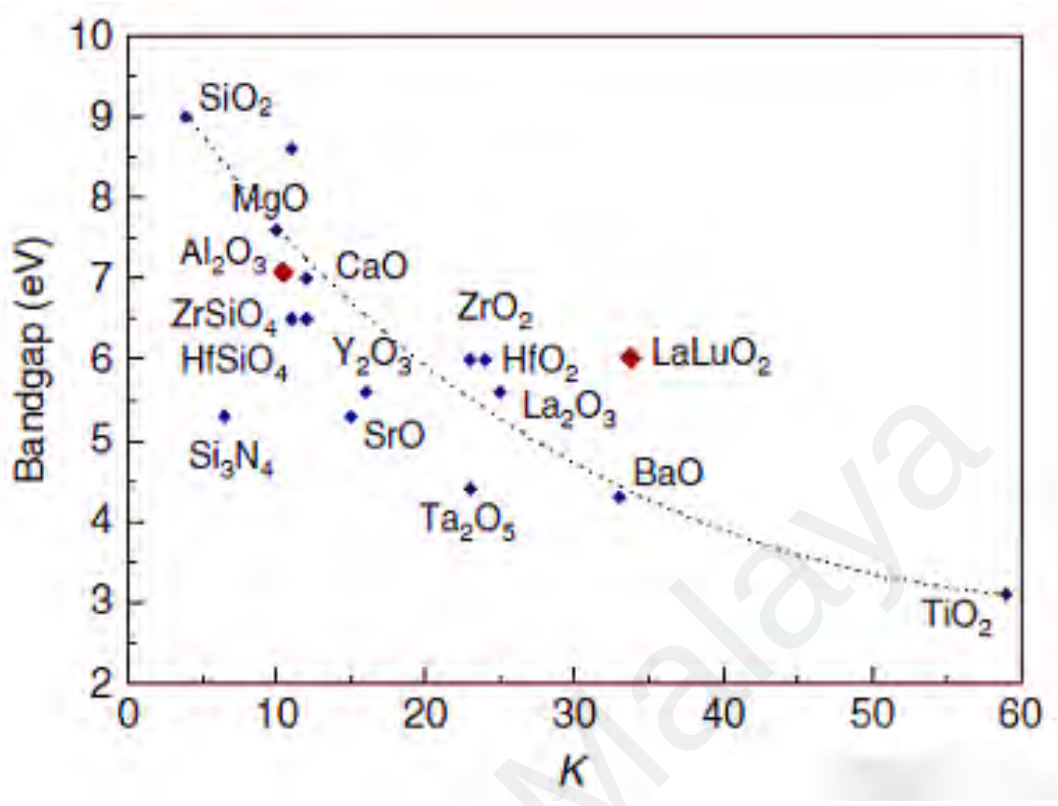


Figure 2.20: Dielectric constant against band gap for various gate oxides (Clark, 2014).

In some previous studies, it was reported that Al_2O_3 has large bandgap and band offset (~ 9 eV & ~ 2.16 eV), high thermal stability, and high κ value (~ 10) (Taube et al., 2016; Q. Wang, Cheng, Zheng, Shen, & Yu, 2018; Zhai, Lv, Zhao, & Lu, 2021). However, some drawbacks have been identified in Al_2O_3 layers. These include large fixed charge, large flat band voltage shift, and large interface trap density. Moreover, the layers of SiO_2 possess a lower interface density than Al_2O_3 (Wallace, 2017). During deposition, or in a post deposition annealing (PDA) environment, unwanted layers of interface are developed easily between the silicon substrates and the Al_2O_3 layers. Reports from previous studies show that ZrO_2 and HfO_2 layers are more appropriate as alternatives for SiO_2 not only because they have beneficial properties, but they also satisfy the six requirements of selecting new oxide (F.-H. Chen et al., 2013; John Robertson & Wallace, 2015; J. Gao et al., 2016; Goh et al., 2016b).

2.14.3 Requirements for the Selection of Various Gates Oxides

The gate terminal of a MOSFET which separates the primary source from the drain is the dielectric layer, called gate oxide. It also links the source and the drain terminals to the conducting passage as soon as the transistor is powered. The formation of gate oxide was done by growing a thin film of silicon dioxide through thermal oxidation, usually an insulating layer in the range (5 - 200 nm). The transistor was later formed by subsequently depositing a conductive dielectric material on the gate oxide. In order to have a strong control over the conductive channel, the gate oxide was made to perform the role of the dielectric layer such that it can withstand a high cross-electric field, which is between 1 to 5 MV/cm (Sah, 1991; Wallace, 2017; T. Li, Tu, Sun, Fu, & Wu, 2020). Large leakage currents and equivalent oxide thickness (EOT) could be observed when high-κ dielectrics are used with metal gate electrodes. This relationship indicates that high-κ dielectrics are of critical importance if technological demands are to be met in the nearest future. A graph of the leakage current versus EOT for different gate oxides is shown in Figure 2.21.

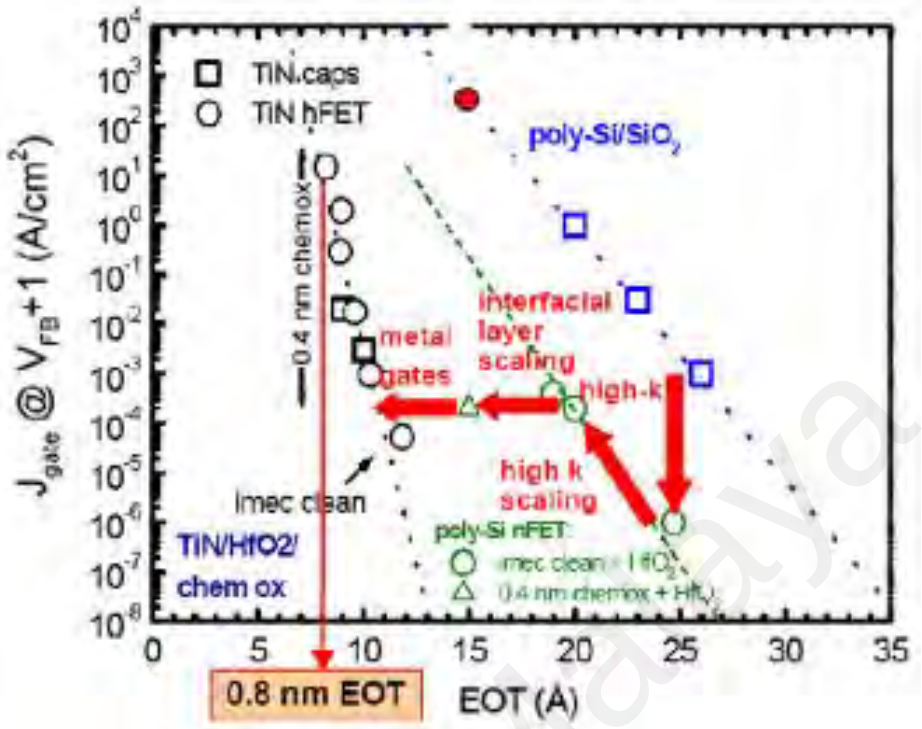


Figure 2.21: Leakage current versus EOT for different gate oxides (He, Zhu, Sun, Wan, & Zhang, 2011).

The gate oxides include a second upper metal silicide placed above the doped first metal silicide. Between the first and second metal silicide, a silicon material may be inserted, or the doped first metal silicide may be overlaid by the second metal silicide thereby developing a silicide bilayer above the gate dielectric. The first metal silicide may be fairly thin, in order to allow moderately dispersed current within it for setting the function of the gate. The inserted silicon and/or the inclusion of the upper silicide may reduce the resistance of the gate contact sheet (Visokay & Colombo, 2009). Normally, a good gate oxide is required to be able to sustain higher processing temperatures, up to 1000 °C without melting. It is also, not permitted for the constituent parts of the gate electrode to penetrate through it or diffuse with either the metal-gate electrode or the Si passage. These are the required characteristics that the gate oxide must possess in order to have low coefficients of atomic diffusion.

Interestingly, the ZrO_2 and HfO_2 that are used in solid oxide fuel cells also belong to the class of fast oxygen ion conductors such as CeO_2. Therefore, diffusion must be reduced for the effective use of a gate oxide (T. Li et al., 2020).

There are several parameters and factors that should be considered before selecting a gate oxide. They include; interface properties, deposition methods, band offsets, thermal stability, and electronic structure designs. In addition to these basic requirements, there are six selection criteria that are required of a gate oxide. They are as follows; It must: (1) function as an insulator with band offsets above 1.0 eV (2) be kinetically stable (3) be thermodynamically stable (4) develop a good electrical interface with Si (5) contain a low density of defects, and (6) have high enough κ (> 12) (T. Li et al., 2020). For a long-term technological involvement in downscaling, the high-κ is expected to be over 10, preferably in a range between 20 and 30. However; due to low bandgap, a very high-κ is not appropriate for the design of CMOS. This may lead to movement of excessive tough fields between the drain and the source. Except for Nd_2O_3, Sm_2O_3 and La_2O_3, the κ value is inversely proportional to the bandgap. More so, the thermal reliability of the oxide must be strong enough to prevent interaction with the Si substrates and creation of SiO_2 (Narayanan, Frank, & Demkov, 2016).

For a gate oxide to be kinetically stable, there must be a strong compatibility between the prevailing process conditions and the oxide. For instance, an oxide must remain in the amorphous state, even after annealing. The κ values may be affected, and the electronic properties degraded due to the changes in grain sizes and crystallographic orientations. The oxide must also play the role of insulator with band offsets above 1 eV. Holes on the oxide band and permission of electric passage due to the release of Schottky electrons should be

avoided. It is required that the best quality in interfacial layer, defects and roughness is achieved, since there is direct contact between the substrates and the oxide.

The production of high-quality interfaces is done in two ways; the use of an amorphous oxide or the development of the crystalline oxide epitaxially. The amorphous oxides are mostly preferred for various reasons. Firstly, amorphous oxides are less expensive than crystalline. Also, the concentration of their interface defects is lower due to their ability to interface bonding configuration. Without forming new phases, the composition of amorphous oxides can be varied gradually. Their carriers will not be scattered during variations due to the collision of various oriented oxide grains, and their isotropic nature. Lastly, they do not possess grain boundaries that perform as passages of stress-free diffusion. Electronic conditions in oxide bandgap that contribute to electrically active imperfections are affected by atomic configurations. These defects may lead to four main problems: (1) instability due to electrical breakdown and failure, (2) reduction of carrier mobility owing to dispersal by trapped charges, (3) unsteady operating features owing to a varying threshold voltage that changes with time, and (4) fluctuation of gate threshold voltage caused by the charge trapped (T. Li et al., 2020).

2.15 Surface Modification and Pre-Treatment of SiC Substrate/ Gate Oxide Interface

2.15.1 Surface Treatment for Enhancement of Electrical Performance of Gate Oxide/SiC Interface

The influence of surface modification as a suitable strategy for tackling some of the various issues limiting the performance of gate oxides on SiC-based MOSFETs cannot be over-emphasized. Despite the significant progress recorded on SiC devices, some pertinent

issues relating to interfaces are still being debated in order to further enhance the performance of semiconductor technology. Several studies have been carried out in this regard. Therefore, the role of pre-oxidation, during and post-oxidation processes on the performance of these devices are discussed in the next sub-section.

2.15.1.1 Pre-Oxidation as a Form of Surface Modification

In a recent study by Idris & Horsfall (2020), an investigation of the effects of surface treatment on SiC substrate was conducted using forming gas annealing and rapid oxidation processes. In the study, the treatment was carried out prior to the deposition of Al_2O_3 gate oxide on the substrate. They carried out the nanoscale electrical characterization of the structure, with much emphasis on the interface under different processing conditions. In their results, significant improvement in the field effect mobility and low interface state density was observed. In another study by Constant et al., (2011), hydrogenation was employed as a means of surface treatment and pre-oxidation on 4H-SiC MOSFET. The hydrogen was applied in form of annealing prior to oxidation by a rapid thermal process. In the study, a great improvement in the electrical stability and mobility channel was recorded. Another technique that was used for surface treatment on SiC substrate is nitridation. In a study by Dhar et al., (2010), nitrogen implantation was employed as a pre-oxidation process for improving the surface of the wafer before the growth of gate oxide. The result of the study showed that an improved field effect and mobility channel with a considerable decrease in threshold voltage was recorded due to the nitridation. Other similar and more recent studies include Wutikuer (2018), Fei et al., (2020) and Shin et al., (2021).

2.15.1.2 Oxidation Techniques for Mitigation of SiC/SiO_2 Interface Challenges

There are several methods that can be utilized as oxidation processes to surmount the structural limitations that are presently encountered by the SiC/SiO_2 system. Presently, the oxidation of SiC involves the release of C atoms, and therefore, a Si atom must also be released occasionally due to the density of Si in SiC, and its size when compared to that of SiO_2 (H. Liu, 2018; Fu, 2020). Multiple interfaces are caused by several factors; for example, since the received oxygen atoms and the released C and Si atoms do not penetrate the SiC side, it is better to "oxidize" sub-oxide bonds first. However, two major challenges are envisaged, i.e some of the released C atoms are likely to be trapped in the region of interface, and secondly, the SiC arrangement may be disrupted by the release of Si and C atoms. It was therefore suggested, that the presence of a kind of interlayer at the interface may be ideal (Arith, 2018; Matocha, Ji, Zhang, & Chowdhury, 2019; J. Wang & Jiang, 2019).

2.15.1.3 The Effects of Oxidation Technique on the Performance of Gate Oxides

One of the most significant processes in the deposition of gate oxides on MOSFETs is the selection of a suitable process of oxidation. The process is as important as the application of the appropriate deposition technique. The process of deposition and growing of native oxides differ in processes. In a study by Zhai et al., (2021), combined low partial pressure of oxygen and high thermal oxidation was applied in the process. The result of the study showed a considerable improvement in the performance of the SiC MOSFET when the process was compared with the conventional method of oxidation.

2.15.1.4 The Effects of Post-Oxidation Processes on SiC Gate Oxides

There are many improvements that are ongoing to enhance the performance of SiC MOSFETs. Most of these processes are required to enhance the quality of the interface between the gate oxides and the SiC substrates (Roccaforte, Fiorenza, & Giannazzo, 2013). Some of these improvements include post oxidation annealing, which has been employed to mitigate the challenges of channel mobility. In the study of Chung, Tin, & Williams (2000) as reported by Roccaforte et al., (2013), post oxidation annealing was used as treatment and the mobility value recorded was in the range of 25 – 50 $cm^2V^{-1}s^{-1}$. In some other studies, nitrogen was introduced during the process to enhance the electrical performance of the device (Kosugi, Umeda, & Sakuma, 2011; Umeda, Esaki, Kosugi, Fukuda, & Ohshima, 2011). Generally, when nitrogen is introduced into post oxidation process, the nitridation annealing allows the nitrogen to diffuse through the SiC interface from the gate oxide where it passivates the interface states (Fiorenza, Giannazzo, & Roccaforte, 2019).

2.16 Common Deposition Methods of Gate Oxide Films

The formation of thin film and deposition methods are of prime importance for the nature of gate oxide films since the final properties are affected by uniformity and homogeneity. Various methods have been developed in the past, and these methods can be categorized majorly into two, namely; CVD and PVD, i.e. chemical and physical vapour deposition, respectively. The previous, which involves synthesizing thin films from the gaseous phase by chemical reaction, consists of other methods such as atomic layer deposition metal organic-CVD. The latter requires that the thin film is physically deposited on the substrate. It is comprised of other methods such as pulsed laser deposition (PLD),

vacuum evaporation, direct current, sputtering (radio frequency (RF), electron beam evaporation, and thermal evaporation (Chin et al., 2010; Wong & Cheong, 2010; He et al., 2011).

2.16.1 Chemical Vapour Deposition (CVD)

This method is comprised of many processes in which a target, usually in solid form is deposited with or without heat on the surface of a substrate by vapour through a chemical reaction. The material formed as a result of this process is in form of a single crystal, powder or thin film. A wide range of chemical and physical properties can be grown by changing some parameters, including the pressure of gas flows, composition of the reaction gas mixture, temperature and component of the substrate. Enhancing the formation of coatings with uniform properties, low porosity thickness even on substrates of intricate shapes and excellent throwing power are some of the outstanding features of the CVD process. Another unique characteristic of the technique is the ability to perform localized or selective deposition on patterned substrates (Van Zeghbroeck, Robinson, & Brow, 2018).

One of the processes involved in CVD is MOCVD, otherwise known as metal organic chemical vapour deposition. It is the main instrument used for the production of LED. MOCVD is used in other applications, such as RF and optoelectronics. In MOCVD, pure gases are injected into a reactor. A thin layer of atoms is deposited by the tool to the wafer, thereby creating an epitaxial growth or crystalline of materials. Basically, MOCVD is comprised of challenging processes, and one of them is the growing of layers with good uniformity. It employs the basic techniques of both ALD and CVD methods. ALD is also known as atomic layer epitaxy (ALE) or atomic layer chemical vapour deposition (ALCVD)

(J. Yin et al., 2021). MOCVD involves the compositional gas stages and two precursors to be grown and oxidized sequentially in an alternating manner on the substrates. The first precursor is applied excessively and a single layer of reactant is chemically absorbed through the surface. Then, the precursor is evacuated using an inert gas before the second one is applied. There is a chemical reaction between the reactant and the second precursor on the surface which generates the kind of film desired. Finally, the evacuation of the second precursor is performed using inert gas which marks the end of the process (H. Gao, 2019). Although, the precursor does not require etching of the prevailing oxides. It must be stable with high purity, no volatile, no disintegration, no gas phase reaction, and must be non-toxic.

Good quality film, low contamination and better electrical properties can be produced by thermal and plasma enhanced ALD (E Schilirò et al., 2017). The film thickness can be controlled specifically with good uniformity by both the ALD and CVD. Due to the growth mechanism constraints of the precursors, there is uniform coverage over intricate shapes (H. Gao, 2019; J. Yin et al., 2021). The effect of CVD on the properties of deposited films on a SiC substrate was studied by Guo et al., (2020). They observed the epitaxial growth of graphene/epitaxial-3C–SiC on Si. The crystal quality of the film was influenced by the temperature of deposition and addition of 3C–SiC composite film to the precursor ratio. Also, Schlech et al., (2021) investigated the influence of temperature on the CVD of SiC coatings. The result of the study shows that the lower deposition temperatures of the coatings improve the elastic modulus of the substrate, but have no significant impact on the fracture toughness.

Owing to the advantages possessed by the CVD process such as; high film density, good composition control, uniform film, large area depositions and high deposition rates, they are more widely used. However, the technique still suffers some setbacks such as volatility,

stability of precursor, and availability of molecular precursor. Post deposition annealing (PDA) and/or high-temperature growth are needed to disintegrate precursors of organic metal. Therefore, there is a possibility of heavy presence of carbon which may be damaging to the power features of the films (S. Lee, 2018).

2.16.2 Physical Vapour Deposition (PVD)

This method utilizes a range of space development processes that are available for the deposition of gate oxides and their layers. It is based on a technique whereby the target migrates to a vapour state from a condensed form and then returns to a thin film condensed state. It is comprised of various methods of deposition such as; Electron beam evaporation, Thermal evaporation, Pulse Laser Deposition (PLD), and cathodic arc deposition. In the study of Kouakou et al., (2017), silicon carbon nitride thin films were grown by PVD magnetron reactive sputtering. The impact of the deposition method on the mechanical and morphological properties of the grown films was studied. The results showed that the adhesion and the chemical bonding of the film were improved when the substrate is biased.

2.16.2.1 Pulse Laser Deposition (PLD)

This is a PVD technique whereby a strong pulsed laser beam is meant to strike a material that needs to be placed inside an empty space. It involves a laser beam eroding the surface material and then vapourize the target source which later sublimates on the material's surface (Milenov et al., 2019). It is a simple and clean process of obtaining various properties, structures, and compositions (Low et al., 2021). Iqbal et al., (2018) used the pulsed DC magnetron sputtering to deposit AIN thin film on 3C-SiC/Si substrate. In their study, the

effect of the process parameters on the structural, morphological properties and the rate of deposition on the film was investigated. The results showed that the quality of the film was improved by increasing the temperature of the substrate.

2.16.2.2 Electron Beam Evaporation (EBE)

In an effort to heat the target and generate vapourized elements that will sublimate and later condense on the substrates under high pressure, an EBE technique was used (Sarangan, 2016). This process can produce ultra-thin and fine films with good conductive features (Z. Yang & Hao, 2016). It can also produce dense and low stress compact films. Therefore, it is not appropriate to be used as a conventional method of production. Several works have been reported on electron beam evaporation; ZrO_2/SiO_2 thin film was deposited on silica by dependence on structure (Jena, Tokas, Thakur, & Sahoo, 2016; Mahajan, Khairnar, & Thibeault, 2016; Bhanu, Babu, & Thangadurai, 2019).

2.16.2.3 Thermal Evaporation

This is a broadly used method of depositing thin films. In this process, an evaporant is pre-loaded into a container in a vacuum ambient. Then, an extremely high temperature is applied to the substrate, usually (above its melting temperature), and later sublimes and condenses on the substrate's surface. There are several reports on SiO_2 thin film deposition on Si substrates. According to Kalkan et al., (2019), a thin SiO_2 film encapsulated with SiC substrates was deposited with monolayer graphene to be shielded from being absorbed by the atmosphere. The covering of the graphene materials was done by employing two separate

methods of growing thin films; namely, thermal evaporation and pulsed electron deposition**.** Also, cadmium telluride (CdTe) film was grown on silicon substrates covered with silicon carbide (SiC) buffer layers. The CdTe film deposition was done by thermal evaporation and condensation in a vacuum (Koryakin, Kukushkin, & Redkov, 2017). The mechanical stresses recorded in the study were as a result of lattice mismatch and change in coefficients of thermal expansion of CdTe film and substrate.

2.16.2.4 Cathodic Arc Deposition

This method is also known as arc-PVD, and uses an electric arc to vapourize from a cathode target. A very high current density (~ 10^{12} A m^{-2}) will be generated to ionize and evaporate the target material in a quick manner. However, the method generates macro-particles or droplets along with the growth technique that will result in the damage of the film properties. A newly created PVD technique also known as high power impulse magnetron sputtering (HiPIMS) possesses the capacity of producing sputtered materials and largely ionized flux of both gases by sending small pulses of high voltage to the target. A high density of the plasma in the range of (10^{17} - 10^{19}) m^{-3}, which is three times higher in magnitude than the conventional dc magnetron sputter (dcMS) can be achieved by the HiPIMS technique through the large fluxes of energetic ions.

A thin film which is more plane and heavier with enhanced adhesion to the substrate can be obtained through this technique, thereby ensuring enhanced electrical, mechanical, and optical properties (C.-L. Chang et al., 2018). Meanwhile, materials that possess higher melting points are easily sputtered, but require a resistance evaporator for the evaporation process. One of the greatest benefits of sputtering by deposition is that there is better adhesion

between the substrates and the evaporated films. Cathodic arc deposition is therefore considered one of the best methods of creating a good film with better adhesion through different pressure of growth. It also, has the advantages of fast, cheap production, large area, and uniformity compared to sputtering deposition (H.-C. Chen, Jan, Lin, & Wang, 2019).

2.16.2.5 Atomic Layer Deposition (ALD)

ALD is a method of thin film deposition that also require a chemical process. It is similar in chemistry to other CVD methods. It is a film growing process that involves changes of state in gaseous chemicals. However, it possesses its unique characteristics, i.e. the deposition is performed through step-by-step reactions on the surface. This is achieved by interchanging the faces of the layers of two or more complementary precursors (X. Liang et al., 2013; Meng, 2017) into the reaction chamber. Therefore, ALD presents different complementary precursors (e.g. $ZrCl_4$ and H_2O) interchangeably into the reactor. Then, one of the precursors will be absorbed onto the surface of the substrate until it is saturated. Hence, no further deposition will occur until the appearance of the second precursor. Generally, the method provides a specific regulation of the film uniformity and thickness (C. Zhu, Han, Geng, Ye, & Meng, 2017).

Owing to its nature and technique of growth, ALD is regarded as the most advantageous method to grow various kinds of very fine films. It depends largely on self-limiting reactions between the substrate and the gaseous target, which by continuous process ensures a sequential layering means of deposition (Oviroh, Akbarzadeh, Pan, Coetzee, & Jen, 2019). This process of growth ensures an evenly deposited coating on a wide surface, and a controlled thickness for relatively low temperatures of growth (100 – 400 ˚C). The ALD

method is much appreciated and has been used in several innovative areas. The continuous demand for very fine films of "high constant dielectrics", and the progressive scaling down of microelectronic components, have been attributed to most of the successes it has recorded. A thin film such as Al_2O_3, HfO_2 has been grown as a gate dielectric layer in ultra-modern semiconductor devices, known as CMOS. Apart from micro-machines and electronics, the increasing demand for ALD cannot be over-emphasized due to several technological applications. These include 2D material growth (S. M. Lee et al., 2019), biotechnological systems (Graniel, Weber, Balme, Miele, & Bechelany, 2018), and photovoltaic structures (Qiu et al., 2020), and water purification equipment (Weber et al., 2018).

Previously, ALD has been studied extensively as a method of growing very fine dielectric films (Emanuela Schilirò, Lo Nigro, Roccaforte, & Giannazzo, 2019). Hoskins et al., (2018) demonstrated that the deposition of films by ALD in an environment with extreme temperature (1000 °C) can successfully decrease the oxidation of SiC by over 60 %. In another study by Cho & Lu (2020), the kinetics of oxidation of SiC in argon, air and steam ambient was investigated. They showed that the thickness of the passivation oxide layer is largely dependent on the deposition time. Another study performed in a wet environment indicated that the oxidation rate is increased by the presence of water vapour according to its quantity (Vyazovkin et al., 2011; Hoskins, Gossett, Musgrave, & Weimer, 2019).

2.16.2.6 Sputtering

Sputtering is a process of deposition in which microscopic particles are extracted from the surface of a material and bombarded by high pressure gas on the substrate in an empty space (Götsch et al., 2019). It is another physical means of depositing ZrO_2 thin films. It is

also a deposition technique where energetic ions are extracted from the surface of a substrate through a target (Stuart, Gimeno-Fabra, Segal, Ahmed, & Grant, 2015). The most widely used methods of sputtering are DC and RF. DC sputtering is used where the coating of a target is bombarded with atomized gases while the latter, also known as radio frequency sputtering is used for low conductive electrical materials. It can also be used where deposition by DC is not possible (Wong & Cheong, 2010; Baby & Mohan, 2019). A magnet is used to improve the application of ionized gas particles and the distance between the paths of electrons in RF magnetron sputtering, thus the ionization efficiency is increased (Chin et al., 2010; Vasin, Neshpor, Mosina, Vedel, & Grigoriev, 2018).

Generally, sputtering has a low temperature rise, high deposition rate on the substrates, good film bonding, and broad availability (Baptista, Silva, Porteiro, Míguez, & Pinto, 2018). Although, sputtering of gate oxide on target by the direct method is easier, the Si substrate can be oxidized and develop a thick oxide film SiO_2 or a layer of metal silicate during film growth (W. F. Lim & Quah, 2020). Moreover, It is performed directly on the target, so it does not apply to complex shapes (Seshan & Schepis, 2018). Table 2.6 presents some properties of gate oxides grown through different deposition techniques.

Table 2.6: Properties of oxide deposited by various methods.

S/N	Deposition method	Properties of Oxide	Ref.
1	Hot filament CVD	High quality 4H-SiC epilayers	(Van Zeghbroeck et al., 2018)
2	MOCVD	Reduction in the mismatch of lattice structure between the SiC substrate and aluminum nitride (AlN) epitaxial layer, and improvement in crystallinity of the oxide layer.	(J. Yin et al., 2021)
3	Pulsed DC magnetron sputtering.	The crystal quality of the AlN films is improved by elevating the temperature of the substrate.	(Iqbal et al., 2018)
4	ALD	High quality Al_2O_3 films were grown by the inclusion of SiO_2 as an interlayer.	(E Schilirò et al., 2017)
5	Electron Beam Evaporation	Uniform, smooth, and crack-free thin films were obtained.	(Bhanu et al., 2019)
6	Thermal evaporation & Pulse electron deposition	Structural defects, such as cracks were readily grown on TE films due to the lack of surface wettability.	(Kalkan et al., 2019)
7	High power impulse magnetron sputtering (HiPIMS)	More plane and heavier thin film with enhanced adhesion to the substrate.	(C.-L. Chang et al., 2018)

2.17 Architecture of Gate Oxides on SiC

The main technology currently used in advanced transistor nodes is the fin device architecture, and it has been in existence since the early 2010s. In a recent study by Thomas

Stuart (2020), the architectural structure of a dielectric gate in a nano-ribbon transistor was investigated, with much emphasis on the electrical performance of the device. The study was performed with single and stacked layers of ribbon channels that are surrounded by gates with a view to examine the difference in their performance. The result of the study shows that the stacking device architecture displayed better current density and enhanced electrostatic regulation of the channel with an allowance for further downscaling. In furtherance of this research, Huang et al., (2015) worked on the multiple stacking gate concept, by stacking layers of Si nano-ribbon semiconductors vertically to form a three-dimensional (3D) stacked nano-ribbon MOS device.

In another study by Bencherif et al., (2020), the reliability of interfaces of different gate oxides/4H-SiC was investigated under carrier-trapping and high thermal conditions. Different gate oxides, namely; HfO_2, Y_2O_3, Al_2O_3, AlN, Si_3N_4 and SiO_2 were examined one after the other. The result of the study shows that the device performance was enhanced when a thin interfacial layer of about 2 nm thickness was inserted in the MOS structure. It was also shown that when Al_2O_3 and SiO_2 gates were stacked alternately on the SiC substrate, there is an improvement in the device structure in terms of reduced leakage current and effectiveness in the gate voltage on-state immunity behaviour. Table 2.7 presents the summary of some high-κ dielectrics, their deposition techniques and process conditions.

Table 2.7: The summary of some High-κ gate oxides and their processing parameters.

Gate oxide	Process condition	Temperature (°C)	Material band gap (eV)	Relative permittivity	Ref.
Al_2O_3	O_2	1150	8.8	9.3	(Bencherif et al., 2020; L. Huang et al., 2021).
SiO_2	OP-ROA	1180	9	3.9	(Bencherif et al., 2020; Z. Yin et al., 2020)
HfO_2	Dry O_2	1150	5.9	22	(Bencherif et al., 2020; Taube, Gierałtowska, Gutt, Małachowski, & Pasternak, 2011)
Y_2O_3	Ar	1000	5.6	15	(Kang, Jung, Seong, Lee, & Ahn, 2017; Zhao, Amnuayphol, Cheong, Wong, & Jiang, 2019)
AIN	N_2	1700	6.2	8.5	(Nawaz, 2015; Uesugi, Hayashi, Shojiki, & Xiao, 2019)
SI_3N_4	$N_{2\backslash}$	430	5.3	7.5	(Bencherif et al., 2020; Gullu & Yildiz, 2020)

2.17.1 Limitations of Low Channel Mobility in SiC Devices and Methods of Improvement

SiC MOS devices are still faced with tough challenges due to limitations in channel mobility and high trap density at the interface between SiO_2 native gate oxide and the SiC substrates (Cabello et al., 2018). Several studies have been reported on some of these limitations (Peters, Basler, Zippelius, & Siemieniec, 2017; J. Wang & Jiang, 2019; Bader et al., 2020; Ramamurthy, Islam, Sampath, Morisette, & Cooper, 2020). Presently, the standard

inversion channel mobility of gate oxides on MOSFET-SiC devices with nitridation is between 25 – 35 cm^2/Vs. One of the methods that have been recently employed for improving the challenges of low mobility is the diffusion of other elements into the gate oxide. This technique has yielded a promising result in the range of 100 – 200 cm^2/Vs mobility value. Other methods, such as the separation of carriers from the gate oxides, and the use of buried-channel devices have produced similar results (Suganuma, 2018).

2.17.2 Reliability Issues of Gate Oxides/SiC Structures

The reliability of different gate oxides on SiC surfaces has always been a source of concern in most CMOS devices. Generally, most high-κ dielectric materials tend to show significant reliability trends, such as lower breakdown strength and larger electric field, especially when compared to silica (Mohsenifar & Shahrokhabadi, 2015). Most of these high-κ gate oxides also show some similar reliability features as that of silica, which include negative and positive bias temperature instability, stress-induced leakage current, and time-dependent dielectric breakdown (Lu & Zhang, 2012). One of the features of reliability that has been considered the most limiting phenomenon in gate oxides is the positive bias temperature instability. The reason is that, it reduces the transconductance and drain current of the MOS device with a corresponding increase in the voltage threshold. A high-κ dielectric such as HfO_2 gate oxide displays some high degree of instability for both positive and negative bias temperatures during thermal-induced stresses.

During constant voltage stress, extra bulk traps are formed which causes a breakdown in the dielectric material when a critical trap density is attained. This phenomenon is referred to as time-dependent dielectric breakdown. The dielectric breakdown is caused by a tunneling

current that occurs due to the creation of an electron channel that is passed across the substrate from the gate oxide when different CMOS are activated near or above their threshold of operating voltages. This situation also results in the formation of defects between the gate oxide and the interface owing to the passage of charge carriers, which can cause a breakdown in the dielectric layer (Lu & Zhang, 2012). Therefore, in most applications where durability and reliability are of great importance, low voltage MOS are used. For instance, in power optimizers, the energy generated by the photovoltaic modules is significantly increased under severe and harsh operating conditions. Even at that, they have to ensure a high degree of reliability over a long operational period. These devices are categorized under the low voltage and low load DC to DC converters (Bencherif et al., 2020).

2.17.3 Oxidation Mechanism Model of Gate Oxides/SiC Structures

Unlike most Si-based MOSFETs in semiconductor technology (Himpsel, McFeely, Taleb-Ibrahimi, Yarmoff, & Hollinger, 1988; Gibson & Lanzerotti, 1989; Ohishi & Hattori, 1994; Watanabe, Kato, Uda, Fujita, & Terakura, 1998), a possible mechanism of oxidation model of the growth of a gate oxide on a SiC surface is yet to be established. The morphological structure observed through an HRTEM machine indicated some transition layers of nm-thickness, with high carbon content (about 20 % below the SiC/SiO_2 interface) (K. Chang, Nuhfer, Porter, & Wahab, 2000; Zheleva, Lelis, Duscher, Liu, & Das, 2008; Biggerstaff et al., 2009). Although, the bulk of the non-stoichiometric area could be responsible for the degradation of the MOSFETs' mobility (Biggerstaff et al., 2009). The report from a previous study on SiC-MOSFET indicates the existence of a near-perfect stoichiometric region based on the ion scattering technique (X. Zhu et al., 2010). Moreover,

the issue of the energy bandgap of SiC/SiO_2 interfaces still remains controversial, despite the fact that the gate leakage current is significantly increased by a low conduction band offset, especially under a high thermal operation and high breakdown electric field (A. K. Agarwal, Seshadri, & Rowland, 1997).

The alternative channel, such as the face of a 4H-SiC substrate has shown larger electron mobility than a conventional substrate of Si-based (Kimoto, Kanzaki, Noborio, Kawano, & Matsunami, 2005). A further decrease in conduction band offset was identified to be responsible for the higher mobility channel of the C-face of SiC substrate (Suzuki, Senzaki, Hatakeyama, Fukuda, & Arai, 2009). There are significant effects of the intrinsic and extrinsic structures of the interface and the electrical defects on the modulation of conduction band offset. However, much information about the background and structures has not been obtained. Another critical challenge confronting SiC-MOSFETs and their related devices is reliability, instability of threshold voltage, and low breakdown electric field due to poor gate oxide.

According to the report of Matocha et al., (2008), there is no correlation between the site of breakdown field and dislocation of SiC-MOSFETs in which gate oxides were grown on SiC substrates by successive oxidation in NO and N_2O environment. It was also shown in the AFM study of thermally grown 4H-SiC/SiO_2 structure that breakdown fields were induced preferentially with step bunching (Kozono et al., 2010). Breakdown of gate oxides is initiated when there is a connection between the substrate and electrode of an electrically defective gate oxide due to a stress field, known as percolation model (Degraeve, Groeseneken, Bellens, Ogier, & Maes, 1998). It was predicted that the concentration of an electric field can occur around the step bunching due to the generation of defects which cause a preferential

breakdown. This implies that the behaviour of oxidation of SiC surfaces that were step-bunched is influenced by epitaxial deposition and high thermal annealing when observed from the macroscopic point of view (Watanabe & Hosoi, 2012).

2.18 Energy Bandgap of Gate Oxides on SiC

A bandgap is the distance between the conduction band and the valence band of electrons. Basically, the bandgap denotes the smallest energy that is needed to activate an electron up to a level in the conduction band where it can contribute to conduction. The narrowed bandgap of nanomaterials could find applications in the area of optoelectronics, visible light-induced photo-catalysis, etc. (Ansari et al., 2014). In the study of Watanabe & Hosoi (2012), the energy bandgap of a thick oxide layer was obtained by synchrotron XPS. Thick and thin gate oxides of about 40 and 3 nm, respectively were obtained on a SiC substrate by thermal oxidation. The thickness of the thin oxide layer was obtained by reducing the thick layer to a thickness of 3 nm through a diluted HF solution. The interface quality and band structure of the SiC/SiO_2 was also obtained by a thermal process with a temperature range of 1000 and 1100 ^{o}C.

The energy bandgap of the gate oxide was investigated with respect to the valence band offset of the interface. It was first calculated from O1s energy loss spectra. This is due to the photo-electrons produced in the oxides experiencing energy losses which originated from electron-hole and Plasmon excitations. The bandgap can also be determined from the energy threshold of an energy loss spectrum in a concentrated O 1s signal (Miyazaki, Nishimura, Fukuda, Ley, & Ristein, 1997). The O 1s energy loss spectra are shown in Figure 2.22. There

is a similarity in the energy band gap of the thin film irrespective of the orientation of the substrate (8.7 eV) (Watanabe, Kirino, Kagei, Harries, & Hosoi, 2011).

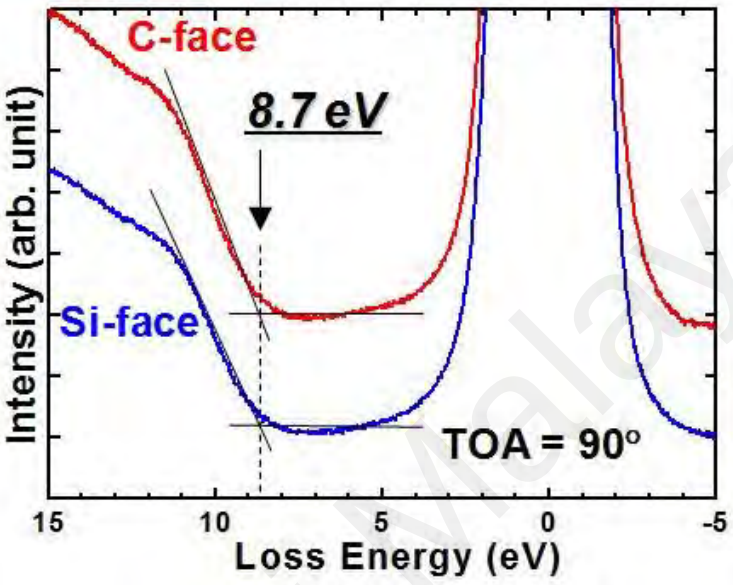


Figure 2.22: O 1s spectra for energy loss in gate oxides on SiC substrates (Watanabe & Hosoi, 2012).

Figure 2.23 shows the deconvoluted and measured values of the valence spectra gotten after depositing 3 nm of SiO_2 gate oxides on the SiC substrates during thermal oxidation. The maximum valence band offset (VBO) of the gate oxides was obtained by removing the reference spectra of SiC substrate (② from the measured spectra of SiC/SiO_2 ①.

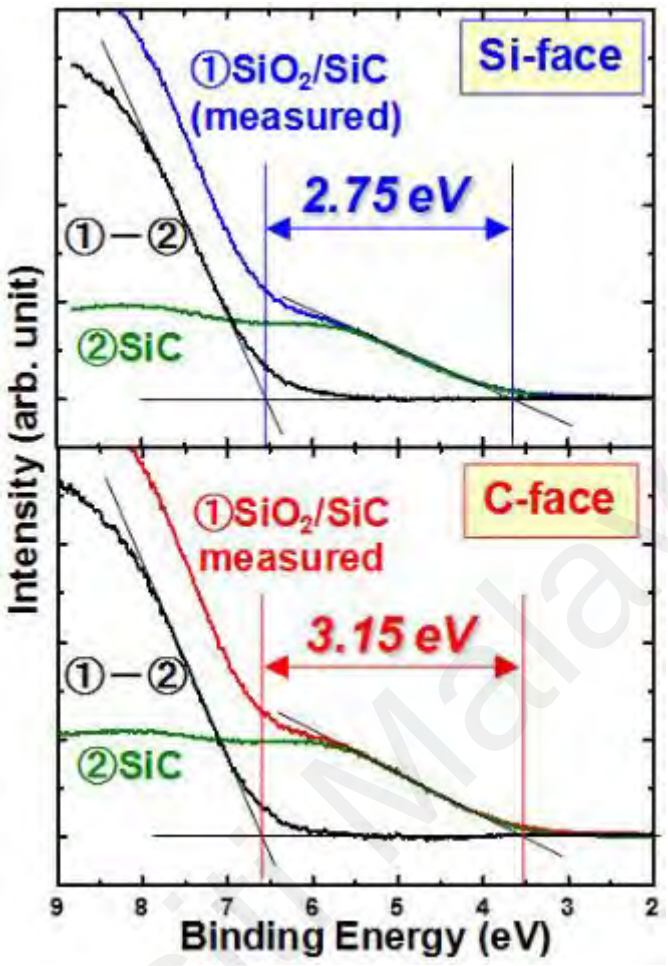


Figure 2.23: Deconvoluted and measured valence band spectra of SiC/SiO_2 structures grown on SiC substrates (Watanabe & Hosoi, 2012).

Considering the high thermal process, (more than 1000 ^{o}C) and low intensity of carbon impurities remaining within the thermally deposited films (Watanabe et al., 2011), the obtained values are quite realistic. These data showed that the VBO of the interface was about 0.4 eV higher than that of the substrate. Also, when a similar synchrotron XPS analysis of thick film samples was carried out to investigate the impact of interfacial imperfections on the modulation of energy bandgap due to an increase in oxide thickness. When the measured data and the SiC energy bandgap of the substrate that was reported were taken into

consideration (about 3.26 eV), the structural energy bandgap was obtained under different conditions. The measured values of the VBOs of the SiO_2/SiC interlayer created under these circumstances are shown. The summary is presented in Figure 2.24.

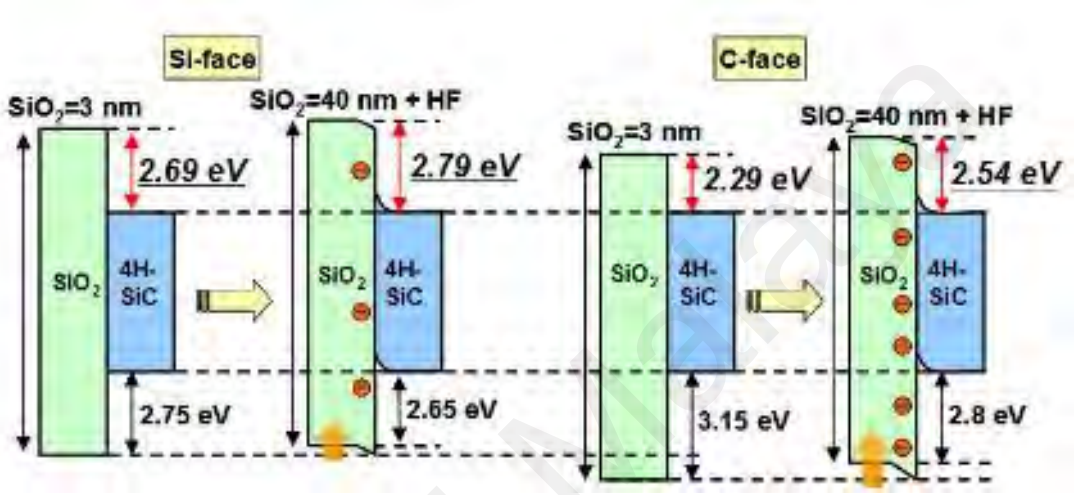


Figure 2.24: bandgap energy of SiO_2/SiC interface gotten by synchrotron XPS analysis (Watanabe & Hosoi, 2012).

The reliability and gate leakage current of the resultant gate oxide which is usually determined by the conduction band offset of the MOSFET device depends largely on the oxide thickness and orientation of the substrate. It could be observed that a lower conduction band offset is displayed by the thin gate oxide of the SiC substrate than that of the Si-face. Then, it can be argued that the issue of degradation encountered in the reliability of SiC-based MOSFETs is an intrinsic problem, which could possibly be as a result of the difference in the electronegativity between the substrate and the oxygen atoms bonded at the interlayer. In addition, when the accumulated negative fixed charges at the SiC/SiO_2 structure were considered; the band modulation of the extrinsic energy owing to interfacial imperfections explains the increase in the band conduction offset of the gate oxide on the SiC substrate.

Therefore, to reduce the gate leakage current on the gate oxide, it is preferable to have an increased band offset, but the reliability and performance of the device could be negatively affected by the electrical defects. In other words, basic approaches, such as growing gate oxides and band energy using the stacking method are very important in the development of SiC-MOSFETs (Hosoi et al., 2009; Noborio, Suda, Beljakowa, Krieger, & Kimoto, 2009; Hosoi et al., 2010; Hosoi et al., 2011; Watanabe & Hosoi, 2012).

2.19 Thermal Reliability and Stability of Thin Films in MOS

Semiconductor devices have experienced impressive improvements due to the role of high dielectric material between the substrate and the interface in various microelectronic systems. The performance reliability and stability of these devices are determined by the surface conditions of the major components on which the integrated transistor circuits are built (Reicher, Black, & Jungling, 2000; Streetman & Banerjee, 2006; Harishsenthil, Chandrasekaran, Marnadu, Balraju, & Mahendarn, 2020). This is necessary for the design and development of electronic structures with nanoscale characteristics for specific purposes. This technique has necessitated the utilization of metal oxides instead of thicker materials in the development and growth of dielectric gate oxides in metal oxide semiconductors (MOS). The use of thin films has made the production of power electronic devices easier. In addition, the coatings provided by the thin layer offer some specific properties and protection to the surface of the devices.

In the past few years, there have been several studies and investigations on the interfaces and surfaces of thin film layers (Hecht, Hu, & Irvin, 2011; Granqvist, 2014; Yanhua Jia et

al., 2021). Actually, the performance of these devices depends more on the optimized match between metal contacts and thin films in organic and inorganic semiconductors (Casu, 2018). When thin films are grown on a wafer, which is usually a different material from the film, the kind of interface formed is called, hetero-interface. The films can have different thicknesses from nanometres to micrometres in single or multilayers depending on the design. They usually have lattice constants that differ from those of the substrates. The lattice constant difference, which is referred to as lattice mismatch causes the thin film to either get elongated or compressed, leading to tensile or compressive interfacial strain, respectively.

Due to renewed interest by researchers in the properties of hetero-structures, especially those of thin films and their interfaces (Jaramillo, Ha, Silevitch, & Ramanathan, 2014; Schlom, Chen, Fennie, Gopalan, & Muller, 2014), the significance of interfacial strain in determining the thermodynamic stabilities of the hetero-structures cannot be over-emphasized. It was shown in a study by Rawat, Fong, & Aidhy (2021), that there is a strong link between the interfacial strain and O_2 interstitials. Other several studies, analytical and experimental have also revealed the importance of the interfacial strain and O_2 interstitials on the thermodynamic stability of functional oxides (Roesch et al., 2015; Alshahed et al., 2015; Barroso, Barth, Correia, Ahzi, & Khaleel, 2016; Molina-Reyes, Uribe-Vargas, Torres-Torres, Mani-Gonzalez, & Herrera-Gomez, 2017). Owing to various structural and electronic considerations, accurate predictions of a long-term operation of these devices can be made. These considerations include; the evaluation of several conduction mechanisms that can reduce the reliability and performance of the devices, specific regulation of atoms in the interfacial layer of the dielectric material, interfacial defects at the dielectric layer, low thermodynamic stability of the dielectric material after being subjected to high thermal

loading, and reduction of excessive gate leakage current density, among others (Molina-Reyes et al., 2017).

Thermal stresses occur in components owing to changes in the thermal gradient as a result of uneven distribution of temperature at the interlayer between the thin films and substrates (Streetman & Banerjee, 2006; Gordon, Dross, Depauw, Masolin, & Poortmans, 2011;). Sometimes, it occurs at the interface of dissimilar materials as residual stress due to texturing, polishing, and development of interlayer during thermal cycling (Namvar, Dehghany, Sohrabpour, & Naghdabadi, 2016; Xiao, Wu, Wu, Yin, & Huang, 2020). The thermal management of gate oxide of smaller thicknesses (less than 20 μm) is very challenging due to change in lateral thermal resistance, which implies strict cooling requirements. Thus, a rational projection of temperature gradients in such devices is very important. In this study, a Ho_2O_3 gate oxide of about 12 nm thickness is employed as a dielectric layer in a MOS device, and subjected to transient and steady-state thermal analysis. Owing to their reduced thicknesses, thin film layers are characterized by low vertical thermal resistance. The resistance of such layers is expected to increase systematically due to the small cross-sectional area. Thus, the thermal characterization and analysis of such a device are important to examine its steady-state and transient thermal properties.

Furthermore, the temperature distribution of the surface as a variable of the working condition is required, so that the thermal interaction between the thin film layer and the substrate can be predicted. However, little attention has been given to the study of their thermodynamic stability and stress analysis. Since, a larger temperature stress between the substrate and the gate oxide will result in low thermal conductivity, it will cause heat dissipation at the anode and strip-off of the thin film layer. Consequently, a thermal mismatch

at the interface will reduce the reliability and performance of the device for high thermal applications. Therefore, this research aims to provide a near-accurate and consistent method of studying the behaviour of the Ho_2O_3 thin film and SiC substrate under high thermal loading to predict the performance and reliability of a semiconductor device.

Thermal residual stress in MOS capacitors is caused by the difference in the thermal expansion coefficients of the SiC substrate and that of the Ho_2O_3 gate oxide. It is generated from cooling temperature which indicates a process from which the bond quality was evaluated (Lapadatu & Jakobsen, 2015). The stress can initiate transverse micro-cracks in microelectronic devices. If the thermal residual stress in the substrate exceeds the yield strength of the component device, shearing or cracking will occur at the substrate/interface (Safarabadi & Shokrieh, 2014). Since the stress occurs as a result of thermal mismatch between the substrate; the oxide layer, and the surrounding materials under high stresses, the device will experience a lower stress when the temperature source is moved away from the substrate.

2.20 Summary of the Review and Research Motivation

A comprehensive review of the features of silicon carbide (SiC) and various methods of deposition of gate oxides have been presented in this section. The SiC material, which is mostly employed as a base component in metal oxide semiconductor field effect transistors is very promising; for its high voltage, high power, high temperature and high breakdown field properties. These features have made it very attractive for use in power electronic devices over its counterparts in the field. Despite these great features, and the significant

progress recorded in the past few years regarding the quality of the material, there are still some issues relating to optimization of the surface and interface processing. This review discussed the effect of surface modification and treatment as a means of enhancing the electrical performance of the SiC-based MOSFETs. It also identified the challenges of controlling the density of dielectric/SiC interface trap that is needed to improve the values of mobility channels, and several oxidation techniques that could be used to surmount the structural limitations presently encountered by the SiO_2/SiC system. Reliability as a significant aspect of electronic structures was also discussed with much emphasis on the causes of their breakdown and possible solutions, especially in high thermal applications.

CHAPTER 3: MATERIALS AND METHODOLOGY

3.1 Introduction

This chapter discusses the materials and the methodology used in this study. The overview of the whole research process is shown in form of a flow chart in Figure 3.1. The details comprising experimental procedures and the preparation of samples are also illustrated in Figure 3.2, while figure 3.3 presents the characterization techniques used in the study. The chapter is comprised of three main sections; namely:

(1.) Materials,

(2.) Experimental procedures, and

(3.) Characterization techniques.

The materials and consumables that are used in this study include:

(i) SiC wafers as substrates

(ii) Chemicals used in the cleaning of the substrates

(iii) Target materials for Holmium and Aluminum sputtering

(iv) Gases used for thermal oxidation processes

The experimental procedures that are involved in the preparation of samples are stated as follows:

(i) Cleaning process of the SiC substrates,

(ii) Sputtering of Ho thin films on the SiC substrates,

(iii) Thermal oxidation of sputtered samples of SiC in O_2 and N_2 medium, and

(iv) Sputtering with an Aluminum target for the production of MOS capacitor.

The characterization techniques that were employed in this research include physical and electrical characterizations. The details are presented in Figure 3.3. The physical techniques include Fourier transform infra-red (FTIR) spectroscopy analysis, X-ray diffraction (XRD), High-resolution transmission electron microscopy (HRTEM), Microscopic Imaging and X-ray photoelectron spectroscopy (XPS), while the current-voltage (*I-V*) analysis is meant for the electrical characterization.

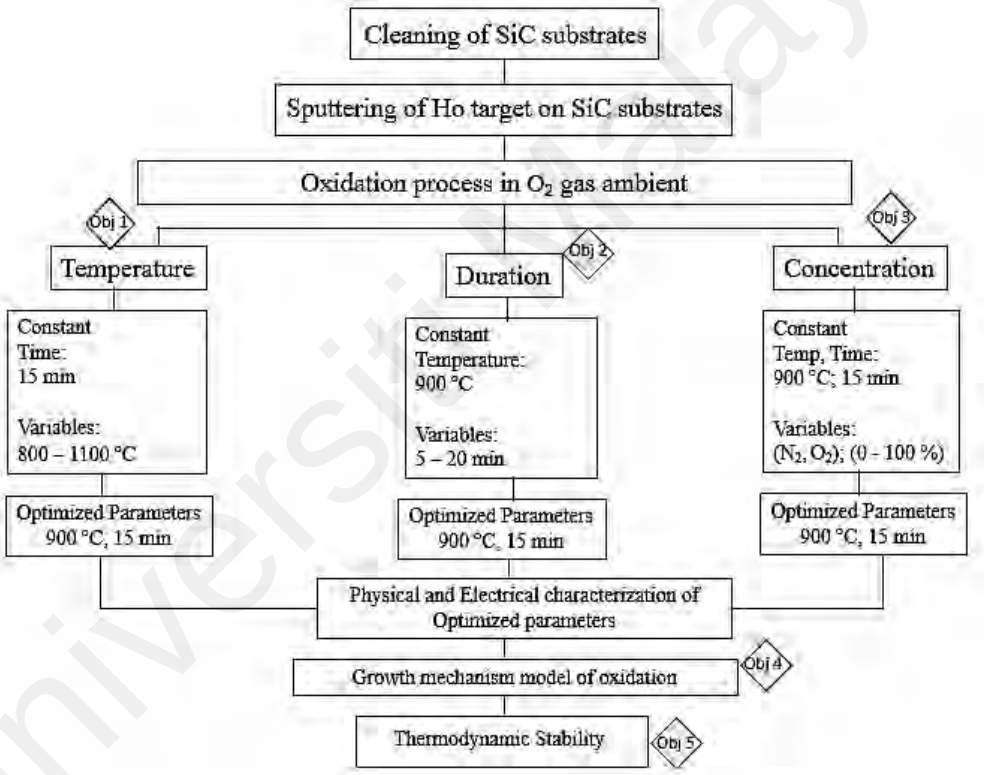


Figure 3.1: Processes, stages and characterizations involved in the fabrication.

Notes:

(i) The objectives refer to the objectives numbered as 1, 2, 3, and 4, respectively.

(ii) Details of the objectives have been described in section 1.3.

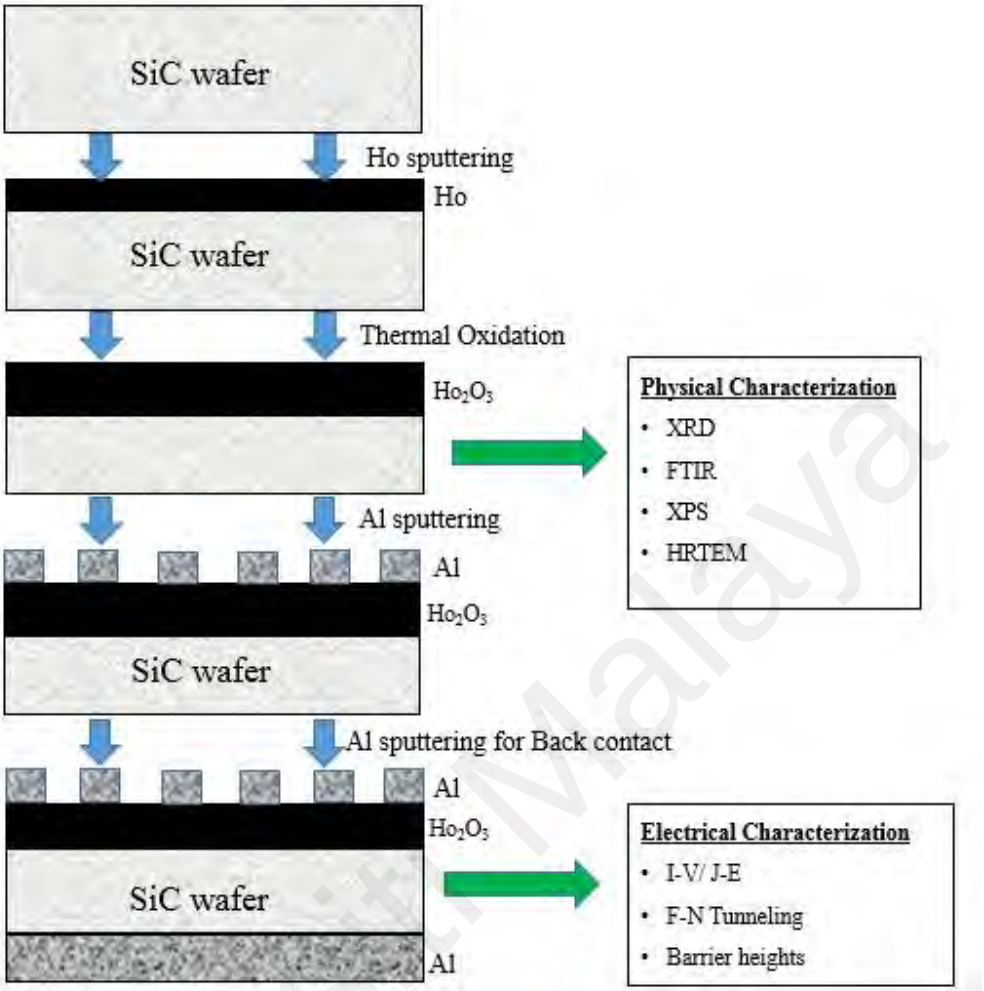


Figure 3.2: Steps involved in the preparation of samples

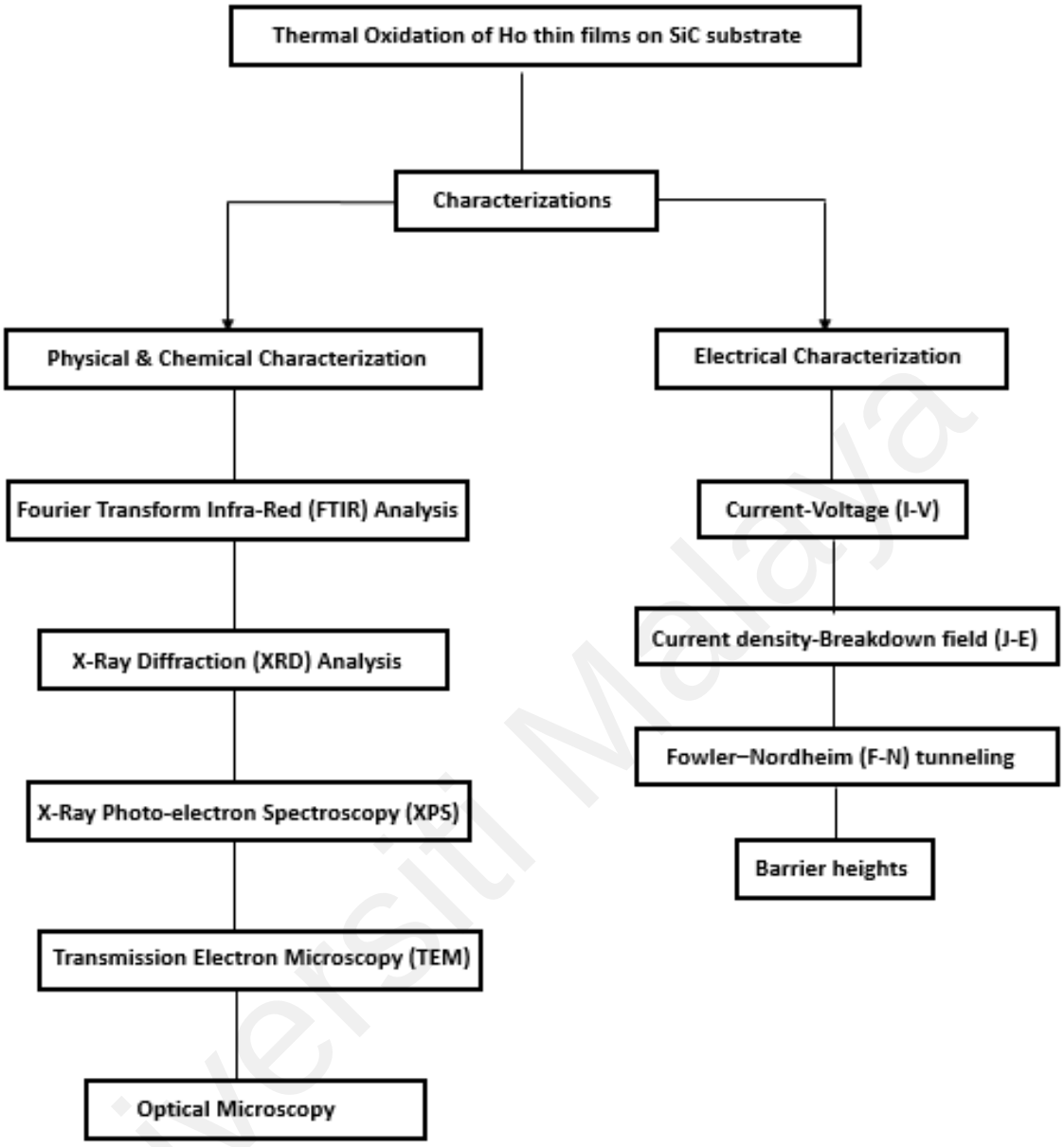


Figure 3.3: The overview of the characterization techniques used in this study

3.2 Materials

3.2.1 Substrate Material

The Silicon carbide wafers (4H-SiC), used as substrates in this research were obtained from CREE Inc. (USA). The wafers are silicon-faced, n-type epitaxial layer, doped with

nitrogen at a concentration of 14×10^{15} cm^{-3}, 0.8 cm × 0.8 cm dimension, 4.09° off-axis, 1-μm thick, resistivity of 0.02 Ω cm, and (0001) oriented.

3.2.2 Materials and Chemicals used for Cleaning of the Substrate

Prior to sputtering, the following chemicals are employed in the preparation of samples. The chemicals include Hydrochloric acid, Hydrogen Fluoride, Hydrogen Peroxide, Ammonia Hydroxide and acetone. They are presented in Table 3.1 according to their percentage concentration and the suppliers' details.

Table 3.1: List of chemicals used in the RCA cleaning process of SiC substrates

No	Chemical	Chemical Formula	Assay	Supplier/CAS No.
1	Ammonia Hydroxide	NH_4OH	29 %	R & M Chemicals / 1336-21-6
2	Acetone	$(CH_3)_2CO$	> 99 %	R & M Chemicals / 67-64-1
3	Hydrogen Fluoride	HF	49 %	R & M Chemicals / 7664-39-3
4	Hydrogen Peroxide	H_2O_2	30 %	R & M Chemicals / 7722-84-1
5	Hydrochloric Acid	HCl	37 %	R & M Chemicals / 7647-01-0

Note: CAS No. is the acronym for Chemical Abstracts Service numbers.

3.2.3 Materials used for Sputtering Process

Holmium and Aluminum targets, and Argon gas were used in this study for metallization process. Prior to sputtering through a physical vapour deposition process, the sputtering chamber was cleaned with acetone to remove any unwanted dirt or dust. The details of the chemicals and the target materials used are presented in Table 3.2.

Table 3.2: Target materials and gases used in the PVD sputtering process.

No	Material	Chemical Formula	Supplier/CAS No.	Specification
1	Argon gas	Ar	Gaslink / 7440-37-1	Purity: 99.99%
2	Acetone	$(CH_3)_2CO$	R & M Chemicals / 67-64-1	Purity: 99.99%
3	Aluminium	Al	Kurt J. Lesker	Purity: 99% Diameter: 101.6 mm Thickness: 3.175 mm
4	Holmium	Ho	Kurt J. Lesker	Purity: 99.9% Diameter: 101.6 mm Thickness: 3.175 mm

3.2.4 Gases used for Thermal Oxidation Process

The gases used for oxidation include O_2 and N_2. Their details are presented in Table 3.3.

Table 3.3: Parameters of gases used during the thermal oxidation process.

No	Gas	Chemical Formula	Supplier/CAS No.	Specification
1	Argon	Ar	Gaslink / 7440-37-1	Purity: 99.99%
2	Nitrogen	N_2	Gaslink / 10024-97-2	Purity: 99.99%
3	Oxygen	O_2	Gaslink / 7782-44-7	Purity: 99.99%

3.3 Experimental Procedures

3.3.1 Cleaning Process for SiC Substrates

Prior to deposition of Ho, the substrates were cut into square sizes of 0.5 × 0.5 cm^2 dimension using a cutter made of diamond material. The substrates were then cleaned by dipping them in solutions containing HF chemicals, followed by rinsing in DI water. The samples were rinsed thoroughly for about 5 times in the DI water to ensure that the chemicals were totally removed. These were done according to the standard process of cleaning Radio Corporation of America (RCA). The flow chart of the cleaning process is presented in Figure 3.4.

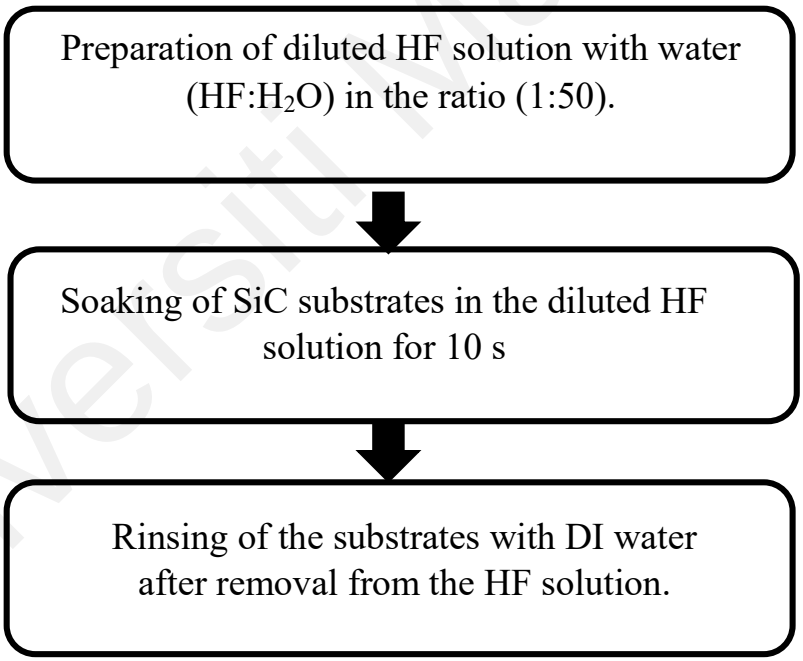


Figure 3.4: Flow chart of the cleaning processes of SiC substrates

3.3.2 Sputtering Process of Ho Thin Films

Ho thin films were grown on the substrates using a physical vapour deposition (PVD) machine, with radio frequency (RF) sputtering system (model no. TF 450). The shutter target, substrate holder, and the sputtering chamber were all cleaned with acetone before the sputtering of Ho on the SIC substrates. This is done to prevent the sputtering chamber from any dirt or risk of contamination. The SiC substrates were fixed on the substrate holder, while the Ho target was placed on the target holder. The door of the sputtering chamber was locked afterwards. Prior to the sputtering process, a pre-sputtering was done to eliminate any native oxide on the surface of the Ho target. This was done for about 3 minutes. The working parameters of the system are, working pressure, 3×10^{-3} Pa, base pressure of 1.5×10^{-3} Pa, volume flow, 25 cm^3/min and RF power supply of 170 W. The distance between the substrate and the target was set to about 200 mm. The schematic diagram of the sputtering system is shown in Figure 3.5.

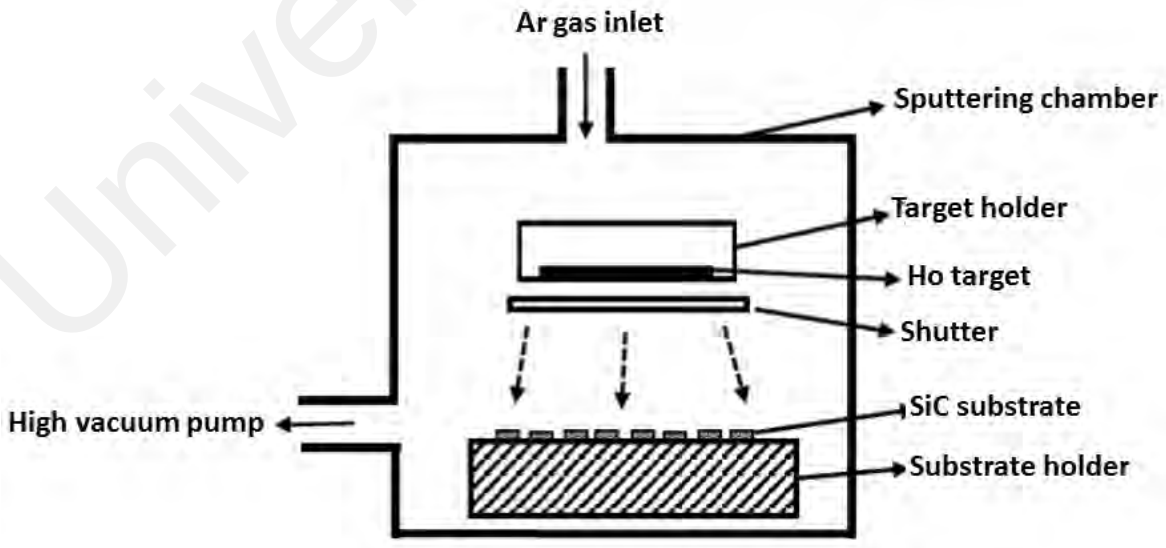


Figure 3.5: The schematic diagram of the PVD sputtering system.

3.3.3 Thermal Oxidation of Sputtered Ho Thin Film on SiC Substrate in O_2 Gas Ambient

Although, more advanced equipment is available in the deposition of thin film dielectric, thermal oxidation of substrate by sputtering is still the most popular method to fabricate the gate dielectric in the CMOS industry (May & Spanos, 2006), the product of SiO_2 in thermal oxidation still remains the dominant gate oxide in CMOS industry (Schlom, Chen, Pan, Schmehl, & Zurbuchen, 2008). The thermal process which includes thermal oxidation and nitridation was performed by using a horizontal tube furnace, while the oxidation process was carried out by heating the SiC substrate in the presence of O_2 in the quartz tube. Prior to the thermal oxidation, the quartz boat and tube were cleaned with diluted HF solution to prevent them from contaminants. Thereafter, the quartz tube containing samples on a quartz boat was placed in a horizontal tube furnace (Figure 3.6). The experimental set-up is shown in Figure 3.7.

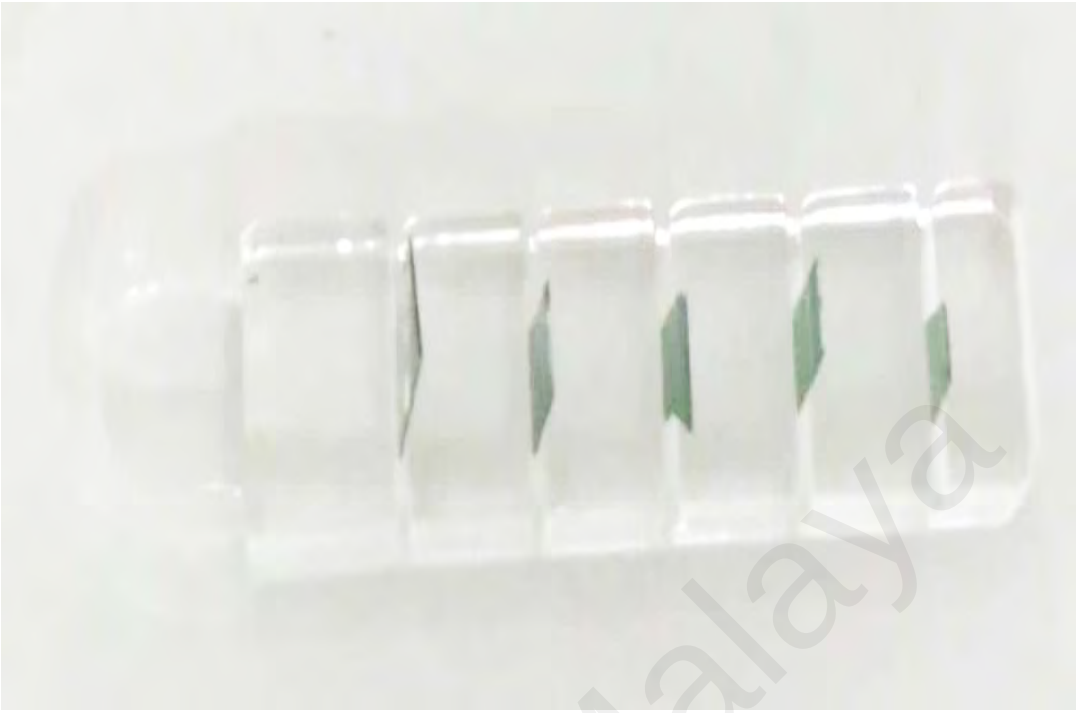


Figure 3.6: Samples on a quartz boat

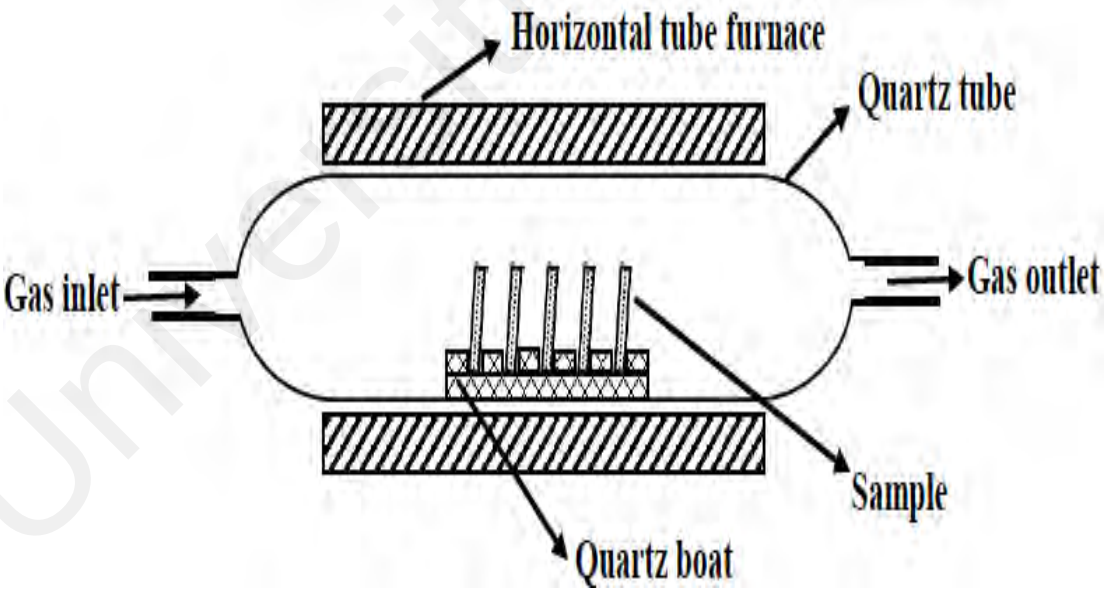


Figure 3.7: Experimental set-up for thermal oxidation

To evaluate the effect of thermal oxidation on the sputtered Ho thin film on the SiC substrate, the samples were heated up to a temperature range of (800 – 1100 °C) at an interval of 100 °C in Ar gas with a heating rate of 10 °C/min. O_2 gas was then introduced into the quartz tube at a flow rate of 150 ml/min for 15 min when the set temperature was attained. The oxidized samples were then cooled down to room temperature. Another set of samples was heated in a similar manner to determine the effect of oxidation time on thermal oxidation of the samples, with a set of duration in a range (5 - 20 min) at an interval of 5 min. The oxidized samples were then cooled in O_2 ambient.

3.3.4 Fabrication of MOS Capacitor

The thermally oxidized samples were fabricated into MOS capacitors. This is meant to evaluate its electrical features and its capacity. For the electrical characterization, a 100 nm thick Al layer was deposited on both the top and bottom surfaces of the sample by sputtering. The process of sputtering in this regard is similar to that of Ho in section 3.3.2, but for back contact metallization, the sputtered surfaces are turned upside down and covered with a shadow mask, and the same procedure of sputtering is repeated using Al target (Figure 3.8)**.** The working parameters, such as the argon gas flow rate, RF power, working pressure, base pressure, and the distance between the target and the substrate were all similar to the ones used for the Ho sputtering.

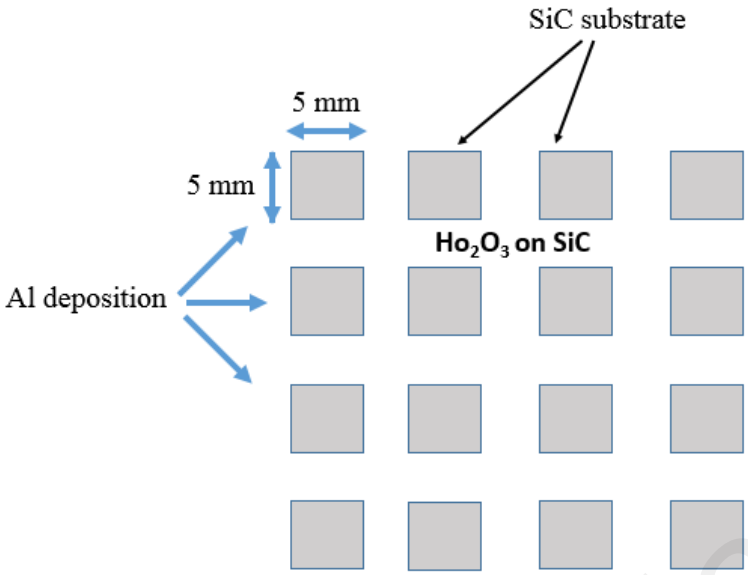


Figure 3.8: Al sputtering for back contact metallization

3.4 Characterizations Techniques

3.4.1 Fourier Transform Infra-Red (FTIR) Analysis

The FTIR is a process employed for obtaining an infra-red spectrum of emission or absorption of a gas, liquid or solid. It is very useful for identifying the functional groups that accommodate some clearly-defined frequencies. It can also be used to obtain high-spectral-resolution data over a wide range of spectra (Goh et al., 2016a; de la Rosa, Portillo, Mora-Ramírez, Téllez, & Moreno, 2020). FTIR analysis was used in this study to examine the chemical working atoms in the samples. The analysis of the samples oxidized at various temperatures are presented in form of figures. FTIR was conducted using the Fourier-transform infrared (FTIR) spectrometer (Bruker Platinum ATR Tensor 27 model). The scanning range of 500 – 1500 cm^{-1} transmittance mode was used.

3.4.2 XRD Analysis

XRD is a method used for the investigation and identification of chemical and physical features of the oxidized samples. It is a common technique for the characterization of the crystal structure of thin films (Wong & Cheong, 2012; Goh et al., 2016a; Hetherin et al., 2017a; Lei et al., 2018). A Rigaku SmartLab x-ray diffractometer (XRD) machine was used to examine the crystallinity of the film in the 2 *theta* scan between 0 and 90 ^{o}C. An x-ray source of 40 kV and 30 mA was used to run the copper radiation (Cu Ka) with a wavelength, λ of 1.5418 nm. The process of diffraction of an x-ray given by Bragg's law is presented in equation 3.1.

$$\lambda = 2d \sin \theta \tag{3.1}$$

where λ is the radiation beam's wavelength (nm), d is the crystal inter-planar spacing (nm), and 2θ is the angle between the transmitted and the diffracted beams (°). Since the structures of most materials are not single crystals, the detection of several potential orientations of crystalline compounds can be done by their pattern of diffraction. Not only the structural or atomic or molecular can be gotten from the pattern of diffraction, but also the phases, composition, and state of polycrystalline compounds.

The samples of Ho_2O_3 thin films were examined by the XRD machine. The plot of diffraction pattern i.e (graph of angle 2θ versus intensity of x-ray) for each sample was obtained after the scanning. The microstrain (Ɛ) due to crystal voids such as dislocations and crystallite size (D) were also determined from the broadening of XRD peak (Venkateswarlu, Bose, & Rameshbabu, 2010; Lei et al., 2017). These two parameters can be obtained from three different methods, namely; Fourier method, simplified integral breadth, and double Voigt method. Out of these methods, the simplified integral breadth method provides the

mean value rather than the distribution of crystallite size (Santra, Chatterjee, & Gupta, 2002; Vives, Gaffet, & Meunier, 2004; Mittemeijer & Welzel, 2008; Herrmann, Förter-Barth, Kempa, & Kroeber, 2009; Mote, Purushotham, & Dole, 2011). The simplified integral breadth approach was used. It consists mainly of two basic methods, namely; Williamson-Hall (W-H) and Debye-Scherrer analysis (Mittemeijer & Welzel, 2008; Mote et al., 2011).

The Williamson-Hall (W-H) analysis uses the broadening of multiple peaks to determine the microstrain and crystallite size. Another independent factor that contributes to the broadening of the total peak is the lattice strain (Venkateswarlu et al., 2010; Mote et al., 2011; Zak, Majid, Abrishami, & Yousefi, 2011). Broadening induced by strain owing to distortion of crystals and voids was given by

$$\varepsilon = \frac{\beta_e}{4\tan\theta} \tag{3.2}$$

where β_e was the peak width at half maximum intensity and θ was the peak position. For the Debye-Scherrer analysis, the Scherrer equation was used to determine the average crystalline size of Ho_2O_3 (Venkateswarlu et al., 2010; Mote et al., 2011). When both microstrain and crystallite size occur together, there is a reflection in the broadening of samples. Therefore, those properties are assumed to be uniform in all crystallographic directions, and the material properties are non-dependent on the direction of measurement. The crystallite size, *D* from the Scherrer equation is given by

$$D = \frac{K\lambda}{\beta_D \cos\theta} \tag{3.3}$$

where *K* is a constant, λ is the radiation's wavelength, which is equal to 0.9, β_D is the peak width at half maximum intensity, and θ is the peak position. Combining equations (3.2) and (3.3), It was observed that the crystallite size varies as $1/\cos\theta$ (integral breadth of Lorentzian component) while the peak width from the strain varies as $\tan\theta$ (integral breadth

of Gaussian component) whereas crystallite size varies as $1/cos\ \theta$ (integral breadth of Lorentzian component) (Mittemeijer & Welzel, 2008; Mote et al., 2011; Zak et al., 2011).

For the W-H analysis, assuming that the strain effects on peak broadening and crystallite size are independent, and both have a Cauchy-like profile (convolution of Gaussian and Lorentzian profile), the broadening induced by strain is the sum of Scherrer (Equation 3.2), and the broadening of the peak (Equation 3.3). Therefore, the sum of Equations 3.2 and 3.3 becomes

$$\beta_{hkl} = \beta_D + \beta_S \tag{3.4}$$

$$\beta_{hkl} = \mathrm{K}\lambda\, \beta_{\mathrm{D}} \cos\theta + 4\varepsilon \tan\theta \tag{3.5}$$

after re-arrangement, the W-H equation then becomes

$$\beta_{hkl\cos\theta} = \mathrm{K}\lambda D + 4\varepsilon \sin\theta \tag{3.6}$$

3.4.3 HRTEM Analysis

High-resolution transmission electron microscopy (HRTEM) is an imaging technique of specialized microscopy mode that permits direct scanning of the atomic structure of samples through a high electron energy beam (Spence, Kolar, Hembree, Humphreys, & Justo, 2006; Lei et al., 2018). It is a very useful method of studying the properties of semiconductor materials on a micro-scale. An image is produced from the interaction between the samples and the transmitted electrons. The magnification of the image is done along with control to focus on the samples. The atomic scale imaging is made possible owing to the high resolution. The HRTEM is capable of providing reciprocal space (in the diffraction mode) and information in real space (in the imaging mode), simultaneously.

In this study, (HR-TEM JOEL model 2200) system was used to analyze the morphological properties of the samples. The films' cross-sections were primed by lamella preparation before imaging with HRTEM. The focused ion beam (FIB) used during the preparation of samples is protected from damaging the samples due to ion bombardment from the deposition of platinum (Pt) on the samples' surface.

3.4.4 Optical Microscope Image Analysis

Generally, optical microscopes are used to examine the surface of samples for further analysis. In this study, magnified images are generated with the aid of the control of high-resolution lenses and visible refracted light. The original images were magnified twice, so that the magnified images can be properly obtained. In the first magnification, the primary image was generated by the objective lens, while the final image was generated by the eye lens. In theory, the image can be magnified as many times as possible, but, the resolution of the generated image is affected by the light wavelength. The limitation in the imaging capacity of the optical microscope is attributed to the resolution of its lens and the bandgap. The image resolution can be improved by reducing the light wavelength, but the photon will be absorbed by the lens once the photon energy is greater than the lens bandgap (Noae, Ikeuchi, Moritni, Endoh, & Yokoyama, 2013; Lei et al., 2018). In this study, the Olympus microscope (model BX61) was used for imaging the samples' surfaces. Two magnification sizes, 50 x and 500 x were used alternately for all the samples, and these were observed up to micro-level.

3.4.5 XPS Measurements

XPS is a technique based on the photoelectric effect which is used for the identification of elements that exist in a material, its surface, chemical state, and the density of the electronic structure through a surface-sensitive quantitative spectroscopy. A spectrum in a photoelectron is captured by calculating free electrons over a range of kinetic energies. The spectrum enables the peaks to appear on atoms from which electrons are emitted for a specific energy characteristic. The peaks of intensities and energies of the photoelectron allow all the surface elements to be identified and quantified with the exception of hydrogen (Levasseur, Vinatier, & Gonbeau, 1999; Opila et al., 1999; Fadley, 2010; Q. S. Wang et al., 2020). It is considered an effective method of measurement owing to the fact that, it does not only display the elemental composition, but also their bond with other elements. It is also used in line-profiling of elements that are present on the surface, or in-depth profiling when matched with ion-beam etching. It is often used to investigate chemical processes of materials in their as-received state or during ion-implantation, ultraviolet light, reactive solutions with gases, scraping, exposure to heat, or after cleavage.

The depth profile and the chemical constituents of the samples were investigated using ESCALAB-250 XPS system with Al-K_α X-ray source with energy ($h\nu$ = 1486.6 eV), an Ar pressure chamber of 4×10^{-5} Pa, ion etching of 5-kV. The area of analysis of the spectrometer is 220×220 μm^2 and was run at a take-off angle of 0^o with respect to the normal surface and operating power of 150 W. CasaXPS software ver. 2.3.23 was used to analyze the XPS data. The values of the binding energy were normalized and calibrated to the C 1s peak at 284.6 eV (Wong & Cheong, 2012). The combined narrow and wide scan was used to obtain the chemical constituents of the films. A wide scan was first carried out to examine the chemical

states of the element with a moving energy of 160 eV for about 9 min. While, a narrow scan was later conducted with passing energy of 20 eV for 5 min, etching time of (0 – 100 s) at 10 s interval per cycle or per level.

3.4.6 Electrical Measurement

3.4.6.1 Current–Voltage (I–V)

The current–voltage (I–V) data was examined from the I–V (Keithley 4200 semiconductor parameter analyzer. The data was later analyzed and represented by leakage current density–breakdown field (J–E). The value of E is gotten from

$$E = (V_g - V_{fb})/t_{ox} \tag{3.7}$$

where V_g represents the gate voltage, flat band voltage and the oxide thickness are represented by V_{fb} and t_{ox}, respectively (Wong & Cheong, 2010; Kurniawan, Cheong, Razak, Lockman, & Ahmad, 2011; Kurniawan, Wong, et al., 2011). The explanation of charge-trapping and the tunneling, i.e passage device for the conduction of the primary gate leakage current is done through the J–E features. Also, the performance of the device is influenced by densities of interface defect and oxide variation due to irradiation of gamma (Manikanthababu, Tak, Prajna, Singh, & Panigrahi, 2020).

3.4.6.2 Fowler–Nordheim (F-N) Tunneling

F-N tunneling is one of the vital processes in the description of the (I–V) features of a MOS device. It is mostly used in conventional thin films to describe the conduction behaviour of the material (Latreche, 2003). It possesses a barrier that has triangular shape and tunneling

from the gate oxide (Song & Rhee, 2005; Hetherin et al., 2017b). Both F–N tunneling and direct tunneling demonstrate similar behaviour in terms of mechanism, i.e channeling to an anode directly from the cathode (Yu, Guan, & Wong, 2011; Goh, Haseeb, & Wong, 2017). Although, their difference is characterized by the nature of their occurrence, but in most cases, F–N tunneling occurs at a higher electric field while direct tunneling occurs at the thinnest gate oxide (Takagi, Yasuda, & Toriumi, 1999; Yu et al., 2011; Goh et al., 2017). In this study, the I–V data which was transformed into J-E result was later used to plot the F–N tunneling linear regression graph. According to the F–N tunneling equation (Forbes, 1999a),

$$J_{\mathrm{FN}} = \mathrm{AE}^2 \exp[\tfrac{-B}{E}], \tag{3.8}$$

$$A = \left[\frac{q^3}{8\pi h \Phi_B}\right][\frac{m}{m_{ox}}], \tag{3.9}$$

$$B = \frac{8\pi (m_{ox}\Phi_B^3)^{1/2}}{3qh}, \tag{3.10}$$

where h denotes Planck's constant (4.135 x 10^{-15} eV s), m_{ox} represents the effective electron mass at the oxide region, while m denotes the free electron mass. By re-arranging all constants, parameters A and B can be given as

$$A = 1.54 \text{ x } 10^{-6}\ [\frac{m}{m_{ox}}][\Phi_B], \tag{3.11}$$

$$B = 6.83 \text{ x } 10^{7}\ [\frac{m_{ox}}{m}][\Phi_B^3]^{1/2}, \tag{3.12}$$

After re-arrangement, equation (3.8) can now be expressed as

$$\ln\left[\frac{\mathrm{J}}{\mathrm{E}^2}\right] = [\frac{-\mathrm{B}}{\mathrm{E}}] + \ln \mathrm{A} \tag{3.13}$$

A and *B* are significant in the design of circuits where floating-gate components are used due to their relationship with offset trimming, pattern recognition circuits and artificial neural

networks (Latreche, 2003; Casados-Cruz, Reyes-Barranca, & Moreno-Cadenas, 2011). According to the linear equation, parameter A is obtained from the y-intercept, while B is derived from the gradient. The effective mass of high dielectric gate is assumed to be 0.3 m in the equation (Goh et al., 2016b; Salmani-Jelodar et al., 2016).

3.4.7 Finite Element Modelling and Simulation of MOS Capacitor

To investigate the thermal characteristics of the Ho_2O_3 thin film and the SiC substrate in a semiconductor device, a three-dimensional (3D) finite element model (FEM) thermal simulation was carried out using ANSYS 2020 R1 software. ANSYS is an engineering analysis software used for predicting and calculating different thermal and mechanical behaviours of materials under certain conditions. The geometry of the simulated capacitor shown in Figure 3.9 was developed in ANSYS Workbench. The capacitor was modelled as a thick plate of SiC with dimensions of 10 mm × 10 mm × 2 mm as the substrate material, while the Ho_2O_3 gate oxide of 10 mm × 10 mm × 11.5 nm dimension was modelled as a thin dielectric layer created on the substrate. Table 3.4 shows the material properties of the thin film used in the simulation. The thermo-physical properties like Young's modulus, density, poisson ratio, thermal conductivity, etc, of the dielectric film were considered as listed in the table. The material properties of SiC are already built-in in the ANSYS software.

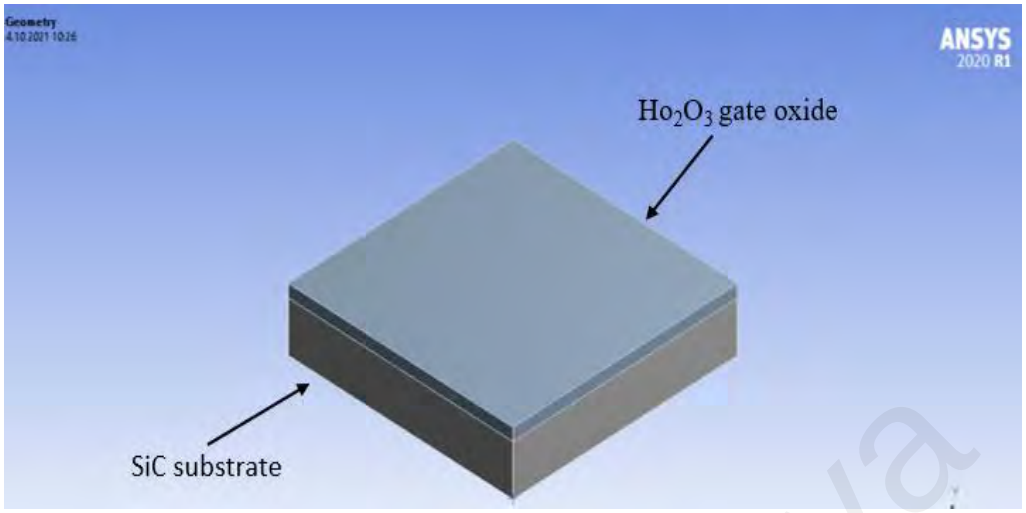


Figure 3.9: The geometry of the SiC substrate/Ho_2O_3 gate oxide structure

Table 3.4: Material properties of Ho_2O_3 used in this study

Property	**Unit**	**Material**	**Ref.**
Density (ρ)	g/cm^3	8.41	(Westrum Jr & Justice, 1963)
Thermal Conductivity (k)	$Wcm^{-1}C^{-1}$	16	(Westrum Jr & Justice, 1963)
Young Modulus (E)	MPa	1.694	(Manning, Hunter Jr, & Powell Jr, 1969)
Shear modulus (G)	MPa	656.4	(Manning et al., 1969)
Bulk Modulus (B)	MPa	1346.8	(Manning et al., 1969)
Poisson ratio (v)	-	0.29	(Manning et al., 1969)

CHAPTER 4: RESULTS AND DISCUSSION

4.0 Introduction

This chapter presents the experimental results, investigation of samples, and their analysis with regards to physical and electrical characterization. It also discusses their output with reference to the results of previous researches. The discussion is divided into four main parts, which bothers on the major objectives of this study: (i) the effects of thermal oxidation on the physical, chemical, and electrical properties of Ho_2O_3 on SiC substrate. (ii) effects of oxidation time on the physical and electrical properties of Ho_2O_3 on SiC substrate. (iii) effects of O_2 and N_2 gas concentrations on the physical and electrical characteristics of Ho_2O_3 on SiC substrate. (iv) thermodynamic stability and thermal stress analysis of Ho_2O_3 thin film on SiC substrate. The oxidation mechanism model was discussed on both effects of thermal oxidation and oxidation time, while the comparison of the effect of thermal oxidation and oxynitridation was also discussed in another section.

4.1 The Effects of Thermal Oxidation on the Physical, Chemical, and Electrical Properties of Ho_2O_3 on SiC Substrate

4.1.1 Physical Characterization

4.1.1.1 FTIR Analysis

FTIR analysis was used in this study to examine the chemical working atoms in the samples (Goh et al., 2016a; de la Rosa et al., 2020). The analysis of the samples oxidized at

various temperatures is displayed in Figure 4.1. The traces of SiO_2 in the oxidized samples were detected between 1000 and 1100 °C by FTIR. This observation was in alignment with the findings in XRD analysis and the features of J-E which will be discussed later in this thesis. The peaks of SiO_2 at 820 and 1050 cm^{-1} (Nagai & Hashimoto, 2001; de Urquijo-Ventura et al., 2020) were detected at those temperatures. The peak values of Ho_2O_3 between 950 and 1250 cm^{-1} were observed in all the samples. Although, characteristic peaks of Ho_2O_3 were noticed in all the samples between 800 and 1100 °C, the highest intensity was observed at 1100 °C.

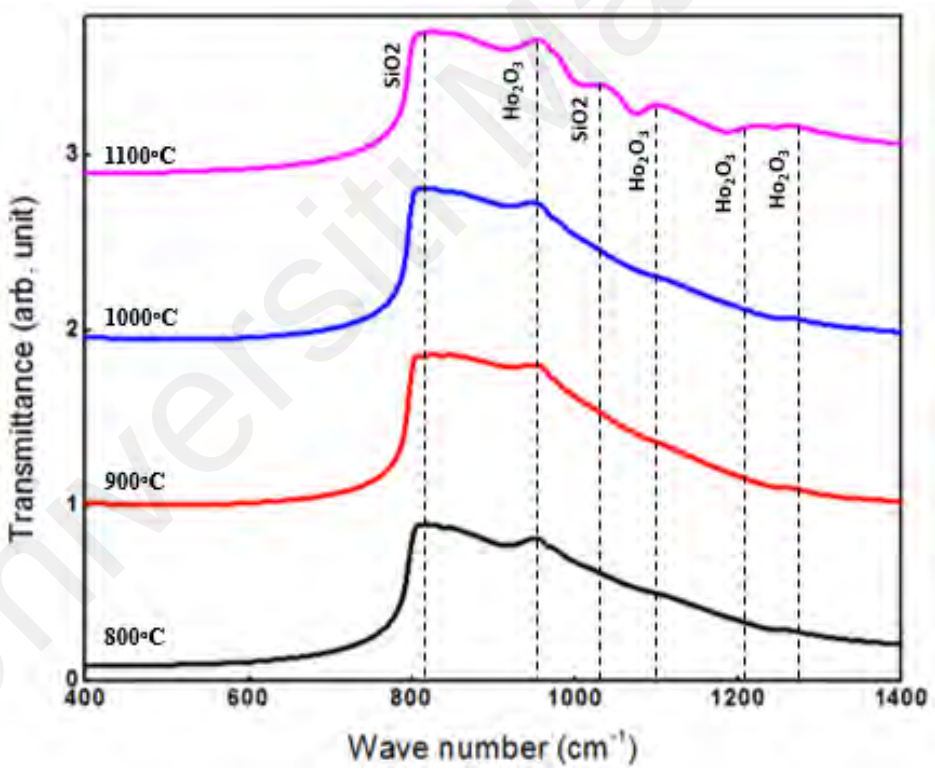


Figure 4.1: FTIR spectra for Ho deposited on SiC substrate at (800 – 1100 ˚C).

4.1.1.2 X-Ray Diffraction (XRD)

The XRD patterns of oxidized samples at various temperatures are presented in Figure 4.2. For the 800, 900, 1000, and 1100 °C samples, six peaks that were identified as monoclinic-(b) Ho_2O_3 (111), Ho_2O_3 (003), Ho_2O_3 (431), Ho_2O_3 (411), Ho_2O_3 (620) and Ho_2O_3 (541) were observed at peaks corresponding to 28.76°, 35.27°, 38.53°, 42.44°, 47.81° and 53.50° respectively. Inorganic Crystal Structure Database (ICSD) with the reference code 67216 was used to match the peaks. The trigonal-(H) SiO_2 (100) and (440), monoclinic-(c) SiO_2 (101), SiO_2 (400), SiO_2 (444), SiO_2 (640) were found at 22.25°, 57.11°, 27.21°, 47.18°, 60° and 69.01°, respectively between 1000 and 1100 °C. These peaks correspond to reference code 24259 of the ICSD. This could contribute to the dispersal of oxygen through the Ho_2O_3 layer that reacted with SiC to form the crystallization of SiO_2. However, the absence of visible diffraction peaks of SiO_2 during oxidation of 800 and 900 °C indicates the amorphous structure of SiO_2 under these conditions. The peak heights are high due to a preferred crystal orientation (Hetherin et al., 2017a).

Accordingly, the peak of 47.18° at 1100 °C corresponds to the preferential crystal orientation of SiO_2 since this peak indicates the highest intensity of SiO_2. As the oxidation temperature increased, the amount of Ho_2O_3 peaks also increased. The preferential crystal orientation of the Ho_2O_3 peak is suggested at 28.76° corresponding to (111) plane. This peak showed the highest Ho_2O_3 intensity for all the investigated samples. However, for all the samples, there was no detectable diffraction peak from the SiC substrate. This is due to the glancing angle mode used during the XRD analysis. This implies that only Ho_2O_3 and SiO_2 compounds on the thin film can be viewed without any course to the substrate.

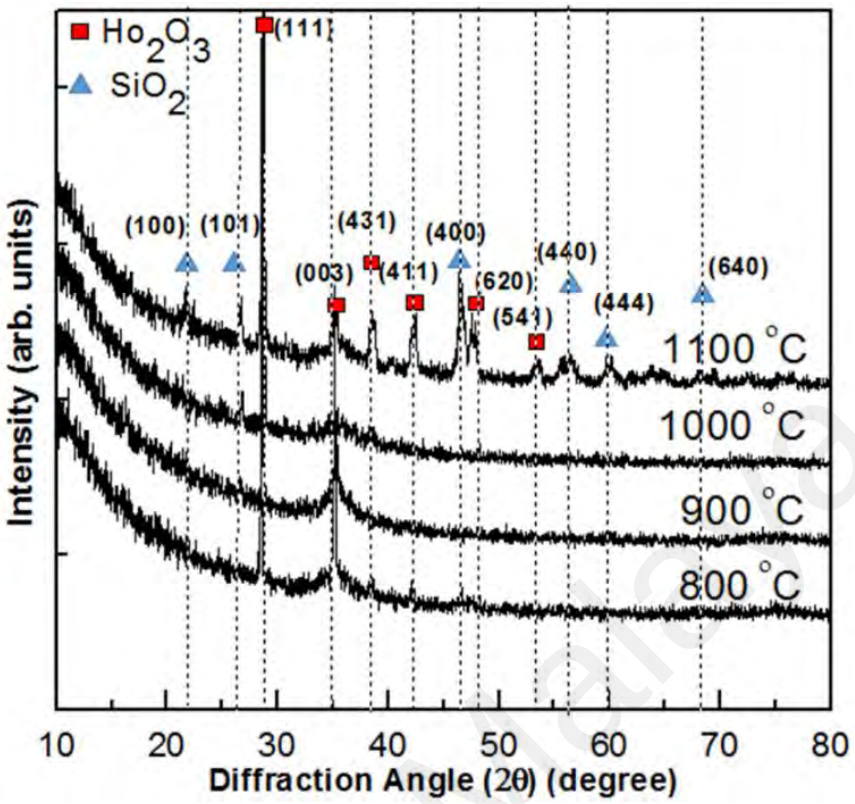


Figure 4.2: XRD spectra of samples of SiC/Ho_2O_3 oxidized at different temperatures

4.1.1.3 W-H Plot Analysis

The results obtained from XRD patterns were used in Williamson-Hall (W-H) analysis to determine crystallite size and micro-strain. This method is one of the best and most accurate techniques, as it provides a better way of calculating the properties of material, especially the structural features, the strain and the phase components. It depends largely on the principle of approximation formula for strain and size broadening X-ray line broadening in metals (Hall, 1949; Kibasomba, Dhlamini, Maaza, Liu, & Rashad, 2018). Since, both micro-strain and crystallite size contribute to peak broadening of the XRD pattern hence, their combined effects are described by a simple sum convolution equation (4.1)

$$\beta_T = \beta_D + \beta_e \quad (4.1)$$

where β_T is the total broadening, β_D and β_e are peak width at half maximum intensity of the peak broadening caused by crystallite size and micro-strain, respectively. According to Debye–Scherrer equation, peak broadening is uniform in all crystallographic directions. Therefore, the material properties are non-dependent on the direction of measurement. The average crystalline size can be determined from Debye–Scherrer equation,

$$D = \frac{k\lambda}{\beta_D \cos\theta} \tag{4.2}$$

where, D is the crystallite size, λ is the wavelength of Cu Kα (0.15406 nm), K is the shape factor which is a constant (0.9) and θ is peak position. Debye-Scherrer analysis is mainly used to approximate the average crystallite sizes where strain-induced broadening is not considered, while utilization of W-H plot approximates both the crystallite sizes and micro-strains simultaneously.

The other benefit of utilizing the W-H approach over Debye–Scherrer method is that the crystallite sizes of several 2θ positions can be estimated at a time, instead of calculating the crystallite size of a particular position. For deriving the W-H process, the induced micro-strain (ε) contributing to peak broadening can be expressed by equation (4.3)

$$\varepsilon = \frac{\beta_e}{4\tan\theta} \tag{4.3}$$

Replacing and rearranging equations (4.2) and (4.3) into equation (4.1), gives W-H equation (4.4)

$$\beta_T \cos\theta = \frac{k\lambda}{D} + 4\varepsilon \sin\theta \tag{4.4}$$

Thus, the W-H approach has been utilized to approximate both the crystallite sizes and micro-strains of Ho_2O_3 diffraction peaks for the oxidation condition between 800 – 1100 °C as

shown in Figure 4.3. A graph of $\beta_T cos\ \theta$ versus 4 $sin\ \theta$ was plotted based on equation (4.4) from the range of distributed values where two points with the best goodness of fit (r^2 =1) are selected. The ε contribution in Ho_2O_3 peak broadening was calculated from the gradient of the graph, while $K\lambda/D$ is the y-intercept and D can be calculated from this relationship. Based on the W-H analysis, it was observed that the crystallite sizes of Ho_2O_3 increased with oxidation temperature, with the values of the crystallite sizes ranging from 2.83 to 3.84 nm. The crystallite sizes exhibit more similarities between 800 and 900 °C, which could be attributed to the uniform shape of the crystals.

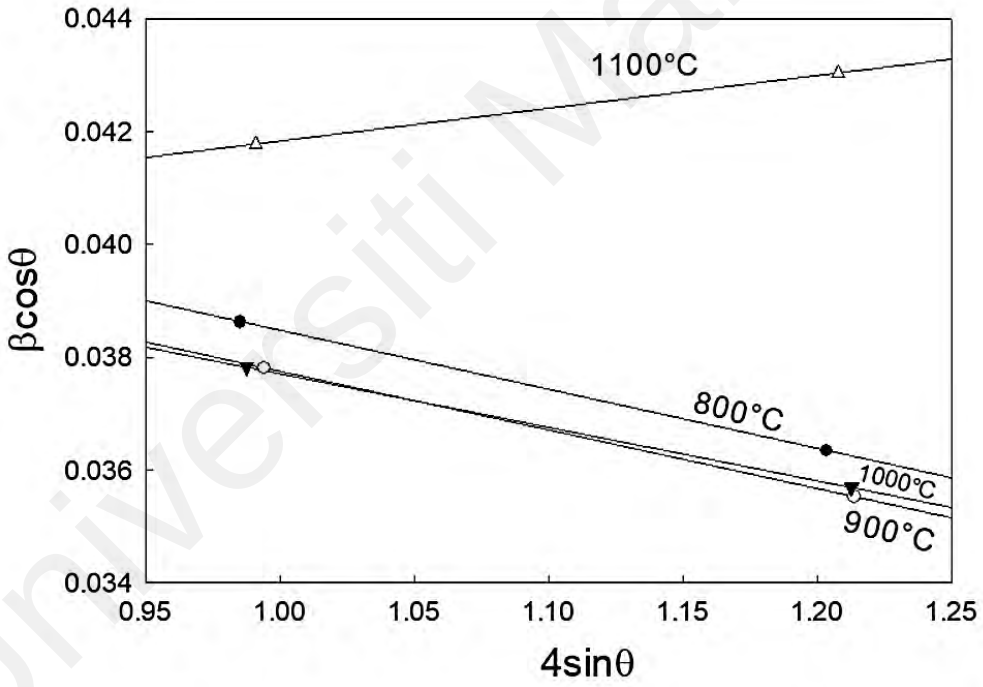


Figure 4.3: W-H plot of Ho_2O_3 for all the oxidized investigated samples.

4.1.1.4 Microstrain Analysis and Crystallites Size

Microstrain is initiated due to the presence of voids, such as spaces or lattice imperfections, excess segment of grain boundaries, and effects of broadening of the XRD peaks (Zak et al., 2011). Therefore, microstrain is a measure of the concentration of defects in the sample. In this case, microstrain was determined indirectly by measuring the defects concentration in the sample, which could be used as a means of correlation between the structural parameters and XRD profile analysis (Zak et al., 2011; Maniammal, Madhu, & Biju, 2017). Figure 4.4 presents the graph of microstrain and crystallite size of Ho_2O_3 at various oxidation temperatures. From the graph, the values of microstrain for 800 °C, 900 °C, 1000 °C, and 1100 °C samples are -0.01046, -0.00987, -0.01037 and 0.00577, respectively. The negative microstrain values obtained at low temperatures are indications of compressive strain, while the positive microstrain value obtained at 1100 °C suggested tensile strain has been induced during this oxidation condition.

The occurrence of tensile strain at 1100 °C was assumed due to excessive diffusion of oxygen atoms from the Ho_2O_3 interface towards the SiC substrate forming SiO_2 and creating O_2 vacancies (Shaaban, Afify, & El-Taher, 2009). Besides, the O atoms interstitial size associated with the vacancies created on the substrate might also be attributed to a positive microstrain. On the contrary, 800, 900, and 1000 °C induced compressive microstrain which is attributed to the more compact structure of the Ho_2O_3, indicating less oxygen vacancies and oxygen interstitials due to minimization of O transportation from the Ho_2O_3 interface. Hence, the minimum compressive strain obtained for 900 °C indicates the least oxygen vacancies and oxygen interstitials within the Ho_2O_3 interface, suggesting a better quality of the Ho_2O_3/SiC interface among all the oxidation conditions. Consequently, the increasing

value of microstrain will contribute to the increase of leakage current by creating more current conduction paths while reduction of microstrain value will aid in improving leakage current.

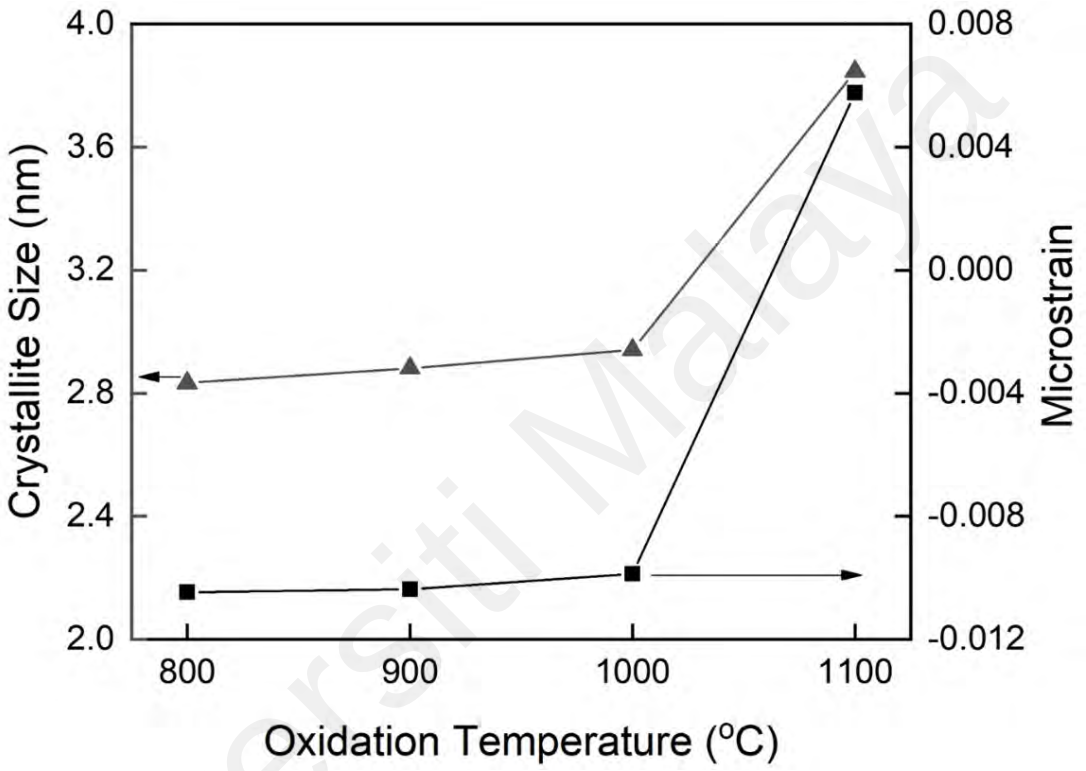


Figure 4.4: Microstrain and crystallites size of Ho_2O_3 at (800 - 1100 °C)

4.1.1.4 Transmission Electron Microscopy (TEM)

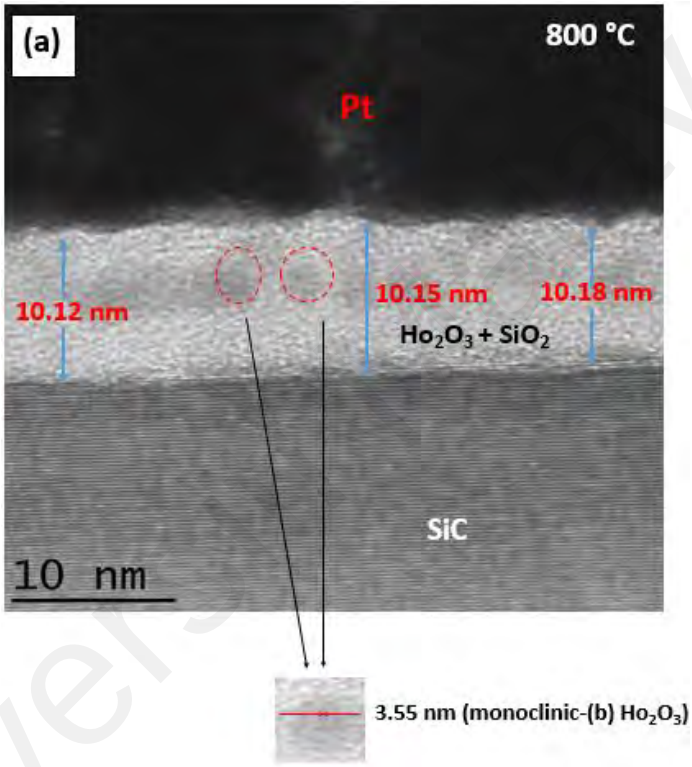
The relationship between oxidation temperature, the thickness of Ho_2O_3 film and the interfacial layer of oxidized samples can be clearly understood through a TEM analysis. This is an important process for the determination of the effect of thickness on the electrical features. In a bid to analyze the Ho_2O_3 films on the SiC substrates, FIB technique was first used to prepare the specimens for the investigation by HRTEM through a hybrid system

comprising of FIB and scanning electron microscope (SEM). During the preparation, platinum coating was deposited on the samples to protect their surfaces from damaging during FIB. The investigation of the cross-sectional area and post-oxidation crystal structure of the Ho_2O_3/SiC interface obtained from HRTEM analysis for 800 and 900 °C samples was shown in Figure 4.5. The images in Figure 4.5 clearly indicate that there are no interfacial layers (IL) detected, but the segment was observed to contain a mixture of both Ho_2O_3 and SiO_2 compounds. The reason for the IL-free may be attributed to the diffusion of SiC substrate into Ho_2O_3 dielectric. The details of the behaviour can be determined by the relative gain between the entropy emerging from the mixture and interfacial energy that are associated with phase separation (Lei et al., 2018).

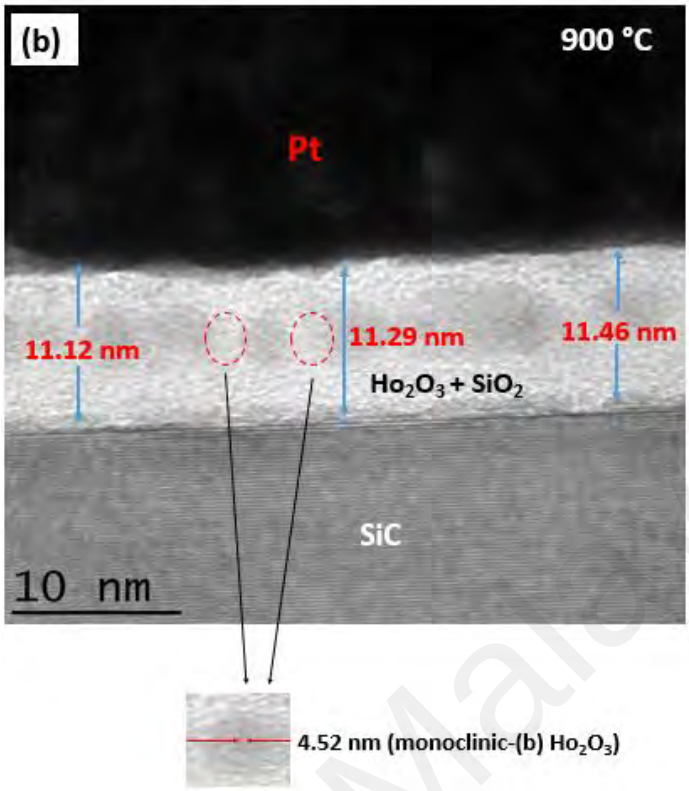
The Ho_2O_3 thin film grown on the SiC substrates displayed amorphous features for both samples, while some crystalline phases were detected at the segment represented by dotted circles on the 800 and 900 °C samples (Figure 4.5 (a) and (b)). Since sharp peaks corresponding to Ho_2O_3 were evident for both samples in the XRD patterns, implying the presence of crystalline phase, hence, the dotted circles are assumed to be monoclinic-(b) Ho_2O_3. The crystal sizes of the samples at both temperatures were measured as 3.55 and 4.52 nm, respectively. Meanwhile, the average thicknesses of the inter-planar segments were measured as 10.15 and 11.29 nm for the 800 and 900 °C, respectively. This finding also agrees with the report of Jeon et al., (2001) and Goh et al., (2016b) that the best electrical results are obtained from the samples that possessed the thinnest layer of interface.

The result of TEM from Figure 4.5 indicates that there is evidence of crystallization of Ho_2O_3 film on the SiC substrate. However, there is no clear evidence of diffusion of carbon into the Ho_2O_3 layer when examined from the XPS that was attached to the TEM equipment.

The thickness of (Ho_2O_3 + SiO_2) film increases when the temperature increased from 800 °C and 900 °C suggesting less oxygen atoms diffusion into the SiC substrate which is consistent with the observation of XPS analysis where SiO_2 integrated area decreased at 900 °C. Figure 4.6 shows the graph of oxidation versus thickness of inter-planar segments.



(a)



(b)

Figure 4.5: TEM images of SiC samples that are Ho-deposited, and oxidized at (a) 800 °C (b) 900 °C

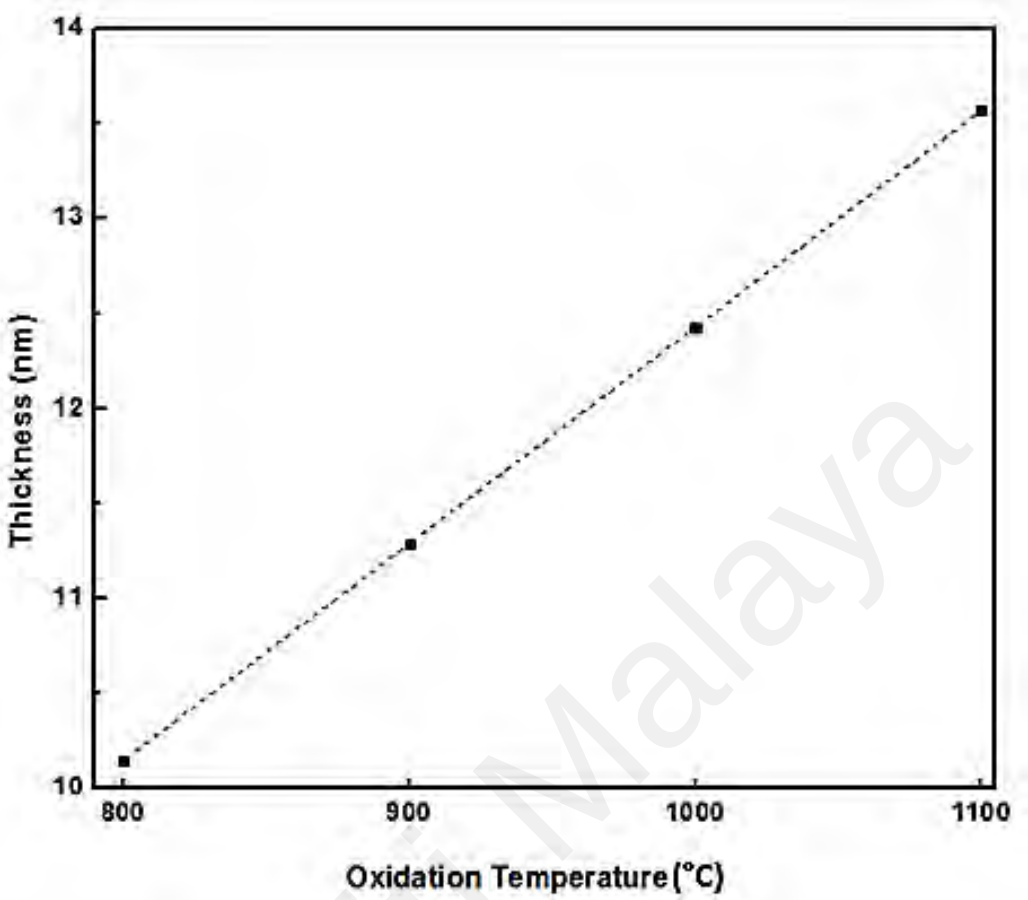


Figure 4.6: Thicknesses of the inter-planar segments of (Ho_2O_3 + SiO_2) thermally oxidized samples

4.1.1.5 Oxidation Mechanism Model

A possible mechanism model of thermal oxidation is proposed here based on the results of XRD, FTIR, XPS, and HRTEM analysis (Figure 4.7). The proposed model is for thermally oxidized samples of Ho_2O_3 on SiC between the temperature range of 800 and 1100 °C (Goh et al., 2016b; Lei et al., 2017; Kageshima, Shiraishi, & Endoh, 2018; Onik, Hawari, Sabri, & Wong, 2021a; C. Yang, Wei, & Wang, 2021). The chemical reaction on the sample is expressed in equation (4.5).

$$2Ho + O_2(g) \rightarrow 2HoO \quad (4.5)$$

At those specified temperatures, the Ho-deposited samples were placed in the furnace, with the application of a controlled volume flow of O_2 gas into the chamber. The samples are thermally oxidized according to the 3-step reactions (Figure 4.8). According to the XPS analysis, the formation of Ho−O indicates less O atom is diffused from Ho_2O_3 into the SiC substrate region which reduced the amount of O atoms during the formation of SiO_2. Ho_2O_3 film was later formed on the SiC surface after the reaction of O_2 gas with the Ho-O as shown in equation (4.6)

$$2Ho_2O + 2O_2(g) \rightarrow 2Ho_2O_3 \quad (4.6)$$

Based on the XRD and FTIR analysis, a characteristic peak of Ho_2O_3 was detected on all the samples. Meanwhile, the HRTEM analysis indicates the presence of monoclinic-(b) Ho_2O_3 crystal structure and IL-free segment in the samples, but, an inter-planar region that comprises of (Ho_2O_3 + SiO_2) film was observed in them.

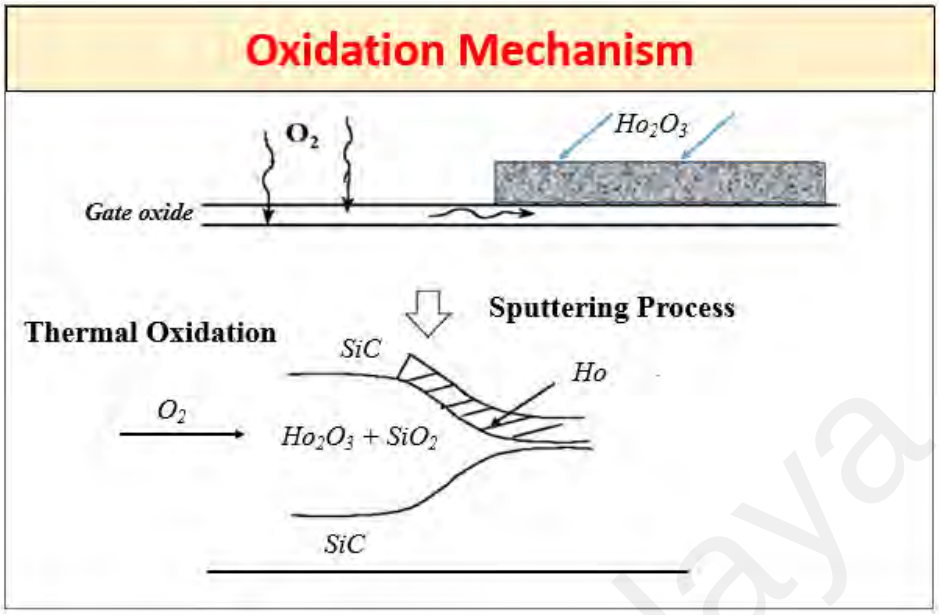
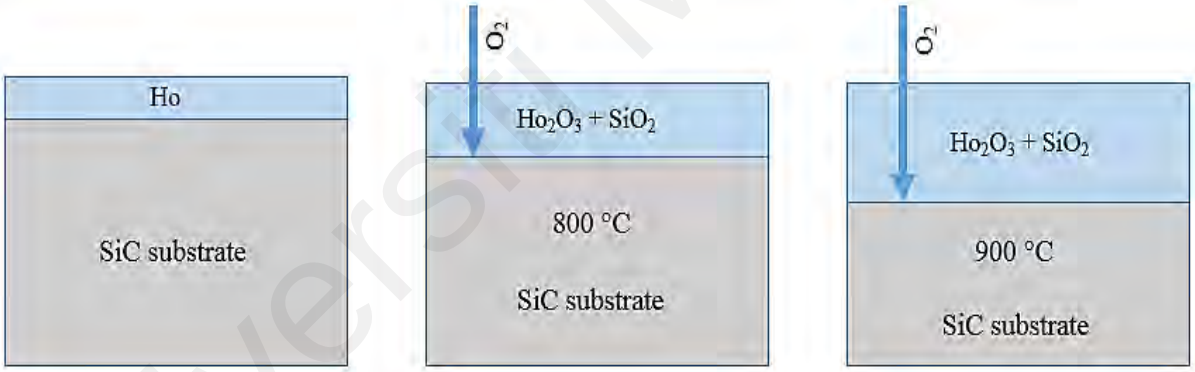


Figure 4.7: Schematic diagram of the oxidation mechanism.



(a) (b) (c)

Figure 4.8: Schematic representation of the oxidation mechanism model (a) Sputtered Ho on SiC substrate, (b) thermal oxidation of samples at 800 °C to form Ho_2O_3 + SiO_2, and (c) thermal oxidation of sample at 900 °C to form Ho_2O_3 + SiO_2.

4.1.1.6 X-Ray Photo-Electron Spectroscopy (XPS)

XPS is employed to determine the quality of the gate oxide, its bandgap and band offsets. Its spectra reveal the interactions between SiC and Ho_2O_3 thin film. The peaks at

different binding energies were calibrated using C1s of 284.6 eV in accordance with C element of the composition (Figure 4.9) (L. Liu, Tang, Huang, Xu, & Lai, 2019).

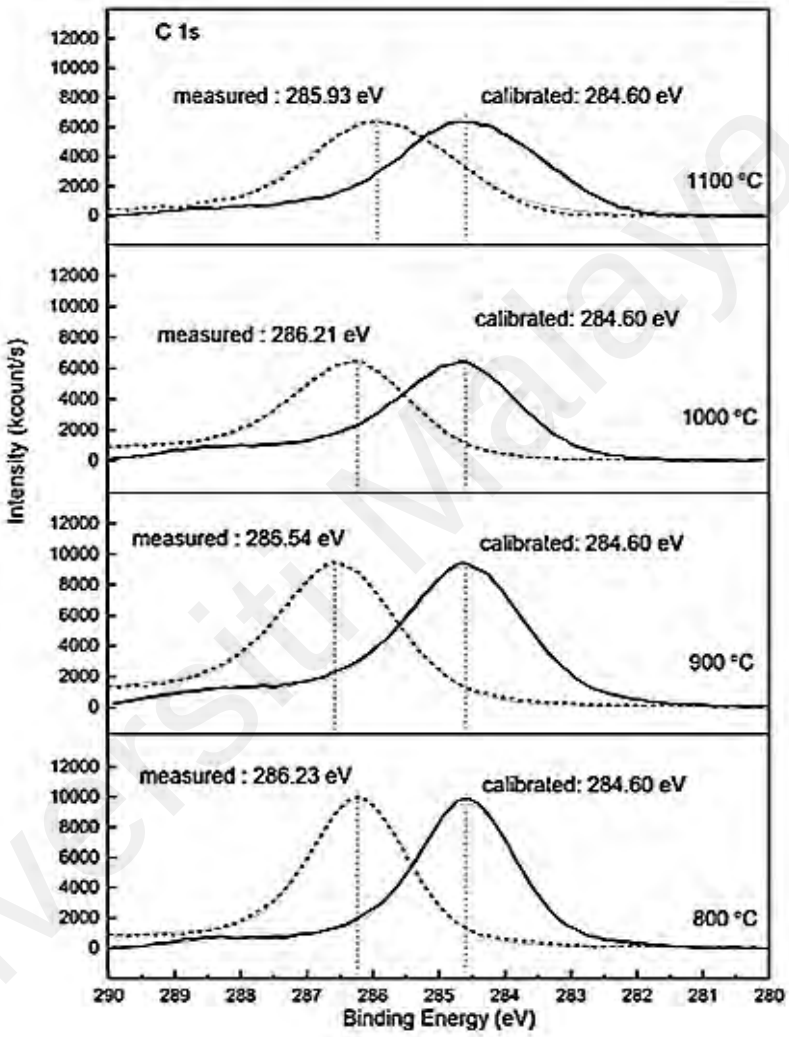


Figure 4.9: XPS spectra of C1s core level for various thermally oxidized samples: 800 – 1100 °C

The formation of Si−O and Ho−O were noticed in the O1s region through the photoelectron spectrum having two constituents of binding energies each at 532 and 531.5 eV, 531.8 and

530.5 eV, 532 and 533 eV, 533 and 531.3 eV at 800, 900, 1000 and 1100 °C respectively (Figure 4.10). The first part is allocated to the O_2 that joined two Si atoms to form Si−O bonding while the second part was assigned to O atoms bonding configurations that were chemically absorbed during Ho−O formation (Pan et al., 2010; Pan & Huang, 2011).

From the O1s spectra, the 800 °C samples displayed the highest Ho_2O_3 in terms of integrated peak area which decreased at increasing oxidation temperature. The increase of Ho−O content suggests less O atoms diffused from Ho_2O_3 into the SiC substrate region which decreased the amount of O atoms incorporated during SiO_2 formation at this temperature. Similar justification can also be applied for 900 °C which showed increasing oxygen content in Ho−O configuration when compared with 1000 and 1100 °C. The 1100 °C samples recorded the lowest peak area of Ho_2O_3. This indicates that the samples at that temperature exhibited higher exaggeration of oxygen diffusion, creating oxygen vacancies that led to sub-stoichiometric atomic bonding of Ho_2O_3 and the formation of more SiO_2. Since the presence of more O transportation during Si−O formation is displayed at the 1000 and 1100 °C samples, it confirms that, apart from the O_2 gas that is absorbed from the ambient, the additional O atoms circulated from Ho_2O_3 at these temperatures which accelerated the growth of SiO_2. This observation is also complimentary with the XRD pattern where the SiO_2 increased for 1000 and 1100 °C.

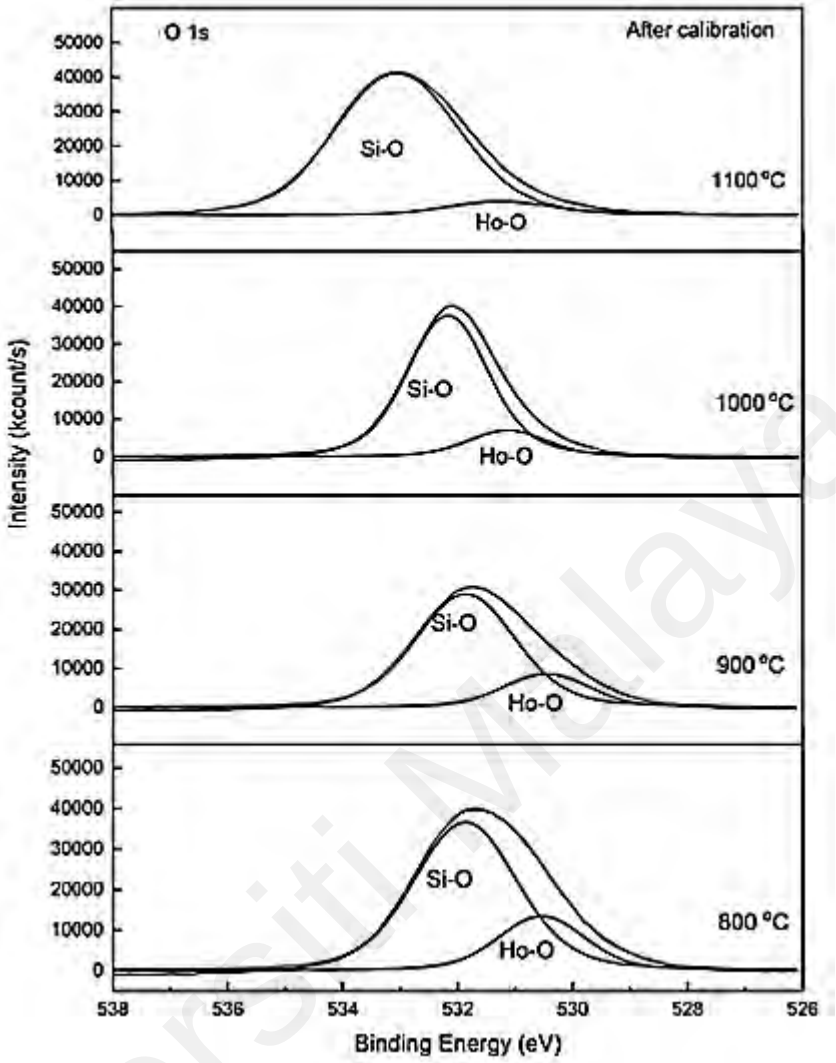


Figure 4.10: XPS spectra of O1s core level for various thermally oxidized samples: 800 – 1100 °C

The narrow scan of Ho 4d for samples that were oxidized at different temperatures from 800 to 1100 °C is shown in Figure 4.11. The positions of peak at binding energy that belongs to Ho 4d in 800, 900, 1000, and 1100 °C samples are 161.39, 160.71, 160.53 and 160.69 eV, respectively (Wiktorczyk & Nitsch, 2001; Abu-Zied & Asiri, 2019; An, Dou, Ju, Wei, & Ji, 2019). Except for the 800 °C samples, it was observed that the binding energy decreased with an increase in thermal oxidation. The decrease of Ho 4d binding energy is an indication of O

diffusion from Ho_2O_3 while increase of binding energy indicates a reduction of O diffusion which preserved a more compact Ho_2O_3 structure. Accordingly, it can be predicted that the growth of Ho_2O_3 will record its highest at 800 °C. The validation of this assumption was explained in the O1s spectra in terms of migration of less O atoms. Based on observation from the Ho 4d spectra, it can be deduced that the growth of Ho_2O_3 is essentially a relationship between Ho and O atoms that dispersed from the interface.

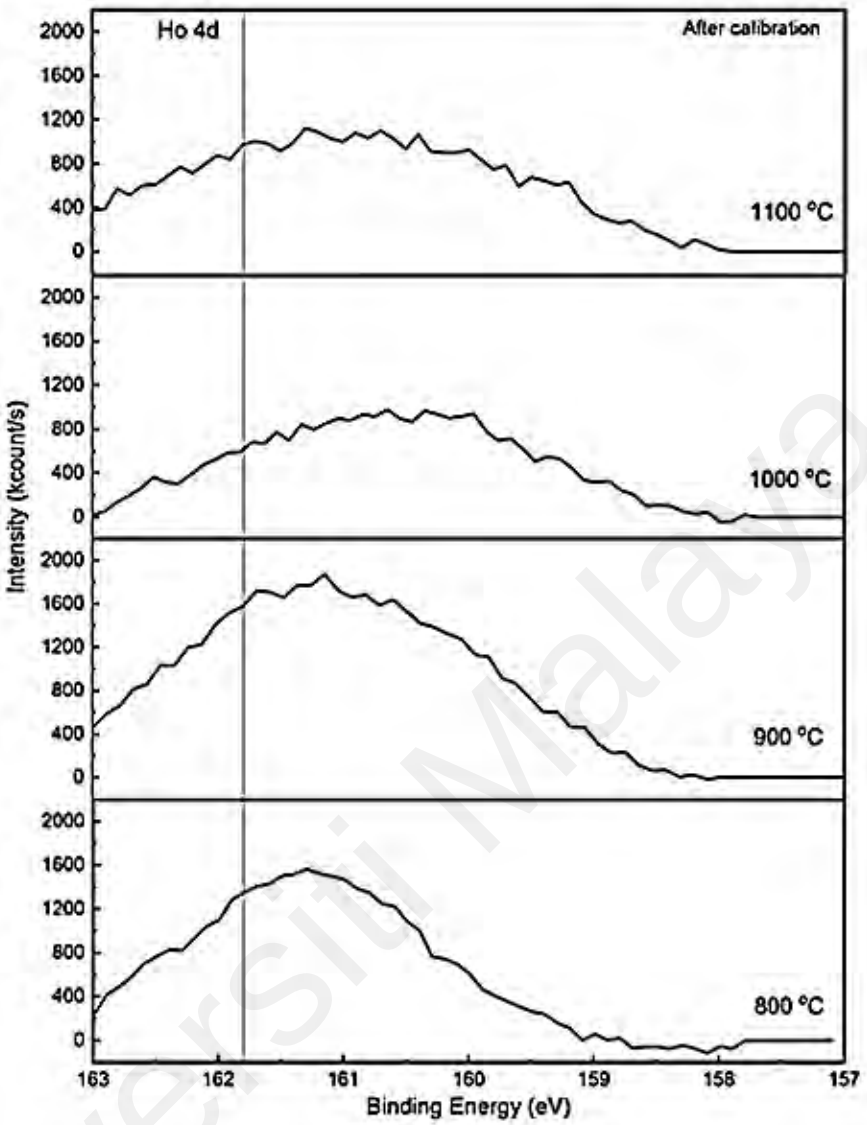


Figure 4.11: XPS spectra of Ho 4d core level for various thermally oxidized samples: 800 – 1100 °C

Figure 4.12 presents the Si 2p region of the samples, it indicates components of SiO_2 at 103, 102.8, 102.7 and 102.92 eV (Platonov, Rumyantseva, Frolov, Yapryntsev, & Gaskov, 2019). From past literature, SiO_2 was found in the range of (101 - 105) eV (Hirose, Sakano, Takahashi, & Hattori, 2002). Comparing the integrated area of SiO_2 using Si 2p spectrums in Figure 4.12, it can be observed that, there is an increase in activation energy of Si which intensified SiO_2 for 800 and 1100 °C oxidation conditions, while the intensities of SiO_2

recorded at 900 and 1000 °C decreases, indicating less incorporation of Si from SiC substrate. It is obvious that the extent of forming SiO_2 is associated with the activation energy of Si and O diffusion from the Ho_2O_3 interface. In summary, it can be inferred that the oxidation condition of 800, 1000 and 1100 °C increases the activation energy of Si, diffusion rate of O atoms and induced more SiO_2 and less Ho_2O_3 when compared to the oxidation condition of 900 °C. The reduction of SiO_2 and increase in the Ho_2O_3 compound are expected to improve the electrical performance of the gate stack.

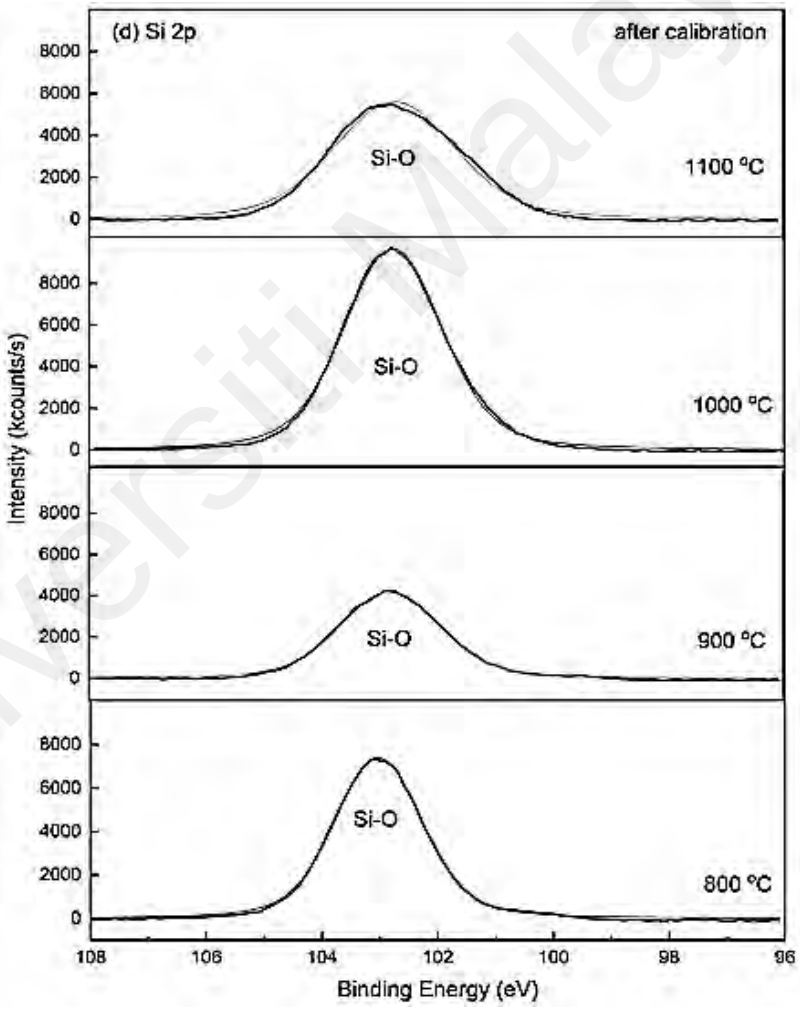


Figure 4.12: XPS spectra of Si 2p core level for various thermally oxidized samples: 800 – 1100 °C

4.1.2 Electrical Characterization

4.1.2.1 J–E Features

The current-voltage (I-V) data was acquired using a semiconductor parameter analyzer (Keithley 4200 semi-conductor parameter analyzer). The data was later analyzed and represented by leakage current density–breakdown field (J–E) as displayed in Figure 4.13. The value of E is gotten from,

$$E = \frac{V_g - V_{fb}}{t_{ox}} \tag{4.7}$$

where V_g represents the gate voltage, flat band voltage and the oxide thickness are represented by V_{fb} and t_{ox}, respectively. The results of the I–V data were later converted to a J–E plot. The explanation of charge-trapping and the tunneling i.e. passage device for the conduction of the primary gate leakage current are done through the J–E features. Also, the performance of the device is influenced by densities of interface defect and oxide variation due to irradiation of gamma (Manikanthababu et al., 2020). Single step breakdowns were experienced by all the oxidized samples between 800 and 1100 °C.

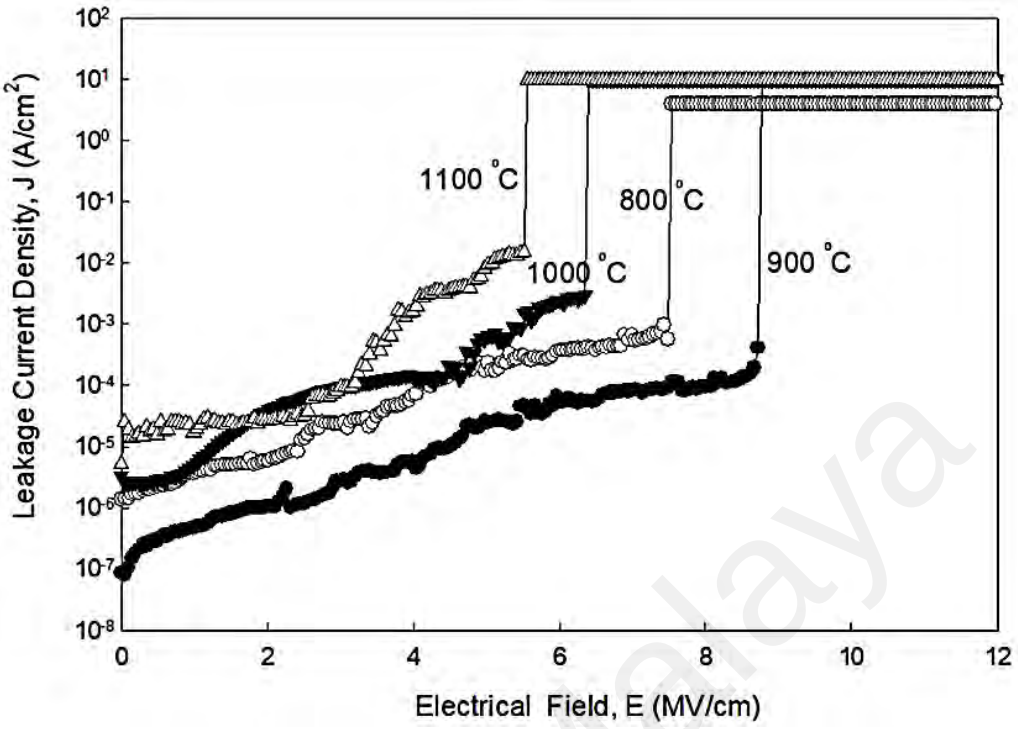


Figure 4.13: J–E plot of samples oxidized at different temperatures from (800 – 1100 ˚C).

Generally, the lower breakdown fields obtained at the initial point are known as soft breakdown, while the ones obtained afterwards, at higher levels are regarded as hard breakdown. For the best sample to be determined by its electrical properties, it is required of such sample to possess a low current leakage density and high electric field voltage. Therefore; from the analysis of this research, the oxidized sample of 900 °C displays the best electrical results, with an E and J values of 8.95 MV/cm and 4.32×10^{-3} A/cm^2, respectively. More so, the breakdown field attained in this experiment is relatively higher than many of those of the previous studies as shown in Table 4.1, this may be ascribed to variation of the film thickness and fabrication process.

Table 4.1: Summary of the various gate oxides with their leakage current density and breakdown field.

S/N	Gate Oxide	Leakage Current Density (A/cm^2)	Breakdown Field (MV/cm)	Ref.
1	Sm_2O_3	1×10^{-8}	0.6	(Goh et al., 2016b)
2	N_2O_3	2.019×10^{-6}	5.26	(Hetherin et al., 2017a)
3	ZrO_3	1×10^{-6}	16.6	(Lei et al., 2017)
4	HfO_2	1×10^{-2}	1×10^{-6}	(Golosov, Vilya, Zavadski, Melnikov, & Komissarov, 2019)
5	Al_2O_3	$2.7\,6 \times 10^{-10}$	11.8	(P. Chang & Hwu, 2018)
6	TiO_2	8.4×10^{-8}	2×10^{-6}	(Dang et al., 2014)
7	Ta_2O_5	1×10^{-8}	3	(Cheng, Sang, Liao, Liu, & Koide, 2012)
8	SiO_2	1×10^{-7}	1	(Esro, Kolosov, Jones, Milne, & Adamopoulos, 2017)
9	Y_2O_3	1×10^{-6}	6.6	(Quah & Cheong, 2013)
10	Ho_2O_3	4.32×10^{-3}	8.95	This work

Meanwhile, a large breakdown electric field, (E) in the dielectric layer of the Ho_2O_3/SiC arrangement was developed. The holes that pass through the Ho_2O_3 gate oxide will gain more kinetic energy under such a large breakdown voltage, and some electrons in the valence band of the gate oxide will be excited. Therefore, the sample oxidized at 900 ºC is observed to have better electrical results due to a lower density of leakage current. This can be as a result of the absence of an interfacial layer. This also conforms with Jeon et al. in their report on the selection of the best electrical data (Jeon et al., 2001). Moreover, the reliability feature of SiC-based MOSFETs is destroyed by a high density of leakage current as a result of low conduction band offset at the interfacial layer of SiO_2/SiC. Hence, conventional SiO_2 will be substituted with high-κ gate oxide to diminish the breakdown voltage across the dielectric insulator under a similar equivalent oxide thickness (Cheng, Sang, Liao, Liu, & Koide, 2012).

4.1.2.2 Fowler–Nordheim (F-N) Tunneling

The F-N tunneling model is used to describe the flow of electrons in a conduction band through a triangular potential barrier of a dielectric material. An F–N tunneling linear regression graph is shown in Figure 4.14, where ln (J/E^2) was plotted against 1/E. The Φ_B was then calculated based on this plot and its relevant equations.

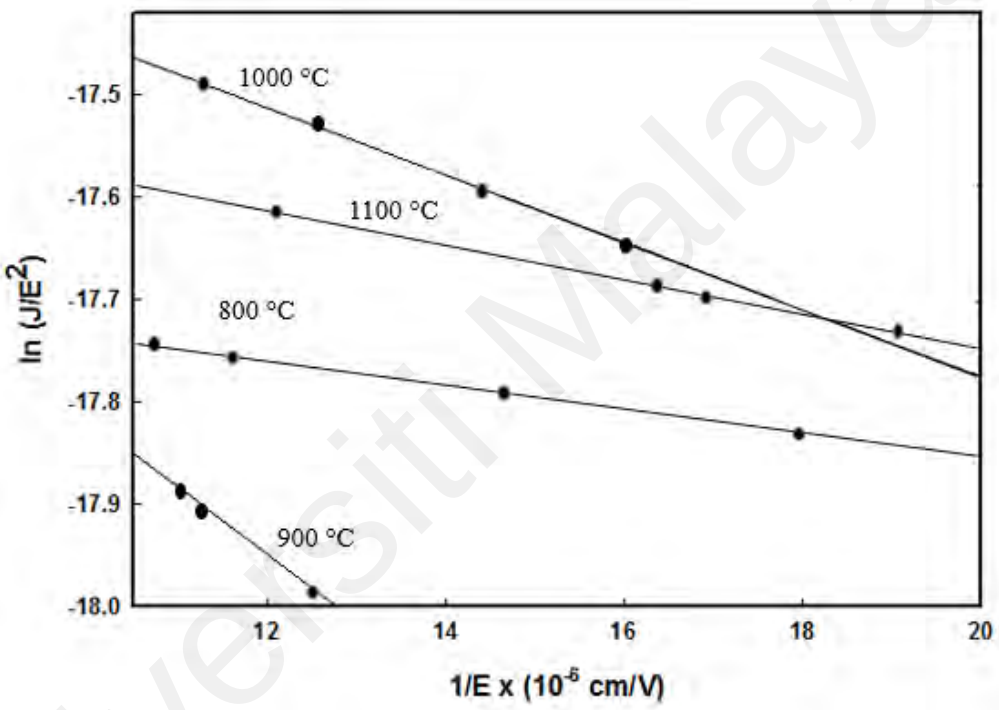


Figure 4.14: F-N tunneling linear regression plot of the oxidized samples at different temperatures, (800 – 1100 ˚C).

4.1.2.3 Barrier Height

The barrier height, Φ_B between conduction band edge of the substrate and the gate oxide was derived from the F–N tunneling regression plot in form of linearized model of ln (J/E^2) versus1/E plot (Forbes, 1999a, 1999b; Chiou, Gambino, & Mohammad, 2001; Forbes & Deane, 2007). Generally, both F–N and direct tunneling are the main paths for conduction

and injection of electron through the gate oxide from the SiC substrate (Hetherin et al., 2017a). The result of barrier height is shown in Figure 4.15. The sample with the highest Φ_B shows the best electrical results at 900 ˚C oxidation temperature, with a barrier height value of 9.82 eV.

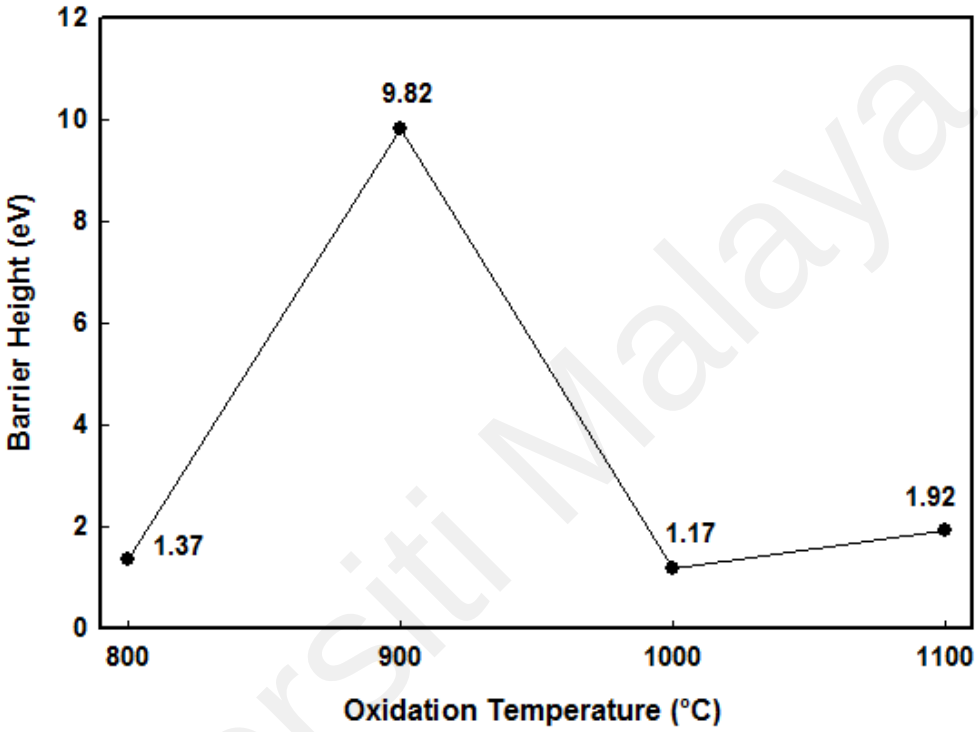


Figure 4.15: Barrier height of the samples at different temperatures, from (800 – 1100 ˚C).

4.2 Effects of Oxidation Duration on the Physical and Electrical Properties of Ho_2O_3 on SiC Substrate

4.2.1 Physical Characterization

4.2.1.1 X-Ray Diffraction (XRD)

The crystal structure and orientation of the oxidized samples were examined with XRD. The XRD patterns at various durations are presented in Figure 4.16. For the 5, 10, 15, and 20

min samples, six peaks that were identified as monoclinic-(b) Ho_2O_3 (111), Ho_2O_3 (190), Ho_2O_3 (440), Ho_2O_3 (620), Ho_2O_3 (622) and Ho_2O_3 (640) were observed at peaks corresponding to 28.73°, 42.95°, 47.89°, 48.24°, 53.76° and 76.40° respectively. Inorganic Crystal Structure Database (ICSD) with the reference codes 160229 was used to match the peaks. The hexagonal SiO_2 (201), SiO_2 (311), and cubic SiO_2 (003), SiO_2 (351), were found at 27.17°, 29.471°, 35.27° and 38.69°, respectively in the samples at all the durations. These peaks correspond to reference code 170522 and 170494 of the ICSD. According to the XRD results, the peaks at 28.73° and 35.27° were observed to increase in intensity with characteristic peaks as the oxidation period of the samples increased from 5 to 20 min. The identification of SiO_2 in the results implies that thermal oxidation could add to the dispersal of oxygen through the Ho_2O_3 layer that reacted with SiC to form crystalized SiO_2 (Hetherin et al., 2017b). The highest intensity of Ho_2O_3 was observed in the 15 min sample while the lowest was recorded at 20 min duration. In a similar manner, the sample oxidized for a duration of 20 min also possess the highest intensity, while the 5 min sample recorded the lowest intensity of SiO_2. Since the degree of crystallinity can be attributed to an increase in intensity, it can be deduced that the increase in oxidation duration between the 5 and 20 min enhanced the crystallinity of the Ho_2O_3 gate oxide (Onik et al., 2021a).

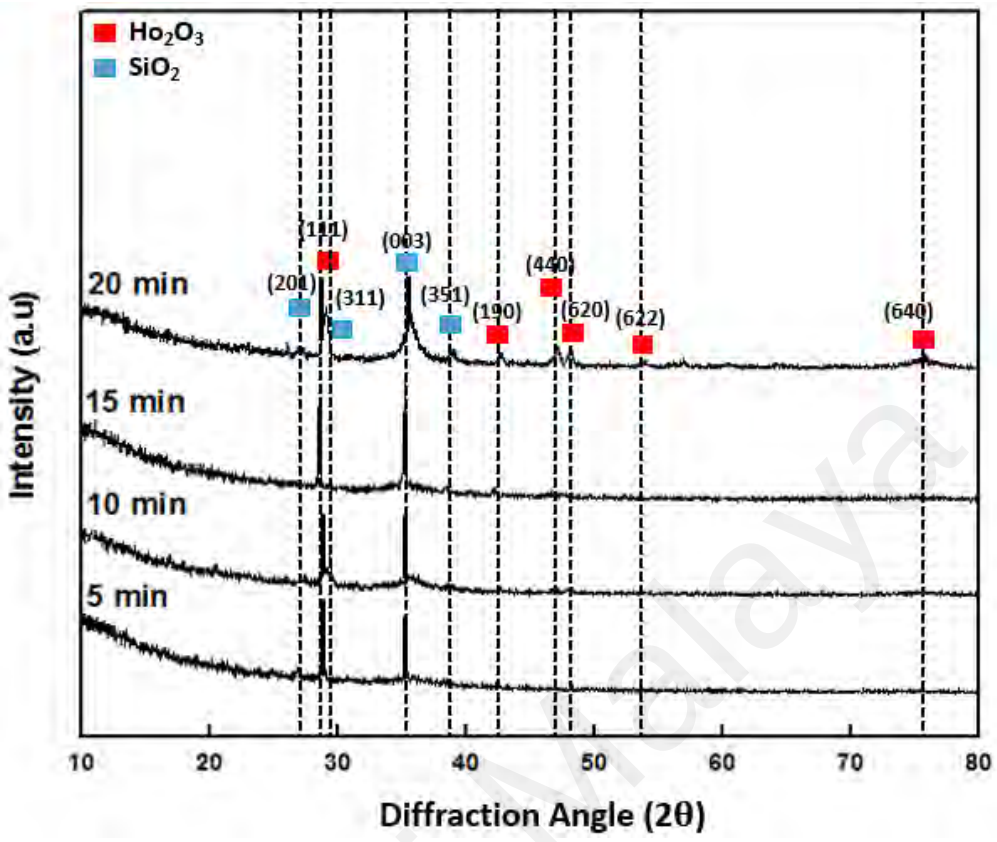


Figure 4.16: XRD patterns of oxidized samples of SiC/Ho_2O_3 at different durations.

4.2.1.2 W-H Plot Analysis

Williamson–Hall (W–H) plot was employed to evaluate the microstrain (ε) and the crystallite size (D) of the crystals that were detected through XRD. In this study, peak broadening of XRD patterns was used to examine the impact of different oxidation duration on the crystallinity of gate oxide due to dislocation and crystal defects (Goh et al., 2016a). Debye-Scherrer analysis was employed mainly for approximation of the crystallite sizes, while W-H plot was used to estimate both the crystallite sizes and microstrains, simultaneously. By applying the Scherrer equation (Goh et al., 2016a & 2016b), the crystallite sizes of the Ho_2O_3 at different peak points for the 5, 10, 15 and 20 min samples were determined.

Figure 4.17 presents the graph of $\beta_T \cos \theta$ against 4 $\sin \theta$ based on the Scherrer equation, meanwhile, the analysis was done according to W-H plot (Mote et al., 2011; Zak et al., 2011). The intercept of the graph, from which the crystallite size and the slope of the line which signifies the microstrain, ε were all determined. From the graph, two points with the best goodness of fit (r^2=1) were chosen from the distributed values, the crystallite sizes obtained are in the range of 0.5572 and 1.3952 nm.

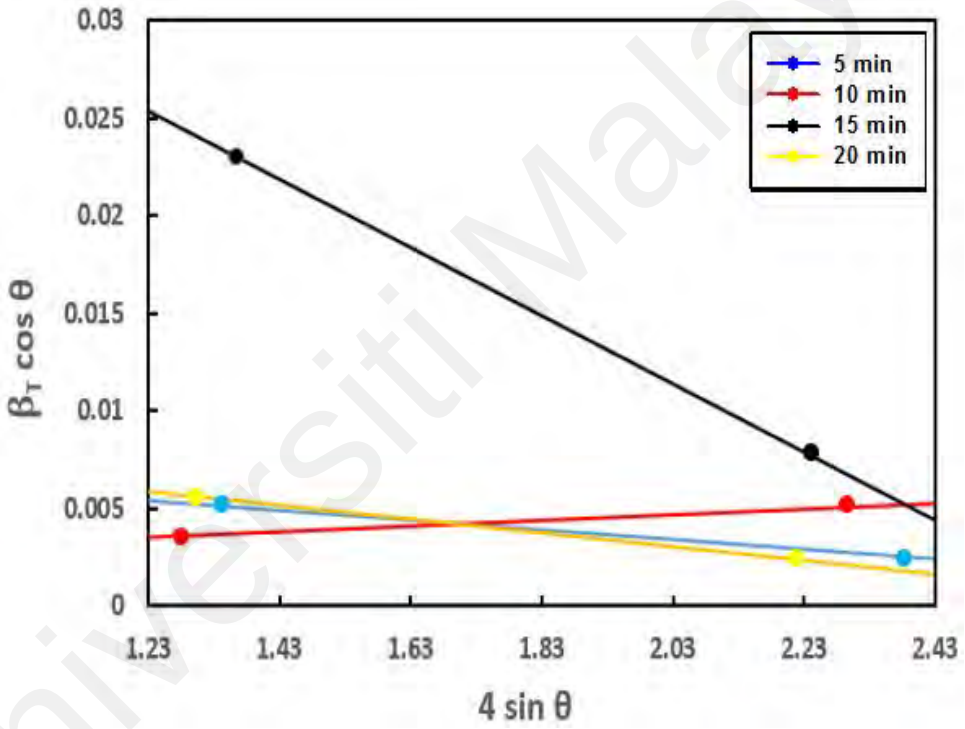


Figure 4.17: W-H plot of thermally oxidized samples of SiC/Ho_2O_3 at different oxidation durations.

4.2.1.3 Microstrain Analysis and Crystallites Size

The relationship between microstrain and the structure of grain boundary of a semiconductor material is a very important factor as it affects the electrical conductivity of

that material. The grain size is therefore largely dependent on the microstrain and the oxidation period of the structure. Figure 4.18 shows the graph of microstrain versus oxidation duration. The microstrain value of Ho_2O_3 increased from 0.0064 to 0.03944 with an increase in oxidation period from 5 to 15 min but later decreased to 0.0099 when the duration was extended to 20 min. In addition, the samples that were oxidized at 5 and 15 min exhibit the lowest and the highest microstrain values, respectively. It was observed that the microstrain of SiO_2 follows a similar trend with values of 0.0032, 0.0046, 0.0208 and 0.0044 at oxidation period of 5, 10, 15 and 20 min, respectively. The lowest and the highest values obtained are 0.0032 and 0.0208 at oxidation duration of 5 and 15 min, respectively. Meanwhile, the lowest and the highest microstrain values were recorded at these durations for both Ho_2O_3 and SiO_2.

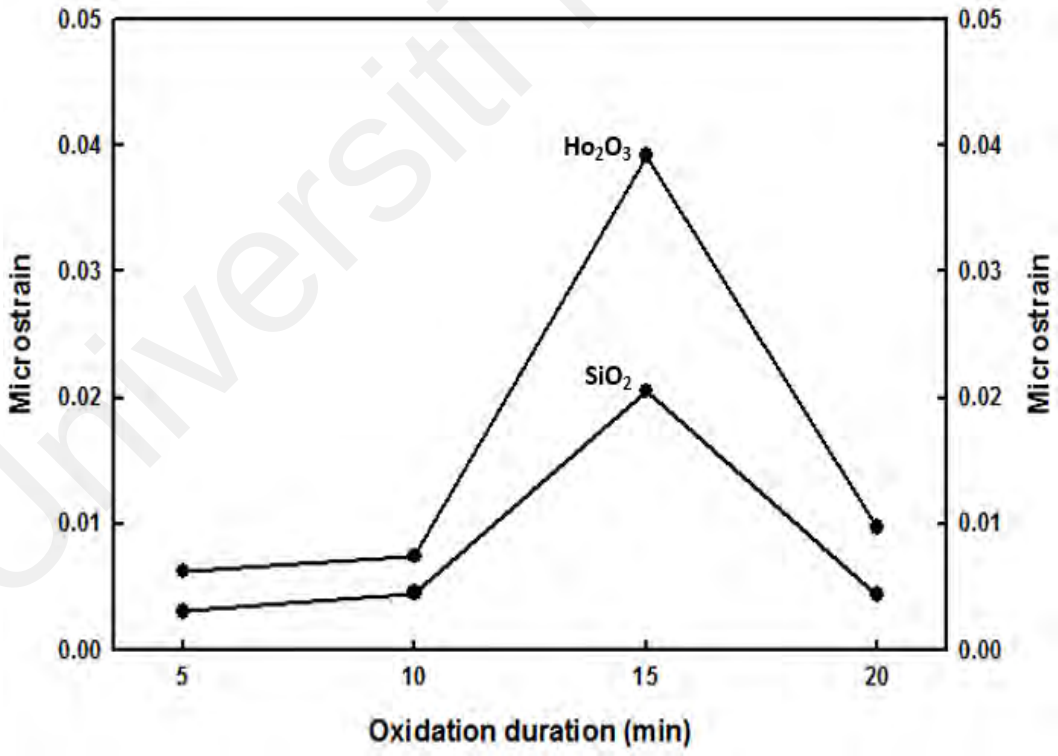


Figure 4.18: Microstrain of samples of SiC/Ho_2O_3 oxidized at different oxidation durations.

The crystallite sizes of Ho_2O_3 and SiO_2 obtained from W-H plot are presented in Figure 4.19. From the figure, the crystallite sizes of Ho_2O_3 samples for oxidation duration of 5, 10, 15 and 20 min are 1.3952, 0.9618, 0.5572, and 0.9238 nm, respectively. The crystallite sizes of SiO_2 were obtained as 0.6761, 0.5334, 0.2189 and 0.6144 nm, respectively at the stated period of thermal oxidation. It was observed that, the crystallite size of SiO_2 shows some closeness in value between oxidation periods of 5 and 10 min, with little differences that could be attributed to evenly distributed crystallites at these oxidation periods (Goh et al., 2016b; Onik, Hawari, Sabri, & Wong, 2021b).

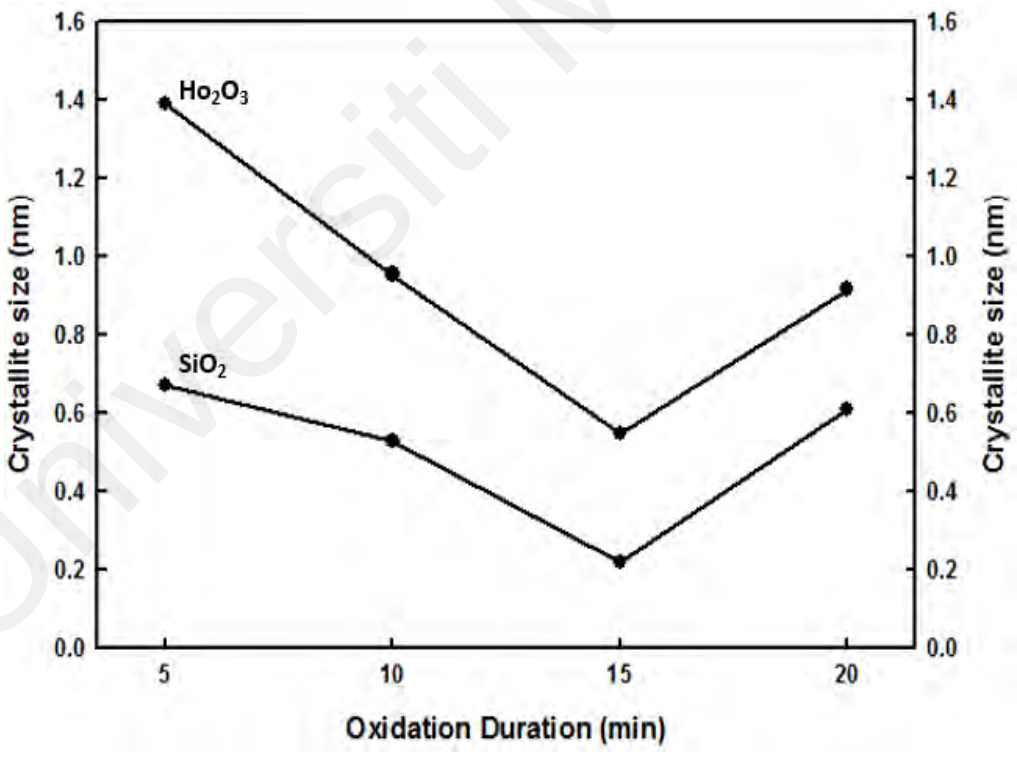


Figure 4.19: Crystallites size of samples of SiC/Ho_2O_3 oxidized at different oxidation durations.

4.2.1.4 Fourier Transform Infra-Red (FTIR)

FTIR was performed to examine the chemical working atoms in the samples (Goh et al., 2016a; de la Rosa et al., 2020). Figure 4.20 presents the FTIR spectra of thermally oxidized samples at different durations of oxidation with a scan range of 400 up to 1400 cm^{-1}. The presence of Ho_2O_3 and SiO_2 were observed in all the oxidized samples between the duration of 5 and 20 min. This finding is in alignment with the results of XRD analysis (section 4.2.1.1), and J-E results which are discussed later in the thesis (section 4.2.2.1). A sharp peak of Ho_2O_3 at 950 cm^{-1} was detected in the 5, 10, 15, and 20 min samples. In a similar manner, the peaks of SiO_2 were detected at 809 and 902 cm^{-1} (Nagai & Hashimoto, 2001; de Urquijo-Ventura et al., 2020) in all the samples. Finally, a sharp peak was obtained when the oxidation time was 5 min, and as the duration was extended from 5 to 10 min, the sharpness decreased. The intensity later increased at 15 min.

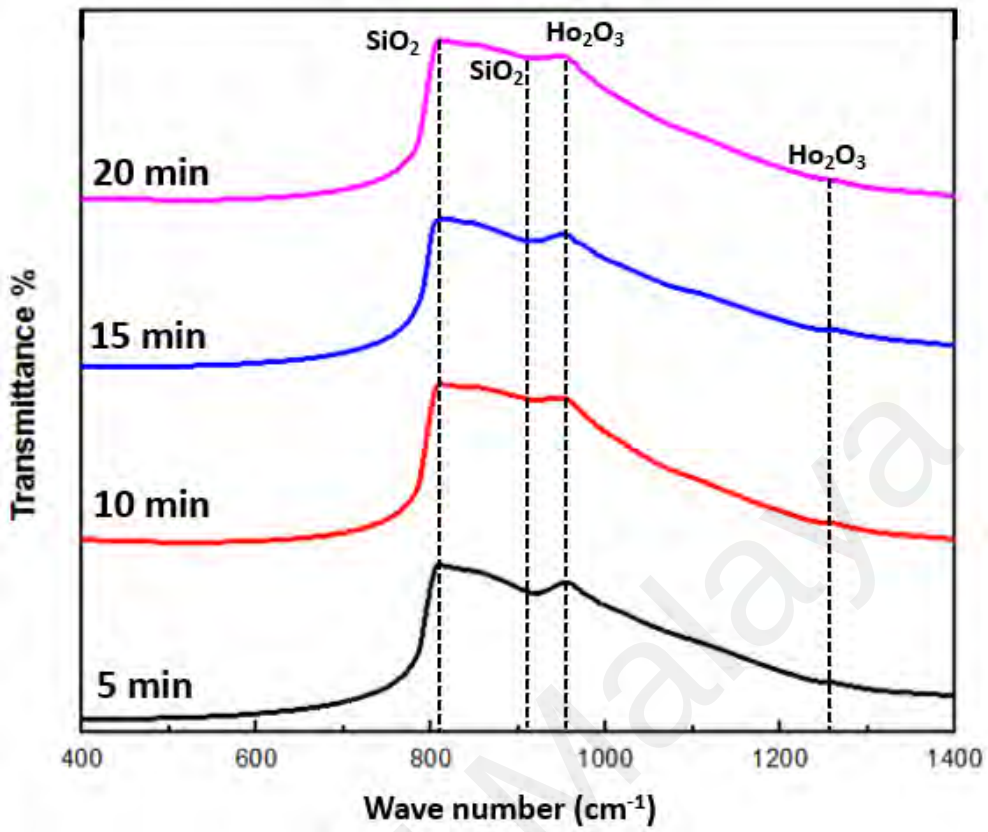


Figure 4.20: FTIR spectra for Ho deposited on SiC substrate at various oxidation durations.

4.2.1.5 High Resolution Transmission Electron Microscopy (HRTEM)

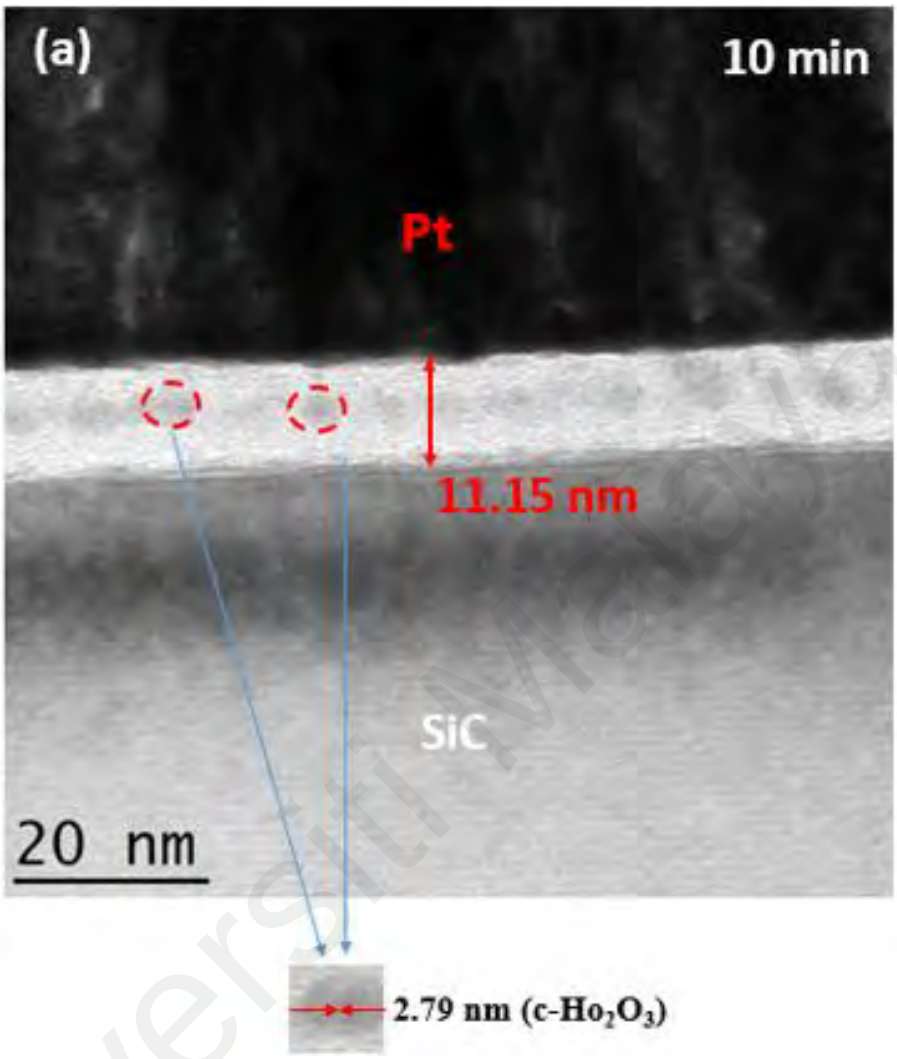
In this study, HRTEM analysis was performed to determine the structural details, the growth, and the quality of the oxide layer of the Ho_2O_3/SiC structure. The Ho_2O_3 thin films grown on the SiC substrates display crystallized monoclinic (b)-phased Ho_2O_3 as shown by the XRD spectra (section 4.2.1.1). Further investigation of the cross-sectional area of the Ho_2O_3/SiC samples by TEM revealed its post-oxidation crystal structure, as shown in Figure 4.21.

The inter-planar spacing of the crystals between the Ho_2O_3 thin film and the SiC substrate was observed. There is an indication that there are no interfacial layers (IL)

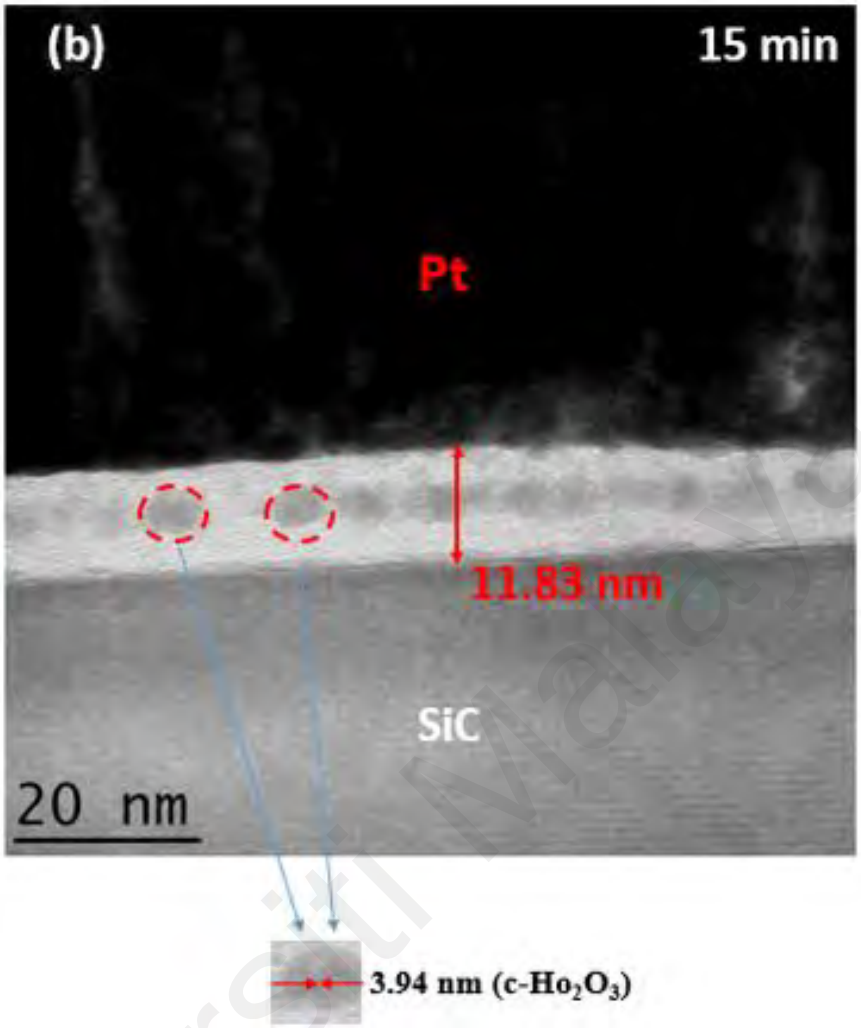
detected, but the segment was observed to contain a mixture of Ho_2O_3 and SiO_2 compounds. The reason for the free IL may be attributed to the diffusion of SiC substrate into Ho_2O_3 dielectric. The details of the behaviour can be obtained by the relative gain between the entropy emerging from the mixture and interfacial energy that are related to phase separation (Lei et al., 2018). The samples that were chosen for HRTEM analysis were selected based on the results of their electrical characteristics, i.e. the samples with the lowest leakage current density. According to the HRTEM analysis, some crystals of Ho_2O_3 were detected at the segment which are represented by dotted circles on the 10 and 15 min samples (Figure 4.21 (a) & (b)).

The crystal sizes of the samples at both temperatures were measured as 2.79 and 3.94 nm, respectively. Meanwhile, the thickness of the inter-planar segment was measured as 11.15 and 11.83 nm respectively. This finding is also in alignment with the report of (Jeon et al., 2001) and (Goh et al., 2016b) that the best electrical results are obtained from the samples that possessed the thinnest inter-planar segment. The result of TEM from the figure indicates that there is evidence of crystallization of Ho_2O_3 film on the SiC substrate. Also, there is no clear evidence of diffusion of carbon into the Ho_2O_3 layer when examined from the XPS that was attached to the TEM equipment.

In order to establish a correlation between the oxidation thickness and the time, a linear regression line is presented in Figure 4.22. According to (Sahari, Ohta, Matsui, Mishima, & Miyazaki, 2013), it was assumed that both the thickness and time are linearly related. Therefore; from the figure, the oxidation thickness of Ho thin films was obtained in the range of approximately 10.5 to 12.5 nm at oxidation duration between 5 and 20 min, respectively. Based on the HRTEM results, there is every indication that the increase in the oxidation time may result in an increase in oxidation time.



(a)



(b)

Figure 4.21: TEM image of SiC samples that are Ho-deposited at oxidation duration of (a) 10 min (b) 15 min.

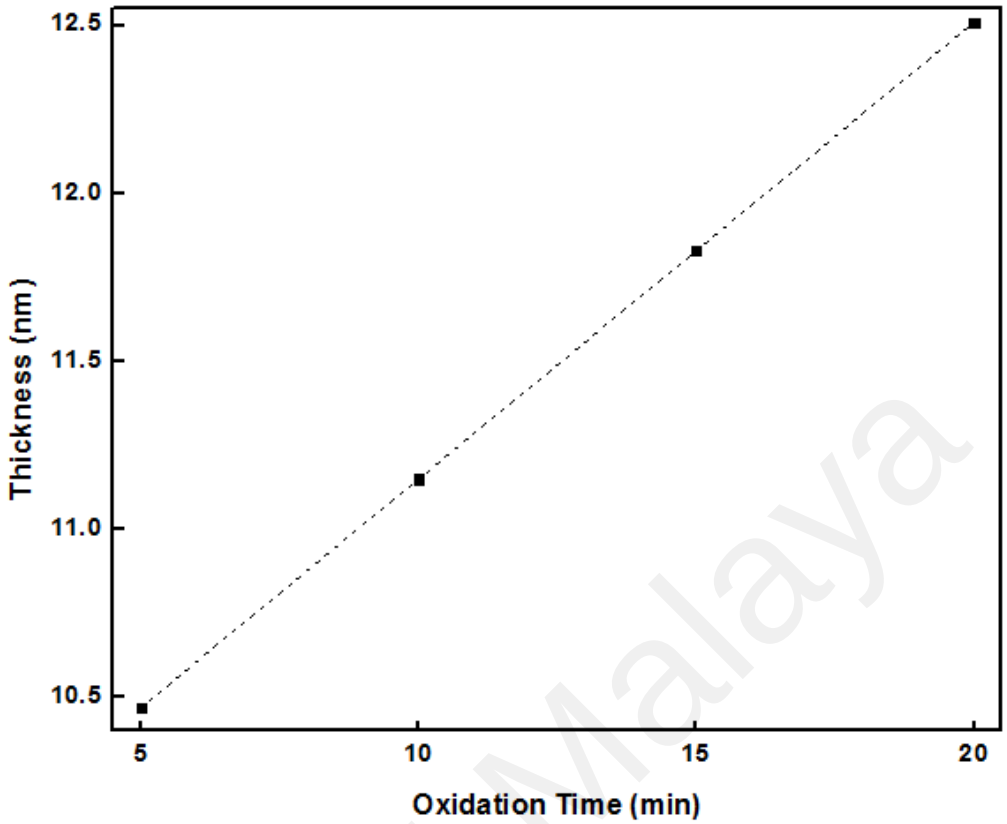


Figure 4.22: Thickness versus oxidation time of thermally oxidized samples, from 5 – 20 min.

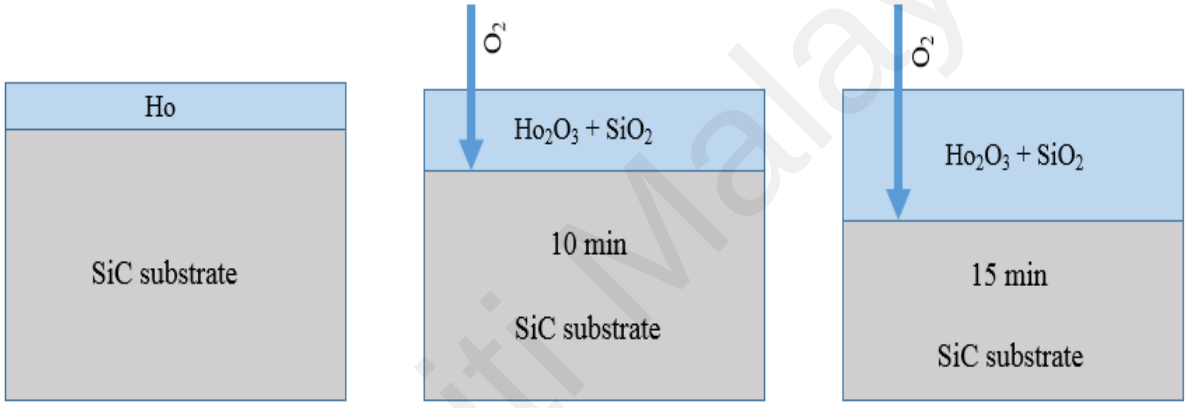
4.2.1.6 Thermal Oxidation Mechanism

Figure 4.23 presents the schematic representation of the oxidation mechanism of the formation of Ho_2O_3 on SiC at different periods of thermal oxidation. The samples, which were thermally oxidized at 5, 10, 15 and 20 min durations reacted with Ho films that were earlier deposited by sputtering process according to equations (4.8) and (4.9). The chemical reaction on the sample is shown below

$$2Ho + O_2(g) \rightarrow 2HoO \quad (4.8)$$

$$2Ho_2O + 2O_2(g) \rightarrow 2Ho_2O_3 \quad (4.9)$$

The samples are thermally oxidized according to the 3-step reactions. According to the XRD analysis, the O_2 is diffused from Ho_2O_3 to react with the SiC substrate. The microstrain values were observed to be positive, with their crystallite sizes significantly larger than the 20 min sample. From the HRTEM analysis, the thickness of the inter-planar was measured as 11.15 and 11.83 nm for the 10 and 15 min samples, respectively. A possible thermal oxidation mechanism model for the samples is similar to the one presented in section 4.1.1.5.



(a) (b) (c)

Figure 4.23: Schematic representation of the oxidation mechanism model (a) Sputtered Ho on SiC substrate, (b) thermal oxidation of samples at 10 min, and (c) thermal oxidation of sample at 15 min.

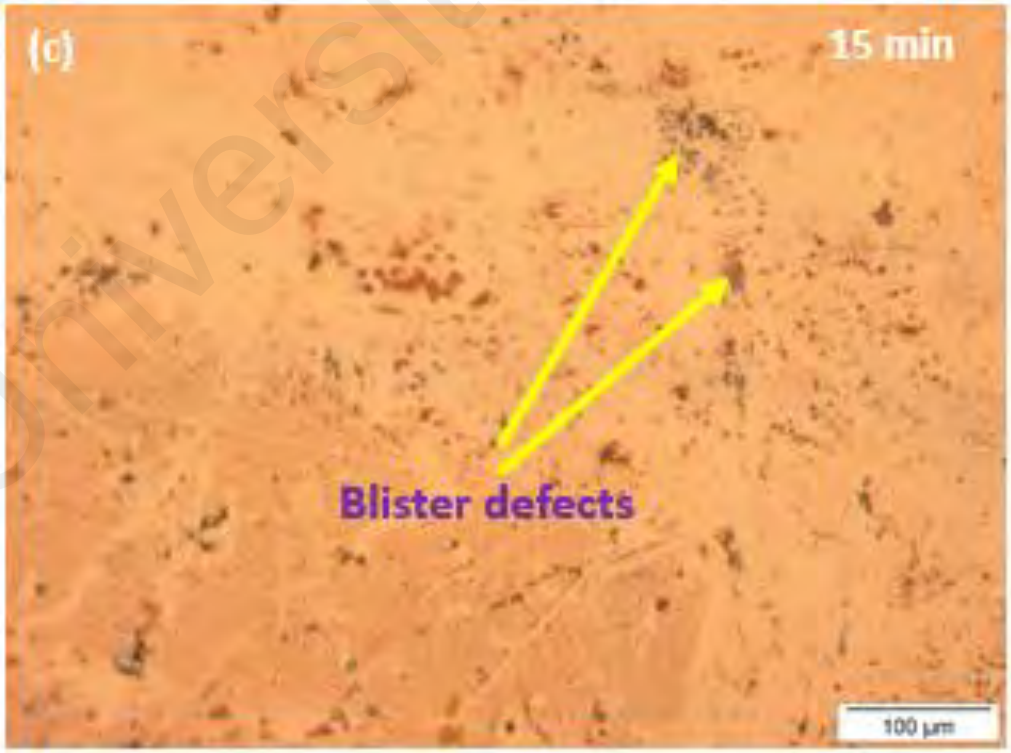
4.2.1.7 Optical Microscope Image Analysis

In order to obtain a high contrast optical microscopic images of Ho_2O_3 thin film, the samples were subjected to experimental investigation. This is to ensure that the morphological features and quality of the samples are properly examined. It is also important to examine the morphology of the gate oxide on the substrate, especially when it is employed as a semiconductor component in MOSFETs. In this study, the optical images of the Ho_2O_3

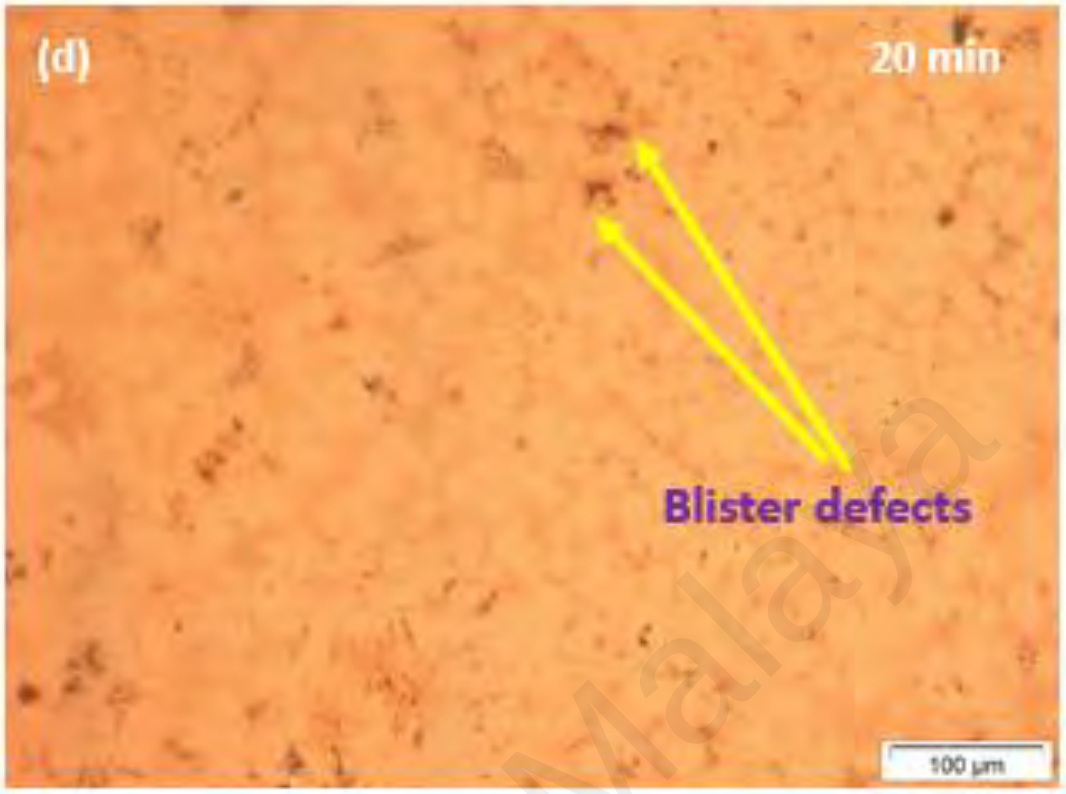
thin film were examined with a conventional optical microscope. The microscopy images of the samples are displayed in Figure 4.24. Figure 4.24 (a) shows the samples oxidized at 5 min duration. Here, blister-like defects were observed in a scattered pattern throughout the samples' surfaces. In Figure 4.24 (b), the 10 min samples displayed more intensities of blister defects with mild film discolouration. Higher concentrations of blister defects and film discolouration were noticed in the 15 min samples Figure 4.24 (c). The samples oxidized at 20 min exhibit more severe blisters and discolouration with dull appearance when viewed with the naked eye (Figure 4.24 (d)). It was generally observed that the blister defects increase with oxidation time.

(a)

(b)



(c)



(d)

Figure 4.24: Microscopy image of the oxidized sample at (a) 5 min (b) 10 min (c) 15 min (d) 20 min oxidation time.

4.2.2 Electrical Characterization

4.2.2.1 Leakage Current Density–Breakdown Field (J–E)

The current–voltage (I–V) data was analyzed and represented by leakage current density–breakdown field (J–E) as displayed in Figure 4.25. It was observed that the MOS capacitor was characterized mostly by two-step breakdowns in all the oxidized samples between 5 and 15 min, while a four-step breakdown was revealed in the 20 min samples. The performance of the device is influenced by densities of interface defect and oxide variation due to irradiation of gamma (Manikanthababu et al., 2020).

For the best sample to be determined by its electrical properties, it is required of such sample to possess a low current leakage density and high electric field voltage (Hetherin et al., 2017a). Therefore; from the analysis of this research, the 15 min sample displays the best electrical results, with an E and J values of 7.57 MV/cm and 6.14×10^{-3} A/cm^2, respectively. More so, the breakdown field attained in this experiment is relatively higher than many of those of the previous studies, this may be ascribed to variation in thickness of the film and the fabrication process.

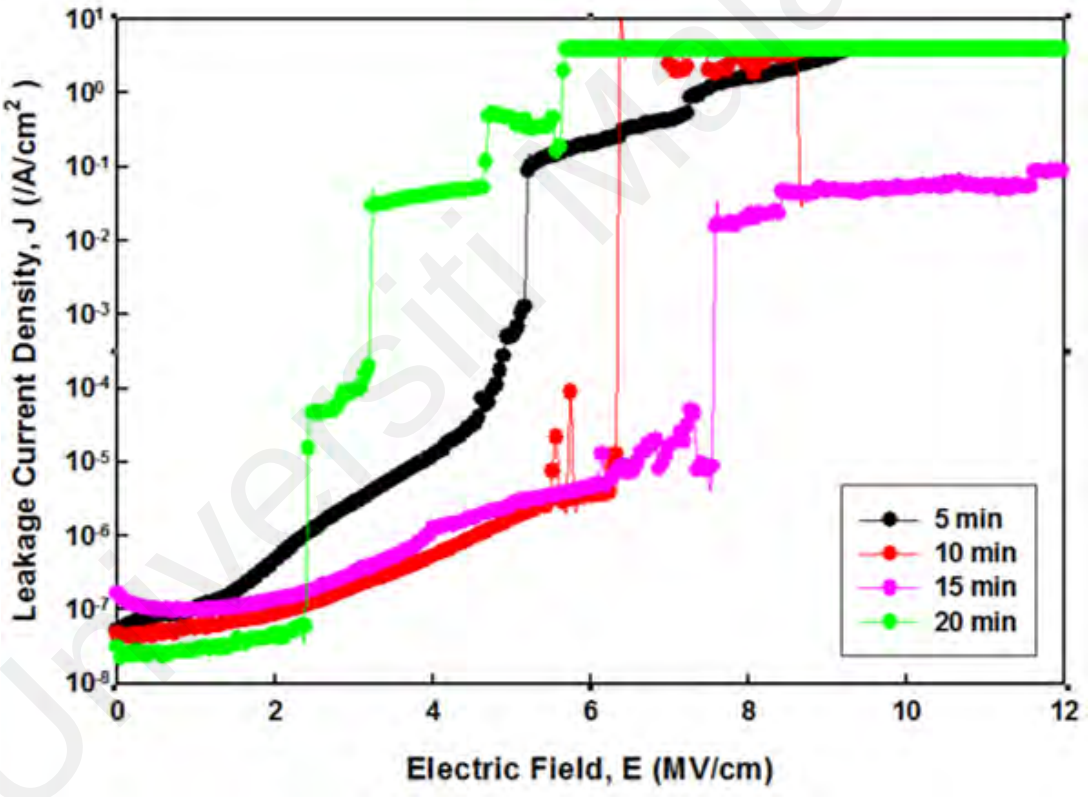


Figure 4.25: J–E plot of samples oxidized at different oxidation time.

4.2.2.2 Fowler–Nordheim (F-N) Tunneling

Figure 4.26 shows the F-N tunneling linear regression graph of thermally oxidized samples from 5 – 20 min. The data obtained for the J-E plot was actually transformed and used to plot the graph of ln (J/E^2) versus 1/E. The barrier height was later calculated using the gradients and intercepts from the graph.

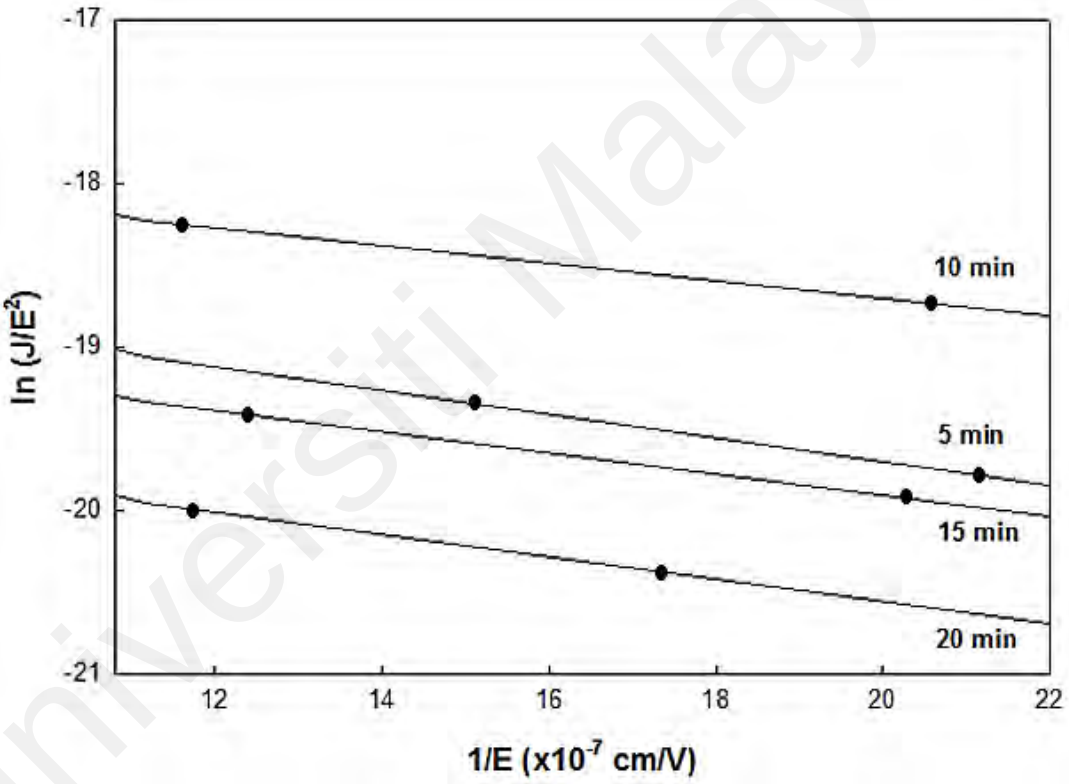


Figure 4.26: F-N tunneling linear regression plot of the oxidized samples at different periods.

4.2.2.3 Barrier Height

Figure 4.27 shows the barrier height graph of the thermally oxidized samples at different durations. The data for this plot was obtained from the F–N tunneling regression

graph (Figure 4.26) (Forbes, 1999a, 1999b; Chiou et al., 2001; Forbes & Deane, 2007). According to Figure 4.27, the sample with the highest Φ_B shows the best electrical results at 15 min oxidation period, with a Φ_B value of 1.67 eV.

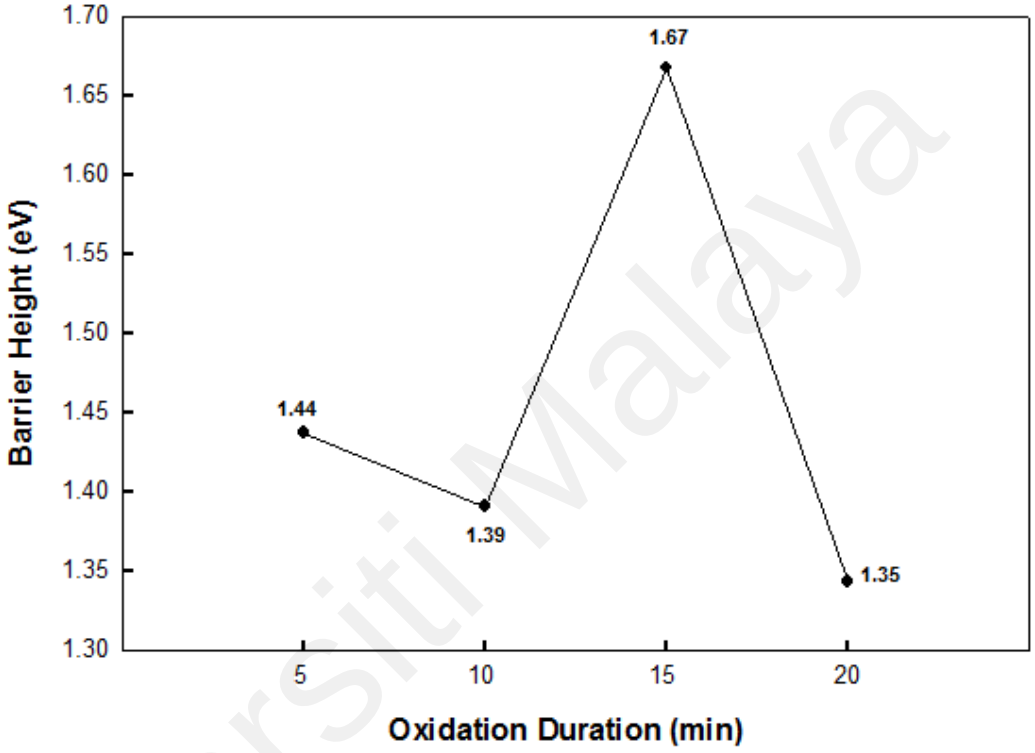


Figure 4.27: Barrier height of the samples at different oxidation time.

4.3 The Effects of O_2 and N_2 Gas Concentrations on the Physical and Electrical Characteristics of Ho_2O_3 on SiC Substrate

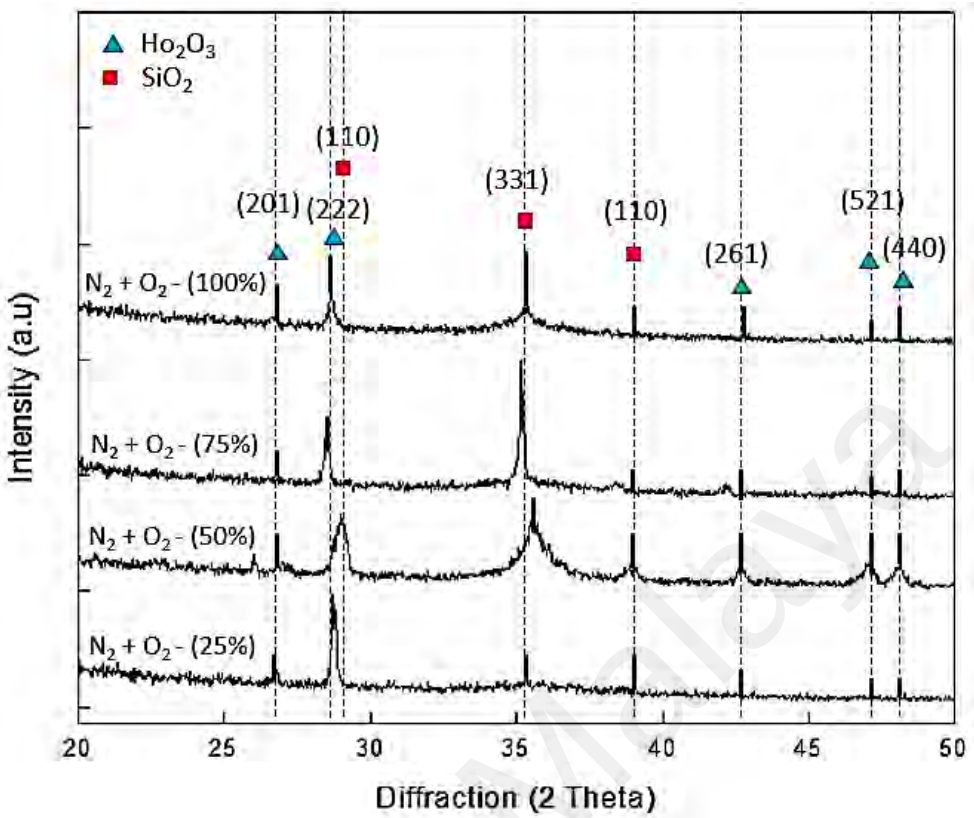
4.3.1 Physical Characterization

4.3.1.1 XRD Analysis

The crystallinity and crystal structure of the chemical compounds formed during thermal oxynitridation of Ho_2O_3 thin films on SiC substrates were examined and presented

in Figure 4.28 as XRD spectra. The figure shows the diffraction patterns of the samples within the range of (25 – 100 %) for various percentages and proportions of N_2 and O_2 gas concentrations in pro rata range of (75, 25 %), (50, 50 %), (25, 75 %) and (0, 100 %) for the N_2 and O_2, respectively. Five diffraction peaks, identified as cubic Ho_2O_3 and denoted as c-Ho_2O_3 were detected at diffraction angles of 27.21°, 28.05°, 42.26°, 47.04° and 48.63° corresponding to plane orientations of (201), (222), (261), (521) and (440) respectively. These samples were matched with reference codes 185248 and 27773 of the Inorganic Crystal Structure Database (ICSD). Also, three other peaks identified as monoclinic (b)-SiO_2 were found at 29.41°, 35.17° and 38.63° which belong to (110), (321), (110), respectively for all the oxynitridated samples. This observation could contribute to the diffusion of N_2O gas formed by the reaction of the N_2 and O_2 gas on the Ho_2O_3 layer, when the Ho reacted with O_2 to form crystallized Ho_2O_3. These findings conform to the J-E results which will be discussed later in this thesis.

A high number of diffraction peaks was observed, owing to a selected crystal orientation (Hetherin et al., 2017a). The highest intensity of Ho_2O_3 was observed on the 100 % sample while the lowest was recorded at 25 % concentration of O_2. Since the degree of crystallinity can be attributed to an increase in intensity, it can be deduced that the increase in O_2 concentration between the 25 and 100 % enhanced crystallinity of the Ho_2O_3 gate oxide (Onik et al., 2021a).



***Interpretation**

$N_2 + O_2$ - (100%) ➔ (0% N_2 + 100 % O_2)
$N_2 + O_2$ - (75%) ➔ (25% N_2 + 75 % O_2)
$N_2 + O_2$ - (50%) ➔ (50% N_2 + 50 % O_2)
$N_2 + O_2$ - (25%) ➔ (75% N_2 + 25 % O_2)

Figure 4.28: XRD spectra of oxynitridated samples of SiC/Ho_2O_3 at various concentrations of N_2 and O_2.

In order to determine microstrain (ε) and the crystal size (D) of the thermally nitridated and oxidized samples, the Williamson–Hall (W–H) plot was employed. This is necessary to evaluate peak broadening due to dislocation and crystal defects. There are two causes of Peak broadening; they are crystallite size and strain. The previous occurs as a result of disordered distribution of finite elements, while the latter is formed by disjointed or non-uniform displacements of elements within the lattice position (Onik et al., 2021b). Figure 4.29 displays the W-H plot for the oxynitridated samples at different flow concentrations. The crystallite size was analyzed based on the peak data from the W-H plot. From the analysis,

the average crystallite sizes of Ho_2O_3 were obtained in the range of 0.94 and 6.35 nm, while that of SiO_2 were gotten in the range of 0.94 and 3.98 nm for all the samples at the different gas concentrations (Figure 4.30).

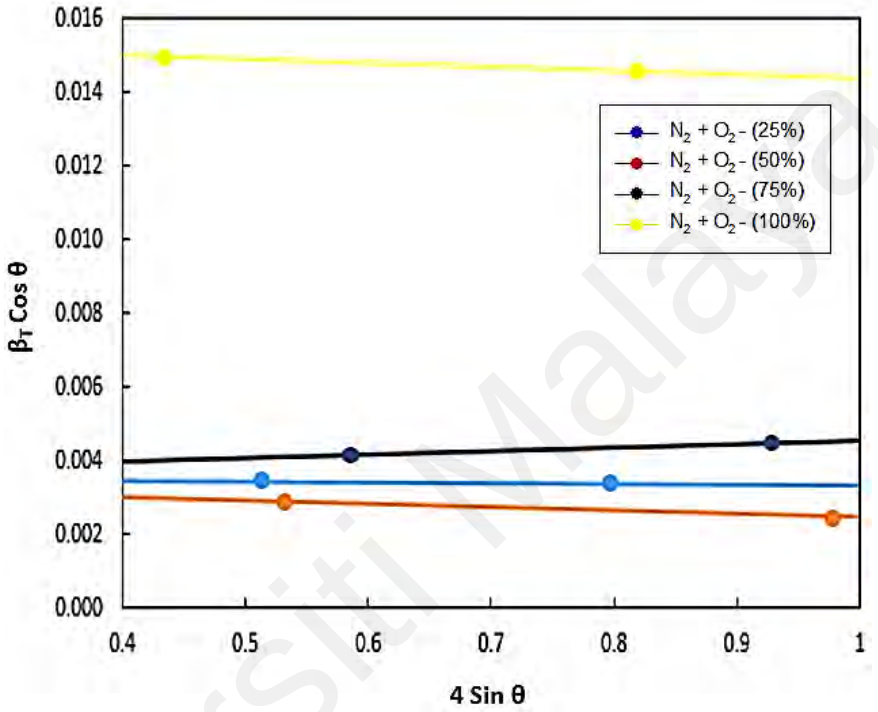


Figure 4.29: W–H plot of oxynitridated Ho_2O_3 for samples at different flow concentrations.

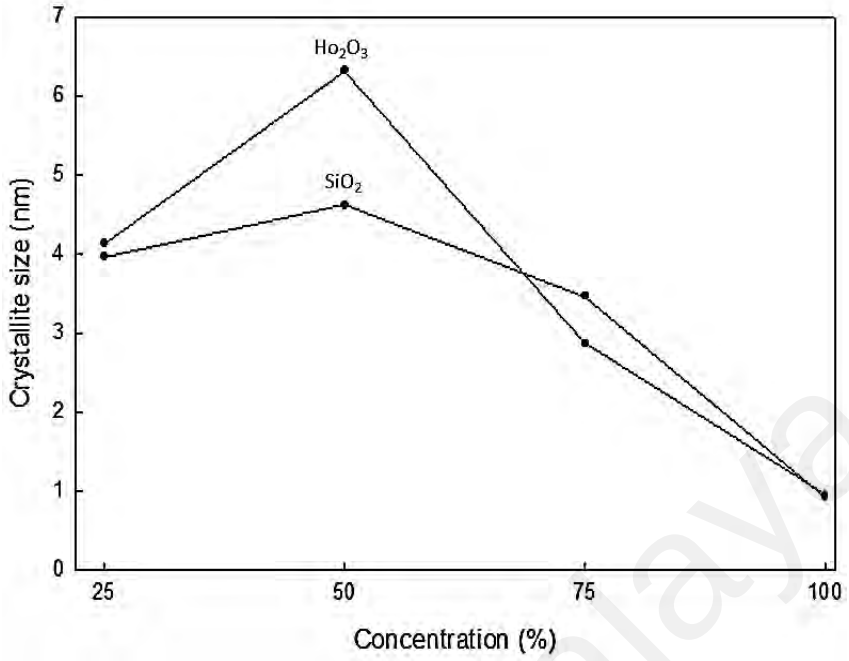


Figure 4.30: Crystallite sizes of oxynitridated Ho_2O_3 and SiO_2 calculated from W–H plot for samples at different flow concentrations.

Figure 4.31 shows the graph of calculated values of the microstrain obtained from the W-H plot. Similar to the crystallite size, the microstrain of the oxynitridated samples of Ho_2O_3 are 0.0003965, 0.0002628, 0.0006109 and 0.0016873 for the 25, 50, 75 and 100 % flow concentrations, respectively. In the same vein, the microstrain for the SiO_2 samples were recorded as 0.0002361, 0.0001553, 0.0003378 and 0.0009802, respectively.

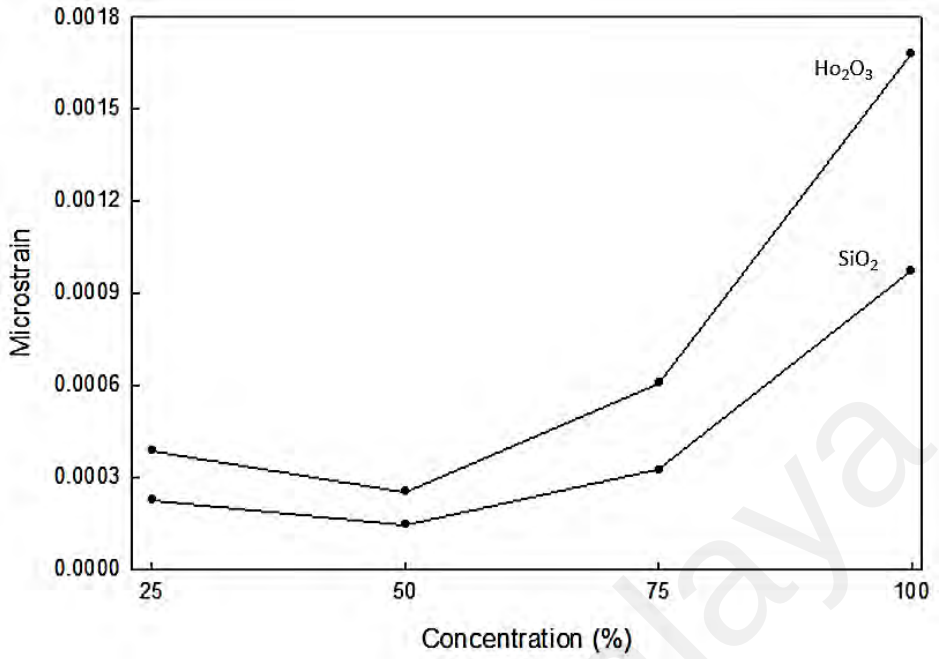


Figure 4.31: Microstrain of Ho_2O_3, SiO_2 at various oxynitridation flow concentrations.

4.3.1.2 FTIR Analysis

Figure 4.32 presents the FTIR spectra of the oxynitridated samples at different gas flow concentrations of N_2 and O_2, with a scan range between 600 and 1100 cm^{-1}. This is meant to evaluate the functional groups and the chemical working atoms of the samples. From the analysis, the traces of Ho_2O_3 were detected in all the samples between 25 and 100 % gas flow concentrations. This observation is in conformity with the XRD analysis and the J-E characteristics results, which are discussed in the next section. SiO_2 peaks at 805 (Hetherin et al., 2017a, 2017b) and 907 cm^{-1} (Deng, Wilkie, Moore, & Mauritz, 1998) were detected in all the specimens. The Ho_2O_3 peaks at 944 and 1002 cm^{-1} (Abu-Zied & Asiri, 2019) were also found in all the samples.

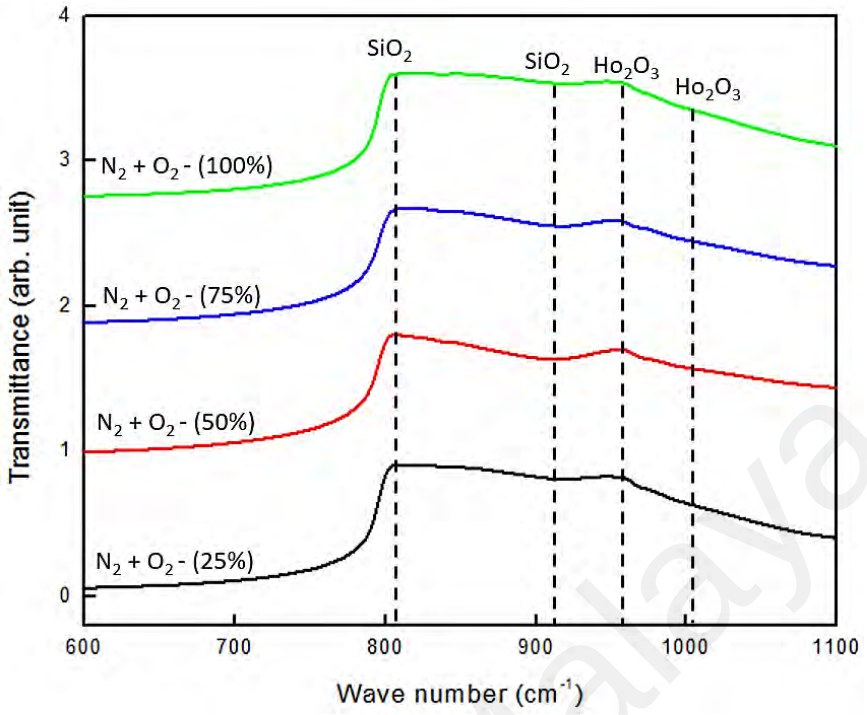


Figure 4.32: Transmittance spectra of oxynitridated samples oxidized at different flow concentrations.

4.3.2 Electrical Characterization

4.3.2.1 J-E Characteristics

The leakage current density–breakdown electric field (J-E) characteristics of the oxynitridated samples at different gas flow concentrations of N_2 and O_2 on Ho_2O_3 thin films on SiC substrates were performed according to Wong & Goh, (2018). Figure 4.33 presents the J-E characteristics of the samples at various gas flow concentration. The electrical breakdown fields were 1.21, 7.52, 8.52, and 5.21 MV/cm. The Electrical results showed that the 75 % samples displayed the largest breakdown electrical field. This analysis shows that the 50 % oxynitridated samples produced the best electrical results at E of 7.52 MV/cm with a leakage current density of 6.05×10^{-2} A/cm^2. It was observed that, as the percentage

concentration of the oxynitridation gas flow increases, the magnitude of the breakdown field first increases, then decreases. This could be attributed to the smooth surface of the sample and the presence of c-Ho_2O_3 and monoclinic-(b) SiO_2 phases in the oxide films as observed by XRD analysis. The 75 % samples showed an almost short circuit in J-E curves, signifying poor dielectric performance. This may be due to the formation of Ho-Al metallic bond. The results also show that the inclusion of nitrogen in the oxidation gas significantly enhanced the lowered leakage current density and electric field (Kaya, Yilmaz, Karacali, Cetinkaya, & Aktag, 2015; Wong & Goh, 2018). Therefore, the 50 % oxynitridated samples possess the best electrical properties for Ho_2O_3 dielectric MOS devices.

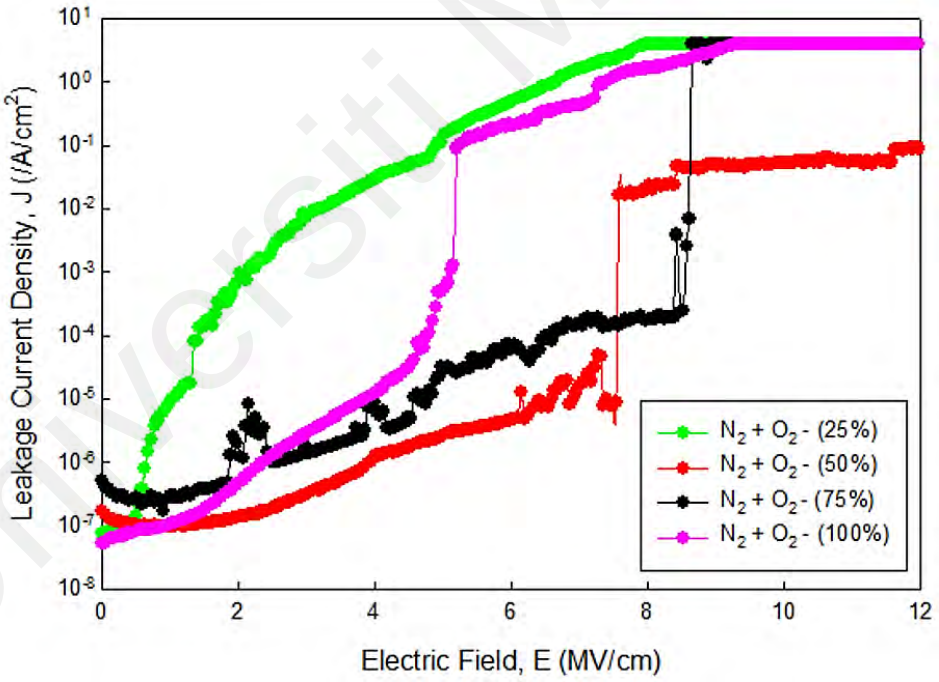


Figure 4.33: J–E plot of oxynitridated samples at various flow concentrations.

4.3.2.2 F-N Tunneling and Barrier Height

Figure 4.34 presents the F-N tunneling graph of the oxynitridated samples. The tunneling mechanism was plotted basically to extract the data for barrier height, Φ_B. The barrier height, Φ_B describes the conduction band between the Ho_2O_3 gate oxide and the SiC substrate. It was derived from the F–N tunneling graph in form of a linearized model (Forbes, 1999a, 1999b; Chiou et al., 2001; Forbes & Deane, 2007).

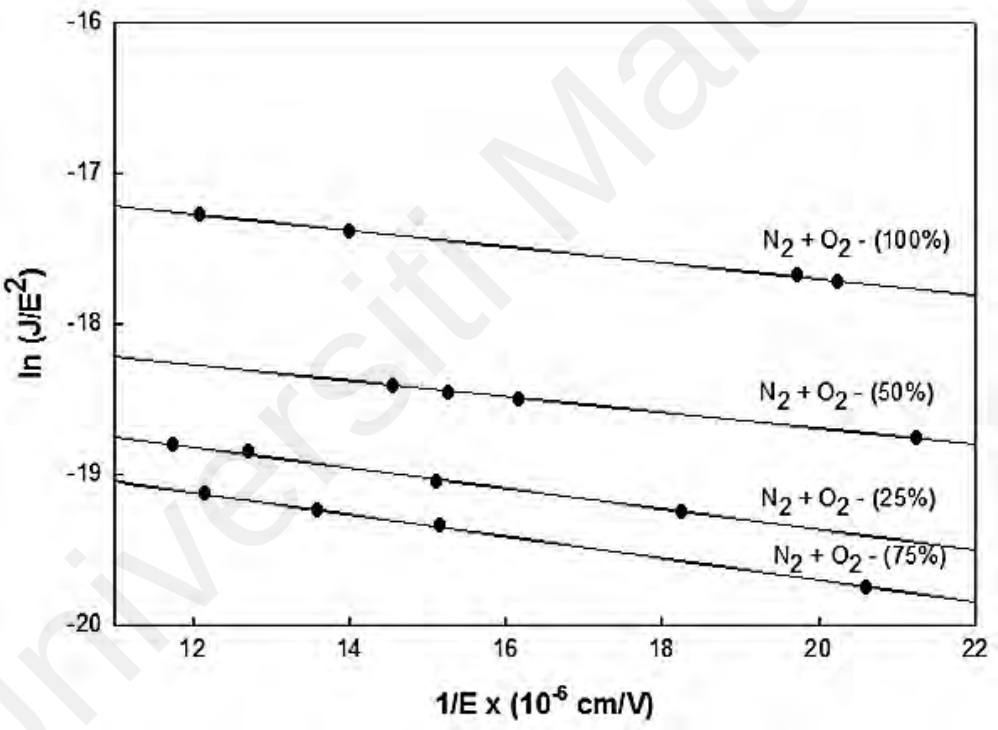


Figure 4.34: F-N tunneling linear regression plot of the oxynitridated samples at different flow concentrations.

The barrier height plot is presented in Figure 4.35. The sample with the highest Φ_B displays the best electrical results at 50 % oxynitridation, with a barrier height value of 18.5 eV.

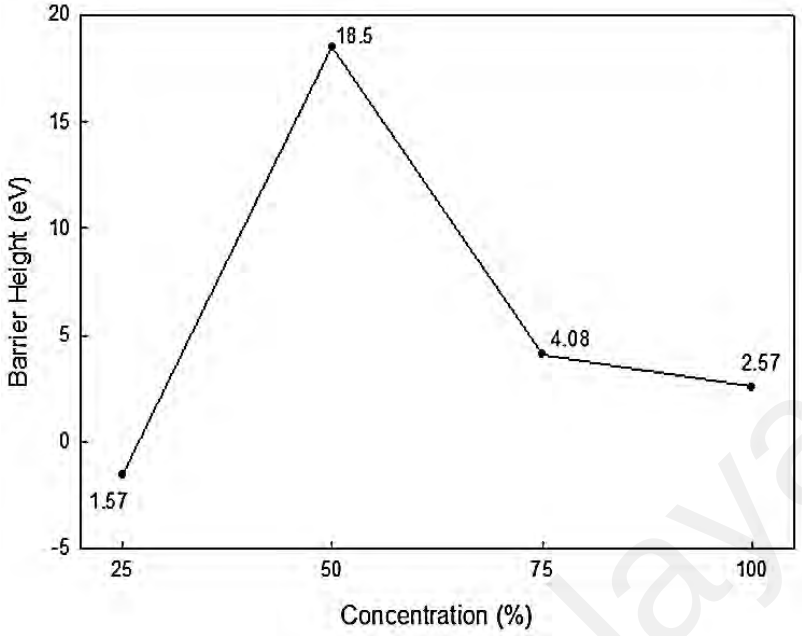


Figure 4.35: Barrier height of the oxynitridated film samples at different flow concentrations.

4.3.3 Comparison of the Effect of Thermal Oxidation and Oxynitridation on the Physical and Electrical Properties of the Ho_2O_3 Thin Film on SiC Substrate

The effect of both thermal oxidation and oxynitridation of the samples with respect to their physical and electrical characteristics were compared after all the necessary analysis have been completed. The comparison of the effects of both processes on the physical and electrical properties of Ho_2O_3 thin film on SiC substrate is presented in Table 4.2. Based on the XRD analysis, six and five planes of Ho_2O_3 were detected for the thermal oxidation and oxynitridation, respectively. According to the FTIR, four peaks of Ho_2O_3 were detected during thermal oxidation, while two were detected during the oxynitridation process. Similarly, two peaks of SiO_2 were observed during both processes. Based on the electrical results, with consideration to the J-E and the barrier height analysis, the thermal oxynitridation samples display a better electrical performance. This suggests the beneficial effect of introducing nitrogen gas concentration into the thermal oxidation process.

Table 4.2: Comparison between the effect of thermal oxidation and oxynitridation on the Physical and electrical properties of the Ho_2O_3 thin film.

Characterization	Properties	Unit	Thermal Oxidation	Crystal System	Thermal Oxynitridation	Crystal System
XRD	Plane of Ho_2O_3		(111), (003), (431), (411), (620), (541)	Monoclinic-(b)	(201), (222), (261), (521), (440)	Cubic
	Plane of SiO_2		(100), (440), (101), (400), (444), (640)	Trigonal (H), Monoclinic-(c)	(110), (321), (110)	Monoclinic-(b)
	Crystallite size of Ho_2O_3 (min)	nm	2.83	-	0.94	-
	Crystallite size of Ho_2O_3 (max)	nm	3.84	-	6.35	-
	Microstrain of Ho_2O_3 (min)	-	-0.00987	-	0.0006109	-
	Microstrain of Ho_2O_3 (max)	-	0.00577	-	0.0016873	-
	Microstrain of SiO_2 (min)	-	-	-	0.0001553	-
	Microstrain of SiO_2 (max)	-	-	-	0.0009802	-
FTIR	Number of Ho_2O_3 peaks	-	4	-	2	-
	Number of SiO_2 peaks	-	2	-	2	-
XPS	Binding Energy of Ho_2O_3 at O1s (min)	eV	530.5	-	-	-
	Binding Energy of Ho_2O_3 at O1s (max)	eV	533	-	-	-
	Binding Energy of SiO_2 at O1s (min)	eV	531.8	-	-	-
	Binding Energy of SiO_2 at O1s (max)	eV	533	-	-	-
HRTEM	Thickness of the oxide layer (min)	nm	3.55	-	-	-
	Thickness of the oxide layer (max)	nm	4.52	-	-	-
	Thickness of the inter-planar segment (min)	nm	10.15	-	-	-
	Thickness of the inter-planar segment (max)	nm	11.29	-	-	-
Electrical	Leakage current density	A/cm^2	4.32×10^{-3}	-	6.05×10^{-2}	-
	Breakdown Field	MV/cm	8.95	-	7.52	-
	Barrier height	eV	9.82	-	18.5	-

4.4 Thermodynamic Stability and Thermal Stress Analysis of Ho_2O_3 Thin film on SiC Substrate

4.4.1 Temperature Distribution

The meshing of the capacitor is shown in Figure 4.36. The substrate and the film are divided into two individual parts so that each one could be meshed separately in the model. This is to ensure that a denser mesh is created on the capacitor where heat is dissipated and reduce it further away for a more effective simulation. To determine the thermal distribution along the device, a steady-state thermal analysis of the model was performed. The surrounding temperature was kept at 22 °C, and a thermal load of 800 °C was applied on the device. Some of the assumptions made in the simulations are that; there is no internal heat generation, heat flow is unidirectional, and the conduction takes place under steady-state conditions (Alshahed et al., 2015). At the completion of the fırst solutıon, the variations in temperature are then considered at a step increment of 100 °C up to 1100 °C as the applied load on the capacitor. The result profiles of the thermal distribution are shown in Figure 4.37 (a) – (d), while the equivalent von misses' stress is discussed in the following sub-section.

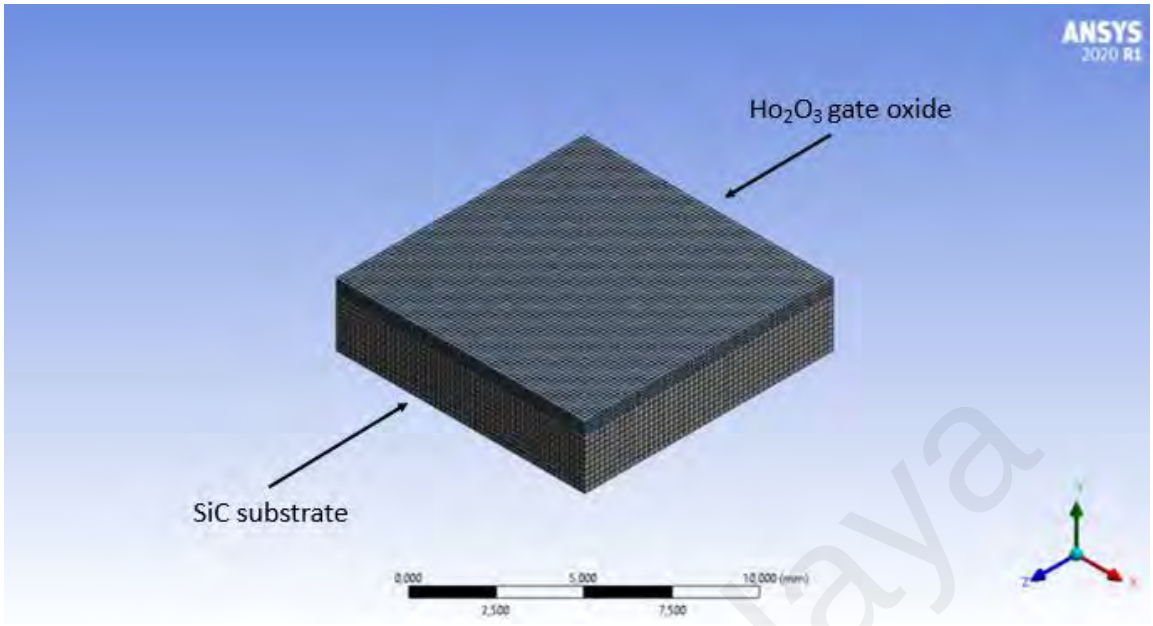
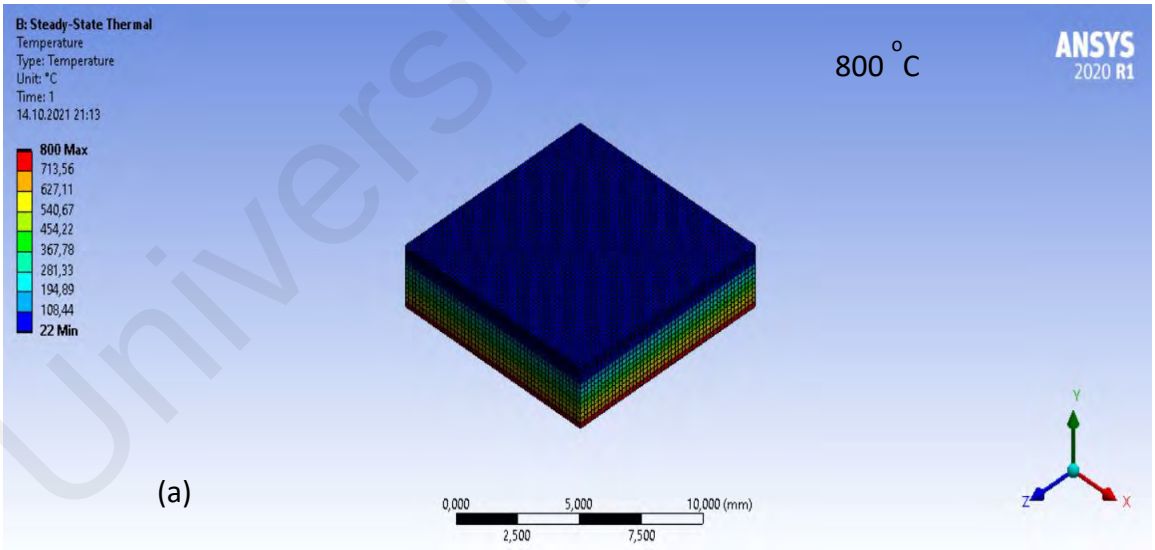
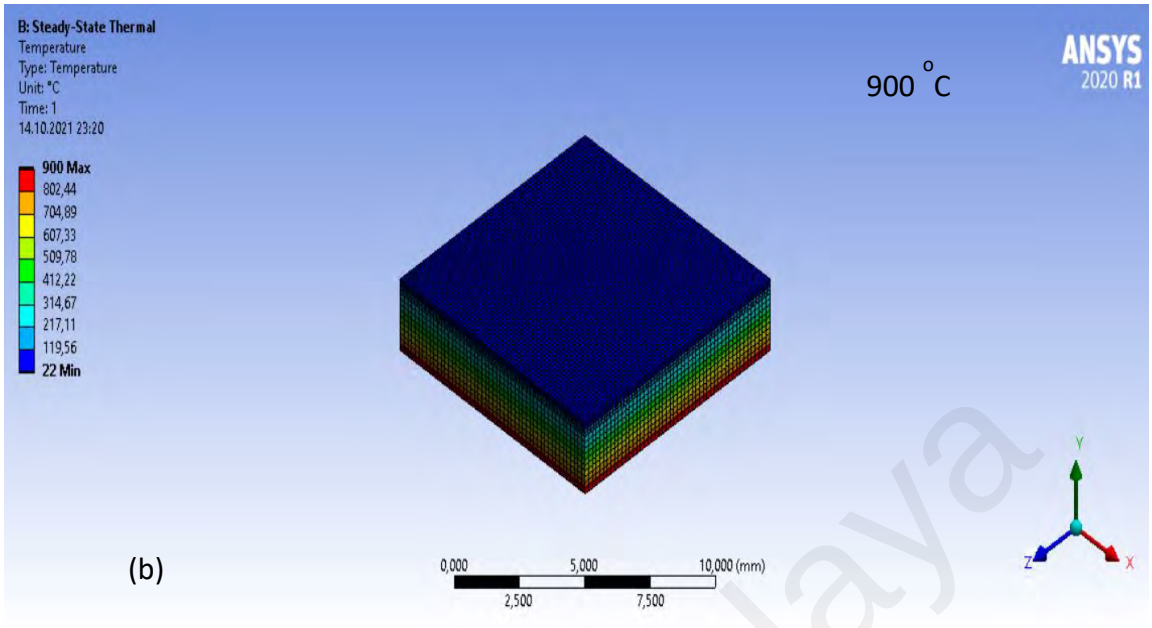


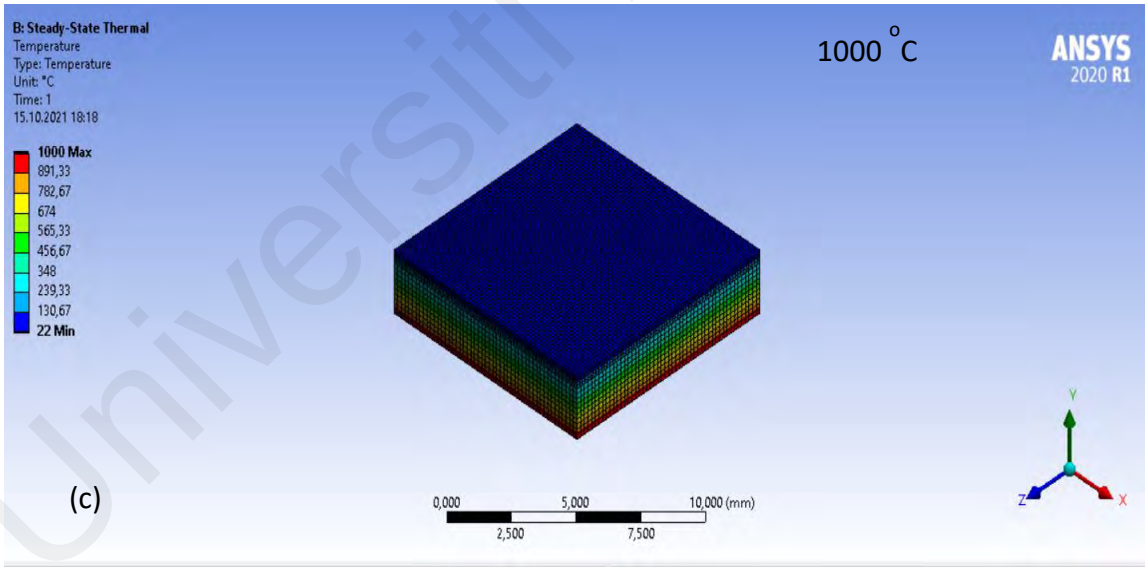
Figure 4.36: The mesh of the SiC substrate/Ho_2O_3 gate oxide structure



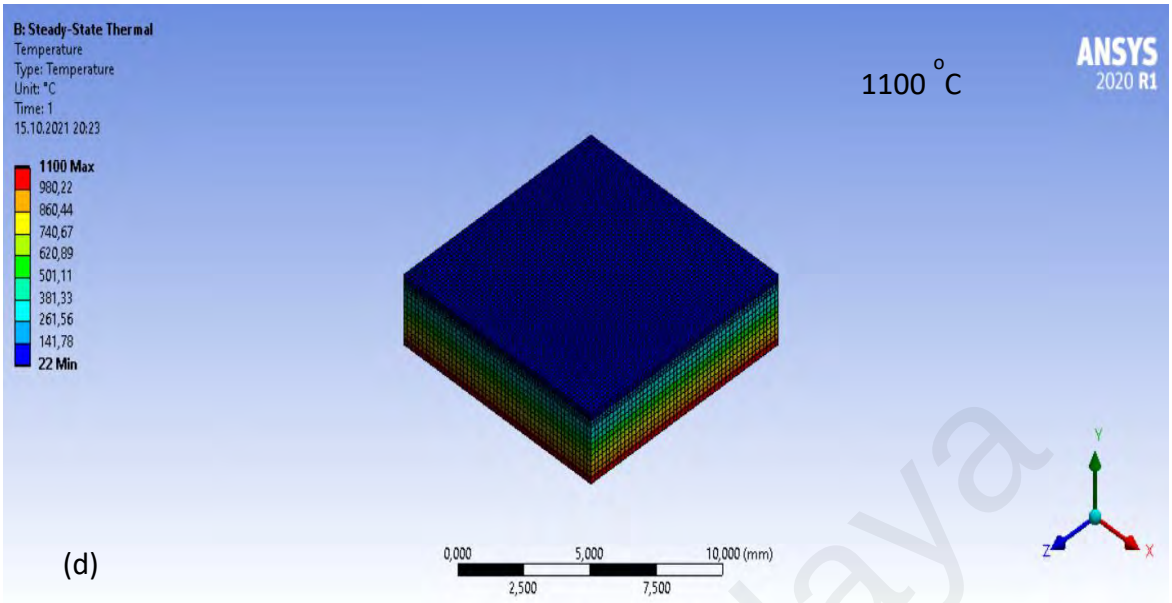
(a)



(b)



(c)

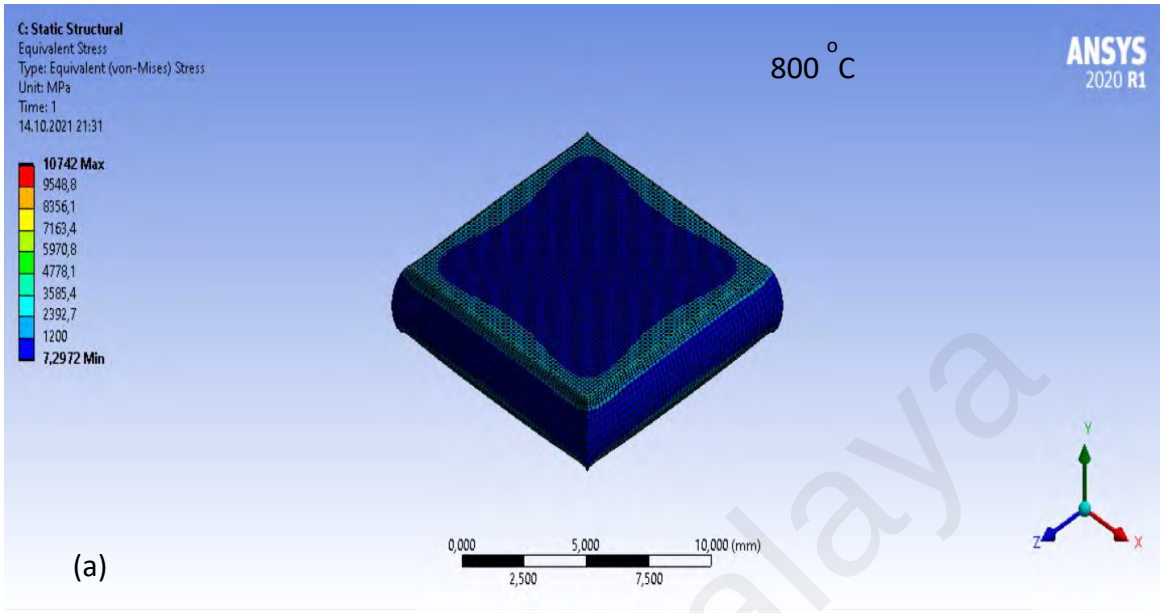


(c)

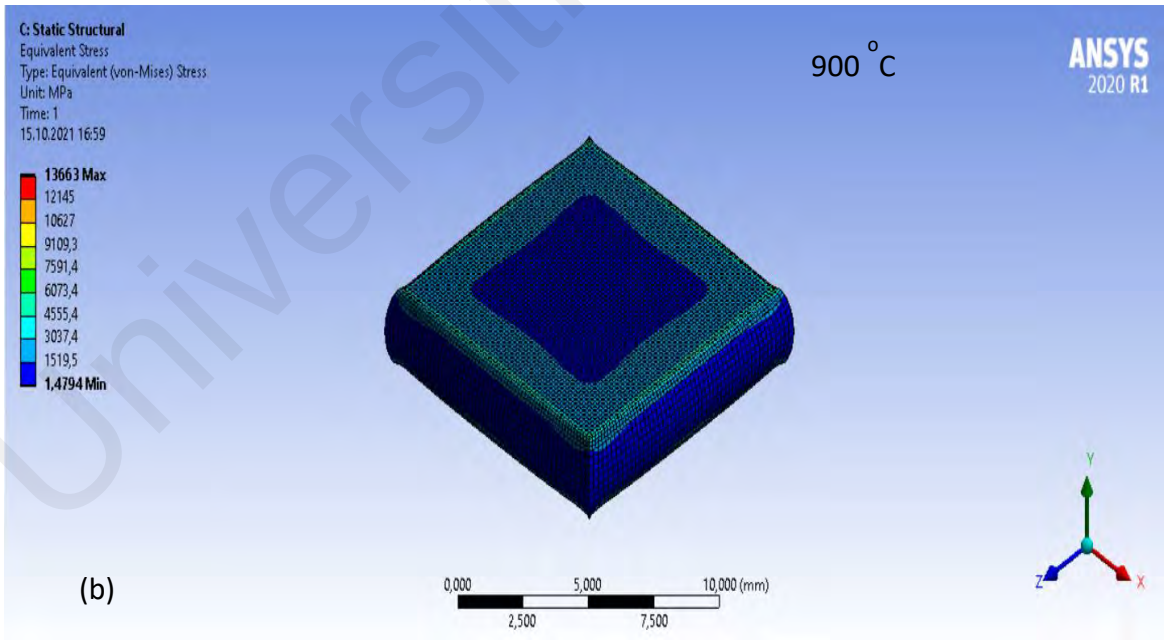
Figure 4.37: Analysis of temperature distribution of the SiC substrate/Ho_2O_3 gate oxide structure from 800 - 1100 ºC.

4.4.2 Thermal Stress Analysis

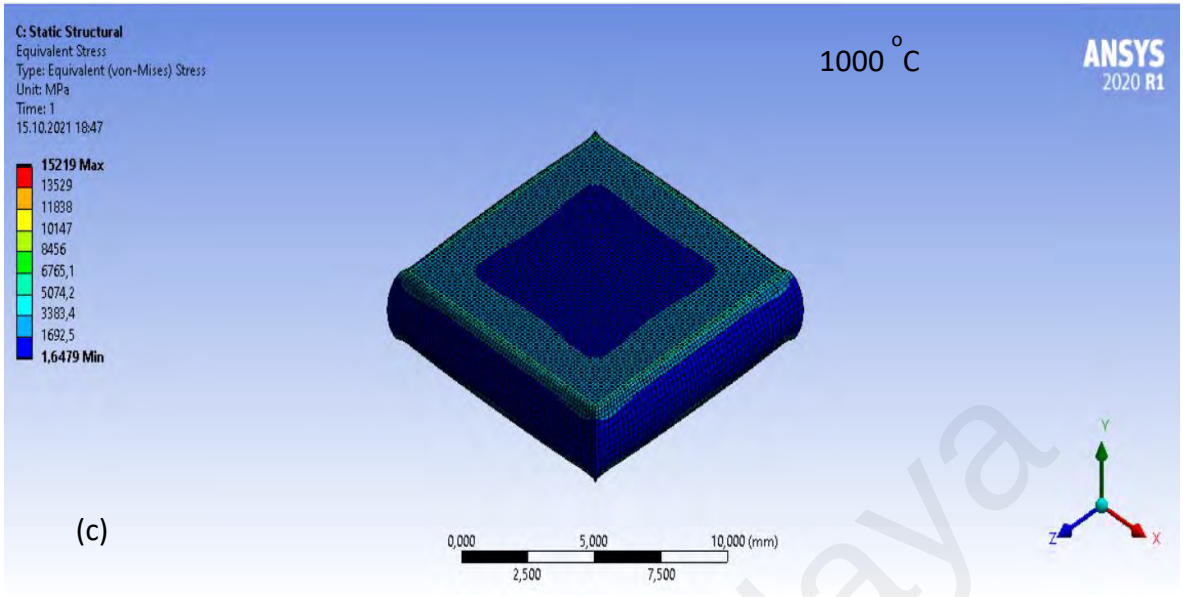
In order to determine the stress distribution in the MOS capacitor, especially at the thin film surface and the interface of the component, the amount of temperature-induced stress required to cause plastic deformation was identified. This stress is expressed in terms of thermal loading applied on the component which can propagate local stress to reach a yield strength of 200 MPa. Figures 4.38 (a) – (d) show the distribution of equivalent Von-misses thermal stress on the components for the applied temperature range, between 800 and 1100 ºC. From the figures, the sections with red colour on the result profiles (scaled residuals) depict the parts of the model on which the effects of thermal loading were mostly felt. From, the simulation results, it was predicted that stress values of 11, 14, 16 and 18 MPa can cause plastic deformation at 800, 900, 1000 and 1100 ºC, respectively.



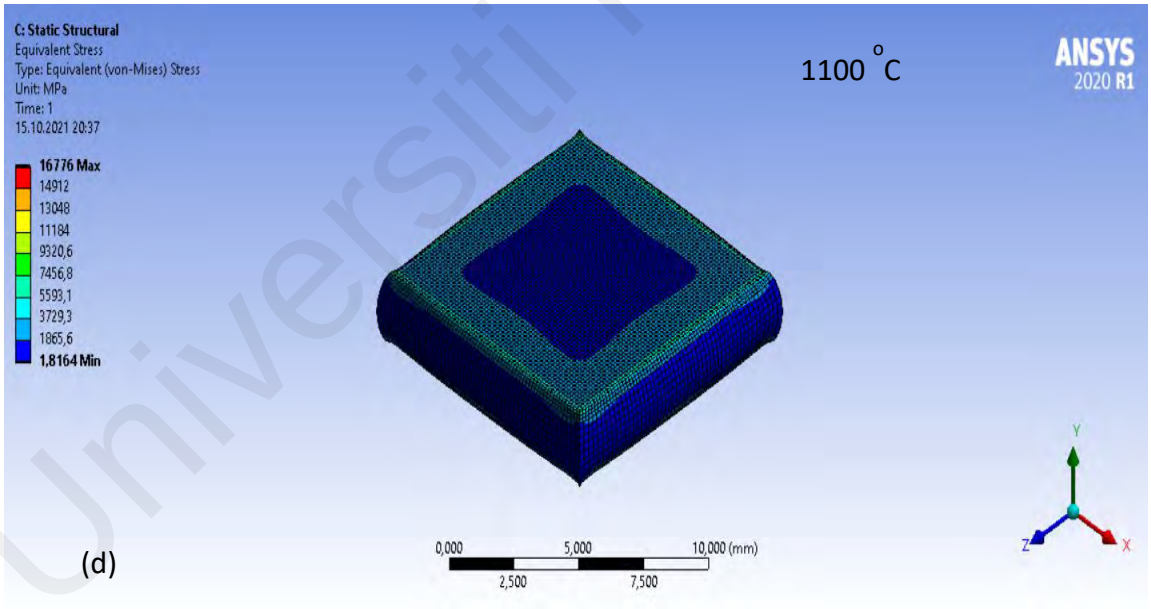
(a)



(b)



(c)



(d)

Figure 4.38: Analysis of Thermal stress (Eq. Von misses) of the SiC substrate/Ho_2O_3 gate oxide structure from 800 - 1100 ºC.

4.4.3 Residual Thermal Stress Relaxation

The stress distribution model, also known as the residual stress model which was developed by Dunand & Mortensen, (1991), and based on the theory of elasticity (Kong, Wang, Wang, Zheng, & Yang, 2019) was used in this study. The residual stress model, expressed in equation (4.10) is derived based on the following assumptions; (1.) no stress is recorded in the device at a particular high temperature, the condition of stress observed at a low temperature can be linked to shrinkage of the MOS capacitor, specifically at the interface, (2.) the SiC substrate and the oxide layer are regular rectangles (Kong et al., 2019). Therefore, the mismatch stress obtained can be expressed as;

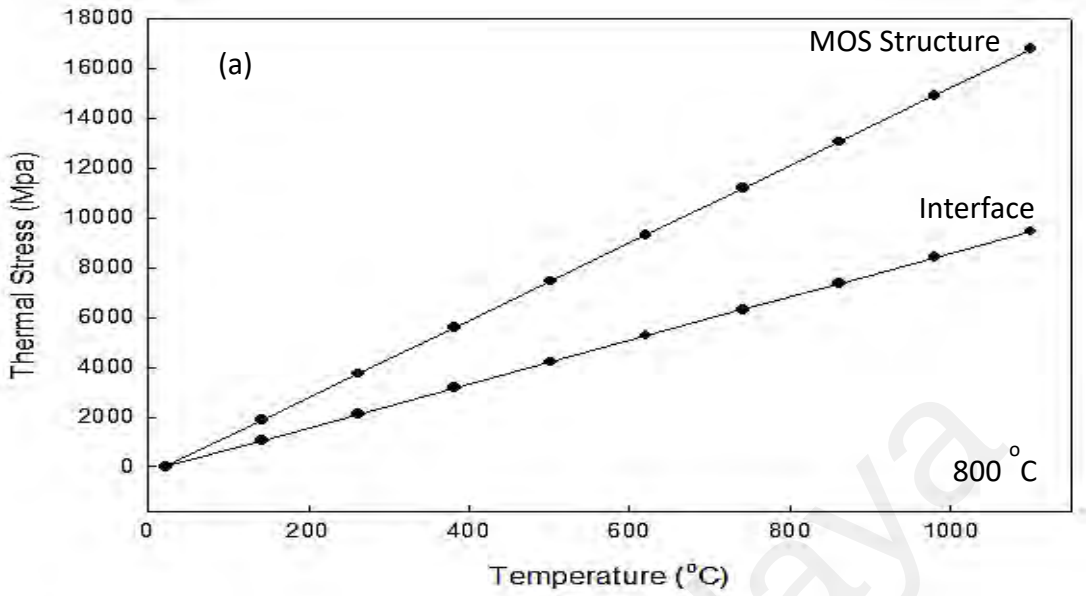
$$\sigma_m = (\Delta\alpha \times \Delta T) \tag{4.10}$$

where σ_m is the mismatch stress, $\Delta\alpha$ is the change in thermal expansion coefficient, and ΔT is the change in temperature. The stress at the interface between the substrate and the gate oxide is expressed as $\sigma_{Intface}$, and can be obtained from the following equation:

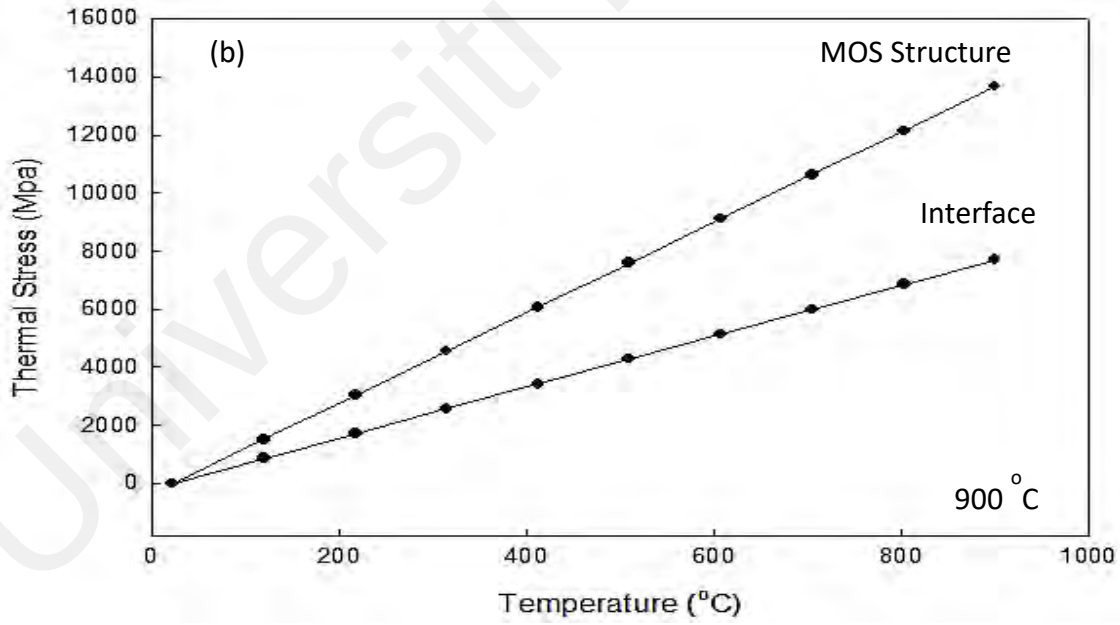
$$\sigma_{Interface} = \frac{(\alpha_S - \alpha_O)\Delta T}{\frac{0.5(1+v_S)+(1-2v_S)v_O}{E_S(1-v_O)} + \frac{1-2\,vo}{E_O}} \tag{4.11}$$

where, α_s is the coefficient of thermal expansion for substrate, α_o is the coefficient of thermal expansion for gate oxide, v_s is the Poisson ratio for substrate, v_o is the Poisson ratio for gate oxide, V_o is the volume fraction for gate oxide, E_s is the Young's modulus for substrate, E_o is the Young's modulus for gate oxide.

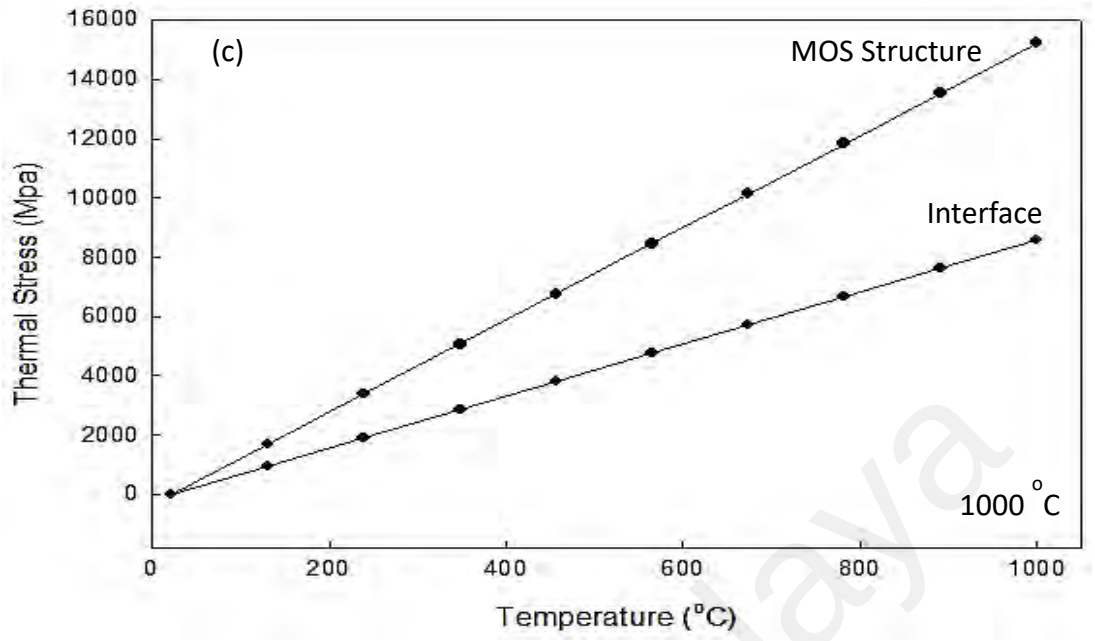
From Figures 4.39 (a) – (d), the thermal stresses obtained at the surface and the interface of the MOS device at 800, 900, 1000 and 1100 ^{o}C temperatures are given as (10.81 and 6.09 Mpa), (13.88 and 7.84 Mpa), (15.31 and 8.69 Mpa) and (16.94 and 9.63 Mpa), respectively.



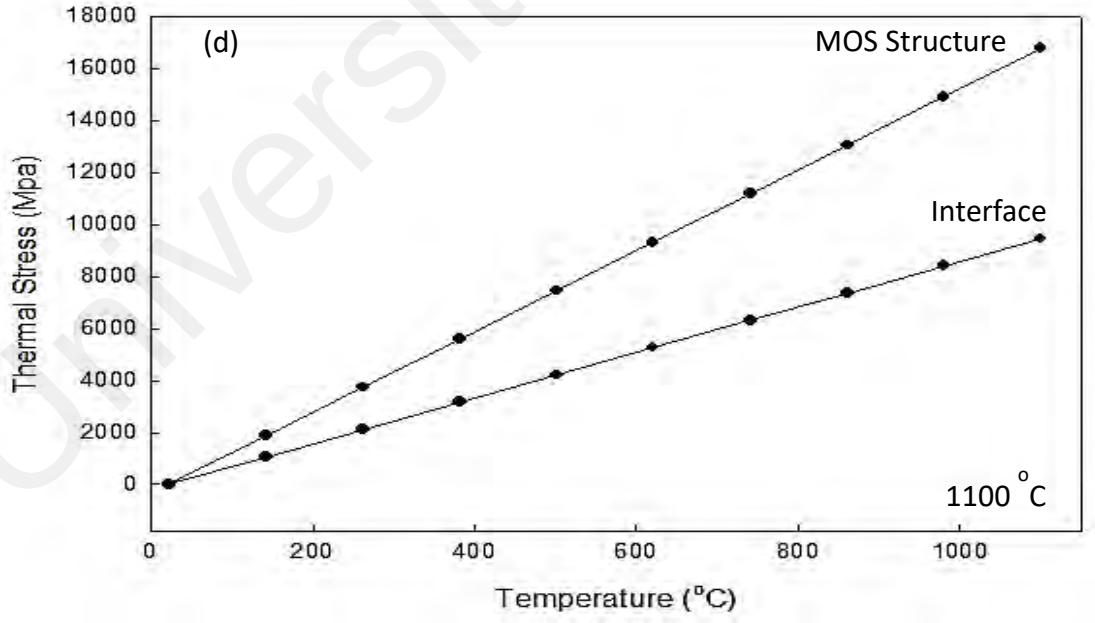
(a)



(b)



(c)



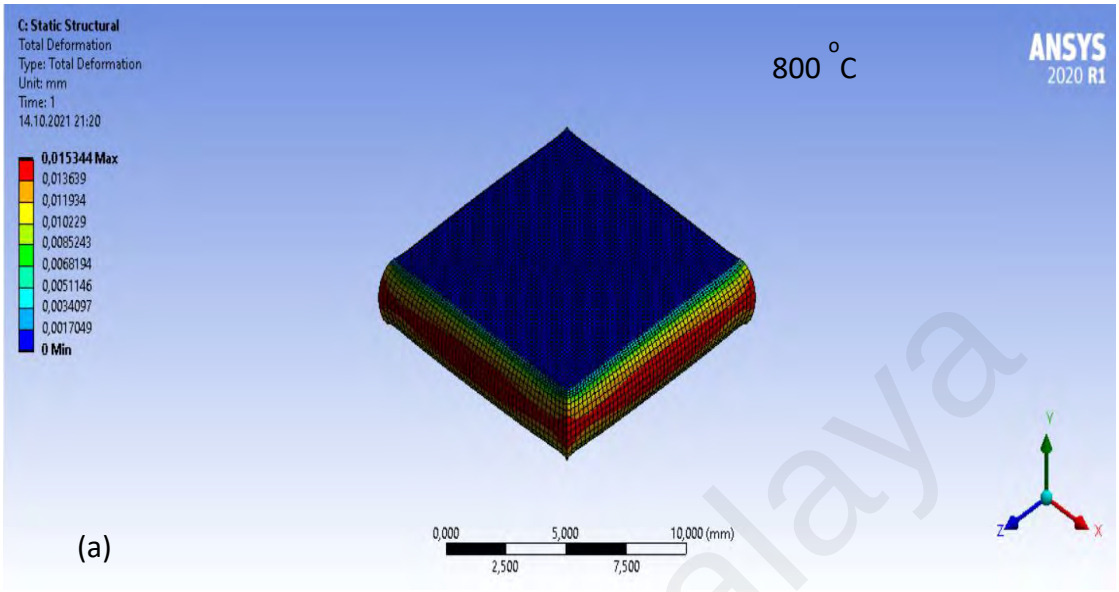
(d)

Figure 4.39: The thermal stress versus applied temperature load on the SiC substrate/Ho_2O_3 gate oxide structure from 800 - 1100 ºC.

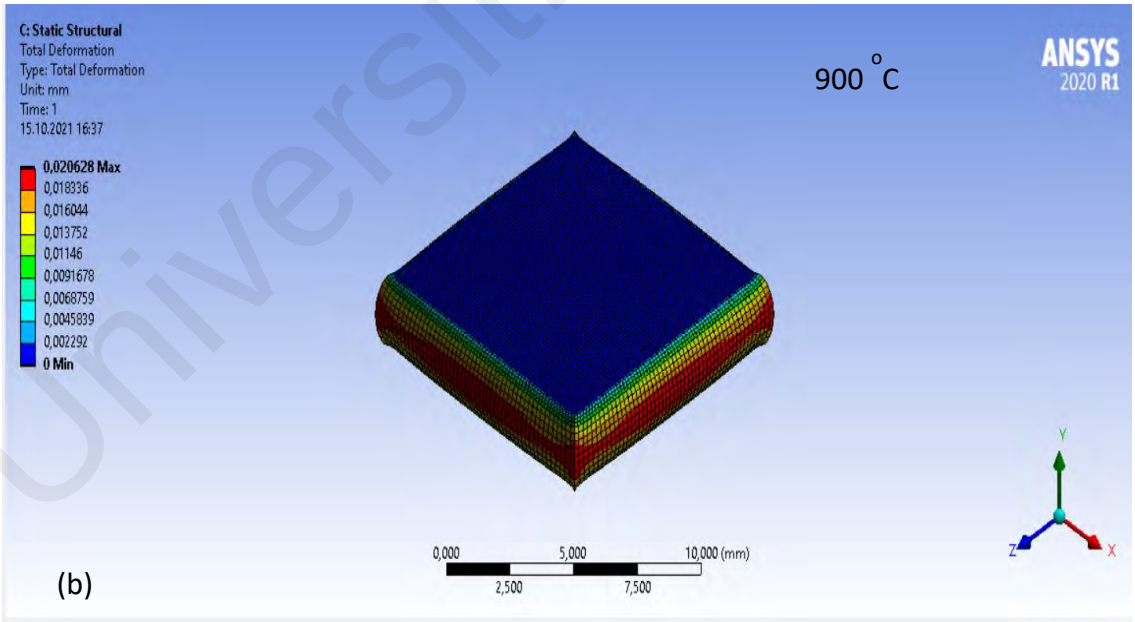
4.4.4 Effect of Deformation on the Device

Excessive thermal stress and deformation are important reasons for having failures in microelectronic devices. One of the significant progress recorded in the evaluation of temperature-induced deformation and thermal stress is the use of the finite element method (FEM) for mechanical and microelectronic devices. Several studies have been carried out in this field of research (Groothuis, Schroen, & Murtuza, 1985; Boiler, 2013; Suhir, 2019; E. Liu, Conti, Bhogaraju, Signorini, & Elger, 2020). Recently, a study on the deformation and thermal stress of a thermo-mechanical device was conducted by (Rajeh, Al-Kbodi, & Zhang, 2020). Von-misses' stress distribution theory was used in that study to analyze and develop a device with minimum stress and deformation-free design.

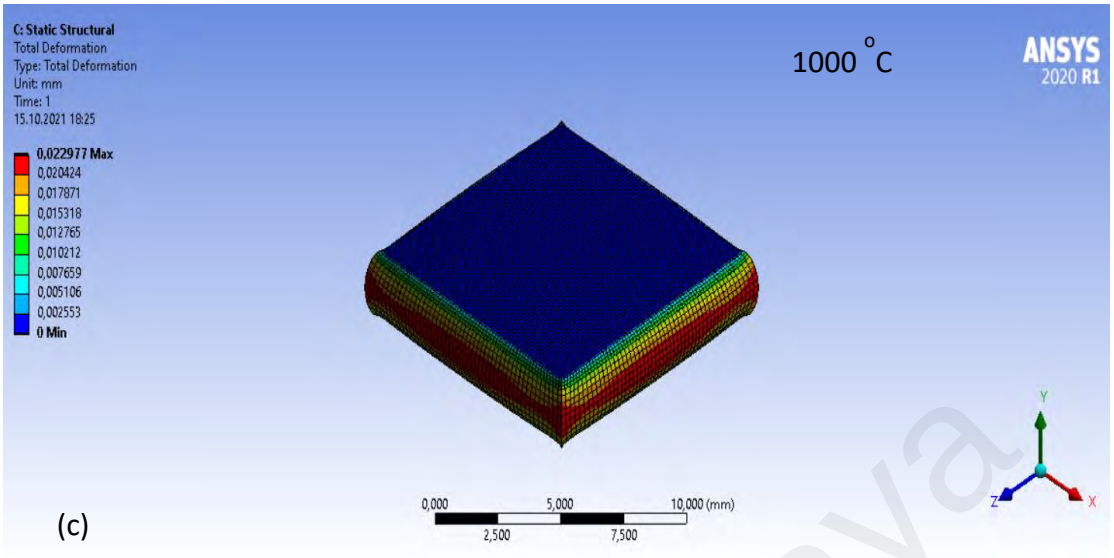
Normally, when the deformation of a structure is reduced, the process of overlay in structural accuracy is increased. More so, there is a direct correlation between a deformed structure and the interfacial stress, and in most cases, the stress affects the distribution of strained bonds at the interface (Krsmanovic et al., 2020). The interfacial layer, being the major part of the microelectronic device varies with breaking and reconnecting of strained bonds. Therefore, in the design of MOS devices, the effect of the deformation of dielectric gates on the performance of the devices should be considered. In this study, the thermal-induced deformation of the device was simulated and analyzed using ANSYS. The simulation results were presented in Figure 4.40 (a) – (d). From the results, it was observed that the substrate and the interface region are more prone to deformation than other parts of the device. This is due to the exposure of the substrate to higher thermal stress. So, it can be deduced from the results that the device is more affected at higher temperatures, hence failure can be propagated at these points.



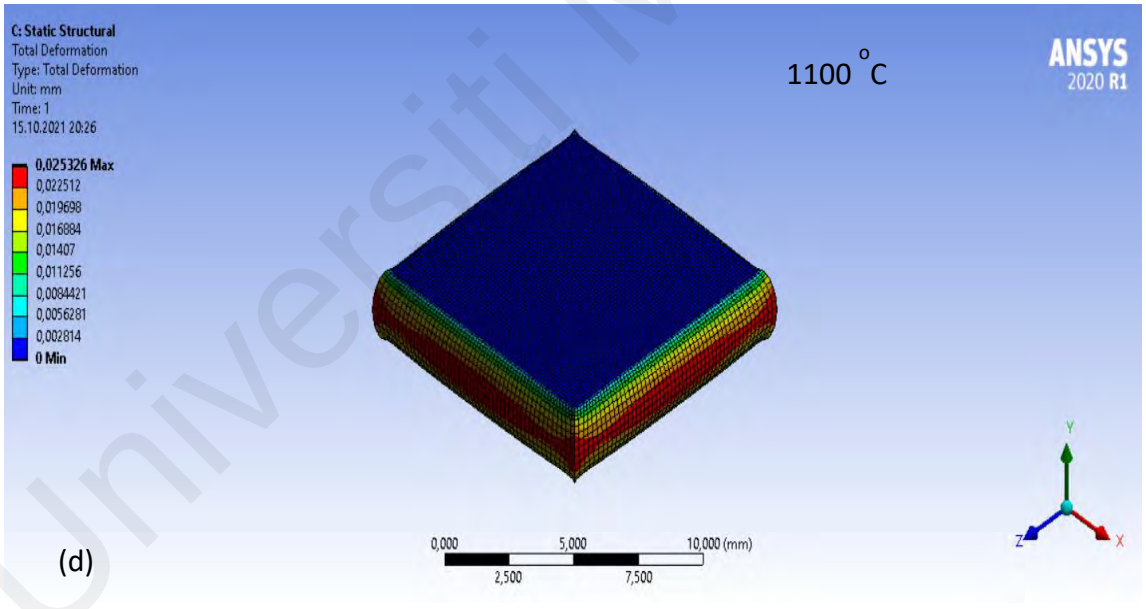
(a)



(b)



(c)



(d)

Figure 4.40: Analysis of total deformation of the SiC substrate/Ho_2O_3 gate oxide structure from 800 - 1100 ºC.

4.4.5 The Effect of Thermal Stress on Electrical Performance

The electrical properties of the dielectrics of a MOS device is strongly dependent on the physical characteristics of the nanocrystal layers and the reliability of the gate oxide (Bonafos et al., 2004; Bonafos et al., 2005). Some process parameters, such as oxide thickness, annealing regime and implantation energy also have correlation with the electrical properties. For instance, an increase in implantation energy increases the magnitude of the flat band voltage, but decreases the electric field required for effective charging (Normand et al., 2004; Bonafos et al., 2005). Previous researches have also shown that the current generated by component devices are exponentially dependent on thermal stress (T.-J. Wang et al., 2008). In order to evaluate the electrical performance of the MOS capacitor in this study, the current density of the device was measured and compared with the thermally stressed regions. It was observed that the MOS samples at higher temperatures of 1000 and 1100 ^{o}C possessed poor break down voltage and leakage current densities. This observation practically shows the adverse effect of thermal stress on the structure. According to the stress distribution model, a thermally stressed substrate will expand in volume, thereby causing a decrease in the performance of the structure (Su, Hong, & Hwu, 2002).

CHAPTER 5: CONCLUSIONS AND FUTURE RECOMMENDATIONS

5.1 Conclusions

Holmium oxide thin films have been successfully grown on SiC substrate at different temperatures, durations and oxynitridation gas flow concentrations for the formation of a metal oxide semiconductor. The effects of these variables on the structural and electrical properties of the semiconductor were studied. The optimum parameters for both thermal oxidation and oxynitridation processes were determined, and the characteristics compared. The sketch models of the oxidation and oxynitridation mechanism were developed and explicated in this thesis. Lastly, the thermodynamic stability and thermal stress reliability of the thin film in the MOS structure were also investigated. A good interfacial adhesion between the substrate and the oxide was observed.

5.1.1 Effect of Temperature on the Physical and Electrical Characteristics of Ho_2O_3 Thin Film on 4H-SiC Substrate

The effects of thermal oxidation on the structural, chemical, and electrical properties of the resulting Ho_2O_3 layers were evaluated experimentally at various temperatures from 800 – 1100 °C. The crystallinity of the Ho_2O_3 films were detected by XRD, while the other physical properties were examined by FTIR, HRTEM, and XPS analysis. The influence of the thermally deposited Ho_2O_3 gate oxide on the morphological, structural, and electrical features of the film developed by PVD on 4H-SiC was determined. The oxidized samples at 900 °C possess the smallest leakage current density and have displayed the largest electric

field. The quality of the crystals of the deposited films increased with increasing temperature of oxidation. Obvious improvements in the oxide properties, gate leakage current density, and breakdown voltage were recorded in this study. The improvements were attributed to the lower number of crystal defects due to the creation of clearly-crystallized Ho_2O_3 arrangement. The result of electrical characterization shows that thermally oxidized samples at 900 °C have the optimum electrical properties, which could be attributed to the thinnest oxide and absence of interfacial layer that was recorded at that temperature. This suggests that, the obtained high-κ Ho_2O_3 thin film is very promising, especially when it is incorporated into power devices that are based on SiC and other systems in various electronics and engineering applications.

5.1.2 Effect of Oxidation Time on the Structural and Electrical Characteristics of Ho_2O_3 Gate Oxide on 4H-SiC Substrate

The impacts of oxidation duration on the physical, and electrical characteristics of the resulting Ho_2O_3 layers were evaluated experimentally at various oxidation periods, from (5 – 20) min and constant temperature of 900 °C. The physical characteristics of the Ho_2O_3 thin film were examined by XRD, FTIR, and HRTEM. The crystallinity of the Ho_2O_3 films was identified by XRD, while crystallites size and microstrain were approximated by W-H plot. The existence of crystallized monoclinic (b)-phased Ho_2O_3 in all the samples was ascertained. The electrical properties were investigated by leakage current density–breakdown electric field, F-N tunneling and barrier height. The result of the morphology and thickness of the film shows that there is no interfacial layer (IL). The good quality of the oxide was demonstrated by the evidence of no interfacial layers detected. The samples

oxidized at 15 min duration possess the smallest leakage current density and also displayed the largest electric field with the highest barrier height value pointing towards the same direction. The quality of the crystals of the deposited films increased with increasing oxidation time. These reported characteristics suggest the suitability of Ho_2O_3 thin film as a promising dielectric candidate in microelectronics and power electronic devices.

5.1.3 Effect of O_2 and N_2 Gas Concentrations on the Physical and Electrical Characteristics of Ho_2O_3 Gate Oxide on SiC Substrate

The structural and the electrical characteristics of oxynitridated Ho_2O_3/SiC structure has been successfully investigated at different flow concentration (25 – 100 %), constant temperature of 900 °C and duration of 15 mins. The XRD and FTIR results showed the presence of Ho_2O_3 and SiO_2 compounds in all the samples, with cubic c-Ho_2O_3 and monoclinic (b)-SiO_2 crystal structures formed in between the SiC substrate and the Ho_2O_3 thin films during the thermal oxynitridation. The optimum electrical results for the Ho_2O_3/SiC structure indicates that the 50 % oxynitridation sample displays the best electrical performance. The results of the electrical characterization showed that short circuit occurred at oxynitridation of 75 %. This implies that the Ho_2O_3 dielectric film was unstable at that condition, and this may be attributed to the active reaction of N_2 in the Ho_2O_3/SiC interface. This information can help in improving on the design of high temperature MOS-based devices.

5.1.4 Comparison between Thermal Oxidation and Thermal Oxynitridation of Sputtered Ho Thin Film on SiC Substrate

In this study, the optimum parameters for the determination of the physical and electrical properties of Ho_2O_3 gate oxides under thermal oxidation and oxynitridation processes were obtained as 900 °C and 15 min for the temperature and duration, respectively. The properties were compared in terms of their physical and electrical characteristics for both thermal oxidation and oxynitridation as presented in section 4.3.3. The oxynitridated samples displayed larger breakdown field than the oxidized samples. At the same time, the oxynitridated samples also showed lower leakage current density. This may be attributed to the smoothness of the thin films on the samples' surface and the crystal orientation of the gate oxides. It was shown that the introduction of N_2 into the thermal oxidation process actually improved and enhanced the electrical properties of Ho_2O_3 thin film on 4H-SiC substrate (Hoffmann & Schmeißer, 2006; Stathis & Zafar, 2006).

5.1.5 Thermodynamic Stability and Thermal Stress Reliability of Ho_2O_3 Thin films on 4H-SiC Substrate

The thermal efficiency of semiconductor devices during operation could be hindered significantly due to thermodynamic instability and mismatch between gate oxide layer and the substrate. Therefore, it is very important to carry out the thermodynamic stability and thermal stress reliability of the dielectric layer, in order to avoid system failure. Owing to variation of temperature during thermal applicatıons, the thin film layers and substrates in complementary metal oxide semiconductor (CMOS) structures undergo high thermal stresses, which can result in large deformation and failure. Therefore, the thermal

characterization and stress analysis is necessary for reliability and durability of the structures. In this study, the distribution of heat and thermal stress between the Ho_2O_3 thin film and the SiC substrate has been simulated numerically with finite element modelling and analysis software (ANSYS). This is necessary to emulate the thermal behaviour of the structure under different thermal loadings, and for each temperature loading, the effects of thermal stress and deformation on the structure were also evaluated. Based on the results of the simulation, an optimum temperature was suggested. The thermal stability and characteristics of the thin film layer/SiC structure were evaluated and validated for better electrical performance. Finally, the thermal reliability of the gate oxide, dielectric thin film layer, as well as the SiC substrate was determined.

5.2 Significant Contribution and Limitation of the Research Work

An investigation into the use of Ho_2O_3 gate oxide as an effective dielectric on a SiC substrate was carried out at the University of Malaya for the first time. Prior to this research, several studies have been conducted in this area, but they were limited to the development of MOS capacitor, and investigation of the effects of thermal oxidation, oxynitidation, and /or post deposition annealing on the characteristics and electrical performance of the device. This research has been able to introduce an effective replacement for the long-serving SiO_2. Consequently, the potential application of the developed MOSFET has significantly improved, most especially beyond the limitations of the Si-based devices in power electronic applications. Another significant contribution of this research is the modelling and simulation of the MOS capacitor. This is the first time that the thermodynamic stability of such component will be investigated through simulation, which implies that the result obtained

from this study will serve as a baseline data for future researchers. However, the band offset and band alignment of the component could not be determined due to limited resources.

5.3 Recommendations for Future Studies

This study has shown that Ho_2O_3 has the potentials and great capabilities of replacing the native SiO_2 gate oxide in MOS applications. Based on the extent of investigation of the present research, the usefulness of its depth of understanding in terms of synthesis of Ho_2O_3 films and the effects of its preparation conditions on the properties and performance of the semiconductor device, the following recommendations are suggested for further studies:

(i) The effect of different annealing processes; such as, post deposition annealing (PDA), post oxidation annealing (POA), and rapid thermal annealing (RTA) on the Ho_2O_3 thin films for better dielectric performance can be studied.

(ii) The conduction and switching losses caused by the resistivity, contact resistance, channel width and the drift region of the semiconductor can be studied for better device performance.

(iii) The thermal dielectric relaxation current of the oxidized and oxynitridated Ho thin films can be determined by investigating the bias stimulated current process that occurs from the release of carriers in charge traps.

(iv) In order to eliminate the serious effect of V_{th} instability in SiC-based MOSFETs, there is a need to study the cause with a view to improving the performance of bias temperature instability (BTI).

REFERENCES

Abe, T., Yamagishi, Y., & Cho, Y. (2018). Visualization of traps at SiO_2/SiC interfaces near the conduction band by local deep level transient spectroscopy at low temperatures. *Japanese Journal of Applied Physics, 57*(8S1), 08NB12.

Abramowitz, M., & Davidson, M. W. (2019). Anatomy of the microscope: Introduction. *online].[cit. 2015-04-28]. Available from: http://www. olympusmicro. com/primer/anatomy/introduction. html*.

Abu-Zied, B. M., & Asiri, A. M. (2019). Genesis of nanocrystalline Ho_2O_3 via thermal decomposition of holmium acetate: Structure evolution and electrical conductivity properties. *Journal of Rare Earths, 37*(2), 185-192.

Afanas' ev, V., Stesmans, A., Bassler, M., Pensl, G., & Schulz, M. (2000). Shallow electron traps at the 4H–SiC/SiO_2 interface. *Applied physics letters, 76*(3), 336-338.

Agarwal, A., Fatima, H., Haney, S., & Ryu, S.-H. (2007). A new degradation mechanism in high-voltage SiC power MOSFETs. *IEEE Electron Device Letters, 28*(7), 587-589.

Agarwal, A. K., Seshadri, S., & Rowland, L. B. (1997). Temperature dependence of Fowler-Nordheim current in 6H and 4H-SiC MOS capacitors. *IEEE Electron Device Letters, 18*(12), 592-594.

Alshahed, M., Yu, Z., Rempp, H., Richter, H., Harendt, C., & Burghartz, J. N. (2015). Thermal characterization and modeling of ultra-thin silicon chips. *Solid-State Electronics, 113*, 121-126.

An, T., Dou, C., Ju, J., Wei, W., & Ji, Q. (2019). Microstructure, morphology, wettability and mechanical properties of Ho_2O_3 films prepared by glancing angle deposition. *Vacuum, 164*, 405-410.

Anderson, P. M., Hirth, J. P., & Lothe, J. (2017). *Theory of dislocations*: Cambridge University Press.

Ansari, S. A., Khan, M. M., Ansari, M. O., Kalathil, S., Lee, J., & Cho, M. H. (2014). Band gap engineering of CeO_2 nanostructure using an electrochemically active biofilm for visible light applications. *RSC Advances, 4*(32), 16782-16791.

Anzalone, R., Litrico, G., Piluso, N., Reitano, R., & Alberti, A. (2017). Carbonization and transition layer effects on 3C-SiC film residual stress. *Journal of Crystal Growth, 473*, 11-19.

Aranzabal, I., de Alegria, I. M., Garate, J., Andreu, J., & Delmonte, N. (2017). *Two-phase liquid cooling for electric vehicle IGBT power module thermal management.* Paper presented at the 2017 11th IEEE International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG).

Arith, F. B. (2018). *4H-SiC metal oxide semiconductor devices.* Newcastle University,

Baby, B. H., & Mohan, D. B. (2019). Structural, optical and electrical studies of DC-RF magnetron co-sputtered Cu, In & Ag doped SnS thin films for photovoltaic applications. *Solar Energy, 194*, 61-73.

Bader, S. J., Lee, H., Chaudhuri, R., Huang, S., Hickman, A., & Chowdhury, N. (2020). Prospects for wide bandgap and ultrawide bandgap CMOS devices. *IEEE Transactions on Electron Devices, 67*(10), 4010-4020.

Baliga, B. J. (2010). *Fundamentals of power semiconductor devices*: Springer Science & Business Media.

Ballestín-Fuertes, J., Muñoz-Cruzado-Alba, J., Sanz-Osorio, J. F., & Laporta-Puyal, E. (2021). Role of wide bandgap materials in power electronics for smart grids applications. *Electronics, 10*(6), 677.

Bandaru, P. (2020). New Trends in Nanoscale Electrodes and Electrochemistry: The Role of Dimensionality. In *21st Century Nanoscience–A Handbook* (pp. 24-21-24-13): CRC Press.

Baptista, A., Silva, F., Porteiro, J., Míguez, J., & Pinto, G. (2018). Sputtering physical vapour deposition (PVD) coatings: A critical review on process improvement and market trend demands. *Coatings, 8*(11), 402.

Barrero, F., & Duran, M. J. (2015). Recent advances in the design, modeling, and control of multiphase machines—Part I. *IEEE Transactions on Industrial Electronics, 63*(1), 449-458.

Barroso, J. S., Barth, N., Correia, J., Ahzi, S., & Khaleel, M. (2016). A computational analysis of coupled thermal and electrical behavior of PV panels. *Solar Energy Materials and Solar Cells, 148*, 73-86.

Bazzi, A. M. (2013). *Electric machines and energy storage technologies in EVs and HEVs for over a century.* Paper presented at the 2013 International Electric Machines & Drives Conference.

Bencherif, H., Pezzimenti, F., Dehimi, L., & Della Corte, F. (2020). Analysis of 4H-SiC MOSFET with distinct high-k/4H-SiC interfaces under high temperature and carrier-trapping conditions. *Applied Physics A, 126*(11), 1-11.

Bhanu, J. U., Babu, G. R., & Thangadurai, P. (2019). Influence of Mg ion concentration in ZrO_2 gate dielectric layered silicon based MOS capacitors for memory applications: Thorough understanding of conduction processes. *Materials science in semiconductor processing, 89*, 85-96.

Bhattacharya, P., Fornari, R., & Kamimura, H. (2011). *Comprehensive semiconductor science and technology*: Newnes.

Biela, J., Schweizer, M., Waffler, S., & Kolar, J. W. (2010). SiC versus Si—Evaluation of potentials for performance improvement of inverter and DC–DC converter systems by SiC power semiconductors. *IEEE Transactions on Industrial Electronics, 58*(7), 2872-2882.

Biggerstaff, T., Reynolds Jr, C., Zheleva, T., Lelis, A., Habersat, D., & Duscher, G. (2009). Relationship between 4H-SiC/SiO_2 transition layer thickness and mobility. *Applied physics letters, 95*(3), 032108.

Blat, C., Nicollian, E., & Poindexter, E. (1991). Mechanism of negative-bias-temperature instability. *Journal of Applied Physics, 69*(3), 1712-1720.

Bohr, M. T., & Young, I. A. (2017). CMOS scaling trends and beyond. *IEEE Micro, 37*(6), 20-29.

Boiler, A. (2013). *Rules for Construction of Pressure vessels*: American Society of Mechanical Engineers New York.

Bojoi, R., Cavagnino, A., Tenconi, A., Tessarolo, A., & Vaschetto, S. (2015). *Multiphase electrical machines and drives in the transportation electrification.* Paper presented at the 2015 IEEE

1st International Forum on Research and Technologies for Society and Industry Leveraging a better tomorrow (RTSI).

Boldea, I., Tutelea, L. N., Parsa, L., & Dorrell, D. (2014). Automotive electric propulsion systems with reduced or no permanent magnets: An overview. *IEEE Transactions on Industrial Electronics, 61*(10), 5696-5711.

Bonafos, C., Cherkashin, N., Carrada, M., Coffin, H., Assayag, G. B., & Fanciulli, M. (2004). Manipulation of 2D arrays of Si nanocrystals by ultra-low-energy ion beam-synthesis for nonvolatile memories applications. *MRS Online Proceedings Library (OPL), 830*.

Bonafos, C., Coffin, H., Schamm, S., Cherkashin, N., Assayag, G. B., & Claverie, A. (2005). Si nanocrystals by ultra-low-energy ion beam-synthesis for non-volatile memory applications. *Solid-State Electronics, 49*(11), 1734-1744.

Bondyopadhyay, P. K. (1998). Moore's law governs the silicon revolution. *Proceedings of the IEEE, 86*(1), 78-81.

Bose, B. K. (2010). Global warming: Energy, environmental pollution, and the impact of power electronics. *IEEE Industrial Electronics Magazine, 4*(1), 6-17.

Burress, T. (2014). Benchmarking EV and HEV technologies. *Oak Ridge National Laboratory*.

Buttay, C., Planson, D., Allard, B., Bergogne, D., Bevilacqua, P., & Joubert, C. (2011). State of the art of high temperature power electronics. *Materials Science and Engineering: B, 176*(4), 283-288.

Cabello, M., Soler, V., Rius, G., Montserrat, J., Rebollo, J., & Godignon, P. (2018). Advanced processing for mobility improvement in 4H-SiC MOSFETs: A review. *Materials science in semiconductor processing, 78*, 22-31.

Calusine, G., Politi, A., & Awschalom, D. D. (2016). Cavity-enhanced measurements of defect spins in silicon carbide. *Physical Review Applied, 6*(1), 014019.

Casados-Cruz, G., Reyes-Barranca, M., & Moreno-Cadenas, J. (2011). A simple method for determination of Fowler–Nordheim tunnelling parameters. *International journal of electronics, 98*(5), 655-666.

Casady, J., & Johnson, R. W. (1996). Status of silicon carbide (SiC) as a wide bandgap semiconductor for high-temperature applications: A review. *Solid-State Electronics, 39*(10), 1409-1422.

Casady, J., Olejniczak, K., McNutt, T., Simco, D., Passmore, B., & Palmour, J. (2017). *88 kilowatt automotive inverter with new 900 volt silicon carbide MOSFET technology*. Retrieved from

Castan, H., Garcia, H., Duenas, S., Bailon, L., Miranda, E., & Leskelä, M. (2015). Conduction and stability of holmium titanium oxide thin films grown by atomic layer deposition. *Thin Solid Films, 591*, 55-59.

Casu, M. B. (2018). Nanoscale studies of organic radicals: surface, interface, and spinterface. *Accounts of chemical research, 51*(3), 753-760.

Chan, C. W. (2018). *Design, simulation and analysis of RESURF Si/SiC power LDMOSFETs.* University of Warwick,

Chanana, R. K. (2019). High density of deep acceptor traps near the 4H-SiC conduction band limits surface mobility and dielectric breakdown field in an n-channel 4H-SiC MOSFET. *IOSR-JEEE, 14*(4), 1-8.

Chang, C.-L., Ho, C.-T., Chen, P.-H., Chen, W.-C., Wang, D.-Y., & Wu, W.-Y. (2018). Synergetic effect for improved deposition of titanium nitride films. *Surface and Coatings Technology, 350*, 1098-1104.

Chang, K., Nuhfer, N., Porter, L., & Wahab, Q. (2000). High-carbon concentrations at the silicon dioxide–silicon carbide interface identified by electron energy loss spectroscopy. *Applied physics letters, 77*(14), 2186-2188.

Chang, P., & Hwu, J. (2018). Electrical characterization of 4H-SiC metal–oxide–semiconductor structure with Al_2O_3 stacking layers as dielectric. *Applied Physics A, 124*(2), 87.

Chatterjee, B., Leach, J. H., Dhar, S., & Choi, S. (2018). *Temperature and Stress Metrology of Ultra-Wide Bandgap β-Ga_2O_3 Thin Films.* Paper presented at the 2018 17th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm).

Chen, F.-H., Hung, M.-N., Yang, J.-F., Kuo, S.-Y., & Pan, T.-M. (2013). Effect of surface roughness on electrical characteristics in amorphous In GaZnO thin-film transistors with high-κ Sm_2O_3 dielectrics. *Journal of Physics and Chemistry of Solids, 74*(4), 570-574.

Chen, H.-C., Jan, D.-J., Lin, J.-H., & Wang, M.-C. (2019). Electrochromic, optical and binding-energy performances of Tantalum Pentoxide and Zirconium dioxide films deposited with RF magnetron sputtering and cathodic arc plasma. *Solar Energy Materials and Solar Cells, 203*, 110158.

Chen, J., Du, X., Luo, Q., Zhang, X., Sun, P., & Zhou, L. (2020). A review of switching oscillations of wide bandgap semiconductor devices. *IEEE Transactions on Power Electronics, 35*(12), 13182-13199.

Cheng, S., Sang, L., Liao, M., Liu, J., Imura, M., & Li, H. (2012). Integration of high-dielectric constant Ta_2O_5 oxides on diamond for power devices. *Applied physics letters, 101*(23), 232907.

Cheng, S., Sang, L., Liao, M., Liu, J., & Koide, Y. (2012). Integration of high-dielectric constant Ta_2O_5 oxides on diamond for power devices. *Applied physics letters, 101*(23), 232907.

Chin, W. C., Cheong, K. Y., & Hassan, Z. (2010). Sm_2O_3 gate dielectric on Si substrate. *Materials science in semiconductor processing, 13*(5-6), 303-314.

Chiou, Y., Gambino, J., & Mohammad, M. (2001). Determination of the Fowler–Nordheim tunneling parameters from the Fowler–Nordheim plot. *Solid-State Electronics, 45*(10), 1787-1791.

Cho, Y. J., & Lu, K. (2020). High temperature oxidation behaviors of bulk SiC with low partial pressures of air and water vapor in argon. *Corrosion Science, 174*, 108795.

Choi, G., Yoon, H. H., Jung, S., Jeon, Y., & Lee, J. Y. (2015). Schottky barrier modulation of metal/4H-SiC junction with thin interface spacer driven by surface polarization charge on 4H-SiC substrate. *Applied physics letters, 107*(25), 252101.

Choi, H. (2016). Overview of silicon carbide power devices. *Fairchild semiconductor*.

Choyke, W. J., Matsunami, H., & Pensl, G. (2013). *Silicon carbide: recent major advances*: Springer Science & Business Media.

Chung, G., Tin, C., & Williams, J. (2000). K. McDonald, M. Di Ventra, ST Pantelides, LC Fledman, and RA Weller. Effect of nitric oxide annealing on the interface trap densities near the band edges in the 4H polytype of silicon carbide. *Appl. Phys. Lett, 76*, 1713.

Clark, R. D. (2014). Emerging applications for high k materials in VLSI technology. *Materials, 7*(4), 2913-2944.

Constant, A., Camara, N., Montserrat, J., Pausas, E., Camassel, J., & Godignon, P. (2011). *Oxidation process by RTP for 4H-SiC MOSFET gate fabrication.* Paper presented at the Materials Science Forum.

Constantinescu, C., Ion, V., Galca, A. C., & Dinescu, M. (2012). Morphological, optical and electrical properties of samarium oxide thin films. *Thin Solid Films, 520*(20), 6393-6397.

Cougo, B., Sathler, H., Riva, R., Dos Santos, V., Nicolas, R., & Sareni, B. (2020). Characterization of low inductance SiC module with integrated capacitors for aircraft applications requiring low losses and low EMI issues. *IEEE Transactions on Power Electronics*.

Crawford, J. H., & Slifkin, L. M. (2013). *Point Defects in Solids: General and ionic crystals*: Springer Science & Business Media.

Damianos, D., Vitrant, G., Kaminski-Cachopo, A., Blanc-Pélissier, D., Ghibaudo, G., & Lei, M. (2018). Field-effect passivation of Si by ALD-Al_2O_3: second harmonic generation monitoring and simulation. *Journal of Applied Physics, 124*(12), 125309.

Dang, V. S., Parala, H., Kim, J. H., Xu, K., Srinivasan, N. B., & Edengeiser, E. (2014). Electrical and optical properties of TiO_2 thin films prepared by plasma-enhanced atomic layer deposition. *physica status solidi (a), 211*(2), 416-424.

Danno, K., Nakamura, D., & Kimoto, T. (2007). Investigation of carrier lifetime in 4H-SiC epilayers and lifetime control by electron irradiation. *Applied physics letters, 90*(20), 202109.

de la Rosa, L. S., Portillo, M. C., Mora-Ramírez, M., Téllez, V. C., & Moreno, O. P. (2020). Synthesis of holmium oxide (Ho_2O_3) nanocrystal by chemical bath deposition. *Optik*, 164875.

de Urquijo-Ventura, M., Rao, M. S., Meraz-Davila, S., Torres-Ochoa, J., Quevedo-Lopez, M., & Ramirez-Bon, R. (2020). PVP-SiO_2 and PVP-TiO_2 hybrid films for dielectric gate applications in CdS-based thin film transistors. *Polymer, 191*, 122261.

Degraeve, R., Groeseneken, G., Bellens, R., Ogier, J. L., & Maes, H. E. (1998). New insights in the relation between electron trap generation and the statistical properties of oxide breakdown. *IEEE Transactions on Electron Devices, 45*(4), 904-911.

Deng, Q., Wilkie, C., Moore, R., & Mauritz, K. A. (1998). TGA–FTIR investigation of the thermal degradation of Nafion® and Nafion®/[silicon oxide]-based nanocomposites. *Polymer, 39*(24), 5961-5972.

Dhar, S., Ryu, S.-H., & Agarwal, A. K. (2010). A study on pre-oxidation nitrogen implantation for the improvement of channel mobility in 4H-SiC MOSFETs. *IEEE Transactions on Electron Devices, 57*(6), 1195-1200.

Dhar, S., Wang, S., Williams, J. R., Pantelides, S. T., & Feldman, L. C. (2005). Interface passivation for silicon dioxide layers on silicon carbide. *Mrs Bulletin, 30*(4), 288-292.

Dimitrijev, S., Han, J., Moghadam, H. A., & Aminbeidokhti, A. (2015). Power-switching applications beyond silicon: Status and future prospects of SiC and GaN devices. *Mrs Bulletin, 40*(5), 399-405.

Dunand, D., & Mortensen, A. (1991). On plastic relaxation of thermal stresses in reinforced metals. *Acta metallurgica et materialia, 39*(2), 127-139.

Duran, M. J., & Barrero, F. (2015). Recent advances in the design, modeling, and control of multiphase machines—Part II. *IEEE Transactions on Industrial Electronics, 63*(1), 459-468.

Dushaq, G., Rasras, M., & Nayfeh, A. (2017). Germanium MOS capacitors grown on Silicon using low temperature RF-PECVD. *Journal of Physics D: Applied Physics, 50*(40), 405107.

Engström, O., Raeissi, B., Hall, S., Buiu, O., Lemme, M. C., & Cherkaoui, K. (2007). Navigation aids in the search for future high-k dielectrics: Physical and electrical trends. *Solid-State Electronics, 51*(4), 622-626.

Eriksson, G. J. P. (2011). *Transport properties at 3C-SiC interfaces.* Universita'degli Studi di Catania,

Esro, M., Kolosov, O., Jones, P. J., Milne, W. I., & Adamopoulos, G. (2017). Structural and electrical characterization of SiO_2 gate dielectrics deposited from solutions at moderate temperatures in air. *ACS applied materials & interfaces, 9*(1), 529-536.

Esteve, R. (2011). *Fabrication and Characterization of 3C-and 4H-SiC MOSFETs.* KTH Royal Institute of Technology,

Esteve, R., Schöner, A., Reshanov, S., Zetterling, C.-M., & Nagasawa, H. (2009). Advanced oxidation process combining oxide deposition and short postoxidation step for N-type 3C- and 4H-SiC. *Journal of Applied Physics, 106*(4), 044514.

Fadley, C. S. (2010). X-ray photoelectron spectroscopy: Progress and perspectives. *Journal of Electron Spectroscopy and Related Phenomena, 178*, 2-32.

Fei, C., Bai, S., Wang, Q., & Huang, R. (2020). Influences of pre-oxidation nitrogen implantation and post-oxidation annealing on channel mobility of 4H-SiC MOSFETs. *Journal of Crystal Growth, 531*, 125338.

Finken, T., Hombitzer, M., & Hameyer, K. (2010). *Study and comparison of several permanent-magnet excited rotor types regarding their applicability in electric vehicles.* Paper presented at the 2010 Emobility-Electrical Power Train.

Fiorenza, P., Giannazzo, F., & Roccaforte, F. (2019). Characterization of SiO_2/4H-SiC interfaces in 4H-SiC MOSFETs: a review. *Energies, 12*(12), 2310.

Fischer, H.-M., & Dorn, L. (2013). Voltage classes for electric mobility. *ZVEI-German Electr. and Electron. Manufacturers' Association*.

Fleetwood, D. M. (2013). Total ionizing dose effects in MOS and low-dose-rate-sensitive linear-bipolar devices. *IEEE Transactions on Nuclear Science, 60*(3), 1706-1730.

Forbes, R. G. (1999a). Field emission: New theory for the derivation of emission area from a Fowler–Nordheim plot. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, 17*(2), 526-533.

Forbes, R. G. (1999b). Refining the application of Fowler–Nordheim theory. *Ultramicroscopy, 79*(1-4), 11-23.

Forbes, R. G., & Deane, J. H. (2007). Reformulation of the standard theory of Fowler–Nordheim tunnelling and cold field electron emission. *Proceedings of the Royal Society A: Mathematical, Physical and Engineering Sciences, 463*(2087), 2907-2927.

Franquelo, L. G., Rodriguez, J., Leon, J. I., Kouro, S., Portillo, R., & Prats, M. A. (2008). The age of multilevel converters arrives. *IEEE Industrial Electronics Magazine, 2*(2), 28-39.

Fu, W. (2020). Study of biaxial stress effect on electronic properties at the 4H-SiC-MOS interface.

Fung, C., & Kopanski, J. (1984). Thermal oxidation of 3C silicon carbide single-crystal layers on silicon. *Applied physics letters, 45*(7), 757-759.

Gao, F., & Weber, W. J. (2003). Recovery of close Frenkel pairs produced by low energy recoils in SiC. *Journal of Applied Physics, 94*(7), 4348-4356.

Gao, H. (2019). Understanding the growth of III-V semiconductor nanowires with component addition in metal-organic chemical vapor deposition. https://doi.org/10.14264/uql.2020.79.

Gao, J., He, G., Sun, Z., Chen, H., & Liu, M. (2016). Modification of electrical properties and carrier transportation mechanism of ALD-derived HfO_2/Si gate stacks by Al_2O_3 incorporation. *Journal of alloys and compounds, 667*, 352-358.

Gibson, J., & Lanzerotti, M. (1989). Observation of interfacial atomic steps during silicon oxidation. *Nature, 340*(6229), 128-131.

Gillen, R., & Robertson, J. (2013). Electronic structure of lanthanide oxide high-K gate oxides. *Microelectronic engineering, 109*, 72-74.

Goh, K. H. (2017). *Samarium oxide and samarium oxynitride thin film gate oxides on silicon substrate/Goh Kian Heng.* University of Malaya,

Goh, K. H., Haseeb, A., & Wong, Y. H. (2016a). Effect of oxidation temperature on physical and electrical properties of Sm_2O_3 thin-film gate oxide on Si substrate. *Journal of Electronic Materials, 45*(10), 5302-5312.

Goh, K. H., Haseeb, A., & Wong, Y. H. (2016b). Physical and electrical properties of thermal oxidized Sm_2O_3 gate oxide thin film on Si substrate: Influence of oxidation durations. *Thin Solid Films, 606*, 80-86.

Goh, K. H., Haseeb, A., & Wong, Y. H. (2017). Trap-assisted tunneling, capacitance–voltage characteristics, and surface properties of Sm_2O_3 thin film on Si substrate. *Journal of Materials Science: Materials in Electronics, 28*(6), 4725-4731.

Golosov, D., Vilya, N., Zavadski, S., Melnikov, S., & Komissarov, I. (2019). Influence of film thickness on the dielectric characteristics of hafnium oxide layers. *Thin Solid Films, 690*, 137517.

Gordon, I., Dross, F., Depauw, V., Masolin, A., & Poortmans, J. (2011). Three novel ways of making thin-film crystalline-silicon layers on glass for solar cell applications. *Solar Energy Materials and Solar Cells, 95*, S2-S7.

Götsch, T., Wernig, E.-M., Klötzer, B., Schachinger, T., Kunze-Liebhäuser, J., & Penner, S. (2019). An ultra-flexible modular high vacuum setup for thin film deposition. *Review of Scientific Instruments, 90*(2), 023902.

Graniel, O., Weber, M., Balme, S., Miele, P., & Bechelany, M. (2018). Atomic layer deposition for biosensing applications. *Biosensors and Bioelectronics, 122*, 147-159.

Granqvist, C. G. (2014). Electrochromics for smart windows: Oxide-based thin films and devices. *Thin Solid Films, 564*, 1-38.

Green, R., Lelis, A., & Habersat, D. (2016). Threshold-voltage bias-temperature instability in commercially-available SiC MOSFETs. *Japanese Journal of Applied Physics, 55*(4S), 04EA03.

Groothuis, S., Schroen, W., & Murtuza, M. (1985). *Computer aided stress modeling for optimizing plastic package reliability.* Paper presented at the 23rd International Reliability Physics Symposium.

Gullu, H., & Yildiz, D. (2020). Temperature and frequency effects on electrical and dielectric properties of n-4H-SiC based metal–insulator-semiconductor (MIS) diode interlayered with Si_3N_4 thin film. *Journal of Materials Science: Materials in Electronics, 31*(11), 8705-8717.

Guo, H., Yang, X., Xu, Q., Lu, W., Li, J., & Li, S. (2020). Epitaxial growth and electrical performance of graphene/3C–SiC films by laser CVD. *Journal of alloys and compounds, 826*, 154198.

Guo, X., Xun, Q., Li, Z., & Du, S. (2019). Silicon carbide converters and MEMS devices for high-temperature power electronics: A critical review. *Micromachines, 10*(6), 406.

Gusev, E., Cabral, C., Under, B., Kim, Y., & Maitra, K. (2004). *Advanced gate stacks with fully silicided (FUSI) gates and high-/spl kappa/dielectrics: Enhanced performance at reduced gate leakage.* Paper presented at the IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004.

Hall, W. (1949). X-ray line broadening in metals. *Proceedings of the Physical Society. Section A, 62*(11), 741.

Harishsenthil, P., Chandrasekaran, J., Marnadu, R., Balraju, P., & Mahendarn, C. (2020). Influence of high dielectric HfO_2 thin films on the electrical properties of Al/HfO_2/n-Si (MIS) structured Schottky barrier diodes. *Physica B: Condensed Matter, 594*, 412336.

Hazra, S., De, A., Cheng, L., Palmour, J., & Bhattacharya, S. (2015). High switching performance of 1700-V, 50-A SiC power MOSFET over Si IGBT/BiMOSFET for advanced power conversion applications. *IEEE Transactions on Power Electronics, 31*(7), 4742-4754.

He, G., Zhu, L., Sun, Z., Wan, Q., & Zhang, L. (2011). Integrations and challenges of novel high-k gate stacks in advanced CMOS technology. *Progress in Materials Science, 56*(5), 475-572.

Hecht, D. S., Hu, L., & Irvin, G. (2011). Emerging transparent electrodes based on thin films of carbon nanotubes, graphene, and metallic nanostructures. *Advanced materials, 23*(13), 1482-1513.

Heiba, Z. K., & Mohamed, M. B. (2015). Structural and magnetic properties of Mn doped Ho_2O_3 nanocrystalline. *Journal of Molecular Structure, 1102*, 135-140.

Herrmann, M., Förter-Barth, U., Kempa, P. B., & Kroeber, H. (2009). Particle Characterization by X-Ray Powder Diffraction. *Chemical Engineering & Technology: Industrial Chemistry-Plant Equipment-Process Engineering-Biotechnology, 32*(7), 1067-1072.

Hetherin, K., Ramesh, S., & Wong, Y. H. (2017a). Effects of thermal oxidation duration on the structural and electrical properties of Nd_2O_3/Si system. *Applied Physics A, 123*(8), 1-11.

Hetherin, K., Ramesh, S., & Wong, Y. H. (2017b). Formation of neodymium oxide by thermal oxidation of sputtered Nd thin film on Si substrate. *Journal of Materials Science: Materials in Electronics, 28*(16), 11994-12003.

Himpsel, F., McFeely, F., Taleb-Ibrahimi, A., Yarmoff, J., & Hollinger, G. (1988). Microscopic structure of the SiO_2/Si interface. *Physical review B, 38*(9), 6084.

Hirose, K., Sakano, K., Takahashi, K., & Hattori, T. (2002). Characterization of SiO_2/Si interfaces by using X-ray photoelectron spectroscopy time-dependent measurement. *Surface science, 507*, 906-910.

Hlali, S., Hizem, N., & Kalboussi, A. (2016). High-k dielectric materials for the gate oxide of a MIS capacitor: effect of interface states on the C–V characteristics. *Journal of Computational Electronics, 15*(4), 1340-1350.

Hoffmann, P., & Schmeißer, D. (2006). Improvement of nitrogen incorporation into oxynitrides on 4H-SiC (0001). *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, 246*(1), 85-89.

Hoskins, A. L., Coffey, A. H., Musgrave, C. B., & Weimer, A. W. (2018). Nanostructured mullite steam oxidation resistant coatings for silicon carbide deposited via atomic layer deposition. *Journal of the American Ceramic Society, 101*(6), 2493-2505.

Hoskins, A. L., Gossett, T. A., Musgrave, C. B., & Weimer, A. W. (2019). The effect of ultrathin ALD films on the oxidation kinetics of SiC in high-temperature steam. *Chemical Engineering Science, 201*, 230-236.

Hosoi, T., Harada, M., Kagei, Y., Watanabe, Y., Shimura, T., & Watanabe, H. (2009). *AlON/SiO_2 stacked gate dielectrics for 4H-SiC MIS devices.* Paper presented at the Materials Science Forum.

Hosoi, T., Kagei, Y., Kirino, T., Mitani, S., Nakano, Y., & Watanabe, H. (2011). *Reduction of Charge Trapping Sites in Al_2O_3/SiO_2 Stacked Gate Dielectrics by Incorporating Nitrogen for Highly Reliable 4H-SiC MIS Devices.* Paper presented at the Materials Science Forum.

Hosoi, T., Kagei, Y., Kirino, T., Watanabe, Y., Kozono, K., & Watanabe, H. (2010). *Improved characteristics of 4H-SiC MISFET with AlON/nitrided SiO_2 stacked gate dielectrics.* Paper presented at the Materials Science Forum.

Hourdakis, E., & Nassiopoulou, A. G. (2020). Microcapacitors for Energy Storage: General Characteristics and Overview of Recent Progress. *physica status solidi (a), 217*(10), 1900950.

Houston Dycus, J., Xu, W., Lichtenwalner, D. J., Hull, B., Palmour, J. W., & LeBeau, J. M. (2016). Structure and chemistry of passivated SiC/SiO_2 interfaces. *Applied physics letters, 108*(20), 201607.

Huang, A. Q. (2019). Power semiconductor devices for smart grid and renewable energy systems. *Power Electronics in Renewable Energy Systems and Smart Grid: Technology and Applications*, 85-152.

Huang, C.-Y., Bao, X., Ye, Z., Lee, S., Chiang, H., & Stemmer, S. (2015). *Ultrathin InAs-channel MOSFETs on Si substrates.* Paper presented at the 2015 International Symposium on VLSI Technology, Systems and Applications.

Huang, L., Liu, Y., Xiao, C., Ding, Y., & Peng, X. (2021). Characterization of Al_2O_3/$LaAlO_3$/SiO_2 Gate Stack on 4H-SiC After Post-Deposition Annealing. *IEEE Transactions on Electron Devices, 68*(4), 2133-2137.

Idris, M. I., & Horsfall, A. B. (2020). *Surface Treatment of 4H-SiC MOSFETs Prior to Al_2O_3 Deposition.* Paper presented at the Materials Science Forum.

Ikeda, N., Kaya, S., Li, J., Sato, Y., Kato, S., & Yoshida, S. (2008). *High power AlGaN/GaN HFET with a high breakdown voltage of over 1.8 kV on 4 inch Si substrates and the suppression of current collapse.* Paper presented at the 2008 20th International Symposium on Power Semiconductor Devices and IC's.

Inoue, Y., Morimoto, S., & Sanada, M. (2013). Control scheme for wide-speed-range operation of synchronous reluctance motor in MT frame synchronized with stator flux linkage. *IEEJ Journal of Industry Applications, 2*(2), 98-105.

Iqbal, A., Walker, G., Hold, L., Fernandes, A., & Mohd-Yasin, F. (2018). The sputtering of AlN films on top of on-and off-axis 3C-SiC (111)/Si (111) substrates at various substrate temperatures. *Journal of Materials Science: Materials in Electronics, 29*(3), 2434-2446.

Ismail, R. (2015). *Novel device architectures and carbon based materials for future nanoelectronics.* Paper presented at the 2015 2nd International Conference on Information Technology, Computer, and Electrical Engineering (ICITACEE).

Jamet, P., Dimitrijev, S., & Tanner, P. (2001). Effects of nitridation in gate oxides grown on 4H-SiC. *Journal of Applied Physics, 90*(10), 5058-5063.

Jaramillo, R., Ha, S. D., Silevitch, D., & Ramanathan, S. (2014). Origins of bad metal conductivity and the insulator–metal transition in the rare-earth nickelates. *Nature Physics, 10*(4), 304-307.

Jena, S., Tokas, R., Thakur, S., & Sahoo, N. (2016). Optical properties of electron beam evaporated ZrO_2: 10% SiO_2 thin films: dependence on structure. *Indian Journal of Physics, 90*(8), 951-957.

Jeon, S., Im, K., Yang, H., Lee, H., & Hwang, H. (2001). *Excellent electrical characteristics of lanthanide (Pr, Nd, Sm, Gd, and Dy) oxide and lanthanide-doped oxide for MOS gate dielectric applications.* Paper presented at the International Electron Devices Meeting. Technical Digest (Cat. No. 01CH37224).

Jia, Q., Huang, K., You, T., Yi, A., & Lin, J. (2018). Free standing ultrathin single-crystalline SiC substrate by MeV H ion-slicing. *Applied physics letters, 112*(19), 192102.

Jia, Y., Jiang, Q., Sun, H., Liu, P., Hu, D., & Pei, Y. (2021). Wearable Thermoelectric Materials and Devices for Self-Powered Electronic Systems. *Advanced materials, 33*(42), 2102990.

Jia, Y., Lv, H., Song, Q., Tang, X., & Xiao, L. (2017). Influence of oxidation temperature on the interfacial properties of n-type 4H-SiC MOS capacitors. *Applied Surface Science, 397*, 175-182.

Jiang, L., & Cheung, R. (2009). A review of silicon carbide development in MEMS applications. *International Journal of Computational Materials Science and Surface Engineering, 2*(3-4), 227-242.

Jiang, X., Zhai, D., Chen, J., Yuan, F., & Wang, J. (2018). *Comparison study of surge current capability of body diode of SiC MOSFET and SiC Schottky diode.* Paper presented at the 2018 IEEE Energy Conversion Congress and Exposition (ECCE).

Jung, C. (2017). Power Up with 800-V Systems: The benefits of upgrading voltage power for battery-electric passenger vehicles. *IEEE Electrification Magazine, 5*(1), 53-58.

Jung, S.-Y., Hong, J., & Nam, K. (2013). Current minimizing torque control of the IPMSM using Ferrari's method. *IEEE Transactions on Power Electronics, 28*(12), 5603-5617.

Junping, W., Jingang, G., & Lei, D. (2009). An adaptive Kalman filtering based State of Charge combined estimator for electric vehicle battery pack. *Energy Conversion and Management, 50*(12), 3182-3186.

Kageshima, H., Shiraishi, K., & Endoh, T. (2018). Reconsideration of Si pillar thermal oxidation mechanism. *Japanese Journal of Applied Physics, 57*(6S3), 06KD02.

Kalkan, S. B., Yanilmaz, A., & Çelebi, C. (2019). Impact of encapsulation method on the adsorbate induced electrical instability of monolayer graphene. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 37*(5), 051502.

Kamata, Y. (2008). High-k/Ge MOSFETs for future nanoelectronics. *Materials today, 11*(1-2), 30-38.

Kang, J.-H., Jung, Y. C., Seong, S., Lee, T., & Ahn, J. (2017). Structural, chemical, and electrical properties of Y_2O_3 thin films grown by atomic layer deposition with an (iPrCp) 2Y (iPr-amd) precursor. *Materials science in semiconductor processing, 63*, 279-284.

Katsikini, M. (2015). Wide Band Gap Materials. In *X-Ray Absorption Spectroscopy of Semiconductors* (pp. 49-76): Springer.

Kaya, S., Yilmaz, E., Kahraman, A., & Karacali, H. (2015). Frequency dependent gamma-ray irradiation response of Sm_2O_3 MOS capacitors. *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, 358*, 188-193.

Kaya, S., Yilmaz, E., Karacali, H., Cetinkaya, A., & Aktag, A. (2015). Samarium oxide thin films deposited by reactive sputtering: effects of sputtering power and substrate temperature on microstructure, morphology and electrical properties. *Materials science in semiconductor processing, 33*, 42-48.

Kerler, M., Burda, P., Baumann, M., & Lienkamp, M. (2014). *A concept of a high-energy, low-voltage EV battery pack.* Paper presented at the 2014 IEEE International Electric Vehicle Conference (IEVC).

Khosa, R. Y., Chen, J.-T., Winters, M., Pálsson, K., Karhu, R., & Sveinbjörnsson, E. (2019). Electrical characterization of high k-dielectrics for 4H-SiC MIS devices. *Materials science in semiconductor processing, 98*, 55-58.

Kibasomba, P. M., Dhlamini, S., Maaza, M., & Liu, C.-P. (2018). Strain and grain size of TiO_2 nanoparticles from TEM, Raman spectroscopy and XRD: the revisiting of the Williamson-Hall plot method. *Results in Physics, 9*, 628-635.

Kibasomba, P. M., Dhlamini, S., Maaza, M., Liu, C.-P., & Rashad, M. M. (2018). Strain and grain size of TiO_2 nanoparticles from TEM, Raman spectroscopy and XRD: the revisiting of the Williamson-Hall plot method. *Results in Physics, 9*, 628-635.

Kim, D. G., Kim, H.-R., Kwon, D. S., Lim, J., & Seo, H. (2021). Comparison of high-k Y_2O_3/TiO_2 bilayer and Y-doped TiO_2 thin films on Ge substrate. *Journal of Physics D: Applied Physics, 54*(18), 185110.

Kim, H., Chen, H., Zhu, J., Maksimović, D., & Erickson, R. (2016). *Impact of 1.2 kV SiC-MOSFET EV traction inverter on urban driving.* Paper presented at the 2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA).

Kim, M., Seo, J.-H., Singisetti, U., & Ma, Z. (2017). Recent advances in free-standing single crystalline wide band-gap semiconductors and their applications: GaN, SiC, ZnO, β-Ga_2O_3, and diamond. *Journal of Materials Chemistry C, 5*(33), 8338-8354.

Kimoto, T. (2015). Material science and device physics in SiC technology for high-voltage power devices. *Japanese Journal of Applied Physics, 54*(4), 040103.

Kimoto, T., & Cooper, J. A. (2014). *Fundamentals of silicon carbide technology: growth, characterization, devices and applications*: John Wiley & Sons.

Kimoto, T., Kanzaki, Y., Noborio, M., Kawano, H., & Matsunami, H. (2005). Interface properties of metal–oxide–semiconductor structures on 4H-SiC {0001} and (1120) formed by N_2O oxidation. *Japanese Journal of Applied Physics, 44*(3R), 1213.

Kodigala, S. R., Chattopadhyay, S., Overton, C., Ardoin, I., & Gordon, B. (2015). Growth and surface analysis of SiO_2 on 4H-SiC for MOS devices. *Applied Surface Science, 330*, 465-475.

Kong, X., Wang, M., Wang, B., Zheng, Y., & Yang, L. (2019). Thermal mismatch stress relaxation and dislocation transformation of 45 % SiCp/Al composites by continuous diode laser heating. *Applied Physics A, 125*(9), 1-10.

Koryakin, A., Kukushkin, S., & Redkov, A. (2017). Nucleation and Growth Mechanisms of Cdte Thin Films on Silicon Substrates with Silicon Carbide Buffer Layers. *Materials Physics & Mechanics, 32*(3).

Kosugi, R., Umeda, T., & Sakuma, Y. (2011). Fixed nitrogen atoms in the SiO_2/SiC interface region and their direct relationship to interface trap density. *Applied physics letters, 99*(18), 182111.

Kouakou, P., Yoboue, P., Ouattara, B., Hody, V., Choquet, P., & Belmahi, M. (2017). Silicon Carbon Nitride Thin Films Produced by Magnetron Reactive Sputtering Physical Vapour Deposition: Structural, Chemical and Mechanical Characterisation. *Journal of Surface Science and Technology, 33*(1-2), 44-52.

Kozono, K., Hosoi, T., Kagei, Y., Kirino, T., Mitani, S., & Watanabe, H. (2010). *Direct observation of dielectric breakdown spot in thermal oxides on 4H-SiC (0001) using conductive atomic force microscopy.* Paper presented at the Materials Science Forum.

Krsmanovic, M., Biswas, D., Ali, H., Kumar, A., Ghosh, R., & Dickerson, A. K. (2020). Hydrodynamics and surface properties influence biofilm proliferation. *Advances in Colloid and Interface Science*, 102336.

Kukli, K., Kemell, M., Dimri, M. C., Puukilainen, E., & Leskelä, M. (2014). Holmium titanium oxide thin films grown by atomic layer deposition. *Thin Solid Films, 565*, 261-266.

Kurniawan, T., Cheong, K. Y., Razak, K. A., Lockman, Z., & Ahmad, N. (2011). Oxidation of sputtered Zr thin film on Si substrate. *Journal of Materials Science: Materials in Electronics, 22*(2), 143-150.

Kurniawan, T., Wong, Y. H., Cheong, K. Y., Moon, J. H., & Bahng, W. (2011). Effects of post-oxidation annealing temperature on ZrO_2 thin film deposited on 4H-SiC substrate. *Materials science in semiconductor processing, 14*(1), 13-17.

La Via, F., Roccaforte, F., La Magna, A., Nipoti, R., Mancarella, F., & Miglio, L. (2018). *3C-SiC Hetero-Epitaxially Grown on Silicon Compliance Substrates and New 3C-SiC Substrates for Sustainable Wide-Band-Gap Power Devices (CHALLENGE).* Paper presented at the Materials Science Forum.

Lapadatu, A. C., & Jakobsen, H. (2015). Anodic bonding. In *Handbook of Silicon Based MEMS Materials and Technologies* (pp. 599-610): Elsevier.

Latreche, A. (2003). An accurate method for extracting the three Fowler-Nordheim tunnelling parameters using IV characteristic. *B br, 2*, 0.

Lee, B., Choi, K., Hande, A., Kim, M., & Wallace, R. (2009). A novel thermally-stable zirconium amidinate ALD precursor for ZrO_2 thin films. *Microelectronic engineering, 86*(3), 272-276.

Lee, J.-G., Kim, H.-S., Seo, K.-S., Cho, C.-H., & Cha, H.-Y. (2016). High quality PECVD SiO_2 process for recessed MOS-gate of AlGaN/GaN-on-Si metal–oxide–semiconductor heterostructure field-effect transistors. *Solid-State Electronics, 122*, 32-36.

Lee, J.-H., Bargatin, I., Park, J., & Milaninia, K. M. (2012). Smart-cut layer transfer of single-crystal SiC using spin-on-glass. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena, 30*(4), 042001.

Lee, S. (2018). *Evaluation of deposited silicon oxide with post-deposition annealing for gate oxide of MOS capacitors on 4H-SiC.* Seoul National University,

Lee, S. K. (2002). *Processing and characterization of silicon carbide (6H-SiC and 4H-SiC) contacts for high power and high temperature device applications.* Mikroelektronik och informationsteknik,

Lee, S. M., Jang, Y., Jung, J., Yum, J. H., Bielawski, C. W., & Cha, H.-Y. (2019). Atomic layer deposition of crystalline BeO on SiC. *Applied Surface Science, 469*, 634-640.

Lee, T. E., Kato, K., Ke, M., Toprasertpong, K., Takenaka, M., & Takagi, S. (2019). Impact of metal gate electrodes on electrical properties of Y_2O_3/SiO. 78 GeO. 22 gate stacks. *Microelectronic engineering, 214*, 87-92.

Lei, Z. C., Abidin, N. I. Z., & Wong, Y. H. (2018). Structural, chemical, and electrical properties of ZrO_2/Ge system formed via oxidation/nitridation in N_2O gas ambient. *Journal of Materials Science: Materials in Electronics, 29*(15), 12888-12898.

Lei, Z. C., Goh, K. H., Abidin, N. I. Z., & Wong, Y. H. (2017). Effect of oxidation temperature on physical and electrical properties of ZrO_2 thin-film gate oxide on Ge substrate. *Thin Solid Films, 642*, 352-358.

Lelis, A., Habersat, D., Olaniran, F., Simons, B., & McGarrity, J. (2006). Time-dependent bias stress-induced instability of SiC MOS devices. *MRS Online Proceedings Library (OPL), 911*.

Levasseur, A., Vinatier, P., & Gonbeau, D. (1999). X-ray photoelectron spectroscopy: A powerful tool for a better characterization of thin film materials. *Bulletin of Materials Science, 22*(3), 607-614.

Levisse, A., Giraud, B., Noël, J.-P., Moreau, M., & Portal, J. M. (2017). *High density emerging resistive memories: What are the limits?* Paper presented at the 2017 IEEE 8th Latin American Symposium on Circuits & Systems (LASCAS).

Li, H.-F., Dimitrijev, S., & Harrison, H. B. (1998). Improved reliability of NO-nitrided SiO_2 grown on p-type 4H-SiC. *IEEE Electron Device Letters, 19*(8), 279-281.

Li, H.-f., Dimitrijev, S., Harrison, H. B., & Sweatman, D. (1997). Interfacial characteristics of N_2O and NO nitrided SiO_2 grown on SiC by rapid thermal processing. *Applied physics letters, 70*(15), 2028-2030.

Li, T., Tu, T., Sun, Y., Fu, H., & Wu, J. (2020). A native oxide high-κ gate dielectric for two-dimensional electronics. *Nature Electronics, 3*(8), 473-478.

Liang, X., Evanko, B. W., Izar, A., King, D. M., Jiang, Y.-B., & Weimer, A. W. (2013). Ultrathin highly porous alumina films prepared by alucone ABC molecular layer deposition (MLD). *Microporous and mesoporous materials, 168*, 178-182.

Liang, Z. (2012). *Status and trend of automotive power packaging.* Paper presented at the 2012 24th International Symposium on Power Semiconductor Devices and ICs.

Lien, W.-C. (2013). *Harsh Environment Silicon Carbide UV Sensor and Junction Field-Effect Transistor*: University of California, Berkeley.

Lim, W., Cheong, K., & Lockman, Z. (2010). Physical characterization of post-deposition annealed metal-organic decomposed cerium oxide film spin-coated on 4H-silicon carbide. *Journal of alloys and compounds, 497*(1-2), 195-200.

Lim, W. F., & Quah, H. J. (2020). Wet oxidation growth of hafnium doped tantalum oxide films with different composition deposited on silicon substrate. *Applied Surface Science, 526*, 146722.

Linewih, H. (2003). *Design and application of SiC power MOSFET*: Griffith University.

Liu, E., Conti, F., Bhogaraju, S. K., Signorini, R., & Elger, G. (2020). Thermo-mechanical stress in GaN-LEDs soldered onto Cu substrates studied using finite element method and Raman spectroscopy. *Journal of Raman Spectroscopy, 51*(10), 2083-2094.

Liu, H. (2018). *High Temperature Degradation of Silicon Carbide (SiC) by Metallic Fission Products (Palladium, Silver) and Oxidation*: The University of Manchester (United Kingdom).

Liu, L., Tang, W., Huang, X., Xu, J., & Lai, P. (2019). Surface Passivation Using Lanthanide Oxynitrides for GaAs Metal–Oxide–Semiconductor Applications. *IEEE Transactions on Electron Devices, 66*(7), 3080-3085.

Liu, S., Gu, C., Wei, J., Qian, Q., Sun, W., & Huang, A. Q. (2016). Repetitive unclamped-inductive-switching-induced electrical parameters degradations and simulation optimizations for 4H-SiC MOSFETs. *IEEE Transactions on Electron Devices, 63*(11), 4331-4338.

Lohrmann, A., Johnson, B., McCallum, J., & Castelletto, S. (2017). A review on single photon sources in silicon carbide. *Reports on Progress in Physics, 80*(3), 034502.

Loncarski, J., Monopoli, V. G., Leuzzi, R., Ristic, L., & Cupertino, F. (2019). Analytical and Simulation Fair Comparison of Three Level Si IGBT Based NPC Topologies and Two Level SiC MOSFET Based Topology for High Speed Drives. *Energies, 12*(23), 4571.

López, I., Ceballos, S., Andreu, J., de Alegría, I. M., & Kortabarria, I. (2013). *Review of Modulation Algorithms for Neutral-Point-Clamped Multilevel Converter.* Paper presented at the International Conference on Renewable Energies and Power Quality, Bilbao.

Lorenz, L., Erlbacher, T., & Hilt, O. (2018). Future technology trends. In *Wide Bandgap Power Semiconductor Packaging* (pp. 3-53): Elsevier.

Low, F. W., Lai, C. W., Samsudin, N. A., Yusoff, Y., Goh, S. M., & Tiong, S. K. (2021). Graphene and its derivatives, synthesis route, and mechanism for photovoltaic solar cell applications. In *Sustainable Materials for Next Generation Energy Devices* (pp. 103-132): Elsevier.

Lu, H. L., & Zhang, D. W. (2012). Issues in High-k Gate Dielectrics and its Stack Interfaces. *High-k Gate Dielectrics for CMOS Technology*, 31-59.

Łukasiak, L., & Jakubowski, A. (2010). History of semiconductors. *Journal of Telecommunications and information technology*, 3-9.

Lutz, J., Schlangenotto, H., Scheuermann, U., & De Doncker, R. (2011). *Semiconductor power devices: physics, characteristics, reliability*: Springer Science & Business Media.

Mack, C. A. (2011). Fifty years of Moore's law. *IEEE Transactions on semiconductor manufacturing, 24*(2), 202-207.

Mahajan, A., Khairnar, A. G., & Thibeault, B. (2016). High Dielectric Constant ZrO_2 Films by Atomic Layer Deposition Technique on Germanium Substrates. *Silicon, 8*(3), 345-350.

Mahapatra, S., Kumar, P. B., & Alam, M. (2004). Investigation and modeling of interface and bulk trap generation during negative bias temperature instability of p-MOSFETs. *IEEE Transactions on Electron Devices, 51*(9), 1371-1379.

Maiti, C., Samanta, S., Dalapati, G., Nandi, S., & Chatterjee, S. (2004). Electrical characterization of TiO_2 gate oxides on strained-Si. *Microelectronic engineering, 72*(1-4), 253-256.

Maity, N., Maity, R., Thapa, R., & Baishya, S. (2014). Study of interface charge densities for ZrO_2 and hfO_2 based metal-oxide-semiconductor devices. *Advances in Materials Science and Engineering, 2014*.

Maity, N. P., Thapa, R., & Baishya, S. (2013). *Comparison of different high-k dielectric materials in MOS device from CV Characteristics.* Paper presented at the Advanced Materials Research.

Maniammal, K., Madhu, G., & Biju, V. (2017). X-ray diffraction line profile analysis of nanostructured nickel oxide: shape factor and convolution of crystallite size and microstrain contributions. *Physica E: Low-dimensional Systems and Nanostructures, 85*, 214-222.

Manikanthababu, N., Tak, B., Prajna, K., Singh, R., & Panigrahi, B. (2020). Radiation sustenance of HfO_2/β-Ga_2O_3 metal-oxide-semiconductor capacitors: gamma irradiation study. *Semiconductor Science and Technology, 35*(5), 055024.

Manning, W., Hunter Jr, O., & Powell Jr, B. (1969). Elastic properties of polycrystalline yttrium oxide, dysprosium oxide, holmium oxide, and erbium oxide: room temperature measurements. *Journal of the American Ceramic Society, 52*(8), 436-442.

Marchesoni, M., Mazzucchelli, M., & Tenconi, S. (1990). A non-conventional power converter for plasma stabilization. *IEEE Transactions on Power Electronics, 5*(2), 212-219.

Marsi, N., Majlis, B. Y., Hamzah, A. A., & Mohd-Yasin, F. (2015). High reliability of MEMS packaged capacitive pressure sensor employing 3C-SiC for high temperature. *Energy Procedia, 68*, 471-479.

Matallana, A., Ibarra, E., López, I., Andreu, J., & Rebollo, J. (2019). Power module electronics in HEV/EV applications: New trends in wide-bandgap semiconductor technologies and design aspects. *Renewable and Sustainable Energy Reviews, 113*, 109264.

Matocha, K., Dunne, G., Soloviev, S., & Beaupre, R. (2008). Time-dependent dielectric breakdown of 4H-SiC MOS capacitors and DMOSFETs. *IEEE Transactions on Electron Devices, 55*(8), 1830-1834.

Matocha, K., Ji, I.-H., Zhang, X., & Chowdhury, S. (2019). *SiC power MOSFETs: Designing for reliability in wide-bandgap semiconductors.* Paper presented at the 2019 IEEE International Reliability Physics Symposium (IRPS).

Matsumoto, T., Nakajima, H., Irishika, D., Nonaka, T., Imamura, K., & Kobayashi, H. (2017). Ultrathin SiO_2 layer formed by the nitric acid oxidation of Si (NAOS) method to improve the thermal-SiO_2/Si interface for crystalline Si solar cells. *Applied Surface Science, 395*, 56-60.

May, G. S., & Spanos, C. J. (2006). *Fundamentals of semiconductor manufacturing and process control*: John Wiley & Sons.

Meng, X. (2017). An overview of molecular layer deposition for organic and organic–inorganic hybrid materials: mechanisms, growth characteristics, and promising applications. *Journal of Materials Chemistry A, 5*(35), 18326-18378.

Menghal, P., & Laxmi, A. J. (2010). *Real time control of electrical machine drives: A review.* Paper presented at the 2010 International Conference on Power, Control and Embedded Systems.

Meynard, T. A., & Foch, H. (1992). *Multi-level conversion: high voltage choppers and voltage-source inverters.* Paper presented at the PESC'92 Record. 23rd Annual IEEE Power Electronics Specialists Conference.

Milenov, T., Dikovska, A., Avdeev, G., Avramova, I., Kirilov, K., & Kolev, S. (2019). Pulsed laser deposition of thin carbon films on SiO_2/Si substrates. *Applied Surface Science, 480*, 323-329.

Militaru, L., Poncet, A., & Leroux, C. (2005). Characterization of ultra-thin SiO_2 by capacitance–voltage and charge pumping measurements. *Microelectronic engineering, 81*(1), 59-65.

Millan, J., Godignon, P., Perpiñà, X., Pérez-Tomás, A., & Rebollo, J. (2013). A survey of wide bandgap power semiconductor devices. *IEEE Transactions on Power Electronics, 29*(5), 2155-2163.

Mittemeijer, E. J., & Welzel, U. (2008). The "state of the art" of the diffraction analysis of crystallite size and lattice strain. *Zeitschrift für Kristallographie, 223*(9), 552-560.

Miyazaki, S., Nishimura, H., Fukuda, M., Ley, L., & Ristein, J. (1997). Structure and electronic states of ultrathin SiO_2 thermally grown on Si (100) and Si (111) surfaces. *Applied Surface Science, 113*, 585-589.

Mohsenifar, S., & Shahrokhabadi, M. (2015). Gate stack high-κ materials for Si-based MOSFETs past, present, and futures. *terminology, 2*, 5.

Molina-Reyes, J., Uribe-Vargas, H., Torres-Torres, R., Mani-Gonzalez, P., & Herrera-Gomez, A. (2017). Accurate modeling of gate tunneling currents in Metal-Insulator-Semiconductor capacitors based on ultra-thin atomic-layer deposited Al_2O_3 and post-metallization annealing. *Thin Solid Films, 638*, 48-56.

Monroy, E., Omnès, F., & Calle, F. (2003). Wide-bandgap semiconductor ultraviolet photodetectors. *Semiconductor Science and Technology, 18*(4), R33.

Moon, J. H., Kang, I. H., Kim, H. W., Seok, O., Bahng, W., & Ha, M.-W. (2020). TEOS-based low-pressure chemical vapor deposition for gate oxides in 4H–SiC MOSFETs using nitric oxide post-deposition annealing. *Current Applied Physics, 20*(12), 1386-1390.

Morimoto, S., Ooi, S., Inoue, Y., & Sanada, M. (2014). Experimental evaluation of a rare-earth-free PMASynRM with ferrite magnets for automotive applications. *IEEE Transactions on Industrial Electronics, 61*(10), 5749-5756.

Morimoto, S., Takeda, Y., Hirasa, T., & Taniguchi, K. (1990). Expansion of operating limits for permanent magnet motor by current vector control considering inverter capacity. *IEEE transactions on industry applications, 26*(5), 866-871.

Morya, A. K., Gardner, M. C., Anvari, B., Liu, L., & Toliyat, H. A. (2019). Wide bandgap devices in AC electric drives: Opportunities and challenges. *IEEE Transactions on Transportation Electrification, 5*(1), 3-20.

Moshrefi, A., Aghababa, H., & Shoaei, O. (2017). *An aging-aware model for the leakage power of nanoscaled digital integrated circuits in IoT era.* Paper presented at the 2017 24th IEEE International Conference on Electronics, Circuits and Systems (ICECS).

Mote, V., Purushotham, Y., & Dole, B. (2011). Structural and morphological studies on Mn substituted ZnO nanometer-sized crystals. *Crystal Research and Technology, 46*(7), 705-710.

Nagai, N., & Hashimoto, H. (2001). FTIR-ATR study of depth profile of SiO_2 ultra-thin films. *Applied Surface Science, 172*(3-4), 307-311.

Nakamura, D., Gunjishima, I., Yamaguchi, S., Ito, T., Okamoto, A., & Takatori, K. (2004). Ultrahigh-quality silicon carbide single crystals. *Nature, 430*(7003), 1009-1012.

Namvar, A., Dehghany, M., Sohrabpour, S., & Naghdabadi, R. (2016). Thermal residual stresses in silicon thin film solar cells under operational cyclic thermal loading: A finite element analysis. *Solar Energy, 135*, 366-373.

Narayanan, V., Frank, M. M., & Demkov, A. A. (2016). *Thin Films on Silicon: Electronic and Photonic Applications* (Vol. 8): World Scientific.

Nawaz, M. (2015). On the evaluation of gate dielectrics for 4H-SiC based power MOSFETs. *Active and Passive Electronic Components, 2015*.

Neeb, C., Teichrib, J., De Doncker, R. W., Boettcher, L., & Ostmann, A. (2014). *A 50 kW IGBT power module for automotive applications with extremely low DC-link inductance.* Paper presented at the 2014 16th European Conference on Power Electronics and Applications.

Nguyen, B.-H., Do, H. V., & Minh, C. T. (2015). *High performance current control of ipmsm for electric vehicles drives using disturbance observer.* Paper presented at the 2015 IEEE Vehicle Power and Propulsion Conference (VPPC).

Nguyen, Q. K., Petrich, M., & Roth-Stielow, J. (2014). *Implementation of the MTPA and MTPV control with online parameter identification for a high speed IPMSM used as traction drive.* Paper presented at the 2014 International Power Electronics Conference (IPEC-Hiroshima 2014-ECCE ASIA).

Nicholls, J. R., Vidarsson, A. M., Haasmann, D., Sveinbjörnsson, E. Ö., & Dimitrijev, S. (2020). Near-Interface Trap Model for the Low Temperature Conductance Signal in SiC MOS Capacitors With Nitrided Gate Oxides. *IEEE Transactions on Electron Devices, 67*(9), 3722-3728.

Nishino, S., Powell, J. A., & Will, H. A. (1983). Production of large-area single-crystal wafers of cubic SiC for semiconductor devices. *Applied physics letters, 42*(5), 460-462.

Noae, T., Ikeuchi, T., Moritni, C., Endoh, H., & Yokoyama, K. (2013). Local damage free Si substrate ultra thinning for backside emission spectral analysis using OBPF for LSI failure mode detection. *Microelectronics Reliability, 53*(12), 1829-1840.

Noborio, M., Suda, J., Beljakowa, S., Krieger, M., & Kimoto, T. (2009). 4H-SiC MISFETs with nitrogen-containing insulators. *physica status solidi (a), 206*(10), 2374-2390.

Normand, P., Kapetanakis, E., Dimitrakis, P., Skarlatos, D., Beltsios, K., & Claverie, A. (2004). Nanocrystals manufacturing by ultra-low-energy ion-beam-synthesis for non-volatile memory applications. *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, 216*, 228-238.

Ohishi, K., & Hattori, T. (1994). Periodic changes in SiO_2/Si (111) interface structures with progress of thermal oxidation. *Japanese Journal of Applied Physics, 33*(5A), L675.

Onik, T. A. M., Hawari, H. F., Sabri, M. F. M., & Wong, Y. H. (2021a). Formation and characterization of holmium oxide on germanium-based metal-oxide-semiconductor capacitor. *International Journal of Energy Research*.

Onik, T. A. M., Hawari, H. F., Sabri, M. F. M., & Wong, Y. H. (2021b). Growth mechanisms and characteristics of Sm_2O_3 based on Ge semiconductor through oxidation and nitridation. *Applied Surface Science, 544*, 148949.

Ooi, S., Morimoto, S., Sanada, M., & Inoue, Y. (2013). Performance evaluation of a high-power-density PMASynRM with ferrite magnets. *IEEE transactions on industry applications, 49*(3), 1308-1315.

Opila, R., Chang, J. P., Du, M., Bevk, J., Ma, Y., & Gurevich, A. (1999). *X-ray photoelectron study of gate oxides and nitrides.* Paper presented at the Solid State Phenomena.

Östling, M., Ghandi, R., & Zetterling, C.-M. (2011). *SiC power devices—Present status, applications and future perspective.* Paper presented at the 2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs.

Oviroh, P. O., Akbarzadeh, R., Pan, D., Coetzee, R. A. M., & Jen, T.-C. (2019). New development of atomic layer deposition: processes, methods and applications. *Science and technology of advanced materials, 20*(1), 465-496.

Pala, V., Van Brunt, E., Ryu, S., Hull, B., & Hefner, A. (2016). *Physics of bipolar, unipolar and intermediate conduction modes in Silicon Carbide MOSFET body diodes.* Paper presented at the 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD).

Palmour, J. W., Carter, C., Edmund, J., & Kong, H.-S. (1993). *6H-silicon carbide power devices for aerospace applications.* Paper presented at the Intersociety Energy Conversion Engineering Conference.

Pan, T.-M., Chang, W.-T., & Chiu, F.-C. (2010). Structural and electrical properties of thin Ho_2O_3 gate dielectrics. *Thin Solid Films, 519*(2), 923-927.

Pan, T.-M., & Huang, M.-D. (2011). Structural properties and sensing characteristics of high-k Ho_2O_3 sensing film-based electrolyte–insulator–semiconductor. *Materials chemistry and physics, 129*(3), 919-924.

Pan, T.-M., & Yen, L.-C. (2010). Influence of post-deposition annealing on structural properties and electrical characteristics of thin Tm_2O_3 and $Tm_2Ti_2O_7$ dielectrics. *Applied Surface Science, 256*(9), 2786-2791.

Pande, P., Dimitrijev, S., Haasmann, D., Moghadam, H. A., Chaturvedi, M., & Jadli, U. (2020). Impact of nitridation on the active near-interface traps in gate oxides on 4H-SiC. *Solid-State Electronics, 171*, 107874.

Parish, C. M., Koyanagi, T., Kondo, S., & Katoh, Y. (2017). Irradiation-induced β to α SiC transformation at low temperature. *Scientific reports, 7*(1), 1-9.

Pengelly, R. S., Wood, S. M., Milligan, J. W., Sheppard, S. T., & Pribble, W. L. (2012). A review of GaN on SiC high electron-mobility power transistors and MMICs. *IEEE Transactions on Microwave Theory and Techniques, 60*(6), 1764-1783.

Pensl, G., Beljakowa, S., Frank, T., Gao, K., Speck, F., & Ciobanu, F. (2008). V. Afanas ev, A. Stesmans, T. Kimoto, and A. Schöner. *Phys. Stat. Sol.(b), 245*(7), 1378.

Peters, D., Basler, T., Zippelius, B., & Siemieniec, R. (2017). CoolSiC trench MOSFET combining SiC performance with silicon ruggedness. *Power Electronics Europe, 3*, 25-27.

Phan, H.-P., Dao, D. V., Nakamura, K., Dimitrijev, S., & Nguyen, N.-T. (2015). The piezoresistive effect of SiC for MEMS sensors at high temperatures: A review. *Journal of Microelectromechanical systems, 24*(6), 1663-1677.

Platonov, V. B., Rumyantseva, M. N., Frolov, A. S., Yapryntsev, A. D., & Gaskov, A. M. (2019). High-temperature resistive gas sensors based on ZnO/SiC nanocomposites. *Beilstein journal of nanotechnology, 10*(1), 1537-1547.

Pou, J., Zaragoza, J., Rodríguez, P., Ceballos, S., & Boroyevich, D. (2007). Fast-processing modulation strategy for the neutral-point-clamped converter with total elimination of low-frequency voltage oscillations in the neutral point. *IEEE Transactions on Industrial Electronics, 54*(4), 2288-2294.

Powell, J. A., Neudeck, P. G., Trunek, A. J., & Spry, D. J. (2008). Method for the growth of large low-defect single crystals. In: Google Patents.

Presser, V., & Nickel, K. G. (2008). Silica on silicon carbide. *Critical reviews in solid state and materials sciences, 33*(1), 1-99.

Qiu, P., Wei, H., An, Y., Wu, Q., Du, W., & He, Y. (2020). Plasma-enhanced atomic layer deposition of gallium nitride thin films on fluorine-doped tin oxide glass substrate for future photovoltaic application. *Ceramics International, 46*(5), 5765-5772.

Quah, H. J., & Cheong, K. Y. (2013). Effects of post-deposition annealing ambient on chemical, structural, and electrical properties of RF magnetron sputtered Y_2O_3 gate on gallium nitride. *Journal of alloys and compounds, 575*, 382-392.

Rajeh, T., Al-Kbodi, B. H., & Zhang, H. (2020). Thermal Stress and Deformation of Hollow Paddle-Shaft Components with Internal High Temperature Molten Salt Flow. *Processes, 8*(12), 1557.

Ramamurthy, R. P., Islam, N., Sampath, M., Morisette, D. T., & Cooper, J. A. (2020). The Tri-Gate MOSFET: A New Vertical Power Transistor in 4H-SiC. *IEEE Electron Device Letters, 42*(1), 90-93.

Rawat, K., Fong, D. D., & Aidhy, D. S. (2021). Breaking atomic-level ordering via biaxial strain in functional oxides: A DFT study. *Journal of Applied Physics, 129*(9), 095301.

Raynaud, C. (2001). Silica films on silicon carbide: a review of electrical properties and device applications. *Journal of Non-Crystalline Solids, 280*(1-3), 1-31.

Razera, R. A., Boudinov, H. I., Rodrigues, F. S., Ferreira, R. Z., & Feil, A. F. (2018). Anomalous Current–Voltage Behavior in Al/TiO_2/n-Si Structures. *physica status solidi (RRL)–Rapid Research Letters, 12*(6), 1800057.

Reicher, D., Black, P., & Jungling, K. (2000). Defect formation in hafnium dioxide thin films. *Applied optics, 39*(10), 1589-1599.

Reimann, T. (2015). Application Manual Power Semiconductors. In *2nd ed., SEMIKRON InternationalGmbH*.

Reimers, J., Dorn-Gomba, L., Mak, C., & Emadi, A. (2019). Automotive traction inverters: Current status and future trends. *IEEE Transactions on Vehicular Technology, 68*(4), 3337-3350.

Robertson, J. (2011). New high-k materials for CMOS applications.

Robertson, J., & Wallace, R. M. (2015). High-K materials and metal gates for CMOS applications. *Materials Science and Engineering: R: Reports, 88*, 1-41.

Roccaforte, F., Fiorenza, P., & Giannazzo, F. (2013). Impact of the morphological and electrical properties of SiO_2/4H-SiC interfaces on the behavior of 4H-SiC MOSFETs. *ECS Journal of Solid State Science and Technology, 2*(8), N3006.

Roccaforte, F., Fiorenza, P., Greco, G., & Nigro, R. L. (2018). Emerging trends in wide band gap semiconductors (SiC and GaN) technology for power devices. *Microelectronic engineering, 187*, 66-77.

Rodríguez, J., Bernet, S., Wu, B., Pontt, J. O., & Kouro, S. (2007). Multilevel voltage-source-converter topologies for industrial medium-voltage drives. *IEEE Transactions on Industrial Electronics, 54*(6), 2930-2945.

Rodriguez, J., Franquelo, L. G., Kouro, S., Leon, J. I., & Portillo, R. C. (2009). Multilevel converters: An enabling technology for high-power applications. *Proceedings of the IEEE, 97*(11), 1786-1817.

Rodriguez, J., Lai, J.-S., & Peng, F. Z. (2002). Multilevel inverters: a survey of topologies, controls, and applications. *IEEE Transactions on Industrial Electronics, 49*(4), 724-738.

Roesch, R., Faber, T., Von Hauff, E., Brown, T. M., Lira-Cantu, M., & Hoppe, H. (2015). Procedures and Practices for Evaluating Thin-Film Solar Cell Stability. *Advanced Energy Materials, 5*(20), 1501407.

Rong, H. (2015). *Development of 4H-SiC power MOSFETs for high voltage applications.* University of Warwick,

Rozen, J. (2008). *Electronic properties and reliability of the SiO_2/SiC interface.* Vanderbilt University,

Rozen, J., Dhar, S., Dixit, S., Afanas' ev, V., Roberts, F., & Feldman, L. (2008). Increase in oxide hole trap density associated with nitrogen incorporation at the SiO_2/SiC interface. *Journal of Applied Physics, 103*(12), 124513.

Safarabadi, M., & Shokrieh, M. (2014). Understanding residual stresses in polymer matrix composites. In *Residual stresses in composite materials* (pp. 197-232): Elsevier.

Sah, C.-T. (1991). *Fundamentals of solid-state electronics*: World Scientific.

Sahari, S., Ohta, A., Matsui, M., Mishima, K., & Miyazaki, S. (2013). *Kinetics of thermally oxidation of Ge (100) surface.* Paper presented at the Journal of Physics: Conference Series.

Sakai, A., Eikyu, K., Sonoda, K., Hisada, K., Arai, K., & Yamaguchi, Y. (2015). *Impacts of the 4H-SiC/SiO2 interface states on the switching operation of power MOSFETs.* Paper presented at the 2015 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD).

Salmani-Jelodar, M., Ilatikhameneh, H., Kim, S., Ng, K., Sarangapani, P., & Klimeck, G. (2016). Optimum high-k oxide for the best performance of ultra-scaled double-gate MOSFETs. *IEEE Transactions on Nanotechnology, 15*(6), 904-910.

Salvado, O. A., Morel, H., Buttay, C., Labrousse, D., & Lefebvre, S. (2018). Threshold voltage instability in SiC MOSFETs as a consequence of current conduction in their body diode. *Microelectronics Reliability, 88*, 636-640.

Samanta, P., & Mandal, K. C. (2016). Simulation of temperature dependent dielectric breakdown in n+-polySi/SiO_2/n-6H-SiC structures during Poole-Frenkel stress at positive gate bias. *Journal of Applied Physics, 120*(6), 064504.

Santra, K., Chatterjee, P., & Gupta, S. S. (2002). Voigt modelling of size-strain analysis: Application to α-Al_2O_3 prepared by combustion technique. *Bulletin of Materials Science, 25*(3), 251-257.

Sarangan, A. (2016). *Nanofabrication: Principles to Laboratory Practice*: CRC Press.

Sarlioglu, B., Morris, C. T., Han, D., & Li, S. (2016). Driving toward accessibility: a review of technological improvements for electric machines, power electronics, and batteries for electric and hybrid vehicles. *IEEE Industry Applications Magazine, 23*(1), 14-25.

Schamm, S., Scarel, G., & Fanciulli, M. (2007). Local structure, composition and electronic properties of rare earth oxide thin films studied using advanced transmission electron microscopy techniques (TEM-EELS). *Rare earth oxide thin films*, 153-177.

Schilirò, E., Fiorenza, P., Di Franco, S., Bongiorno, C., Saggio, M., & Roccaforte, F. (2017). Effect of SiO_2 interlayer on the properties of Al_2O_3 thin films grown by plasma enhanced atomic layer deposition on 4H-SiC substrates. *physica status solidi (a), 214*(4), 1600365.

Schilirò, E., Lo Nigro, R., Roccaforte, F., & Giannazzo, F. (2019). Recent Advances in Seeded and Seed-Layer-Free Atomic Layer Deposition of High-K Dielectrics on Graphene for Electronics. *C—Journal of Carbon Research, 5*(3), 53.

Schlech, T., Horn, S., Wijayawardhana, C., & Rashidi, A. (2021). Experimental and FEM based investigation of the influence of the deposition temperature on the mechanical properties of SiC coatings. *Journal of Advanced Ceramics, 10*(1), 139-151.

Schlom, D. G., Chen, L.-Q., Fennie, C. J., Gopalan, V., & Muller, D. A. (2014). Elastic strain engineering of ferroic oxides. *Mrs Bulletin, 39*(2), 118-130.

Schlom, D. G., Chen, L. Q., Pan, X., Schmehl, A., & Zurbuchen, M. A. (2008). A thin film approach to engineering functionality into oxides. *Journal of the American Ceramic Society, 91*(8), 2429-2454.

Schneider-Ramelow, M., Baumann, T., & Hoene, E. (2008). *Design and assembly of power semiconductors with double-sided water cooling.* Paper presented at the 5th International Conference on Integrated Power Electronics Systems.

Schöner, A., Krieger, M., Pensl, G., Abe, M., & Nagasawa, H. (2006). Fabrication and characterization of 3C-SiC-based MOSFETs. *Chemical Vapor Deposition, 12*(8-9), 523-530.

Schulz, S. E. (2017). Exploring the High-Power Inverter: Reviewing critical design elements for electric vehicle applications. *IEEE Electrification Magazine, 5*(1), 28-35.

Sekhar, M. C., Reddy, N. N. K., Akkera, H. S., & Reddy, B. P. (2017). Role of interfacial oxide layer thickness and annealing temperature on structural and electronic properties of $Al/Ta_2O_5/TiO_2/Si$ metal–insulator–semiconductor structure. *Journal of alloys and compounds, 718*, 104-111.

Senesky, D. G., Jamshidi, B., Cheng, K. B., & Pisano, A. P. (2009). Harsh environment silicon carbide sensors for health and performance monitoring of aerospace systems: A review. *IEEE Sensors Journal, 9*(11), 1472-1478.

Sereni, J. G. R. (2016). Reference module in materials science and materials engineering.

Seshan, K., & Schepis, D. (2018). *Handbook of thin film deposition*: William Andrew.

Shaaban, E. R., Afify, N., & El-Taher, A. (2009). Effect of film thickness on microstructure parameters and optical constants of CdTe thin films. *Journal of alloys and compounds, 482*(1-2), 400-404.

Shah, R., & Dhavse, R. (2021). Novel hybrid silicon SETMOS design for power efficient room temperature operation. *Silicon, 13*(2), 587-597.

Sharma, A., Lee, S. J., Jang, Y. J., & Jung, J. P. (2014). SiC based Technology for High Power Electronics and Packaging Applications. *Journal of the Microelectronics and Packaging Society, 21*(2), 71-78.

Sharma, A., Tripathi, S., & Shripathi, T. (2009). X-ray photoelectron study of annealed Co thin film on Si surface. *Applied Surface Science, 256*(2), 530-535.

Sharma, R., & Rana, A. K. (2015). *Strained Si: Opportunities and challenges in nanoscale MOSFET.* Paper presented at the 2015 IEEE 2nd International Conference on Recent Trends in Information Systems (ReTIS).

Sharma, Y. (2012). *Advanced SiO_2/SiC Interface Passivation.*

Sharma, Y., Ahyi, A., Isaacs-Smith, T., Modic, A., Park, M., & Xu, Y. (2013). High-mobility stable 4H-SiC MOSFETs using a thin PSG interfacial passivation layer. *IEEE Electron Device Letters, 34*(2), 175-177.

She, X., Huang, A. Q., Lucía, Ó., & Ozpineci, B. (2017). Review of silicon carbide power devices and their applications. *IEEE Transactions on Industrial Electronics, 64*(10), 8193-8205.

Shenai, K. (2019). High-density power conversion and wide-bandgap semiconductor power electronics switching devices. *Proceedings of the IEEE, 107*(12), 2308-2326.

Shenai, K., Scott, R. S., & Baliga, B. J. (1989). Optimum semiconductors for high-power electronics. *IEEE Transactions on Electron Devices, 36*(9), 1811-1823.

Shenoy, J. N., Cooper, J., & Melloch, M. R. (1997). High-voltage double-implanted power MOSFET's in 6H-SiC. *IEEE Electron Device Letters, 18*(3), 93-95.

Shin, M.-C., Lee, Y.-J., Kim, D.-H., Jung, S.-W., & Schweitz, M. A. (2021). Improved Electrical Characteristics of Gallium Oxide/P-Epi Silicon Carbide Static Induction Transistors with UV/Ozone Treatment Fabricated by RF Sputter. *Materials, 14*(5), 1296.

Singh, J., Jain, A. K., & Kumar, M. J. (2019). Realizing a planar 4H-SiC junctionless FET for Sub-10-nm regime using P+ pocket. *IEEE Transactions on Electron Devices, 66*(7), 3209-3214.

Soler, V., Cabello, M., Berthou, M., Montserrat, J., Rebollo, J., & Sebastián, J. (2017). High-voltage 4H-SiC power MOSFETs with Boron-doped gate oxide. *IEEE Transactions on Industrial Electronics, 64*(11), 8962-8970.

Sometani, M., Okamoto, D., Harada, S., Ishimori, H., Takasu, S., & Okumura, H. (2016). Threshold-voltage instability in 4H-SiC MOSFETs with nitrided gate oxide revealed by non-relaxation method. *Japanese Journal of Applied Physics, 55*(4S), 04ER11.

Son, N. T., Trinh, X. T., Løvlie, L. S., Svensson, B. G., Kawahara, K., & Makino, T. (2012). Negative-U system of carbon vacancy in 4H-SiC. *Physical review letters, 109*(18), 187603.

Song, M.-K., & Rhee, S.-W. (2005). Direct liquid injection metal organic chemical vapor deposition of Nd_2O_3 thin films using Tris (2, 2, 6, 6-tetramethyl-3, 5-heptanedionato) neodymium. *Thin Solid Films, 492*(1-2), 19-23.

Soo, M. T., Cheong, K. Y., & Noor, A. F. M. (2010). Advances of SiC-based MOS capacitor hydrogen sensors for harsh environment applications. *Sensors and Actuators B: Chemical, 151*(1), 39-55.

Spence, J., Kolar, H., Hembree, G., Humphreys, C., & Justo, J. (2006). Imaging dislocation cores–the way forward. *Philosophical Magazine, 86*(29-31), 4781-4796.

Sridhar, N. (2017). Driving the future of HEV/EV with high-voltage solutions. *Texas Instruments*.

Stathis, J. H., & Zafar, S. (2006). The negative bias temperature instability in MOS devices: A review. *Microelectronics Reliability, 46*(2-4), 270-286.

Stockmeier, T. (2008). *From packaging to un-packaging trends in power semiconductor modules.* Paper presented at the 2008 20th International Symposium on Power Semiconductor Devices and IC's.

Storasta, L., & Tsuchida, H. (2007). Reduction of traps and improvement of carrier lifetime in 4H-SiC epilayers by ion implantation. *Applied physics letters, 90*(6), 062116.

Streetman, B. G., & Banerjee, S. (2006). *Solid state electronic devices* (Vol. 10): Pearson/Prentice Hall Upper Saddle River, NJ.

Stuart, B., Gimeno-Fabra, M., Segal, J., Ahmed, I., & Grant, D. M. (2015). Preferential sputtering in phosphate glass systems for the processing of bioactive coatings. *Thin Solid Films, 589*, 534-542.

Su, J.-L., Hong, C.-C., & Hwu, J.-G. (2002). Enhanced thermally induced stress effect on an ultrathin gate oxide. *Journal of Applied Physics, 91*(8), 5423-5428.

Subotic, I., Bodo, N., Levi, E., Jones, M., & Levi, V. (2015). Isolated chargers for EVs incorporating six-phase machines. *IEEE Transactions on Industrial Electronics, 63*(1), 653-664.

Suganuma, K. (2018). *Wide Bandgap Power Semiconductor Packaging: Materials, Components, and Reliability*: Woodhead Publishing.

Suhir, E. (2019). Analytical thermal stress modeling in electronics and photonics engineering: Application of the concept of interfacial compliance. *Journal of Thermal Stresses, 42*(1), 29-48.

Suzuki, T., Senzaki, J., Hatakeyama, T., Fukuda, K., & Arai, K. (2009). *Reliability of 4H-SiC (000-1) MOS gate oxide using N_2O nitridation.* Paper presented at the Materials Science Forum.

Sveinbjörnsson, E. Ö., Allerstam, F., Ólafsson, H. Ö., Rödle, T., & Jos, R. (2007). *Sodium enhanced oxidation of Si-face 4H-SiC: A method to remove near interface traps.* Paper presented at the Materials science forum.

Sze, S. M., Li, Y., & Ng, K. K. (2021). *Physics of semiconductor devices*: John wiley & sons.

Takagi, S.-i., Yasuda, N., & Toriumi, A. (1999). Experimental evidence of inelastic tunneling in stress-induced leakage current. *IEEE Transactions on Electron Devices, 46*(2), 335-341.

Ťapajna, M., Paskaleva, A., Atanassova, E., Dobročka, E., Hušeková, K., & Fröhlich, K. (2010). Gate oxide thickness dependence of the leakage current mechanism in $Ru/Ta_2O_5/SiON/Si$ structures. *Semiconductor Science and Technology, 25*(7), 075007.

Taube, A., Gierałtowska, S., Gutt, T., Małachowski, T., & Pasternak, I. (2011). Electronic properties of thin HfO_2 films fabricated by atomic layer deposition on 4H-SiC. *Acta Physica Polonica A, 119*(5), 696-698.

Taube, A., Gierałtowska, S., Gutt, T., Małachowski, T., Pasternak, I., & Wojciechowski, T. (2011). Electronic properties of thin HfO_2 films fabricated by atomic layer deposition on 4H-SiC. *Acta Physica Polonica A, 119*(5), 696-698.

Taube, A., Guziewicz, M., Kosiel, K., Gołaszewska-Malec, K., & Piotrowska, A. (2016). Characterization of Al_2O_3/4H-SiC and Al_2O_3/SiO_2/4H-SiC MOS structures. *Bulletin of the Polish Academy of Sciences. Technical Sciences, 64*(3), 537--551.

Thomas, S. (2020). Gate-all-around transistors stack up. *Nature Electronics, 3*(12), 728-728.

Thomas, S., Sharma, Y., Crouch, M., Fisher, C., & Mawby, P. (2014). Enhanced field effect mobility on 4H-SiC by oxidation at 1500 C. *IEEE Journal of the Electron Devices Society, 2*(5), 114-117.

Thomas, S. M., Jennings, M. R., Sharma, Y. K., Fisher, C. A., & Mawby, P. A. (2014). *Impact of the oxidation temperature on the interface trap density in 4H-SiC MOS capacitors.* Paper presented at the Materials Science Forum.

Thompson, S. E., & Parthasarathy, S. (2006). Moore's law: the future of Si microelectronics. *Materials today, 9*(6), 20-25.

Trancho, E., Ibarra, E., Arias, A., Kortabarria, I., Jadli, U., & Gragger, J. V. (2017). PM-assisted synchronous reluctance machine flux weakening control for EV and HEV applications. *IEEE Transactions on Industrial Electronics, 65*(4), 2986-2995.

Trancho, E., Ibarra, E., Arias, A., Salazar, C., & Peña, A. (2016). *IPMSM torque control strategies based on LUTs and VCT feedback for robust control under machine parameter variations.* Paper presented at the IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society.

Tsui, B.-Y., Huang, Y.-T., Wu, T.-L., & Chien, C.-H. (2021). Time-dependent dielectric breakdown of gate oxide on 4H-SiC with different oxidation processes. *Microelectronics Reliability, 123*, 114186.

Ueno, K., Asai, R., & Tsuji, T. (1998). 4H-SiC MOSFETs utilizing the H_2 surface cleaning technique. *IEEE Electron Device Letters, 19*(7), 244-246.

Uesugi, K., Hayashi, Y., Shojiki, K., & Xiao, S. (2019). Fabrication of AlN templates on SiC substrates by sputtering-deposition and high-temperature annealing. *Journal of Crystal Growth, 510*, 13-17.

Uhlemann, A., & Hymon, E. (2018). *Directly cooled Hybrid PACK power modules with ribbon bonded cooling structures.* Paper presented at the PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management.

Umeda, T., Esaki, K., Kosugi, R., Fukuda, K., & Ohshima, T. (2011). Behavior of nitrogen atoms in SiC-SiO_2 interfaces studied by electrically detected magnetic resonance. *Applied physics letters, 99*(14), 142105.

Van Zeghbroeck, B., Robinson, H., & Brow, R. R. (2018). *Hot filament CVD growth of 4H-SiC epitaxial layers.* Paper presented at the Materials Science Forum.

Vasin, A., Neshpor, I., Mosina, T., Vedel, D., & Grigoriev, O. (2018). Amorphous SiOxCy (: Er) films deposited by RF-magnetron sputtering on ZrB2–SiC ceramics: Antioxidation and strengthening effects. *Surface and Coatings Technology, 343*, 11-16.

Venkateswarlu, K., Bose, A. C., & Rameshbabu, N. (2010). X-ray peak broadening studies of nanocrystalline hydroxyapatite by Williamson–Hall analysis. *Physica B: Condensed Matter, 405*(20), 4256-4261.

Visokay, M., & Colombo, L. (2009). Methods of fabricating MOS transistor gates with doped silicide. In: Google Patents.

Vives, S., Gaffet, E., & Meunier, C. (2004). X-ray diffraction line profile analysis of iron ball milled powders. *Materials Science and Engineering: A, 366*(2), 229-238.

Vyazovkin, S., Burnham, A. K., Criado, J. M., Pérez-Maqueda, L. A., Popescu, C., & Sbirrazzuoli, N. (2011). ICTAC Kinetics Committee recommendations for performing kinetic computations on thermal analysis data. *Thermochimica acta, 520*(1-2), 1-19.

Wallace, R. M. (2017). Dielectric materials for microelectronics. In *Springer handbook of electronic and photonic materials* (pp. 1-1): Springer.

Wang, J., & Jiang, X. (2019). Review and analysis of SiC MOSFETs' ruggedness and reliability. *IET Power Electronics, 13*(3), 445-455.

Wang, Q., Cheng, X., Zheng, L., Shen, L., & Yu, Y. (2018). Influence of LaSiOx passivation interlayer on band alignment between PEALD-Al_2O_3 and 4H-SiC determined by X-ray photoelectron spectroscopy. *Applied Surface Science, 428*, 1-6.

Wang, Q. S., Liu, Z., Su, W. J., Yang, Y. Q., Zhao, W. F., & Cheng, X. B. (2020). *Effect of Surface Treatment on XPS Test of Graphene Films.* Paper presented at the Materials Science Forum.

Wang, T.-J., Ko, C.-H., Chang, S.-J., Wu, S.-L., Kuan, T.-M., & Lee, W.-C. (2008). The effects of mechanical uniaxial stress on junction leakage in nanoscale CMOSFETs. *IEEE Transactions on Electron Devices, 55*(2), 572-577.

Wang, X. W., Bu, H., Laube, B., Caragianis-Broadbridge, C., & Ma, T. (2002). *Improving 4H-SiC/SiO_2 interface properties by depositing ultra-thin Si nitride layer prior to formation of SiO_2 and annealing.* Paper presented at the Materials Science Forum.

Wang, Y., Dai, X., Liu, G., Li, D., & Jones, S. (2016). *An overview of advanced power semiconductor packaging for automotive system.* Paper presented at the CIPS 2016; 9th International Conference on Integrated Power Electronics Systems.

Watanabe, H., & Hosoi, T. (2012). Fundamental aspects of silicon carbide oxidation. *Physics and technology of silicon carbide devices*, 235-250.

Watanabe, H., Hosoi, T., Kirino, T., Kagei, Y., Uenishi, Y., & Shimura, T. (2011). Synchrotron x-ray photoelectron spectroscopy study on thermally grown SiO_2/4H-SiC (0001) interface and its correlation with electrical properties. *Applied physics letters, 99*(2), 021907.

Watanabe, H., Kato, K., Uda, T., Fujita, K., & Terakura, K. (1998). Kinetics of initial layer-by-layer oxidation of Si (001) surfaces. *Physical review letters, 80*(2), 345.

Watanabe, H., Kirino, T., Kagei, Y., Harries, J., & Hosoi, T. (2011). *Energy band structure of SiO_2/4H-SiC interfaces and its modulation induced by intrinsic and extrinsic interface charge transfer.* Paper presented at the Materials Science Forum.

Waye, S. (2016). *High-temperature air-cooled power electronics thermal design: annual progress report*. Retrieved from

Weber, M., Iatsunskyi, I., Coy, E., Miele, P., Cornu, D., & Bechelany, M. (2018). Novel and facile route for the synthesis of tunable boron nitride nanotubes combining atomic layer deposition and annealing processes for water purification. *Advanced Materials Interfaces, 5*(16), 1800056.

Wei, J., Liu, S., Yang, L., Li, S., & Sun, W. (2018). Comprehensive analysis of electrical parameters degradations for SiC power MOSFETs under repetitive short-circuit stress. *IEEE Transactions on Electron Devices, 65*(12), 5440-5447.

Wen, H., Xiao, W., Wen, X., & Armstrong, P. (2012). Analysis and evaluation of DC-link capacitors for high-power-density electric vehicle drive systems. *IEEE Transactions on Vehicular Technology, 61*(7), 2950-2964.

Westrum Jr, E. F., & Justice, B. H. (1963). THERMOPHYSICAL PROPERTIES OF THE LANTHANIDE OXIDES. III. HEAT CAPACITIES, THERMODYNAMIC PROPERTIES, AND SOME ENERGY LEVELS OF DYSPROSIUM (III), HOLMIUM (III), AND ERBIUM (III) OXIDES1. *The Journal of Physical Chemistry, 67*(3), 659-665.

Wiktorczyk, T., & Nitsch, K. (2001). Dielectric properties of holmium oxide films. *IEEE Transactions on Dielectrics and Electrical Insulation, 8*(3), 447-453.

Wong, Y. H., & Cheong, K. Y. (2010). ZrO_2 thin films on Si substrate. *Journal of Materials Science: Materials in Electronics, 21*(10), 980-993.

Wong, Y. H., & Cheong, K. Y. (2012). Formation of Zr-oxynitride thin films on 4H-SiC substrate. *Thin Solid Films, 520*(22), 6822-6829.

Wong, Y. H., & Goh, K. H. (2018). *Electrical Characteristics of Samarium Oxynitride Thin Film on Silicon-Based MOS Device.* Paper presented at the 2018 20th International Conference on Electronic Materials and Packaging (EMAP).

Wright, N., & Horsfall, A. (2007). SiC sensors: a review. *Journal of Physics D: Applied Physics, 40*(20), 6345.

Wutikuer, O. (2018). Fabrication and Characterization of 4H-SiC MOS Capacitors with Different Dielectric Layer Treatments. In.

Xiao, K., Wu, X., Wu, C., Yin, Q., & Huang, C. (2020). Residual stress analysis of thin film photovoltaic cells subjected to massive micro-particle impact. *RSC Advances, 10*(23), 13470-13479.

Yakimova, R. (2006). Developments in the growth of wide bandgap semiconductors. *Physica Scripta, 2006*(T126), 121.

Yamamoto, K., Nagaya, M., Watanabe, H., Okuno, E., Yamamoto, T., & Onda, S. (2012). *Influence of threading dislocations on lifetime of gate thermal oxide.* Paper presented at the Materials Science Forum.

Yang, C., Wei, S., & Wang, D. (2021). Bias temperature instability in SiC metal oxide semiconductor devices. *Journal of Physics D: Applied Physics, 54*(12), 123002.

Yang, Z., & Hao, J. (2016). Progress in pulsed laser deposited two-dimensional layered materials for device applications. *Journal of Materials Chemistry C, 4*(38), 8859-8878.

Yin, J., Chen, D., Yang, H., Liu, Y., Talwar, D. N., & Feng, Z. C. (2021). Comparative spectroscopic studies of MOCVD grown AlN films on Al_2O_3 and 6H–SiC. *Journal of alloys and compounds, 857*, 157487.

Yin, Z., Yang, C., Zhang, F., Su, Y., Qin, F., & Wang, D. (2020). Low temperature re-oxidation of near-interface defects and voltage stability in SiC MOS capacitors. *Applied Surface Science, 531*, 147312.

Yoshioka, H., Nakamura, T., & Kimoto, T. (2012). Generation of very fast states by nitridation of the SiO_2/SiC interface. *Journal of Applied Physics, 112*(2), 024520.

Yu, S., Guan, X., & Wong, H.-S. P. (2011). Conduction mechanism of TiN/HfOx/Pt resistive switching memory: A trap-assisted-tunneling model. *Applied physics letters, 99*(6), 063507.

Zak, A. K., Majid, W. A., Abrishami, M. E., & Yousefi, R. (2011). X-ray analysis of ZnO nanoparticles by Williamson–Hall and size–strain plot methods. *Solid State Sciences, 13*(1), 251-256.

Zhai, D., Lv, Z., Zhao, Y., & Lu, J. (2021). Pre-deposition growth of interfacial SiO_2 layer by low-oxygen-partial-pressure oxidation in the Al_2O_3/4H-SiC MOS structure. *Microelectronic engineering*, 111574.

Zhang, C., Srdic, S., Lukic, S., Kang, Y., Choi, E., & Tafti, E. (2018). *A SiC-based 100 kW high-power-density (34 kW/L) electric vehicle traction inverter.* Paper presented at the 2018 IEEE Energy Conversion Congress and Exposition (ECCE).

Zhang, J., & Eccleston, W. (1998). Positive bias temperature instability in MOSFETs. *IEEE Transactions on Electron Devices, 45*(1), 116-124.

Zhang, X., Li, Q., Wang, M., Zhang, Z., & Akhmadaliev, S. (2018). Defects in hydrogen implanted SiC. *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, 436*, 107-111.

Zhao, F., Amnuayphol, O., Cheong, K. Y., Wong, Y. H., & Jiang, J.-Y. (2019). Post deposition annealing effect on properties of Y_2O_3/Al_2O_3 stacking gate dielectric on 4H-SiC. *Materials Letters, 245*, 174-177.

Zheleva, T., Lelis, A., Duscher, G., Liu, F., & Das, M. (2008). Transition layers at the SiO_2/ SiC interface. *Applied physics letters, 93*(2), 022108.

Zheng, P., Sui, Y., Fu, Z., Tang, P., Wu, F., & Wang, P. (2014). *Investigation of a five-phase 20-slot/18-pole PMSM for electric vehicles.* Paper presented at the 2014 17th International Conference on Electrical Machines and Systems (ICEMS).

Zhu, C., Han, K., Geng, D., Ye, H., & Meng, X. (2017). Achieving high-performance silicon anodes of lithium-ion batteries via atomic and molecular layer deposited surface coatings: An overview. *Electrochimica Acta, 251*, 710-728.

Zhu, J., Kim, H., Chen, H., Erickson, R., & Maksimović, D. (2018). *High efficiency SiC traction inverter for electric vehicle applications.* Paper presented at the 2018 IEEE Applied Power Electronics Conference and Exposition (APEC).

Zhu, X., Lee, H. D., Feng, T., Ahyi, A. C., Mastrogiovanni, D., & Feldman, L. C. (2010). Structure and stoichiometry of (0001) 4H–SiC/oxide interface. *Applied physics letters, 97*(7), 071908.

Zhu, Z.-Q., & Howe, D. (2007). Electrical machines and drives for electric, hybrid, and fuel cell vehicles. *Proceedings of the IEEE, 95*(4), 746-765.

LIST OF PUBLICATIONS AND PAPER PRESENTED

K. O. Odesanya, T. A. M. Onik, R. Ahmad, A. Andriyana, S. Ramesh, and Y. H. Wong, "Physical and electrical characteristics of Ho_2O_3 thin film based on 4H-SiC wide bandgap semiconductor," *Thin Solid Films,* vol. 741, p. 138997, 2022 (Published).

K. O. Odesanya, R. Ahmad, A. Andriyana, Y. H. Wong, "Effects of Oxidation Duration on the Structural and Electrical Characteristics of Ho_2O_3 Gate Oxide on 4H-SiC Substrate," *Journal* of *Electronic Materials*, vol. 51, p. 4357–4367, 2022 (Published).

K. O. Odesanya, R. Ahmad, A. Andriyana, S. Bingol, R. Çetinkaya, "Thermal Characterization and Stress Analysis of Ho_2O_3 Thin film on 4H-SiC Substrate," submitted to *Materials Science in Semiconductor Processing*.

K. O. Odesanya, R. Ahmad, A. Andriyana, S. Bingol and Y. H Wong, "Gate Oxide Thin Films Based on Silicon Carbide: A Review." *ECS Journal of Solid State Science and Technology*, Vol. 11, No. 8, 2022 (Published).

K. O. Odesanya, R. Ahmad, A. Andriyana, S. Ramesh, C. Y. Tan, Y. H. Wong, "Effects of O_2 and N_2 Gas Concentration on the Formation of Ho_2O_3 Gate Oxide on 4H-SiC Substrate" *Silicon* (2022). https://doi.org/10.1007/s12633-022-02040-8 (published).