FORMATION AND CHARACTERIZATION OF RARE EARTH OXIDES AS HIGH-K GATE DIELECTRICS ON GERMANIUM SUBSTRATE

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FACULTY OF ENGINEERING
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ABSTRACT

In this study, Sm_2O_3/Ge and Ho_2O_3/Ge stack based metal oxide semiconductor (MOS) capacitors were prepared from radio frequency (RF) sputtered metallic Sm on Ge substrate and metallic Ho on Ge substrate followed by thermal oxidation/nitridation in N_2O ambient. The effects of several oxidation/nitridation temperatures, i.e., 300 °C – 600 °C on the sputtered Sm/Ge and influence of various oxidation/nitridation durations, i.e., 5 – 20 min on both sputtered Sm/Ge and Ho/Ge system have been comprehensively investigated. The film crystallinity and phase identification, chemical composition, interface chemical bonding states stability and structural morphology were characterized from X-ray diffraction (XRD), Raman spectroscopy, X-ray photoelectron spectroscopy (XPS) and High-resolution transmission electron microscopy (HRTEM). Formation of stoichiometric trigonal-Sm_2O_3 dielectric interface has been verified for thermally oxidized/nitrided sputtered Sm/Ge system. In contrary, sub-stoichiometric cubic-Ho_2O_3 has been identified for thermally oxidized/nitrided sputtered Ho/Ge system. Both the stacking structure produced sandwiched interfacial layer containing asymmetrically distributed Ge−O, and Ge−N contents while oxidized/nitrided Sm/Ge stack produced an additional stable interfacial germanate (Sm−O−Ge). Suppression of GeO (g) volatilization was evident from the XPS analysis due to GeO (g) trapping mechanism instigated by interfacial germanate (Sm−O−Ge) formation for oxidized/nitrided Sm/Ge while IL rich with Ge_3N_4 contributed to inhibit the volatilization of GeO (g) for oxidized/nitrided Ho/Ge system. The HRTEM analysis also validated double stack amorphous interfaces obtaining physical oxide thickness, $t_{ox} \sim 4.25 - 6.91$ nm for oxidized/nitrided Sm/Ge and $t_{ox} \sim 8.22 - 9.78$ nm were obtained for oxidized/nitrided Ho/Ge system. Thermal oxidation/nitridation

model related to the growth mechanism of Sm_2O_3/IL and Ho_2O_3/IL as high-*k* gate dielectrics have been suggested after considering the findings of XRD, XPS and HRTEM. Band alignment mapping and electrical measurements revealed that oxidized/nitrided Sm/Ge at 400 °C for 15 min exhibited symmetrical band offsets distribution comprising highest conduction band offset (CBO), ΔE_c of 2.60 eV and valence band offset (VBO), ΔE_v of 2.98 eV leading to lowest leakage current density $J_g \sim 8.38 \times 10^{-6}$ A cm^{-2} at enhanced breakdown field, E_{BD} of 13.31 MV cm^{-1}. As for Ho/Ge system the sample oxidized/nitrided at 400°C for 10 min exhibited the maximum $\Delta E_c \sim 2.47$ eV and $\Delta E_v \sim 4.67$ eV inducing lowest $J_g \sim 10^{-5}$ A cm^{-2} at highest $E_{BD} \sim 8.59$ MV cm^{-1}. The electrical results of these samples also revealed higher dielectric constant, k of 31.19 and 13.60 for Sm_2O_3/IL/Ge and Ho_2O_3/IL/Ge gate stacks, respectively. However, both the gate stacks expensed high average interface trap density, $D_{it} \sim 10^{13}$ eV^{-1}cm^{-2}. Additionally, effective oxide charge, slow trap density, hysteresis was also estimated from *C-V* curve which eventually ascribed the variance of electrical breakdown field for the investigated gate stacks. Comparing the physical and electrical properties of oxidized/nitrided sputtered Sm/Ge and Ho/Ge system it has been anticipated Sm_2O_3 could be more convenient choice for high-*k* gate dielectric oxide for Ge based MOS devices.

Keywords: rare-earth, high-*k*, germanium, thermal oxidation/nitridation, MOS capacitor.

PEMBENTUKAN DAN PENCIRIAN OKSIDA NADIR BUMI SEBAGAI DIEL-EKTRIK GET-K TINGGI PADA SUBSTRAT GERMANIUM

ABSTRAK

Dalam kajian ini, kapasitor semikonduktor oksida logam (MOS) berasaskan struktur Sm_2O_3/Ge dan Ho_2O_3/Ge telah disediakan menggunakan teknik percitan frekuensi radio (RF) Sm di atas substrat Ge dan Ho di atas substrat Ge, diikuti dengan pengoksidaan/penitridaan terma dalam ambien N_2O. Kesan suhu pengoksidaan/penitridaan, iaitu, 300 °C – 600 °C pada Sm/Ge dan pengaruh pelbagai tempoh pengoksidaan/nitridasi, iaitu 5 – 20 min pada kedua-dua sistem Sm/Ge dan Ho/Ge dikaji secara menyeluruh. Penghabluran filem dan pengenalpastian fasa, komposisi kimia, ikatan kimia antaramuka (IL) yang menyatakan kestabilan dan morfologi struktur telah dikaji dan dicirikan menggunakan pembelauan sinar-X (XRD), spektroskopi Raman, spektroskopi fotoelektron sinar-X (XPS) dan mikroskop elektron penghantaran resolusi tinggi (HRTEM). Pembentukan antaramuka dielektrik trigonal-Sm_2O_3 stoikiometri telah disahkan dalam sistem struktur Sm/Ge teroksida/ternitrida. Sebaliknya, sub-stoikiometrik kubik-Ho_2O_3 telah dikenal pasti untuk sistem struktur Ho/Ge teroksida/ternitrida. Kedua-dua struktur menghasilkan lapisan antaramuka yang mengandungi kandungan Ge−O dan Ge−N yang teragih tidak simetri manakala struktur Sm/Ge teroksida/ternitrida menghasilkan percambahan antaramuka yang stabil (Sm−O−Ge). Penindasan pemeruapan GeO (g) terbukti daripada analisis XPS disebabkan oleh mekanisme perangkap GeO (g) yang dicetuskan oleh pembentukan percambahan antaramuka (Sm−O−Ge) untuk Sm/Ge teroksida/ternitrida manakala antaramuka yang kaya dengan Ge_3N_4 menyumbang untuk menghalang pemeruapan. daripada GeO (g) untuk sistem Ho/Ge teroksida/nitrid. Analisis HRTEM juga mengesahkan antaramuka bersifat amorfus mempunyai ketebalan oksida fizikal, $t_{ox} \sim 4.25 - 6.91$ nm bagi struktur Sm/Ge teroksida/ternitrida dan $t_{ox} \sim 8.22 - 9.78$ nm bagi struktur Ho/Ge teroksida/ternitrida. Model pengoksidaan/nitridasi terma yang

berkaitan dengan mekanisme pertumbuhan Sm_2O_3/IL dan Ho_2O_3/IL sebagai dielektrik get-k tinggi telah dicadangkan selepas mempertimbangkan analisis XRD, XPS dan HRTEM. Pemetaan penjajaran jalur dan pengukuran elektrik mendedahkan bahawa Sm/Ge pengoksidaan/nitridasi pada 400 °C selama 15 minit mempamerkan taburan offset jalur simetri yang terdiri daripada offset jalur konduksi tertinggi (CBO), ΔE_c daripada 2.60 eV dan offset jalur valens (VBO), ΔE_v sebanyak 2.98 eV membawa kepada ketumpatan arus bocor terendah $J_g \sim 8.38 \times 10^{-6}$ A cm^{-2} dan medan pecah tebat dipertingkatkan, E_{BD} sebanyak 13.31 MV cm^{-1}. Bagi struktur Ho/Ge teroksida/ternitrida pada 400 °C selama 10 minit menunjukkan maksimum $\Delta E_c \sim 2.47$ eV dan $\Delta E_v \sim 4.67$ eV mendorong $J_g \sim 10^{-5}$ A cm^{-2} terendah pada $E_{BD} \sim 8.59$ MV cm^{-1} yang tertinggi. Keputusan elektrik sampel ini juga menunjukkan pemalar dielektrik yang lebih tinggi, k sebanyak 31.19 dan 13.60 untuk struktur Sm_2O_3/IL/Ge dan Ho_2O_3/IL/Ge, masing-masing. Walaubagaimanapun, kedua-dua struktur mempamerkan ketumpatan perangkap antara muka yang tinggi, $D_{it} \sim 10^{13}$ eV^{-1}cm^{-2}. Selain itu, caj oksida, ketumpatan perangkap perlahan, histerisis juga dianggarkan daripada lengkung *C-V* dan dihubungkait dengan varians medan pecah tebat elektrik. Perbandingan sifat fizikal dan elektrik di antara sistem Sm/Ge dan Ho/Ge teroksida/ternitrida telah dilakukan. Sm_2O_3 boleh menjadi pilihan yang lebih baik untuk oksida dielektrik get tinggi untuk peranti MOS berasaskan Ge.

Kata kunci: nadir bumi, high-*k*, germanium, pengoksidaan/penitridaan terma, kapasitor MOS

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LIST OF SYMBOLS AND ABBREVIATIONS

ε_o	:	Permittivity of free space (Fm^{-1})
ε	:	Micro-strain
θ	:	Diffraction angle (°)
λ	:	Wavelength (cm^{-1})
μ	:	Carrier mobility ($cm^2V^{-1}s^{-1}$)
μ_e	:	Electron mobility ($cm^2V^{-1}s^{-1}$)
μ_h	:	Hole mobility ($cm^2V^{-1}s^{-1}$)
φ_s	:	Surface potential (eV)
A	:	Gate electrode area (cm^2)
C_{ox}	:	Oxide capacitance (μF)
D	:	Crystallite size (nm)
D_{it}	:	Interface trap density (ev^{-1} cm^{-1})
E	:	Electrical field (MV cm^{-1})
E_{BD}	:	Electrical breakdown field (MV cm^{-1})
E_g	:	Energy Band Gap (eV)
E_v	:	Valance band edge (eV)
ΔE_c	:	Conduction band offset (CBO) (eV)
ΔE_v	:	Valance band offset (VBO) (eV)
I	:	Current (A)
I_D	:	Drive current (A)
J_g	:	Leakage current density (A cm^{-1})
k	:	Dielectric constant
L	:	Channel length (cm)

t_{ox}	:	Oxide thickness (nm)
V_g	:	Gate voltage (V)
V_{FB}	:	Flatband voltage (V)
W	:	Channel Width
ALD	:	Atomic layer deposition
CVD	:	Chemical vapor deposition
CMOS	:	Complementary metal oxide semiconductor
CET	:	Capacitance equivalent thickness
EOT	:	Equivalent oxide thickness
HRTEM	:	High resolution transmission electron microscopy
IL	:	Interfacial layer
MBD	:	Molecular beam deposition
MOS	:	Metal oxide semiconductor
MOSFET	:	Metal Oxide semiconductor field effect transistor
PLD	:	Pulse Laser Deposition
PVD	:	Physical vapor deposition
PDA	:	Post deposition annealing
RTA	:	Rapid thermal annealing
REOs	:	Rare earth oxides
STD	:	Slow trap density
TMOs	:	Transitional metal oxide
XRD	:	X-Ray diffraction
XPS	:	X-Ray photoelectron spectroscopy

CHAPTER 1: INTRODUCTION

1.1 Background of Study

Complementary Metal oxide Semiconductor (CMOS) technology are progressing very rapidly to generate high performance and more speedy powerful electronic devices including transistors and capacitors. Aggressive development of Silicon (Si)-based complementary metal oxide semiconductor (CMOS) technology has immensely contributed to the semiconductor industry for decades. The advancement has been made according to the Gordon Moore's prediction of scaling where the number of components in an integrated circuit doubles every two years (Mack, 2011; Thompson & Parthasarathy, 2006). This substantial expansion of metal oxide semiconductor (MOS) technology entails ultrathin gate oxide ($\sim$ 1.2 nm or $4-5$ atomic layers) (Houssa et al., 2006; Robertson & Wallace, 2015). Hence a superior MOS with an ultrathin gate oxide functionality has become the potential demand. Till now SiO_2/Si gate stack has been serving the semiconductor industry due to its excellent insulating properties of native SiO_2 (Frank & Taur, 2002; Park & Kim, 2005; Wilk, Wallace, & Anthony, 2001). However, due to drastic downscaling of SiO_2/Si interface it has reached the potential limit, further downscaling led to large leakage current and degradation of interface quality. The increment of leakage current at an undesirable scale due to extreme reduction of oxide thickness ($\sim$ 1 nm) triggered substantial concern regarding reliability and static power dissipation which obstructs the demand of low power consumption devices. (Gordon, Becker, Hausmann, & Suh, 2001; He, Zhu, Sun, Wan, & Zhang, 2011; Robertson & Wallace, 2015). Hence, a physically thicker oxides with similar equivalent oxide thickness (*EOT*) are required to replace conventional SiO_2. Since for MOS devices the capacitance is directly proportion to dielectric constant, k and inversely proportional to gate oxide thickness, t_{ox} (Goley &

Hudait, 2014; Wong & Cheong, 2010). This led the interest toward high-*k* materials that can provide physically thicker oxide but provides same equivalent thickness as SiO_2. For the last 20 years, an immense progress has taken place on the selection criterion of high-*k* gate dielectrics on Si substrate while exploring their physical and electrical properties for integration of high performance CMOS devices (Chew et al., 2016; Cui, Tuokedaerhan, Cai, & Lu, 2022; Juan. Gao et al., 2016; He et al., 2011; Kaya & Yilmaz, 2015, 2019; J. S. Lee et al., 2014; Robertson, 2004; Shao et al., 2003; Wilk et al., 2001). However, deposition of high-*k* gate oxides on Si semiconductor are governed by several limitation which includes growth of thick interfacial layer, increment of fixed oxide charges, excessive charge trapping, large interface trap density and degradation of electron mobility. It is well known that for high-*k* gate dielectric tunneling current increases exponentially with reduction barrier height on the other hand the bandgap maintains an inversely proportional relationship proportional to dielectric constant which limits the choice of high-*k* material due to low bandgap issue (Wilk et al., 2001). Since, drive current, I_D is proportional to the carrier mobility μ and so superior mobility substrate is required (He et al., 2011). For consideration of high speed operation low hole carrier mobility Si limits device performance and so replacing Si with higher mobility semiconductor is an alternative to deliver high speed MOS applications. Accordingly, Germanium (Ge) has gained widespread interest to replace Si substrate due to its higher carrier mobility than Silicon (Kamata, 2008). Moreover, ease of integration process also added additional advantage towards Germanium. Thus, finding suitable combination of high-*k* gate oxide on Ge for the improvement of MOS device performance is one of the major scopes of this research.

1.2 Problem Statement

For past few generations, scaling of oxide thickness has been the key route to cater the demand of low power consumption and high-speed devices. In accordance with the current CMOS scaling, it is required to maintain higher capacitance between the integrated gate dielectric and substrate while reducing the oxide film thickness with a smaller gate area. Currently, CMOS technology reached the scaling limit in order of sub-100 nm regime and beyond (Wilk et al., 2001). Rapid downscaling of SiO_2/Si structure has pressed the SiO_2 thickness below 1.2 nm for sub-100 nm (Kurniawan, Cheong, Razak, Lockman, & Ahmad, 2011a; Wilk et al., 2001; Wong & Cheong, 2010). The physical thickness of SiO_2 has become thinner below the threshold of electron tunneling limit ($\sim$ 2 nm) which causes unacceptable gate leakage current density, J_g (exceeding 1 A cm^{-2} at $V_g = 1$V) due to oxide tunneling effect, limiting the low power application (Kamata, 2008; Robertson & Wallace, 2015). In addition, relatively low carrier hole mobility, (μ_h) in Si is another significant drawback for high-speed CMOS device operation (Kamata, 2008). To address this issue beside shrinking approach numerous alternative high mobility substrate materials from group IV and III-V with superior mobility have been extensively studied for replacement of SiO_2 (Del Alamo, 2011; Juan. Gao et al., 2017; He, Chen, & Sun, 2013). Germanium, (Ge) gained widespread interest due to having higher hole mobility, (μ_h) in contrast to other group IV and III-V which is (1900 cm^{2}V^{-1}s^{-1}) four times higher than Si. Moreover, the small bandgap of 0.67 eV enables formation of low resistance metal contacts which is advantageous for further voltage scaling in MOSFET devices (Kamata, 2008; Lei, Goh, Zainal Abidin, & Wong, 2017; Saraswat, Chui, Krishnamohan, Nayfeh, & McIntyre, 2005). It has been reported, current MOS scaling requires $EOT \sim 0.68$ nm which needs a $t_{ox} \sim 4.36$ nm for Ge substrate interfaces (Goley & Hudait, 2014).

Unfortunately, the interface quality of native oxide GeO_2/Ge is highly unstable in counter to SiO_2/Si interface within the CMOS scaling limit. It has been identified that the quality of Ge MOS interface degrades mainly due to hygroscopic nature of GeO_2 and deteriorating tendency of GeO_2 into detrimental Ge−O species during thermal processing even below 420 ^oC thus degrading the electrical properties (Kita et al., 2008; Prabhakaran, Maeda, Watanabe, & Ogino, 2000). In addition, GeO_2 possess a low conduction band offset of 1 eV or less with a small dielectric constant ($k \sim 5-7$) which is a prominent obstacle in scaling for the expected CMOS devices (Chroneos, Schwingenschlögl, & Dimoulas, 2012). Therefore, the major issue regarding Ge is to maintain the integrity of GeO_2, while having ultra-thin GeO_2 interface without degradation of electrical properties.

Fortunately, the continuous development of high-*k* gate dielectrics has brought the opportunity to utilize both geometry of high-*k* and Ge together. Deposition of high-*k* materials on Ge substrate was expected to improve the imperfection of native oxide as well as would comply with the scaling limit. Several high-*k* materials have been extensively on Ge including transitional metal oxides (TMOs) hafnium oxide, HfO_2 (Oh et al., 2015; Venkata Rao et al., 2018), Aluminum oxide, Al_2O_3 (Botzakaki et al., 2018; X. Yang et al., 2014) Zirconium oxide, ZrO_2 (Lei et al., 2017; Lei, Zainal Abidin, & Wong, 2018) and rare earth oxides (REOs) such as Lanthanum oxide, La_2O_3 (Mavrou et al., 2007; J. Song et al., 2009), cerium oxide, CeO_2 (Brunco et al., 2007), Gadolinium oxide Gd_2O_3, (Evangelou, Rahman, & Dimoulas, 2009), Yttrium oxide, Y_2O_3 (Nishimura et al., 2011; Seo et al., 2017; Zimmermann, Bethge, Winkler, Lutzer, & Bertagnolli, 2016), Thulium oxide, tm_2O_3 (Zurauskaitea et al., 2018), Samarium oxide, Sm_2O_3 (C. C. Lin, Wu, Wu, & Lee, 2014) has been widely studied to improve the MOS device. It has been reported that REOs were found to be more Ge friendly in improving electrical properties and thermodynamic stability in compare to transitional metal oxides (Chroneos et al., 2012; Houssa, Pourtois, Caymax, Meuris, & Heyns, 2008; Lu et al., 2014). The key reason for such

improvement has been pointed due to–spontaneous growth of rare earth germanate (RE−O−Ge) interfacial layer (IL) caused by catalytic oxidation of Ge atoms through the vigorous reaction between REOs and Ge interface (Chroneos et al., 2012; Zhao, Liu, Wang, Wang, & Wang, 2018). However, a complete MOS device based on REOs/Ge which can compete the superior features of SiO_2/Si is still an open question. Although REOs have emerged as potential contenders for high-*k* material but yet but many of high-*k* metal oxides (both TMOs and REOs) in Germanium still suffers from high thermodynamic instability, large leakage current density J_g, poor *C*-*V* characteristics, low recrystallization temperature and high interface trap density, D_{it} in compare to conventional SiO_2 (Dimoulas et al., 2007; Evangelou, Mavrou, Dimoulas, & Konofaos, 2007; Goley & Hudait, 2014; Kamata, 2008; Venkata Rao et al., 2018). For instance, La_2O_3 exhibits low $D_{it} \sim 10^{11}$ eV^{-1} cm^{-2} and well-shaped *C*-*V* (capacitance – voltage) curve, but with an expense of large gate leakage $J_g \sim 10^{-1}$ A cm^{-2} with lower $k \sim 9$ which conflicts with the requisite of scaling (Mavrou, Galata, et al., 2008). Moreover, another major concern for REOs is their hygroscopic characteristic, which influences adversely on MOS scaling by causing increment of physical thickness and reduction of dielectric constant (Chin, Cheong, & Hassan, 2010). Thus, selection of suitable high-*k*/Ge gate stack with coordination of good interfacial and electrical properties is still a key challenge.

Among these oxides, Sm_2O_3 can be a potential choice of high-*k* gate oxide material to be integrated on Ge substrate due to its relatively high dielectric constant, k value (7 – 18), which is the second highest among the REO below La_2O_3, large energy band gap, $E_g \sim$ (4.33 eV), high electrical breakdown field, E_{BD} (5 MV cm^{-1} to 7 MV cm^{-1}) and conduction band offset, CBO (ΔE_c) ~ 2.7 eV with Si (Goh, Haseeb, & Wong, 2016b; C. C. Lin et al., 2014). Moreover, Sm_2O_3 possesses less hygroscopic nature because of its less electro-positivity due to small ionic radius (Goh, Haseeb, & Wong, 2017a). Numerous investigations of Sm_2O_3 have revealed well behaved electrical characteristics and

thermodynamic stability when it is employed on Si substrate (Chin & Cheong, 2011; Goh et al., 2016b; Pan & Huang, 2010). Conversely, there are very limited investigation of Sm_2O_3 on Ge substrate. C.C Lin et al., (2014) reported the growth and electrical properties of Sm_2O_3 on Ge substrate, deposited via e-beam evaporator followed by furnace annealing. The investigation has demonstrated that post-annealing of Sm_2O_3 on Ge reduces average interface trap density D_{it} in the order of 10^{11} eV^{-1} cm^{-2}, increase gate capacitance with less frequency dispersion and exhibits significantly low equivalent oxide thickness, $EOT \sim 0.61$ nm. The improvement was reasoned due to formation samarium germanate ($SmGeO_x$) interfacial layer (IL). Moreover, it was predicted that the fourfold coordinated configuration of Samarium (Sm) in the GeO_2 network was advantageous in passivating Ge dangling bonds to improve the electrical characteristics. (C. C. Lin et al., 2014). Since there is very limited study on Sm_2O_3/Ge gate stack and the reported investigation provides partial insight on Sm_2O_3/Ge, henceforth this material is considered for further investigation.

Another alternative REO is Holmium oxide (Ho_2O_3) can also be a potential candidate for transforming into MOS gate stack, since this material entails a moderate dielectric constant $k \sim 13$ and bandgap energy, E_g (5.3 eV), conduction band offset, CBO (ΔE_c) ~ (2 eV) with respect to Si substrate (Pan, Chang, & Chiu, 2010). Ho_2O_3 indicates least hygroscopic nature among (REOs) due to owing higher electronegativity and lattice energy. Despite of having such potential characteristics, the investigation on Ho_2O_3 based MOS devices are very scarce. Pan, Chang, et al., (2010) has demonstrated inspiring outcome in terms of electrical and thermal properties for Ho_2O_3/Si gate stack MOS device. However, there is no pertinent investigation of Ho_2O_3 as dielectric material for Ge based MOS devices. Therefore, beside Sm_2O_3 the investigation will also consider Ho_2O_3 for realization of High-*k*/Ge gate stack.

So far, several studies have demonstrated that incorporation of nitrogen (N) is an efficient technique to improve chemical and thermodynamic stability of oxide/Ge interface (Dushaq, Nayfeh, & Rasras, 2018; Fukuda, Okamoto, Iwasaki, Otani, & Ono, 2011; Maeda et al., 2004, 2006; Yi, Chang-Liao, Hsu, & Huang, 2018). It was found that incorporation of nitrogen effectively passivates Ge dangling bond and suppresses oxygen (O) diffusion by forming Ge−N /Ge−O−N interfacial layer which blocks the formation unstable Ge−O species in some extent and thus reducing leakage current density increasing capacitance and the interface quality (Kutsuki, Okamoto, Hosoi, Shimura, & Watanabe, 2009; Maeda, Nishizawa, Morita, & Takagi, 2007; Otani et al., 2007). N_2O and NO are commonly used gases for CMOS fabrication using thermal oxidation and nitridation in semiconductor industry. N_2O was selected for this study because it has less toxic nature higher activation energy than NO (Lei et al., 2018). Besides, a sputtering process with pure metal followed by thermal oxidation and nitridation in N_2O ambient has shown promising outcome forming stoichiometric metal oxide and improving electrical characteristics for both Ge and Si substrate (Lei et al., 2018; Wong & Cheong, 2011b, 2011c). However, there is no substantial investigation on thermal oxidation and nitridation using N_2O for sputtered Samarium (Sm) and Holmium (Ho) into Ge substrate. Nonetheless, oxide film and interfacial layer quality as well as the electrical properties can be significantly influenced by the oxidation ambient, deposition temperature, deposition duration and type of substrate (Goh, Haseeb, & Wong, 2016a; Hetherin, Ramesh, & Wong, 2017a; Lei et al., 2017; Wong & Cheong, 2012a) . Therefore, it is imperative to investigate the effect of oxidation/nitridation (N_2O ambient) while varying deposition temperatures and durations of sputtered Samarium on Germanium (Sm/Ge) and Holmium on Germanium (Ho/Ge) system.

1.3 Objective of the Research

The main purpose of this study is to develop Samarium oxide (Sm_2O_3)/Ge and Holmium oxide (Ho_2O_3)/Ge based gate stack using metal sputtering followed by thermal oxidation/nitridation (oxy-nitridation) within current MOS scaling trend corresponding to high electrical performance and greater thermodynamic stability. The following goals are to be attained for this research.

1. To investigate the effect of various temperatures and durations on the chemical, structural, and electrical properties of sputtered pure Samarium (Sm) metal on Ge substrate following thermal oxidation/nitridation in N_2O ambient.
2. To investigate the influence of various thermal oxidation/nitridation durations on the chemical, structural, and electrical properties of pure Holmium (Ho) metal on substrate Ge in N_2O ambient.
3. To determine the band alignment mapping of both thermally oxidized/nitrided Sm_2O_3/Ge and Ho_2O_3/Ge gate stack.
4. To develop a possible mechanism model of thermal oxidation/nitridation to demonstrate the growth of the thermally oxidized/nitrided sputtered pure Sm thin film on Ge substrate as well as for the thermally oxidized/nitrided sputtered pure Ho thin film sputtered on Ge substrate.
5. To compare physical and electrical properties between thermally oxidized/nitrided sputtered pure Sm/Ge and Ho/Ge.

1.4 Scope of Study

This investigation aims on the deposition of sputtered Sm/Ge and Ho/Ge using radio frequency (RF) Physical Vapor Deposition (PVD). Sm_2O_3 and Ho_2O_3 gate dielectric layer is expected to form after thermal oxidation/nitridation of sputtered Sm/Ge and Ho/Ge. Several variables will be investigated in this study which includes (i) effect of thermal oxidation/nitridation in N_2O gas ambient for several temperatures of sputtered Sm/Ge (ii) Influence of different thermal oxidation/nitridation durations on sputtered Sm/Ge in N_2O gas ambient (iii) Influence of different thermal oxidation/nitridation durations in N_2O gas ambient for sputtered Ho/Ge. Chemical and structural properties will be analyzed using X-Ray Diffraction (XRD), X-Ray Photoelectron Spectroscopy (XPS), RAMAN Spectroscopy, High Resolution Transmission Electron Microscopy (HRTEM). Meanwhile the electrical properties will be determined from Semiconductor Characterization System (SCS).

1.5 Structure of Thesis

This thesis is segmented into five chapters. Chapter 1 provides a brief introduction based on the research gap and main objectives of this research. Chapter 2 discusses the relevant theory and previous works associated to the development of MOS technology. The experimental design and process flow, required equipment, experimental procedures, and characterization techniques has been discussed in chapter 3. The chapter 4 discusses experimental findings which incorporates detail analysis and comparison with previous reported works. Chapter 5 concludes and summarizes the investigations of this study along with recommendation for future research.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

Due to aggressive downscaling of SiO_2/Si based MOS technology SiO_2 has reached its potential limit and further downscaling led to degradation of thermal and electrical properties of the downscaled devices. Accordingly, improvement in the structure of transistor and incorporation new materials has become the key route for increasing MOS technology and field-effect transistors (FETs) performance for last few generations. Immense progress has been made by the introduction of high-*k* materials and by re-implementing Germanium (Ge) based gate stacks in recent years. Nevertheless, numerous challenges have been introduced for high-*k*/Ge interface which includes suitability of dielectrics on Ge, complexities in deposition methods and incompatibility of metal gate and high-*k* interface. Based on current progress trends and fundamental considerations, the literature review chapter includes brief discussion on current MOS scaling trend, limitation of Si based MOS technology, requirements for high-*k* material. This chapter also reviews superior properties of Germanium as alternative substrate material and concerns regarding native GEO_2. Following that commonly used transitional metal oxides (TMOs) as high-*k* dielectrics on Ge has been documented. As rare earth oxides (REOs) as high-*k* has been the key route of this study, so this chapter also describes selection criteria of rare earth oxides (REOs), common deposition methods of REOs and subsequently, performance of several materials from lanthanide group has been reviewed for integration into REOs/Ge MOS application. Since Sm_2O_3 and Ho_2O_3 was selected for this study and so this chapter pays particular consideration in reviewing the physical characteristics, elec-

trical features, and various deposition techniques as high-*k* oxides. Lastly, role of incorporating nitrogen (N) during the fabrication process of gate oxides into Ge has been described.

2.2 Moore's Law and MOS Scaling Trend

The device downscaling of Si based metal-oxide field effect transistor (MOSFET) has become inevitable to cater the increasing demand of low power consumption, high speed operation, high performance device reliability, and indeed lowering the cost of MOSFET devices (Thompson & Parthasarathy, 2006; Wilk et al., 2001). This advancement has been made according to the Gordon Moore's prediction of scaling. In 1965, Gordon Moore the founder of intel predicted that the quantity of transistors in an integrated circuits (ICs) will be double every two years (Mack, 2011). For past few decades the components of an integrated circuited was truly doubled about every 18 months. Corresponding to this prediction for every technology generation the channel length should reduce 0.7 times. In 1970s, the channel length was downscaled to 8 μm. Following the downscaling trend in year 2003 the channel length reached nano-meter scale (Radamson, H. & Thylen, 2014). As the density of transistor increased exponentially the quantity eventually transistor per chip also experienced an exponential growth. In 1975 quantity of transistors per chip was 16000 which now turned in a range above a billion (Mack, 2011). The evolution of transistor gate length from 1970 to 2030 is shown in Fig. 2.1. Since planar Si MOS have confronted its scaling limit under gate length of 20 nm and breakthrough is essential for further expansion. In the modern CMOS scaling the technology node has reached sub-100 nm and beyond (Chin et al., 2010; He et al., 2013; Ieong, Doris, Kedzierski, Rim, & Yang, 2004; Kurniawan et al., 2011a). It has been reported that according to the current MOS scaling trend the gate oxide should be scaled down at a physical gate oxide thickness of 1.5 nm at maximum gate leakage allowance

of 1.5×10^{-2} A cm^{-2} a gate voltage, V_g of 1V without sacrificing the breakdown voltage (Ieong et al., 2004; Muller et al., 1999; Robertson & Wallace, 2015). Table 2.1 displays the downscaling evolution where the native SiO_2 could serve as gate insulation oxide up to it reached 90 nm. Afterwards SION substituted the pure native SiO_2. In future it is expected that new high-*k* element will swap SiON. Nevertheless, the physical oxide thickness remained at 5 atomic layers in order to inhibit the QMDT current conduction (Sicard & Aziz, 2011).

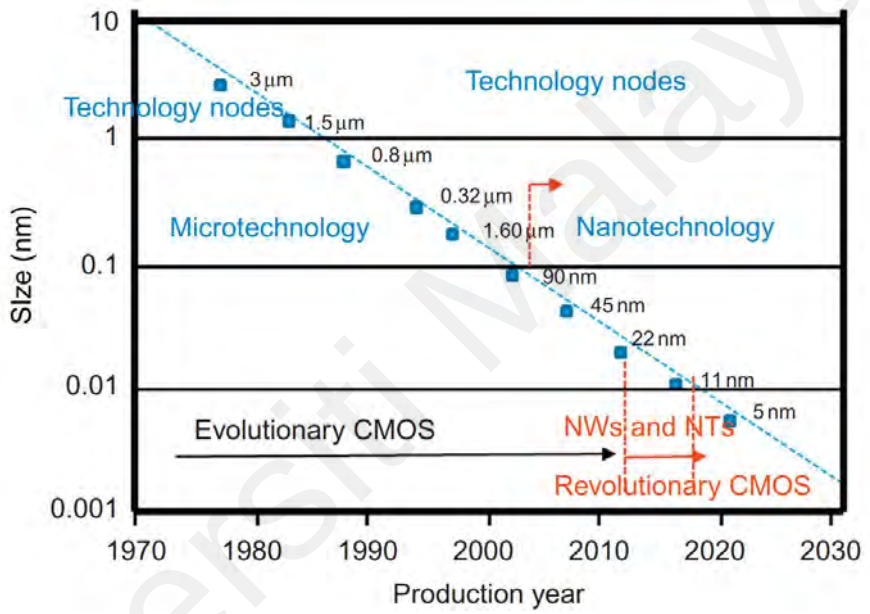

Figure 2.1: Evolution of transistor gate length from 1970 to 2030 (Radamson, H. & Thylen, 2014).

Table 2.1: CMOS technology node evolution (Sicard & Aziz, 2011).

Technology node	**0.18 µm**	**0.13 µm**	**90 nm**	**65 nm**	**45 nm**	**32 nm**	**22 nm**
Gate length	130	70	50	35	25	17	12
Gate atoms	10	8	5	5	5-10	5-10	5-10
Gate material	Poly SiO_2	Poly SiO_2	Poly SiO_2	Poly SION	Metal High-*k*	Metal High-*k*	Metal High-*k*
Manufacture year expected	1999	2001	2003	2005	2007	2008	2011

2.3 Basic Principle of MOS and MOSFET

In order to understand the fundamentals of MOS scaling it is vital to recall the basic structure of MOS capacitor and a MOSFET. A typical MOS structure arrangement with stacking layer is shown in Fig. 2.2a where gate oxide layer is inserted between gate electrode and substrate. I_{in} denotes the input current while I_{out} indicates the output current. The functionality of a capacitor basically based on capacitances induced due to insulation properties of gate oxide. On the other hand, typically, a MOSFET consists of three building blocks which includes gate (G), source (S) and drain (D) as shown in Fig. 2.2b. In operation of MOSFET applied voltage in the gate capacitor junction controls the device performance. Depending on the applied gate voltage, a positive or negative charges are introduced in the channel region underneath the gate capacitor. According to the polarity of carriers induced in the channel region, the nodes of drain and source either connects or isolates (He et al., 2011; Taur, 2002). The extent of induced charge (Q) induced across the channel region is a combination of gate capacitance (C_{ox}) and applied gate voltage (V) which can be expressed by Eq. 2.1 (Goley & Hudait, 2014)

$$\boldsymbol{Q = C_{ox}V} \qquad \text{(Equation. 2.1)}$$

The gate capacitance, ($\boldsymbol{C_{ox}}$) of a parallel plate MOS capacitor can be expressed by Eq. 2.2 (Goley & Hudait, 2014; Houssa et al., 2006; Robertson & Wallace, 2015).

$$\boldsymbol{C_{SiO_2} = \frac{k_{SiO_2}\,\varepsilon_o\,A}{t_{SiO_2}}} \qquad \text{(Equation. 2.2)}$$

Where, $k_{\boldsymbol{SiO_2}}$ is the relative dielectric constant of SiO_2, ε_0 is the permittivity of free space, t_{SiO_2} is the physical oxide thickness of SiO_2 and A is the area of gate electrode.

Another important constraint of MOSFET device operation is to maintain high drive current between drain-source nodes along the channel region. The relationship of drive current, I_D and gate capacitance can be given by Eq. 2.3 (Taur, 2002).

$$\boldsymbol{I_D = \frac{W}{L}\,\mu C_{ox}(V_G - V_T)^2} \qquad \text{(Equation. 2.3)}$$

Where, I_D = Drive current, W = Channel width, L = Channel Length, C_{ox} = Gate capacitance, V_T = Threshold voltage, V_G = Gate voltage, μ = Carrier mobility. From Eq. 2.2 and 2.3 it is apparent that, reduction of channel length and physical oxide thickness of the MOSFET dimensions enables to increase the drive current between drain and source region. Instinctually, shrinkage of t_{ox} increases C_{ox} and hence the of amount induced charged in the channel region is increased, while the reduction of L reduces the travelling distance of the induced charges to initiate current flow. Reduction of the gate oxide thickness along with the channel length also facilitates to retain the gate electrode's control on the short channel effects. Based on Eq. 2.2, the gate electrode area (A) is constant and so reduction of gate oxide thickness is the most preferrable way to increase gate capacitance which ultimately attributes to maintain high drive current in the channel region. Accordingly, shrinkage of oxide thickness technology has been considered as the key route for device downscaling for last few decades. Tremendous advancement of planer Si-CMOS has been driven by the capability of continual shrinkage of these critical dimensions due to excellent insulating properties of native SiO_2 (Hirose et al., 2000). It is obvious that the potentiality of most reliable SiO_2/Si interface that has been used in today's semiconductor industry will sooner reach limits of scaling, thus introducing a major question towards the sustainability for continuity of device miniaturization.

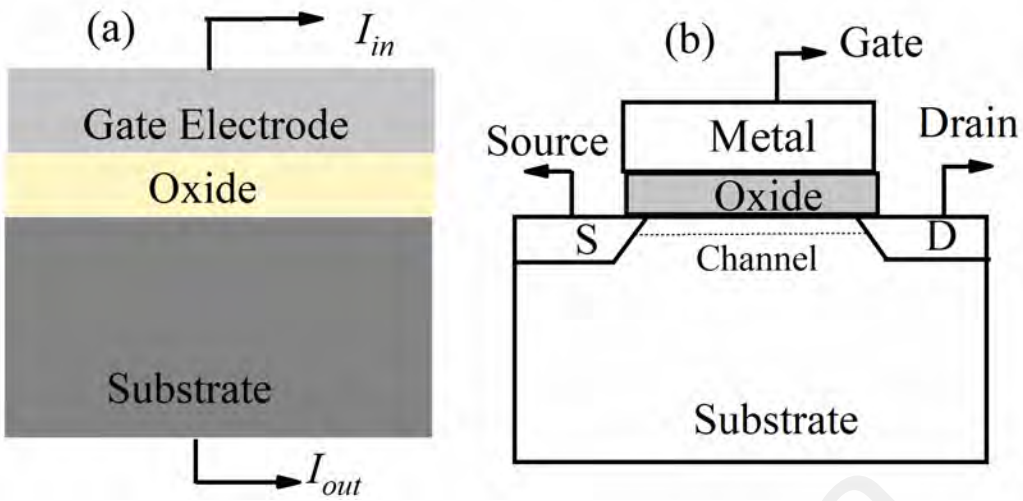

Figure 2.2: (a) Typical MOS capacitor stacking arrangement (b) Conventional structure of a MOSFET.

2.4 Limitations of SiO_2/Si Scaling

It has been reported that SiO_2/Si exhibits low interface trap density, $D_{it} \sim 10^{11}$ eV^{-1} cm^{-2}, leakage current density, $J_g \sim 1 \times 10^{-12}$ A cm^{-2} and electrical breakdown field, $E_{BD} \sim 15$ MV cm^{-1} with high thermodynamic stability. (Houssa et al., 2006; Park & Kim, 2005; Wilk et al., 2001). Despite of owing such outstanding properties further downscaling of SiO_2 is confronting significant challenges to comply with the current scaling trend. The main issue of SiO_2 based metal oxide semiconductor (MOS) downscaling is associated with SiO_2 layer thickness and electron tunneling mechanism which exponentially increases leakage current density with the decrease of SiO_2 thickness (Cui et al., 2022; D. Wang, He, Fang, et al., 2019). It has been reported that, aggressive downscaling of SiO_2/Si interface below 1.2 nm causes direct tunneling effect resulting in an unacceptably higher gate leakage current density (> 1 A cm^{-2} at 1 V) (He et al., 2011; Kurniawan et al., 2011a; Robertson, 2004; D. Wang, He, Hao, Gao, & Zhang, 2019). This has been reasoned that due to drastic downscaling the oxide thickness has become so thin that, it has reached the electrons tunneling limit of ~ 2 nm which allows electron to penetrate through SiO_2 layer without passing through the conduction band (Goley & Hudait, 2014; Kamata, 2008). It is notable that for SiO_2/Si interface $J_g \sim 1 \times 10^{-12}$ A cm^{-2} for 3 nm

oxide thickness which increased to unacceptably higher of $J_g \sim 1$ A cm^{-2} (twelve order magnitude higher) when thickness reduced to 1.5 nm (Lo, Buchanan, Taur, & Wang, 1997; Robertson, 2004). Over and above the drastic downscaling of SiO_2 also springs up difficulty in manufacturing such thin oxide layer while maintain thickness reliability issue. When the oxide layer reaches such thin thickness critical defect density at the SiO_2/Si interface has been introduced by the flow of excessive charge carriers during MOSFET operation leading to the breakdown of SiO_2/Si gate unit (He et al., 2011). Consequently, the increment of leakage current expands the thermal load of the MOS device which brings severe challenges to the aim of developing low power consumption energy efficient devices. Thus, the relationship established in Eq. 2.2 motivates to increase gate capacitance, C_{ox} by increasing the dielectric constant, k value while the oxide thickness cannot be reduced further, and the gate area remains constant. Hence, alternative material with higher permittivity known as high-*k* is required for replacement of SiO_2 (H. D. Kim & Roh, 2006; Wilk et al., 2001; Wong & Cheong, 2010). Additionally, the low hole mobility (μ_h) of Si is another potential drawback on the way to high-speed CMOS devices (Frank & Taur, 2002; Kamata, 2008). From Eq. 2.3, it is obvious that high carrier mobility, μ is a potential factor on the way to high-speed device operation. Accordingly, replacement of Si substrate with alternative higher carrier mobility substrate and high-*k* dielectric material is a potential solution on way to realization of low power consumption and high-speed devices within the scaling trend.

2.5 Requirements for Implementing High-*k* Gate Oxide

The crucial purpose of high-*k* oxides is to obtain larger physical oxide thickness while obtaining similar capacitance as of SiO_2 by increasing the dielectric permittivity *k* value of new dielectric material following Eq. 2.2. The high-*k* gate stack provides benefit to obtain physically thicker oxide layer equivalent to SiO_2 thickness as shown in Fig.2.3.

It has been reported that, using high-*k* dielectric material reduces gate leakage between dielectric oxide layer and the substrate (Liang et al., 2018; D. Wang, He, Fang, et al., 2019). This is because high-*k* leads to physically thicker oxide material which could be barrier for electron tunneling through dielectric layer (Goley & Hudait, 2014). Since further downscaling SiO_2 below 1.2 nm is no longer applicable, the new suitable high-*k* oxide should maintain a convenient equivalent oxide thickness, (*EOT*) calculated according to Eq. 2.4 (Goley & Hudait, 2014; Robertson & Wallace, 2015).

$$\boldsymbol{t_{ox} = EOT = \left(\frac{3.9}{k_{high-k}}\right) t_{high-k}} \qquad \text{(Equation 2.4)}$$

Where, k_{high-k} is the dielectric permittivity of new high-*k* material, t_{high-k} is the physical oxide thickness of new high-*k* dielectric material. For the purposes to retain gate oxide thickness of 1.2 nm or to further downscale the *EOT* the thickness of high-*k* or/and the *k* value could be enhanced (Sharma, Kumar, & Anthony, 2001; Wong & Cheong, 2010). Fig.2.4 illustrates the benefit of employing high-*k* in terms of mitigation of gate leakage between insulator and the substrate layer for MOS devices.

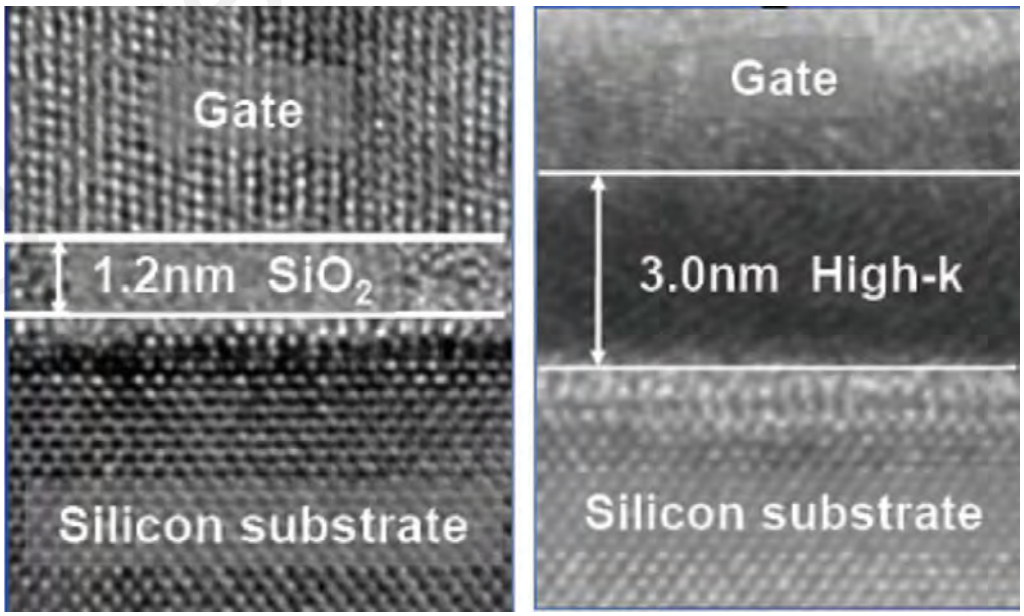

Figure 2.3: TEM image of SiO_2/Si and HfO_2/Si gate stack thickness (Robertson & Wallace, 2015).

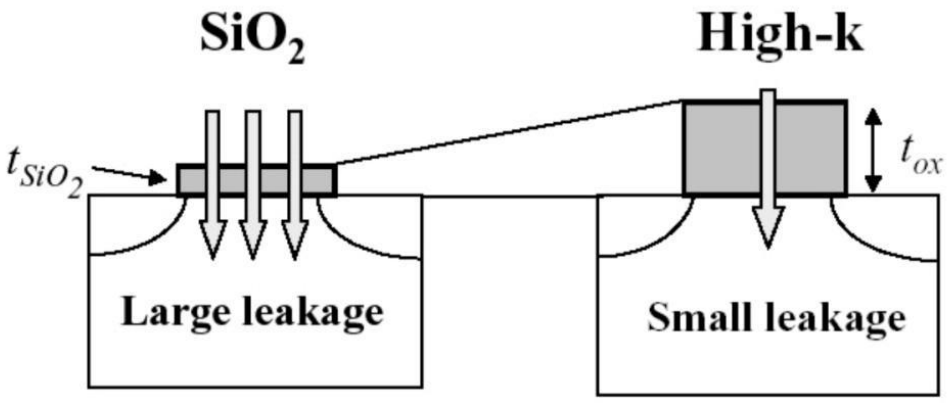

Figure 2.4: Advantage of using high-*k* as gate material to reduce leakage current.

However, reduction of only t_{high-k} using ultra-thin gate high-*k* oxides could not resolve the problem of gate leakage current owing to direct electron tunneling thus, selection of high-*k* material with large k value is the key route to mitigate this problem In order to be applicable for dielectric oxide for MOS integration the selection of high-*k* should retain k value ranging from $10 - 30$. (Engstrom et al., 2007; Gillen & Robertson, 2013; Goh et al., 2017a). However, selection of k value should not be larger than 25 because very large k enhances the thickness of gate oxide beyond the dimension of gate channel length which diminishes the gate control on channel region. Eventually, degrade the FET device performance owing to short channel effect. (He et al., 2011; Houssa et al., 2006). It is well known that dielectric tunneling current is dependent on barrier height of oxide/substrate interface where reduction of barrier height exponentially increases the leakage current. Thus, it is required to have a higher conduction band offset (CBO) > 1 eV which could retain a moderate barrier height to impede the direct tunneling of electron into conduction band of high-*k* material that causes unacceptable leakage of the device. In order to achieve large CBO with the semiconductor substrate it is important to select high-*k* material with higher bandgap. It has been suggested that, a higher bandgap, E_g > 5 eV is preferably acceptable for high-*k* gate oxides. (Houssa et al., 2006; Robertson, 2006; Robertson & Wallace, 2015). Fig. 2.5 shows the trend of bandgap of high-*k* dielec-

trics with respect to dielectric constant where the bandgap shows an inversely proportional relationship to dielectric constant. Consequently, range of selecting high-*k* dielectric material is being restricted due to low bandgap dispute which would hamper the aim to retain large CBO requirement.

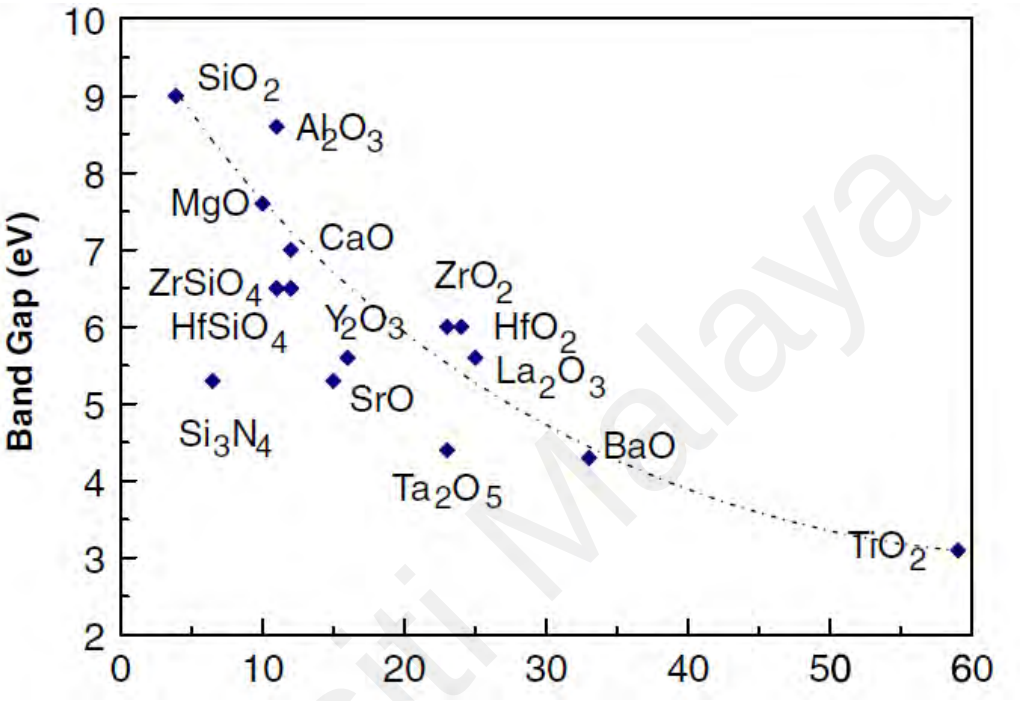

Figure 2.5: Trend of bandgap of high-*k* dielectrics with respect to dielectric constant (Wilk et al., 2001).

In addition, the high-*k* should maintain good interface quality and thermodynamic stability with the substrate material, superior film morphology, and compatibility with the current integration in order to be used for current and future CMOS technology (Kamata, 2008; Kaya & Yilmaz, 2019). For Ge based MOS device *EOT* limit has reached 0.68 nm. In order to serve this purpose a high-*k* material corresponds to physical oxide thickness $t_{ox} \sim 4.36$ nm with dielectric constant $k \sim 20$ is required. The following key requirements should be fulfilled for being applicable for high-*k* dielectric gate oxide material. (Goley & Hudait, 2014; Robertson & Wallace, 2015).

1. Meet the scaling trend set by ITRS of low equivalent oxide thickness.
2. The leakage current density must not exceed $J_g \sim 1.5 \times 10^{-2}$ A cm^{-2} at $V_g \sim 1$V.
3. Should have high enough conduction band offset and valance band offset (at least 1 eV for both).
4. Should exhibit low interface trap density D_{it} (less than 10^{11} cm^{-2}·eV^{-1}).
5. Acceptable high dielectric electric breakdown field, E_{BD}
6. Thermodynamic and kinetic stability.

Several high-*k* gate oxides such as Al_2O_3,(I. S. Jeon et al., 2003; Lale et al., 2021; Rahman, Kim, Kim, & Kim, 2019; Shao et al., 2003), ZrO_2 (Chew et al., 2016; H. D. Kim & Roh, 2006; Shuan Li et al., 2020; Weinreich et al., 2009; Wong & Cheong, 2011b), HfO_2 (Choi, Shin, Park, & Yoon, 2001; Liang et al., 2018; Park & Kim, 2005; Srivastava, Nahar, & Sarkar, 2011; Tan, 2010; Tirmali, Khairnar, Joshi, Electronics, & 2011, 2011), La_2O_3 (Fei, Liu, Wang, Zhao, & Wang, 2016; Jun, Jun, Wang, Won, & Choi, 2002; Ramana et al., 2011; Schamm et al., 2009; J. Q. Song, Qian, & Lai, 2018), Y_2O_3 (Evangelou, Wiemer, Fanciulli, Sethu, & Cranton, 2003; Ioannou-Sougleridis et al., 2004; Pan & Lee, 2007; Quah & Cheong, 2015), Ta_2O_5 (Rao, Verma, & Singh, 2015; Spassov, Atanassova, & Virovska, 2006), TiO_2 (Gullu & Yildiz, 2021; Nagabharana, Kumaraswamy, Gundanna, Susheel, & Umananda, 2020; Sekhar, Nanda Kumar Reddy, Venkata Rao, Mohan Rao, & Uthanna, 2014) and Gd_2O_3 (S. Li et al., 2019) were widely investigated on Si substrate for replacing SiO_2 in realization of advanced MOS technology. However, high-*k*/Si are subjected to several limitations (Chin et al., 2010; Leskela, Kukli, & Ritala, 2006; Wong & Cheong, 2010). Previous researchers has classified some major limitations which includes (i) growth of interfacial layer during fabrication period and afterwards at the point of post deposition annealing (Kurniawan, Cheong, Razak, Lockman, & Ahmad, 2011b; Ma & Zhang, 2008; Wong & Cheong, 2010) (ii) lateral oxidation takes place at the edge of oxide interface and development of micro crystal

during heat treatment (Iwai et al., 2002) (iii) dielectric defects caused by the precursors used during chemical vapor deposition (Choi et al., 2001) (iv) existence of fixed charges which shifts the flatband voltage and large interface trap density (Juan. Gao et al., 2016; Iwai et al., 2002; Loo et al., 2005; Naumann, Otto, Wehrspohn, Werner, & Hagendorf, 2012; Wong & Cheong, 2011b). (v) lowering of conduction band offset with respect Si (Alers et al., 1998; Robertson & Wallace, 2015; Shao et al., 2003). Moreover, low-*k* value and increment of overall dielectric thickness by the expansion of additional interfacial thickness made it challenging to utilize these metal oxides with Si interface under the current MOS scaling trend below 1.2 nm (He et al., 2011; Houssa et al., 2006). Therefore, combination of high-*k* with alternative substrate material intended to replace SiO_2 and Si substrate is the potential aspect for this research.

2.6 Ge as Alternative Substrate Material

The continuous progress of integrated circuit (IC) efficiency through device miniaturization has been the key route for the rapid success of semiconductor micro-electronics industry. Currently, several materials such as Germanium (Ge), strained $Si_{1-x}Ge_x$ and III−V group compounds have been widely investigated to replace Si in order to continue the miniaturization of CMOS device (Del Alamo, 2011; Kamata, 2008; Simoen et al., 2012; J. Q. Song et al., 2018; Yao et al., 2021). It is well known that CMOS technology is a combination of NMOS and PMOS components, and so both high electron mobility μ_e and high hole mobility μ_h is required. Due to low μ_h of Si, integration PMOS devices is bottle-neck for further development. In this regard mobility enhancement through strained technology has been subjected to limitations due to lattice mismatch, threading dislocations, thermal budget mismatch and abrupt change in conduction band. Shifting on the III−V compounds NMOS device has been successfully integrated due to its high electron mobility μ_e while integration of PMOS still remains a key challenge. This fact

is reasoned due to large discrepancy between μ_e and μ_h in III−V compounds where the μ_e several times larger than μ_h (Del Alamo, 2011; Juan. Gao et al., 2016; Goley & Hudait, 2014; He et al., 2013; Simoen et al., 2012). According to Table 2.2, among all the alternative material Ge has gained widespread due to its higher electron mobility which is 2 × μ_e(Si) and hole mobility 4 × μ_h(Si) (Kamata, 2008). Ge also maintains smaller band gap ~ 0.67eV which will be advantageous for scaling supply voltage, V_T (Saraswat et al., 2005). It is expected that replacing Si with Ge would reduce the amount of power consumption and enhance the high-speed operation for PMOS device. Based on these backgrounds, it can be accepted that Ge would be the best choice to replace Si for further miniaturization of CMOS devices.

Table 2.2: Electron mobility, μ_e and hole mobility, μ_h of different semiconductor materials (Kamata, 2008).

Semiconductor Material	μ_e (cm²/Vs)	μ_h cm²/Vs
Si	1400	450
Ge	3900	1900
GaAs (III−V)	8500	400
InP (III−V)	4600	650

2.6.1 Issues in growth of Native GeO_2

Although Ge has attracted more attention due to its superior carrier mobility, however, it has turned challenging to realize in practical applications. This is because the native, GeO_2 is not that thermodynamically stable as SiO_2. While comparing Si and Ge as substrate material it was found that the native oxide GeO_2 of Ge grows faster than that of SiO_2 when exposed to air (Kita et al., 2008; Sahari et al., 2013).

It was pointed that the thickness of native GeO_2 increases 0.4 nm with 10 min after exposure to air at 24 °C. The thickness of GeO_2 increases between growth rate of 0.2 nm – 0.3 nm with an interval of 10 minute per step as shown in Fig. 2.6. This variation has been attributed to the layered growth phenomenon of GeO_2 and the bond length of Ge–O which was about 0.2 nm. It was also observed that the growth rate of n-Ge (100) orientation is faster than the p-Ge (100) which indicates a more stable surface for p-Ge (100) (Sahari et al., 2013). Since the native oxide of Ge deteriorates the electrical performance of MOS devices hence it is required to clean the wafer surface for eliminating the detrimental native GeO_2 prior to deposition of dielectric film into Ge. For the cleaning of bare Ge surface all halogen acids which includes, hydrochloric acid (HCL), hydrofluoric acid (HF) and hydroiodic acid (HI) could be utilized to remove the native GeO_2 and other impurities of Ge (Kamata, 2008).

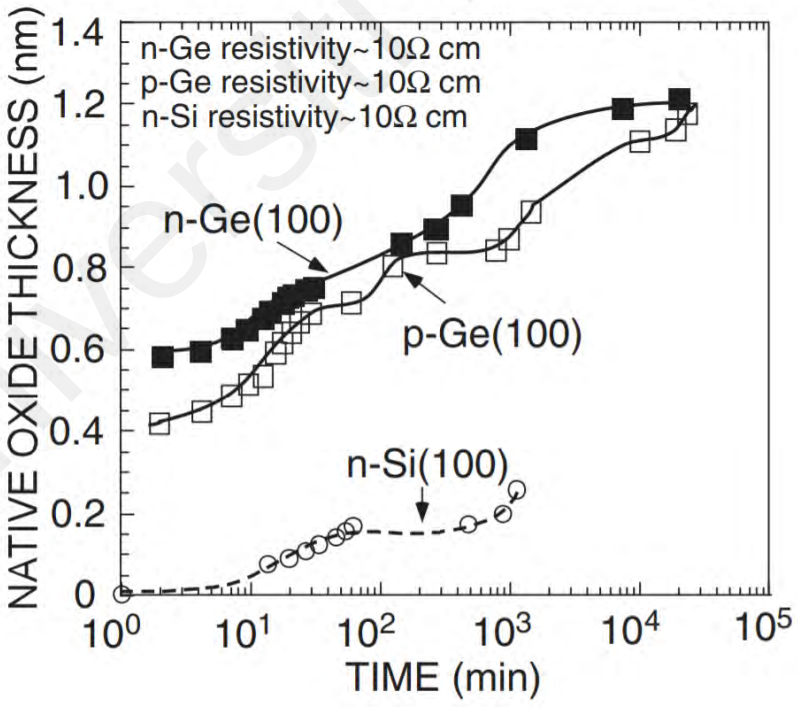

Figure 2.6: Comparison of native oxide Growth rate for Si and Ge substrate (Sahari et al., 2013).

2.6.2 Thermal Issues of GeO_2/Ge Stack

Since the native GeO_2 growth increases rapidly during air exposure and so elevation of temperature is an effective method for hindering the growth of native GeO_2 prior to the deposition of dielectric film into Ge substrate. However, it has been pointed that the desorption of GeO_2 occurs at GeO_2/Ge while such desorption was not found in GeO_2/Si interface (Kita et al., 2008). It is believed that the origin of GeO_2 degradation is caused by the interfacial redox reaction between GeO_2 and Ge which initiates volatile GeO desorption according to Eq. 2.5 (Prabhakaran et al., 2000).

$$GeO_2 + Ge \rightarrow 2GeO(s) \text{ or } 2GeO\ (g) \text{ at } 400\ ^\circ C \qquad \text{(Equation 2.5)}$$

S. K. Wang et al., (2010) have demonstrated that oxygen vacancies that are being generated from Eq. 2.5 diffuses through the GeO_2 network leading to GeO (g) desorption as shown in Fig. 2.7. It is also pointed that exchange of in-diffusing O with GeO_2/Ge interface also reinforces the oxygen vacancy production during thermal oxidation (S. K. Wang et al., 2010). It has been reported that the diffusivity of oxygen is much higher than Ge as a result the prominent transportation of oxygen through the native GeO_2 occurs at low temperature in contrast to SiO_2/Si stack processing temperature (500 – 600) °C. In fact, the transportation of oxygen into GeO_2/Ge interface has been observed below 500 °C temperature which was mediated by generation of mobile oxygen vacancies (Da Silva, Rolim, Soares, Baumvol, & Krug, 2012; X. Wang, Nishimura, Yajima, & Toriumi, 2017). Moreover, the diffusion mechanism of oxygen into GeO_2/Ge structure and production of oxygen vacancies from GeO_2 network also influences the thermal processing of metal/dielectric oxide/semiconductor substrate stack structure. This has been evidenced from comparison of thermally annealed Pt/HfO_2 gate stack based on both Si and Ge substrate at O_2 ambient. It was found that Ge substrate introduces higher quantity of O diffusion

into the dielectric/substrate interface at processing temperature (450 – 500) °C in compared to Si substrate due to defective character of native GeO_2 than SiO_2 (Rolim, Gobbi, Soares, & Radtke, 2015). This stimulates higher oxidation of the Ge substrate which creates major challenges in terms of thermodynamic stability, scalability and gate capacitance of dielectric oxide since oxygen diffusion promotes higher growth rate of interfacial GeO_2 interface (Etcheverry, Boudinov, & Soares, 2019). Beside GeO desorption, water solubility of GeO_2 is another major concern in the way to integration Ge based MOS devices (Kamata, 2008; Watanabe et al., 2012).

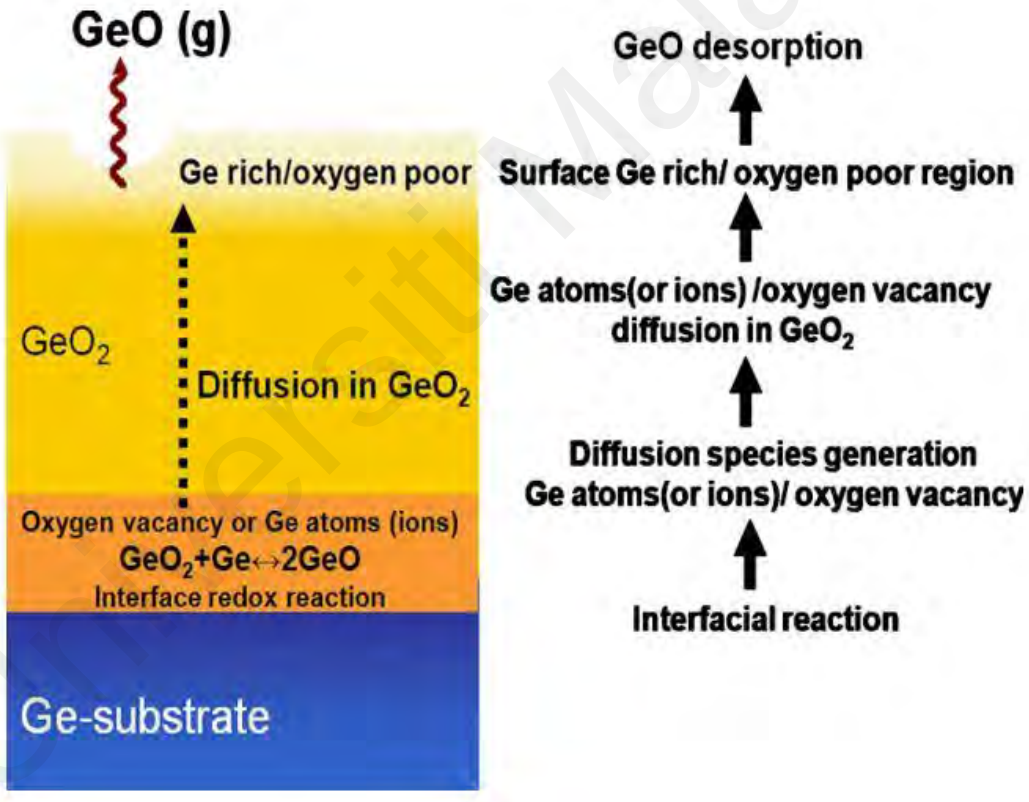

Figure 2.7: Schematic of GeO desorption mechanism from GeO_2/Ge interface (S. K. Wang et al., 2010).

2.6.3 Electrical Characteristics of GeO_2

Several reports evidenced that, desorption of large amount of GeO (g) ultimately deteriorates the electrical performance by generation additional fixed charges, inevitable hysteresis effect, large flatband voltage shift and large interface trap density (Bellenger et al., 2008; Jung et al., 2012). The investigation of Kita et al., (2008) recorded a superior *C-V* feature for GeO_2 when deposited on Si while a huge hysteresis observed for GeO_2/Ge as shown in Fig. 2.8. This suggests that the instability of GeO_2 is not an intrinsic property rather incorporation of Ge into GeO_2 network during thermal processing is responsible for the instability of GeO_2/Ge stack (Kita et al., 2008). In case of GeO_2/Ge stack, the interface trap density, D_{it} was found to be scattered in range of 10^{11} – 10^{12} $eV^{-1}cm^{-2}$ which is significantly higher with respect to SiO_2/Si interface $D_{it} \sim 10^{10}$ $eV^{-1}cm^{-2}$ (Hosoi et al., 2009). Matsubara et al., (2008) reported that GeO_2/Ge formed by standard dry oxidation at 500 – 600 $^{\circ}C$ in O_2 ambient can achieve $D_{it} \sim 10^{11}$ $eV^{-1}cm^{-2}$ although the hysteresis was around >100 mv and physical oxide thickness 30.9 – 30.7 nm (Matsubara, Sasada, Takenaka, & Takagi, 2008). The dielectric constant k of GeO_2/Ge has been estimated around 5.5 – 5.9 which is another prominent obstacle for scaling that increases the equivalent oxide thickness (*EOT*). Furthermore, the conduction band offset of GeO_2/Ge has been reported less than $<$ 1eV as shown in Fig. 2.9 which increases the leakage current density (Chroneos et al., 2012; Dimoulas et al., 2007; L. Lin, Xiong, & Robertson, 2010; Matsubara et al., 2008).To mitigate these issues several high-*k* materials with different deposition techniques have been coupled as gate dielectric for Ge-based MOS application (Goley & Hudait, 2014; Kamata, 2008).

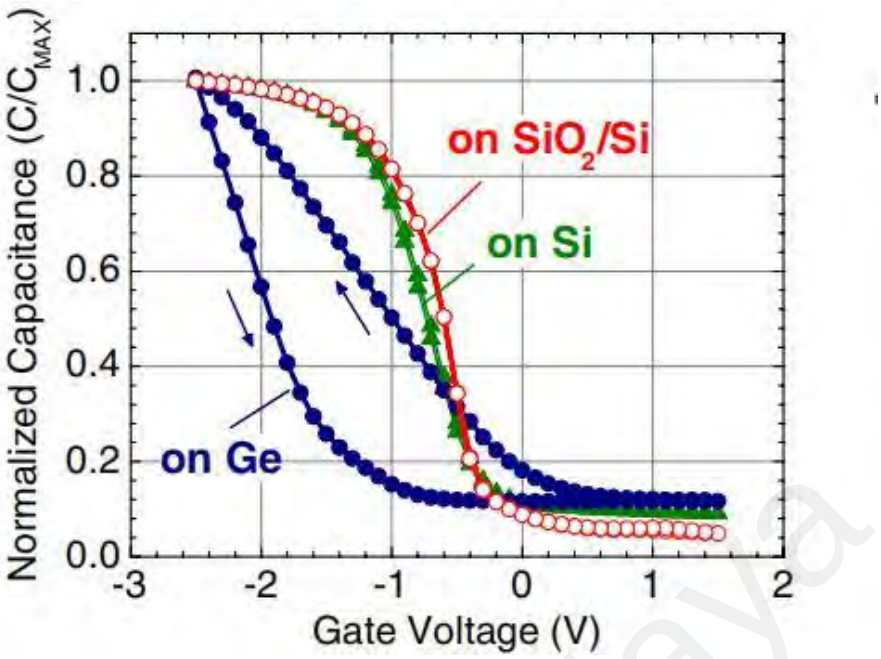

Figure 2.8: Bidirectional *C–V* curve at (1 MHz) of sputtered GeO_2 on Ge, Si, and thermally oxidized Si substrates followed by post deposition annealing 400 °C (Kita et al., 2008).

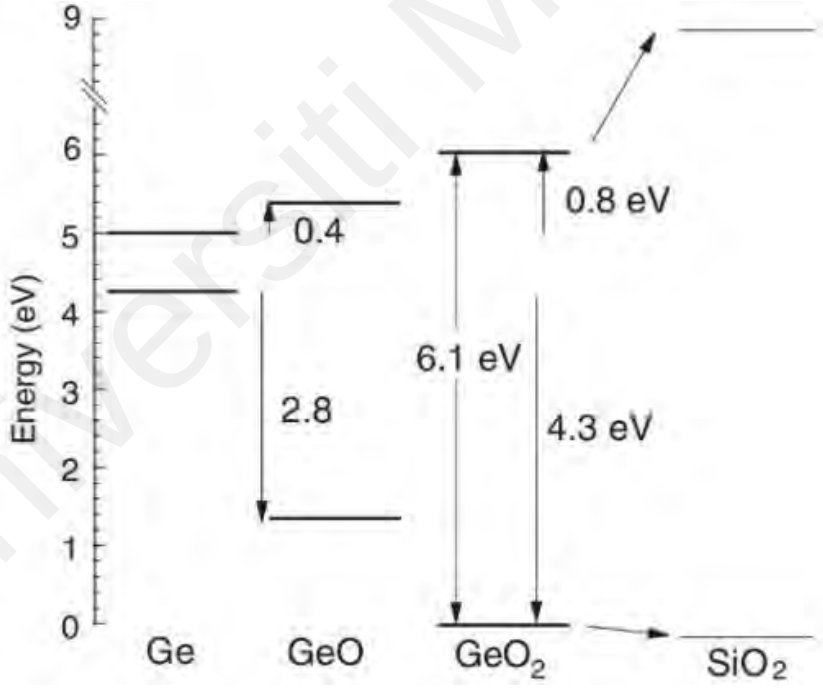

Figure 2.9: Band alignment schematic of GeO_2/Ge interface and comparison with the band offset of SiO_2/Si interface. (L. Lin et al., 2010).

2.7 Common High-*k* Oxides on Ge

Since, native GeO_2 of Ge is thermally unstable, integration of high-*k* material into Ge has created the exciting prospect of using Ge as substrate material for MOS gate stack. Various transitional metal oxides which include HfO_2 (Arora et al., 2009; Chandra, Jeong, Park, Yoon, & Choi, 2011; Jung et al., 2012; Kita, Kyuno, & Toriumi, 2004; Misra, Garg, Srinivasan, Rahim, & Chowdhury, 2006; Oh et al., 2015; Venkata Rao et al., 2018), ZrO_2 (C. O. Chui, Ramanathan, Triplett, McIntyre, & Saraswat, 2002; Kamata, Kamimuta, Ino, & Nishiyama, 2005; H. Kim, Chui, Saraswat, & McIntyre, 2003; Lei et al., 2017, 2018; Wong, Lei, & Abidin, 2021) and Al_2O_3 (Bom et al., 2012; Botzakaki et al., 2018; Ke, Takenaka, & Takagi, 2018; Xiang et al., 2020; X. Yang et al., 2014; Yoshida et al., 2014; R. Zhang, Iwasaki, Taoka, Takenaka, & Takagi, 2011) has been intensively studied for integration of high-*k*/Ge gate stack. These materials were widely investigated because of their relatively high band offsets and large dielectric constant as shown earlier in Fig. 2.5. Although HfO_2 has shown compatibility with Si substrate, but this material introduces large leakage current $J_g \sim 10^{-3}$ A cm^{-2} when it is directly deposited on Ge (Kamata et al., 2005). An improved electrical property for HfO_2/Ge gate stack comprising $J_g \sim 10^{-9}$ A cm^{-2} at $V_g = 1$ V and $t_{ox} \sim 6.4$ nm stack has been achieved by inserting an additional interfacial layer of Ge_3N_4 at annealing temperature of 400 °C in O_2 and forming gas ambient (Venkata Rao et al., 2018). Nevertheless, this investigation is still limited to poor *C-V* characteristics, scaling issues and D_{it} has not been studied. Meanwhile, ZrO_2/Ge gate stack without an interfacial layer free interface inducing $J_g \sim 10^{-7}$ A cm^{-2} at enhanced breakdown field E_{BD} of 16.6 MV cm^{-1} stack has been reported using thermally oxidation (500 °C in O_2 ambient) (Lei et al., 2017). Although ZrO_2 could be formed without an interfacial layer but is limited to large hysteresis > 200 mv and large interface charge traps of D_{it} of 7×10^{12} cm^{-2} (H. Kim et al., 2003). In regard to MOS fabrication process a thermal budget of 400 °C for 30 min has been acknowledged which

requires the gate dielectric layer should not recrystallize at this temperature rather be amorphous in order to maintain the high-*k* requirements (C. Chui, Kim, & Chi, 2002). One of the major concerns for HfO_2/Ge and ZrO_2 /Ge gate stack is that Ge could diffuse toward HfO_2 and ZrO_2 dielectric layer even at low temperature less than 300 °C. Consequently, interdiffusion of Ge instigates electrically active state within the interstitial or substitutional sites of these oxides' leading to higher interface trap density (Caymax et al., 2008; Zhu, Tamagawa, M., Furukawa, & Ma, 2002).The recrystallization of HfO_2 occurs at 400 °C which is also a critical issue that effects the thermodynamic stability of HfO_2/Ge stack. Considering Al_2O_3 based Ge MOS device X. Yang et al., (2014) developed Al_2O_3/GeO_x/Ge gate stack showing superior electrical properties with a low $D_{it} \sim 1.9 \times 10^{11}$ eV^{-1} cm^{-2}, $J_g \sim 10^{-7}$ A cm^{-2} at $V_g = 1$ eV and small hysteresis, better *C-V* characteristic but with an expense of *EOT*~ 2.7 nm. However, TiO_2/Al_2O_3 /Ge gate stack could provide promising *EOT* as low as 0.6 nm but exhibits poor $J_g \sim 10^{-2}$ A cm^{-2} at $V_g =$ -1 eV which has been reasoned due to near zero CBO of TiO_2 on Ge (L. Zhang, Gunji, Thombare, & McIntyre, 2013). Another promising development of Al_2O_3/GeO_x/Ge was made by using plasma post oxidation demonstrating *EOT* ~ 1 nm and $D_{it} \sim 1 \times 10^{11}$ eV^{-1} cm^{-2}. It was pointed that controlling GeO_x thickness is the critical issue for reduction of interfacial layer (IL) which results sharp increase of D_{it} while the J_g also becomes very high exceeding 1 A cm^{-2} (R. Zhang, Iwasaki, Taoka, Takenaka, & Takagi, 2012). Since direct deposition of transitional metal oxides could not comply with all the requirements needed for high-*k* based gate stack it has turned interest in employing rare earth oxides (REOs). In addition, the *EOT* expenses including an IL layer has also triggered the motivation towards REOs.

2.8 Rare earth oxide as Alternative High-*k*

Recently, lanthanide based rare earth oxides have gained widespread interest for its superior features which includes high dielectric constant, large band gap and conduction band offset, high chemical, and thermal stability (Chin et al., 2010; Goh et al., 2017a; Leskela et al., 2006; Shuan Li, Wang, Lin, Wang, & Li, 2022). Fig. 2.10 displays partly section of the periodic table for rare-earth (lanthanide) elements. Among the 15 materials of lanthanides, Pm has been eliminated, since it is considered as unstable radioactive material (Iwai et al., 2002). The lanthanide REOs can appear at different oxidation states including (+2, +3, and +4) states which differentiates the oxygen composition of lanthanide oxides LnO_x. Thus, various stoichiometries of lanthanide oxides could be in form of Ln_2O_3, LnO_2 and LnO depending on the oxidation state. Among the lanthanide oxides, the stoichiometry of Ln_2O_3 has been focused for utilization into high-*k* MOS application. Since, the stoichiometry of LnO_2 is steady at +3 oxidation state while stoichiometry of LnO lacks insulating properties (Chin & Cheong, 2011; Osten et al., 2008; Scarel, Svane, & Fanciulli, 2006). Therefore, lanthanide based rare earth oxides of Ln_2O_3 have gained widespread interest for its superior features.

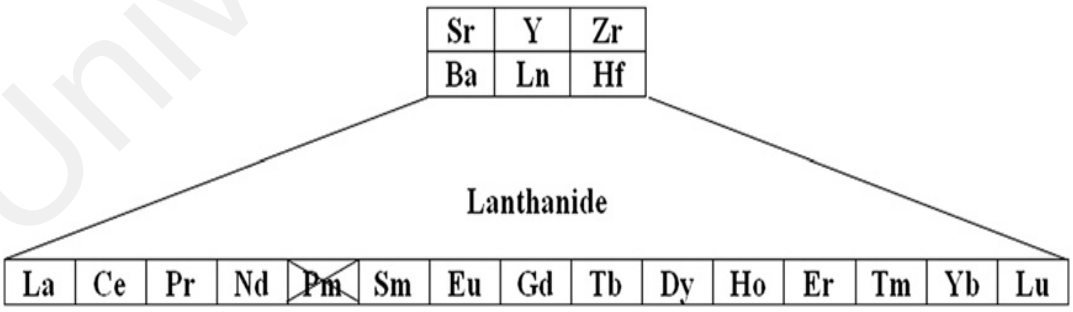

Figure 2.10: Candidates for metal oxide high-*k* gate insulator (Iwai et al., 2002).

As mentioned in earlier section the potential range of dielectric constant, k should be between $10 - 30$ (Chin & Cheong, 2011; Houssa et al., 2006). REOs are well known for owing high dielectric constant, k values ranging between $7 - 30$ as shown in Fig. 2.11 The high dielectric constant values of REOs should grant them to lower the *EOT* which is desirable for fulfilling the downscaling trend (Gillen & Robertson, 2013; Goh et al., 2017a). The dielectric constant values of REOs are associated with the crystalline composition of oxide components. Those REOs which own higher dielectric constant, k values are recommended to form stable hexagonal configurations which are known as light REOs consisting of La_2O_3 – Pr_2O_3. Meanwhile, the comparatively lower k value REOs are suggested to form stable cubic and monoclinic configurations for (Sm_2O_3 – Lu_2O_3) (Adachi & Imanaka, 1998; Iwai et al., 2002). Although, very limited evidence is found to verify this phenomenon. On the other hand, the oxide deposition technique, its formation defect and thickness are likely to be more influential on varying the dielectric constant values (Scarel et al., 2006). For instance, $k \sim 30$ was approximated for Pr_2O_3/Si interface which was deposited employing MBE method. On the contrary, $k \sim 15$ was approximated for the same oxide when it was deposited using Atomic layer deposition (ALD) with a film thickness ranging between 80 nm to 100 nm (Fissel, Osten, & Bugiel, 2003; Kukli et al., 2004).

In order to replace SiO_2 it is essential that, the REOs should owe a high energy bandgap, E_g above 5 eV which could act as potential barrier for electron tunneling to maintain better insulation (He, Liu, et al., 2014; Houssa et al., 2006). Fig. 2.12 shows the bandgap of REOs which indicates that among the REOs the dielectric oxide of La_2O_3 , Sm_2O_3, Gd_2O_3, Ho_2O_3, Er_2O_3, Tm_2O_3, and Lu_2O_3 could be serve as replacement of SiO_2 due to their high bandgap > 5eV (Goh et al., 2017a; Ohmi et al., 2001). Therefore, these REOs has been the primary consideration from lanthanide list while some of them are being widely investigated in the last few years for integration of Ge based MOS devices.

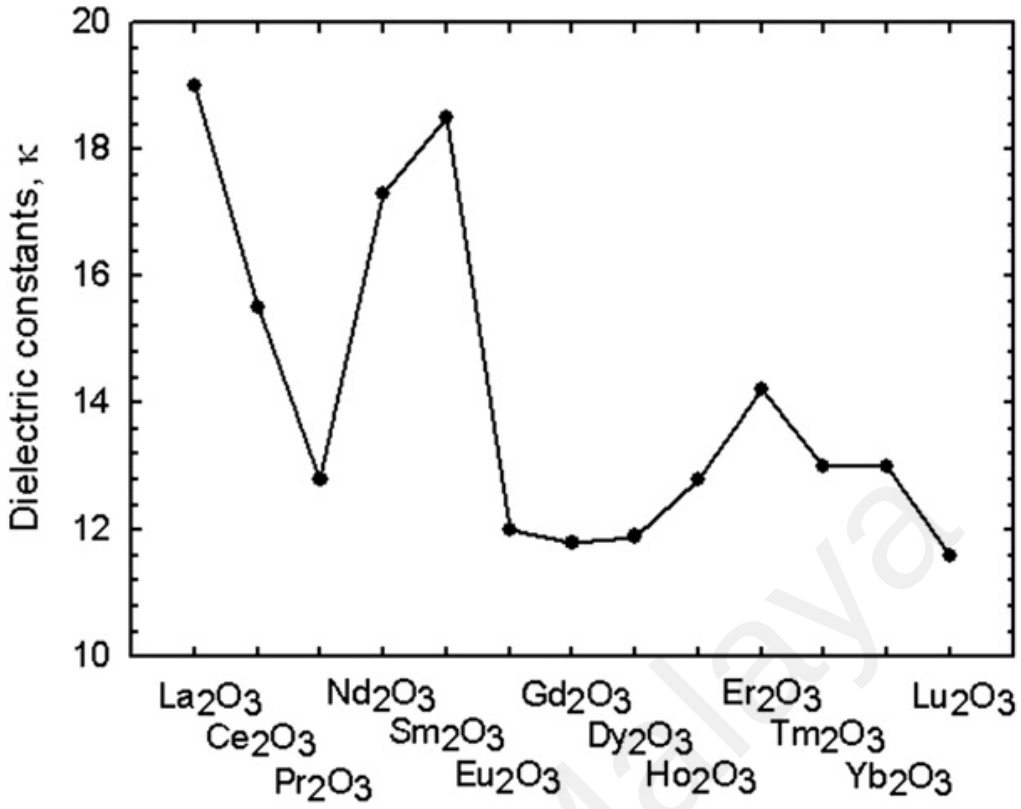

Figure 2.11: Dielectric constants of rare-earth oxides (Chin & Cheong, 2011).

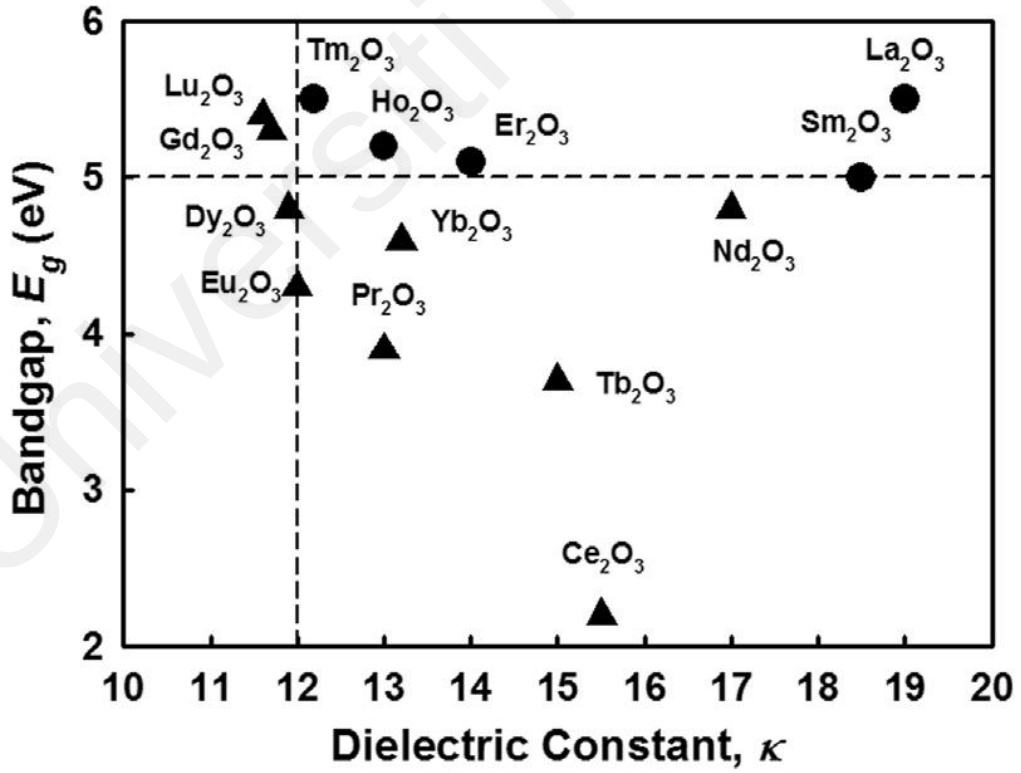

Figure 2.12: Band gaps of rare-earth oxide (Goh et al., 2017a).

For consideration of high-*k* dielectric in replacement of SiO_2 another important criterion is that the band offset should be above 1 eV. In the work of Robertson, (2002) it has been suggested that, the stochiometric ratio between metal and oxygen could effectively influence the value of band offset. The greater ratio value between metal: oxygen should impose higher value of band offset. According to this investigation the CBO of HfO_2 was around 1.5 eV while La_2O_3 exhibited a CBO of 2.3 eV with respect Si interface. This has been reasoned that La_2O_3 considers larger stoichiometric ratio of metal and oxygen and so, a larger CBO was obtained in counter to HfO_2 (Robertson, 2002). This outcome also put up REOs to be a superior alternative. The comparison of CBO of several REOs as function of dielectric has been portrayed in Fig. 2.13. It is found that all the estimated CBO of REOs is above 1 eV which makes them potential candidate to be investigated for high-*k* dielectrics.

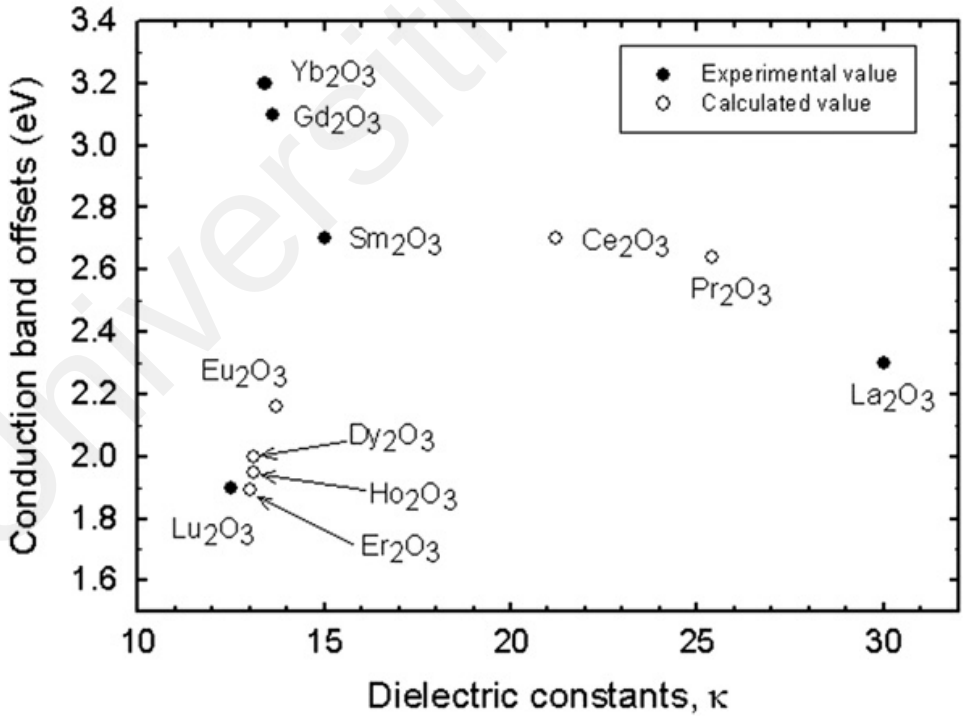

Figure 2.13: Conduction band offsets (CBO) of various REOs on Si as a function dielectric constant (Chin & Cheong, 2011).

The hygroscopic nature of rare earth material is one of the major difficulties during deposition of REOs. Due to moisture absorption the hydride $Ln_2O_3–H_2O$ is formed in REOs which ultimately initiate the growth of hydroxide [$Ln(OH)_3$]. The formation of such hydroxide would eventually enhance the thickness of deposited dielectric REOs film and as well as drops the *k* value of the film (Engstrom et al., 2007). The reaction rate of forming hydroxide (OH^-) in REOs due to moisture absorption increases when the ionic radius of the rare earth component is decreases (S. Jeon & Hwang, 2003). In addition, the moisture reactivity of REOs is also influenced by the positive ion electronegativity and lattice energy of REOs. The positive ion of REOs having lower electronegativity is found be highly reactive with negative ion of (OH^-) while increasing the moisture reactivity. Moreover, with the increment of lattice energy of REOs decreases reactivity to water which declines the hygroscopic behaviour of REOs (Chin & Cheong, 2011; Goh et al., 2017a; Iwai et al., 2002). Fig. 2.14 shows the electronegativity and lattice energy values of various REOs. According to Fig. 2.14, the Lu_2O_3 is the least hygroscopic REOs as this oxide possess highest electronegativity and lattice energy while La_2O_3 is the most hygroscopic REOs for having lowest electronegativity and lattice energy. In order to mitigate the moisture absorption difficulties in REOs a typical gate electrode of Al can be deposited on the top of the dielectric REOs. It has been suggested that deposition of a gate electrode could decrease the moisture reactivity which effectively reduce the formation of (OH^-) in REOs and so the resulting in lowering of *EOT* (Iwai et al., 2002). Furthermore, the hygroscopic behaviour of REOs also effects adversely on surface roughness of the dielectric interface which eventually increases the extent of leakage current density. Fig. 2.15 displays the variation of leakage current density due to surface roughening which was caused after the moisture absorption of REOs (Kakushima et al., 2006; J. Song et al., 2009). Therefore, rare earth element imposing smaller ionic radius and less hygroscopic nature are preferably considered for integration into future High-*k* based MOS devices.

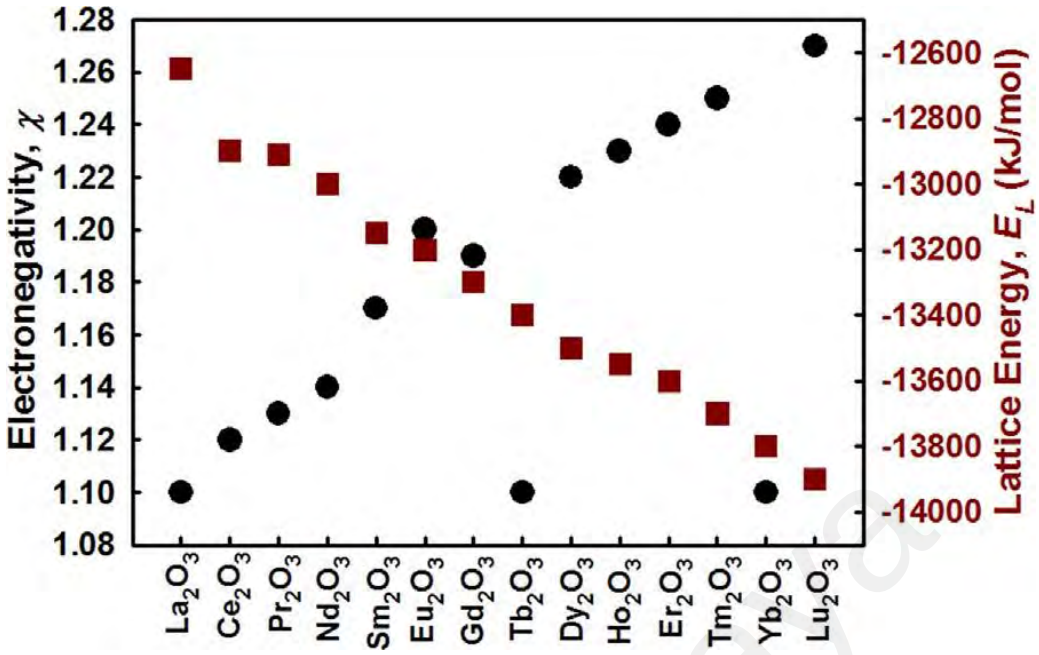

Figure 2.14: The electronegativity and lattice energy of lanthanide REOs (Goh et al., 2017a).

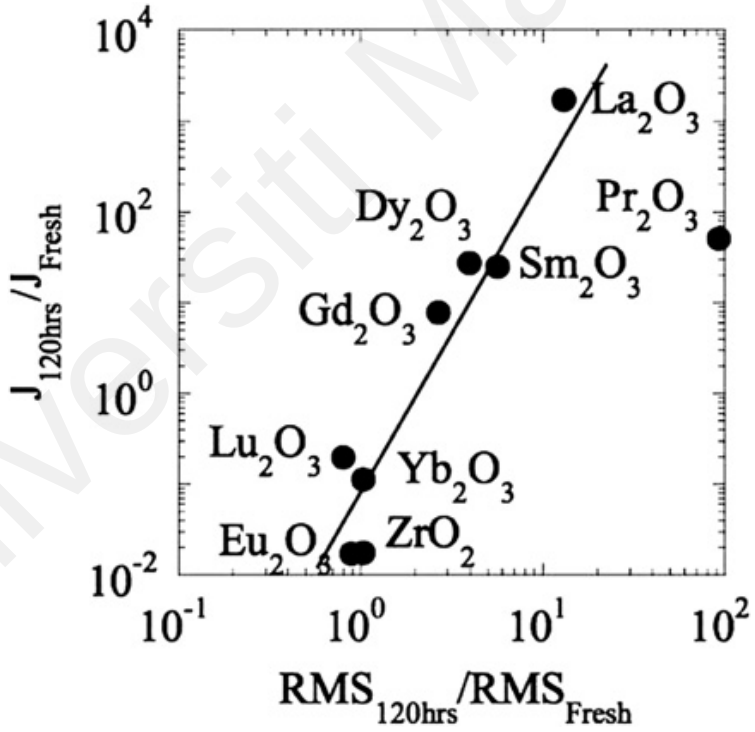

Figure 2.15: Effect of surface roughness of rare-earth oxides on leakage current (Kakushima et al., 2006).

2.9 Common Deposition Methods of REOs

Several deposition methods have been investigated for the development of REOs as high-*k* dielectric. The deposition method of REOs can be segmented into two major categories which includes chemical vapor deposition (CVD) and physical vapor deposition (PVD). The CVD has been classified into two major techniques which includes mainly atomic layer deposition (ALD) and metal organic chemical vapor deposition (MOCVD). Meanwhile, the PVD includes several deposition techniques which includes magnetron sputtering, electron beam evaporation, thermal evaporation and pulsed laser deposition (Chin et al., 2010; Goh et al., 2017a; He, Liu, et al., 2014; Houssa et al., 2006; Wong & Cheong, 2010).

2.9.1 Chemical Vapor Deposition (CVD)

The deposition of thin film using ALD basically utilizes chemical gas phase of two or more precursors. These precursors are deposited into the substrate surface through saturation reaction deposition between precursors substrate material by utilizing alternative oxidation in a subsequent process causing different monolayers of the reactant precursors within the reaction chamber. Subsequently, deposition of dielectric oxide occurs by the regulation of surface controlled growth cycles. Primarily, an excessive amount of complementary gaseous precursors is exposed to the substrate surface which introduces complementary monolayer of reactant. A controlled temperature and gas flow is regulated in such way until the reactant precursors monolayer could chemically absorb the maximum substrate surface so that there is no further expansion of the complementary precursors until the anticipation of the second precursor. Before the exposure of second precursors the residual of complementary precursors gas is taken out by purging an inert gas into reaction chamber. In the last stage second precursor is purged into the chamber which

reacts with first reactant monolayer and chemically saturates the reactant to form the desired dielectric thin film. Subsequently, again the second precursor is brought out from the reaction chamber by purging an inert gas which completes the ALD process (Goh et al., 2017a; Jo, Ha, Park, Kang, & Kim, 2006; W. H. Kim, Maeng, Moon, Myoung, & Kim, 2010; Paivasaari et al., 2006). The ALD method is also defined in various names such atomic layer epitaxy (ALE) and atomic layer chemical vapor deposition (ALCVD) (Wong & Cheong, 2010). Regarding ALD process the precursor should be non-toxic and volatile, maintain high-level of purity, certainly not participate in reactions at gas phase and the oxide should be free of any etching and self-decomposition (Leskela & Ritala, 2003). Utilization of thermal and plasma enhanced ALD could produce much better quality of thin film with less impurities, good interface and electrical properties (Khosla, Schwarz, Funk, Guguieva, & Schulze, 2021; W. H. Kim et al., 2010; Zhao et al., 2018). The MOCVD deposition method is another technique under CVD for deposition of thin film on substrate. This process utilizes both fundamental principles of ALD and CVD. The primary distinction between ALD and MOCVD is that during MOCVD process metalorganic compounds with hydrate or alkyl group are used as precursor into the reactor chamber. In this method usage of liquid precursor is beneficial for avoiding unwanted particle formation where the molecules of decomposed liquid precursors are to be transferred into heated substrate by utilizing (H_2 or N_2) as gas carrier and afterwards surface reaction takes place to form thin films (Chin & Cheong, 2011; Houssa et al., 2006). Both the ALD and MOCVD are widely used since these methods are advantageous to for uniform thin film while enables to control the oxide film thickness accurately. These methods also hiders the growth of complex atomic configuration because the precursors could control self-constraining growth process. Furthermore, these methods also allow to grow higher-level film density covering a wide region of depositions with higher deposition

rates and control the film composition (Goh et al., 2017a; He et al., 2011; Jo et al., 2006; Mallem et al., 2019).

Nevertheless, these methods are subjected to some limitations which includes availability, stability, and volatility of molecular precursor, For the decomposition of metal organic precursor relatively higher temperature and a post deposition annealing are essential. Accordingly, the electrical characteristics are hampered due to the presence of large volume of detrimental carbon (Goh et al., 2017a; He, Liu, et al., 2014; Kosola, Päiväsaari, Putkonen, & Niinistö, 2005). Wong and Cheong, (2010) encapsulated three major concerns of ALD (1) it's complicated and challenging to transfer particles from source to the deposited film since the dimension of particles is very delicate (2) poor nucleation on hydrogen terminated silicon, and (3) residual defects at the film edge (Wong & Cheong, 2010). For instance, Nd_2O_3 dielectric film was left over with a substantial volume of residual carbon in its film region during ALD procedure (Kosola et al., 2005).

2.9.2 Physical Vapor Deposition (PVD)

The pulsed laser deposition is a PVD technique using laser ablation to deposit thin films on the substrate. In this method laser beam with high energy density irradiates target source which ablates away some particles of the material in vaporized form that ultimately transported towards the substrate surface. The radioactivity of repetitive laser pulse subsequently generates reoccurring vapor clouds which causes to form a new material on the substrate surface (Goh et al., 2017a; Wong & Cheong, 2010). However, the kinetic energy and specific ratio of the ablated vaporized particles depends on wavelength, intensity, and pulse width of the laser. During the PLD process formation of thin film includes three phases which are (i) interaction of laser radiation through the target

source (ii) dynamic aspects of excision materials (iii) sublimation of extracted source material into substrate and formation of the desired thin film (Chin & Cheong, 2011). PLD is a simple technique to form thin oxide film which could serve variety of film compositions and structures. However, PLD deposited REOs tends to increase surface roughness and crystallization occurs with increment of substrate temperature (Balakrishnan et al., 2013; Constantinescu, Ion, Galca, & Dinescu, 2012). Electron beam evaporation is one more common deposition techniques that has been widely utilized to grow thin solid film on substrate surface. In this method an electron beam is employed as an energy source at high-level vacuum ambient which heats up the target material for producing vaporized form of the target material and then condensed on the surface of substrate to grow thin solid film (Chin & Cheong, 2011; C. Yang, Fan, Qiu, Xi, & Fu, 2009). It has been reported that this method could form smooth thin oxide films which reveals promising electrical properties. Electron beam evaporation can produce ultrathin and smooth films with excellent electrical properties (Sen et al., 2007). This method also allows to form compact and densified oxides with low stress (Goh et al., 2017a; C. Yang et al., 2009). Nevertheless, this method is not compatible for conventional manufacturing procedure.

Sputtering is the simplest and frequently used procedure of depositing thin film under PVD. This is a deposition procedure where the solid source materials known as target source discharge plasma particles towards the solid substrate material positioned inside a vacuum chamber. At the beginning of this process the target source is applied to a negative bias which discharge plasma particles. Accordingly, positively charge gas ion is being produced across the plasma domain. Consequently, the negatively biased target material source attracts the positive gas ions incredibly at high velocity from the plasma domain. Therefore, ejection of target material source occurs due to an exchange of momentum amongst the target source particles caused by the surface bombardment through energetic particles. (Chin & Cheong, 2011; Goh et al., 2017a; Wong & Cheong, 2010).

The magnetron sputtering basically involves radio frequency (RF) sputtering and direct current (DC) sputtering. The type to be used depends on the electrical conductivity of target material. The target source material with low electrical conductivity utilizes RF sputtering while the high electrical conductivity target source material employs DC sputtering (Goh et al., 2017a; Robertson, 2004). RF magnetron sputtering is a widely used straightforward method for high-*k* deposition which is broadly available to deliver high growth rate during deposition, deposit smooth surface good quality adhesion among the oxide film and substrate material (Jagadeesh Chandra, Choi, Uthanna, & Mohan Rao, 2010; Kaya, Yilmaz, Karacali, Cetinkaya, & Aktag, 2015). Although deposition of thin film using the sputtering from target material (such as metal or metal oxide) is quite easier and straightforward than other methods, but the problem is oxygen and argon flow is used for the formation oxide in this method could possibly oxidize substrate material leading thicker interfacial layer of native oxides (Pampillon et al., 2011; Pan & Huang, 2010). Apart from that sputtering does not provide good quality of coverage on complex structure since this process only deposits line up of spots (Robertson, 2004). Several studies reported that using pure metal target source during RF sputtering at an argon ambient subsequently following thermal oxidation could be a superior choice for thin film formation into MOS gate stack (Lei et al., 2017; Wong & Cheong, 2012a; Wong et al., 2021). This is because combination of pure metal RF sputtering with subsequent thermal oxidation process could provide formation of stochiometric metal oxide while controlling unwanted interfacial layer.

2.10 Performance of Commonly Used REOs/Ge Stack

Rare earth oxides (REOs) have been found to be thermodynamically stable with Ge due to vigorous reaction between REOs with the Ge interface. The catalytic oxidation of Ge atom with REOs promotes the spontaneous growth of rare earth germanate (RE – O – Ge) leading to low interface trap densities, $D_{it} \sim 10^{11}$ eV^{-1} cm^{-2} (Mitrovic et al., 2014; Zhao et al., 2018). Moreover, rare earth oxides do not involve any pre-deposited interfacial layer between REOs and Ge since they form stable germanate layer during deposition or annealing process (Dimoulas et al., 2007; W. Liu et al., 2022). The most used high-*k* transition metal oxides, HfO_2, ZrO_2 and Al_2O_3 reveals drawbacks in electrical properties and thermodynamic stability of the gate oxide (Kamata et al., 2005; H. D. Kim & Roh, 2006; X. Yang et al., 2014). Hence, REOs have drawn major attention in the high-*k* dielectric researchers. Lu et al. (2014) has been demonstrated that REOs provide more attractive properties for M-GeO_2/Ge (i.e., M= Al, Sc, Y, La, and Hf) gate stack in terms of aggressive scaling, electrical properties, and thermodynamic stability. Fig. 2.16 shows that rare earth metal-based compound Y–GeO_2 reveals the lowest $D_{it} \sim 1 \times 10^{11}$ eV^{-1} cm^{-2} while Hf– GeO_2 yielded the highest, $D_{it} \sim 10^{12}$ eV^{-1} cm^{-2} (Lu et al., 2014). The interface trap density found for Y–GeO_2 is quite close according to the state of art GeO_2/Ge interface formulated by high pressure oxidation (C. H. Lee, Nishimura, Nagashio, Kita, & Toriumi, 2011). The most used rare earth oxides as high-*k* dielectric on Ge substrate are La_2O_3 (Dimoulas et al., 2010; Kanashima et al., 2015; Q. Liu, Fang, Liu, Tan, & Chen, 2014; Mavrou et al., 2007; J. Song et al., 2009; Zhao et al., 2018; Zhao, Liu, Wang, Wang, & Wang, 2019), Y_2O_3 (Bethge et al., 2014; D. G. Kim et al., 2021; Mitrovic et al., 2014; Nishimura et al., 2011; Seo et al., 2017; Zimmermann et al., 2016), CeO_2 (Brunco et al., 2007; Dimoulas et al., 2007), Gd_2O_3, (Evangelou et al., 2009), and Tm_2O_3 (Žurauskaitėa et al., 2018).

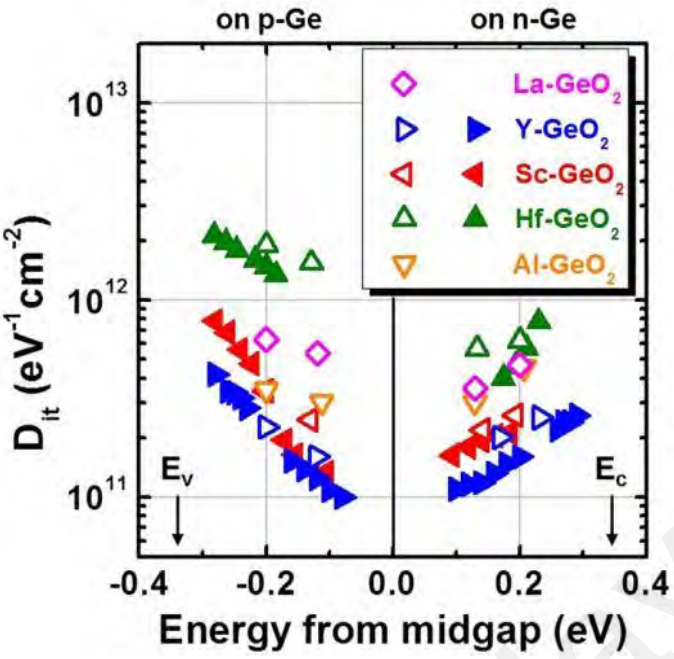

Figure 2.16: Comparison of interface trap densities among transitional metal and rare earth metal deposited on GeO_2/Ge interface. (Lu et al., 2014).

2.10.1 La_2O_3/Ge Gate Stack

In work of J. Song et al., (2007) La_2O_3/Ge gate stack developed by electron beam evaporation with post deposition annealing (PDA) in 5% (O_2+N_2) ambient at (500 – 400) ^oC. A gate leakage current density, $J_g \sim 10^{-4}$ A cm^{-2} by introducing an interfacial La−O−Ge. Although formation of additional GeO_x during the annealing process induces higher D_{it} in order of magnitude 10^{12} eV^{-1} cm^{-2} which impacted to higher hysteresis. In work of Mavrou, Galata, et al., (2008) a promising *C-V* characteristic with negligible hysteresis and reduced accumulation frequency dispersion with lower D_{it} in order of magnitude 10^{11} eV^{-1} cm^{-2} but with high $EOT \sim 5.7$ nm has been achieved while utilizing La_2O_3 deposited through MBD at temperature above 200 $^\circ C$ and subsequent PDA. However, it was found that deposition temperature below 200 $^\circ C$ degrades the electrical and interface properties. It is suggested that electrical properties can be improved using high deposition temperature or by annealing. The improvement of La_2O_3 based Ge stack has

been attributed due to four fold configuration of La within GeO_x which changes the surface chemistry through saturation of Ge dangling bonds by creation of interfacial $LaGeO_x$. However, formation of $LaGeO_x$ exhibited low- k values of 9, and high J_g of 10^{-1} A cm^{-2} at $V_g = +1$V which hinder the MOS scaling (Dimoulas et al., 2010; Mavrou, Galata, et al., 2008). The reduction of k value has also been predicted due to the hygroscopic nature of La_2O_3. In the same study using combination HfO_2 with 1 nm La_2O_3 improved gate leakage current density up to 10^{-8} A cm^{-2} and k value up to 17 but expenses high interface trap density. Combination of ZrO_2 and La_2O_3 through MBE provides higher k of around 40, leading to *EOT* as low as 1.2 nm but increases the interface trap density as well (Mavrou, Tsipas, et al., 2008). Q. Liu et al., (2014) deposited 10-nm La_2O_3/Ge by RF magnetron sputtering following rapid thermal annealing (RTA) in O_2 ambient at 200 °C. In this work the conduction band offset, $\Delta E_c \sim 1.75$ eV, valance band offset, $\Delta E_v \sim 2.76$ eV and energy band gap $E_g \sim 5.18$ eV was determined using krauts method and Xray photoelectron spectroscopy. An improved $\Delta E_c \sim 2$ eV and $E_g \sim 5.18$ eV has been determined for La_2O_3/Ge at a deposition temperature of 400 °C by MBE (Mitrovic et al., 2014). However, MBE is not a conventional thin deposition method for MOS fabrication.

2.10.2 Y_2O_3/Ge Gate Stack

Mitrovic et al., (2011) demonstrated that Y_2O_3 is more Ge friendly than La_2O_3 which exhibits a band gap of $E_g \sim 5.7$ eV and CBO, $\Delta E_c \sim 2.3$ eV with the Ge interface and reduced the leakage current below 10^{-6} A cm^{-2} using MBE deposition method at temperature 400 °C (Mitrovic et al., 2014). A high electron mobility, μ_e of 1480 cm^{2}V^{-1}s^{-1} and $D_{it} \sim 10^{11}$ eV^{-1} cm^{-2} has been attained recently by employing high pressure oxygen annealing (Nishimura et al., 2011) .

In work of Bethge et al., (2014), Y_2O_3/Ge gate stack was developed by employing ALD with PDA exhibiting D_{it} as low as 10^{10} eV^{-1} cm^{-2} with very low $J_g \sim 5.7 \times 10^{-4}$ A cm^{-2} at relatively higher thermal budget of 600 °C but with the price of higher capacitance equivalent thickness (CET) of 10 nm and hysteresis of 140 mv. The improvement in interface trap density and gate leakage current density for Y_2O_3/Ge has been attributed to penetration of Y atom into oxygen deficient GeO_2 causing reduction of GeO_x defects by the growth interfacial $YGeO_X$ (Bethge et al., 2014; Nishimura et al., 2011). Meanwhile, $YGeO_x$/Ge/Si stacked has shown improved performance at high temperature of 750 °C through thermal oxidation which induced small hysteresis < 50 mv but with relatively low-*k* of 10.8 that impeded the scaling of the device (Seo et al., 2017). Typically, the dielectric constant, k of Y_2O_3/Ge has been reported ranging between $11-18$ (Mitrovic et al., 2014; Nishimura et al., 2011).

2.10.3 CeO_2/Ge Gate Stack

Dimoulas et al., (2007) demonstrated CeO_2 gate stack by Molecular Beam Deposition (MBD) which revealed moderate-surface passivation with the reaction of Ge substrate inducing relatively higher $D_{it} \sim 10^{11} - 10^{12}$ eV^{-1} cm^{-2}. However, this CeO_2/Ge gate stack showed small but visibly noticeable frequency dispersion and hysteresis in the *C-V* curve and revealed high leakage current density (> 0.1 A cm^{-2} at $V_g = +1V$). The high leakage current density could be reduced to $J_g \sim 10^{-7}$ order magnitude along with higher dielectric constant $k \sim 20.5$ when rare earth metal Ce was doped with HfO_2 using optimum mixing condition of Ce: HfO_2 = 1:4 for $CeHfO_2$/Ge gate stack developed by ALD with subsequent PDA process. However, the defect density and hysteresis were quite high where $D_{it} \sim 10^{13}$ eV^{-1} cm^{-2} which requires a controllable doping ratio (Maeng et al., 2014).

2.11 Sm_2O_3 and Ho_2O_3 as Alternative Dielectric

Although high-*k* materials of (TMOs and REOs) emerged to be potential contender for upcoming MOS technology but each of TMOs and REOs are still subjected to their own deficiencies in terms of gate leakage, interface trap densities, dielectric constant, *EOT* and thermodynamic stability (Goley & Hudait, 2014; Kamata, 2008; Mavrou, Galata, et al., 2008; Oh et al., 2015; Venkata Rao et al., 2018). Additionally, hygroscopic nature of REOs is an additional limiting factor on the way of MOS scaling which lowers dielectric constant and enhances equivalent oxide thickness (Chin et al., 2010; Goh et al., 2017a). Accordingly, it is imperative to seek for an appropriate high-*k* gate oxide material for Ge based gate stack which can compete the superior properties of conventional SiO_2/Si. Amongst the REOs Sm_2O_3 can be a prospective contender for MOS application, since this high-*k* material possesses larger $k \sim 7 – 15$, higher energy bandgap $E_g \sim 4.33$ eV, CBO ~ 2.7 eV with an electrical breakdown field $E_{Bd} \sim 5 – 7$ MV cm^{-1}, low frequency dispersion, low leakage current, with high gate capacitance with Si substrate (Chen et al., 2013; Chin & Cheong, 2011; Dakhel, 2004; Goh et al., 2016a, 2017a). In addition, Sm_2O_3 possess the second highest position of k value below La_2O_3 and less hygroscopic nature due to high electronegativity and large lattice energy in counter to other lanthanide oxide REOs as shown in earlier Fig. 2.14. So far, numerous studies were conducted on Sm_2O_3/Si using several deposition methods of CVD and PVD which revealed encouraging electrical and thermodynamic features (Chin & Cheong, 2011; Chin et al., 2010; Constantinescu et al., 2012; Goh et al., 2017a; Kaya et al., 2015; Paivasaari, Putkonen, & Niinisto, 2005; Pan, Huang, You, & Yeh, 2008). Table 2.3 demonstrates the dielectric constant and leakage current density for Sm_2O_3/Si gate stack different deposition methods (S. Jeon et al., 2001; Paivasaari et al., 2005; Pan & Huang, 2010; D. Yang, Xue, & Devine, 2003).

In works of Paivasaari et al., (2005) 50-nm Sm_2O_3 has been deposited on p-type Si using ALD that revealed low leakage current density, $J_g \sim 1.1 \times 10^{-8}$ A cm^{-2} at electrical breakdown field $E_{Bd} \sim 0.32$ MV cm^{-1} and $k \sim 10$. The improvement of leakage current density has been attributed to the smooth surface and to the growth of polycrystalline cubic phase of Sm_2O_3. The surface roughness was measured to be around root mean square, RMS ~ 1.2 nm. A smooth and amorphous surface of Sm_2O_3 was also developed using both PLD and RF sputtering at room temperature where a low surface roughness around RMS ~ 0.31 nm for sputtering was recorded (Constantinescu et al., 2012; Pan et al., 2008). However, an improved k value can be achieved from PLD , and electron beam evaporation as shown in Table 2.3 (S. Jeon et al., 2001; D. Yang et al., 2003).

Several researchers have deposited Sm_2O_3 thin film using RF magnetron from Sm_2O_3, or pure metal target source followed by thermal oxidation or post deposition annealing (PDA) to improve the physical and electrical properties Sm_2O_3/Si gate stack (Chen et al., 2013; Chin & Cheong, 2011; Goh et al., 2016a, 2016b; Goh, Haseeb, & Wong, 2017b; Kaya et al., 2015; Pan & Huang, 2010; Pan et al., 2008). In works of (Pan et al., (2008) Sm_2O_3/p-type Si gate stack combination of RF magnetron and RTA in O_2 ambient at 700 °C induced a low *EOT* ~ 2.75 nm and $k \sim 9.93$ at low J_g of 1.1×10^{-8} A cm^{-2} at $V_g = -1$V, and average interface trap density $D_{it} \sim 1.68 \times 10^{11}$ eV^{-1} cm^{-2} at mid-gap. A well-shaped *C-V* curve with high capacitance and low hysteresis was also achieved. The improvement has been attributed to the formation of uniform cubic polycrystalline Sm_2O_3which obstructed the inter diffusion of oxygen that eventually reduced the growth of interfacial SiO_2 and Sm-silicate interface. In further work, Pan & Huang, (2010) developed Sm_2O_3/Si film using reactive sputtering of pure Sm in different Ar/O mixture following with subsequent PDA at various temperatures in O_2 ambient. The sample developed using O/Ar ratio 15/10 at 700 °C improved the dielectric constant up to k

$\sim$ 14.3 with $J_g \sim 10^{-8}$ A cm^{-2} at V_g = -1V. It was found that formation of more uniform structure of Sm_2O_3 and improved recrystallization at this deposition condition enables to increase dielectric constant and reduced trapped charges within the dielectric surface. Goh et al., (2017a) summarized the electrical features of the leakage current density with respect to electrical breakdown field (*J-E*) for Sm_2O_3/Si films for several film deposition techniques as shown Fig. 2.17 (Goh et al., 2017a). According to Fig. 2.17, Sm_2O_3/Si developed using RF magnetron sputtering shows superior leakage current and higher electrical breakdown field.

However, investigation relating Sm_2O_3 /Ge stack for MOS application is very limited and scarce in counter to Sm_2O_3 /Si gate stack. In work of C. C. Lin et al., (2014), Sm_2O_3/Ge stack has been investigated by combining e-beam evaporation with subsequent furnace annealing process in O_2 ambient at 400 $^{\circ}$C, which corresponded promising outcome of high dielectric constant k $\sim$17.1 inducing very low *EOT* $\sim$ 0.68 nm and low interface trap density of $D_{it} \sim 5.10 \times 10^{11}$ eV^{-1} cm^{-2}. The reduction of interface traps has been attributed to the four fold configuration of Sm atoms which saturates the vacant locations of Ge dangling bonds inside the GeO_2 network by composing Sm−O−Ge interfacial layer. Although, the report outlined some potential findings, but this gate stack suffers from high gate leakage current, and several other aspects of Sm_2O_3/Ge interface are still unexplored which requires further investigation. Therefore, Sm_2O_3 on Ge substrate has been selected for this investigation for the realization of high-*k*/Ge MOS capacitor.

Table 2.3: Leakage current density and dielectric constant of Sm_2O_3/Si gate stack for different deposition techniques (S. Jeon et al., 2001; Paivasaari et al., 2005; D. Yang et al., 2003).

Deposition process	Thickness (nm)	Leakage current Density A/cm^2	Dielectric Constant *k*
ALD	50	1.11×10^{-8}	10
Electron Beam Evaporation	25	9.5×10^{-5}	11.4
PLD	111	1.63×10^{-6}	12.8
RF Magnetron Sputtering	7−8	10^{-7}	14.3

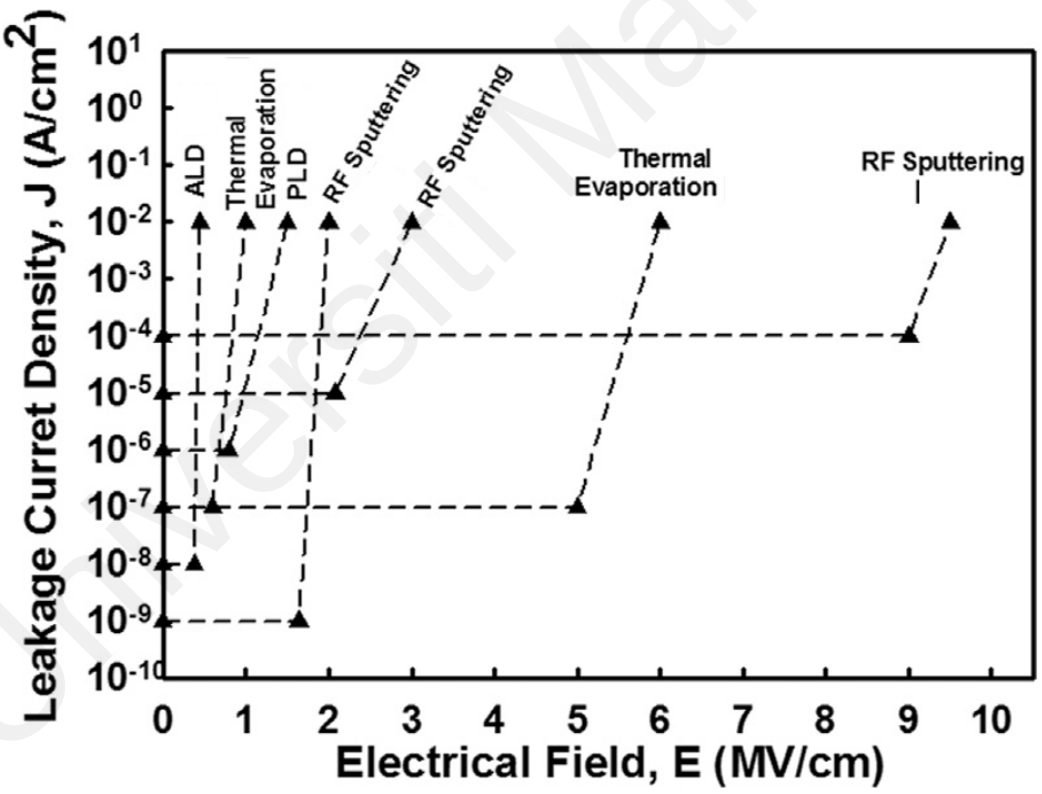

Figure 2.17: Review of leakage current density against electrical breakdown voltage for Sm_2O_3/Si gate stack for different deposition techniques (Goh et al., 2017a).

Among the REOs, Ho_2O_3 could be another prospective contender for realization of High-*k*/Ge because it befalls on the selection criterion of high-*k* dielectric. Ho_2O_3 owns a dielectric constant value k ~13.1, large enough bandgap energy, E_g ~ (5.3 eV) and high enough conduction band offset (CBO) of (2 eV) with respect to Si substrate (Paivasaari et al., 2005; Pan, Chang, et al., 2010; Pan & Huang, 2011). In addition, Ho_2O_3 possesses the highest electronegativity and the highest lattice energy among all other eligible REOs as shown in Fig. 2.14 indicating the least hygroscopic nature of Ho_2O_3 which would be favourable for implementing Ho_2O_3/Ge gate stack within the expected MOS scaling limit (Goh et al., 2017a; Iwai et al., 2002). Based on superior properties of Ho_2O_3 has been integrated as dielectric insulator material in sensor application for electrolyte-insulator-semiconductor (EIS) device yielding higher sensitivity and pH sensing efficiency (Pan, Huang, Lin, & Wu, 2010). Despite of such attarctive features the investigation on Ho_2O_3 based MOS is very scarce. In work of Pan, Chang, et al., (2010) a 11nm Ho_2O_3 /p-type Si stack has been developed utilizing RF sputtering with a subsequent RTA in O_2 ambient at temperature range $(600 - 800)$ ˚C. A well behaved *C-V c*urve with less hysteresis as shown Fig. 2.18 has been obtained which induced k ~10.1, and low interface trap density of $D_{it} \sim 3.10 \times 10^{11}$ $eV^{-1}cm^{-2}$ at 700 ˚C. The low interface trap density indicated thermodynamic stability of Ho_2O_3 during deposition process. A smooth surface has been formed with a roughness around RMS ~ 0.86 nm which aided in reducing leakage current density, $J_g \sim 10^{-8}$ A cm^{-2} order magnitude at V_g = -1V as in Fig. 2.19. However, one order magnitude higher leakage current density was found at 700 ˚C in counter to 800 ˚C RTA samples which has been attributed to the increment of surface roughness due to crystallization or grain decomposition. Paivasaari et al., (2005) showed that, Ho_2O_3/Si film grown using ALD at 300 ˚C induces dielectric constant of 9.9 with low leakage current density of $J_g \sim 1.2 \times 10^{-8}$ A cm^{-2} at E_{Bd} ~ 2.06 MV cm^{-1}. However, the surface roughness might be affected by the contaminants (carbon, sodium, and hydrogen) from

reactor and precursor which limits the usage of this procedure. In works of Castan et al., (2015), $HoTiO_x$ metal insulator metal (MIM) was developed through ALD at 300 °C following RTA process in N_2 ambient. It is observed that, $HoTiO_x$ film with higher Ho content possess a poor *C-V* characteristic, but the gate leakage is less. This has been attributed to better re-crystallization of Ho-O content during annealing. However, a well behaved *C-V* has been reported for 16 nm-$HoTiO_3$/Si gate stack fabricated from reactive sputtering and subsequent annealing process. It was found that, well crystallized $HoTiO_3$ was formed at 700 °C inducing low leakage current density $J_g \sim 1.2 \times 10^{-8}$ A cm^2 and hysteresis < 9 mv (Pan, Yen, Hu, & Sheng, 2010). Till to date there has been no pertinent study for integration of Ho_2O_3/Ge based MOS device.

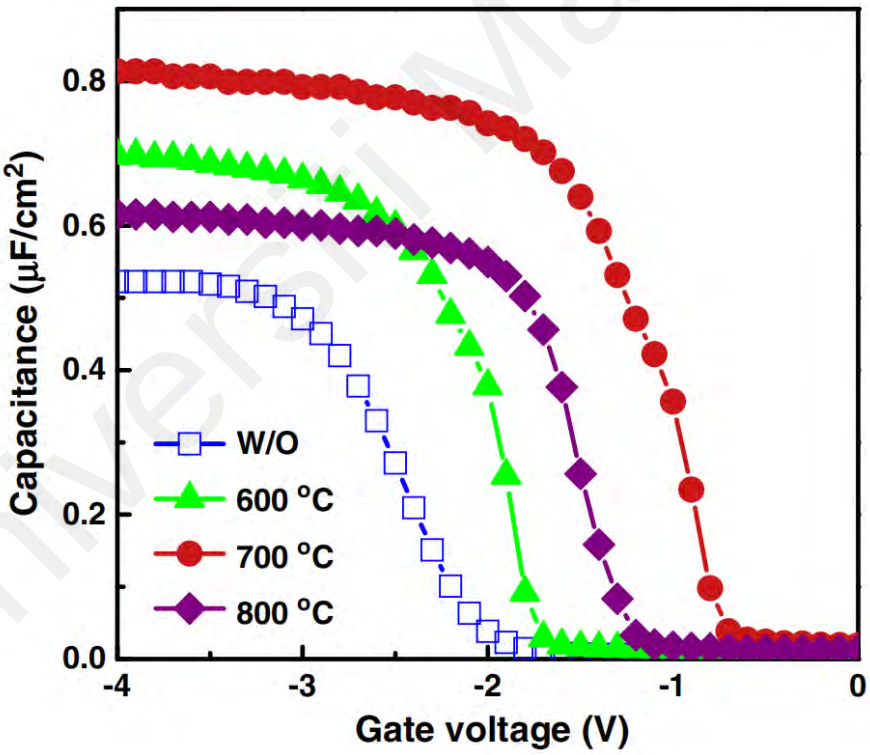

Figure 2.18: *C-V* curve for Ho_2O_3/Si gate stack for diiferent annealed temperatures (Pan, Chang, et al., 2010).

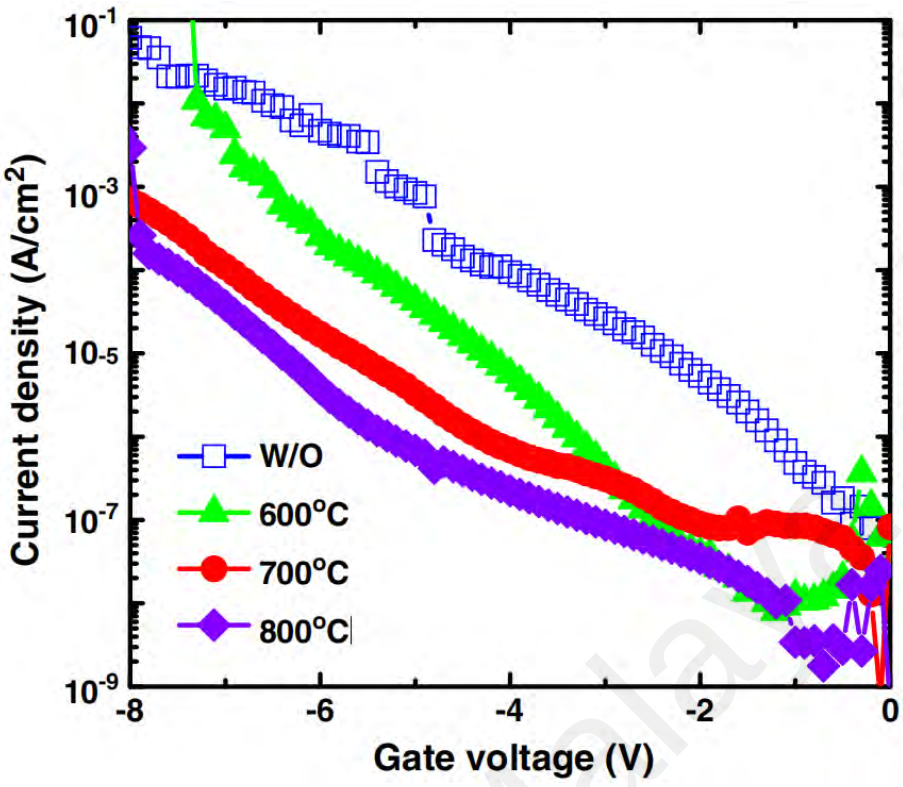

Figure 2.19: Leakage curren density (*J-V*) with respect to gate voltage for Ho_2O_3 / p type Si gate stack annealed at different RTA temperatures (Pan, Chang, et al., 2010).

2.12 Role of Nitrogen (N) for Ge passivation

Surface nitridation procedure using N_2 and/or NH_3 has been comprehensively examined in several studies for the stabilization of high-*k* oxide/Ge (Dushaq, Rasras, & Nayfeh, 2016; Fukuda et al., 2011; Kutsuki et al., 2009; Maeda et al., 2004, 2006; Mallem et al., 2019; Xie et al., 2012). Since, single layer of Ge−N/Ge−O−N possess low dielectric constant and so more investigation was focused on using Ge−N/Ge−O−N as an interfacial layer in conjunction with high-*k* dielectric layer. It was found that incorporation of N atom into GeO_2 forming Ge−O−N/Ge−N interfacial layer improves dielectric constant and thermal stability of the gate stack (Bhatt, Chaudhuri, Kothari, Nainani, & Lodha, 2013; Dushaq et al., 2018; Q. L. Li et al., 2011; Maeda et al., 2007; Otani et al., 2007). Nevertheless, improvement of electrical properties was found for directly grown Ge−N interfacial layer on Ge substrate topped with High-*k* gate stack.

Otani et al., (2007) reported that for $Ta_2O_5/Ge_3N_4/Ge$ gate stack inserting a 2 nm thick Ge−N interfacial layer beneath Ta_2O_5 exhibits low $D_{it} \sim 4.0 \times 10^{11}$ eV^{-1} cm^{-1} at mid-gap while more improvement of $D_{it} \sim 1.84 \times 10^{11}$ eV^{-1} cm^{-1} at mid-gap was reported with slightly thick 2.4 nm Ge_3N_4 for HfO_2/Ge gate stack (Maeda et al., 2007; Otani et al., 2007). However, the key perspective is that creation of Ge−N/Ge−O−N interfacial layer beneath the dielectric layer with incorporation of N atom improves the thermodynamic stability, dielectric constant, and electrical properties of High-*k*/Ge interface. It has also been reported that blocking capability of Ge−N/Ge−O−N hinders the inter-diffusion and Ge surface oxidation which is advantageous removing Ge dangling bonds and blocking the formation unstable GeO_x contents in some extent and thus improving the interface quality (Kutsuki et al., 2009; Maeda et al., 2006). Furthermore, incorporation N during REOs has been considered an effective way to passivate GeO_x which improves the thermal stability and electrical properties of the gate stack. It has been reported that, N incorporation into La_2O_3 lessened the formation of GeO_x and germanate as a result thermodynamic stability increased leading a low interface traps up-to $D_{it} \sim 6.34 \times 10^{11}$ eV^{-1} cm^{-1} with a leakage current density $J_g \sim 10^{-4}$ A/cm^2 at $V_g = 1V$ (Z. X. Cheng, Liu, Xu, Huang, & Lai, 2016). Typically, N_2O and NO gases are extensively utilized in semiconductor industry during thermal oxidation/nitridation process. N_2O was used for this investigation due to its higher activation energy and less toxicity than NO. Several reported literatures (Lei et al., 2017; Wong & Cheong, 2011b, 2012a) evidenced that MOS gate stack established from the combination of metal deposition utilizing radio frequency (RF) magnetron sputtering with subsequential thermal oxidation/nitridation flowing N_2O gas could enhance the dielectric film quality and improve the electrical features.

CHAPTER 3: RESEARCH METHODOLOGY

3.1 Research Overview

This chapter focuses on describing and illustrating the experimental methods and materials applied in this research. Typically, high-*k* gate oxide on Ge should maintain all the six requirements listed in section 2.5 for MOSFET operation enduring thermal budget at least 400 °C for 10 min while using thermal oxidation and nitridation (Goley & Hudait, 2014; Kamata, 2008). Moreover, several previous reports have evidenced that variation in deposition condition in terms of oxidation/nitridation temperatures and durations could significantly impact the interface morphology, electrical and thermodynamic properties of MOS capacitors (Hetherin et al., 2017a; Lei et al., 2018). Hence, the framework for the experimental steps and designated variables were employed for this investigation according to Fig. 3.1. The experimental and sample preparation methodology are segmented into three sections:

(i) Required Materials.

(ii) Experimental Methodology.

(iii) Characterization techniques.

The dimensions of the required materials are segmented into four sub sections as follows:

(i) Dimensions of Ge substrate material.

(ii) Chemicals applied for Ge substrate and quartz tube cleaning.

(iii) Chemicals and gases applied for Sm, Ho and Al sputtering process.

(iv) Gases applied during thermal oxidation/nitridation process.

The sequential steps required for sample preparation are shown in Fig. 3.2. The experimental method for sample preparation is mainly segmented in four sequential steps (i) Ge substrate cleaning (ii) Sputtering of metal (Sm) and metal (Ho) (iii) thermal oxidation/nitridation and (iv) top electrode and back contact deposition for MOS structure.

The physical and electrical characterization used in this research is shown Fig. 3.3. The physical properties are analysed using four physical characterization techniques which involves (i) X-Ray Diffraction (XRD) (ii) X-Ray Photoelectron Spectroscopy (XPS) (iii) RAMAN Spectroscopy (iv) High Resolution Electron Transmission Microscopy (HRTEM). The electrical characterization consists of two fundamental features which are (i) Current – Voltage (*I-V*) measurements (ii) Capacitance – Voltage (*C-V*) measurements.

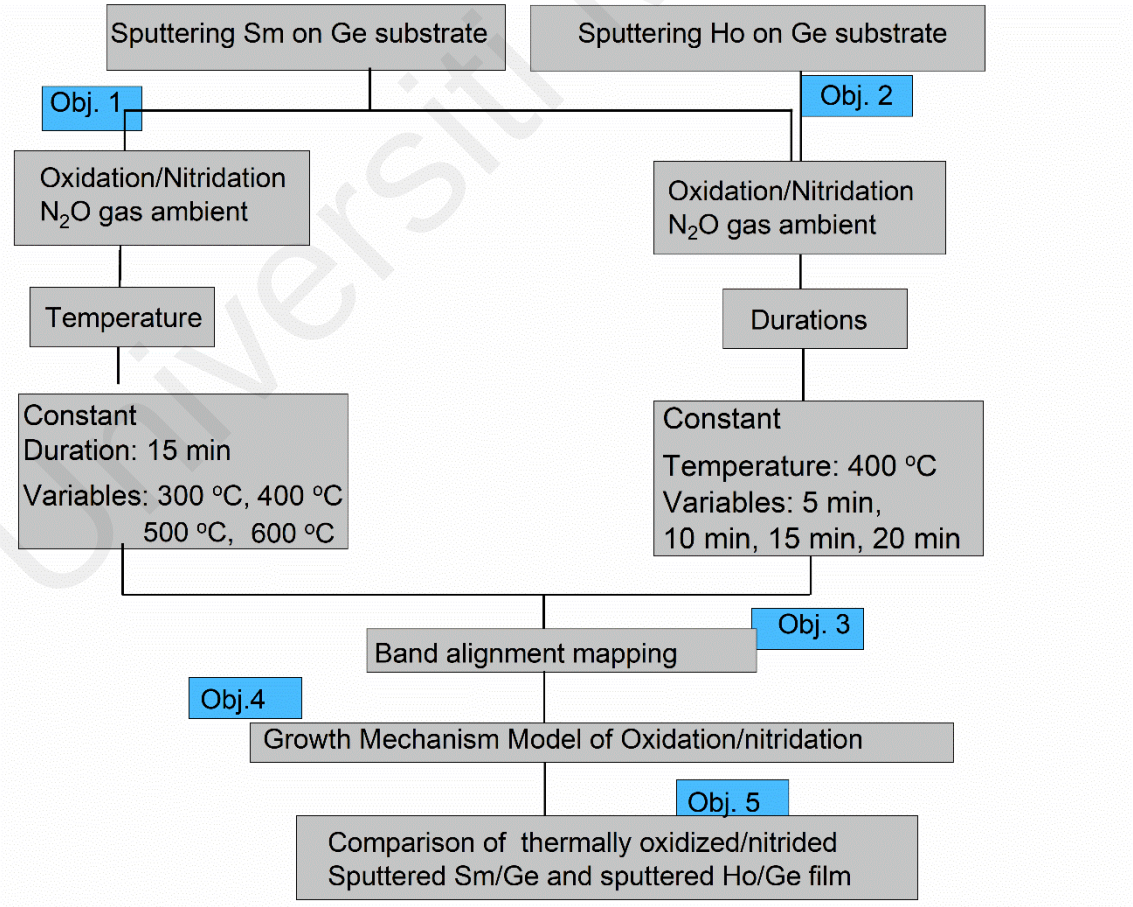

Figure 3.1: Experimental design and variables for investigation.

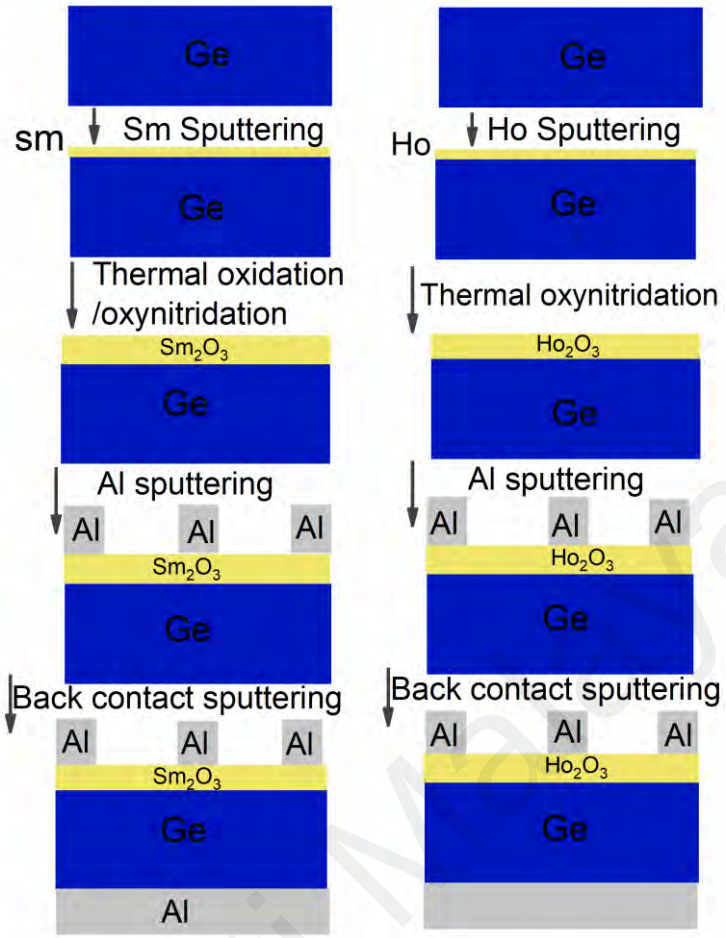

Figure 3.2: Sequential Steps for Sample Preparation.

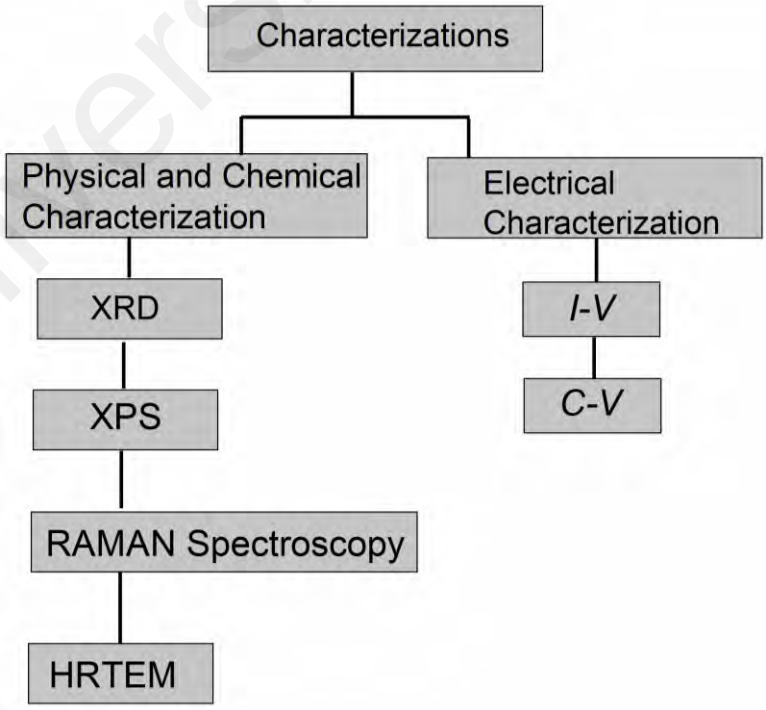

Figure 3.3: Overview of characterization techniques.

3.2 Required Materials

3.2.1 Dimension of Substrate Material

The substrate material using for this research is Germanium (Ge). The Ge wafers used in this research following the dimension as n-type, antimony (Sb) doped Ge:Sb (100) orientation with resistivity of (0.005 – 0.02) Ωcm and with a one-sided polished surface. The Ge wafers were supplied by Wafer World, Inc.

3.2.2 Chemical Required for Substrate and Quartz Tube Cleaning

Chemical that has been used for Ge substrate cleaning is hydrofluoric acid (HF). For the dip-cleaning process HF solution was prepared with ratio maintaining (HF: H_2O = 1: 50). On the other hand, Acetone has been utilized as chemical material during the cleaning of quartz tube of the thermal furnace. The details parameter of chemical materials utilized for Ge substrate and quartz tube cleaning is given in Table 3.1.

Table 3.1: Parameter details of chemical utilized for Ge substrate and quartz tube cleaning.

No	Chemical	Chemical Formula	Assay (%)	Supplier /(CAS) No
1	Hydrofluoric Acid	HF	49%	R & M chemicals 7664-39-3
2	Acetone	$(CH_3)_2CO$	>99%	R & M chemicals 67-64-1

3.2.3 Chemical, Gas and Materials for Sputtering Process

Rare earth metals of pure Samarium (Sm) and pure Holmium (Ho) has been utilized for sputtering process as target source for high-*k* deposition. Aluminum (Al) has been used as target source in the sputtering process during deposition of top electrode and bottom contact. The inert Argon (Ar) gas was utilized as sputtering gas. Acetone has been

utilized as chemical agent for cleaning the sputter chamber and substrate holder. The details parameter of chemical, gas and materials utilized during sputtering procedure is given in Table 3.2.

Table 3.2: Parameter details of chemical, gas, materials used during sputtering process.

No	Chemical and Material	Chemical Formula	Specifications	Supplier /(CAS) No
1	Samarium	Sm	Purity: 99.9%, Diameter: 101.6 mm, Thickness: 3.175	Kurt J. Lesker
2	Holmium	Ho		
3	Aluminum	Al		
3	Acetone	$(CH_3)_2CO$	>99%	R & M chemicals 67-64-1
4	Argon	Ar	Purity: 99.99%	Gaslink 7440-37-1

3.2.4 Required Gases for Sputtering Process

Two types of gases have been utilized during the thermal oxidation/nitridation process which are nitrous oxide (N_2O) and inert Argon (Ar). The detail specifications of these gases in terms of chemical formula, purity, and supplier have been given in Table 3.3.

Table 3.3: Detail specifications for gases used during thermal oxidation/nitridation.

No	Chemical	Chemical Formula	Purity (%)	Supplier /(CAS) No
1	Nitrous Oxide	N_2O	99%	Gaslink 10024-97-2
2	Argon	Ar	99%	Gaslink 7440-37-1

3.3 Experimental Procedure

3.3.1 Ge substrate Dip cleaning

In first step the Ge wafer is sliced into pieces at a dimension 1 cm × 1 cm using diamond cutter. In second step each of the sample pieces underwent for wet cleaning treatment. During the wet cleaning process the Ge substrates were dipped into hydrofluoric acid, HF solution (1:50 HF: H_2O) and deionized water DI water for 15s to eradicate native GeO_2 and any other contaminants. Sequentially, in the last step the wet substrates were dried using N_2 air gun. During the wet cleaning process, it is expected to remove native GeO_2, and any other additional impurities present in the substrate.

3.3.2 Sputtering of Rare Earth Metal on Ge substrate

Physical Vapor Deposition (PVD) radio frequency (RF) sputtering system (TF 450) model equipment has been utilized for sputtering process in this research. Before initiating the sputtering process the parts of sputtering system including the sputter chamber, target source holder, substrate holding plate, and shutter were cleansed using acetone to eliminate the possibility of contamination from these parts.

For fabrication of Sm_2O_3 gate stack pure samarium (Sm) metal and for Ho_2O_3 gate stack pure Holmium (Ho) metal was placed into the target holder as source material. Subsequently, Ge substrate sample pieces were laid on the substrate holding plate and then the gate of the sputtering chamber was shutdown. The distance of (Sm or Ho) target source with Ge substrate holder plate was about 0.2 meter. Fig. 3.4 displays the schematic of (RF) sputtering system. In summary, during the metal sputtering stage metallic rare earth metal (Sm) or (Ho) with thickness of 3-nm is being sputtered on the cleaned Ge substrate through radio frequency (RF) sputtering system (TF450) from rare earth metal (Sm or Ho) target source. The radio frequency (RF) sputtering system was regulated at

the RF power of 170 W, base pressure of 3×10^{-5} mbar, sputtering time of 75 s and inert Argon (Ar) gas flow rate of 25 cm^3/min during the sputtering process

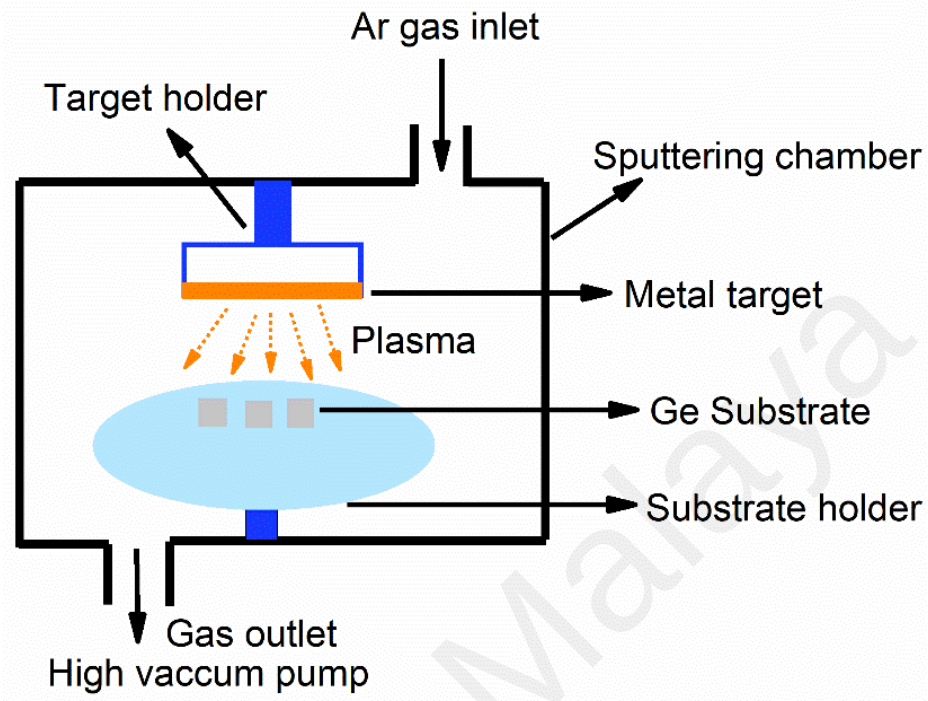

Figure 3.4: Schematic of PVD RF sputtering system.

3.3.3 Thermal Oxidation and Nitridation Process

In this research Carbolite CTF model no: (12/65/550) tube furnace has been utilized for conducting thermal oxidation and nitridation process. Thermal oxidation /nitridation (oxy-nitridation) processes were carried in N_2O gas ambient, for both sputtered (Sm) and sputtered (Ho). Before initiating the thermal oxidation and oxidation/nitridation processes, quartz tube and sample carrier quartz boat were cleaned applying acetone $(CH_3)_2CO$. Then, the samples standing in the quartz boat was placed into the middle location of horizontal CTF tube furnace as displayed in Fig.3.5. Subsequently, the desired gas is flowed when the furnace reached set temperature according to experimental variables. The section below demonstrates the design for each oxidation and oxidation/nitridation setup.

To explore the impact of various oxidation/nitridation temperatures for sputtered Sm on Ge substrate, thermal oxidation/nitridation were conducted at different temperature 300 °C, 400 °C, 500 °Cand 600 °C using CTF tube furnace in N_2O ambient. The samples of sputtered Sm on Ge substrate were placed into the middle of horizontal tube furnace and heated up from room temperature (heating rate of 10 °C/min) to the experimental setting temperature for each sample in an Ar ambient. When the furnace tube has reached the experimental set temperature (300 °C, 400 °C, 500 °C and 600 °C) N_2O gas was purged into the horizontal tube with a gas flow rate of 150 mL/min for 15 min and Ar gas flow is turned off. The furnace tube was cooled down to room temperature and then the samples were taken out.

To explore the influence of various oxidation/nitridation durations for sputtered Sm/Ge and sputtered Ho/Ge, thermal oxidation/nitridation was conducted at different durations of 5 min, 10 min, 15 min and 20 min at 400 °C using CTF tube furnace in N_2O ambient. Samples of sputtered Sm/Ge were placed into the center of furnace tube for fabricating Sm_2O_3 stack. On the other hand, for fabricating Ho_2O_3 gate stack samples of sputtered Ho/Ge were placed into the center of furnace tube. Subsequently, the furnace tube with the samples of (sputtered Sm/Ge or Ho/Ge) was heated up from room temperature to a set temperature of 400 °C (heating rate of 10 °C/min) in an argon (Ar) ambient. When the set temperature was achieved, Ar gas supply has been turned off while N_2O gas purged into the horizontal tube using flow rate of 150 mL/min for various oxidation/nitridation durations (5, 10, 15, and 20 min). When the furnace tube cooled down to room temperature and then the samples are brought out.

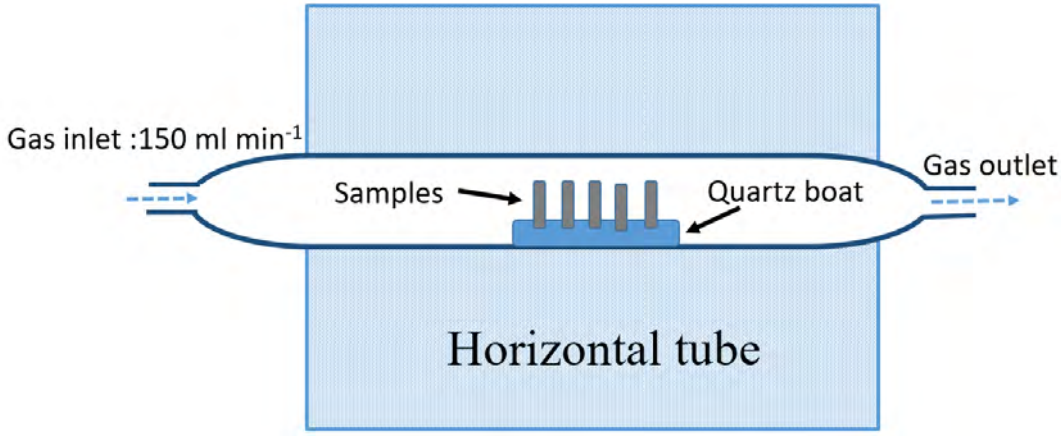

Figure 3.5: Schematic of horizontal furnace tube setup for thermal oxidation and nitridation.

3.3.4 MOS Capacitor Test Structure

To examine the electrical properties of dielectric films, MOS capacitors test structures with area 500 µm × 500 µm was fabricated. Firstly, 100 nm Aluminum (Al) metal electrode was formed by sputtering Al target on the oxidized/nitrided film through a shadow mask using Physical Vapor Deposition (PVD) radio frequency (RF) sputtering system (TF 450) as presented in Fig. 3.6. Afterwards, 100 nm ohmic contact is formed on the backside of the Ge substrate by sputtering Al without shadow mask. The sputtering process of Al follows the same sequential steps as described for metal (Sm) and (Ho) sputtering procedure shown in earlier Fig. 3.4. For electrode deposition and ohmic contact formation metal Al was placed into the target holder as source material. The radio frequency (RF) sputtering system was regulated at the RF power of 170 W, base pressure of 4.93×10^{-7}mbar, and inert Argon (Ar) gas flow rate of 25 cm^3/min during the sputtering process.

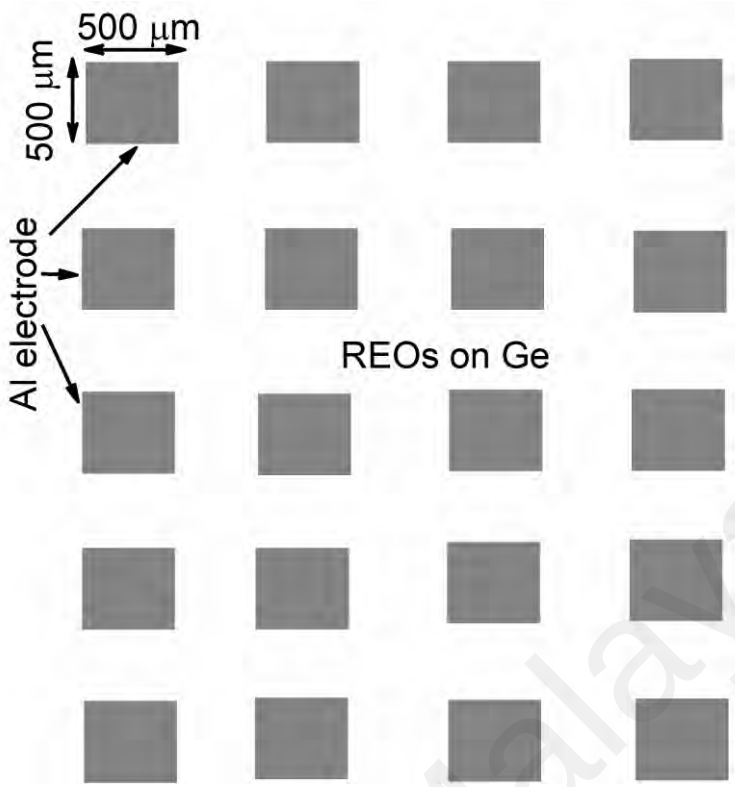

Figure 3.6: Al Gate electrode deposited in top of REOs/Ge.

3.4 Characterization Techniques

3.4.1 Xray Diffraction (XRD) Analysis

XRD is widely used versatile characterization technique which could effectively deliver the chemical analysis report including elemental detection of the deported thin film demonstrating the phase identification, and crystallinity information. (e.g. amorphous or polycrystalline). This technique also well recognized for phase identification. In addition, XRD could also provide information regarding chemical composition and crystal structure of the deposited film. This information is gathered by the monochromatic Xray diffraction interference Xray within the crystal atoms at specified diffraction angle according to Eq. 3.1.

$$\lambda = 2dsin\theta \qquad \text{(Equation. 3.1)}$$

Where,

$\lambda =$ Wavelength of Xray radiation beam (nm),

$d =$ Interplanar spacing in a crystal atom (nm)

$2\theta =$ Diffraction angle between the diffracted and transmitted beam (°)

In order to verify crystal phase orientation and crystallinity of the fabricated films X-ray diffraction (XRD) pattern were collected from Rigaku Miniflex Benchtop diffractometer. As X-ray radiation source copper radiation (Cu Kα) has been applied corresponding operating power 40 kV with a wavelength $\lambda \sim 0.154$ nm and the measurement were taken at scan range $2\theta = 10°$ to 80° at scanning rate 0.02°. The XRD pattern for designated sample can be obtained by plotting the intensity of Xray with respect to the diffraction angle 2θ.

It is important to evaluate the crystallite size and micro-strain in order to get insight on peak broadening due to crystal defect or dislocation. Peak broadening caused by crystallite size occurs due to incoherent dispersion between finite size elements. On the other side the peak broadening due to strain is initiated by the dislocation or non-uniform displacements of atom with the reference to lattice position. The crystallite size can be estimated using both Debye–Scherrer equation and Williamson − Hall (W - H) plot. The crystallite size using Debye–Scherrer approach is calculated using Eq. 3.2 (Goh et al., 2016b; Hetherin, Ramesh, & Wong, 2017b; J. W. Zhang et al., 2014).

$$\boldsymbol{D = \frac{k\lambda}{\beta_D \cos\theta}} \qquad \text{(Equation 3.2)}$$

Where, D is the crystalline size, K is the shape factor which is a constant (0.9), λ is the wavelength of Cu Kα (0.154 nm), β_D is the peak width with half maximum intensity

and θ is the peak position. Since the Debye–Scherrer equation only provides lower bound of crystallite size while micro-strain is not considered in this calculation. Thus, William-son - Hall (W-H) plot was applied for calculating both crystallite size (D) and micro-strain (ε) at the same time for various diffraction angles (2θ) from the obtained XRD patterns of the thin film samples. Alongside with crystallite size (D), micro-strain (ε) of finite size particles is another important independent factor that can affect the peak broad-ening of the diffraction pattern. Hence, the total peak broadening of a diffraction pattern is an accumulated impact induced from combination of crystallite size and micro-strain which can be expressed as Eq. 3.3.

$$\boldsymbol{\beta_\tau = \beta_D + \beta_\varepsilon} \qquad \text{(Equation. 3.3)}$$

Where, β_τ is the total peak broadening, β_D and β_ε are the peak width with half maximum intensity due to crystallite size and induced strain, respectively. The induced strain (ε) due to crystal defect or dislocation of atom is given by Eq. 3.4

$$\boldsymbol{\varepsilon = \frac{\beta_\varepsilon}{4\tan\theta}} \qquad \text{(Equation. 3.4)}$$

Replacing and rearranging the Eq. 3.2 and Eq. 3.4 into Eq. 3.3 gives the W-H as Eq. 3.4.

$$\boldsymbol{\beta_\tau \cos\theta = \frac{\kappa\lambda}{D} + 4\varepsilon \sin\theta} \qquad \text{(Equation. 3.5)}$$

A graph of $\beta_\tau \cos\theta$ versus $4\varepsilon \sin\theta$ will be plotted according to Eq. 3.5. The intercept of the graph is equal to $\frac{\kappa\lambda}{D}$ which provides the estimation of crystallite size D, whereas the gradient (slope) of linear regression gives the micro-strain, ε value.

3.4.2 X-ray Photoelectron Spectrometer (XPS) Analysis

The interface chemical bonding states and chemical compositions of the oxidized/nitrided sputtered Sm/Ge thin films has been quantified ULVAC-PHI Quantera II, X-ray photoelectron spectrometer (XPS) with an X-ray source of monochromatic Al-k_α ($hv = 1486.69$ eV) was used. The chemical composition was measured from combination of both survey scan and narrow scan. Both survey scan and narrow scan was recorded at X-ray operating power of 50 W, X-ray beam size with an area of 300 μm × 300 μm using take off angle 45° with reference to normal surface. For the elemental analysis, survey scan has been recorded using high energy passing energy of 112 eV and energy resolution of 1eV/step. Afterwards, for chemical states quantification narrow scan has been recorded using a low passing energy of 112 eV with energy resolution 0.1 eV/step. In order to establish the band alignment mapping of Sm_2O_3/Ge interface an additional valance band scan was operated using this XPS system applying passing energy ∼112 eV and higher energy resolution step size 0.1eV/step at binding energy ranging from -5 to 20 eV.

On the other side X-ray Photoelectron spectroscopy (model: Thermo Scientific K-Alpha) were used to study chemical compositions and chemical bonding states of thermally oxidized/nitrided sputtered Ho/Ge thin films. Both survey scan and narrow scan measurements were conducted at output power 150 W, with area of 400 × 400 μm^2 (X-ray beam size), take of angle 0° with respect to the normal surface. The survey scan was performed at passing energy of 160 eV and energy resolution of 1eV/step. Subsequently narrow scan measurement was taken at a low passing energy of 20 eV with high resolution step size 0.1 eV/step. Band alignment mapping of Ho_2O_3/Ge structure was also investigated from the XPS measurements. Considering the band alignment analysis, a valance band scan was performed using this XPS system where the binding energy ranging

from -5 to 20 eV with the same passing energy and energy resolution as used in this survey scan.

Deconvolution of the XPS spectrums was performed using CasaXPS software (version 2.3.19). Prior to deconvolution the linear background was corrected on this software. Afterwards, each of the narrow scan spectrums for both thermally oxidized sputtered Sm/Ge and Ho/Ge were calibrated with respect to C1s binding energy (B.E) at 284.80 eV (Lei et al., 2017) . The deconvolution of multiple peaks was processed by applying non-linear Gaussian-Lorentzian function during extraction of integrated area and fitting the line position (Wong & Cheong, 2011c).

3.4.3 RAMAN Analysis

Raman spectroscopy is well known as vibrational spectroscopic system which uses a monochromatic radiation from laser source to identify the existence of various organic and inorganic components residing into the crystals of material (Nickel, Friedrich, Rommelure, & Galtier, 2005). During RAMAN spectroscopy monochromatic radiation of phonons is irradiated on the material surface. As a result, the material surface molecules will be elevated to a higher level of excitement state due to high extent of molecular vibration. Subsequently new phonons will be generated from the surface once the molecular excitement is lowered to the preliminary position. According to the character of newly emitted phonons the species/compounds incorporating within the material has been identified by RAMAN spectroscopy (Larkin, 2017). In order to get further details on chemical composition and bonding stability Raman spectrums of thermally oxidized/nitrided sputtered Sm/Ge were collected from Horiba Xplora One Raman spectrometer using a scan ranging from (0 – 3000) cm^{-1}.

3.4.4 HRTEM Analysis

HRTEM is a kind of imaging microscope where transmission of electron beam at a higher energy level is being accelerated into the thin film sample plane. Due to the interference between sample film plane with the scattered/transmitted wave of electrons will generate an image of the sample plane. Afterwards, the sample plane image is being focused by an imaging device which produces high resolution magnified images. This image processing technique could capture images at atomic scale since the resolution is below 0.14 nm. HRTEM can come up with both real and reciprocal space information at the same time. Since, imaging mode for real space and diffraction mode for reciprocal space can run simultaneously (Kumar, Pavithra, & Naushad, 2019).

In this study, HRTEM was used to examine the cross sectional structural morphology and thickness of the thin film grown after thermal oxidation and nitridation. Before proceeding to HRTEM characterization samples underwent for focus ion beam lamella preparation employing Helios NanoLab 650 for attaining a cross-sectioned thin film. An additional sputtered Pt protective layer was deposited on the top of the sample surface in order to avert the ion bombardment defect induced during the focused ion beam lamella preparation. Afterwards, the cross-sectional morphology of the film was captured form the TECNAI G2 F20 high resolution transmission electron microscope. The HRTEM analysis was operated at enhanced voltage (20 – 200) kV with magnification scale 13.5 x to 134 kx. The pressure of HRTEM chamber was applied at 2.7×10^{-5} Pa in a vacuum ambient. In this study, HRTEM captured images of 1024×1024 pixels. Lastly, ImageJ software was used to extract the thickness from the HRTEM images. Furthermore, to verify the crystallinity, diffraction patterns of deposited thin films was generated employing Fast Fourier Transformation (FFT) process on HRTEM images regulated by ImageJ Software.

3.4.5 I-V Measurement

The current – voltage *(I-V)* characterization was performed from BPW-800 probe station linked with Keithley 4200 SCS semiconductor characterization system. The *(I-V)* measurement was reordered at frequency f ~ 50 Hz and sweep range (0 – 30) V with step size 0.05V. The current–voltage (*I-V*) measurement was transformed to leakage current density with respect to electrical field (*J-E*) plot by applying Equation Eq.3.6 (Hetherin et al., 2017a; Lei et al., 2018; Wong & Cheong, 2011b).

$$\mathbf{E} = \frac{V_g - V_{FB}}{t_{ox}} \qquad \text{(Equation. 3.6)}$$

Where, V_g denotes gate voltage, V_{FB} is flatband voltage and t_{ox} signifies total oxide thickness including interfacial layer.

3.4.6 C-V Measurement

The capacitance – voltage (*C-V*) characteristics were also gained from mutual arrangement system of BPW-800 8" probe station and Keithley 4200 semiconductor characterization system (SCS). For *C-V* measurement gate voltage was swept bidirectionally using linear DC voltage ramp. For forward bias condition the gate voltage was swept between +10 V to -10V while for reverse bias condition the gate voltage was swept ranging -10 V to +10 V. To observe the frequency dispersion behaviour the measurement was taken for various frequencies of 100 kHz, 500kHz and 1MHz using forward bias sweep +10 V to -10 V. Several important electrical features of MOS capacitors have been retrieved from *C-V* curve which includes dielectric constant k, effective fixed oxide charge, Q_{eff}, hysteresis amount, slow trap density (*STD*), Q_{it} and average interface trap density, D_{it}.

CHAPTER 4: RESULTS AND DISCUSSION

4.1 Introduction

According to the objective of this research, the experimental findings obtained from various characterization techniques has been analysed and described in this chapter. The chapter consists of four main sections: (i) effect of various thermal oxidation/nitridation temperatures on RF magnetron sputtered Sm/Ge in N_2O ambient (ii) influence of various thermal oxidation/nitridation durations on RF magnetron sputtered Sm/Ge in N_2O ambient. (iii) influence of various thermal oxidation/nitridation durations on RF magnetron sputtered Ho/Ge in N_2O ambient. (iv) Comparison between thermally oxidized/nitrided sputtered Sm/Ge and Ho/Ge stack.

4.2 Effect of Various Thermal Oxidation/Nitridation Temperatures on Sputtered Sm/Ge in N_2O Ambient

4.2.1 XRD Analysis

A detailed investigation of` XRD measurements were performed to examine the crystalline structure and crystallite growth of the developed thin film. Fig. 4.1 shows the diffraction spectrum of sputtered Sm on Ge substrate after oxidation/nitridation at different temperatures 300 °C, 400 °C, 500 °Cand 600 °C. Six diffraction peak of Trigonal-H, T-Sm_2O_3 are detected at diffraction angle of 27.16°, 31.15°, 47.28°, 48.26°, 54.04° and 56.36° corresponding to plane orientation (100), (101), (003), (110), (103) and (200) respectively for all the oxidized sample. Addition to these peaks one weaker peak of T-Sm_2O_3 found at 59.82° for 300 °C and a strong peak at 59.08° for 500 °C corresponding to plane (201). Two more T-Sm_2O_3 weak peak for 600 °C were detected at 40.98° and 60.48° corresponding to plane (102) and (004) respectively. These peaks were confirmed by Inorganic Crystal Structure Database (ICSD) reference code no. 647455 and 77685. The diffraction peak belongs to GeO_2 was detected in two different phases namely Tetragonal and Trigonal-H which are denoted as t_1-GeO_2 and t_2-GeO_2. Three diffraction peaks of t_1-GeO_2 were detected at 29.16°, 42.92°, 57.18° corresponding to (110), (111) and (211) plane, respectively for all the oxidized sample. The peak found at 29.16° increased sharply when the temperature raised to 600 °C while the peak broadened with lower intensities for 300 °C – 500 °C samples. The t_2-GeO_2 was detected at 39.22° corresponding to (102) plane for all samples except 600°C. Along with these peaks four more additional t_2-GeO_2 peaks were found for 300 °C in diffraction angles of 20.52°, 25.96°, 38.10° and 41.78° corresponding to (1 0 0), (101), (012) and (200) plane, respectively. t_1-GeO_2 and t_2-GeO_2 peaks were confirmed by ICSD reference code no. 158593 and 53870. A sharp peak belongs to Ge_3N_4 was found for 500 °C at diffraction angle of 31.72° corresponding plane (211) while at 35.76° a weak peak appeared with corresponding plane

(311) for all the oxidation temperatures. These diffraction peaks matched well with the ICSD reference code no. 97568 and 156338 which represents the cubic phase of c-Ge_3N_4. Moreover, for 600 °C orthorhombic o-Sm_4Ge_7 peaks were found at 22.84° and 39.14° with a plane of (101) and (203) respectively, while no such peaks were detected for other temperatures. These peaks were confirmed by the ICSD reference code 237695. However, there was no detectable diffraction peak from the substrate-Ge in the XRD pattern. Similar phenomenon was also observed in the XRD pattern of for ZrO_2/Ge system were prepared via thermal oxidation and nitridation in N_2O ambient (Lei et al., 2018). The XRD pattern confirms the formation of Sm_2O_3 for oxidation/nitridation temperature at (300-600) °C and presence of GeO_2, Ge_3N_4 and Sm_4Ge_7 indicates the formation of interfacial layer (IL) between oxide layer and Ge substrate. The findings also suggest that, the number of Sm_2O_3 peaks increased with the increment of oxidation/nitridation temperature which can be attributed to excessive diffusion of oxygen atoms from the atmosphere towards the high *k*/IL while increasing temperature. Conversely, the GeO_2 peak number decreases at 600 °C which might be due to in-diffusion of Sm or out-diffusion of Ge towards the high *k*/IL favouring the formation of Sm_4Ge_7 in place of GeO_2.

Furthermore, the highest intensity peak for Sm_2O_3 belongs to plane orientation of (110) and (201) for 300 °C and 500°C, respectively while (003) plane was highest for 400 °C and 600 °C samples. Meanwhile, the highest intensity peaks of GeO_2 for 300 °C were at t_2GeO_2 (101) plane and t_1GeO_2 (110) plane for rest of the samples. The highest diffraction peak intensity of Ge_3N_4 for 500 °C belongs to (211) plane while (311) plane was highest for 300 °C, 400 °C and 600 °C samples.

To investigate the effect of different oxidation and nitridation temperatures on the crystallinity of oxide and interfacial layer the highest intensities of Sm_2O_3, GeO_2 and Ge_3N_4 are plotted as shown in Fig. 4.2. Since the increase in intensities of diffraction peaks indicates the degree of crystallization. Hence, Fig. 4.2 reveals that GeO_2 has the highest intensities at 600 °C followed by 300 °C the second highest while intensities are almost same for 400 °C and 500 °C. This implies that, crystallinity of GeO_2 increases at higher oxidation temperature above 500°C. However, the peak intensity of GeO_2 is slightly higher for low temperature 300 °C in counter to 400 °C and 500 °C samples which indicates the improvement of GeO_2 crystallinity for 300 °C sample during the oxidation/nitridation process. The improved GeO_2 crystallinity at this oxidation/nitridation condition can be attributed to the self-diffusion of O atom from High-*k* interface. Consequently, increases the availability of O atom near the Ge substrate and inside the GeO_2 network which strengthens Ge−O inter-atomic bonding causing slightly intensified GeO_2 peak. The release of oxygen atom from Sm_2O_3 for 300 °C was evident from XPS Sm 3d spectra will be discussed in section 4.2.3. Meanwhile, the highest intensities of Sm_2O_3 and Ge_3N_4 are recorded at 500 °C. This observation indicates that, Sm_2O_3 and Ge_3N_4 are in more crystalline form for 500 °C while Sm_2O_3 and Ge_3N_4 appears to be in less crystalline form for rest of the temperatures. Comparing the intensities of Sm_2O_3, GeO_2 and Ge_3N_4 among all the temperatures it can be concluded that, both oxide and interfacial layer are relatively less crystalline for 400 °C sample.

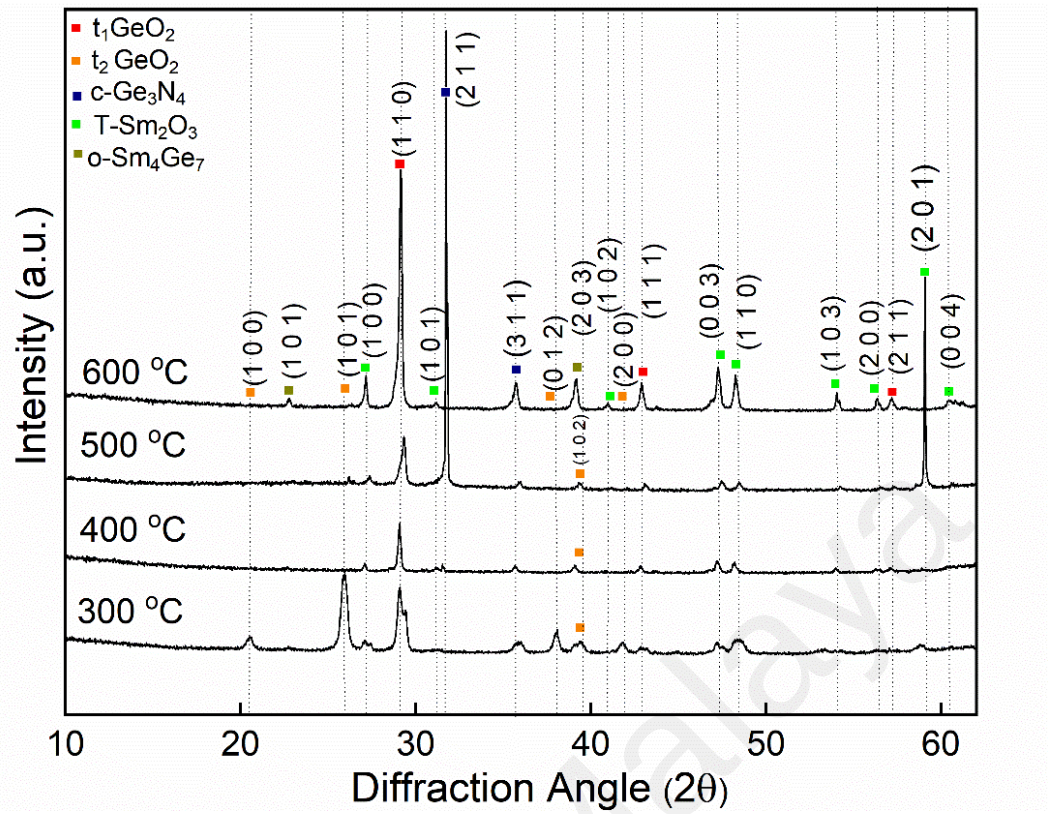

Figure 4.1: XRD patterns of the Sm based gate stack at various oxidation/nitridation temperatures of 300 °C, 400 °C, 500 °C and 600 °C.

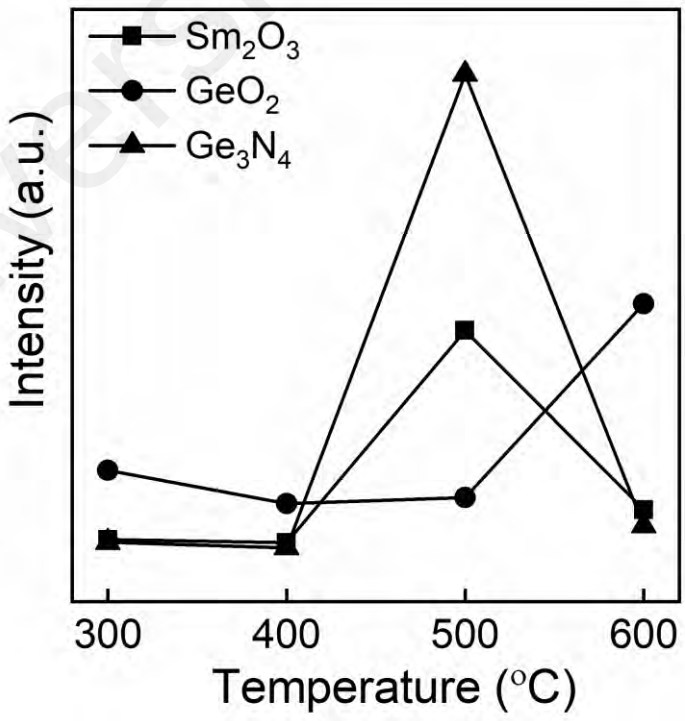

Figure 4.2: Intensities of Sm_2O_3, GeO_2 and Ge_3N_4 at various oxidation/nitridation temperatures (300 – 600) °C.

In order to get insight on peak broadening due to crystal defect or dislocation. crystallite size, (D) and micro-strain, (ε) has been estimated using Williamson - Hall (W-H) as described in section 3.4.1. A graph of $\beta_\tau \cos\theta$ versus $4\varepsilon \sin\theta$ for Sm_2O_3 and GeO_2 was plotted according to Eq. 3.5 as in Fig. 4.3. A linear fitting was performed with selected point from the distributed values at regression co-efficient $r^2 = 1$. According to Eq. 3.5 the crystallite size, D has been approximated from the intercept of the graph and micro-strain, ε was approximated from the gradient (slope) of the line. The crystallite sizes of Ge_3N_4 and Sm_4Ge_7 were not calculated because the number of peaks were insufficient for the calculation.

The crystallite size (D) and micro-strain (ε) calculated from W-H plot are shown in Fig. 4.4. The crystallite size of Sm_2O_3 for sample 300 °C, 400 °C, 500 °C and 600 °C are 18.39 nm, 32.48 nm, 32.26 nm, and 59.19 nm, respectively, while the crystallite size of GeO_2 increases gradually from 39.40 nm to 68.72 nm with increment of oxidation temperature. It is observed that, Sm_2O_3 crystallite sizes at 400 °C and 500 °C exhibits very close value with smaller differences which might be due to more homogenous distribution of crystallites at these temperatures (Goh et al., 2016b). Meanwhile, all the samples show negative micro-strain values for Sm_2O_3 crystallite except sample oxidized at 300 °C. On the other hand, the micro-strain of GeO_2 crystallite exhibits positive values for all samples except 400 °C oxidized sample. Additionally, the highest micro-strain value for both Sm_2O_3 and GeO_2 crystallites were recorded at 300 °C while the lowest recorded at 400 °C. However, the micro-strain value of Sm_2O_3 crystallite was same for both 500 °Cand 600 °C while the second highest value of GeO_2 crystallite was recorded at 600°C.

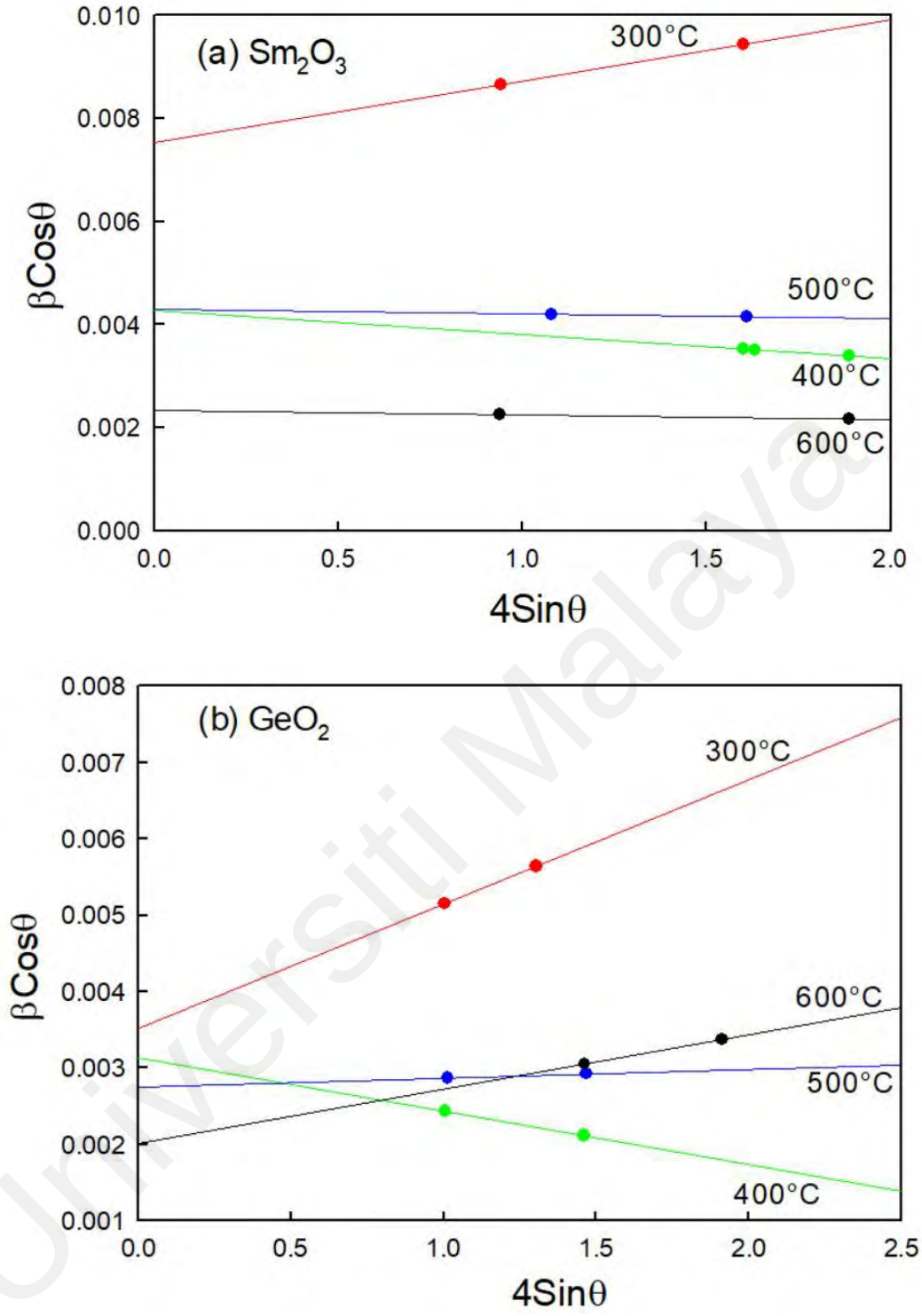

Figure 4.3: W–H linear regression plot of a. Sm_2O_3, b. GeO_2 at regression co-efficient $r^2 = 1$ for various oxidation/nitridation temperatures (300 °C, 400 °C, 500 °C, and 600 °C).

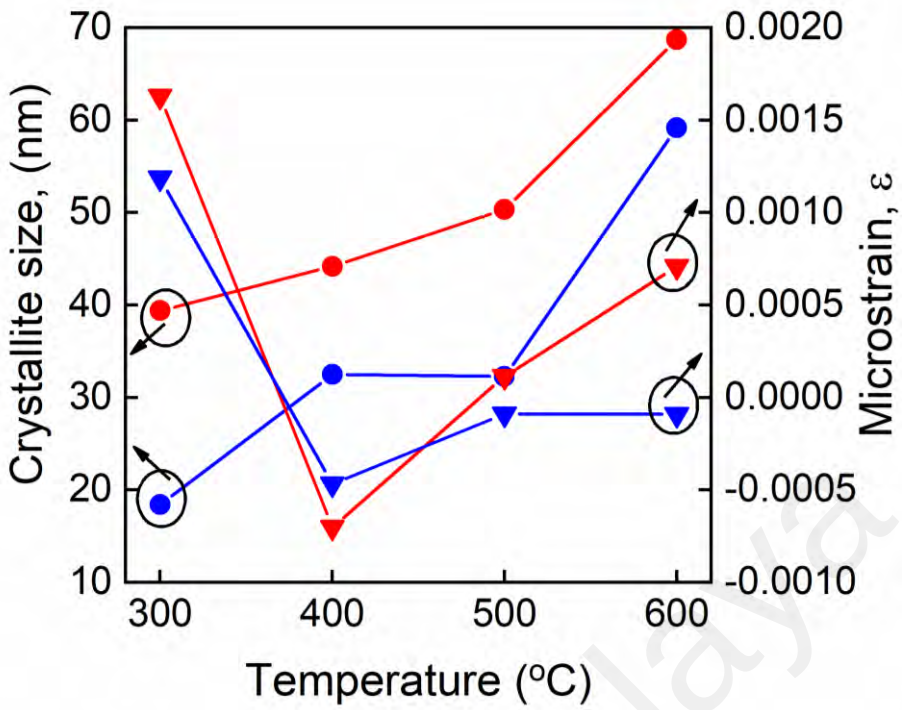

Figure 4.4: Micro-strain and crystallites of Sm_2O_3 and GeO_2 at various oxidation and nitridation temperatures (300 °C, 400 °C, 500 °C, and 600 °C).

4.2.2 J-E Characteristics

Fig. 4.5 displays the typical leakage current density Vs electrical breakdown field (*J-E*) for different oxidation/nitridation temperature 300 °C, 400 °C, 500 °C and 600°C. The (*J-E*) plot was converted from the current–voltage (*I-V*) measurement by using following Eq. 3.6. The sample that yields the highest breakdown electrical field, E_{BD} and the lowest leakage current density, J_g is considered as the best electrical properties. Two step breakdowns (E_{SBD} and E_{HBD}) are being observed for all the samples except 600 °C oxidized/nitride sample. The presence of interfacial layer and Sm_2O_3 layer is the reason behind two step breakdowns (Goh et al., 2016a; Wong & Cheong, 2011a). The breakdown at lower electric field along with relatively small instantaneous increment leakage current density is considered as soft breakdown, E_{SBD}. Conversely, the breakdown at higher electric field with large instantaneous increment leakage current density labelled as hard breakdown, E_{HBD}. The recorded electrical breakdown field of E_{HBD} for 300 °C, 400 °C, and 500 °C samples were 9.14 MV cm^{-1}, 13.31 MV cm^{-1} and 11.25 MV cm^{-1}, respectively.

The leakage current density of E_{HBD} for these samples were in 10^{-4}, 10^{-6}, and 10^{-5} order of magnitude, respectively. This analysis shows that 400 °C sample yielded the highest electrical breakdown field, E_{BD} of 13.31 MVcm^{-1} with lowest leakage current density, J_g of 8.38×10^{-6} A cm^{-2}. Therefore, 400 °C oxidized/nitrided sample has the best electrical properties for Sm_2O_3 dielectric MOS devices. For 600 °C sample *J-E* plot reveals almost a short circuit behaviour. The reason for short circuit nature is due to the formation of Sm−Ge metallic bond. The presence of Sm−Ge for 600 °C sample was confirmed from the XRD pattern. Moreover, 400 °C sample has shown comparatively higher electrical breakdown field and lower leakage current density than the reported literature of ZrO_2/Ge and Sm_2O_3/Si based MOS structure (Goh et al., 2016a; Lei et al., 2018).

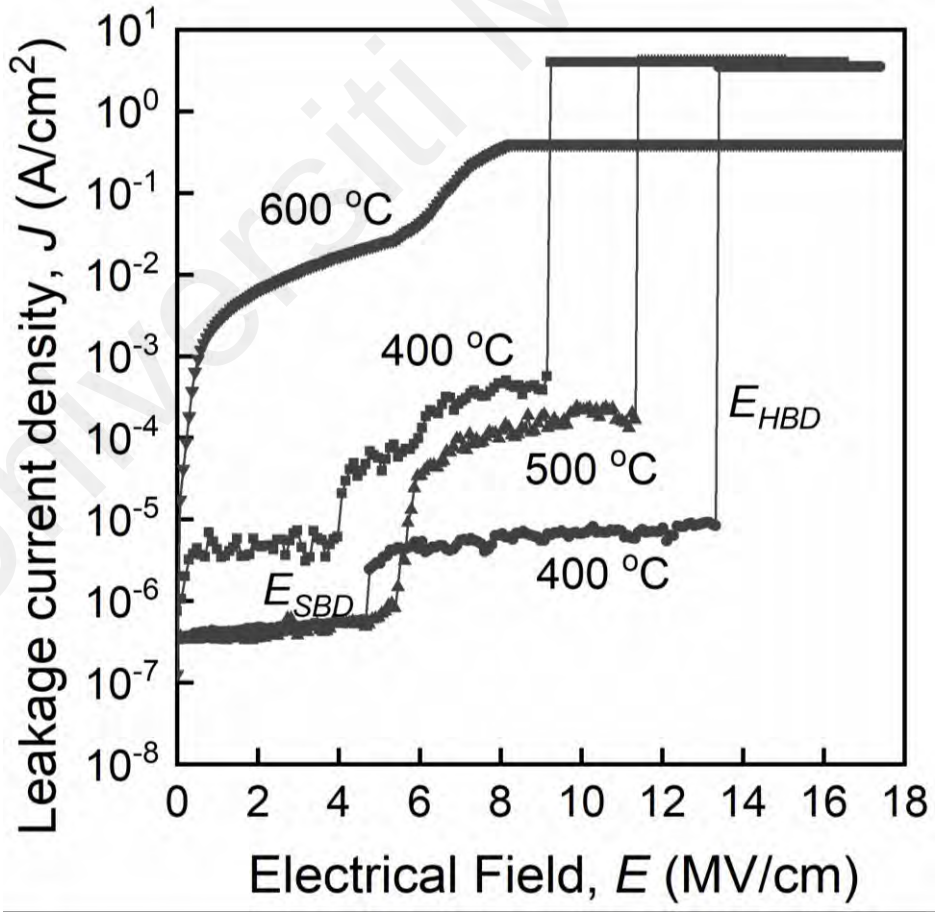

Figure 4.5: *J-E* characteristics of Sm_2O_3/Ge gate stack at different oxidation and nitridation temperatures (300 °C, 400 °C, 500 °C, and 600 °C).

4.2.3 XPS Analysis

Based on XPS wide scan Sm 3d, Ge 3d, Ge 2p, Ge 3s and O1s (data not shown) core level spectra were detected. The core level spectra of N1s were untraceable during the wide scan might be due to very low atomic percentage of nitrogen content below the XPS detection limit range (0.1 – 1) at %. Moreover, the deep penetration of N1s content nearby the Ge substrate during thermal oxidation/nitridation in N_2O ambient was evident from reported literature (Lei et al., 2018). Since Ge_3N_4 was observed in the XRD analysis and so it is suspected that N content is deeply seeded near the Ge substrate which was not detected in XPS measurement due to limited surface analysis depth (~5 nm). Narrow scan of core level spectrum Sm 3d and Ge 3d were performed to examine the structural and compositional changes of Sm_2O_3/Ge dielectric for various oxidation/nitridation temperatures (300 – 500) °C as shown in Fig. 4.6 and Fig. 4.8.

Fig. 4.6 shows the deconvoluted peaks of Sm 3d narrow scan for different oxidation/nitridation temperatures of 300 °C, 400 °C and 500 °C. For 400 °C and 500 °C samples the centroid Sm3d peak shifts positively towards higher binding energy by (0.20 – 0.37) eV with respect to reference position of Sm 3d at 1084.0 eV (C. C. Lin et al., 2014). The line position of Sm 3d spectra shifting towards higher binding energy clearly suggests the presence of Sm−O−Ge interfacial layer (IL) between the Sm_2O_3 film and Ge substrate. The growth of Sm−O−Ge is mainly related with the out-diffusion of Ge and Sm−O−Sm suboxide elimination. Since the Ge−Ge covalent bond breaks even at room temperature and so, out diffusion of Ge atom is more prominent at higher oxidation temperature (Mitrovic et al., 2014). It is well known that Ge is more electronegative than Sm (electronegativity Ge = 2.01 and Sm = 1.7 using Pauling's scale) indicating relatively higher electron accepting nature of Ge.

Thus, the diffused Ge atoms replaces the Sm atoms from Sm−O−Sm bonding configuration promoting the formation of Sm−O−Ge (C. C. Lin et al., 2014). Based on this assumption, it is suggested that positive shifting in 400 °C and 500 °C samples was due to partial elimination of Sm−O−Sm suboxide caused by out-diffusion of Ge atoms. Meanwhile it is noted that, 300 °C sample shifts slightly toward lower binding energy from the reference line position which indicates the deficiency of Sm−O−Ge as interfacial layer component.

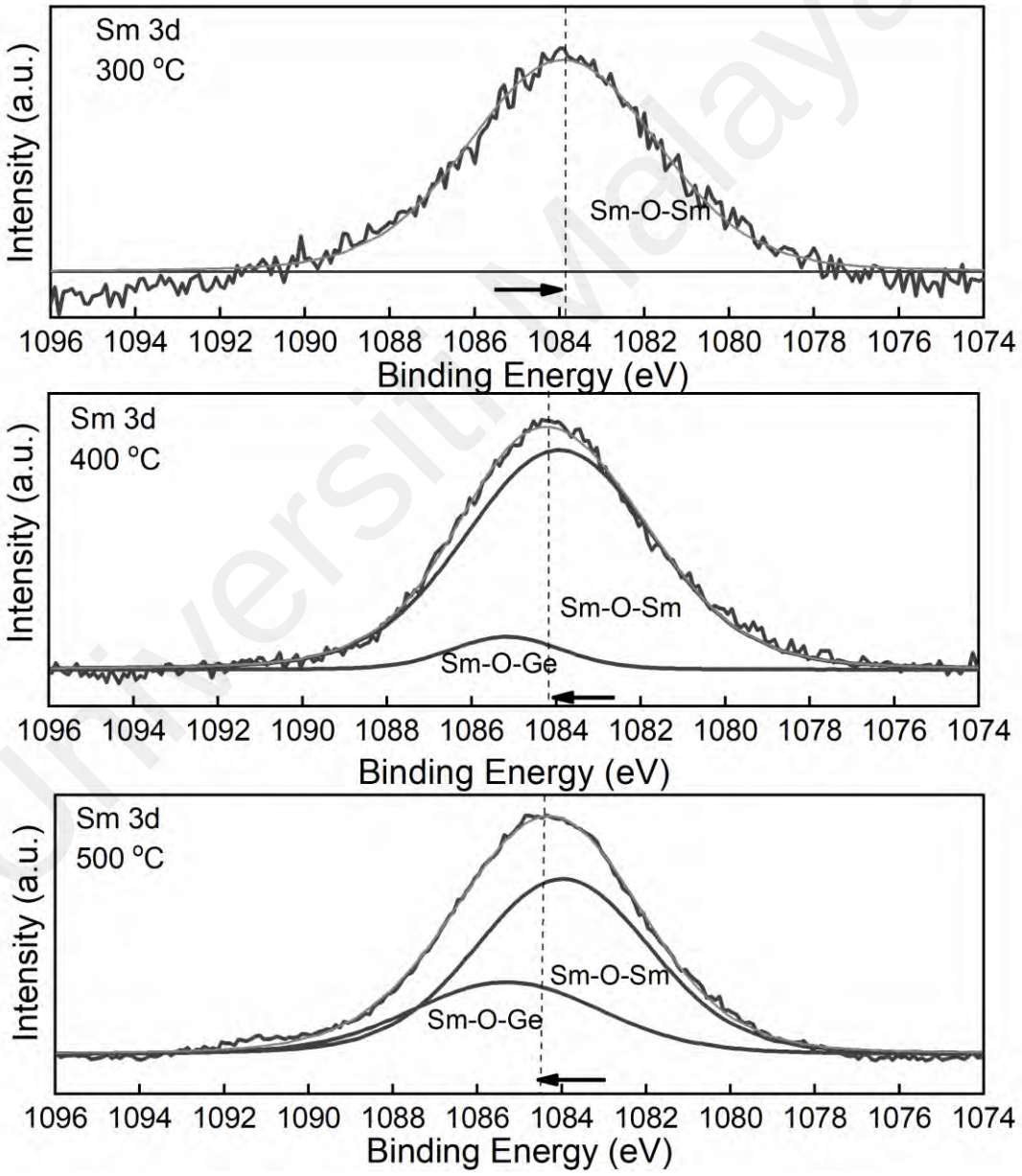

Figure 4.6: Sm 3d narrow scan deconvoluted spectra for various oxidation and nitridation temperatures (300 °C, 400 °C, and 500 °C).

According to the literature peak position of Sm_2O_3 was reported in lower binding energy at 1083.90 eV and Sm−O−Ge in higher binding energy at 1086.2 eV (C. C. Lin et al., 2014). The sample oxidized/nitrided at 300 °C comprises only a single peak in the lower binding energy at 1083.88 eV which confirms the formation of Sm_2O_3. For, sample oxidized/nitrided at 400 °C and 500 °C was deconvoluted into two peaks where Sm_2O_3 located at lower binding energy site and Sm−O−Ge on higher binding energy site. For 400 °C and 500 °C sample the Sm 3d peak belongs to lower binding energy site are at 1083.93 eV and 1083.97 eV for 400 °C and 500 °C, respectively which corresponds to Sm_2O_3. Sm 3d peak belongs to higher binding energy lies at 1085.17 eV and 1085.31 eV, respectively for these temperatures which corresponds to Sm−O−Ge.

The effect of different oxidation temperature on the growth of dielectric oxide is analysed by comparing the integrated peak area is of Sm_2O_3 and Sm−O−Ge. The Sm_2O_3 integrated peak area increased at 400 °C and reduced subsequently for 500 °C and 300 °C. On the Contrary, the integrated peak area of Sm−O−Ge increased gradually while increasing oxidation temperature from 400 °C to 500 °C. For 400 °C the increase of Sm_2O_3 and reduction of Sm−O−Ge is due to fewer diffusion of Ge atom into the Sm_2O_3 dielectric. Conversely, for 500 °C reduction of Sm_2O_3 and increase in Sm−O−Ge is mainly due to excessive amount Ge diffusion into Sm_2O_3 causing large amount Sm substitution during Sm−O−Sm suboxide elimination. For 300 °C the reduction of Sm_2O_3 and deficiency of Sm−O−Ge is due to O diffusion from the dielectric Sm_2O_3 itself toward the interface preventing the diffusion of Ge into Sm_2O_3 dielectric.

Fig. 4.7 depicts the oxidation level of 300 °C, 400 °C and 500 °C oxidized samples by plotting the binding energy shift of Sm 3d versus temperature. For 400 °C sample Sm 3d binding energy is closer to full oxidation level in counter to 500 °C indicating certain level of over-oxidation condition for 500 °C sample.

As of for 300 °C sample Sm 3d binding energy is below the full oxidation level indicating under-oxidation condition. From this observation it is evident that oxidation rate gradually increases with the increment of oxidation/nitridation temperature. In contrast with the *J-E* characteristics discussed in section 4.2.2 both the under-oxidation and over-oxidation condition influenced adversely on the electrical breakdown field voltage. The 400 °C samples exhibit moderate oxidation rate and the highest electrical breakdown field voltage.

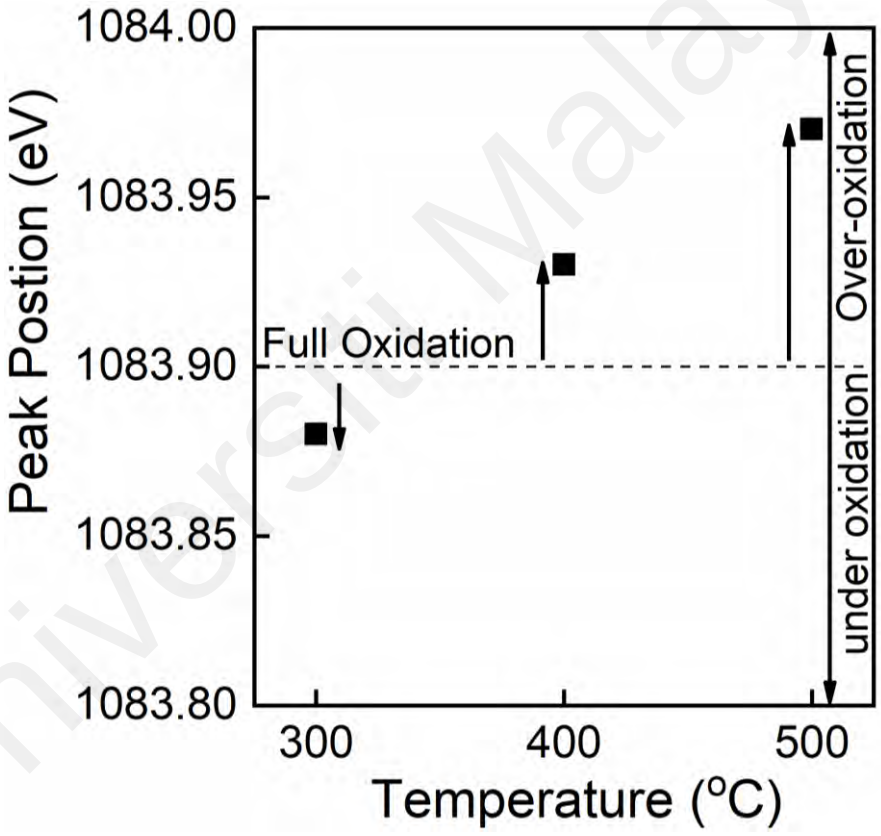

Figure 4.7: XPS Sm 3d narrow scan peak position of various investigated temperatures (300 °C, 400 °C and 500 °C).

Fig. 4.8 demonstrates the Ge 3d spectra at different oxidation and nitridation temperature of 300 °C, 400 °C and 500 °C. Ge 3d was deconvoluted into four peaks with the reference position of Ge $3d^0$ at 29.6 eV (Fu et al., 2014). The four peaks corresponding to Ge^{1+}, Ge^{2+}, Ge*, Ge^{4+} were well fitted with a core level shift of +0.8 eV, +1.8eV,

+2.4 eV and > +3 eV, respectively. It has been reported that, the shift lies at +0.8 eV can be denoted as GeO_x while shift lies at +1.8 eV was denoted as GeO (Mitrovic et al., 2014; J. Song et al., 2007). The Ge^{4+} was assigned for native oxide GeO_2 which is expected to appear in between +3 to +3.4 eV (Dimoulas et al., 2010; Mitrovic et al., 2014; Sasada, Nakakita, Takenaka, & Takagi, 2009). The shift lies at +2.4 can be ascribed as Ge* corresponds to Sm−O−Ge, since the metal germanate ($M_xGe_yO_z$) of rare earth material tends to occur in between the Ge^{2+} and Ge^{3+} in range of 1.8 eV to 2.8 eV due to second nearest neighbour effect (Mitrovic et al., 2014). From Fig. 4.8 it is evident that, the content of native oxide GeO_2 formed for all oxidation temperatures. A strong existence of $Sm_xGe_yO_z$ and GeO_x is found for the temperature 400 °C and 500 °C except 300 °C. Conversely, volatile GeO is found at 300 °C and 500 °C except 400 °C.

The effect of various oxidation temperature on interface stability is examined by comparing the integrated area of deconvoluted peaks from Fig. 4.8. The stoichiometric stable phases of GeO_2 with higher binding energy is found more for the sample oxidized at 400 °C and reduces subsequently at 500 °C and 300 °C samples. Consequently, the lower binding energy sub-stoichiometric component $Sm_xGe_yO_z$, GeO_x and GeO with unstable phase are fewer for 400 °C than those of 300 °C and 500 °C. In addition, 500 °C sample exhibits larger integrated area of stoichiometric GeO_2 and less GeO than 300 °C sample. Since GeO is the most thermally unstable interface component compare to other sub-oxide of Ge (D. Wang, He, Fang, et al., 2019). Hence, most pronounce growth of volatile GeO at 300 °C sample indicates highly defected interface quality which will deteriorate the electrical properties. The reduction of volatile GeO for both 400 °C and 500 °C sample can be attributed to the spontaneous formation of oxygen deficient $SmGeO_x$. The oxygen deficient $SmGeO_x$ traps the desorbing GeO and concurrently preserves the integrity of GeO_2 (H. Wang, Chroneos, Dimoulas, & Schwingenschlögl, 2012). In addition, the fewer unstable phases at 400 °C sample might be related to the formation of

amorphous Ge_3N_4 due to N^+ atom diffusion which effectively passivates excessive Ge diffusion during this oxidation-nitridation process (Maeda et al., 2007; Venkata Rao et al., 2018). The detail mechanism of GeO trapping, and Ge passivation will be discussed in section 4.2.6. Based on the above discussion it can be ascribed that, 400 °C oxidized sample exhibits more stable IL layer with high composition of stoichiometric components and fewer traps which will improve the electrical properties of the dielectric.

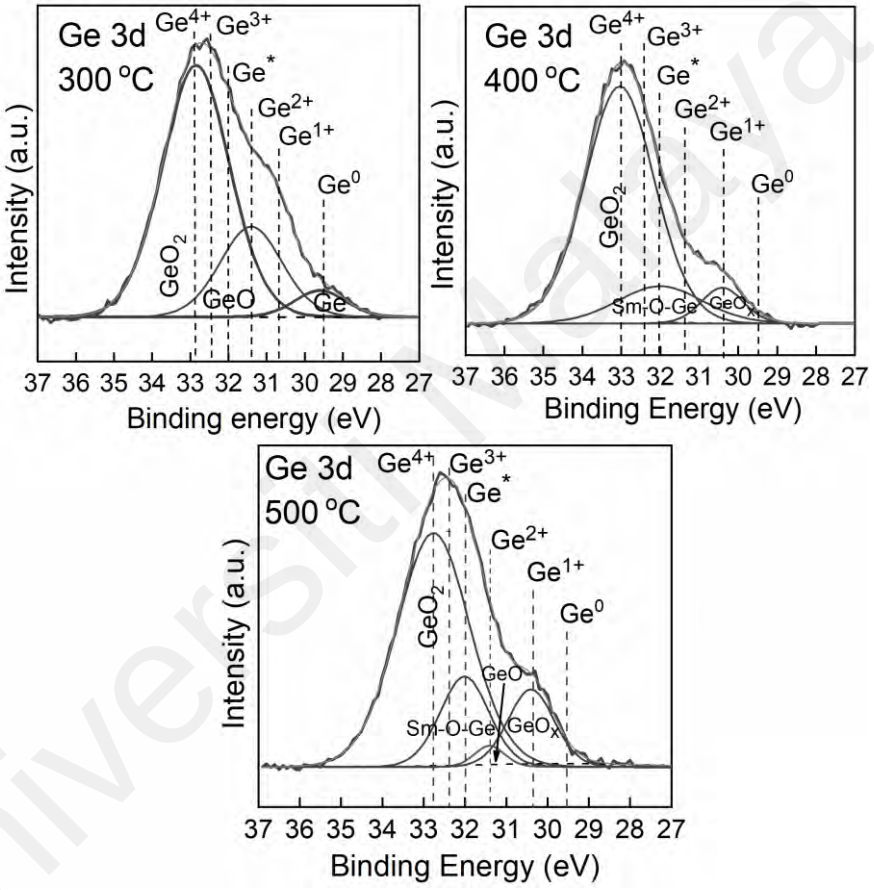

Figure 4.8: Deconvoluted Ge 3d narrow scan spectra of oxidized/nitrided sputtered Sm/Ge for various oxidation / nitridation temperatures (300 °C, 400 °C, and 500 °C).

4.2.4 Band Alignment

The band diagram of Sm_2O_3/IL/Ge was obtained for different oxidation temperature of 300 °C, 400 °C and 500 °C by deducing O1s plasmon loss XPS spectra and valance band spectra as shown in Fig. 4.9. Based on Krauts method the same extraction procedure described in the reported literature by Wong & Cheong, (2011a, 2012a) were

employed to determine the valance band edge, (E_v) and bandgaps, (E_g) of Sm_2O_3/IL. Fig. 4.9a illustrates the XPS valance band spectra for sample investigated at 300 °C, 400 °C and 500 °C. A typical small tail is observed in the valence band spectra which is considered as Ge signal. The valence band edge, (E_v) of Ge = 0.10 eV was used as reference from literature (Cao, Wu, Wu, & Li, 2017; S. J. Wang et al., 2004). The valance band edge, (E_v) for sm_2O_3/IL was calculated by extrapolation of the maximum negative slope near the edge to the minimum horizontal Ge signal baseline as illustrated in Fig. 4.9a (Cao et al., 2017; Wong & Cheong, 2011a). The valance band edge, (E_v) of Sm_2O_3/IL with respect to Ge substrate were estimated 3.27, 3.02 and 3.08 eV for 300 °C, 400 °C and 500 °C, respectively. The valence band offset, VBO (ΔE_v) was estimated from the difference between valance band edges, (E_v) of Sm_2O_3/IL and Ge using Eq. 4.1:

$$\Delta E_v\ (Sm_2O_3/IL) = (E_v)\ (Sm_2O_3/IL) - (E_v)\ (Ge) \qquad \text{(Equation 4.1)}$$

The valence band offsets, ΔE_v (Sm_2O_3/IL) were estimated 3.17, 2.98, 2.92 eV for 300 °C, 400 °C and 500°C, respectively. The conduction band offset, CBO (ΔE_c) of Sm_2O_3/IL/Ge can be estimated using the following Eq. 4.2, where E_g (Sm_2O_3/IL) and E_g (Ge) are the energy bandgaps of Sm_2O_3/IL and Ge respectively.

$$\Delta E_c\ (Sm_2O_3/IL) = E_g\ (Sm_2O_3/IL) - E_g\ (Ge) - \Delta E_v\ (Sm_2O_3/IL) \qquad \text{(Equation 4.2)}$$

The energy bandgap of Sm_2O_3/IL for different oxidation/nitridation temperature were extracted from their respective O1s plasmon loss XPS spectra as shown in Fig. 4.9b. The energy bandgaps E_g (Sm_2O_3/IL) were estimated to be ranging between 5.56 – 6.25 eV for the investigated oxidation/nitridation temperature. The energy bandgap, E_g (Ge) value of 0.67 eV was obtained from the report of (Kamata, 2008). Fig. 4.10 summarizes the schematic energy band alignment of Sm_2O_3/IL/Ge corresponding to different oxidation/nitridation temperature. The CBO, ΔE_c (Sm_2O_3/IL) were estimated 1.72, 2.60 and

2.05 eV respectively, for 300 °C, 400 °C and 500 °C sample as shown in Fig. 4.10. According to the band offset schematic it can be suggested that both VBO and CBO for oxidation/nitridation temperature (300 – 500) °C of Sm_2O_3 on Ge substrate is above 1 eV which makes it eligible contender for high-k dielectric on Ge based MOS devices. In addition, 400 °C exhibits the highest value of ΔE_c (Sm_2O_3/IL) compared to other investigated samples. The increment of ΔE_c (Sm_2O_3/IL) indicates reduction of defect gap states in the conduction band edge of Sm_2O_3/IL with Ge substrate. It is anticipated that, formation of stochiometric Sm_2O_3 and stable interfacial Sm−O−Ge at this temperature reduces defect gap states. During the formation of Sm−O−Ge the four folded configuration of Sm atom would permit to channel with four unoccupied bonds of Ge atoms eventually removing the Ge dangling bond causing defect gap state free Sm_2O_3/IL edge with Ge. The increase in ΔE_c (Sm_2O_3/IL) reduces the leakage current of and breakdown voltage of the device which is in well agreement with the *J-E* characteristics discussed in section 4.2.2. Furthermore, Fig. 4.9b reveals that energy bandgap, E_g of (Sm_2O_3/IL) for 300 °C and 500 °C drops by 0.69 eV and 0.61 eV, respectively than the 400 °C sample bandgap $E_g \sim 6.25$ eV. Decreasing of band gap for oxide/Ge interface can be attributed to the generation of defect states due to GeO (g) desorption (Kita, Lee, Nishimura, Nagashio, & Toriumi, 2009). Accordingly, for 300 °C and 500 °C samples it is considered that, desorption of volatile GeO (g) through the Sm_2O_3 dielectric film induced oxygen vacancy and Ge^{2+} defects in the Sm_2O_3/IL interface. These defects triggered the generation of interface defect states in the bandgap region of Sm_2O_3/IL interface causing bandgap reduction for these samples. However, all the investigated samples induced higher bandgap E_g (Sm_2O_3/IL) in counter to the typical Sm_2O_3 energy bandgap, $E_g \sim 4.33$ eV. Since, the bandgap was calculated including interfacial layer accordingly the energy bandgap E_g (Sm_2O_3/IL) was higher which might be due to the contribution of sandwiched interfacial layer between the Sm_2O_3 and Ge substrate.

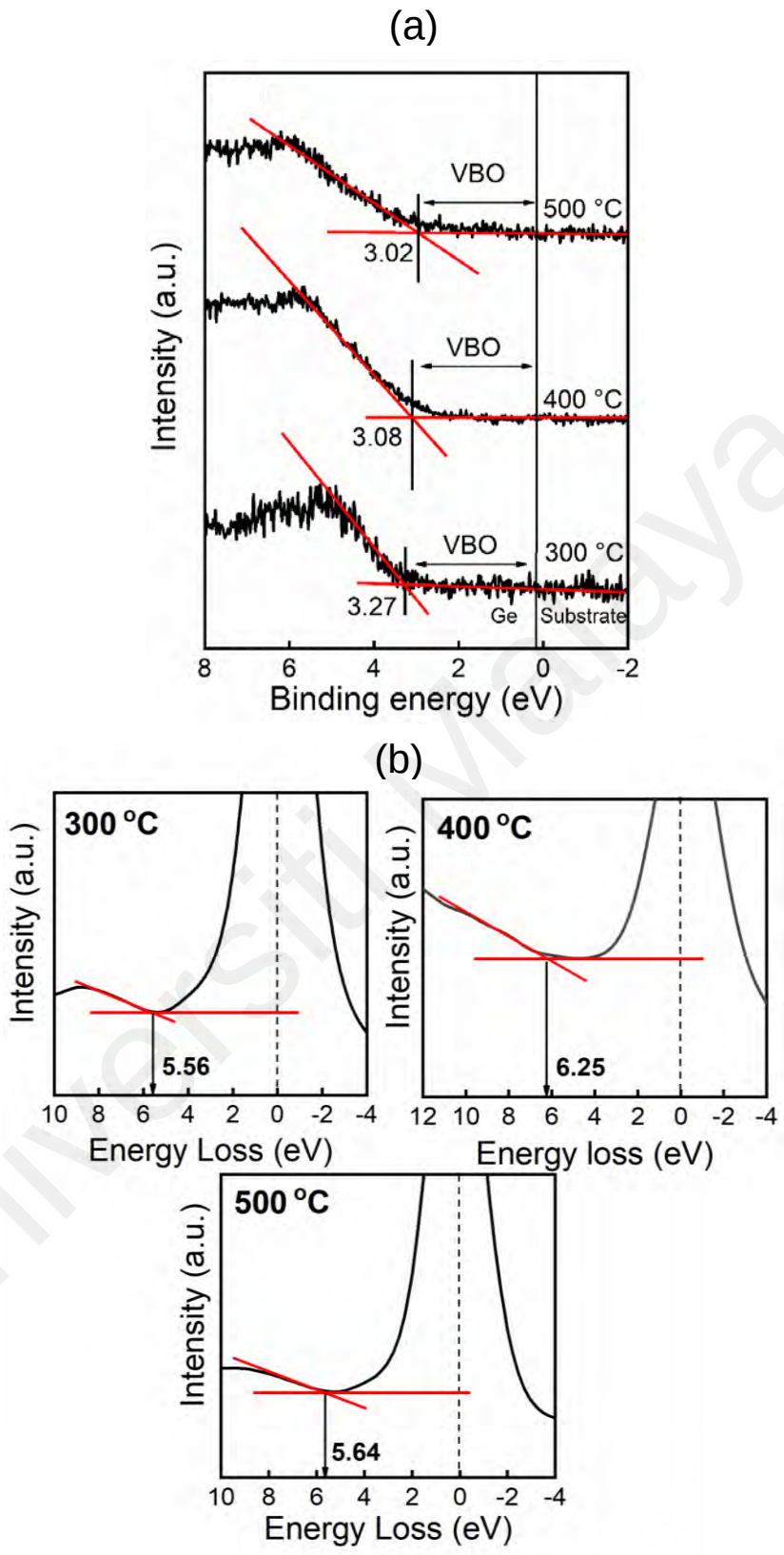

Figure 4.9: Estimation of valance band offset (ΔE_v) and energy bandgap (E_g) for Sm_2O_3/IL/Ge structure at various oxidation/nitridation temperatures 300 °C, 400 °C and 500 °C (a) Valance band edge, E_v and VBO extraction from XPS valence band spectra. (b) Energy band gap deduction from oxygen plasmon loss XPS spectra.

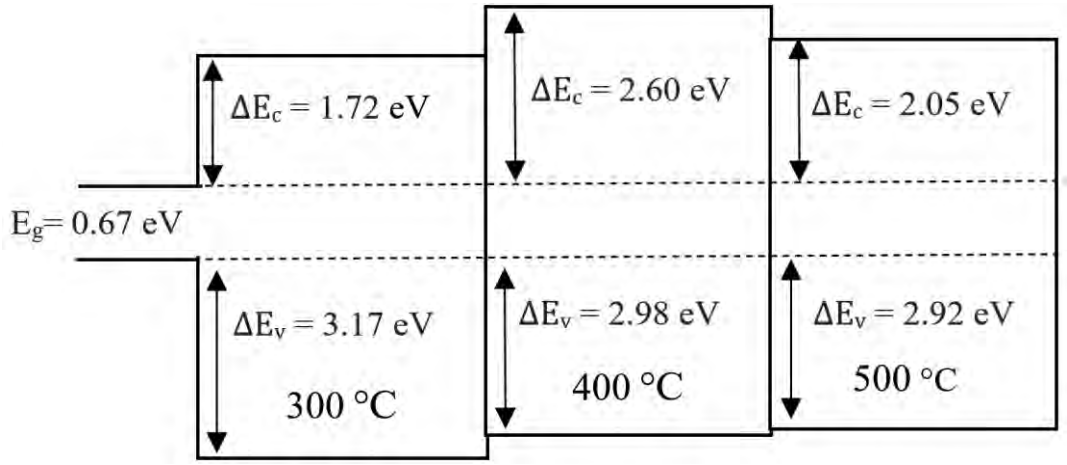

Figure 4.10: Schematic of band alignment for Sm_2O_3/IL/Ge gate stack for different oxidation/nitridation temperatures.

4.2.5 HRTEM Analysis

It is important to realize the relation between film thickness with the functioning oxidation and nitridation temperature of the fabricated Sm_2O_3 gate stack to verify the compliance with MOS scaling limit. The sample underwent for HRTEM analysis was selected based on their electrical properties where 400 °C sample is having the lowest leakage current density and 500 °C sample is having the second lowest leakage current. Hence, the cross-sectional view obtained from HRTEM for sample oxidized/nitride at 400 °C and 500 °C is shown in Fig. 4.11. Two distinguishable layers is clearly visible on the Ge substrate, which confirms the presence of interfacial layer along with oxide layer. The layer close to the Ge substrate is assigned as the IL layer while layer in the top with relatively larger distance from Ge substrate is assigned as Sm_2O_3 dielectric layer. According, XPS and XRD analysis the interfacial layer consists of Ge−O, Ge−N and Sm−O−Ge. The measured thickness of Sm_2O_3 dielectric for 400 °C and 500 °C sample was approximately 3.56 nm and 3.05 nm, respectively while the interfacial layer (IL) was around 2.44 nm and 3.26 nm, respectively. This result indicates that, the IL layer increases, and the oxide layer decreases with the increment of temperature. Based on the

result demonstrated in XPS analysis it can be assumed that degree of oxidation level increases with the increment of oxidation/nitridation temperature which caused severe out-diffusion of Ge into the Sm_2O_3 dielectric for 500 °C sample and thus increased the interfacial thickness. However, the obtained film thickness is not similar with the crystallite size trend of Sm_2O_3 ($18.39 - 59.19$ nm) and GeO_2 ($39.40 - 68.72$ nm) found from XRD. The possible reason could be attributed to the crystal alignment (Wong & Cheong, 2012c) as illustrated in Fig. 4.12 in which the approximated crystallite size of Sm_2O_3 (110) plane was not in the direction of $t_{ox(max)}$ or $t_{ox(min)}$while crystallite size of GeO_2 (110) plane was not in the direction of $t_{IL(max)}$ or $t_{IL(min)}$. The crystal plane orientation of Sm_2O_3 (110) and GeO_2 (110) were used as reference obtained from the XRD pattern.

Furthermore, to verify the crystallinity, diffraction pattern of the HRTEM images was obtained from ImageJ software using fast Fourier transform (FFT) method shown as inset image. Considering the inset FFT image it can be inferred that, 500 °C forms partially crystalline Sm_2O_3 layer which is confirmed by the presence of multiple spotted patterns while interfacial layer is found to be amorphous with cloudy spot pattern. Conversely, both the Sm_2O_3 and interfacial layer were in amorphous form (cloudy spot pattern) for 400 °C. This result is in well agreement with the crystallinity observed in XRD pattern section 4.2.1.

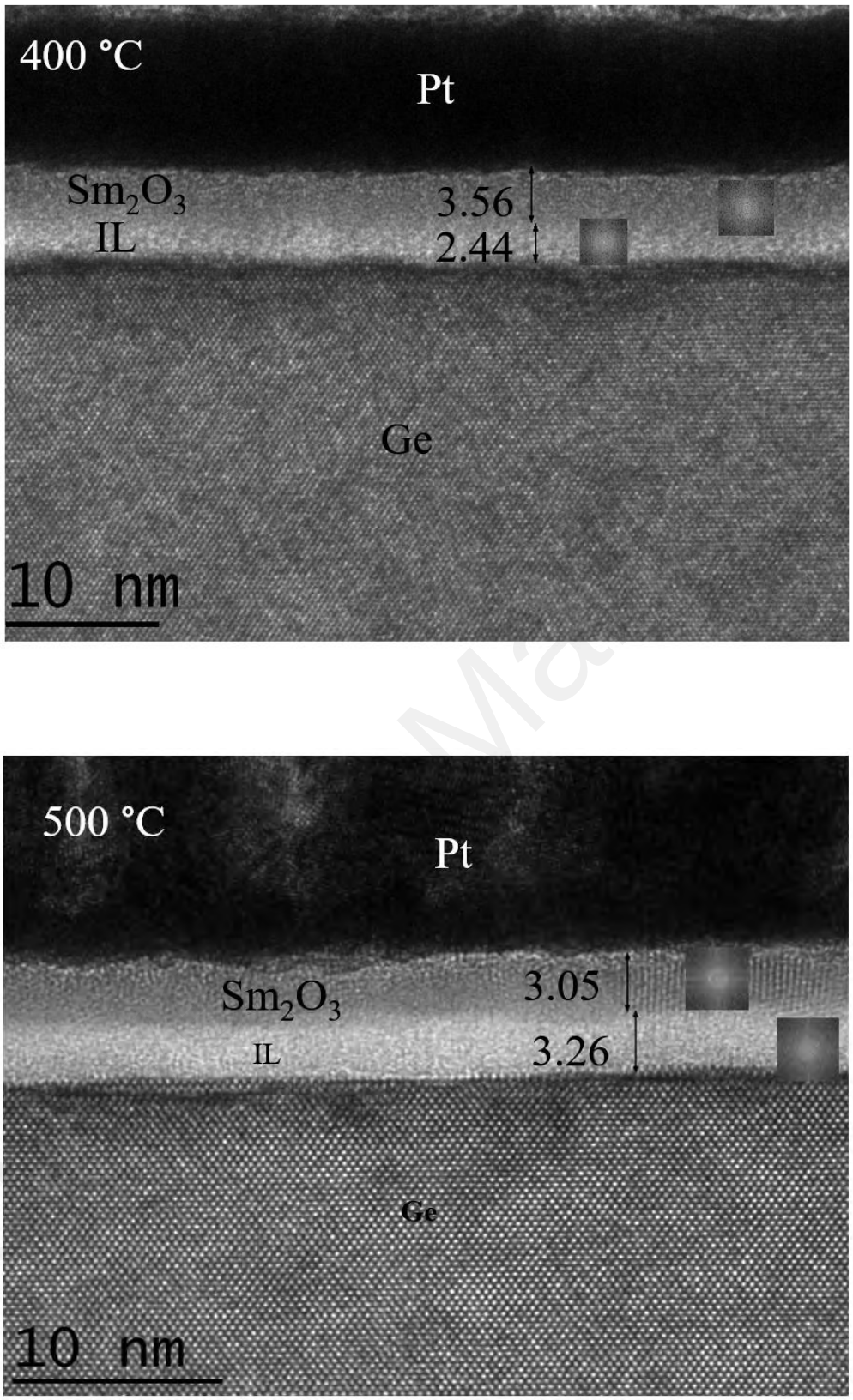

Figure 4.11: Cross-sectional HRTEM images of sputtered Sm/Ge samples oxidized/Nitrided at 400 °C and 500 °C. Inset showing diffraction pattern obtained using FFT method.

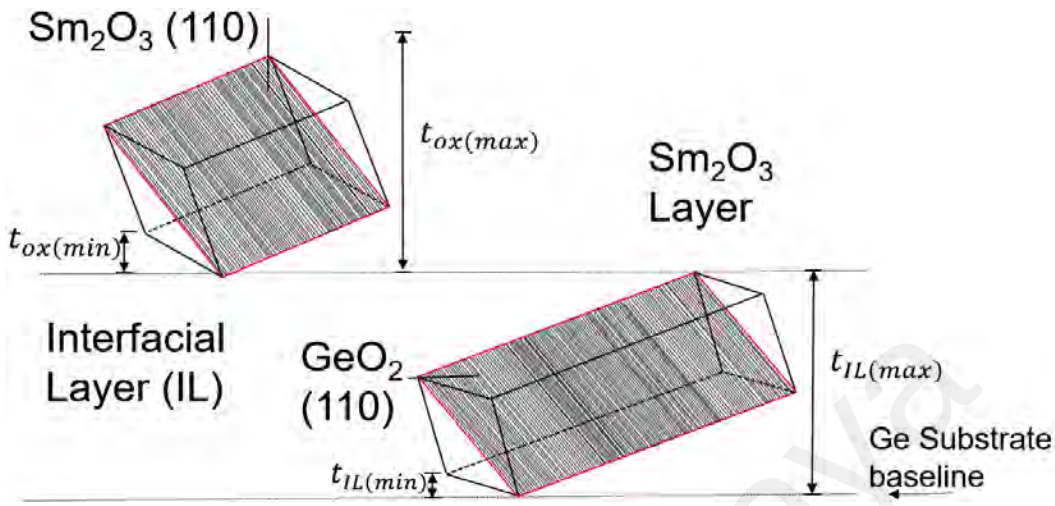

Figure 4.12: Schematic illustration of crystal structure arrangement for Sm_2O_3 (110) and GeO_2 (110) with respect to the thickness from the Ge substrate baseline.

4.2.6 Oxidation and Nitridation Mechanism Model

Based on the observation reported in XRD, XPS and HRTEM a possible oxidation and nitridation mechanism for Sm_2O_3/IL/Ge gate stack has been shown in Fig. 4.13 for various oxidized/nitrided sample at 300 °C, 400 °C, 500 °C and 600 °C. Initially, for all the investigated sample N_2O diffused and reacted with sputtered Sm of the Ge substrate surface according to Eq. 4.3:

$$2Sm + 3N_2O(g) \rightarrow Sm_2O_3 + 3N_2(g) \qquad \text{(Equation 4.3)}$$

Meanwhile, the extent of oxidation/nitridation increased for all the temperatures thus, N_2O gained enough energy to diffuse through the Sm_2O_3 dielectric and reacted with Ge substrate into two step reaction. In the first step only GeO_2 was formed with Ge wafer according to the reaction of Eq. 4.4 while in the second step both GeO_2 and Ge_3N_4 was formed by Eq. 4.5. It was assumed that some extent of Ge dangling bonds was passivated during the reaction of Eq. 4.5 creating an amorphous Ge_3N_4 in the interfacial layer. Presence of Ge_3N_4 for all the temperatures were confirmed in XRD analysis.

$$Ge + 2N_2O(g) \rightarrow GeO_2 + 2N_2(g) \quad \text{(Equation 4.4)}$$

$$4Ge + 2N_2O\,(g) \rightarrow GeO_2 + Ge_3N_4 \quad \text{(Equation.4.5)}$$

Concurrently, for 400 °C and 500 °C sample Ge atom out-diffused towards the Sm_2O_3 dielectric and reacted with Sm atom, since Ge atoms were active at these temperatures (Kamata, 2008; Lei et al., 2017). Subsequently, $SmGeO_x$ was formed in the IL layer according to Eq. 4.6 which was confirmed in XPS observation.

$$Sm_2O_3 + Ge \rightarrow SmGeO_x \quad \text{(Equation 4.6)}$$

Afterwards, for all the investigated sample once GeO_2 was formed volatile GeO (g) gas desorption occurred due to the redox reaction between GeO_2 and Ge wafer for all the investigated sample according to Eq. 4.7 (Kamata, 2008; Kita et al., 2008). For, 300 °C there was continuous desorption of GeO (g) into the dielectric through the interfacial layer which resulted in defective dielectric interface as shown in Fig. 4.13a

$$3GeO_2 + 3Ge \rightarrow 6GeO(g) \quad \text{(Equation 4.7)}$$

Since, at 300 °C temperature the extent of oxidation/nitridation was not adequate to fully oxidize the Sm_2O_3 dielectric hence additional O_2 in-diffused toward IL layer which strengthened the detrimental redox reaction of Eq. 4.7. Subsequently, for 400 °C and 500 °C sample GeO (g) desorbed into the IL layer and reacted with interfacial $SmGeO_x$. As a product denser $Sm_xGe_yO_z$ was formed with an additional growth of Ge sub-oxide GeO_x, by trapping the volatile GeO through the reactive reaction of Eq. 4.8:

$$SmGeO_x + GeO \rightarrow Sm_xGe_yO_z + GeO_x \quad \text{(Equation 4.8)}$$

Regarding the trapping process of GeO (g) into $SmGeO_x$, it is assumed that at the initial phase of the oxidation/nitridation an oxygen deficient $SmGeO_x$ was produced. Afterwards desorption of GeO (g) favoured the oxygen deficient $SmGeO_x$ to restore some of oxygen loss balancing the propensity of Sm and O (Mitrovic et al., 2014; Nishimura et al., 2011; H. Wang et al., 2012). This preceded to oxygen densification of oxygen deficient $SmGeO_x$ and thereby formed an amorphous sub-stoichiometric $Sm_xGe_yO_z$ with residual GeO_x in the IL layer as shown in Fig. 4.13b. Therefore, restricted the GeO (g) volatilization toward the Sm_2O_3 dielectric film. Since Sm_4Ge_7 was found in XRD for 600 °C, it is assumed to be formed by the reaction of Eq. 4.9.

$$2Sm_2O_3 + 20GeO \rightarrow Sm_4Ge_7 + 13GeO_2 \qquad \text{(Equation 4.9)}$$

It is thought that excessive desorption of GeO(g) at this temperature damaged the Sm_2O_3 dielectric leaving several metallic defects as shown in Fig. 4.13c which resulted in a short circuit as illustrated in section 4.2.2 *J-E* characteristics.

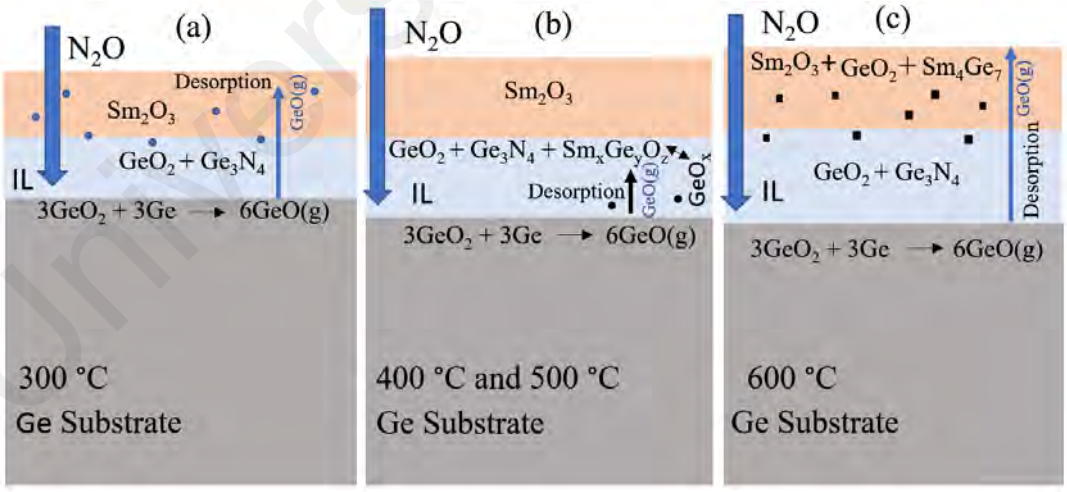

Figure 4.13: Schematic of a possible oxidation and nitridation mechanism and layer distribution model for different temperature oxidized/nitrided sputtered Sm/Ge sample a. 300 °C b. 400 °C and 500 °Cand c. 600 °C.

4.2.7 Capacitance-Voltage (C-V) Characteristics

Fig. 4.14 illustrates the *C-V* characteristics of the investigated samples of different oxidation/nitridation temperature 300 °C, 400 °C and 500 °C. The *C-V* measurement was taken at frequency of 100 kHz and gate bias was bi-directionally swept from -1 V to +1.5 V. The inset of Fig. 4.14 shows the relationship of effective dielectric constant (k) and different oxidation/nitridation temperature. The effective dielectric constant (k) were extracted by using the Eq. 4.10 (Goley & Hudait, 2014).

$$\boldsymbol{C_{ox} = \frac{k\varepsilon_o A}{t_{ox}}} \qquad \text{(Equation 4.10)}$$

Where, C_{ox} is the oxide capacitance, (k) is the dielectric constant, ε_o is the permittivity of free space, $8.854 \times 10^{-12} Fm^{-1}$, A is the capacitor area and t_{ox} is the total physical oxide thickness including Sm_2O_3 layer and the interfacial layer of the deposited film. Since, A and ε_o are constant for this work, it can be anticipated that the oxide capacitance is proportional to $\frac{k}{t_{ox}}$. Hence, the oxide capacitance is influenced by the physical oxide thickness and dielectric constant.

From Fig. 4.14 it is clearly visible that, 400 °C sample yielded highest oxide capacitance among the investigated samples. It was evident from the HRTEM analysis that 400 °C induces lower thickness than 500 °C hence, increasing the oxide capacitance. Moreover, the highest dielectric constant, k_{eff} value was obtained for 400 °C which leads to the higher oxide capacitance. The increase of k_{eff} can be attributed to the higher concentration of Sm_2O_3 and better thermal stability of Sm_2O_3/IL/Ge structure at this oxidation/nitridation condition (Pan & Huang, 2010). Although the lowest Sm_2O_3/IL thickness were estimated at 300 °C yet exhibits the lowest oxide capacitance which is due to lowering of effective dielectric constant, k_{eff}. The reduction of dielectric constant can be

attributed to the degraded interface quality of oxide/IL/Ge structure. In addition, the equivalent oxide thickness (*EOT*) estimated for the Sm_2O_3/IL/Ge MOS interface were 0.75 nm, 0.61 nm, and 0.68 nm for 300 °C, 400 °C and 500 °C, respectively obtained from their respective dielectric constant, k_{eff} value.

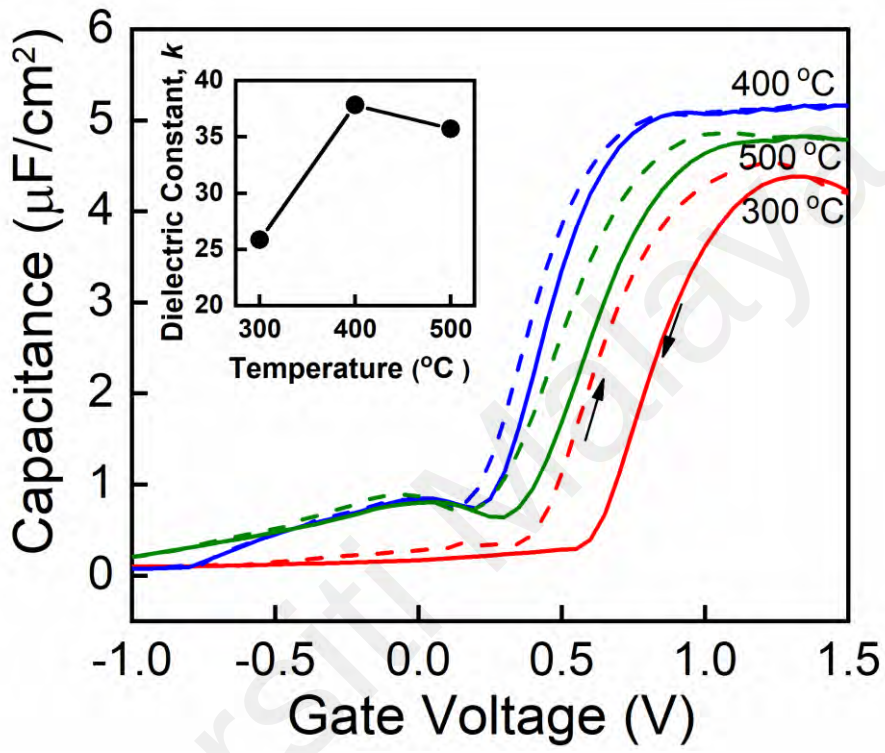

Figure 4.14: 100 kHz, *C–V* curve measured in forward and reverse bias condition for oxidized/nitrided Sm_2O_3/IL/gate stack at various temperatures (300 °C – 500°C). The inset is the effective dielectric constant of the investigated samples as a function of oxidation/nitridation temperatures.

In *C-V* plot, depletion region was found in positive bias side for all the investigated capacitors. This finding indicates that flatband voltage (V_{FB}) shifted positively, which confirms the presence of negative oxide charges or native defects in the gate stack (C. C. Cheng et al., 2007; J. Gao et al., 2017; Wong & Cheong, 2012c). Several reported literatures have demonstrated that oxygen vacancies generated by GeO desorption causes flatband voltage (V_{FB}) shift by generating additional negative charges (Cao et al., 2017; C. C. Cheng et al., 2007). It is clearly visible from Fig. 4.14 that, 400 °C sample shows

an obvious negative shift in compared to other investigated samples. This indicates generation of fewer negative oxide charges for 400 °C sample which might be due to alleviation of oxide defects or existence of singly or doubly negatively charged oxygen interstitial (J. Gao et al., 2017).

Hysteresis phenomenon has been n oticed in the *C-V* curve between the forward bias and reverse condition for all the investigated samples. The occurrence of hysteresis phenomena has been attributed to the presence of slow trapped charges located in the bulk oxide of gate dielectric or in the adjacent region between interfacial layer and high-*k* interface (Ke et al., 2018; Wong & Cheong, 2012c). Hence, it can be projected that induced hysteresis effect for Sm_2O_3/IL/Ge MOS capacitor is associated with the amount of defects/traps generated in the Sm_2O_3 gate insulator and at the Sm_2O_3/IL interface. Since slow trap density (*STD*) are related with hysteresis hence, *STD* has been approximated according to equation Eq. 4.11 (Wong & Cheong, 2012c).

$$\boldsymbol{STD} = \frac{\boldsymbol{\Delta V C_{ox}}}{\boldsymbol{qA}} \qquad \text{(Equation 4.11)}$$

Where, ΔV is the flatband voltage difference between hysteresis curve, A is the capacitor area and q is the electronic charge. Fig. 4.15 shows the relationship of slow trap density and hysteresis voltage calculated from the *C-V* curve with respect to different oxidation/nitridation temperature. The recorded hysteresis voltage shown in Fig. 4.15 indicates that 400 °C sample exhibits the lowest hysteresis voltage ~ 50 mV while the hysteresis voltage subsequently increases for 500 °C and 300 °C samples. Fig. 4.15 also reveals that 400 °C sample yielded the lowest *STD* ~ 1.62×10^{12} cm^{-2} while the *STD* increases subsequently for 500 °C and 300 °C sample. Hence, it is obvious that the reduction of slow trap density contributed to lowering the hysteresis effect for 400 °C sample. On the other hand, the increment of slow trap density enhanced the hysteresis effect for 300 °C and

500°C. It is worth noting that hysteresis voltage increases proportionally to the slow trap density. The increment of slow trap density can be attributed to the tunnelling of large amount carrier charge (electron or hole) from the Ge substrate into the interfacial layer or in bulk oxide (Ke et al., 2018). The *STD* value ~ 1.62×10^{12} cm^{-2} obtained for 400 °C sample in our work is comparatively lower than the *STD* value ~ 5.56×10^{12} cm^{-2} of Sm_2O_3/Si structure (Goh et al., 2017b). Furthermore, noticeable hump was observed for both 400 °C and 500 °C while a small kink appears for 300 °C in the inversion region. This phenomenon might be induced by the generation of slow interface states located in Sm_2O_3/IL or in bulk Sm_2O_3 interface due to N^+ atom out-diffusion during oxidation and nitridation process (Misra et al., 2006).

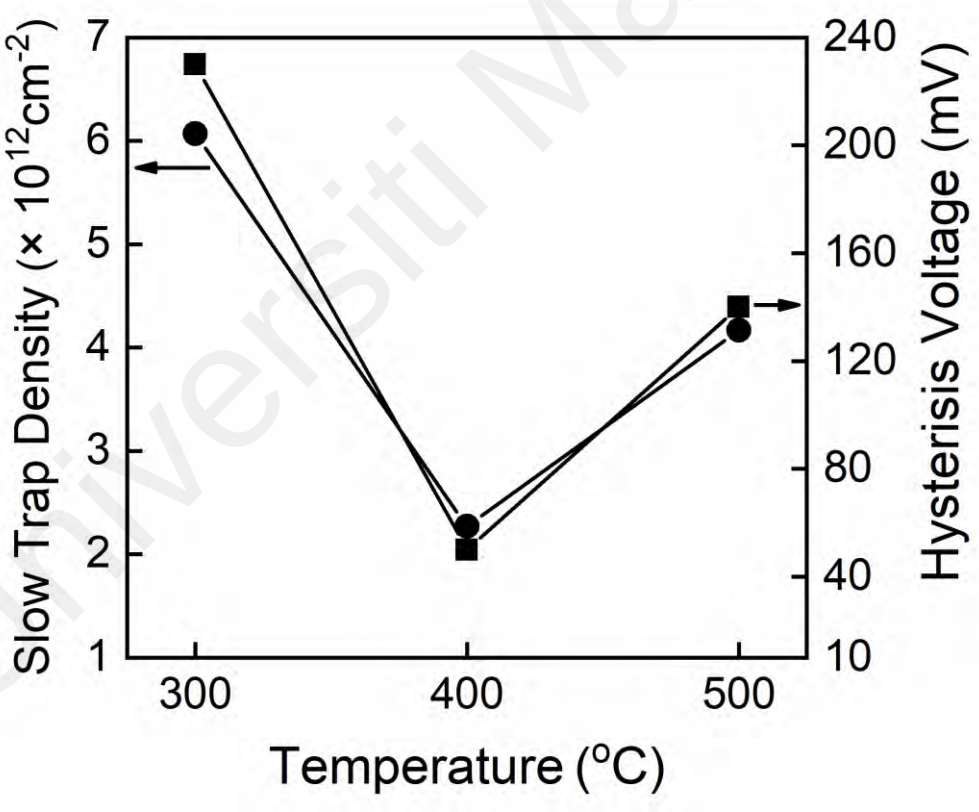

Figure 4.15: Slow trap density and hysteresis voltage as function for Sm_2O_3/IL/Ge gate stack at different oxidation/nitridation temperature (300 – 500) °C.

Fig. 4.16 shows the average interface trap density D_{it} as function of trap energy level (E_C – E) of for different oxidation-nitridation temperature from (300 – 500°C) °C. The average interface trap density D_{it} was approximated using Terman method ascribed in Eq. 4.12 (Schroder, 2015; Wong & Cheong, 2011b).

$$\boldsymbol{D_{it} = \frac{\Delta V_g C_{ox}}{\varphi_s q A}} \qquad \text{(Equation 4.12)}$$

Where, φ_s is the surface potential of substrate Ge at a specified gate voltage V_g and ΔV_g indicates the difference between ideal gate voltage and experimental gate voltage. The surface potential of a particular capacitance was obtained from the ideal MOS capacitor. The gate voltage was obtained from experimental *C–V* curve with same capacitance as that of φ_s . The steps were repeated until a relevant D_{it}versus ($E_c - E$) curve was obtained as shown in Fig. 4.16. The observation reveals that 400 °C sample yielded the lowest average interface trap density, D_{it} was approximated to be 4.76×10^{13} eV^{-1} cm^{-2}. Concerning the root of interface traps, it is believed that inclusion of Ge dangling bonds (DB) and the oxygen-defect (OD) are generally liable for the charge trapping procedure at the dielectric/Ge interface (Baldovino, Molle, & Fanciulli, 2008; Bethge et al., 2014). According to Fig. 4.16 it is evident that 400 °C sample exhibits fewer DB and OD density than 300 °C and 500°C. Since OD is primarily generated from GeO desorption and thus reduction of OD indicates the suppression of GeO desorption at 400 °C complementary with the XPS observation (Chroneos et al., 2012; Mitrovic et al., 2014). Meanwhile, the reduction of DB might be due to formation amorphous Ge_3N_4 and stoichiometric GeO_2 as observed in XRD and XPS analysis. The exclusion of DB can also be clarified from the valency passivation approach owing to beneficial trivalent characteristic of Sm^{3+}. In this approach Sm atom owing distinct valency than Ge would breach into oxygen deficient

GeO_2 and consequently displaces unbonded Ge atoms by forming interfacial Sm−O−Ge (C. C. Lin et al., 2014).

Comparing with the previous literature, the lowest $D_{it} \sim 4.76 \times 10^{13}$ eV^{-1} cm^{-2} achieved for 400 °C sample in this investigation is significantly higher than the post deposition annealed (PDA) Sm_2O_3/Ge interface $D_{it} \sim 5.1 \times 10^{11}$ eV^{-1} cm^{-2} and Sm_2O_3/Si interface $D_{it} \sim 3.8 \times 10^{12}$ eV^{-1} cm^{-2} as reported in (Chin & Cheong, 2011; C. C. Lin et al., 2014). However, $D_{it} \sim 10^{13}$ eV^{-1} cm^{-2} obtained in this investigation is relatively lower than the Sm_2O_3/Si interface $D_{it} \sim 10^{14}$ eV^{-1} cm^{-2} fabricated using sputtering process followed by thermal oxidation in O_2 ambient (Goh et al., 2017b).

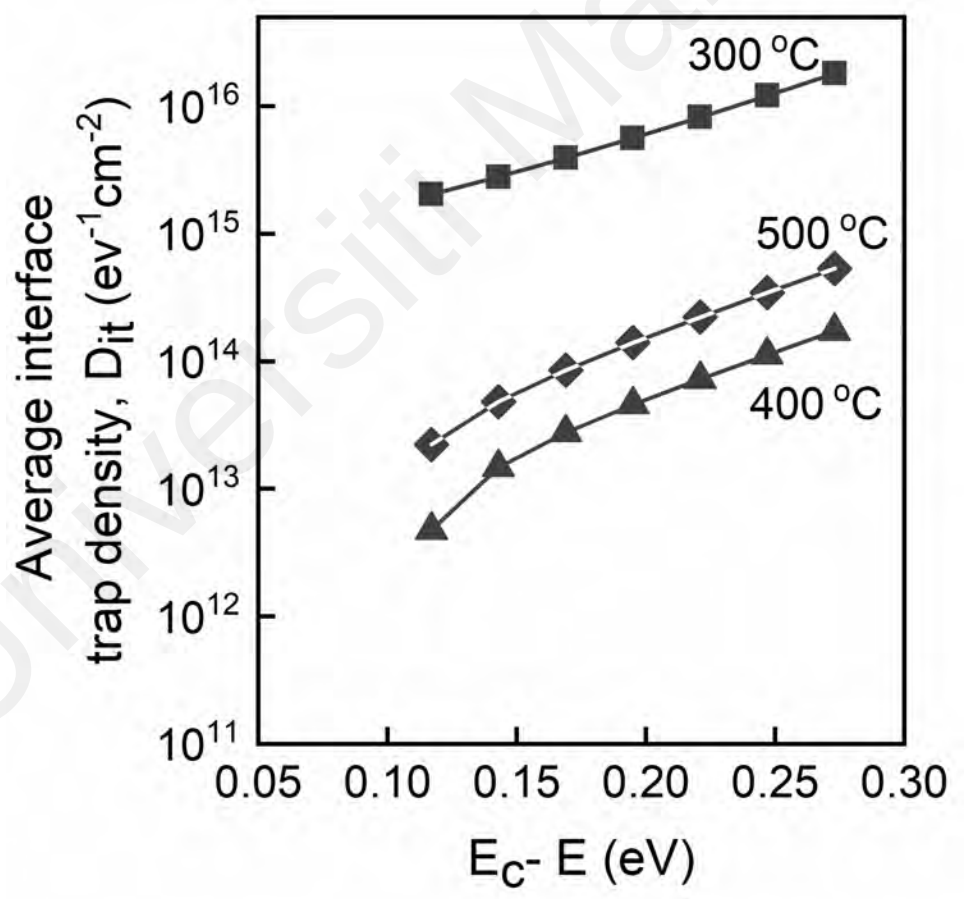

Figure 4.16: The average interface trap density D_{it} of Sm_2O_3/IL/Ge gate stack for different oxidation and nitridation temperature (300 – 500) °C.

The *C-V* measurement was also performed at various frequencies of 50 kHz, 100 kHz and 500 kHz to explore the accumulation and inversion trend for different oxidized/nitride sample at (300 − 500) °C. According to Fig. 4.17 frequency dispersion phenomenon is observed in both accumulation and inversion region for all the investigated sample. Strong frequency dispersion at accumulation region has been observed for 300 °C sample has been where the accumulation capacitance dropped abruptly at higher frequency of 500 kHz. Meanwhile, 400 °C sample revealed the least frequency dispersion. Kouda et al., (2012) reported that frequency dispersion phenomenon at the accumulation region is related to the frequency dependent changes of dielectric constant caused by the oxygen vacancies (Kouda et al., 2012). According to this notion, it can be ascribed that 300 °C oxidation/nitridation condition favours the generation of more oxygen vacancies due to GeO (g) desorption causing dispersive accumulation capacitance during the frequency dispersion. Hence, it can be suggested that more defective Sm_2O_3 film was generated at this oxidation/nitridation temperature. On the other hand, small frequency dispersion in the accumulation region for 400 °C sample indicates that Sm_2O_3 has gained structural uniformity due to reduction of oxygen vacancies, which is caused by the barrier role of interfacial Sm−O−Ge during the oxidation/nitridation process. Moreover, presence of interfacial traps triggers the variation in the weak inversion region during the frequency dispersion (Zhao et al., 2018). Accordingly, the lower interface trap density obtained for 400 °C sample contributed to generate small frequency dispersion in the inversion region than those of 300 °C and 500 °C sample. An anomalous hump/kink has been observed in the weak inversion region for all the investigated samples which is attributed to the presence of large interfacial trap densities.

Based on the findings of *C-V* measurement analysis it is obvious that, 400 °C is the optimum oxidation/nitridation condition for Sm_2O_3/Ge gate stack which enforces the alleviation of defect/traps in the bulk Sm_2O_3 and as well as in the Sm_2O_3/IL. Therefore, it can be suggested that 400 °C oxidation and nitridation temperature shows the best *C-V* characteristics.

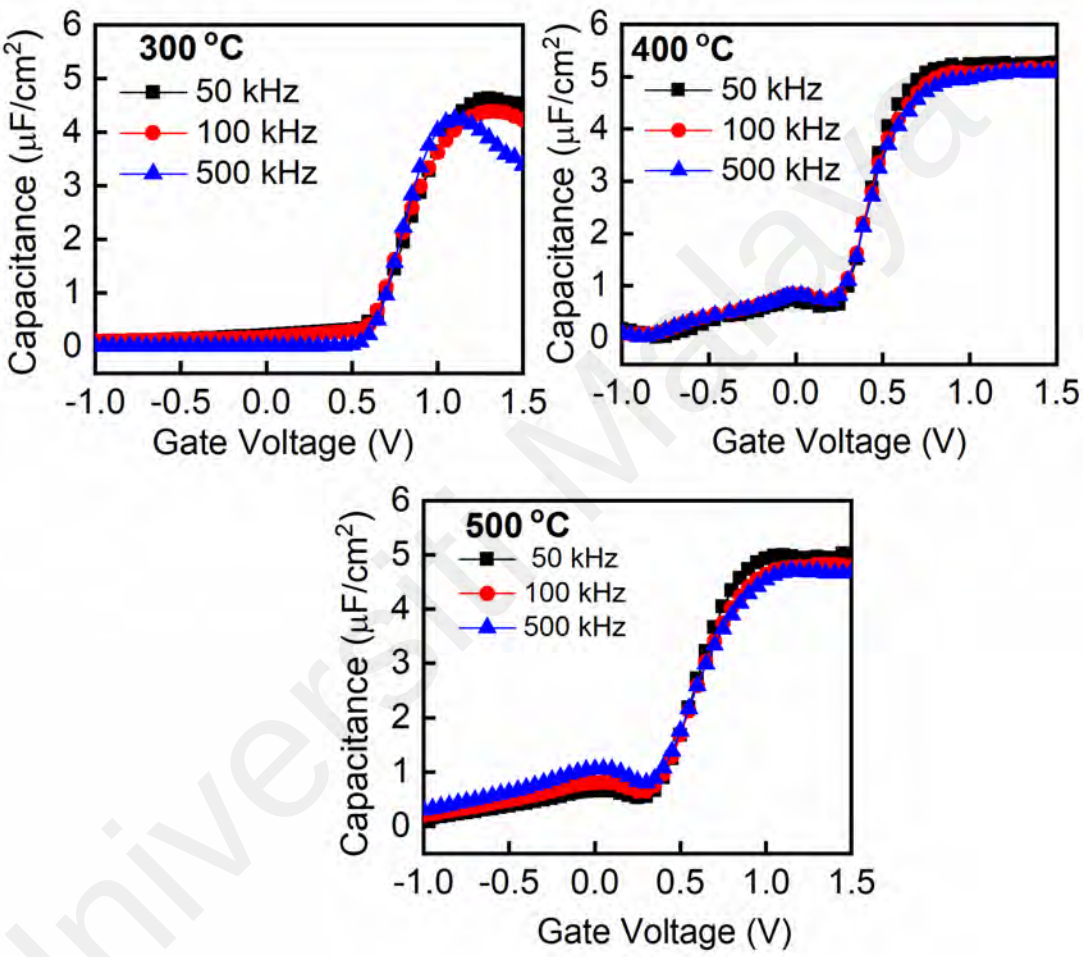

Figure 4.17: *C-V* characteristics measured at different frequencies of 50 kHz, 100 kHz and 500 kHz for Sm_2O_3/IL/Ge gate stack at various oxidation/nitridation temperature (300 – 500) °C.

4.3 Influence of Various Thermal Oxidation/nitridation Durations on Sputtered Sm/Ge in N_2O ambient.

4.3.1 XRD Analysis

Fig. 4.18 displays XRD pattern at a close-up 2θ range (10° – 60°) obtained for different thermal oxidation/nitridation durations (5 – 20) min in order to identify the crystal structure and crystallinity of the chemical compounds formed during oxidation/nitridation process. For all the investigated oxidation/nitridation durations three peaks were spotted at different 2θ angle of 27.16°, 47.28°, 48.26° and 54.04° corresponding to trigonal Sm_2O_3 (tri-Sm_2O_3) phase (100), (003), and (103). Besides, another weaker Tri-Sm_2O_3 peak at 48.26° with a plane orientation (110) was spotted for both 15 and 20 min excluding 5 and 10 min. Two additional blunt diffraction peaks were also found at 31.15° and 56.36° belonging to (101) and (200) planes, respectively for only 15 min. The trigonal phase of Sm_2O_3 fitted well with the ICSD reference code no. 647455. Among the tri-Sm_2O_3 peaks (003) plane is suggested to be the preferential plane orientation for all the samples. Furthermore, the tetragonal GeO_2 (tetra - GeO_2) diffraction peaks appeared at 29.15°, 42.69° and 57.17° revealing phase orientation (110), (111) and (211), respectively. Another GeO_2 peak of trigonal phase (tri-GeO_2) was noticed for all the samples at 39.22° which corresponds to (102) plane. Meanwhile one addition tri-GeO_2 was also identified at 19.36° which belongs to (100) for 5,10 and 20 min except 15 min. The preferential plane orientation for tetra-GeO_2 and tri-GeO_2 is suggested to be (110) and (102) planes, respectively. The ICSD reference code of 158,593 and 53870 ensures the formation of tetra-GeO_2 and tri-GeO_2, respectively. Two diffraction peaks of cubic Ge_3N_4 (c-Ge_3N_4) were found at diffraction angle 31.72° and 31.76° for 15 and 20 min with plane orientation (211) and (311), respectively. Because of amorphous phase no visible Ge_3N_4 peaks was exposed for 5 and 10 min. The (311) plane is recommended as the preferential plane orientation for c-Ge_3N_4. The peak of c-Ge_3N_4 was verified from ICSD reference

code no. 156338. Based on XRD diffraction patterns growth of Sm_2O_3 dielectric has been verified. Besides, the XRD patterns also suggested the growth of an interfacial layer (IL) due to detection of GeO_2 and Ge_3N_4 diffraction peaks. The presence of IL has been further verified in later section 4.3.2 and 4.3.3.

Figure 4.19 displays the intensity variation of preferential plane orientations of tri-Sm_2O_3 (003), tetra-GeO_2 (110) and tri-GeO_2 (102) to verify the impact of different oxidation/nitridation durations on the crystallinity of Sm_2O_3/IL. Regarding, Sm_2O_3 it is observed that the intensity increased gradually with the increase of oxidation durations. It is well known that the increase of intensity suggests the increment of crystallinity. Accordingly, the Sm_2O_3 compound is less crystalline for 5, 10 and 15 min since these durations induced the lower intensities. Meanwhile the most crystalline Sm_2O_3 structure is suggested for 20 min because the intensity of this duration increases substantially compared to other oxidation/nitridation durations. Both tetra-GeO_2 (110) and tri- GeO_2 (102) revealed similar intensity trend for all the samples. It is observed that, for GeO_2 phases the intensity increased to highest for 10 min while decreased subsequently for 5, 20, and 15 min. Consequently, GeO_2 becomes less crystalline at 15 min while the 10 min caused the most crystalline GeO_2 structure. On the basis of above consequences, it is predicted that 15 min oxidation/nitridation duration formed more amorphous interfaces since both Sm_2O_3 and GeO_2 is less crystalline at these durations.

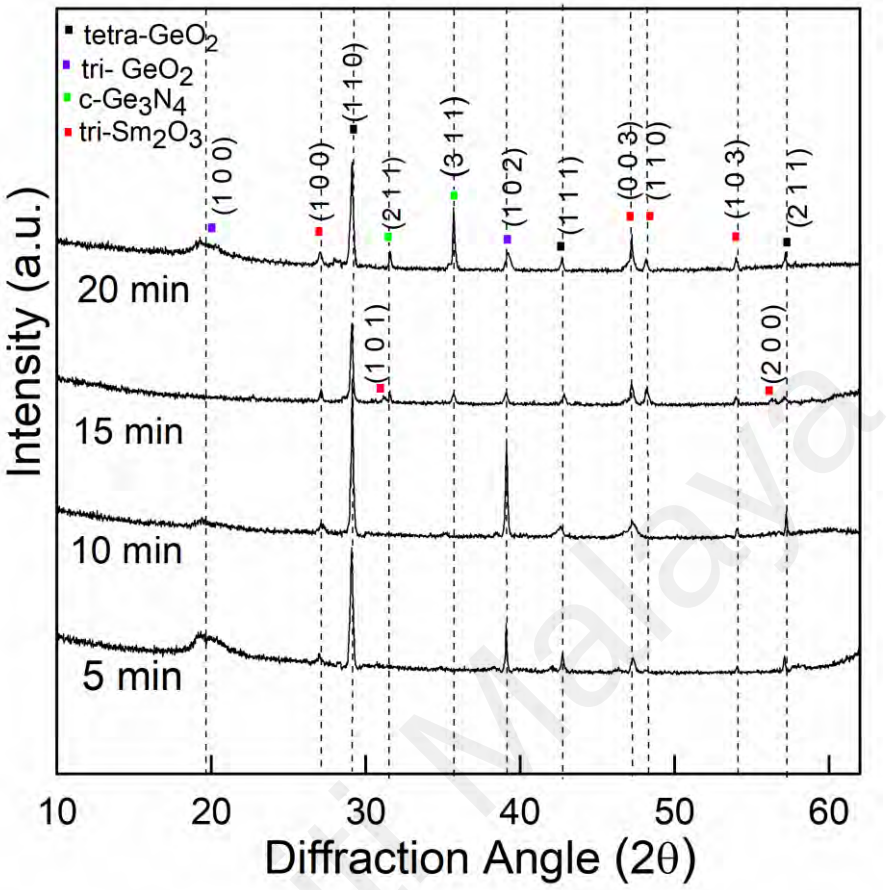

Figure 4.18: XRD diffraction patterns for sputtered Sm/Ge film thermally oxidized/nitrided at several durations (5 – 20) min.

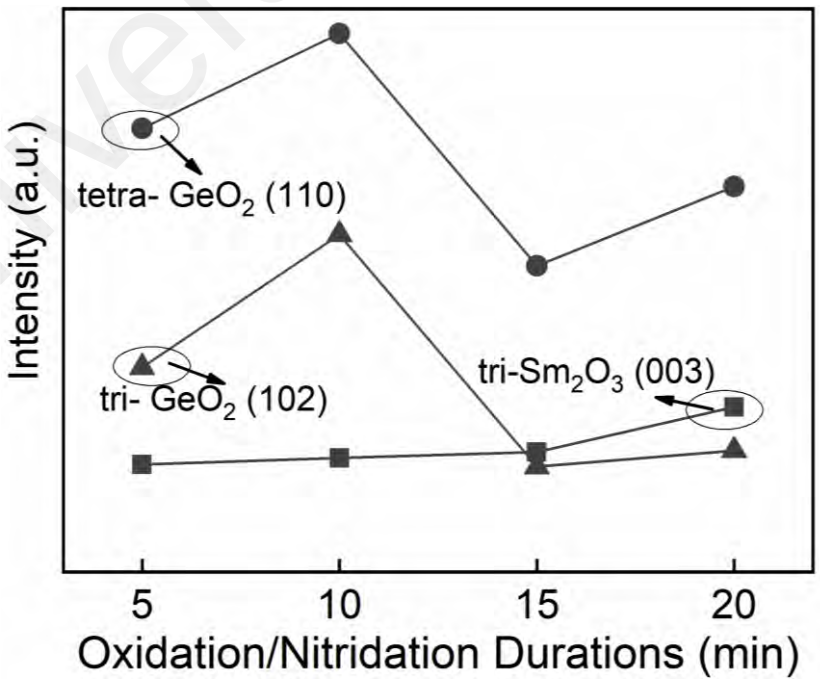

Figure 4.19: Intensity trend of preferential plane orientations of tri-Sm_2O_3 (003), tetra-GeO_2 (110) and tri- GeO_2 (102) as function of thermal oxidation/nitridation durations (5 – 20) min.

4.3.2 Raman Analysis

Fig. 4.20 illustrates the findings of Raman spectrums for different thermal oxidation/nitridation durations (5 – 20) min. The peak appeared at 300.95 cm^{-1} (Batra, Kabiraj, & Kanjilal, 2007; Lei et al., 2018) is denoted as Substrate Ge for all the investigated oxidized/nitrided samples. Three peaks corresponded to Sm_2O_3 was spotted at 162.41 cm^{-1} (Jiang, Liu, Lin, Li, & Li, 2013; Mandal, Sarkar, Deb, & Chakrabarti, 2014), 177.62 cm^{-1} (Jiang et al., 2013), 411.20 cm^{-1} (Hongo, Kondo, Nakamura, & Atou, 2007; Mandal et al., 2014). Meanwhile, the peaks of GeO_2 were identified at 221.72 cm^{-1} (Lignie, Hermet, Fraysse, & Armand, 2015), 517.32 cm^{-1} (Kartopu et al., 2003) for all the samples while the GeO_2 peaks at 445.44 cm^{-1} (Kartopu et al., 2003) was detected for 5,10 and 20 min except 15 min. A single peak corresponding to Ge_3N_4 was identified at 459.44 cm^{-1} (Deb, Dong, Hubert, McMillan, & Sankey, 2000; Lei et al., 2018) for all the investigated oxidation/nitridation durations. However, an additional unknown peak was detected at 353.12 cm^{-1} for extended durations of 15 and 20 min. Since this peak neither corresponds to Sm_2O_3, GeO_2, or Ge_3N_4 and so it is inferred as interfacial $Sm_xGe_yO_z$ following the XPS spectrums of later section 4.3.3 where existence of $Sm_xGe_yO_z$ was found at 15 and 20 min. Although, Sm-O-Ge peaks was not found in XRD patterns which is predicted due to its amorphous crystal structure. The inset image of Fig. 4.20 shows the intensity of Sm_2O_3, GeO_2 and Ge_3N_4 at 177.62 cm^{-1} 517.32 cm^{-1} and 445.44 cm^{-1}, respectively. It is noticed that Sm_2O_3 and Ge_3N_4 increases at extended durations 15 and 20 min where the highest intensity of these compounds was produced at 15 min' oxidation/nitridation duration. Meanwhile, the generation of GeO_2 soaring higher at shorter durations of 5 and 10 min and reduced at elevated durations of 15 and 20 min where 10 min induced the highest intensity of GeO_2. The observation of RAMAN spectrums is complementary with the findings of XPS and XRD.

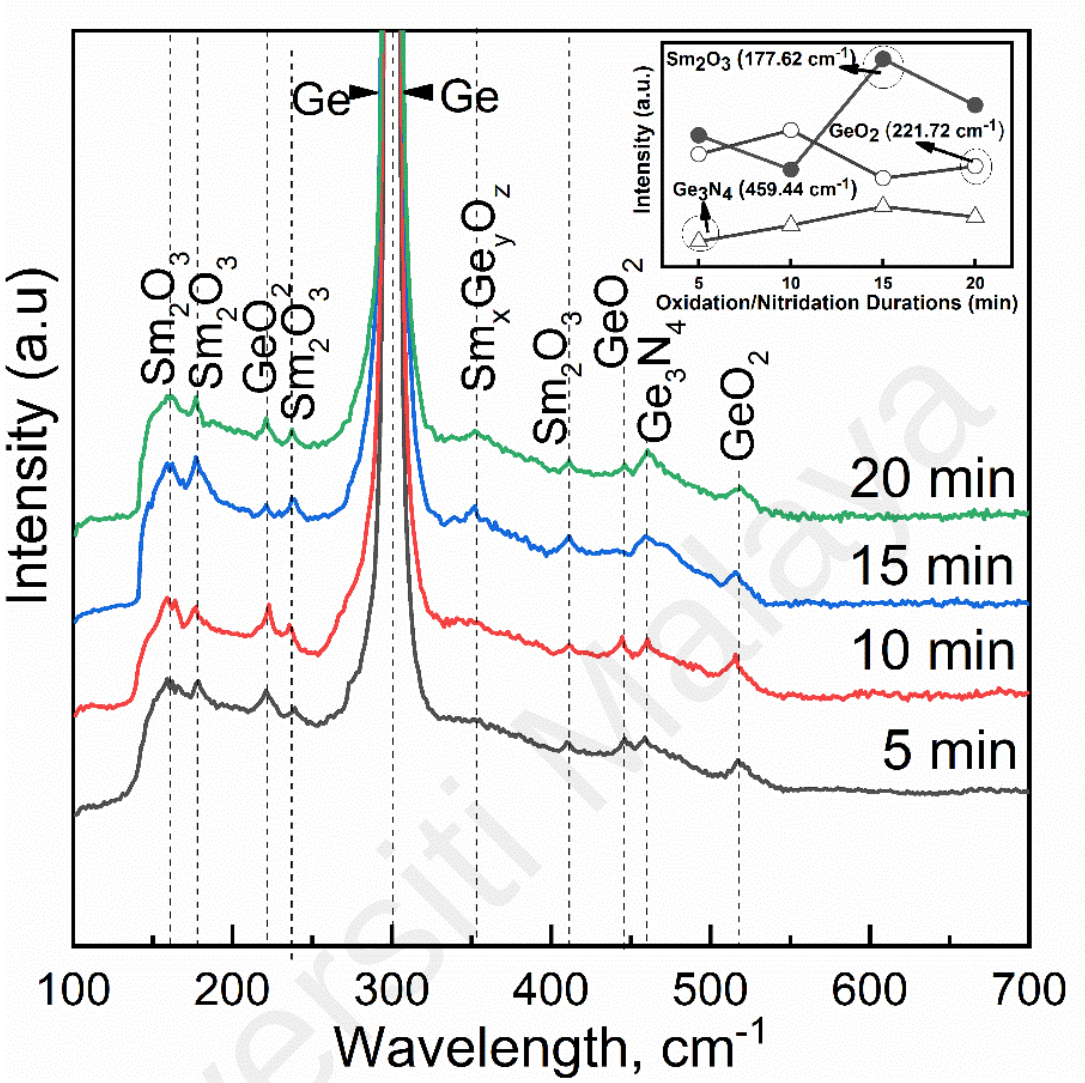

Figure 4.20: Raman Spectrums for sputtered Sm/Ge film thermally oxidized and nitrided under different oxidation/nitridation durations (5 – 20) min.

4.3.3 XPS Analysis

The evolution of core level narrow scan spectra of Sm 3d, Ge 3d and O1s at different thermal oxidation/nitridation durations 5, 10, 15 and 20 min were conducted to investigate the chemical bonding states configurations of Sm_2O_3/Ge stack. The narrow scan spectrums are shown in Fig. 4.21, 4.22 and 4.23.

Fig. 4.21 illustrates the variation of Sm 3d spectra at different oxidation/nitridation durations (5 − 20) min. From Fig. 4.21 it is apparent that, the line position of Sm 3d centroid peaks for 5 and 10 min oxidation/nitridation shifted negatively by 0.28 eV and 0.32 eV in the direction of low binding energy (B.E) with respect to reported Sm_2O_3 reference B.E of Sm 3d = 1084.0 eV (C. C. Lin et al., 2014). Primarily, the negative shift of Sm 3d spectra along low B.E implies that, the interfacial layer is deficient of Sm-O-Ge content during shorter oxidation/nitridation durations of 5 and 10 min. Conversely, when the oxidation/nitridation durations is extended to 15 and 20 min the reference line position of Sm 3d centroid peaks shifted positively by 0.23 eV and 0.18 eV in the direction of higher (B.E). This outcome clearly implies the creation of Sm−O−Ge content close to the dielectric interface within the interfacial region during the extended oxidation/nitridation of 15 and 20 min. The generation of interfacial Sm−O−Ge compound for these durations can be attributed due to partial exclusion of (Sm−O−Sm) sub-oxide configuration. Since Sm atoms are less electronegative than Ge hence, the catalytic oxidation of Ge atoms substituted Sm atoms by penetrating into Sm_2O_3 causing spontaneous growth of Sm−O−Ge content near the dielectric interface at elevated oxidation/nitridation durations (C. C. Lin et al., 2014). Regarding the Sm−O−Ge content deficiency for 5 and 10 min it is presumed that, due to shorter oxidation/nitridation time the activation energy of Ge atoms from GeO_2 network or substrate Ge was inadequate to initiate the catalytic oxidation of Ge atoms with Sm_2O_3 interface. Consequently, creation of Sm−O−Ge compound was prevented.

Fig. 4.21 also illustrates the deconvoluted compounds of Sm 3d peaks in order to inspect the influence of different oxidation/nitridation durations on thermodynamic stability and evolution of Sm_2O_3 dielectric interface. Typically, the peak corresponding to Sm_2O_3 appears at lower B.E of 1083.90 eV while Sm−O−Ge peaks were found at relatively higher B.E of 1086.02 eV (C. C. Lin et al., 2014). Accordingly, a single peak

corresponding at lower B.E of 1083.76 eV and 1083.63 eV appeared for 5 and 10 min, respectively is assigned as Sm_2O_3. On the other hand, the 15 and 20 min composed two peaks where the former peaks represented as Sm_2O_3 which emerged at lower B.E region of 1083.93 eV and 1083.81 eV, respectively. Meanwhile the latter peak was designated for Sm−O−Ge which appeared at higher B.E of 1085.23 eV and 1085.19 eV for 15 and 20 min samples, respectively. Comparing all the investigated durations, the peak corresponding to Sm−O−Sm exhibited the highest integrated area at 15 min followed by 20 and 5 min while the lowest integrated area of Sm−O−Sm was observed for 10 min oxidation/nitridation. This observation suggested that 10 min oxidation/nitridation condition accelerates more pronounced out-diffusion of O atoms from dielectric interface itself forming thermally unstable sub-stochiometric Sm_2O_3 film. Contrariwise, 15 min oxidation/nitridation is more convenient to inhibit the out-diffusion of O atoms which stimulated more stochiometric Sm_2O_3 film. In addition, creation of Sm−O−Ge interlayer with relatively higher B.E also contributed to the stabilization of Sm_2O_3 film for this duration. Although, both 15 and 20 min generated Sm−O−Ge interlayer but 15 min revealed better stoichiometry of Sm_2O_3 which can be attributed to the uniform in-diffusion of Ge atoms into Sm_2O_3 dielectric layer causing balanced elimination of (Sm−O−Sm) sub-oxide during Sm−O−Ge formation.

Thus, the findings of Sm 3d suggests that, merely Sm_2O_3 was generated during 5 and 10 min while co-existence of Sm_2O_3 dielectric film and interfacial Sm−O−Ge content were evident when oxidation/nitridation durations elevated to 15 and 20 min. Furthermore, 15 min oxidation/nitridation induced more stochiometric Sm_2O_3 dielectric interface and relatively stable Sm−O−Ge interfacial compound. The formation of Sm_2O_3 can be governed by the Eq. 4.13 and Eq.14 where sputtered Sm^+ reacted with the atmospheric N_2O for all the investigated samples to produce Sm_2O_3 dielectric interface on the uppermost surface. Meanwhile, the generation of spontaneous Sm−O−Ge content across

the interfacial layer for 15 and 20 min took place according to the vigorous chemical reaction of Eq. 4.14 by the penetration of Ge atoms into Sm_2O_3 interface.

$$Sm^+ + N_2O \rightarrow SmO^+ + N_2 \quad \text{(Equation 4.13)}$$

$$SmO^+ + N_2O \rightarrow Sm_2O_3 + N_2 \quad \text{(Equation 4.14)}$$

$$Sm_2O_3 + Ge \rightarrow SmGeO_x \quad \text{(Equation 4.15)}$$

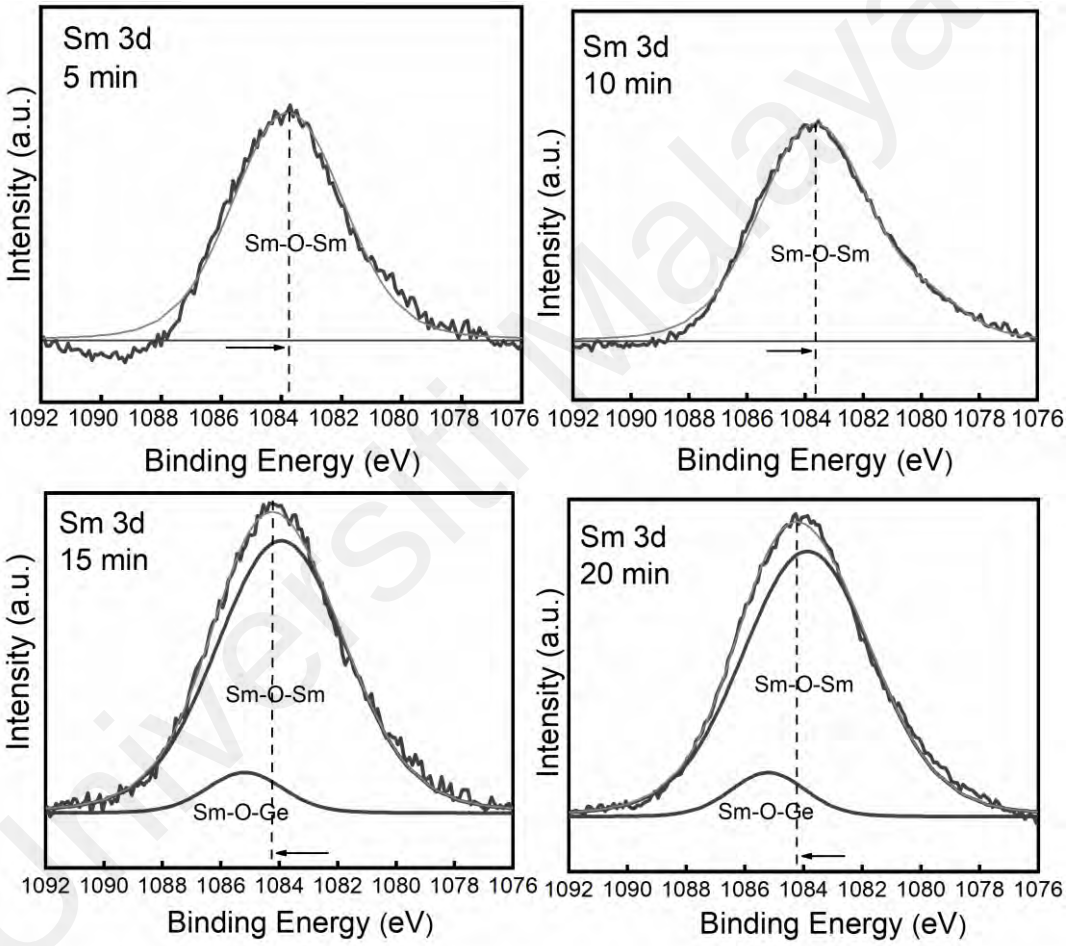

Figure 4.21: Deconvoluted narrow scan spectrums of Sm 3d at different oxidation and nitridation durations (5 – 20) min for Sm_2O_3/Ge stack.

Fig. 4.22 signifies the evolution of several interfacial compounds obtained from Ge 3d spectrums at various oxidation/nitridation durations (5 – 20) min. According to Fig. 4.22, a single peak composing mixture of various interfacial compounds have been deconvoluted with reference to elemental substrate Ge^0 at 29.6 eV (Mitrovic et al., 2014). The interfacial chemical bonding states were deconvoluted into three Ge suboxides (GeO_x) of Ge^{1+} (Ge_2O), Ge^{2+} (GeO), Ge^{3+} (Ge_2O_3) , and a native oxide Ge^{4+} (GeO_2) at B.E shift of +0.8 eV, +1.8 eV, +2.8 eV and > +3 eV, respectively (J. Song et al., 2009). Another additional interfacial chemical bonding state of Ge* fitted well for 15 and 20 min at B.E shift of +2.4 eV. It has been reported that, rare earth germanate typically appears between +1.7 to +2.8 eV owing to nearest neighbour effect which shows distinct difference with respect to GeO_2 of > +3eV shift (Mitrovic et al., 2014). Hence, the Ge* content found between Ge^{2+} and Ge^{3+} is designated as Sm−O−Ge. However, no such Sm−O−Ge peak was found for 5 and 10 min samples which is consistent with the Sm 3d spectrums.

According to Fig. 4.22, the content of Ge^{1+} (Ge_2O) and the native oxide Ge^{4+} (GeO_2) was formed for all the investigated samples. Meanwhile, Ge^{3+} (Ge_2O_3) was exposed for 5,10 and 20 min samples excluding 15 min. However, it is noteworthy that desorption of volatile GeO compound appeared for 5 and 10 min samples while GeO was deficient during oxidation/nitridation of 15 and 20 min samples. The above findings imply an amorphous IL structure beneath the Sm_2O_3 dielectric layer involving Ge_2O, GeO, Sm−O−Ge, Ge_2O_3, and GeO_2 contents. However, the growth of these IL compounds shows variance in densities for different oxidation/nitridation durations which effected the thermal stability of Sm_2O_3/Ge stack. From Fig 4.22, it is also observed that the growth of sub-stoichiometric unstable Ge suboxides (GeO_x) compounds is greater for 10 min followed by 5 min sample. On the contrary, the growth of suboxides (GeO_x) shrinks at 20 min and the lowest integrated area was recorded at 15 min sample. Furthermore, in several literatures it has been asserted that among all the Ge oxides excessive growth of native

GeO_2 (Ge^{4+}) and GeO (Ge^{1+}) compounds would cause an abrupt thermodynamic instability and degradation of Ge based MOS devices (Juan. Gao et al., 2017; D. Wang, He, Fang, et al., 2019). Since, lowering of GeO_2 (Ge^{4+}) and the deficiency of GeO (Ge^{2+}) was observed for 15 and 20 min accordingly, these durations expose more thermally stable IL interface than those of 5 and 10 min sample. The reason of better thermal stability for 15 and 20 min durations is due to the evolution of Sm−O−Ge content which suppressed the desorption of volatile GeO and compressed the GeO_x and GeO_2 content for these samples. Regarding the GeO suppression mechanism, it is predicted that formerly an oxygen deficient $SmGeO_x$ were generated which trapped the out-diffusing GeO species and as final product densified $Sm_xGe_yO_z$ was produced by preserving oxygen loss (C. H. Lee et al., 2011; H. Wang et al., 2012). Amongst all the samples 10 min duration prevailed the highest integrated area of GeO_2 (Ge^{4+}) and GeO (Ge^{2+}) species suggesting the most thermally unstable interfacial interface. The increase of GeO_2 (Ge^{4+}) and GeO (Ge^{1+}) might be associated with the interdiffusion and re-arrangement mechanism of oxygen substances and unsaturated Ge atoms during thermal oxidation/nitridation and cooling process. Hence, 10 min oxidation/nitridation condition would decline the electrical features of the Sm_2O_3/Ge stack. Now, comparing 15 and 20 min samples, Ge_2O (Ge^{1+}) and Ge_2O_3 (Ge^{3+}) content decreases while a slight increase in Sm−O−Ge content is observed for 15 min sample. This finding suggests that 15 min oxidation/nitridation increases the activation energy of Ge promoting out-diffusion of Ge atoms to generate denser Sm−O−Ge which controlled the distribution of oxygen substances in such way so that GeO_x growth was minimized. Furthermore, intense GeO_2 (Ge^{4+}) peak is noticeable at this duration alike other samples, but the peak shifted toward higher B.E while the density slightly dropped. This outcome suggests that GeO_2 (Ge^{4+}) became more stochiometric when the oxidation/nitridation duration reached 15 min. The formation of stochiometric GeO_2 can also be attributed to the initial oxygen deficient $SmGeO_x$ which later regulated the propensity

of O and Sm distribution to retain the integrity of interfacial native GeO_2. Thus, among all the oxidized/nitrided samples 15 min duration is more suitable condition to achieve thermodynamically stable interfacial layer with less sub-stochiometric Ge sub oxides defects and more stochiometric GeO_2.

In summary, based on Ge 3d spectra the interfacial oxidation/nitridation mechanism of forming interfacial oxides such as GeO_x, GeO_2 and desorption process of GeO can be expressed by the following hypothetical chemical reaction. It should be noted that, the interfacial reactions of Eq. 4.16 and Eq.17 occurs for all the samples while Eq 4.18 takes place for 5, 10, and 20 min oxidation/nitridation. The desorption process of volatile GeO has been hindered for the 15 and 20 min following Eq. 4.19.

$$Ge + 2N_2O \rightarrow GeO_2 + 2N_2 \quad \text{(Equation 4.16)}$$

$$3GeO_2 + 3Ge \rightarrow 6GeO \quad \text{(Equation 4.17)}$$

$$4Ge + 2O_2 \rightarrow Ge_2O + Ge_2O_3 \quad \text{(Equation 4.18)}$$

$$SmGeO_x + GeO \rightarrow Sm_xGe_yO_z + GeO_x \quad \text{(Equation 4.19)}$$

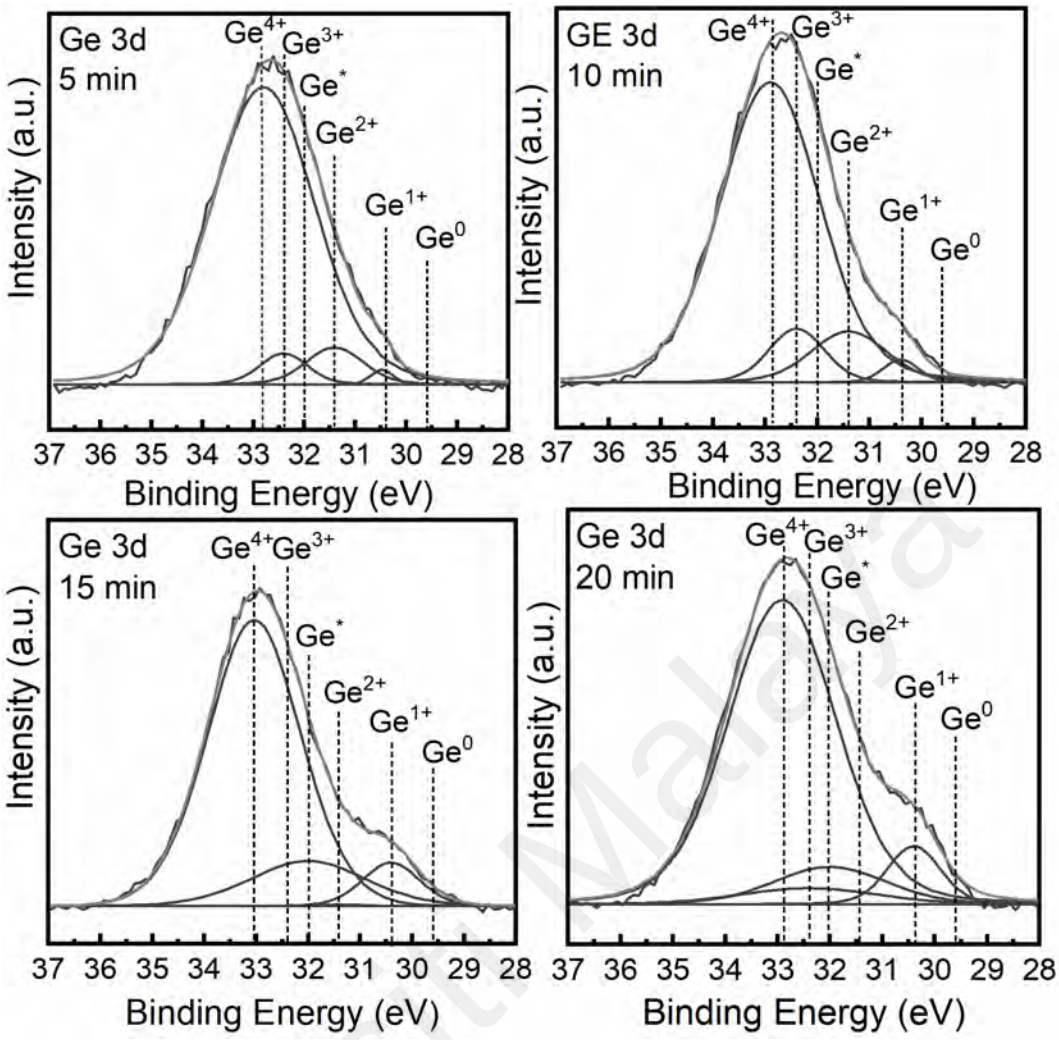

Figure 4.22: Deconvoluted Ge 3d narrow scan spectrums of oxidized/nitrided sputtered Sm/Ge for different oxidation/nitridation durations (5 – 20) min.

Fig. 4.23 depicts the evolution of O1s spectra as function of several oxidation/nitridation durations (5 – 20) min. The O1s spectra shows that all the investigated samples can be deconvoluted into two common peaks at 530.40 eV and 532.0 eV while an extra peak at 531.80 eV was found for 15 and 20 min samples. The peaks at 530.40 eV, 531.80 eV and 532.00 eV have been allocated for Sm−O−Sm, Sm−O−Ge and Ge−O, respectively (Pan & Huang, 2010; D. Wang, He, Fang, et al., 2019). From O1s spectrum it is apparent that, the oxygen content within the Sm−O−Sm configuration enhanced largely at 15 min oxidation/nitridation followed by 20 and 5 min while substantial decrease is noticed for 10 min. This observation is supportive with the Sm 3d spectra, which again

confirms that 15 min oxidation/nitridation condition significantly promotes the growth of stochiometric Sm_2O_3 while 10 min condition is less suitable to form stochiometric Sm_2O_3 interface. Considering, the Ge−O content an opposite growth phenomenon was spotted where the Ge−O species showed the largest expansion for 10 min followed by 5 min sample. Since the O1s peak corresponding to Sm−O−Sm content lessened and Ge−O content increased for 5 and 10 min, hence it is obvious that the disproportionate out-diffusion of O atoms from Sm_2O_3 network contributed to enhance Ge−O species for these samples. As a result, the IL region grown beneath the Sm_2O_3 film is densified by unstable GeO_x and GeO_2 for 5 and 10 min oxidation/nitridation which is complementary with Ge 3d spectra. Meanwhile, O1s corresponding to Ge−O species decreased subsequently for 20 and 15 min which signifies the reduction of GeO_x and GeO_2. The lowest Ge−O content for 15 min in O1s spectra suggests that among all samples the smallest amount of oxygen atoms diffused from Sm_2O_3 itself at this duration. Thus, based on both O1s and Ge 3d spectra it is obvious that 10 min is more convenient for growing Ge−O compounds while 15 min oxidation/nitridation impedes the growth the Ge−O contents. In addition, the Sm−O−Ge content found in O1s spectra also follows identical growth phenomena observed in Sm 3d and Ge 3d spectra where this content maximized at 15 min oxidation/nitridation condition.

The extent of oxidation/nitridation level was estimated by plotting the B.E of Sm_2O_3 extracted from Sm 3d spectrums as function of various oxidation/nitridation durations 5, 10, 15 and 20 min displayed in Fig. 4.24. According to Fig. 4.24 the B.E for shorter oxidation/nitridation of 5 and 10 min and the longest oxidation/nitridation of 20 min emerged below the baseline of full oxidation level indicating under-oxidized condition. Since, 10 min sample is distributed in the lowest distance below full oxidation level hence, structural quality of Sm_2O_3 at this duration will be most defective due to deep

under-condition which adversely effects the electrical properties. Among all the investigated samples the longer oxidation/nitridation duration of 15 min emerged near the full-oxidation baseline.

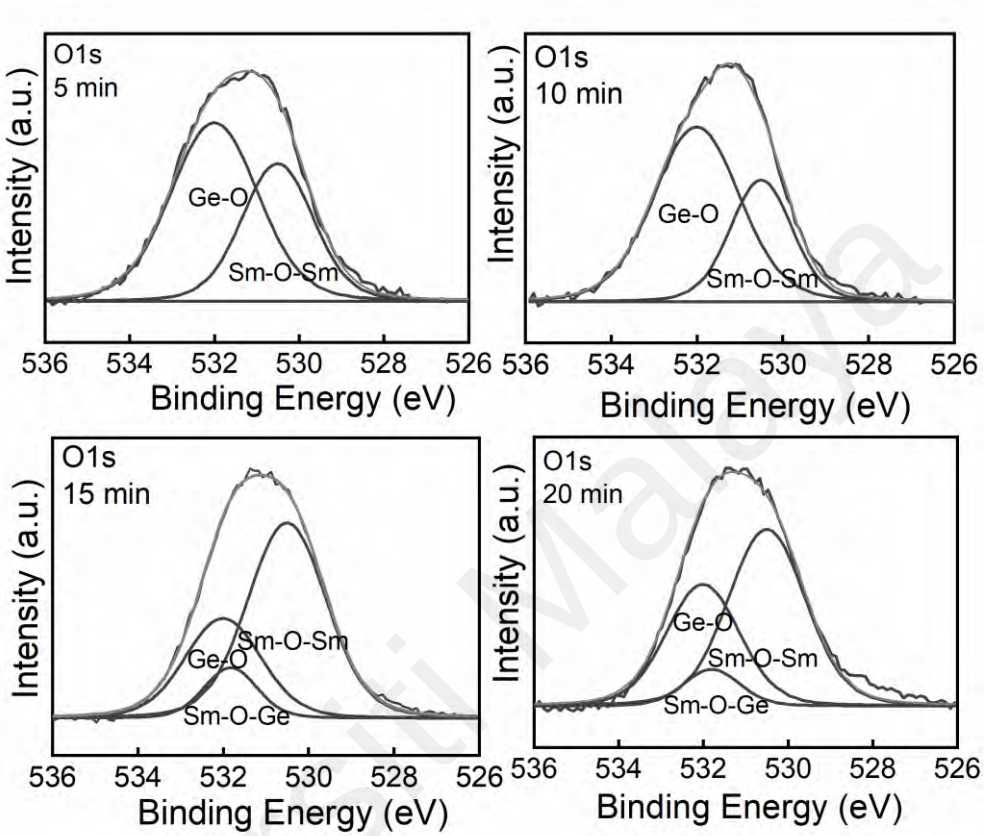

Figure 4.23: Deconvoluted core level narrow scan spectrums of O1s for different oxidation/nitridation durations (5 – 20) min.

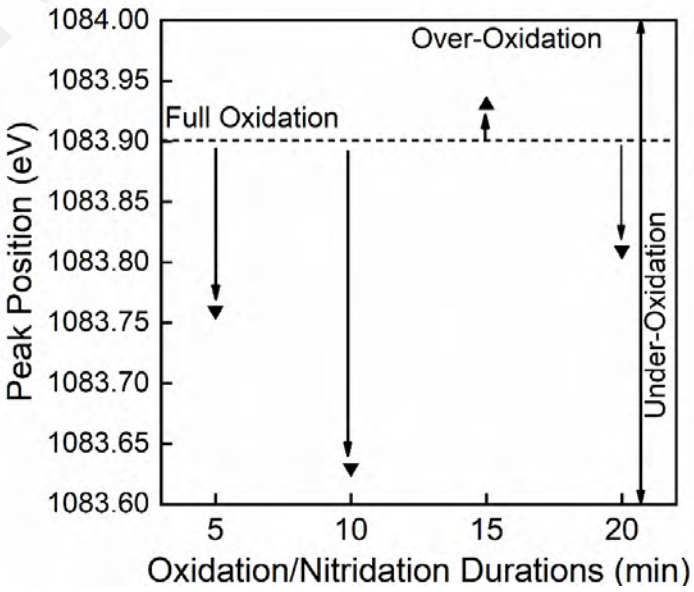

Figure 4.24: Degree of oxidation/nitridation level as function of different durations.

4.3.4 Band Alignment

The band offset value of high-*k* oxide between substrate material is one of the critical issues in utilization of high-*k* material for MOS devices. The band offset value of high-*k* oxide should be minimum 1eV with respect to semiconductor substrate material (Goley & Hudait, 2014; Robertson & Wallace, 2015). Hence, the band alignment of Sm_2O_3/IL/Ge for various oxidation/nitridation has been determined from O1s plasmon loss XPS and valance band, (VB) spectra as described earlier in section 4.2.4. Accordingly, the valance band offsets (VBO), ΔE_v of (Sm_2O_3 + IL) and conduction band offset (CBO), ΔE_c (Sm_2O_3+IL) on substrate Ge are evaluated following Eq. 4.1 and Eq. 4.2, respectively. The valance band edge, E_v (Sm_2O_3 + IL) has been measured by an extrapolation of leading negative slope edge of VB spectrums towards the horizontal baseline of substrate Ge baseline as represented in Fig. 4.25a. The intercept tip is considered as E_v (Sm_2O_3 + IL) which was measured 2.94 eV, 2.72 eV, 3.08 eV and 3.04 eV for oxidation/nitridation durations of 5, 10, 15 and 20 min, respectively. According to Eq. 4.1. VBO, ΔE_v (Sm_2O_3 + IL) with respect to substrate Ge for 5, 10, 15 and 20 min oxidation/nitridation durations are 1.90 eV, 1.82 eV, 2.60 eV and 2.43 eV, respectively.

The energy bandgaps, E_g measured using O1s plasmon loss spectrums obtained from respective XPS survey scan of 5, 10, 15 and 20 min are 5.41 eV, 5.11 eV, 6.35 eV and 6.02 eV, respectively as depicted in Fig. 4.25b. Meanwhile, Fig 4.26 presents the combined band alignment mapping at different oxidation/nitridation durations for Sm_2O_3/IL/Ge stack durations. The CBO, ΔE_c (Sm_2O_3 + IL) measured on the substrate Ge for thermally oxidized/nitrided samples of 5,10,15 and 20 min are 1.90 eV, 1.82 eV, 2.60 eV and 2.43 eV, respectively as in Fig. 4.26. In response to the mapping of band alignment it is apparent that 15 min induced the biggest ΔE_c and ΔE_v followed by 20 and 5 min while decreased to the smallest at 10 min. For high-*k* based MOS devices increment

of CBO, ΔE_c and VBO, ΔE_v is considered as an essential aspect which regulates reduction of gate leakage current density (J. Gao et al., 2017). The band offset mapping also indicates 5 min induced more asymmetrical mapping while 15 min induced near-symmetrical mapping among all the samples. The asymmetrical mapping between ΔE_c and ΔE_v would also contribute to increase the gate leakage current (He, Gao, et al., 2014). Therefore, for 15 min the enhanced ΔE_c and ΔE_v with near-symmetrical mapping would contribute to improve the *J-E* features. Meanwhile, the decreased ΔE_c and $\Delta E_v$of 10 min and asymmetrical band offset mapping of 5 min would be a concerning factor in deteriorating device performance. The increase of ΔE_c and ΔE_v with near-symmetrical band alignment for 15 min is related to better interfacial interface caused by the reduction of GeO_x structural defects and other oxygen associated defects observed in XPS analysis. On the contrary, for 5, 10 and 20 min the decrease of ΔE_c and ΔE_v is associated with higher densities defect gap states generated inside the bandgap of Sm_2O_3/IL through volatilization of GeO (g) and diffusion of interfacial GeO_x defects. Due to reduction of $\Delta E_c$and ΔE_v the bandgap of 5, 10 and 20 min dropped by 0.84 eV, 1.14 eV and 0.23 eV, respectively. Since 10 min generated the smallest ΔE_c and ΔE_v causing the lowest bandgap. Furthermore, for all the investigated samples it is noticeable that both $\Delta E_c$and ΔE_v is larger than 1 eV which signifies the eligibility of Sm_2O_3/IL/Ge structure to be a potential contender for high-*k* based MOS devices.

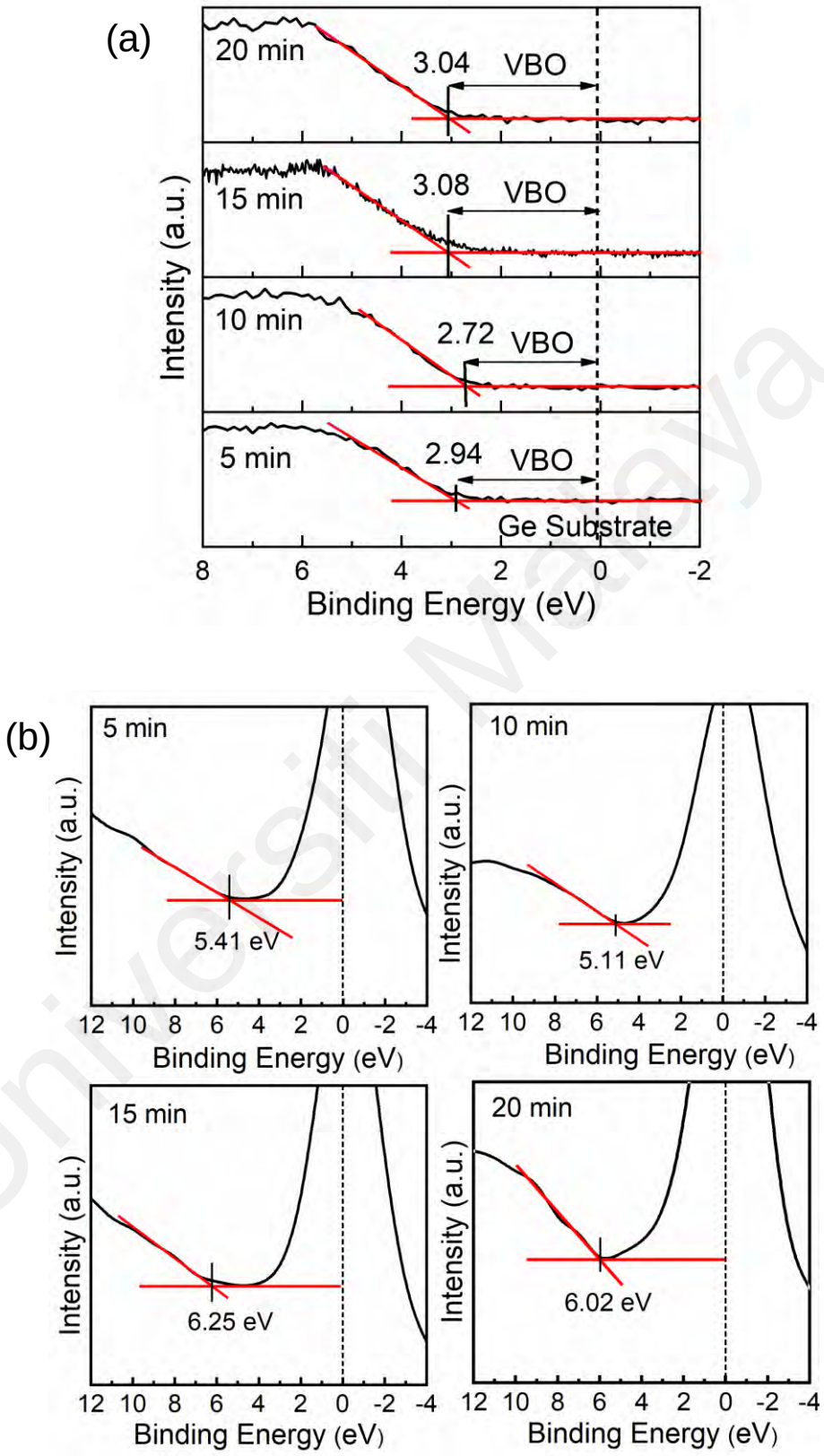

Figure 4.25: Estimation of valance band offset (ΔE_v) and energy bandgap (E_g) for Sm_2O_3/IL/Ge structure at various oxidation/nitridation durations (5 – 20) min (a) Valance band edge, E_v and VBO extraction from XPS valence band spectra. (b) Energy band gap deduction from oxygen plasmon loss XPS spectra.

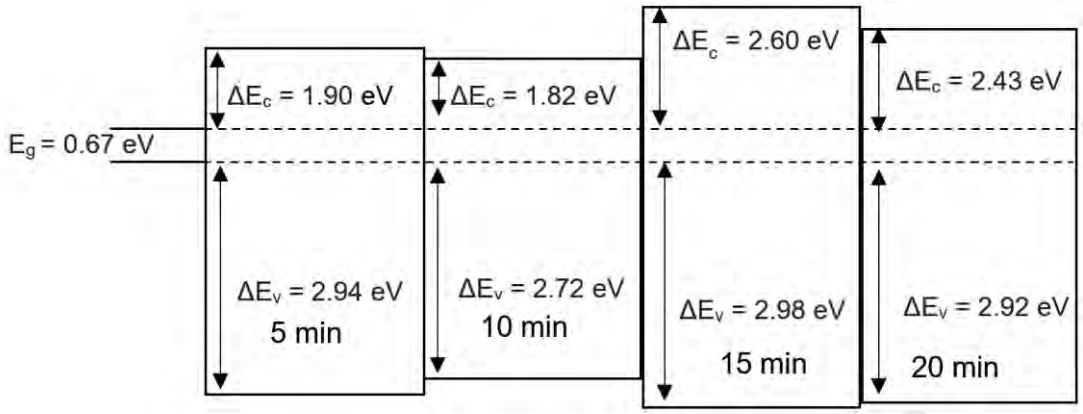

Figure 4.26: Band Alignment mapping of (Sm_2O_3 + IL) with respect to Ge substrate for various oxidation/nitridation durations (5 −20) min.

4.3.5 HRTEM Analysis

The compatibility of the fabricated Sm_2O_3 /Ge stack with respect to ongoing MOS scaling has been verified by conducting HRTEM analysis. In Fig. 4.27 HRTEM cross sectional images disclosed double stacked layer interface for Sm_2O_3/Ge based gate stack. The uppermost surface is regarded as Sm_2O_3 dielectric film interface since it is positioned at larger distant with respect to Ge wafer while the middle position stack layer is denoted as interfacial layer (IL) as it is confined at the nearer interface from the Ge wafer. On the basis of XRD, Raman and XPS analysis the IL layer is composed of various chemical bonding such as Ge−O (i.e., GeO_2 and GeO_x), Ge−N and Sm−O−Ge. In Fig. 4.27 relatively thinner physical oxide thickness (Sm_2O_3 + IL) of 6.00 nm was formed for 15 min duration while the total physical oxide thickness increased by 0.91 nm when the duration was extended to 20 min at value of 6.91 nm. It is notable that, bulk Sm_2O_3 thickness shrank from 3.56 nm to 3.20 nm while the IL thickness incremented from 2.44 nm to 3.71 nm for 15 and 20 min, respectively. Accordingly, the reduction of total thickness at 15 min is caused by inhibition of IL growth which instigated to increase the bulk Sm_2O_3 thickness. Conversely, for 20 min the total oxide becomes thicker due to prompted growth of IL which impeded the growth of high *k* bulk Sm_2O_3.

Thus, the enhancement of bulk Sm_2O_3 high-*k* interface for 15 min is expected to improve the dielectric constant *k* value of the total gate stack. Meanwhile, the increased growth of IL for 20 min would impact negatively on dielectric constant, *k* and other electrical features. Additionally, total (Sm_2O_3 + IL) physical thickness of 5 and 10 min was extracted at value of 4.25 nm and 5.09 nm, respectively from the linear regression of total oxide thickness with respect to 15 and 20 min samples as depicted in Fig. 4.28. It has been assumed that (Sm_2O_3 + IL) thickness incremented linearly with extension of oxidation/nitridation durations.

Furthermore, diffraction patterns of Sm_2O_3, IL and Ge substrate for both 15 and 20 min was generated employing Fast Fourier Transformation (FFT) process on HRTEM images regulated by ImageJ Software. The diffraction patterns acquired from FFT is shown as inset image in Fig. 4.27. According to FFT it is apparent that both 15 and 20 min prompted the formation of amorphous bulk Sm_2O_3, and amorphous IL which is confirmed from the exposure of cloudy spotted FFT diffraction patterns. Additionally, detection of multiple spotted diffraction patterns from FFT suggested the polycrystalline orientation of substrate Ge for both the durations.

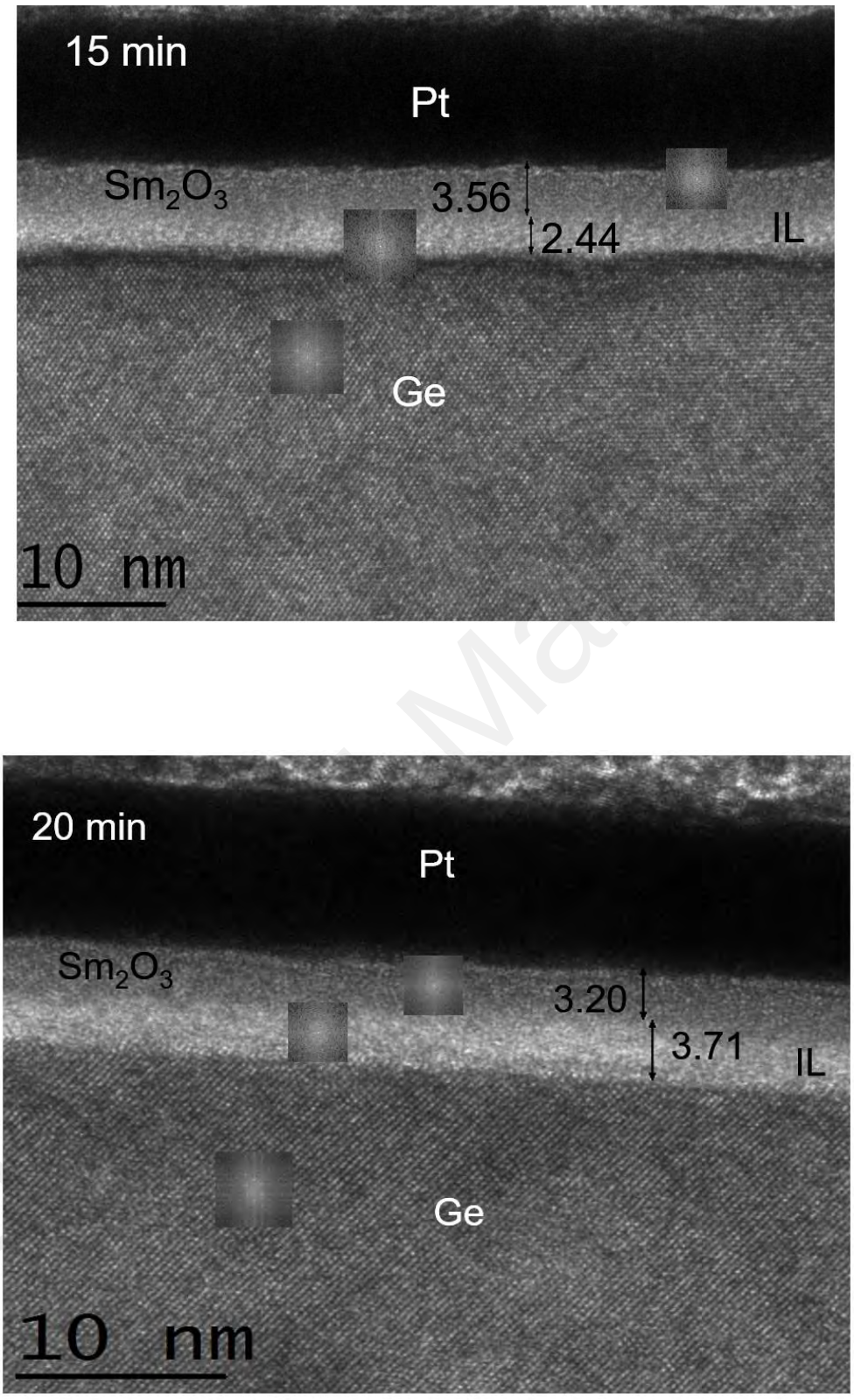

Figure 4.27: HRTEM cross-sectional morphology for thermally oxidized/nitrided 15 and 20 min samples.

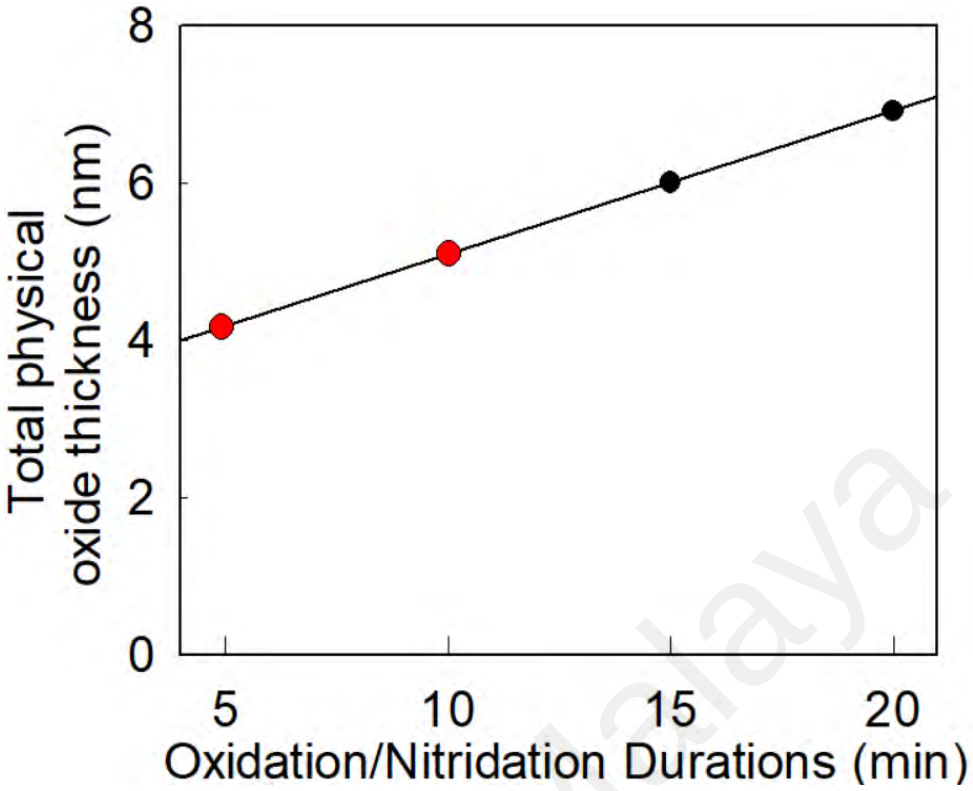

Figure 4.28: Linear regression plot of total oxide thickness of Sm_2O_3/IL/Ge as function of various oxidation/nitridation durations (5 – 20) min.

4.3.6 *C-V* Characteristics

Fig. 4.29 displays a high frequency (1 MHz) capacitance-voltage (C-V) plot obtained at room temperature for several thermal oxidation/nitridation durations (5 – 20) min. The measurements were taken using both forward and reverse gate bias condition by sweeping bidirectionally between -1 to +2V.

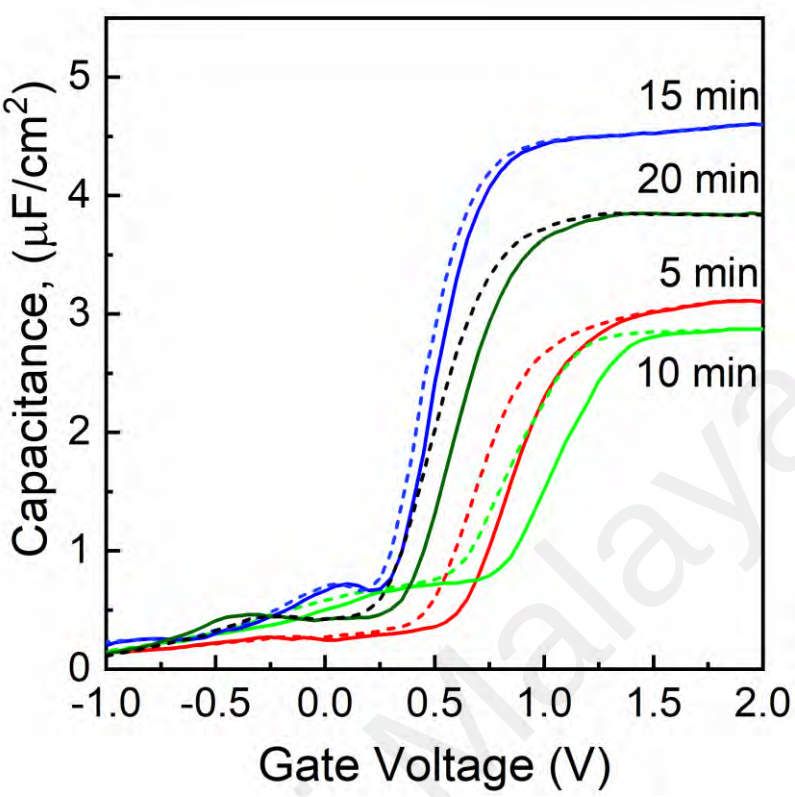

Figure 4.29: *C-V* features recorded at high frequency 1Mhz for Sm_2O_3/IL/Ge based MOS capacitors oxidized/nitrided at different durations (5 – 20) min.

In Fig. 4.29 the accumulation capacitance decreases substantially when the oxidation/nitridation duration is extended from 5 to 10 min but increases with a longer duration of 15 and 20 min. However, a significant drop of accumulation capacitance is observed when the duration is extended from 15 to 20 min. Overall, 15 min oxidation/nitridation condition exhibited the highest oxide capacitance while 10 min induced the lowest. On the basis of Eq. 4.10, the difference in accumulation capacitance level is associated with the total physical oxide thickness and dielectric constant value (k) since, $C_{ox} \propto \frac{k}{t_{ox}}$ when A and ε_o are constant. Accordingly, the oxide capacitance increases with shrinking of oxide thickness while the increment dielectric constant also attributes to increase the capacitance level. Moreover, the existence of IL has a crucial effect on the overall capacitance of a stack layered capacitor (Wilk et al., 2001).

According to earlier HRTEM Fig. 4.27, it was obvious that15 min owned thinner total oxide thickness as well as a thinner IL in counter to 20 min which might influenced to enhance the accumulation capacitance for 15 min oxidation/nitridation condition. Although, the total physical oxide thickness of 5 and 10 min is estimated to be lower than 15 and 20 min (shown in Fig. 4.28) but yet exhibited lower oxide capacitance. This observation suggested that the accumulation capacitance does not only varies due to oxide thickness but also depends on the interface quality and dielectric constant k value. For further clarification, the effective dielectric constant, C value of Sm_2O_3/IL/Ge gate stack were acquired from *C-V* curve using Eq. 4.10. According to Fig. 4.31 the k_{eff} values are 17.27 15.82, 31.19, 29.96, under 5,10, 15 and 20 min oxidation/nitridation, respectively. The findings of effective dielectric constant k_{eff} value and oxide capacitance reveal a proportional relationship as interpreted in Eq. 4.10. As observed in XPS, 10 min revealed the most thermally unstable interface and promoted the densification of low-k interfacial compounds (i.e., GeO_2 and GeO_x) which induced smallest k_{eff} value leading to lowest accumulation capacitance. Conversely, 15 min oxidation/nitridation induced largest k_{eff} value causing highest accumulation capacitance which is due to escalation of high-k Sm_2O_3 and suppression of interfacial low-k compounds. Regarding the k value of Sm_2O_3 MOS gate stack Pan & Huang, (2010) reported $k \sim 8.1 – 14.3$ for Sm_2O_3/(p-type) Si prepared using combination of RF sputtering rapid thermal annealing in (Ar/O_2) ambient. In other study, Chin & Cheong, (2011) reported the $k \sim 5.4 – 7.2$ for Sm_2O_3/(n-type) Si fabricated using furnace annealing in (N_2/H_2) ambient. However, the k_{eff} value obtained in this study does not reveals the same range. It has been reported that dielectric constant is largely contingent on type of electrode and substrate, physical characteristics of substrate-oxide interface and deposition procedure (Wong & Cheong, 2012b). Since, total physical thickness including interfacial layer was considered k_{eff} value estimation and amorphous Sm_2O_3 growth was observed in this investigation which might be one of the

possible reasons for k_{eff} value deviation from Sm_2O_3/Si interface (Chin & Cheong, 2011; Pan & Huang, 2010) where crystalline Sm_2O_3 was formed. The *EOT* measured at the corresponding k_{eff} values were found to be in range of 0.75 – 1.25 nm for oxidized/nitrided Sm_2O_3/IL/Ge stack layer in several durations as presented in Fig. 4.30. The 15 min oxidation/nitridation exhibited the lowest *EOT* ~ 0.75 nm due to its highest k and relatively thinner IL.

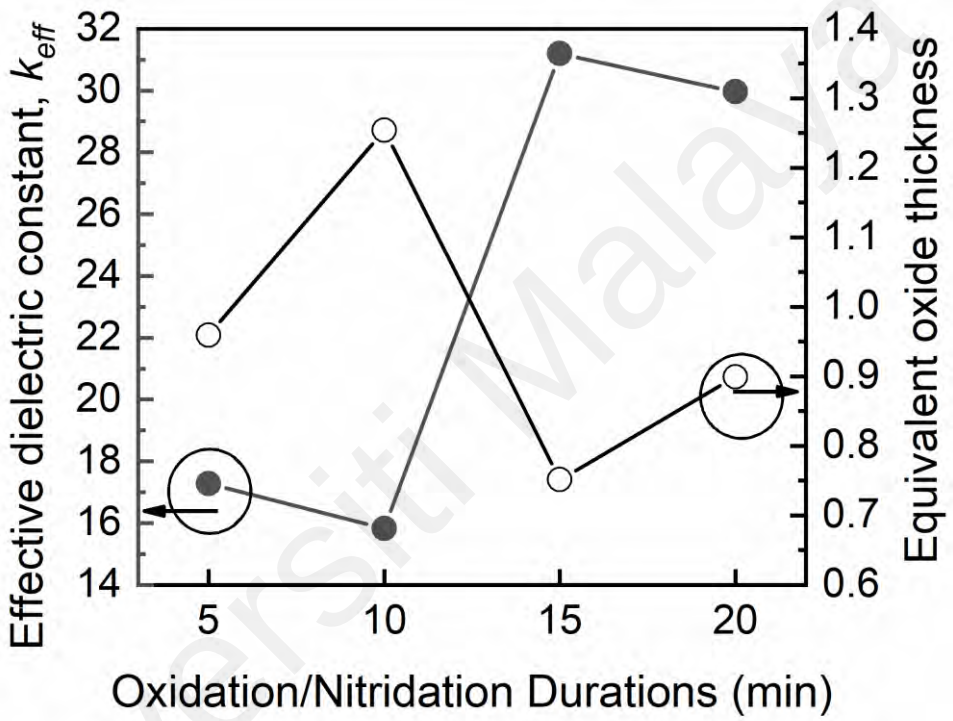

Figure 4.30: Effective dielectric constant, k_{eff} and equivalent oxide thickness obtained for Sm_2O_3/IL/Ge stack with respect to different oxidation/nitridation durations (5 – 20) min.

Furthermore, in Fig. 4.29 a stretch-out phenomenon towards the positive voltage region has been observed for all the investigated samples which confirms the presence of interfacial defect states at conduction band edge of Ge (He, Gao, et al., 2014). The 10 min oxidation/nitridation condition executed the strong stretch-out phenomenon as well as non-quasi saturation at accumulation regime. Since XPS confirmed increment of Ge−O contents at 10 min hence both of these phenomenon's is mainly due to generation of higher density defect states caused by the transportation of trap charges induced from

Ge−O and Ge−Ge bonding into the CB edge of substrate Ge. Meanwhile, for 15 min sample the stretch-out effect has been reduced substantially which is due to better interfacial interface consisting of less Ge−O bonding and Ge point defects as observed in Ge 3d and O1s spectra of XPS.

The *C-V* measurements of Fig. 4.29 also reveals that the flatband voltage, V_{FB} moved towards positive gate voltage axis for all the oxidation/nitridation durations. The positively shifted V_{FB} signifies the existence of negative oxide trap charges at/near the edge of Sm_2O_3 film interface (J. Gao et al., 2017; Wong & Cheong, 2012c). Amongst all the oxidation/nitridation durations 10 min persuaded the maximum V_{FB} shift followed by 5 and 20 min while 15 min oxidation/nitridation generated minimal shift. Hence, 10 min will generate more negative oxide charges while 15 min will reduce the amount of negative oxide charges which is depicted in Fig. 4.31. Typically, in MOS devices flatband voltage shift is caused by the oxygen vacancies within the high-*k* oxide interface. Accordingly, the extended V_{FB} shift for 5 and 10 min sample is caused by volatilization of GeO (g) as observed in Ge 3d spectra which enhanced oxygen vacancies into dielectric Sm_2O_3 film by adding extra negative oxide trap charges (C. C. Cheng et al., 2007). The smallest voltage shift for 15 min may be implicated by the presence of negative charged (singly or doubly) O interstitial. The effective oxide charge at different oxidation/nitridation durations has been estimated by Eq. 20.

$$\boldsymbol{Q_{eff} = \frac{\Delta V_{FB} C_{ox}}{qA}} \qquad \text{(Equation 4.20)}$$

Where, Q_{eff} represents effective oxide charge, ΔV_{FB} defines the difference of flatband voltage between ideal and experimental curve and q specifies for electronic charge. From Fig. 4.31 it is apparent that 15 min induced the lowest Q_{eff} of -2.88×10^{12} cm^{-2} and when the oxidation/nitridation reached 10 min the negatively oxide charges increased

drastically at Q_{eff} of -1.20×10^{13} cm^{-2}. The negatively charged Q_{eff} is attributed to the acceptor like traps at/near the Sm_2O_3 dielectric interface which could act as fixed charges when it is not sited in the edge of majority band (Ji, Xu, Lai, Li, & Liu, 2011; Wong & Cheong, 2012b). The Sm_2O_3/Ge gate stack fabricated at 15 min oxidation/nitridation condition could reduce the broken bonds and oxygen vacancies within the Sm_2O_3 film which preserves the homogeneousness of Sm_2O_3 interface causing diminution in Q_{eff}. Conversely, the 10 min increased the Q_{eff} due to degraded Sm_2O_3 interface quality caused by the severe O atoms out-diffusion from Sm_2O_3 film. The lowest $Q_{eff} \sim -2.88 \times 10^{12}$ cm^{-2} achieved for Sm_2O_3/Ge interface is significantly lower than Sm_2O_3/Si (Goh et al., 2017b) and Tm_2O_3/Ge (Žurauskaitėa et al., 2018).

Besides, fixed oxide charges the interface dipole formation can also contribute to the shift of flat-band voltage in the case of high-*k* dielectric stacked gate insulator (Kita & Kamata, 2017; Kita & Toriumi, 2009). It has been reported that flatband voltage shift due to dipoles are physically originated from the chemical bonding differences caused by the oxygen movement initiated from oxygen area density difference at interface within high-*k* oxide/interfacial oxide (Kita & Toriumi, 2009). It was pointed that oxygen movement between the high-*k* /IL interface induces Frenkel type defect of vacancy−interstitial pair which corresponds to form interface dipoles. However, the amount of dipole formation may change according to the process condition which effects the V_{FB} shifting. The contribution of interface dipoles in regulating V_{FB}shift can be explained from the difference of chemical bonding characteristics of dielectric Sm−O and interfacial Ge−O denoted in XPS and Raman analysis. Since strong deformation of Ge−O and Sm−O bonding's were observable at 10 min and so it is anticipated that the free energy of Sm_2O_3 and IL interface is increased activating more oxygen movement. As a result, anomalous coordination of negatively charged oxygen between Sm_2O_3 and IL (GeO_2 or GeO_x) has been

enhanced inducing large amount of interface dipoles by maximizing the vacancy−interstitial pair leading to the largest V_{FB} shift. Meanwhile, it is predicted that reduction of flatband voltage (relatively negative shift) is caused by minimization of charge imbalance that corresponds to interface dipoles by lessening oxygen density abruptness in Ge−O and Sm−O interface (Kita & Kamata, 2017). The relatively negative V_{FB} shift for 15 min can also be attributed the minimum interface dipole formation due to denser Sm−O−Ge formation and comparatively more nitrogen incorporation which impeded imbalance charge generation caused by anomalous oxygen transmission mechanism from Sm_2O_3 towards GeO_2 or GeO_x interface. The interface dipole within high-*k*/high-*k* was not considered rather high-*k*/IL region was considered since deformation of covalent Ge−O could trigger much higher driving force in oxygen diffusion than those of Sm−O ionic bonds for high-*k* dielectrics (Kita & Toriumi, 2009).

A clearly visible hysteresis effects in the *C-V* curves have been noticed, ranging from 50 – 200 mv which is presented in Fig. 4.32. It was pointed that hysteresis effect typically occurs during the bidirectional swept when an electron filling a trap and leaving the traps does not coincide at same gate bias voltage which is caused by the existence of slow traps states (He, Liu, et al., 2014; Ke et al., 2018). The slow trap density, (Q_{it}) can be estimated using Eq. 4.11. Fig. 4.31 also shows that, 10 min sample generated the highest $Q_{it} \sim 3.44 \times 10^{12}$ cm^{-2} while the lowest $Q_{it} \sim 1.41 \times 10^{12}$ cm^{-2} occurred when the duration raised to 15 min. Accordingly, suppression of hysteresis for 15 min has been induced from generation of fewer slow trap states during the oxidation/nitridation process. The slow traps in the gate stack are generally caused by the (i) defective high-*k* interface (ii) defect states localized at/nearby high-*k*/IL interface and (iii) tunneling of charged carriers (electron or hole) from Ge wafer towards high-*k*/IL interface (C. C. Cheng et al., 2007; Ke, Yu, Chang, Takenaka, & Takagi, 2016). From XPS measurement it was established that 10 min oxidation/nitridation upsurged the oxygen content diffusion

from Sm_2O_3 itself which escalated the rapid chemical reaction between diffused Ge and O atoms causing higher defect states at/nearby Sm_2O_3/GeO_x interface. Consequently, triggering the slow traps states at this duration. Conversely, for 15 min barrier role of Sm−Ge−O inhibited such inter-diffusion leading to fewest slow traps. According to the *STD* findings, tunneling of both electron and hole towards Sm_2O_3/IL interface from substrate Ge increased the most for 10 min oxidation/nitridation while transmission of carrier charges lessened at 15 min. Besides, accumulation of interstitial N^+ atoms at high-*k* or near high-*k*/IL also induces additional slow trap states (Misra et al., 2006). Accordingly, the increase of *STD* for shorter durations 5 and 10 min directs that these oxidation/nitridation conditions promote the piling of N^+ atoms which is asymmetrically distributed into the Sm_2O_3/IL or Sm_2O_3 interface. Meanwhile, it is suggested that longer duration of 15 and 20 min decreases extent of out-diffusing N^+ atom and also maintains a homogenous distribution since compensation of *STD* is being observed. These indications are supportive with Raman and XRD analysis, which showed more intensified and crystalline Ge_3N_4 for 15 and 20 min due to less N^+ atoms out-diffusion, while the non-uniform accumulation of N^+ atoms induced an amorphous Ge_3N_4 with lowest intensity for 5 and 10 min. The kink and hump appeared at weak inversion regime for several oxidation/nitridation durations is associated with the additional slow trap states caused by N^+ atoms distribution. The alteration of *STD* with respect to various durations exposed similar pattern with Q_{eff}. The $Q_{it} \sim 1.41 \times 10^{12}$ cm^{-2} for 15 min obtained in this study is inferior to previously reported *STD* (Q_{it}) of Sm_2O_3/Si $\sim 5.56 \times 10^{12}$ cm^{-2} (Goh et al., 2017b).

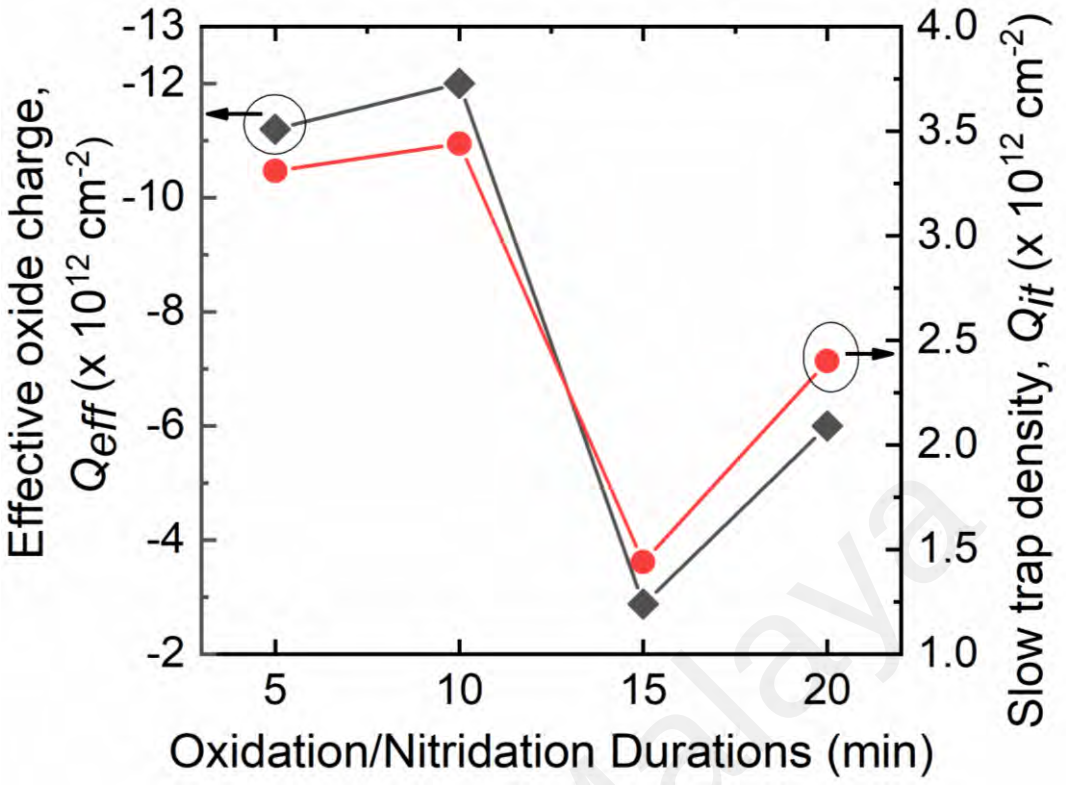

Figure 4.31: Effective oxide charge, Q_{eff} and slow trap density, Q_{it} acquired from *C-V* plot of Sm_2O_3/IL/Ge gate stack at different oxidation/nitridation durations (5 – 20) min.

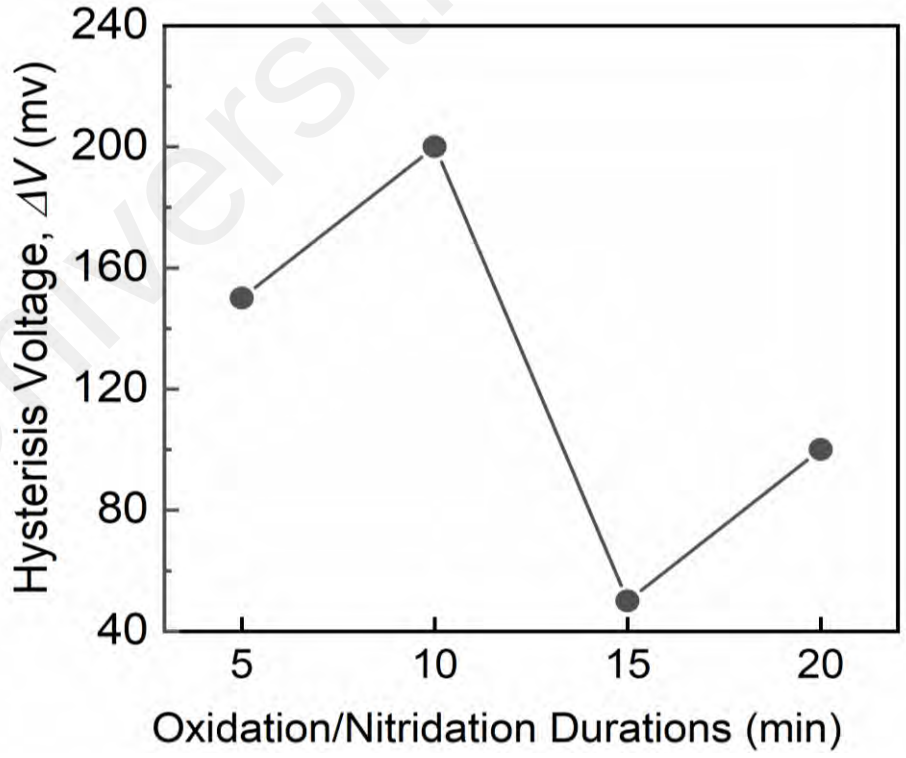

Figure 4.32: Hysteresis voltage variations of Sm_2O_3/IL/Ge gate stack for various thermal oxidation/nitridation durations (5 – 20) min.

Furthermore, in Fig. 4.33 the average interface trap density D_{it} as function of trap energy level $(E_c - E)$ for different oxidation/nitridation durations (5 − 20) min were extracted from *C-V* curve using Terman method which is governed by Eq. 4.12**.** From Fig. 4.33 it was found that the average interface trap density D_{it} scattered between $\sim 10^{13} - 10^{14}$ eV^{-1} cm^{-2} at trap energy level $(E_c - E)$ = 0.09 − 0.27 eV. Amongst all the oxidation/nitridation condition 10 min provides the highest $D_{it} \sim 2.49 \times 10^{14}$ eV^{-1} cm^{-2} and the lowest $D_{it} \sim 4.84 \times 10^{13}$ eV^{-1} cm^{-2} at mid-gap of $(E_c - E)$ = 0.2 eV was acquired for 15 min. Concerning oxide/Ge interfaces typically, D_{it} is enhanced due to degraded interface quality by the volatilization of GeO (g) and decomposition of GeO_2 (Matsubara et al., 2008; Zhao et al., 2018). The reduction of D_{it} for 15 min can be attributed to generation of higher density of Sm−O−Ge and Ge_3N_4 as observed in XPS and Raman spectra. The diffusion barrier role of Sm−O−Ge and Ge_3N_4 played a vital part to saturate the oxygen vacancies and in alleviation of un-bonded Ge caused by desorption and decomposition of GeO and GeO_2. It is anticipated that, growth of denser Sm−O−Ge and Ge_3N_4 at this duration restricted the intermixing of Ge and O atoms near the substrate Ge interface and within interfacial GeO_2 network. Eventually, prompted less defective retarded the expansion of sub-stochiometric Ge suboxides (GeO_x) and causing reduction of interface trap density. Due to the same reason 20 min oxidation/nitridation caused lower D_{it} than 5 and 10 min samples. On the contrary, the highest D_{it} for 10 min is caused by extreme GeO (g) volatilization and GeO_x densified IL layer due to enhancement of oxygen related defects and Ge dangling bonds. Since this duration was not suitable for growing Sm−O−Ge. Besides, creation of sub-stoichiometric Sm_2O_3 also generated more charged traps confining spots located at/near Sm_2O_3/IL which included additional interfacial traps at this duration.

The inset image of Fig. 4.33 shows the total interface trap density D_{total} acquired by estimating the integrated area under D_{it} vs $(E_c - E)$. The pattern of D_{total} as function of different oxidation/nitridation durations follows analogous variation as of effective fixed oxide charge, (Q_{it}) and *STD*, (Q_{it}). The lowest D_{total} attained for this investigation is 1.2×10^{13} cm^{-2} during oxidation/nitridation of 15 min. In comparison with previous reports the minimum $D_{it} \sim 4.84 \times 10^{13}$ eV^{-1} cm^{-2} (at energy level, $E_c - E \sim 0.2$ eV) for this investigation is larger than post annealed Sm_2O_3/Ge interface $D_{it} \sim 5.10 \times 10^{11}$ eV^{-1} cm^{-2} (C. C. Lin et al., 2014) and multi stacked $HfO_2/Al_2O_3/GeO_x$/Ge interface $D_{it} \sim 2.0 \times 10^{11}$ eV^{-1} cm^{-2} (R. Zhang et al., 2013) . Although, in this study relatively smaller $D_{it} \sim 10^{13}$ eV^{-1} cm^{-2} and $D_{total} \sim 1.2 \times 10^{13}$ cm^{-2} has been integrated than the Sm_2O_3/Si thermally oxidized gate stack with a $D_{it} \sim 10^{14}$ eV^{-1} cm^{-2} and $D_{total} \sim 7.30 \times 10^{13}$ cm^{-2} (Goh et al., 2017b).

From the overall *C-V* features, it is noted that, Sm_2O_3/Ge gate stack oxidized/nitrided at15 min could exhibit a high *k* value of 31.19 with a low *EOT* ~ 0.75 nm but expenses higher $D_{it} \sim 10^{13}$ eV^{-1}cm^{-2} which is still inconvenient for MOS application hence, a D_{it} reduction strategy is required. In summary, it is suggested that 15 min thermal oxidation/nitridation durations possesses the best *C-V* features for Sm_2O_3/IL/Ge gate stack.

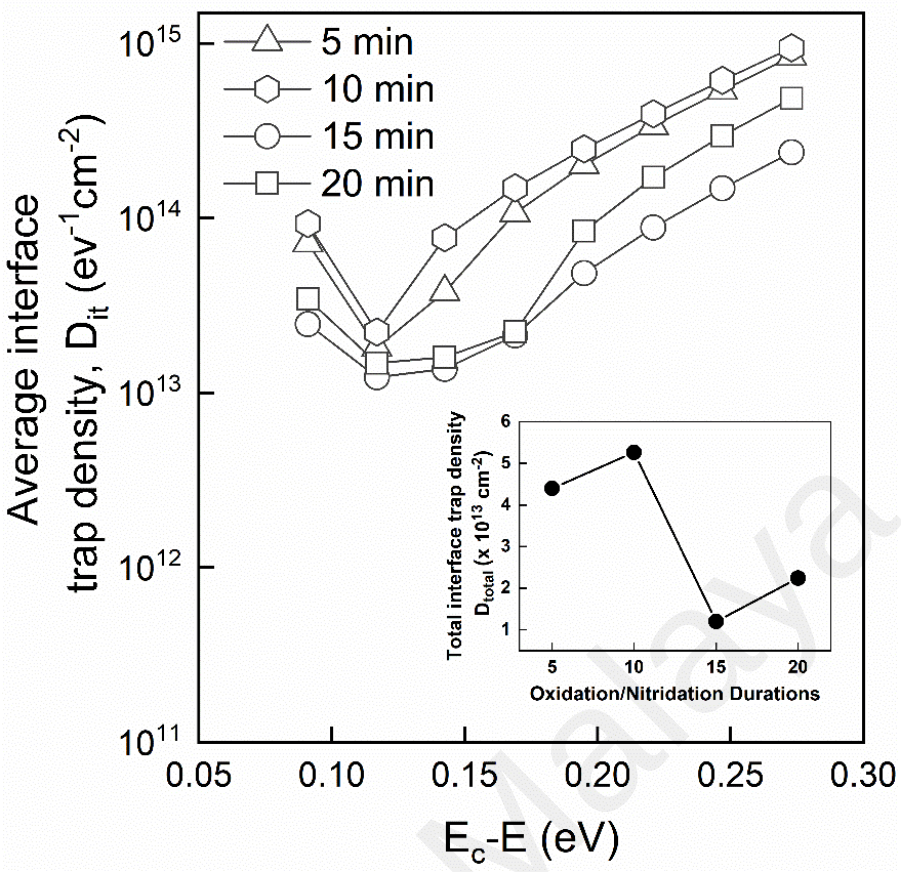

Figure 4.33: Average interface trap density D_{it} approximated with respect to trap energy level ($E_C - E$) for Sm_2O_3/IL/Ge gate stack developed under different oxidation/nitridation (5 – 20) min. Inset image presenting total interface density as function of different durations.

4.3.7 J-E Characteristics

Fig. 4.34 depicts the electrical features of gate leakage current density, versus electrical field E for the gate stacks investigated at different thermal oxidation/nitridation durations (5 – 20) min. In Fig. 4.34 two-step electrical breakdown field is noticed due to creation of interfacial layer (IL) interface. It is assumed that any of the interface either Sm_2O_3 or IL was broken at pre-mature electric field causing two step breakdown fields. The electrical field broken at lower stage is classified as soft breakdown denoting E_{SBD} and the broken electrical field at higher stage is quantified as hard breakdown E_{HBD}.

The leakage current density and breakdown field for various instigated durations occurred at E_{HBD} is considered for quantifying electrical features of *J-E* curve. The Sm_2O_3/ IL/Ge stack which induces lowest J_g and highest E_{HBD} is regarded as the finest *J-E* featured MOS capacitor. From the *J-E* curve the E_{HBD} is observed at 7.81 MV cm^{-1}, 5.67 MV cm^{-1}, 13.31 MV cm^{-1} and 9.98 MV cm^{-1} for 5, 10, 15 and 20 min, respectively. Meanwhile, the leakage current density value at E_{HBD} was recorded at10^{-3}, 10^{-4}, 10^{-5} order of magnitude for 5, 10 and 20 min, respectively whereas J_g value dropped to 10^{-6} order magnitude when the oxidation/nitridation duration reached 15 min. Comparing all the samples, 15 min oxidation/nitridation durations induced the lowest leakage current density, $J_g \sim 8.38 \times 10^{-6}$ A cm^{-2} and largest hard breakdown field $E_{HBD} \sim$ 13.31 MV cm^{-1}. Besides, this duration also exhibited the largest soft breakdown $E_{SBD} \sim$ 4.67 MV cm^{-1} at gate leakage current density, 5.91×10^{-6} A cm^{-2}. The increase of leakage current for 5 and 10 min is due to volatilization of GeO (g). Since 10 min condition accelerated the GeO (g) desorption as confirmed in XPS analysis and so causing lowest J_g due to deterioration of insulation properties at Sm_2O_3 interface. Suppression of GeO (g) for 15 and 20 min gate stack attributed to improve the leakage current densities. From several previous reports (Wong & Cheong, 2011b, 2012c) it was found that increase of IL layer causes lower electrical breakdown field. The HRTEM images (Fig. 4.27) evidenced that, the IL layer is reduced at 15 min in counter to 20 min hence a larger breakdown field and one order lower leakage current has been generated at 15 min. Besides, the biggest CBO, ΔE_c obtained for 15 min would limit the movement of electrons from substrate Ge to the gate electrode through Sm_2O_3/IL which also instigated to achieve lowest J_g magnitude. Conversely, the lowest CBO, ΔE_c observed for 10 min assisted the electrons to cross over the barrier height between (Sm_2O_3 + IL) and substrate Ge causing largest leakage current density while initiating faster electrical breakdown.

In addition, the reduction of leakage current density at 15 min is also complementary with the XRD findings where more amorphous Sm_2O_3 was formed during the 15 min oxidation/nitridation which diminished the current conduction path due to grain consolidation. Furthermore, the fewest Q_{eff}, Q_{it}, D_{it} also aided in generating largest breakdown field for 15 min oxidation/nitridation condition. The lowest $J_g \sim 8.38 \times 10^{-6}$ A cm^{-2} and largest $E_{HBD} \sim 13.31$ MV cm^{-1} exhibited for Sm_2O_3/Ge gate stack is higher than the ZrO_2/Ge (Lei et al., 2018), La_2O_3/Ge (Zhao et al., 2018), Sm_2O_3/Si, (Goh et al., 2016b) and Nd_2O_3/Si (Hetherin et al., 2017a). Therefore, it is suggested that 15 min oxidation/nitridation condition facilitates best electrical properties in *J-E* plot.

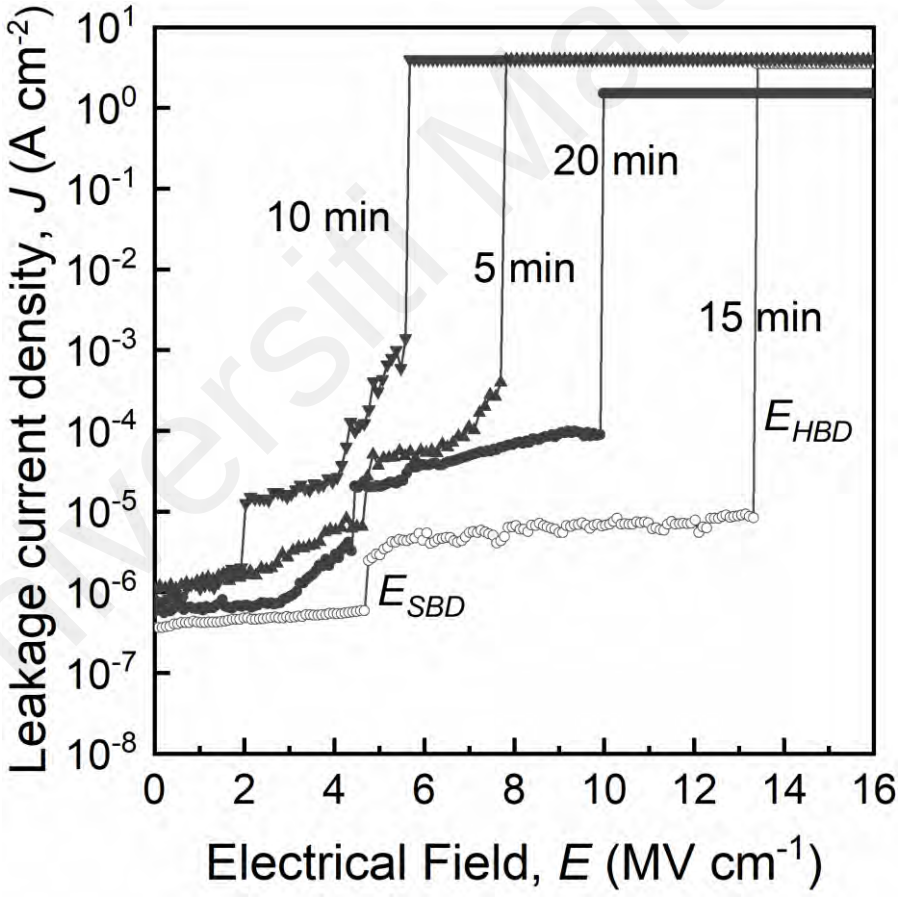

Figure 4.34: *J-E* features for Sm_2O_3/IL/Ge based MOS capacitors at different oxidation/nitridation durations (5 − 20) min.

4.4 Influence of Various Thermal Oxidation/Nitridation Durations on Sputtered Ho/Ge in N_2O Ambient.

4.4.1 XRD Analysis

A systematic study of XRD patterns were conducted to get detail insight on the crystal orientation and structure of the fabricated gate stack. Fig. 4.35 displays the close up XRD patterns at 2θ range within (10° – 60°) for various oxidization/nitridation durations 5 min, 10 min, 15 min and 20 min. Two strong peaks and a weaker peak belong to cubic Ho_2O_3 denoted as c-Ho_2O_3 were detected at 29.16°, 59.08° and 48.20° corresponding to plane orientations (222), (631) and (440), respectively for all the investigated samples. Besides, two more weaker peaks of c-Ho_2O_3 also appeared at 35.56° with plane orientation (411) was detected for 10 and 15 min samples while the peak at 47.35° corresponding to c-Ho_2O_3 with plane orientation (512) appeared for the 5, 10 and 20 min samples. Meanwhile, four additional relatively blunt peaks of c-Ho_2O_3 were detected at 41.97°, 54.15°, 56.34° and 57.17° corresponding to plane orientations of (431), (602), (541) and (622), respectively for 10 min samples. The c-Ho_2O_3 peaks phases matched with the Inorganic Crystal Structure Database (ICSD) reference code no. 33655 and 152458. The diffraction peaks of GeO_2 appeared in tetragonal phase denoted as t-GeO_2 found at 27.16° and 39.11° with plane orientations (110) and (201), respectively for 5 and 10 min. Meanwhile, GeO_2 was not detected for 15 and 20 min samples which indicates the amorphous structure of GeO_2 for these durations. The t-GeO_2 peaks were confirmed by the ICSD reference code no. 9015579. Moreover, a sharp diffraction peak of Ge_3N_4 revealed at 31.73° corresponding to plane (211) for 10 and 15 min while the peak became weaker for 5 min sample. Due to amorphous structure of Ge_3N_4 no diffraction pattern of Ge_3N_4 was detected for 20 min sample. The diffraction peak corresponded well with the ICSD reference code no. 152551 which signifies the cubic phase of Ge_3N_4.The findings from XRD spectra validates formation of Ho_2O_3 dielectric layer and existence of Ge_3N_4

and GeO_2 suggests the creation of interfacial layer (IL) between the dielectric oxide film layer and Ge substrate.

Furthermore, according to the XRD pattern it is noticed that peak intensity of c-Ho_2O_3 at 29.16° (222), 59.08° (631) and 48.20° (440) increases when the oxidation/nitridation duration extended from 5 min to 10 and 15 min but gradually decreasing from 10 to 20 min as shown in Fig. 4.36. It is apparent that 10 min exhibits the highest Ho_2O_3 peak intensity followed by 15 and 5 min samples and 20 min sample exhibits the lowest intensity. Since increment of intensity indicates the degree of crystallinity and thus, it can be suggested that 10 and 15 min oxidation/nitridation durations enhances crystallinity of Ho_2O_3 dielectric interface while oxidation/nitridation of both shorter time (5 min) and longer time (20 min) decreases crystallinity of Ho_2O_3 film. Comparing all the investigated sample it can be inferred that the dielectric oxide film is more crystalline for 10 min sample and least crystalline for 20 min sample. The decrease of Ho_2O_3 intensity for 5 and 20 min samples may be induced from large amount of defects caused by the excessive O atom diffusion from the dielectric interface. Thus, the peaks became broader with lower intensities. The release of O atom from Ho_2O_3 film for 5 and 20 min samples were also apparent from XPS analysis as discussed in section 4.5.3.

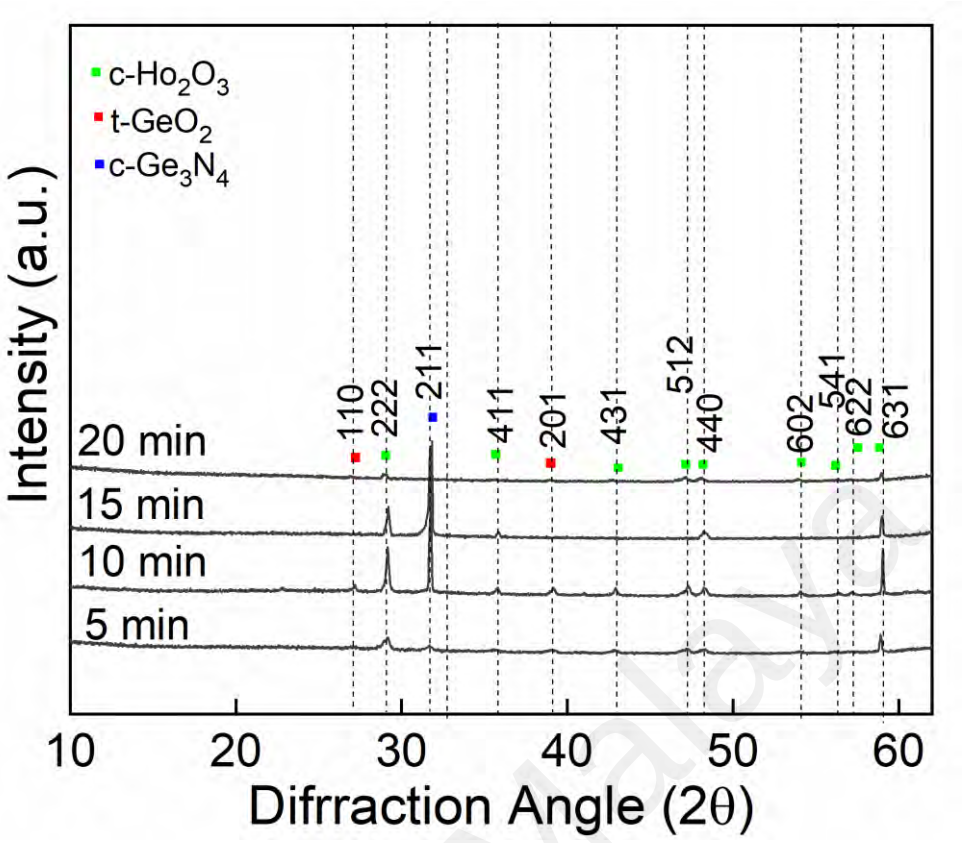

Figure 4.35: XRD spectra of the Ho/Ge samples oxidized/nitrided at different durations (5 min, 10 min, 15 min, and 20 min).

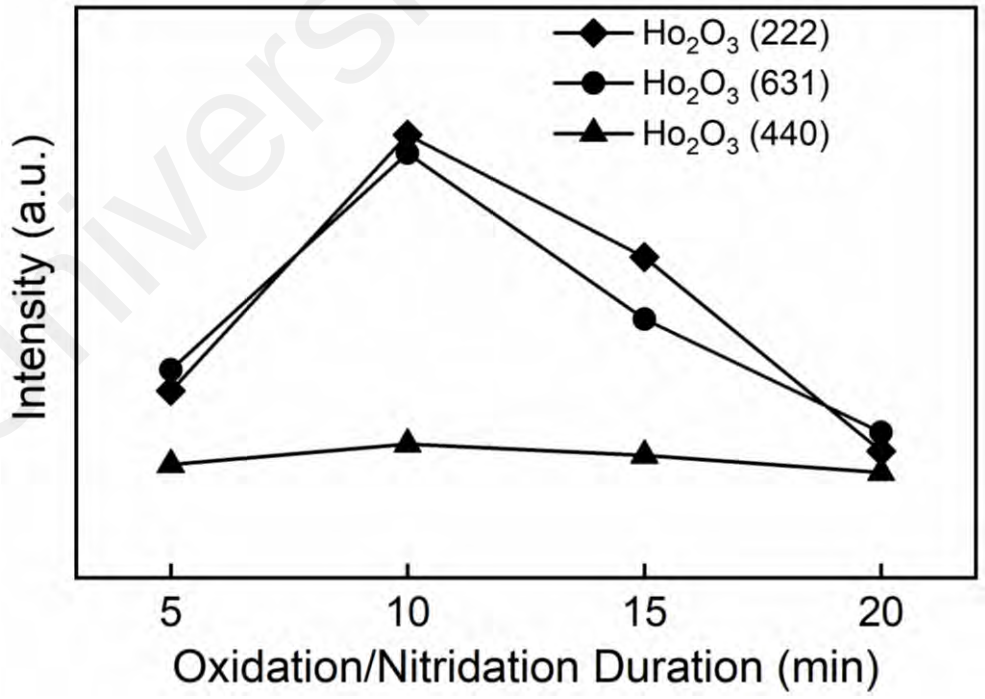

Figure 4.36: Cubic, c-Ho_2O_3 intensities at various oxidation/nitridation durations (5 min, 10 min, 15 min, and 20 min).

The crystallite sizes, D and micro-strains, ε of the detected elements has been estimated from the peak broadening of the XRD pattern employing Williamson−Hall plot. According to Eq. 3.5, a graph of $\beta_\tau \cos\theta$ as a function of $4\varepsilon \sin\theta$ for Ho_2O_3 has been plotted as shown in Fig. 4.37. The well fitted points with regression co-efficient $r^2 = 1$ were considered for linear fitting from the range of distributed values. As defined in Eq. 3.5, the intercept of the graph is equal to $\frac{\kappa\lambda}{D}$ which provides the estimation of crystallite size D whereas the gradient of linear regression gives the micro-strain, ε value. Crystallite sizes of GeO_2 and Ge_3N_4 were not calculated due to insufficient number of peaks which were insignificant for the approximation.

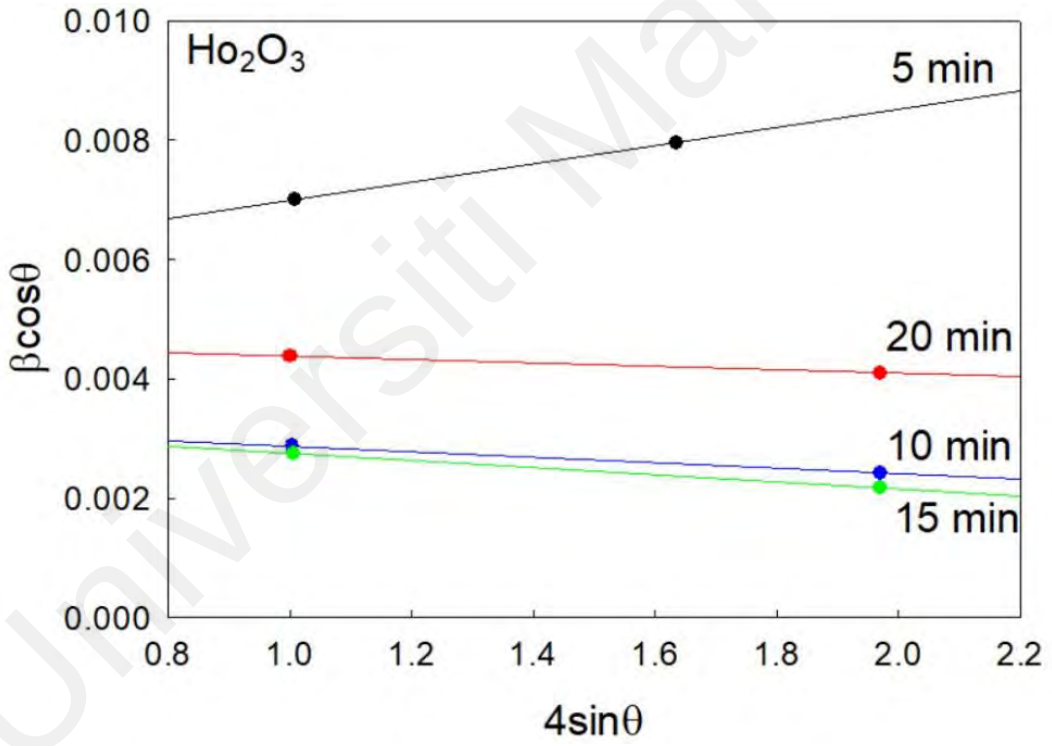

Figure 4.37: Williamson−Hall (W−H) plot of c-Ho_2O_3 for investigated oxidized/nitrided samples at various durations (5 − 20) min.

The crystallite sizes and micro-strain of Ho_2O_3 calculated from W-H plot is displayed in Fig 4.38. The crystallite sizes of Ho_2O_3 increased from 25.33 nm to 41.25 nm when the oxidation/nitridation duration extended from 5 to 10 min but decreased from 41.61 nm to 29.53 nm after extending the duration from 15 to 20 min. However, it is noticeable that crystallite sizes increased slightly from 41.25 nm to 41.61 nm while incrementing the duration from 10 to 15 min. The small difference of crystallite size between 10 and 15 min samples might be due to well distributed and more homogenous crystallite size. Meanwhile, positive micro-strain value was found for 5 min sample while the other investigated samples yielded negative micro-strains. The highest micro-strain value of 0.0015 was recorded for 5 min sample and the second highest value of -0.0003 was recorded for 20 min oxidation/nitridation duration. However, the micro-strain of 10 and 15 min samples are almost same with a value of -0.0004.

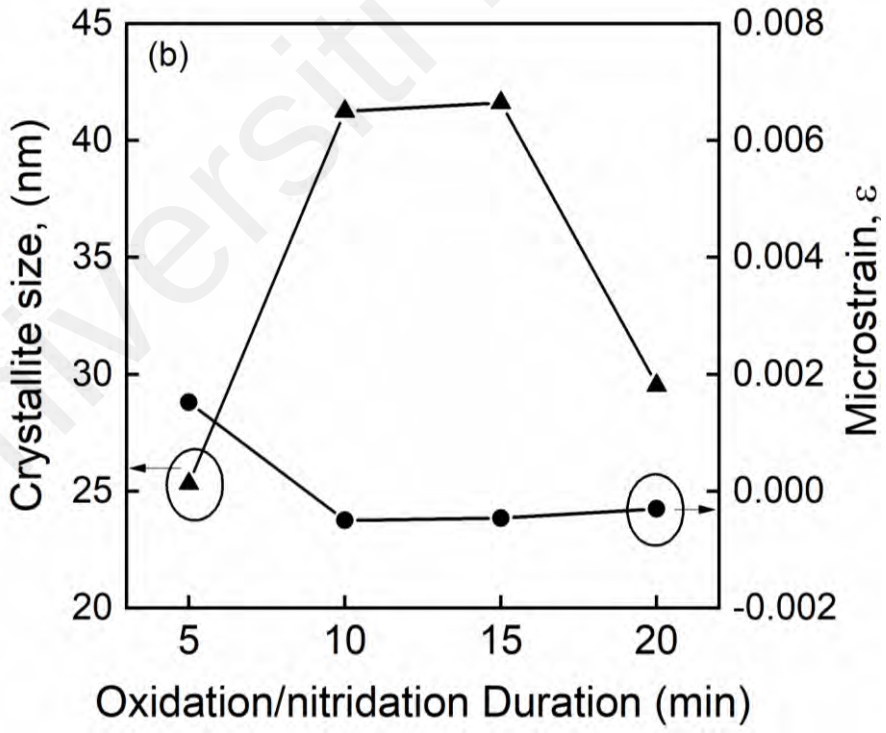

Figure 4.38: Crystallite sizes (triangle symbol, left axis) and micro-strains (circle symbol, right axis) of Ho_2O_3 at various oxidation/nitridation durations (5 min, 10 min, 15 min, and 20 min).

4.4.2 J-E Characteristics

Fig. 4.39 demonstrates the leakage current density, J_g with the function of electrical field, E for various oxidation and nitridation durations 5 min, 10 min, 15 min and 20 min. The current–voltage (*I-V*) measurement was transformed to (*J-E*) plot by applying Eq. 3.6 According to the *J-E* plot the sample which corresponds to lowest leakage current density, J_g and retains highest electrical breakdown field, E_{BD} was regarded as the best electrical behaviour over other samples. Two step breakdowns were recorded for all the investigated samples. Formation of top Ho_2O_3 layer and an interfacial layer between dielectric and Ge substrate is the main reason for the occurrence of two-step breakdowns (Wong & Cheong, 2011c). The initial stage breakdown that occurs in the lower electric field has been labelled as soft breakdown, E_{SBD} where the instant increase of leakage current density remains relatively low. On the other hand, the sharp the breakdown observed on the higher electric field is considered as hard breakdown, E_{HBD} where the increase of instantaneous leakage current density is larger. The electrical field breakdown and leakage current density occurred on the hard breakdown, E_{HBD} position was considered for evaluating best electrical properties among the investigated capacitors. The recorded hard electrical field breakdown, E_{HBD} for 5 min, 10 min, 15 min and 20 min samples were 4.47 MV cm^{-1}, 8.59 MV cm^{-1}, 7.25 MV cm^{-1} and 2.97 MV cm^{-1}, respectively. It is observed that leakage current density, J_g at E_{HBD} for 10 and 15 min were in 10^{-5}, 10^{-4} order of magnitude respectively while the leakage current density, J_g increased to 10^{-3} order of magnitude for 5 and 20 min samples. Among all the investigated capacitors 10 min sample exhibits highest electrical breakdown field, E_{HBD} of 8.59 MV cm^{-1} with the lowest leakage current density, J_g of 5.34×10^{-5} A cm^{-2} at E_{HBD}. In addition, 10 min sample also induces highest soft breakdown field, E_{SBD} of 4.58 MV cm^{-1} at leakage current density, J_g of 1.77×10^{-7} A cm^{-2}.

Therefore, 10 min oxidized/nitride sample yields the best *J-E* performance for Ho_2O_3 dielectric based MOS devices. It is noticeable that 20 min sample initially kicked off with a leakage behaviour and leakage current density was unusually high before the hard breakdown which might be due to damaged Ho_2O_3 dielectric layer caused by the extreme desorption of GeO from the Ge substrate during the extended oxidation/nitridation process (Lei et al., 2017). The improvement of dielectric breakdown and leakage current density for 10 min and 15 min samples are possibly related to the alleviation of structural defect comprising oxygen vacancies and Ge dangling bonds in Ho_2O_3/IL interface (Hosoi et al., 2009). Moreover, 10 and 15 min samples of Ho_2O_3/Ge revealed comparatively lower leakage current density, $J_g \sim 10^{-5} - 10^{-4}$ A cm^{-2} and higher electrical breakdown field, $E_{BD} \sim 7.25 - 8.59$ MV cm^{-1} than the reported ZrO_2/Ge system thermally oxidized/nitrided in N_2O ambient [where, $J_g \sim 10^{-3}$ A cm^{-2} and $E_{BD} \sim 6.9$ MV cm^{-1}] (Lei et al., 2018).

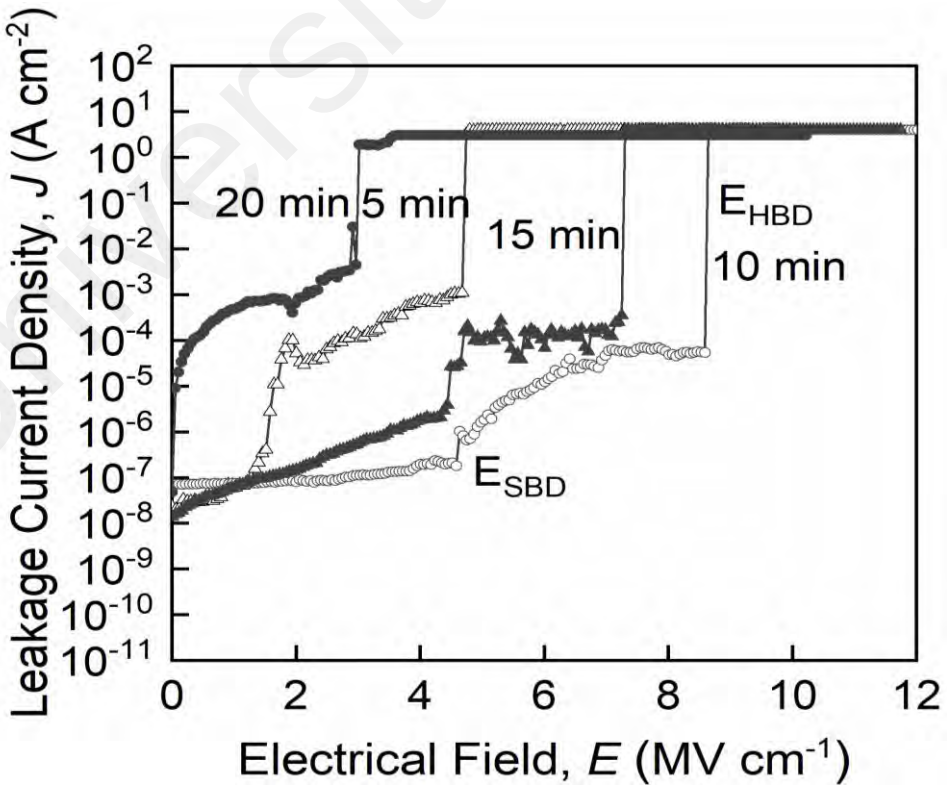

Figure 4.39: *J-E* curve of various oxidized/nitrided sample at durations (5 min, 10 min, 15 min, and 20 min).

4.4.3 XPS Analysis

XPS analysis was conducted to get insight on the structural and compositional properties of Ho_2O_3 dielectric gate stack. According to the survey scan core level spectra of Ho 4d, Ge 3d, O1s, N1s were detected. Narrow scan of Ho 4d, Ge 3d, O1s were performed for samples oxidized/nitrided at different durations 5 min, 10 min, 15 min and 20 min. Fig. 4.40 depicts the deconvoluted peaks of Ho 4d narrow scan for various oxidation/nitridation durations 5 min, 10 min, 15 min and 20 min. The reference peak position of Ho_2O_3 in the Ho 4d spectra was reported at 161.8 eV (Pan, Chang, et al., 2010; Pan, Yen, et al., 2010). It is clearly visible that the centroid peak of Ho 4d shifts negatively towards the lower binding energy by 1.07 eV, 0.66 eV, 0.87 eV, and1.17 eV, respectively for 5, 10, 15, and 20 min with respect to reference position of Ho_2O_3. The negative shift towards the lower binding energy indicates the formation of sub-stoichiometric Ho_2O_3 for all the investigated samples (Wong & Cheong, 2011c). This finding suggests the release of O atom from the Ho_2O_3 dielectric itself towards the Ge substrate. Since 10 min sample yields the lowest negative shift of binding energy in other way it can be said that shifting toward higher binding energy in compared to other samples which indicates comparatively less O diffusion than the other investigated samples. Hence, 10 min sample promotes formation of more stoichiometric Ho_2O_3 and exhibits higher growth of Ho_2O_3 than those of 5, 15 and 20 min samples. Conversely, 20 min sample yields the highest negative shift towards the lower binding energy site followed by 5 and 15 min samples. In this case it can be assumed that the growth of Ho_2O_3 is hampered due to excessive O diffusion from the Ho_2O_3 film which induces formation of less stoichiometric Ho_2O_3 dielectric layer while leaving large amount of oxygen vacancies. Therefore, according to the binding energy shift of Ho 4d spectra it is predicted that Ho_2O_3 growth will be highest Ho_2O_3 for 10 min sample followed by 15 min and 5 min while the lowest at 20 min sample. The validation of this assumption will be explained in the O1s spectra.

Based on Ho 4d spectra observation, it can be suggested that better growth of Ho_2O_3 is primarily related to the degree of sub-oxide (Ho–O–Ho) transformation and the amount of O atom diffusing from Ho_2O_3 dielectric itself. Furthermore, the negative shift in the direction of lower binding energy also indicates Ho_2O_3 gate stack does not create any Germanate (Ho–O–Ge) compound in the interfacial layer.

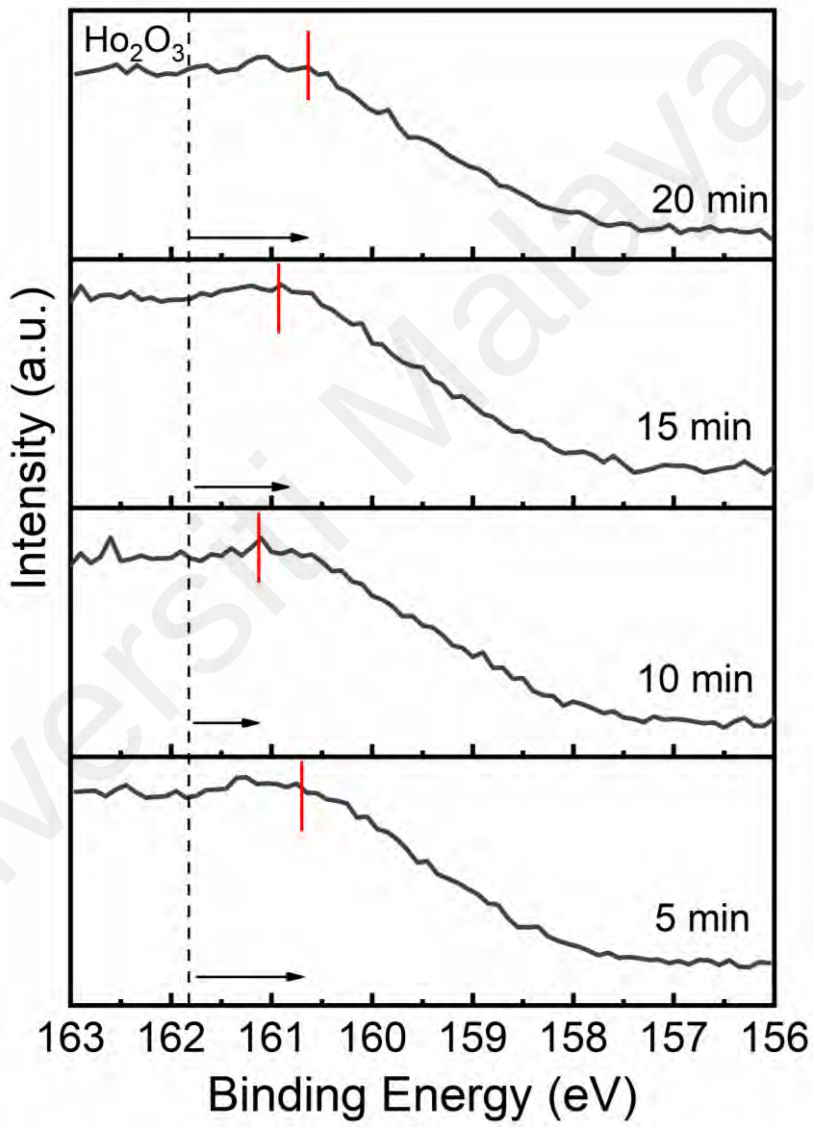

Figure 4.40: Ho 4d narrow scan spectra measured for oxidized/nitrided sputtered Ho/Ge samples at different oxidation/nitridation durations (5 – 10) min.

Fig. 4.41 elucidates the Ge 3d spectra of different oxidation/nitridation durations (5 – 20) min. Ge 3d spectra comprises two broad peaks which incorporates Ge^0 and mixture of various chemical bonding states of distinctive Ge sub-oxides. It has been reported that, Ge 3d peak positions typically appears in the range of 28.6 eV to 29.6 eV (Mitrovic et al., 2014) The chemical composition of Ge suboxides (GeO_x) and native oxide (GeO_2) were deconvoluted into Ge^{1+}, Ge^{2+}, Ge^{3+}, Ge^{4+} bonding states with binding energy shift of +0.8 eV, +1.8 eV, +2.6 eV and > +3 eV, respectively from the relative reference position of elemental Ge^0 at 29.0 eV. An additional peak denoted as Ge* was well fitted in between Ge^{2+} and Ge^{3+} with core level energy shift of +2.3 eV. The Ge^{4+} chemical bonding state denotes GeO_2 native oxide of Ge, since it has been projected to occur in the range of +3 to +3.4 eV (Dimoulas et al., 2010; Mitrovic et al., 2014; Sasada et al., 2009). The Ge* is represented as Ge_3N_4, which predictably appears in smaller range than that of Ge^{4+} (GeO_2) +3 eV in between +1.9 to +2.3 eV energy shift (Maeda et al., 2004, 2006; Minoura et al., 2013) The chemical energy shift of Ge sub-oxides lies at +0.8 eV, +1.8 eV and +2.6 eV can be denoted as Ge_2O, GeO and Ge_2O_3 according to the reported literature (J. Song et al., 2007). It is observed that, the content of Ge^{4+} native oxide GeO_2 and Ge* (Ge_3N_4) existed for all the investigated sample. It is notable that, there is a strong presence of volatile species of Ge^{2+} (GeO) for 5, 15, and 20 min samples except 10 min sample. Meanwhile, Ge^{3+} (Ge_2O_3) was found for 5 and 20 min while no Ge^{3+} (Ge_2O_3) were formed both 10 and 15 min samples. Moreover, the content of Ge^{1+} (Ge_2O) was detected for all the investigated samples except 15 min sample. This observation suggests the formation of amorphous interfacial layer which is evident from the presence of intermixing chemical bonding state of GeO_2 Ge_2O, GeO, Ge_2O_3 and Ge_3N_4.

The influence of various oxidation/nitridation durations upon thermodynamic stability of interfacial layer was investigated from the comparison of integrated area of the deconvoluted peaks as displayed in Fig. 4.41. Ge 3d spectra reveals that the sum of lower binding energy unstable phases of sub-stoichiometric GeO_x (Ge^{1+} and Ge^{3+}) and Ge^{2+}(GeO) are found more for 20 min sample followed by 5 min sample while these unstable phases reduced significantly at oxidation/nitridation duration of 10 min followed by 15 min. The content of Ge^{4+}(GeO_2) increases subsequently for 20 and 5 min samples whereas there is significant reduction of Ge^{4+}(GeO_2) for 10 and 15 min samples. Meanwhile, it is noticeable that, G*(Ge_3N_4) peaks substantially increases for 10 min sample followed by 15 min sample while Ge_3N_4 decreases subsequently for 5 and 20 min sample. It is noteworthy that, Ge^{4+}(GeO_2) are dominant compound for 5 and 20 min samples while Ge_3N_4 compound shows more pronounce appearance for 10 and 15 min samples. Hence, it is predicted that GeO_2 and Ge_3N_4 becomes more stoichiometric for 10 and 15 min samples due to the reduction of sub-stoichiometric unstable phases of GeO_x and GeO. It is believed that the content of Ge^{2+} (GeO) and Ge^{4+}(GeO_2) are more thermally unstable than those of Ge^{1+} (Ge_2O) and Ge^{3+} (Ge_2O_3) (Juan. Gao et al., 2017; D. Wang, He, Fang, et al., 2019). Consequently, presence of large amount Ge^{2+} (GeO) and Ge^{4+}(GeO_2) will cause sharp degradation on thermodynamic stability of gate stack. In addition, it is well documented that Ge_3N_4 is more thermodynamically stable with high-*k* permittivity in counter to GeO_2 (Kutsuki et al., 2009; Q. L. Li et al., 2011; Maeda et al., 2004). Accordingly, the interfacial layer rich with Ge−N bonding rather than Ge−O compounds will exhibit more thermally stable interfacial layer. Based on this assumption and above discussion it can be suggested that more thermally stable interfacial layer was formed for 10 and 15 min oxidation/nitridation since these samples consist of more stoichiometric Ge_3N_4 compound and fewer sub-stoichiometric GeO_2, GeO_x and GeO than those of 5 and 20 min samples. In addition, 10 min sample yielded the highest growth of Ge_3N_4 and

lowest growth of $Ge^{4+}(GeO_2)$ and GeO_x (Ge^{1+}) content without forming any $Ge^{2+}(GeO)$ species indicating most thermally stable interfacial layer among all the investigated samples. Conversely, 20 min sample exhibits the most thermally unstable interfacial layer since this sample reveals the highest density of $Ge^{4+}(GeO_2)$, $Ge^{2+}(GeO)$ and lowest growth of Ge_3N_4. The increase of sub-stoichiometric GeO_2 and volatile GeO species will have severe detrimental consequences on the electrical performance of the gate stack. The aspect of GeO_2 and GeO_x densification and Ge_3N_4 reduction has been explained in later section 3.6. Considering, 10 and 15 min samples fewer GeO_2, GeO_x formation and reduction of volatile GeO species are related to the pronounce growth of Ge_3N_4 compound. It is assumed that substantial incorporation of N^+ atom increases Ge_3N_4 density at this oxidation/nitridation durations which obstructed the O vacancy diffusion paths and also retarded the disproportionate transportation of O atom into the Ge substrate. Consequently, hindered the growth of unstable GeO_x compounds and reduced volatile GeO desorption while maintaining the integrity of GeO_2 (Copetti & Soares, 2016; Etcheverry et al., 2019). Therefore, based on the Ge 3d spectra observation it can be suggested that 10 min sample exhibits the superior configuration of stoichiometric contents with minority composition of GeO_x traps that might help in improving the device performance of the high-*k* interface.

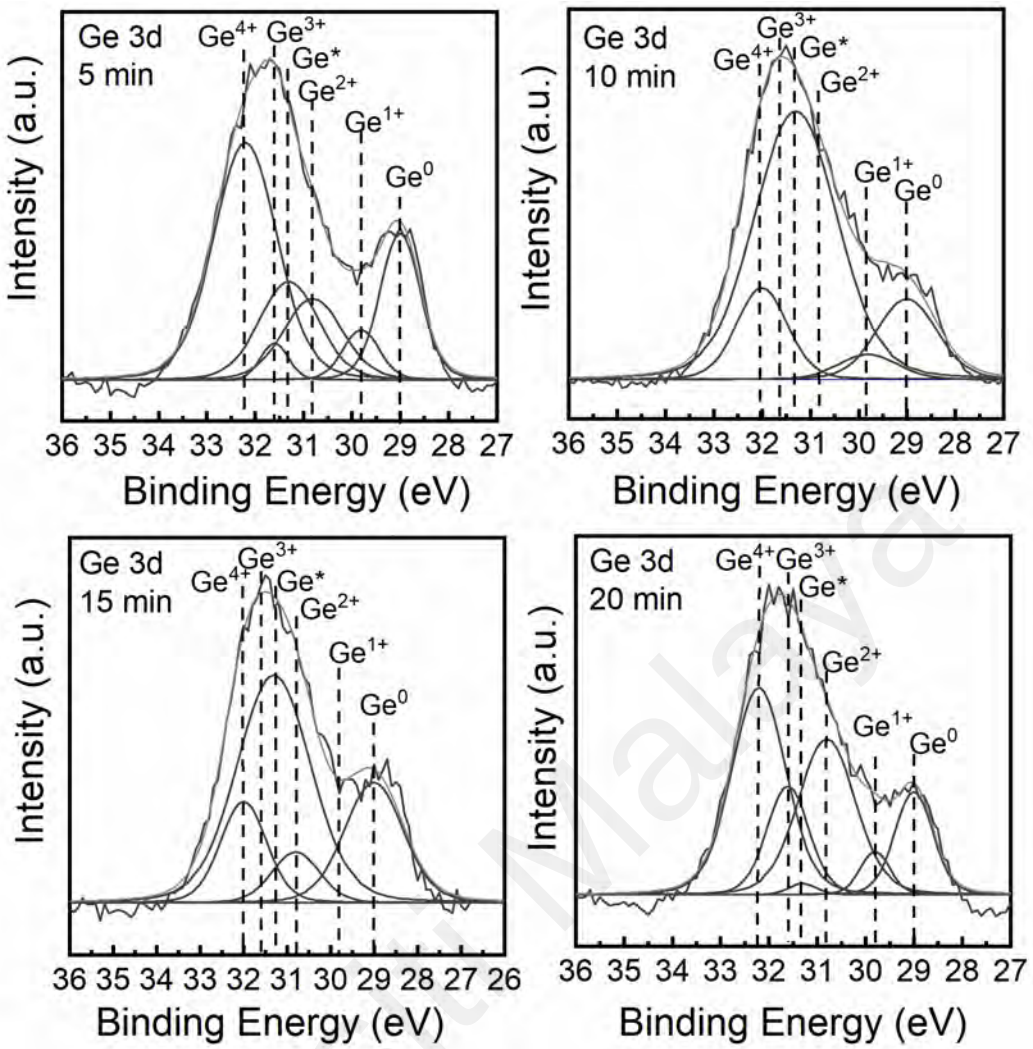

Figure 4.41: Deconvolution of O1s narrow band spectra for oxidized/nitrided sputtered Ho/Ge samples at different oxidation/nitridation durations (5 – 10) min.

Fig. 4.42 shows the O1s spectra for investigated samples at various oxidation/nitridation durations (5 – 20) min. The O1s spectra were deconvoluted into two peaks of Ho_2O_3 and Ge−O content. The Ho_2O_3 was well fitted in the lower binding energy site at peak position 529.80 eV and Ge−O content fitted well in the higher binding energy site at peak position 531.10 eV (J. Gao et al., 2017; Pan, Chang, et al., 2010). According to the O1s spectra 10 min sample exhibited the highest integrated peak area of Ho_2O_3 followed by 15 and 5 min samples while 20 min oxidation/nitridation duration induced lowest Ho_2O_3 peak area. This finding indicates that 10 min oxidation/nitridation is more favourable for higher Ho_2O_3 growth while longer time ~ 20 min oxidation/nitridation is less

convenient for the growth of Ho_2O_3. This observation supports the Ho_2O_3 growth prediction assumed in the Ho 4d spectra. In counter to Ho_2O_3 growth a reverse effect is observed for the growth of Ge−O species. It is observed that, Ge−O species growth is highest for 20 min sample followed by 5 min and 15 min samples while decreases substantially for 10 min sample with the lowest Ge−O growth. Since Ho_2O_3 peak reduced for 5 and 20 min samples hence, it is evident that the increased growth of Ge−O component at these oxidation/nitridation durations is due to large amount of O atoms diffusion from Ho_2O_3 dielectric itself toward the Ge substrate. The additional in-diffused O atoms contributed to form more unstable phases of GeO_2 or GeO_x interfacial layer compound between Ho_2O_3 dielectric film and substrate Ge. The Ge−O growth observation in O1s spectra is consistent with the Ge 3d spectra.

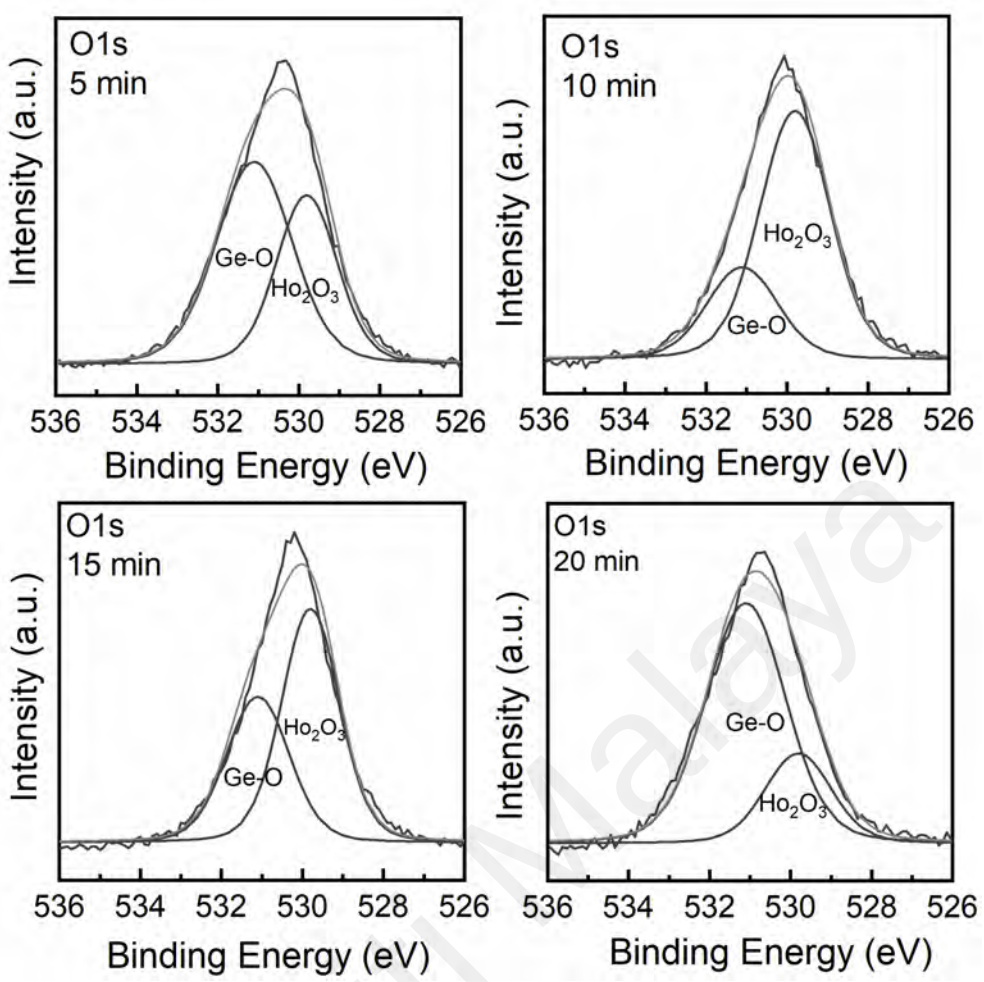

Figure 4.42: Deconvolution of O1s narrow band spectra for oxidized/nitrided sputtered Ho/Ge samples at different oxidation/nitridation durations (5 – 10) min.

The degree of oxidation/nitridation level for Ho_2O_3 growth were analyzed by plotting the Ho 4d binding energy shift with respect to oxidation/nitridation durations as depicted in Fig. 4.43. It is notable that Ho 4d binding energy are below the full oxidation level for all the investigated samples which indicates all samples are in under-oxidized condition. However, the 5 min and 20 min samples are located substantially in far distance below the full oxidation level which reveals more profound under-oxidized condition. On the other hand, the 10 min sample is closer to the full oxidation level followed by the 15 min sample which indicates increase of oxidation level for these samples. In conjunction with the *J-E* properties as described in Fig. 4.39, it can be inferred that the deep under-oxidation condition of Ho_2O_3 has an adverse impact on the electrical field breakdown.

The 10 min oxidized/nitrided duration condition generates moderate and controlled oxidation/nitridation rate leading to highest electrical field breakdown.

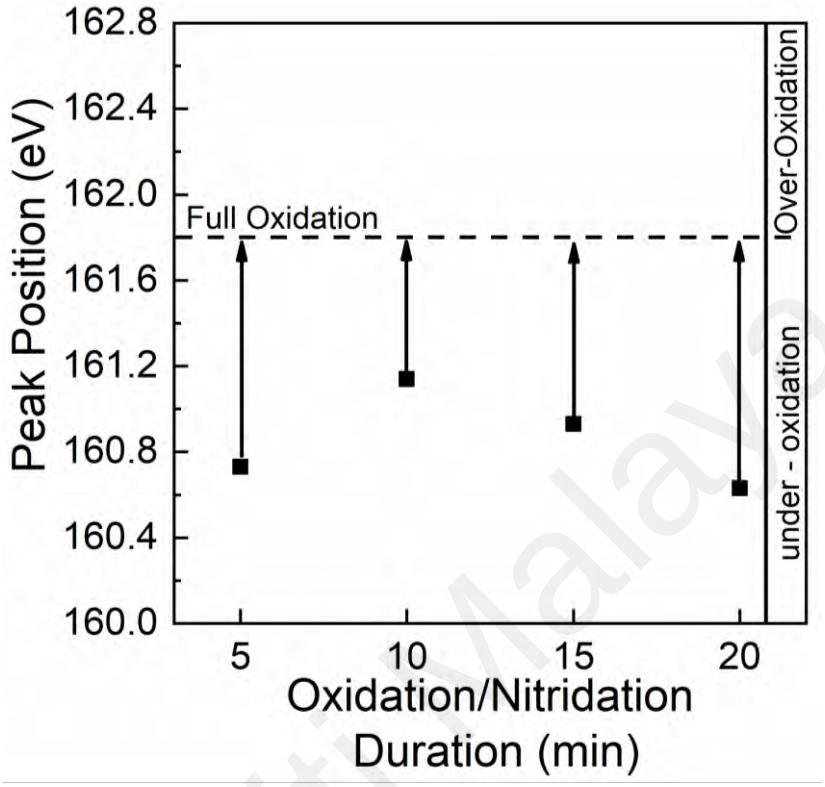

Figure 4.43: Peak position of Ho 4d narrow scan spectra as function of various oxidation/nitridation durations estimating the degree of oxidation level.

4.4.4 Band Alignment

The band alignment of Ho_2O_3/IL/Ge system has been developed by applying the same technique as described in section 4.3.2. Accordingly, XPS valance band (VB) spectra were used to estimate the valance band (VB) edges, E_v and valance band offsets (VBO) while energy bandgaps, E_g were extracted from O1s plasmon loss XPS spectra as shown in Fig. 4.44. The conventional tailed region observed at low binding energy site of VB spectra is being considered as Ge substrate signal. The reference position of VB edge, E_v (Ge) was considered at 0.10 eV and was assumed to be constant for various oxidation/nitridation duration (Cao et al., 2017). The VB edge, E_v of Ho_2O_3/IL was approximated by the linear extrapolation intercept of maximum negative slope leading edge in

VB spectra with the minimum edge of Ge substrate baseline as demonstrated in Fig. 4.44a.The measured VB edges, E_v of Ho_2O_3/IL with respect to substrate Ge were approximated to be 4.39, 4.77, 4.54 and 4.26 eV for 5 min, 10 min, 15 min and 20 min samples, respectively. The differences between VB edge, E_v of Ho_2O_3/IL and VB edge, E_v of Ge ascribed in Eq. 4.21 provides the VBO, $\Delta E_v$of Ho_2O_3/IL.

$$\Delta E_v\ (Ho_2O_3/IL) = E_v\ (Ho_2O_3/IL) - E_v\ (Ge) \qquad \text{(Equation 4.21)}$$

The VBO, ΔE_v (Ho_2O_3/IL) has been determined to be 4.29 eV, 4.67 eV, 4.44 eV and 4.16 eV for 5 min, 10 min, 15 min and 20 min samples, respectively. Finally, the conduction band offset (CBO), ΔE_c of Ho_2O_3/IL/Ge has been determined from Eq. 4.22.

$$\Delta E_c\ (Ho_2O_3/IL) = E_g\ \ (Ho_2O_3/IL) - E_g\ (Ge) - \Delta E_v\ (Ho_2O_3/IL) \qquad \text{(Equation 4.22)}$$

Where, E_g (Ho_2O_3/IL) and E_g (Ge) denotes energy bandgaps of Ho_2O_3/IL and substrate Ge, respectively. The energy bandgaps, E_g (Ho_2O_3/IL) was deduced by the intercept of linear extrapolation from respective O1s plasmon loss of XPS spectrums, for each of the oxidized/nitrided investigated samples as illustrated in Fig. 4.44b. The E_g (Ho_2O_3/IL) has been estimated to be 6.83 eV, 7.81 eV, 7.37 eV and 6.43 eV for oxidation/nitridation durations 5, 10, 15 and 20 min, respectively. The E_g (Ge) ~ 0.67 eV has been considered (Kamata, 2008). The band alignment schematic of Ho_2O_3/IL/Ge structure for different oxidation/nitridation durations is illustrated in Fig. 4.45. The CBO, ΔE_c (Ho_2O_3/IL) interface for various oxidation/nitridation durations were estimated 1.87 2.47, 2.26 and 1.60 eV for 5, 10, 15 and 20 min, respectively.

According to the band alignment schematic it is notable that all the investigated samples exhibited VBO and CBO above 1 eV which fulfilled the fundamental requirement of being an eligible candidate for high-*k* dielectric in MOS devices.

It has been reported that large conduction band offset facilitates in decreasing leakage current density and increasing electrical breakdown field (J. Gao et al., 2017; Wong & Cheong, 2011a). Accordingly, it is anticipated that the largest CBO, ΔE_c (Ho_2O_3/IL) obtained for 10 min sample restrained inclusion of electrons between Ho_2O_3/IL and Ge substrate which compensated the leakage current density and as well as enhanced the electrical breakdown field at this oxidation/nitridation duration. Contrariwise, for 20 min sample the decrease in ΔE_c (Ho_2O_3/IL) exaggerated the electron tunnelling that could exceed the barrier height between Ho_2O_3/IL and Ge interface and thereby causing highest leakage current density with lowest electrical breakdown field. Ultimately, continual decrease of CBO and VBO increases the gate leakage and lowers the breakdown field eventually deteriorating the device capability which is consistent with the *J-E* performance as shown earlier Fig. 4.39.

Furthermore, it is also observed that the energy bandgap, E_g (Ho_2O_3/IL) drops by 0.44 –1.38 eV for 5, 15 and 20 min with respect to the 10 min sample energy bandgap, $E_g \sim 7.81$ eV. The reduction of E_g is caused by the creation of defect gap states owing to GeO desorption and other GeO_x defects (Kita et al., 2009). Accordingly, it is predicted that higher density defect gap states have been generated into the Ho_2O_3/IL energy bandgap region through oxygen vacancies and Ge^{2+} defects diffusion induced from volatile GeO desorption and GeO_x interlayer causing energy bandgap reduction for 5, 15 and 20 min samples. Since 20 min sample induced highest GeO desorption and GeO_x defects consequently the smallest bandgap has been achieved. However, the energy bandgaps, $E_g \sim 6.43 – 7.81$ eV evaluated for Ho_2O_3/IL/Ge system is comparatively higher than typical Ho_2O_3 bandgap, $E_g \sim 5.3$ eV which can be contributed to the inclusion of interfacial layer, since the bandgap was calculated considering both (Ho_2O_3 + IL) layer.

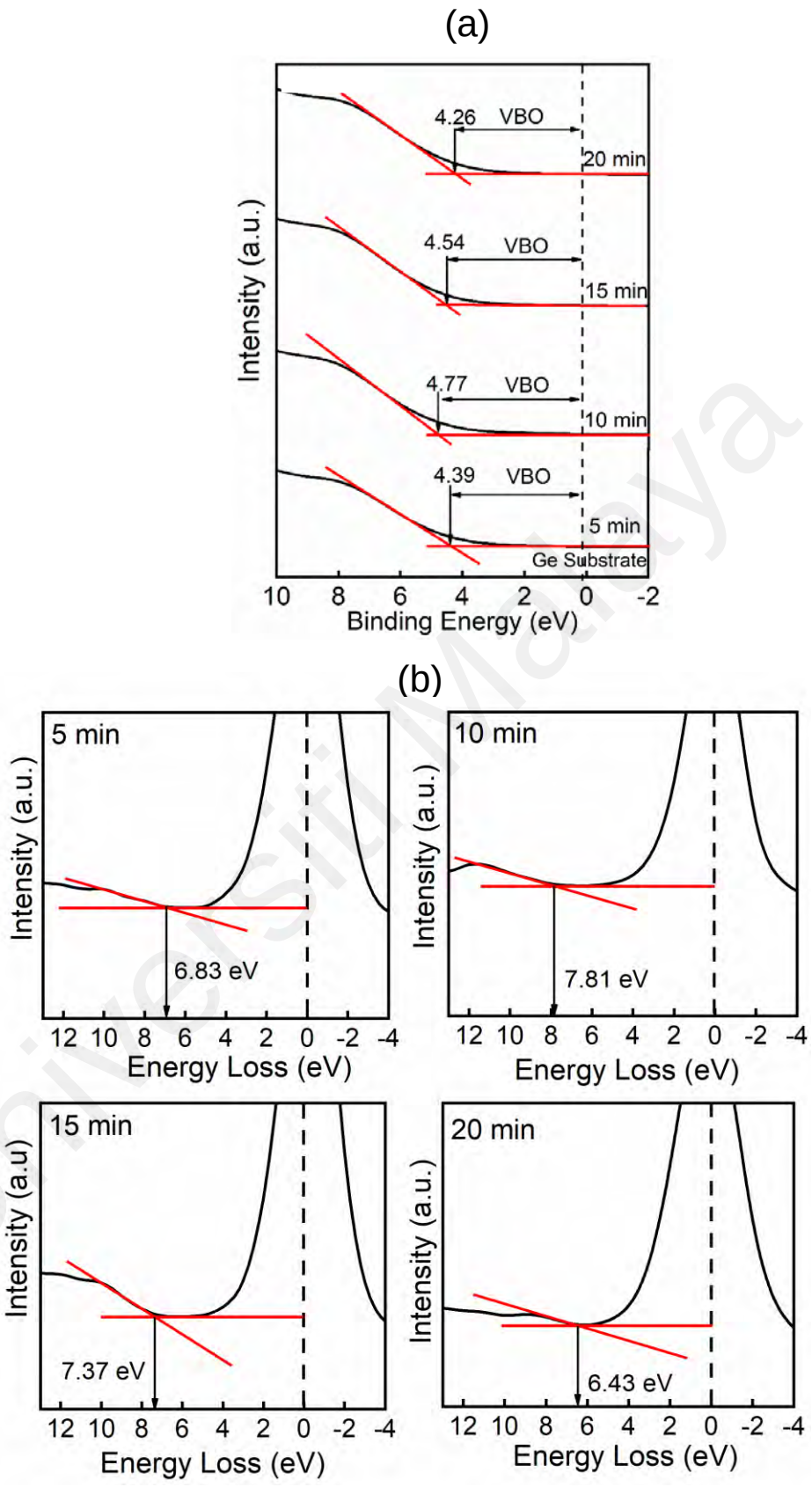

Figure 4.44: Valance band offset (ΔE_v) and energy bandgap (E_g) Ho_2O_3/IL/Ge structure at various oxidation/nitridation durations (5 – 20) min (a) Extraction of valance band edge, E_v and VBO estimation from valance band spectra (b) Energy bandgap extraction from O1s plasmon loss XPS spectrum.

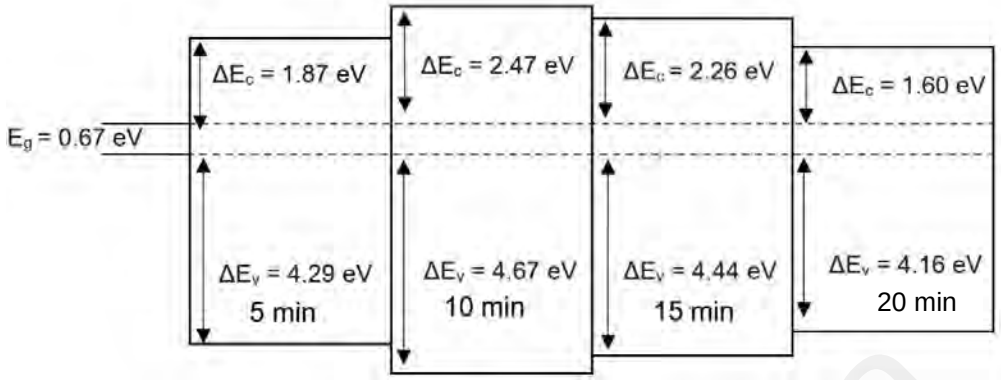

Figure 4.45: Band alignment schematic Ho_2O_3/IL/Ge stack for various oxidation and nitridation durations (5 – 20) min.

4.4.5 HRTEM Analysis

In order to justify the suitability of Ho_2O_3 as high-*k* gate oxide material with the MOS scaling limit it is imperative to understand the effect of oxidation/nitridation process on the physical thickness of the functioning Ho_2O_3/Ge gate stack. Fig. 4.46 displays the cross-sectional images acquired from HRTEM analysis for the oxidation/nitridation durations 10 min and 20 min. It has been spotted that both the samples comprise two distinct layers. The top layer at the surface is considered to be dielectric Ho_2O_3 layer since it is located at far distance position from substrate Ge baseline. Meanwhile the layer sandwiched between Ho_2O_3, and the Ge substrate is considered as interfacial layer (IL) as it is relatively closer to Ge substrate. Based on the XPS and XRD analysis it is considered that the interfacial layer is combination of various Ge−O (i.e. GeO_2 and GeO_x) compounds and Ge_3N_4. It is apparent from Fig. 4.46 that Ho_2O_3 dielectric thickness layer increases for 10 min sample while decreases for 20 min sample. On the contrary, interfacial layer decreases for 10 min sample while interfacial increases for 20 min sample. The thickness of Ho_2O_3 layer measured from HRTEM images are 4.33 nm and 3.60 nm for 10 min and 20 min samples, respectively. Meanwhile the interfacial layer is measured to be 4.39 nm

and 6.18 nm, for 10 min and 20 min samples, respectively. Accordingly, it can be suggested that the oxidation/nitridation rate of forming dielectric oxide is higher for 10 min sample while oxidation/nitridation rate of forming interfacial layer is higher for the extended duration of 20 min sample. This finding also indicates that interfacial layer becomes dominant during longer oxidation/nitridation. The total thickness of 5 min and 15 min samples were approximated using linear regression plot as displayed in Fig. 4.47, assuming the total thickness of the gate stack increases linearly with the increment of oxidation/nitridation duration. The total thickness approximated from linear regression plot is 8.22 nm and 9.18 nm for 5 and 15 min, respectively while the total thickness measured from the HRTEM images Figure 12 was 8.72 nm and 9.78 nm for 10 and 15 min, respectively.

Furthermore, the crystallinity of the Ho_2O_3/IL film was also verified by analyzing diffraction pattern of HRTEM images. Fast Fourier Transform (FFT) measurement was conducted over HRTEM images using ImageJ software in order to obtain the diffraction pattern displayed as inset image in Fig. 4.46. Presence of cloudy spots pattern in Ho_2O_3 layer as well as in interfacial layer confirms that both of these layers are in amorphous phase for both 10 min and 20 min samples. Moreover, both the sample reveals polycrystalline structure of Ge substrate which has been validated by the existence of multiple spotted FFT image diffraction pattern.

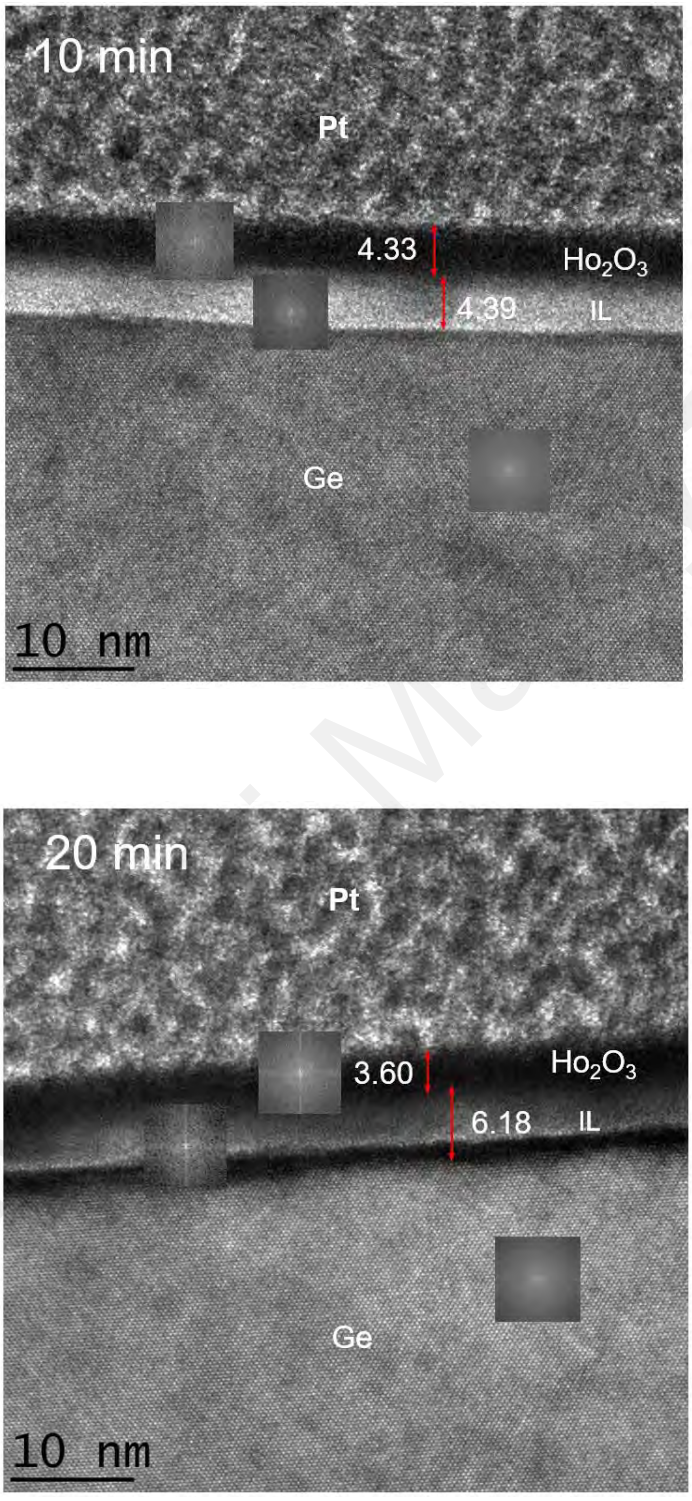

Figure 4.46: Structural cross-sectional morphology obtained from HRTEM for oxidized/nitrided sputtered Ho/Ge samples at 10 min and 20 min durations. Inset images shows FFT diffraction.

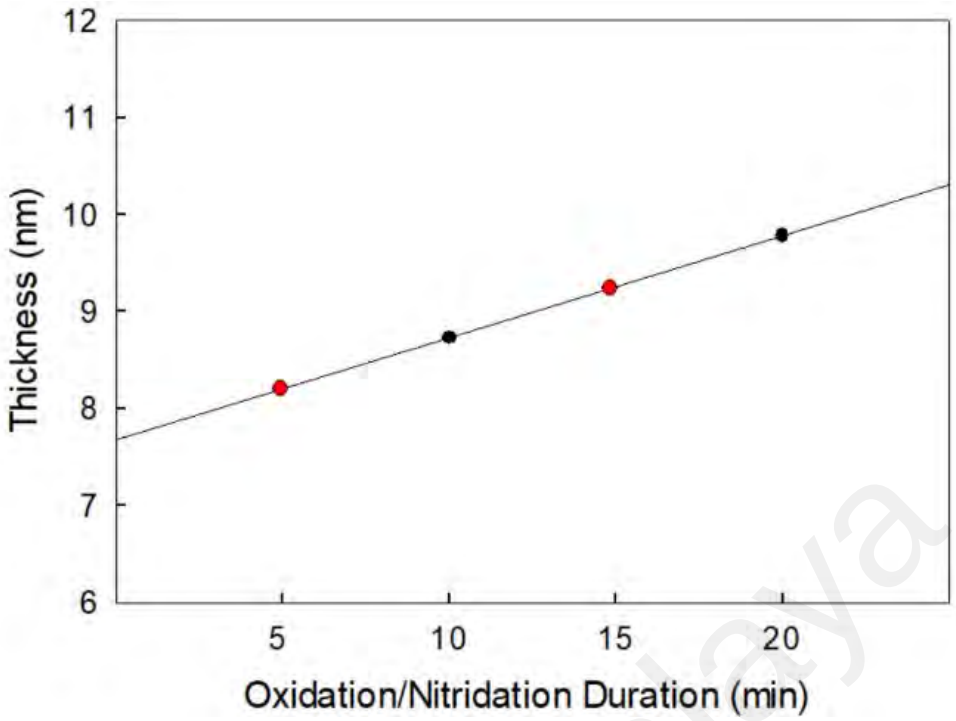

Figure 4.47: Determination of Ho_2O_3/IL/Ge stack physical thickness for investigated samples at various oxidation/nitridation durations (5 – 10) min.

4.4.6 Oxidation/Nitridation Mechanism Model

Oxidation and nitridation mechanism process for Ho_2O_3/IL/Ge stack has been established based on the correlation of HRTEM and XPS analysis considering oxidized/nitrided samples at duration of 10 and 20 min as illustrated in Fig. 4.48. The schematic of Ho sputtered on Ge substrate before thermal oxidation/nitridation is shown in Fig. 4.48a. Initially, during the beginning of oxidation/nitridation process N_2O diffused from the atmosphere and reacted with the top surface sputtered Ho of the Ge substrate following Eq. 4.23

$$2Ho + 3N_2O(g) \rightarrow Ho_2O_3 + 3N_2(g) \qquad \text{(Equation 4.23)}$$

Afterwards, N_2O received adequate energy to diffuse throughout the Ho_2O_3 film layer while forming interfacial layer comprising GeO_2 and Ge_3N_4 compounds for both the samples, by the reaction of substrate Ge and in-diffused N_2O gas according to Eq. 4.24. Corresponding to XPS analysis substantial reduction of GeO_2 and an additional growth of Ge_3N_4 was observed for 10 min. Hence, at these oxidation/nitridation durations Ge dangling bonds from GeO_2 network reacted with the atmospheric in-diffused N_2O generating Ge_3N_4 rich interfacial layer according to Eq. 4.25. Meanwhile, the residual product of O atom in Eq. 4.25 out-diffuses toward the Ho_2O_3 interface which filled up the oxygen vacancy of Ho_2O_3 contributing to the thicker dielectric layer for 10 min oxidation/nitridation duration. On the other hand, GeO_2 rich interfacial layer was revealed for 20 min sample. Due to longer oxidation time large extent of O atom in-diffused from the Ho_2O_3 film which reacted with the out-diffused Ge atom from unstable phases of Ge_3N_4 and GeO_2 network producing large amount of GeO_2 compound in the interfacial layer according to Eq. 4.26.

$$4Ge + 2N_2O\ (g) \rightarrow GeO_2 + Ge_3N_4 \qquad \text{(Equation 4.24)}$$

$$6GeO_2 + 4N_2O\ (g) \rightarrow 2Ge_3N_4 + 8O_2\ (g) \qquad \text{(Equation 4.25)}$$

$$3Ge + 3O_2\ (g) \rightarrow 3GeO_2 \qquad \text{(Equation 4.26)}$$

Considering, the 20 min sample once GeO_2 is formed by the Eq. 4.24 and Eq. 4.26 afterwards GeO_2 reacting with the substrate Ge causing GeO (g) desorption due to oxygen vacancy (V_o) diffusion through GeO_2 interface by redox reaction of Eq. 4.27 (Kita et al., 2008). Moreover, this detrimental reaction is also reinforced by the enhanced O atom in-diffusion from Ho_2O_3 film interface consequentially generated severely defective Ho_2O_3 film interface as shown in Figure 4.48c.

$$GeO_2 + Ge \rightarrow 2GeO\ (g) \qquad \text{(Equation 4.27)}$$

Meanwhile, GeO (g) desorption disappears for 10 min sample. It has been suggested that when any material is deposited above GeO_2 that retards GeO (g) desorption tends to annihilate oxygen vacancy diffusion (V_o) following the disproportionation reaction of Eq. 4.28 (S. K. Wang, Liu, & Toriumi, 2012).

$$2GeO \rightarrow GeO_2 + Ge \qquad \text{(Equation 4.28)}$$

Hence, at this oxidation/nitridation duration generation of Ge_3N_4 rich interfacial compound suppressed the desorption of volatile GeO by blocking oxygen vacancy diffusivity through the Ho_2O_3/IL interface initiating reverse GeO reaction ascribed in Eq. 4.28 Accordingly, less defective Ho_2O_3 interface was obtained for 10 min sample as shown in Fig. 4.48b.

Furthermore, existence of Ge_2O, Ge_2O_3 and reduction of Ge_3N_4 was evident for 20 min sample in XPS analysis. It is assumed that Ge_3N_4 bonding deteriorated by producing additional Ge suboxides Ge_2O and Ge_2O_3 due to the reaction between in-diffusing O atom from Ho_2O_3 and out-diffusing Ge atom from Ge_3N_4 according to Equ.4.29 and Eq. 4.30. Unlike 20 min sample, small amount of Ge_2O detected for 10 min sample which was formed by the reaction between out-diffused Ge from GeO_2 network or Ge wafer and in-diffused O atom from Ho_2O_3 dielectric as shown in Eq. 4.31. However, these reactions induced additional defects in the interfacial layer for both the samples.

$$4Ge_3N_4 + 3O_2\,(g) \rightarrow 6Ge_2O + 8N_2\,(g) \qquad \text{(Equation 4.29)}$$

$$4Ge_3N_4 + 9O_2\,(g) \rightarrow 6Ge_2O_3 + 8N_2\,(g) \qquad \text{(Equation 4.30)}$$

$$4Ge + O_2\,(g) \rightarrow 2Ge_2O \qquad \text{(Equation 4.31)}$$

Based on this model it can be summarized that sufficient oxidation/nitridation of Ho_2O_3 at 10 min duration minimized the inter-diffusion of O and Ge atom causing thicker Ho_2O_3 layer with less GeO_x defect and more consolidated Ho_2O_3/IL/Ge gate stack is formed. When the oxidation/nitridation is extended to 20 min a reverse phenomenon has been observed where interfacial layer becomes thicker since diffusion rate of O and Ge atom increases due to longer oxidation/nitridation time. Therefore, atoms become less consolidated causing more defective Ho_2O_3/IL interface.

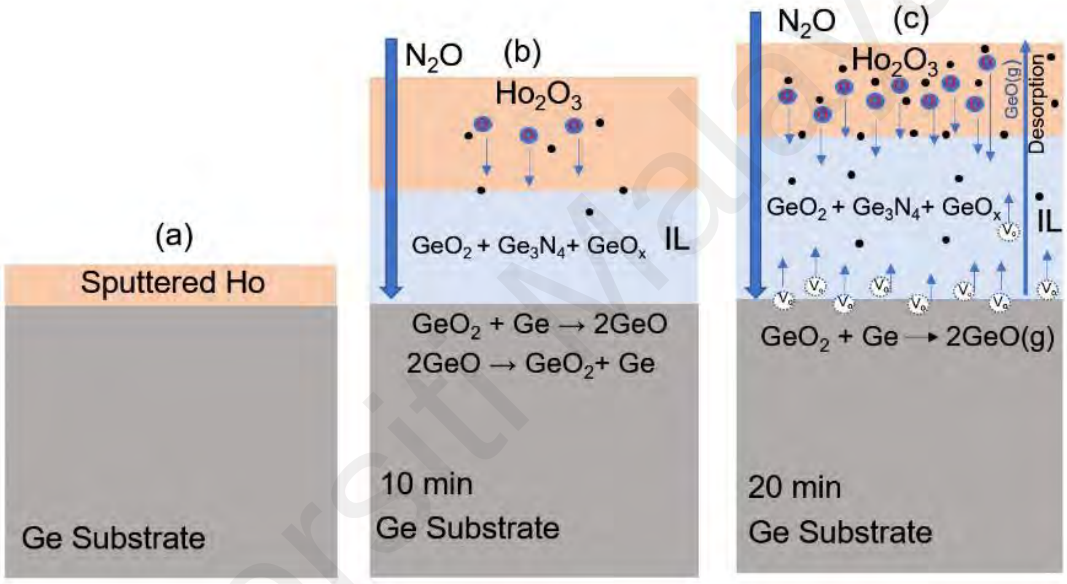

Figure 4.48: Oxidation/nitridation mechanism model for sputtered Ho/Ge after subsequent oxidation/nitridation at different duration 10 and 20 min. Dotted circle represents oxygen vacancies, blue filled circle denotes in-diffusing oxygen and IL is interfacial layer.

4.4.7 C-V Characteristics

Fig. 4.49 elucidates the typical current – voltage (*C–V*) characteristics for different oxidation/nitridation durations 5min, 10 min, 15 min, 20 min where gate voltage of 6 V to +1 V has been swept directionally at high frequency of 1 MHz. It is observed that the capacitance at accumulation region increases as the oxidation/nitridation extended from 5 min to 10 min but decreases while the duration incremented from 10 min to 20 min. The highest accumulation capacitance is recorded for 10 min followed by 15 and 5 min samples while 20 min oxidation/nitridation duration exhibited the lowest capacitance. The variation of accumulation capacitance can be explained based on the formula of Eq. 4.10 (Goley & Hudait, 2014; Wong & Cheong, 2011b). The Eq. 4.10 shows that oxide capacitance is proportional to $\frac{k}{t_{ox}}$. Accordingly, the degree of capacitance increases with higher dielectric constant k value and reduction of total film thickness, t_{ox} = Ho_2O_3 + IL. Based on this relationship the highest capacitance for 10 min sample can be attributed to the higher dielectric constant, k (inset of Fig. 4.49) and reduction of total oxide thickness t_{ox} (Fig. 4.46).

The effective dielectric constant k_{eff} was evaluated using Eq. 4.10 where C_{ox} has been achieved from C-V curve while total physical oxide thickness (Ho_2O_3 + IL) was extracted using HRTEM images. Inset image inserted in Fig. 4.49 reveals the correlation between effective dielectric constant k_{eff} value and accumulation capacitance with respect to various oxidation/nitridation durations. It is noticeable that the changes of accumulation capacitance followed the same trend according to the of variation effective dielectric constant k_{eff}. The calculated k_{eff} values for Ho_2O_3/ IL/Ge are 9.50, 13.60, 13.09 and 8.52 for 5, 10, 15 and 20 min samples, respectively. As reported by Pan et al., (2010) the k value of sputtered Ho_2O_3 deposited on Si substrate ranges between ~ 6.5-10.1. Paivasaari et al., (2005) reported the k value of ~ 9.9 for Ho_2O_3 with respect to SiO_2/Si

substrate. However, the 20 min sample min has a lower k_{eff} value which might come from the higher composition of low-*k* (Ge−O) interfacial compound and lower composition of high-*k* Ho_2O_3 compound. On the other hand, improvement of k_{eff} value for 10 min sample is due to better thermal stability of Ho_2O_3/IL interface caused by the densification of high-*k* Ho_2O_3 compound and reduction of low-*k* (Ge−O) interfacial compound. In contrast with observation of XPS analysis (Fig. 4.43) the k_{eff} value increases with higher Ho_2O_3 density while k_{eff} value reduces for higher Ge−O density. Therefore, the dielectric constant, *k* of Ho_2O_3/ IL/Ge structure is much dependent on the growth rate of high-*k* Ho_2O_3 film and low-*k* (Ge−O) interfacial content during the oxidation/nitridation process.

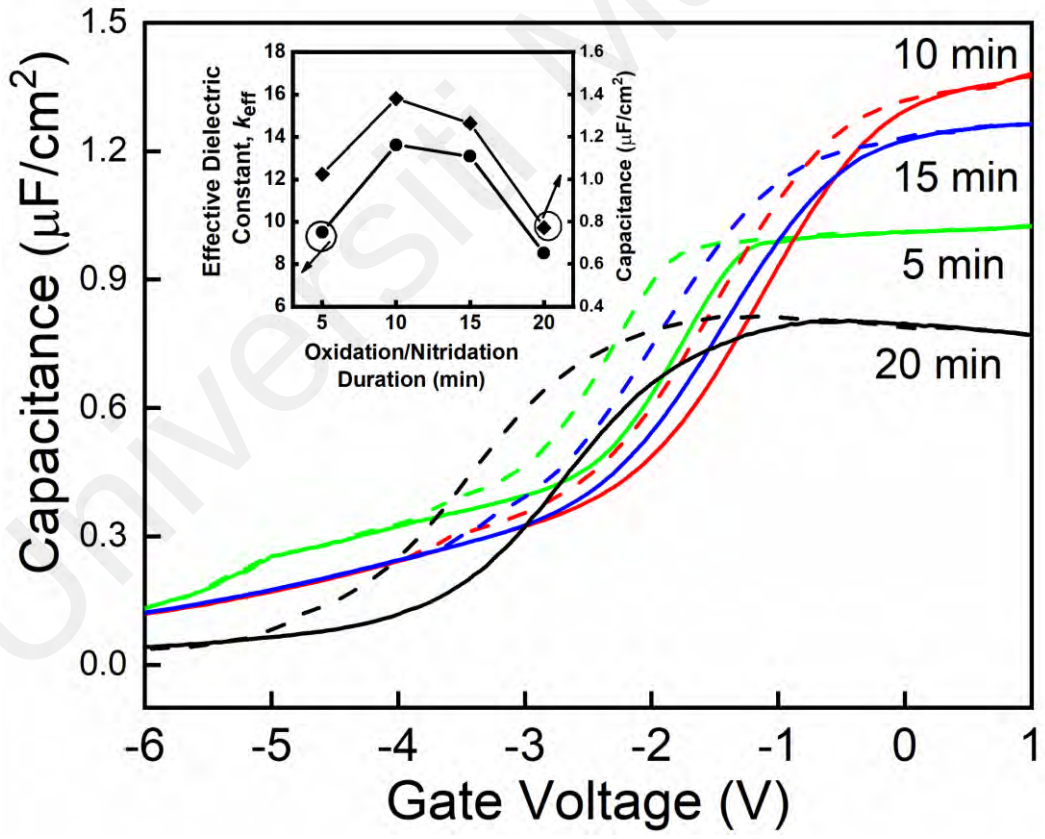

Figure 4.49: (a) *C–V* characteristics of Ho_2O_3/IL/Ge MOS capacitors measured at 1 MHz for bidirectionally swept gate bias for various oxidation/ nitridation durations (5 min, 10 min, 15 min, and 20 min). The inset displays effective dielectric constant and accumulation capacitance and effective dielectric constant as function oxidation and nitridation durations.

From the *C-V* plot, it is apparent that depletion region appeared in the negative bias region for all the investigated capacitors. The negative shift of flatband voltage, V_{FB} confirms the accumulation of positive oxide charges accumulated in the Ho_2O_3 interface during the thermal oxidation/nitridation process (Taoka et al., 2011). The effective positive charges Q_{eff} are calculated using the Eq. 4.20. The calculated effective positive charges for all the oxidation/nitridation durations are shown in Fig. 4.50. The source of positive oxide charges is possibly related to the large amount of defects existing in the Ho_2O_3 interface generated from dangling bonds and oxygen vacancies (Deng et al., 2011; Pan, Chang, et al., 2010). The 10 min sample exhibits the lowest positive oxide charge $Q_{eff} \sim 8.80 \times 10^{12}$ cm^{-2} and 20 min sample exhibit the highest positive oxide charges of $Q_{eff} \sim 1.41 \times 10^{13}$ cm^{-2}. The compensation of positive oxide charges for 10 min sample indicates that Ho_2O_3 has gained more homogenous structure at this oxidation/nitridation condition due to reduction of oxygen vacancies and other oxygen related defects.

Furthermore, hysteresis phenomena have been observed for all the investigated samples ranges between 343 mV – 882 mV as shown in Figure 4.51. It has been reported that presence of charged slow traps located in the border of high-*k* and interfacial layer interface or in the bulk of high-*k* dielectric causes hysteresis effect (Ke et al., 2018; Wong & Cheong, 2011b). Hence, evaluating the amount of slow trap density (*STD*), Q_{it} can explain the variation of hysteresis voltage since slow trap density is indirectly related with the hysteresis behaviour based on Eq. 4.11. According to the estimated *STD*, (Q_{it}) as displayed in Fig. 4.50 it is identified that 10 min sample yielded the lowest $Q_{it} \sim 2.93 \times 10^{12}$ cm^{-2} while the 20 min sample exhibited the highest $Q_{it} \sim 4.24 \times 10^{12}$ cm^{-2}. Based on the findings of *STD* and hysteresis voltage displayed in Fig. 4.50 and Fig. 4.51 it can be remarked that hysteresis voltage reveals a proportional relationship with

the slow trap density. Accordingly, lowering of *STD* compensated hysteresis voltage for 10 min oxy-nitrided sample while generation of large amount slow trap density during 20 min oxidation/nitridation enhanced the hysteresis phenomena. The origin of slow traps is predicted due to out-diffusion of N^+ atom and also tunnelling of carrier charges (electrons or holes) from Ge substrate (Ke et al., 2018; Misra et al., 2006) Hence, the increase of slow traps for 20 min sample is believed due to excessive N^+ atom piling up towards the dielectric interface and large amount of carrier charges transportation from Ge substrate into the Ho_2O_3 film or Ho_2O_3/IL interface. Furthermore, the variation of *STD* and Q_{it} in response to various oxidation/nitridation duration follows the identical trend as Q_{eff}.

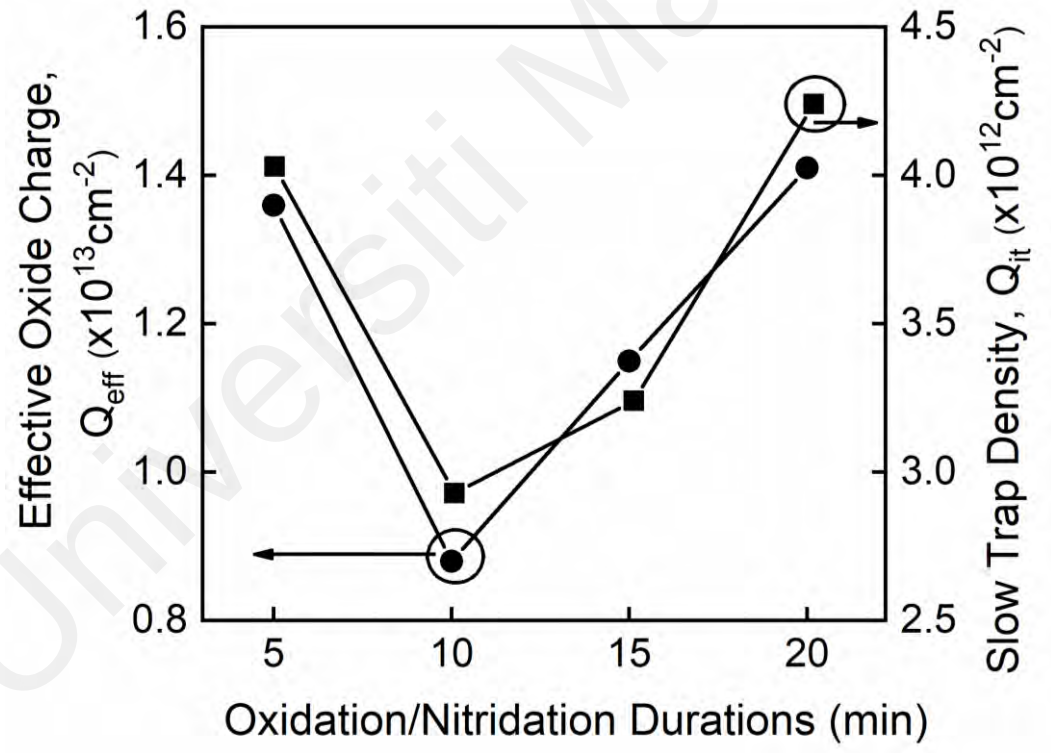

Figure 4.50: Amount of Effective oxide charge, Q_{eff} and slow trap density, Q_{it} existing in the Ho_2O_3/IL/Ge MOS capacitors for oxidized/nitrided samples at durations (5 – 20) min.

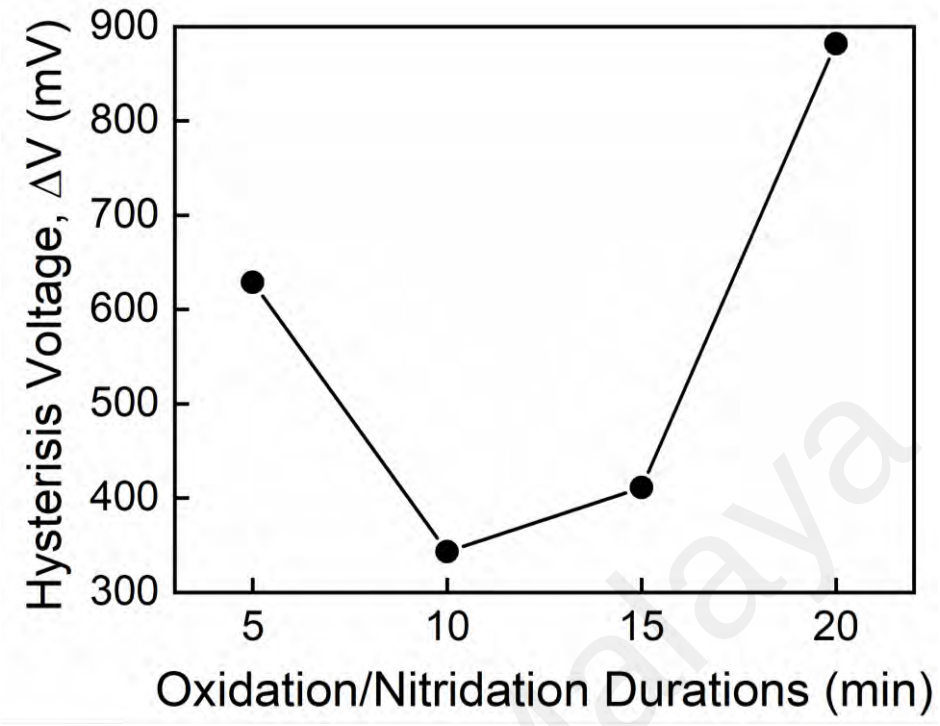

Figure 4.51: Changes in hysteresis voltage with the variation of oxidation and nitridation durations (5 – 20) min for Ho_2O_3/IL/Ge MOS capacitors.

Fig. 4.52 illustrates average interface trap density, D_{it} with respect to trap energy level ($E_C - E$) for various oxidation and nitridation durations (5 – 20) min. The Terman method has been employed for approximation of average interface trap density D_{it} for the oxidized/nitrided Ho_2O_3/IL/Ge MOS capacitors according to Eq. 4.12. According to the D_{it} vs ($E_C - E$) curves, oxidized/nitrided film of 10 min duration poses the lowest average interface trap density, $D_{it} \sim 10^{13} - 10^{14}$ $eV^{-1}cm^{-2}$ at ($E_C - E$) = 0.09 – 0.27 eV. For the estimation of total interface trap density D_{total} of the energy range ($E_C - E$), area under D_{it} – ($E_C - E$) was determined which is portrayed as inset image in Fig. 4.52. The lowest D_{total} was found for 10 min sample approximated to be $1.97 \times 10^{13} cm^{-2}$ while extending the oxidation/nitridation to 20 min exposed the highest $D_{total} \sim 6.51 \times 10^{13}$ cm^{-2}. The variability trend of D_{total} with respect to oxidation/nitridation duration is similar with the variation of Q_{eff} and Q_{it}.

Considering the root of interfacial traps, it is predicted that structural defect comprising oxygen-defect (OD) and Ge dangling bonds that existed between dielectric film and Ge substrate are primarily associated with the charge capturing process for the MOS interface (Bethge et al., 2014). It is believed that decomposition of GeO_2 and desorption of GeO is the major source for oxygen vacancy incorporation and insertion of dangling or broken bonds (Kita et al., 2008; S. K. Wang et al., 2010). In contrast with XPS analysis the minimum interface trap density for 10 min sample should be attributed to the formation of Ge_3N_4 rich interfacial layer which effectively blocked the GeO desorption as well as acted as diffusion barrier against oxygen in-diffusion and Ge out-diffusion. As a result, oxygen vacancies and Ge dangling bond (DB) has been minimized that lead to decrease the interface trap density. Moreover, tendency of forming pure Ho_2O_3 compensated oxygen deficiency and passivated growth of undesirable GeO_x interlayer content, which also contributed to reduce interface traps at this oxidation/nitridation duration. On the contrary, higher interface trap density for 20 min sample indicates enhancement of unsaturated oxygen vacancies and surplus of Ge dangling bonds, which is caused by the bond weakening of interfacial Ge_3N_4 compound and excessive oxygen in-diffusion from Ho_2O_3 film. Consequently, strengthened the GeO (g) desorption and induced large amount of GeO_x defects leading to higher interface traps at the Ho_2O_3 and Ho_2O_3/IL interface. In addition, formation of sub-stoichiometric Ho_2O_3 also reinforced the charge trapping sites in the dielectric/IL interface.

Comparing with previous literature the lowest average interface trap density, D_{it} $\sim 9.39 \times 10^{13}$ $eV^{-1}cm^{-2}$ (at mid $E_C - E = 0.2$ eV) of Ho_2O_3/IL/Ge stack for 10 min oxidized/nitrided sample value is higher than the reported post annealed Ho_2O_3/Si interface D_{it} $\sim 3.00 \times 10^{11}$ $eV^{-1}cm^{-2}$ (Pan, Chang, et al., 2010). However, a lower $Q_{eff} \sim 8.80 \times 10^{12}$ cm^{-2}, $Q_{it} \sim 2.93 \times 10^{12}$ cm^{-2}, $D_{it} \sim 10^{13}$ $eV^{-1}cm^{-2}$ (at mid $E_C - E =$ 0.2 eV) and $D_{total} \sim 1.97 \times 10^{13}$ cm^{-2} has been acquired in this work in counter to

thermally oxidized Sm_2O_3/Si interface (Goh et al., 2017b) [$Q_{eff} \sim 2.81 \times 10^{13}$ cm^{-2}, $Q_{it} \sim 5.56 \times 10^{12}$ cm^{-2} , $D_{it} \sim 10^{14}$ eV^{-1}cm^{-2} (at mid $E_C - E = 0.2$ eV) and $D_{total} \sim 7.30 \times 10^{13}$ cm^{-2}]. Based on the above discussion it can be concluded that 10 min oxidation/nitridation duration holds the superior electrical properties of *C-V* characteristics for Ho_2O_3/IL/Ge gate stack.

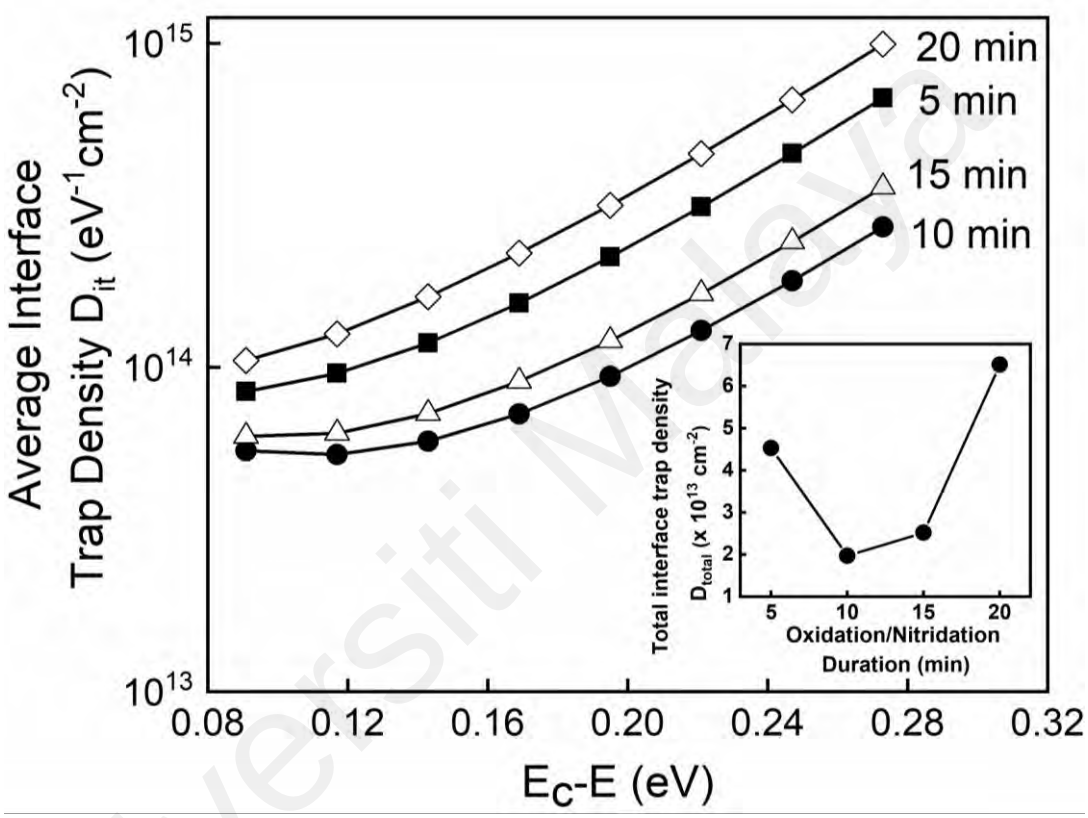

Figure 4.52: Average interface trap density D_{it} and total interface density contained in Ho_2O_3/IL/Ge MOS capacitors at different oxidation/nitridation durations (5 – 20) min.

4.5 Comparison Between Oxidized/Nitrided Sputtered Sm/Ge and Ho/Ge Stack

The comparison of Sm_2O_3/Ge and Ho_2O_3/Ge stack has been demonstrated by comparing the physical and electrical properties obtained at their optimized thermal oxidation/nitridation deposition condition in N_2O ambient. After conducting thermal oxidation/nitridation of sputtered Sm/Ge and Ho/Ge at different temperatures and durations the best possible thermal deposition condition has been achieved as shown in Table 4.1. The optimized thermal oxidation/nitridation duration at constant temperature 400 °C for oxidized/nitrided Sm/Ge is achieved at 15 min while 10 min thermal oxidation/nitridation duration has been optimized for oxidized/nitrided sputtered Ho/Ge. The comparison has been considered based on the physical and electrical properties achieved at optimized condition.

Table 4.1: Optimum thermal oxidation/nitridation durations for sputtered Sm/Ge and Ho/Ge at constant 400 °C.

Thermal Oxidation and Nitridation	Oxidation Nitridation Ambient	Constant Temperature (°C)	Duration (min)
Sputtered Sm/Ge	N_2O	400	15
Sputtered Ho/Ge		400	10

4.5.1 Comparison of Physical Properties

The comparison of several physical properties for thermally oxidized/nitrided sputtered Sm/Ge and Ho/Ge includes the findings of XRD, XPS and HRTEM are summarized in Table 4.2. From the comparison of the findings of XRD it is found that after oxidation/nitridation in N_2O ambient trigonal phase of Sm_2O_3 has been formed with a preferential plane orientation of (003) for oxidized/nitrided Sm thin film while cubic Ho_2O_3 phase structure corresponding to preferential plane of (631) is being produced for

the oxidized/nitrided Ho thin film. Moreover, from XRD analysis it is also found that Ho_2O_3 introduces larger crystallite size than Sm_2O_3 while both Sm_2O_3 and Ho_2O_3 oxides comprises negative micro-strain of same value. According to the XPS analysis for oxidized/nitrided Sm/Ge in N_2O ambient, exposed the formation of stoichiometric Sm_2O_3 with an interfacial layer (IL) consisting of sub-stoichiometric mixed compounds $Sm_xGe_yO_z$, native oxide GeO_2, suboxides GeO_x, with Ge_3N_4 has been formed. Meanwhile, sub-stochiometric Ho_2O_3 along with IL of intermixing sub-stoichiometric content of native oxide GeO_2, sub-oxides GeO_x and Ge_3N_4. Unlike interfacial Sm−O−Ge of Sm_2O_3/IL/Ge stack no such interfacial rare earth germanate (Ho−O −Ge) was formed in the Ho_2O_3/IL/Ge stack. Moreover, the band alignment mapping extracted using XPS valence spectra and O1s plasmon loss XPS spectra it is found that Sm_2O_3/IL interface exhibited higher CBO, ΔE_c than Ho_2O_3 /IL interface with respect to Ge substrate. From the band offset mapping it is also noticed that Sm_2O_3/IL exposed more symmetrical band alignment than the Ho_2O_3/IL interface. Although Ho_2O_3/IL interface exhibited larger energy band gap, E_g than Sm_2O_3/IL but the reduction of ΔE_c for Ho_2O_3 /IL interface indicates that relatively more defect gap states has been introduced between the conduction band edge of Ho_2O_3/IL interface and substrate Ge. Eventually, it is conspicuous that thermally oxidized/nitrided sputtered Sm/Ge generates more thermally stable Sm_2O_3/IL interface than that of Ho_2O_3/IL interface. Lastly, coming to the HRTEM analysis it is found that both oxidized/nitrided Sm/Ge and Ho/Ge exhibits distinguishable bulk oxide and interfacial layer where Sm_2O_3/IL/Ge stack exhibited the lower total oxide thickness including lower thickness of both bulk and interfacial layer compared to Ho_2O_3 /IL/Ge stack. Both of these stacks induced amorphous interface for both bulk oxide and interfacial layer.

Table 4.2: Comparison of physical properties between thermally oxidized/nitrided sputtered Sm/Ge and Ho/Ge.

Analysis Technique	Features	Thermally oxidized/nitrided sputtered Sm/Ge	Thermally oxidized/nitrided sputtered Ho/Ge
XRD	Phase of Oxide	Trigonal-Sm_2O_3	Cubic-Ho_2O_3
	Plane Orientation	(100), (003), (103), (110), (101) & (200)	(222), (631), (440), (411), (512), (431), (602), (541) & (622)
	Preferred Plane orientation	(003)	(631)
	Crystallite size (D) (nm)	32.48	41.25
	Micro-strain	- 0.0004	- 0.0004
XPS	Chemical Composition of bulk	Sm−O	Ho−O
	Chemical Composition of IL	$Sm_xGe_yO_z$, Ge−O & Ge−N	Ge−O & Ge-N
	Dielectric Stoichiometry	Stoichiometric Sm_2O_3	Sub-stoichiometric Ho_2O_3
	E_g (eV) of Sm_2O_3/IL & Ho_2O_3/IL	6.25	7.81
	ΔE_c (eV) of Sm_2O_3/IL & Ho_2O_3/IL	2.60	2.47
	ΔE_v (eV) of Sm_2O_3/IL & Ho_2O_3/IL	2.98	4.67
HRTEM	Bulk thickness t_{bulk} (nm)	3.56	4.33
	Interfacial layer thickness, t_{IL} (nm)	2.44	4.39
	Total oxide thickness, t_{ox}	6	8.72
	Crystallinity of bulk and IL	Amorphous	Amorphous
	Crystallinity of bulk and IL	Amorphous	Amorphous

4.5.2 Comparison of Electrical Properties

The electrical properties of thermally oxidized/nitrided sputtered Sm/Ge and Ho/Ge is shown in Table 4.3. According to the *C-V* features, it is noticed that Sm_2O_3/IL/Ge gate stack enhanced the gate capacitance, C_{ox} than the Ho_2O_3/IL/Ge gate stack. This has been attributed to the lowering of total oxide thickness and increment of k values of the gate stack. From the Table 4.2, it is noticed that Sm_2O_3/IL/Ge gate stack induces more than double k value than the Ho_2O_3/IL/Ge gate stack. Additionally, from the *C-V* curve of Ho_2O_3/IL/Ge gate stack it is observed that the flat band voltage, (ΔV_{fb}) shifted negatively inducing positive fixed oxide charge (Q_{eff}) with the bulk Ho_2O_3 interface. On other hand, *C-V* curve Sm_2O_3/IL/Ge gate stack indicates the presence of negative Q_{eff} within the bulk Ho_2O_3 interface by a positive shift of ΔV_{fb}. Since Ho_2O_3/IL/Ge exhibited larger Q_{eff}which caused wider ΔV_{FB} shift for Ho_2O_3/IL/Ge gate stack. As of for Sm_2O_3/IL/Ge gate stack relatively lower hysteresis and slow trap density (Q_{it}) has been noticed than the Ho_2O_3/IL/Ge indicating less transmission of carrier charge from the Ge substrate. Moreover, Ho_2O_3/IL/Ge gate stacks generates higher D_{it} and D_{total} in counterpart to Sm_2O_3/IL/Ge. This attributes to the existence of more Ge dangling bonds and oxygen vacancies which induced enormous, charged traps within the Ho_2O_3/IL interface. However, the D_{it} is quite high for both the samples. Now, comparing the *J-E* properties it is observed that Sm_2O_3/IL/Ge gate stack induces lower leakage current density at a higher electrical breakdown field than the Ho_2O_3/IL/Ge gate stack. Comparatively lower Q_{eff}, Q_{it}, D_{it} and higher ΔE_c contributed to improve the *J-E* properties for Sm based gate stack. Additionally, the improvement of electrical properties for Sm_2O_3/IL/Ge gate stack in counter to Ho_2O_3/IL/Ge gate stack is due to relatively more thermally stable and less defective Sm_2O_3/IL interface formation. This can be attributed to the homogeneity of Sm_2O_3 and trapping effect of interfacial Sm−O−Ge effectively reduced oxygen-defects

by restricting GeO desorption. Besides, valency passivation approach of Sm−O−Ge and formation of interfacial Ge_3N_4 due to activation of N incorporation also lessened the Ge dangling bonds.

Table 4.3: Comparison of electrical features between thermally oxidized/nitrided sputtered Sm/Ge and Ho/Ge.

Electrical Properties	Unit	Sm_2O_3/IL/Ge Gate stack	Ho_2O_3/IL/Ge Gate stack
Capacitance, C_{ox}	μF/cm^2	4.60	1.38
Dielectric Constant, k	-	31.19	13.60
Leakage Current Density, J_g	A cm^{-2}	8.38×10^{-6}	5.34×10^{-5}
Electrical Breakdown Field, E_{BD}	MV cm^{-2}	13.31	8.59
Fixed Oxide Charge, Q_{eff}	cm^{-2}	-2.88×10^{12}	8.80×10^{12}
Slow trap Density, Q_{it}	cm^{-2}	1.41×10^{12}	2.93×10^{12}
Average interface trap density, D_{it}	eV^{-1} cm^{-2}	4.84×10^{13}	9.39×10^{13}
Total interface trap density, D_{total}	cm^{-2}	1.20×10^{13}	1.97×10^{13}

CHAPTER 5: CONCLUSION AND RECOMMENDATIONS

5.1 Novelty and Significance of the Findings

For last few decades the gate oxide thickness of Si based MOS technology has been continuously downscaled to cater the ongoing demand of low power consumption and high speed devices. Si based MOS technology has reached its potential limit due to drastic downscaling of SiO_2 and low hole mobility of Si. Accordingly, higher hole carrier alternative Ge and high-*k* gate oxide has gained widespread importance to replace SiO_2/Si. Various REOs with combination of Ge substrate has been widely investigated by other researchers for last few years, but REOs/Ge MOS devices are subjected to several limitations in terms of electrical and thermodynamic properties when compared to conventional SiO_2/Si MOS device. Among the REOs, both Sm_2O_3 and Ho_2O_3 owns promising features to be used as high-*k* oxides for MOS devices, owing higher dielectric constant *k* value, higher band gap value with less hygroscopic behaviour. Despite of having such attractive features the investigation of Sm_2O_3/Ge is very limited, while Ho_2O_3/Ge has not been reported till to date using the industrial deposition method of thermal oxidation and nitridation. Therefore, this study investigated the deposition condition of thermal oxidation and nitridation for sputtered Sm/Ge and Ho/Ge based on the electrical, physical, and thermodynamic properties. Moreover, the band alignment mapping and underlying thermal oxidation and nitridation mechanism of oxidized/nitrided Sm/Ge and Ho/Ge has also been reported.

In this study, Sm_2O_3/Ge stack based capacitor prepared from thermally oxidized/nitrided sputtered metallic Sm on Ge semiconductor in N_2O ambient for several oxidation/nitridation temperatures (300 – 600) °C and durations (5 – 20) minutes have been

comprehensively investigated. Besides, the influence of different thermal oxidation/nitridation durations (5 – 20) minutes in N_2O gas ambient for transforming metallic Ho sputtered on Ge substrate have been systemically investigated to develop Ho_2O_3/Ge based on metal-oxide-semiconductor (MOS) device. The film crystallinity, chemical composition and interface chemical bonding states stability was characterized from X-ray diffraction (XRD), Raman spectroscopy and X-ray photoelectron spectroscopy (XPS). Structural morphology characterization using high resolution transmission electron microscope (HRTEM). The optimum deposition condition for thermally oxidized/nitrided Sm/Ge was achieved at 400 °C and 15 min. On the contrary, a duration of 10 min at constant temperature 400 °C has been optimized for thermally oxidized/nitrided Ho/Ge. From the findings of electrical properties, it is apparent that the optimized Sm_2O_3/IL/Ge stack in this investigation provides improved dielectric constant, $k \sim 31.19$ eV, leakage current density, $J_g \sim 8.38 \times 10^{-6}$ A cm^{-2} at enhanced breakdown field, E_{BD} of 13.31 MV cm^{-1} compared to the previous reported work of (Goh et al., 2017b; C. C. Lin et al., 2014) . Besides, *EOT* as low as 0.75 nm and higher $\Delta E_c \sim 2.60$ eV has been achieved which is complementary for the ongoing MOS scaling trend. Moreover, the optimized Ho_2O_3/Ge gate stack in this investigation also exposed higher electrical breakdown, $E_{BD} \sim 8.59$ MV cm^{-1} and higher dielectric constant $k \sim 13.60$ comparing with previous reported works, (Pan, Chang, et al., 2010). Conduction band offset of $\Delta E_c \sim 2.60$ eV and $\Delta E_c \sim 2.47$ eV has been achieved for Sm_2O_3/IL/Ge and Ho_2O_3/IL/Ge, respectively which impeded the electron tunneling through gate oxide eventually contributed on reducing gate leakage current density.

5.1.1 Effect of Various Thermal Oxidation/Nitridation Temperature on Sputtered Sm Thin Film Based on Ge Substrate

In summary, a comprehensive study of Sm_2O_3/IL/Ge gate stack prepared at various thermal oxidation and nitridation temperature (300 – 600) °C in N_2O ambient were presented considering the physical and electrical characteristics of MOS devices. Based on XRD and XPS characterization formation of Trigonal Sm_2O_3 and presence of interfacial layer comprising of Ge−O, Ge−N, and Sm−O−Ge were identified. From XPS. It was found that thermal oxidation and nitridation at 400 °C was more favourable to form a uniform amorphous Sm_2O_3 film and more stoichiometric thermally stable amorphous interfacial $Sm_xGe_yO_z$ with less GeO_x and interface defects. It was evident that, formation of uniform $Sm_xGe_yO_z$ plays vital role in suppressing desorption of volatile GeO. Thus, at this temperature moderate *C-V* characteristic were obtained with higher capacitance and higher dielectric constant, less flat band voltage shift, low slow trap density with reduced average interface trap density and frequency dispersion in counter to another investigated sample. The band alignment at this temperature shows higher conduction band offset, ΔE_c and high enough VBO, ΔE_v. Hence, the high CBO impeded electron tunneling and enhanced the electric breakdown field, $E_{BD} \sim 13.31$ at low leakage current density $J_g \sim 8.38 \times 10^{-6}$A cm^{-2}. The overall improvement at 400 °C has been attributed to the sufficient N_2O incorporation to reach full oxidation level that produced stoichiometric Sm_2O_3 and stable interfacial Sm−O−Ge eventually minimized unbonded Sm^{3+} and Ge defects that maintained the integrity of stacking interface. Based on the results from XRD, XPS and HRTEM a possible oxidation and nitridation model has been proposed. Therefore, it is suggested that deposition temperature of 400 °C is more favourable for thermal oxidation/nitridation of sputtered Sm/Ge in N_2O ambient for developing Sm_2O_3/Ge gate stack.

5.1.2 Effect of Various Thermal Oxidation/Nitridation Durations on Sputtered Sm Film Based on Ge Substrate

The impact of different oxidation/nitridation durations (5 – 20) minutes on structural characteristics, chemical bonding states, band alignment mapping and electrical features for oxidizing/nitriding sputtered metal Sm on Ge prepared in N_2O ambient at 400 °C were presented. On the basis of XPS, Raman, XRD findings formation of Sm_2O_3 thin film layer with incorporation of an interfacial layer involving corelated content of Ge−O and Ge−N was confirmed for all the investigated durations. An additional interfacial Sm−O−Ge content was only detected for the extended durations of 15 and 20 min validated from Raman and XPS analysis. Besides, XRD analysis confirmed trigonal phase of Sm_2O_3, tetragonal and trigonal phase of GeO_2 and cubic phase of Ge_3N_4. The HRTEM image also supported the formation double stacked layer film involving a Sm_2O_3 dielectric layer mounted on IL interface. The XPS analysis indicated that 15 min oxidation/nitridation induced more thermally stable and less defective interface due to the growth of more stochiometric Sm_2O_3 and reduction of sub-stoichiometric GeO_x. Additionally, based on Raman and XPS analysis it was anticipated that formation of denser interfacial Ge_3N_4 and growth of stable $Sm_xGe_yO_z$ assisted the alleviation of oxygen vacancies and Ge dangling eventually suppressed GeO (g) volatilization at 15 min oxidation/nitridation duration. The electrical features also clearly suggests that 15 min is more convenient oxidation/nitridation condition at constant temperature of 400 °C to achieve superior *C-V* properties and smallest gate leakage current density of 10^{-6} A cm^{-2} order magnitude at breakdown field $E_{BD} \sim 13.31$ MV cm^{-1}.

Moreover, this duration also revealed a symmetrical band alignment mapping with superior $\Delta E_c \sim 2.60$ eV and $\Delta E_v \sim 2.98$ eV which reduced the gate leakage. Furthermore, a *EOT* of 0.75 nm was achieved for this duration which is correlated to lower interfacial thickness observed in HRTEM analysis and higher dielectric constant, $k \sim 31.19$ eV obtained from *C-V* curve. Overall, the improvement in *C-V* features, *J-E* characteristic, and ΔE_c for 15 minutes has been ascribed due to suppression of GeO (g), lessening of defective GeO_x while lowering the oxygen associated traps within Sm_2O_3 film. Contrariwise shorter oxidation/nitridation duration such as 10 minutes degrades the homogeneity of Sm_2O_3 and triggers detrimental GeO (g) volatilization along with severe GeO_x defects formation thereby, worsening the interface quality and downgraded the electrical features. Therefore, as concluding remark it is suggested that 15 minutes thermal oxidation/nitridation duration is the optimum requirement in N_2O ambient at 400 °C for Sm_2O_3/Ge based MOS gate stack.

5.1.3 Effect of Various Thermal Oxidation/Nitridation Durations on Sputtered Ho Film Based on Ge Substrate

In this work, investigation of chemical compositions, structural morphology and electrical phenomena of Ho_2O_3/IL/Ge structure were fabricated through oxidation/nitridation in N_2O gas ambient at various durations (5 – 20) min has been reported. According to the XRD and XPS analysis growth of sub-stoichiometric cubic -Ho_2O_3 and intermixing interfacial layer consisting of Ge sub-oxides GeO_x, native oxide GeO_2 and Ge_3N_4 has been confirmed. XPS analysis demonstrates that for 10 min sample formation of relatively stoichiometric Ho_2O_3 rather than sub-stoichiometric Ge–O contents helped to improve the thermal stability and interface defect alleviation. It was also apparent that formation of Ge_3N_4 rich interfacial layer during the oxidation/nitridation process aided in blocking vacancy diffusivity which ultimately suppressed the volatile GeO gas desorption. The band

alignment clearly evidenced that this oxidation/nitridation condition is also advantageous to attain high band offsets ($\Delta E_c \sim 2.47$ eV and $\Delta E_v \sim 4.67$ eV). Thus, lowest leakage current density $J_g \sim 5.34 \times 10^{-5}$ A cm^{-2} and higher electric breakdown field $E_{BD} \sim 8.59$ MV cm^{-1} were achieved. Moreover, this sample induces higher gate oxide capacitance, larger effective dielectric constant $k \sim 13.60$ and relatively lower interface trap density which confirmed that 10 min oxidation/nitridation condition is more favourable to increase the growth of high-k Ho_2O_3 while maintaining structural homogeneity. On the contrary longer oxidation/nitridation such as 20 min sample deteriorates the uniformity of Ho_2O_3 and favours the growth of detrimental Ge–O species thereby, degrades the thermal stability and electrical properties. Thickness estimated from HRTEM also reveals that 10 min oxidation/nitridation condition induced thinner Ho_2O_3/IL ~ 8.72 nm but needed to be further downscaled for being acceptable with the current scaling trend of MOS devices. Therefore, it can be concluded that oxidized/nitrided sample at 400 °C for 10 min duration in N_2O ambient is the optimized condition for Ho_2O_3/IL/Ge gate stack.

5.1.4 Comparison Between Thermally Oxidized/Nitrided Sputtered Sm/Ge and Ho/Ge

According to the findings achieved in terms of physical and electrical properties, the optimum thermal oxidation/nitridation durations for oxidized/nitrided Sm/Ge and Ho/Ge are 15 and 10 minutes, respectively at constant temperature 400 °C. The obtained physical and electrical properties of both oxidized/nitrided Sm/Ge and Ho/Ge have been summarized in Table 4.2 & 4.3. As of for the for Sm based sample at optimum deposition condition it is found that stoichiometric, trigonal-Sm_2O_3 has been formed while sub-stochiometric cubic Ho_2O_3 has been detected for Ho based sample. Additionally, both the gate stack includes an interfacial layer beneath the dielectric interface where oxidized/nitrided Sm/Ge induced both the lower bulk oxide and IL thickness than oxidized/nitrided

Ho/Ge stack. The Sm_2O_3 /IL/Ge stack exposing higher CBO, with symmetrical band alignment mapping and higher dielectric constant, inducing lower leakage current density at high electrical breakdown field and higher gate capacitance than Ho_2O_3/IL/Ge. Although both Sm_2O_3 /IL/Ge and Ho_2O_3/IL/Ge gate stack experienced high interface trap density which requires further investigation for improvement. Accordingly, Sm based gate stack exhibits more thermally stable Sm_2O_3 /IL interface with higher electrical properties in counter to Ho_2O_3/IL interface of Ho based gate stack. According to the physical and electrical properties found in this study constitutes that both Sm_2O_3 and Ho_2O_3 could serve as dielectric material for future high-*k*/Ge stack based metal oxide semiconductor technology. Overall, it can be concluded that Sm_2O_3 is a superior choice in counter to Ho_2O_3 for developing Ge based gate stack using thermal oxidation/nitridation.

5.2 Recommendation for Future Research

The findings of this investigation are anticipated to provide new insight on the realization of REOs for MOS application which requires comprehensive evaluation for future revolution of MOS devices. The following concepts are suggested for future prospective research.

(i) It will be interesting to investigate the impact of post deposition annealing (PDA) temperature in various gas ambient (such as Ar, N_2, and O_2) for further improvement of thermally oxidized/nitrided sputtered Sm/Ge or Ho/Ge.

(ii) The influence of N_2O gas concentration on the electrical and physical properties for sputtered Sm/Ge or Ho/Ge following thermal oxidation/nitridation could further advance the process of utilizing Sm_2O_3 and Ho_2O_3 as alternative High-*k*.

(iii) Thermal oxidation/nitridation for developing bilayer gate stack with combination of (Sm_2O_3 + TMOs)/Ge or (Ho_2O_3 + TMOs)/Ge where TMOs such as Al_2O_3 or ZrO_2 could be utilized for realization of Ge based MOS devices.

(iv) To gain further insight for Sm_2O_3/Ge or Ho_2O_3/Ge gate stack the reliability evaluation in terms of bias temperature instability (BTI) performance and current conduction mechanism will be another potential aspect for further research.

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