CHAPTER ONE: INTRODUCTION

The demand for higher quality thin oxide films on larger silicon wafers in order to improve the production yield of ultra large scale integrated circuit (ULSI) metal oxide semiconductor (MOS) devices has been steadily increasing. However, defect present in the SiO_2 layer is one of the major causes of low yield in fabrication of ULSI devices [1-3]. To meet this demand, many techniques have been developed to characterize defects in oxide films. Some of these techniques are listed in Table 1.

Table 1: Methods of analyzing localized film defects [4]

Method	Technique
1. Optical methods	i. Brightfield, darkfield, phase-contrast microscopy
	ii. Nomarski differential interference-contrast microscopy
	iii. Multiple-beam interferometry
	iv. Light scatterng
2. Electrical methods	i. Gate oxide integrity measurement (GOI)
	ii. Electrochemical autography
	iii. Electrolytic copper decoration
	iv. Electrolytic gas bubble formation
	v. Electrophoretic decoration
	vi. Corona-charging decoration
3. Electronic methods	i. Scanning electron microscopy
	ii. Transmission electron microscopy
	iii. Replica electron microscopy
	iv. Electron diffraction
4. Mechanical methods	i. Surface profilometry by stylus instruments
	ii. Sectioning techniques
5. Chemical methods	i. Selective solution etching of films or substrates
	ii. Preferential high temperature gas-phase etching

6. Localized Composition-Analytical Microvolume Methods	i. Electron scanning chemical analysis ii. Scanning Auger microprobe analysis iii. Laser scanning photoemission iv. Neutron activation combined with autoradiography v. X-ray and electron diffraction

However, it is found that most of the methods listed in Table 1 are not a rapid method of oxide defect detection. This is because of the minute size of defects and the highly reflective nature of the dielectric film. Moreover, techniques such as Gate Oxide Integrity (GOI) measurement, needs considerable investment in installing and maintaining a poly-silicon line for GOI gate fabrication. In addition, it requires extensive preparation and interpretative effort.

Copper decoration technique is an alternative method used for locating defects in dielectric film. This technique was first developed in 1970 by Shannon [5]. It is a combination of applying a constant voltage to stress the oxide layer, and electrolysis process. This technique is cheaper, easier to set up and to carry out compared to GOI measurement. As a result, it is adopted by companies such as S.E.H. (M) Sdn. Bhd. to monitor the quality of the silicon wafers at its production lines.

The present work has two main objectives, namely:

(i) To study the formation of copper dots on oxide surface, and

(ii) To study the effects of copper concentration on copper decoration results.

This thesis comprises of five chapters. Chapter 1 introduced the project. Chapter 2 presents relevant background theory on copper decoration technique and the motive to carry out this project. Chapter 3 describes the measurement and experimental setup. Chapter 4 reports experimental results to explain the growth of copper dots on oxide surface and the effects of copper concentration on the copper dots formation. Lastly, Chapter 5 concludes the main findings of this project.