CHAPTER TWO: LITERATURE REVIEW

This chapter starts with overview of copper decoration technique. Since this technique involves oxide breakdown and deposition of copper ions at the breakdown spots, more details discussion will be done on the following topics, i.e, growing of silicon dioxide layer via dry oxidation process, defects in oxide layer and electrolysis process. Furthermore, some of the features in copper decoration technique are similar with Gate Oxide Integrity (GOI) measurement technique. Therefore, GOI measurement and oxide breakdown at metal-oxide-semiconductor (MOS) structure will be described briefly too. Finally, works that are going to be done in this project are summarized in the last portion of this chapter.

2.1 Overview of copper decoration technique

As mentioned earlier, copper decoration technique is an alternative method to determine oxide quality. This is because it provides a rapid way to locate the dielectric defects. This technique requires a copper decoration unit, which consist of one teflon beaker, one piece of glass plate, two electrodes (copper plates) and one DC power supply as illustrated in Fig. 2.1 (a). To prevent damages on oxide surface due to direct contact with anode, the wafer polished surface and anode are separated by a gap of ≈ 5mm. This gap is then filled with methanol during copper decoration process.

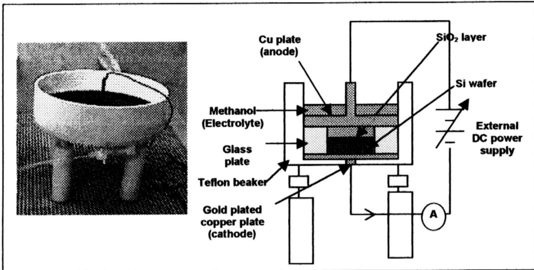

Figure 2.1 (a): Schematic diagram of the copper decoration apparatus.

To carry out copper decoration, polished wafer is loaded into the equipment. Then, a constant DC power is supplied to the equipment. This DC power supply provides electric field to stress oxide layer of the sample. Eventually, copper dots are formed on oxide surface as shown in Fig. 2.1 (b). The mechanism of copper dots formation will be discussed in more details in section 2.3 and section 4.1.

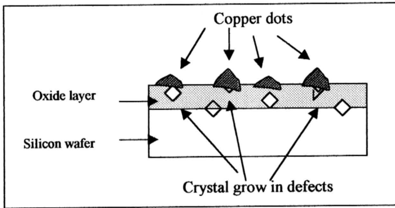

Figure 2.1(b): Copper dots form right on top of the defects in oxide layer.

At stress field of 5 ± 0.5 MV/cm, most of the defects detected on a good wafer by copper decoration technique are crystal grown in defects, mainly contributed by gigantic vacancies (also know as D-defects) [10-26]. Copper dots form due to other process induced defects at this applied field is negligible. Figure 2.2 (a) (i) and (ii) shown copper decorated samples of normal Czochralski (Cz) wafer and low defect Cz wafer. It is found that the copper dots are randomly distributed on the surface for normal Cz wafer. However, copper dots are concentrated at the centre portion of low defect Cz wafers. The distribution of copper dots on these wafers are correlated with the distribution of crystal grown in defect detected using Secco etching (preferential etching) as shown in Fig. 2.2 (b) (i) and (ii). In this case, defect revealed by Secco etching is also known as Flow Pattern Defects (FPDs) [6].

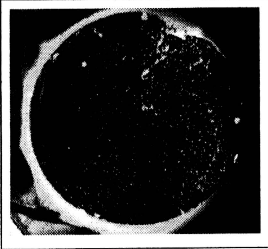

Figure 2.2. (a) (i): Normal Cz wafer after copper decoration.

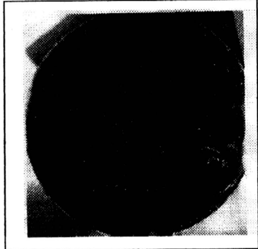

Figure 2.2 (a) (ii): Low defect Cz wafer after copper decoration

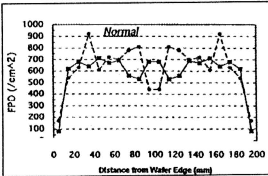

Figure 2.2 (b) (i): Distribution of defects (FPDs) across the diameter of wafer on Normal Cz wafer after preferential (Secco) etching.

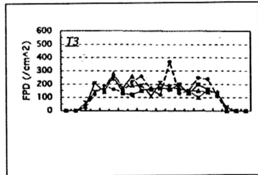

Figure 2.2 (b) (ii): Distribution of defects (FPDs) across the diameter of wafer on Low Defect Cz wafer after preferential (Secco) etching.

2.1.1 Growth of silicon dioxide (SiO_2) layer

Silicon dioxide (SiO_2) film plays an important role in semiconductor technology. It is the most frequently used dielectric film in semiconductor technology. SiO_2 layer is used for masking during doping, for electrical insulation, for junction

passivation, for storing charges and sometimes for mechanical protection of the structure.

SiO_2 layer has superior characteristics compared to other dielectric materials such as Si_3N_4 and polysilicon. It becomes a good dielectric because of the following properties, (i) no residual constituent will outgas during later processing stage, (ii) good step coverage, (iii) ease of etching using HF solution, (iv) high temperature stability and (v) high breakdown field ($\approx$ 10MV/cm). The oxide layer can be grown easily by thermal oxidation, chemical vapor deposition (CVD), plasma CVD, physical vapor deposition (PVD) and sputtering [3-4,6-7].

The oxide layer of all the samples used in this project is grown by dry thermal oxidation. It is performed in an open-ended quartz tube kept in a resistance-heated furnace at the temperature of 900°C. The oxidized ambient is dry oxygen. Fig. 2.3 shows the schematic of a dry oxidation system.

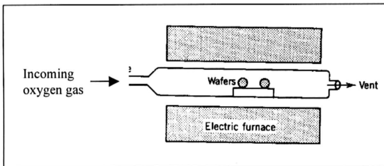

Figure 2.3: Cross-sectional view of a dry oxidation system [6].

Prior to oxidation process, wafers are loaded into a quartz boat. Then, they are placed inside the furnace that is already heated to the desired temperature. To start the oxidation process, high purity oxygen gas is supplied through the inlet. The gas

flows through the furnace and oxygen molecules will react with silicon atoms of wafer to form silicon oxide.

$$Si\ (s) + O_2\ (g) \longrightarrow SiO_2\ (s)$$

According to oxidation model proposed by Deal and Grove [8], 44.5% of the oxide thickness that grows on the wafer surface is contributed by the silicon wafer as illustrated in Fig. 2.4.

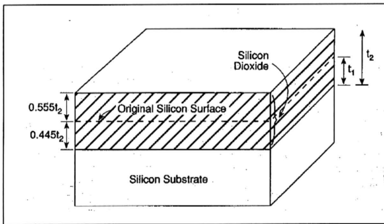

Figure 2.4: Planar growth of silicon dioxide on silicon. For a growth of oxide of thickness t_2, a 0.445 t_2 thick layer of Si is consumed [8].

As a result, particles, scratches, metallic contamination or crystal grown in defects such as D-defects that is present on or near surface will be integrated into the oxide layer during oxidation as shown in Fig. 2.5 [3-4, 6-7].

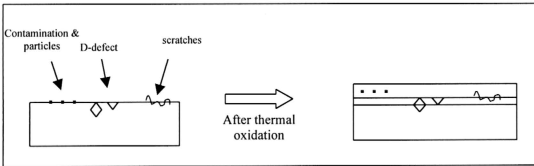

Figure 2.5: Defects near or at the surface of wafer are integrated into oxide layer after thermal oxidation.

2.1.2 Defects in the SiO_2 layer [1, 3-5, 9]

Defects in SiO_2 layers can be categorized into process induced defects and crystal grown in defects. There are many types of process induced defects present in the silicon wafers. For instance, these defects can be metallic contamination such as sodium ions, copper ions or iron ions. These metallic ions have high diffusivity and able to degrade the SiO_2 film. Moreover, particulate contaminants (dust or reaction products) in the gas or on the substrate surface during thermal oxidation will interfere with film growing. This result in voids, thin spots, partial or complete pinholes or hillocks. If particulate impurities are embedded in the film during thermal oxidation, they may constitute a potential source of device failure due to local weakening of the dielectric breakdown strength [1, 3-5, 9].

On the other hand, crystal-grown in defects can be an interstitial type of defects such as dislocation and oxygen induced stacking fault (OSF), or vacancy type of defects such as D-defects (giant vacancy). Since copper decoration

technique is more sensitive to D-defects [10-26], the origin of this defect will be discussed in more details in the following paragraphs.

Publications have appeared concerning D-defects content and shape [10-13]. D-defects have been recognized as surface defects or micro pits. They originate from grown in defects and cannot be removed by conventional cleaning processes [14-15]. In recent studies, D-defects in silicon bulk had been observed directly with combination of copper decoration techniques, TEM and EDX [10, 12, 16-19]. The polyhedron structure with its sides is oriented along the (110) axis. As shown in Fig. 2.6, the angle between a face and the Si surface is 55°, which indicates the face has a (111) orientation. [5, 16].

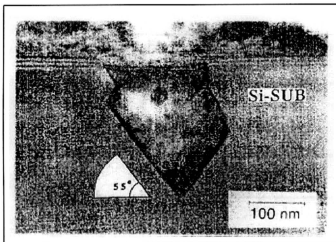

Figure 2.6: TEM observation of the D-defect, cross section view [16].

The size of the structure is about 150 - 300 nm. [20]. T. Ueki *et. al.* also [21] reported that there are two types of twin octahedral defects: an overlapping type and an adjacent type.

In the analysis of the D-defects by secondary ion mass spectrometry (SIMS), oxygen atoms were detected [22]. Moreover, energy-dispersive X-ray spectroscopy (EDS) analysis [12] and Auger electron spectroscopy [11, 19] analysis on these defects suggest that the side walls are covered with thin oxide films. Therefore, it has been clarified that the grown in defects are composed of incomplete octahedral voids and thin SiO_x walls of several nanometers thickness surrounding the void [11-12, 19].

Figure 2.7 illustrates developing of D-defects during Si crystal growth [16].

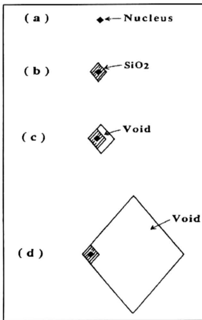

Figure 2.7: D-defect generation model during crystal growing proposed by M. Itsumi *et. al.*[16].

A nucleus (or nucleation) is generated in the CZ- Si ingot as shown in Fig. 2.7 (a). It acquires not only oxygen but also vacancies. These nucleuses develop many voids during the long period of crystal growth, as shown in Fig. 2.7 (b). Eventually,

these small voids join together to form gigantic vacancies [16, 23], i.e. D-defects. The generation probability of D-defects is large when growth rate is large [24-25].

Many methods have been developed to detect and characterize the D-defects. Different names are given to D-defects corresponding to the inspection techniques. It is known as flow pattern defect (FPD) after Secco etching [26] and observed by low power microscope. The flow patterns are originated at the etch pits. On the other hand, these grown in defects are also known as crystal originated particles (COPs) after SC1 cleaning using NH_4OH/ H_2O_2/H_2O solution and measured by particles counter [14]. The disadvantage of this technique is the difficulty in directly observing the morphology of the D-defects. This is due to the destructive nature of etching process. One of the non-destructive measurements to detect D-defects is by infrared (IR) laser. The defects are then called as laser scattering tomography defects (LSTD) [27]. To avoid confusion of the names given to this defect, "D-defects" will be used to describe this gigantic void through out the writing of this thesis.

Copper decoration technique enables researchers to locate the D-defects easily for the past thirty years ago [5, 10, 16, 20, 28-36]. Some of the advantages of this technique in locating D-defects are

(i) Copper dots are formed right on top of the defects. This allows researchers to identify the location of the defect easily. By using this information and with the help of focus ion beam (FIB) to reduce the sample thickness, one can observe the defects using transmission electron microscope (TEM).

(ii) The electronic current flows through the oxide breakdown paths during copper decoration is smaller compared to dielectric breakdown in MOS structures. There is a little joule-heating effect at these oxide breakdown paths. The heat released by the current at the breakdown path is not able to melt the surrounding silicon and silicon dioxide. This result in the structure of the D-defect can be preserved and observed.

(M. Itsumi *et. al.* [34] made an attempt to characterize the D-defects by using GOI measurement. MOS structures were fabricated on wafer surface. Then, a high voltage is applied to the gate electrode to cause the dielectric breakdown. After the breakdown, they tried to observe the spot by TEM. However, only ambiguous shapes of structure were observed. As a result they could not characterize the oxide defects. The reason that the shapes were not well defined was due to excessive current flowed through the weak spot during oxide breakdown. This damages the oxide defect structure itself due to local joule heating by high current density.)

The images of D-defect that detected by copper decoration technique, following by FIB and TEM is shown in Fig. 2.8 [37].

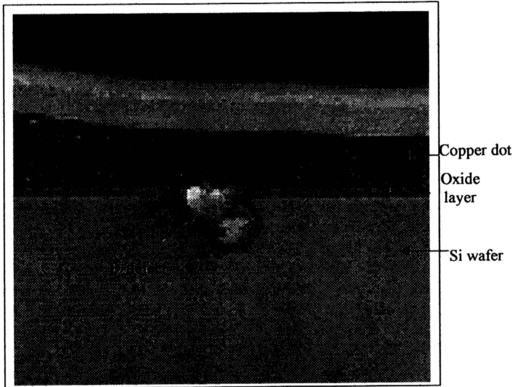

Figure 2.8: TEM image shown that part of the COPs is integrated into the oxide layer. These COPs are detected at the bottom of the copper dot [37].

Researchers claimed that D-defects affect the gate oxide integrity (GOI) yield [11, 38-45]. One of the explanations is believed due to oxide thinning at the corner of D-defects [20]. This is shown in Fig. 2.9.

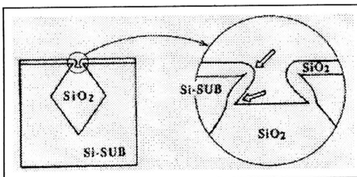

Figure 2.9: Schematic of the oxide-defect results oxide thinning spots at oxide layer [20].

However, S.Oka *et. al.* [28] proposed another breakdown model due to D-defects. His analysis showed that the D-defects is filled with "imperfect silicon", rather than a void. Therefore, the oxide breakdown occurs due to the formation of degraded oxide, which is made out of the imperfect silicon during oxidation. D-defects in oxide layer most frequently fail at the range of 3-8 MV/cm stressed field in conventional GOI measurement [10-12, 20, 28].

2.1.3 Electrolysis process [39-40]

As mentioned earlier, during copper decoration process, copper ions are ejected from anode into the methanol. These copper ions are positively charged.

$$Cu\,(s) \longrightarrow Cu^{2+}\,(ac) + 2\,e^{-}$$

As a result of electropotential between anode and cathode, copper ions experience force exerted by electric field. They are driven from anode to cathode, and deposit as copper dots on oxide surface (cathode).

2.1.3.1 Ions transportation in electrolyte [39-40]

Ions can be transported to the surface of an electrode by three mechanisms, namely (i) diffusion, (ii) migration, and (iii) convection. Diffusion occurs when there is a concentration difference between two regions in solution. Ions or molecules move from the more concentrated region to the more dilute region. This ultimately leads to a disappearance of the concentration difference. The rate of diffusion is directly proportional to the concentration difference. This can be described by Fick's first law:

$$J_i = -D_i\left(\frac{\partial c_i}{\partial x}\right) \qquad (1)$$

where J_i is the flux of species i with concentration c_i in direction x, and $\left(\frac{\partial c_i}{\partial x}\right)$ is the concentration gradient. D_i is the proportionality factor between flux and concentration gradient, know as the diffusion coefficient [39]. The negative sign arises because the flux of species tends to annul the concentration gradient.

On the other hand, migration happens when ions move under the influence of an electric field. This process is the primary cause of mass transfer in the bulk of the solution in cell. Migration affects only on charged species (effectively, owing to the existence of dipoles, or induced dipoles in neutral species). The rate at which ions migrate to or away from an electrode surface generally increases as the electrode potential increases. This charge movement constitutes a current, which

also increases with potential. In the presence of an applied electric field, $E = \frac{\partial \phi}{\partial x}$, the rate of ions migration is given as

$$J_i = -z_i c_i \left(\frac{F}{RT} \right) E \qquad (2)$$

where z_i is oxidation number of ions, c_i is concentration of ions, F is Faraday number, R is constant of ideal gas and T is the temperature.

Lastly, convection is the mechanical transport of ions or molecules through a solution as a result of stirring, vibration, or temperature gradient. This mechanism is not possible without stirring, vibration or temperature gradient.

2.1.3.2 Effects of ions concentration on the conductivity of electrolyte

It is found that the ways of ions transport and its concentration in the electrolyte will affect the conductivity of the electrolyte. Consider ions transportation via migration mechanism, the rate at which ions migrate to or away from an electrode surface generally increases as the electrode potential increases. This charge movement constitutes a current, which also increases with potential. Let us consider an isolated ion under the influence of an electric field [39]. The force due to the electric field is

$$F = z_i e E \qquad (3)$$

where z_i is oxidation number of ions, e is charge of electron and E is electric field gradient. This force is counterbalanced by a viscous force given by Stoke's equation

$$F_i = 6\pi\eta r_i v_i \tag{4}$$

where η is the solution viscosity (kg/ sec. m), r_i the radius of the solvated ion (m) and v_i the velocity vector (m/s). The retarding effects are neglected. The maximum velocity is

$$v_i = \frac{z_i eE}{6\pi\eta r_i} = \left(\frac{eE}{6\pi\eta}\right)\left(\frac{z_i}{r_i}\right) \tag{5}$$

The flux of charge, j_i is

$$j_i = z_i e v_i c_i N_A = \left(\frac{e^2 N_A E}{6\pi\eta}\right)\left(\frac{z_i^2}{r_i}\right)c_i \tag{6}$$

where $z_i e$ is the charge of each ion (C), v_i is the velocity, and $c_i N_A$ $\left\{ \left(\frac{mol}{m^3}\right)\left(\frac{1}{mol}\right) \right\}$ is the numerical ion density. The current, I (A) that passes between two parallel electrodes of area A is related to the flux of charge j, and to the potential difference between them, ΔV, by

$$I = j_i = k_i \left(\frac{A \Delta V}{l} \right) = k_i E A \qquad (7)$$

where k_i is the conductivity (S) and l (m) is the distance between the electrodes that apply the electric field of strength $E = \left(\frac{\Delta \phi}{l} \right) = constant$. By combining (6) and (7), one immediately concludes that conductivity of each ion is

$$k_i = \left(\frac{e^2 N_A}{6 \pi \eta} \right) \left(\frac{z_i^2}{r_i} \right) c_i \qquad (8)$$

Equation (8) indicates that the conductivity of electrolyte (k_i) is proportional to the ions concentration in the electrolyte (c_i).

2.1.3.3 Voltage drop in electrochemical cell

When there is a current in an electrochemical cell, the cell potential is no longer simply the difference between the electrode potentials of the cathode and the anode. Ohmic potential or also known as voltage drop requires application of potentials greater than the thermodynamic potential to operate an electrolytic cell.

Electrochemical cells like metallic conductors, resist the flow charge. In both types of conduction, Ohm's law describes the effect of this resistance. That is,

$$E = I\,R \qquad (9)$$

where E is the potential difference in volts across the cell resistance, R is the cell resistance in ohms, and I is the current in the cell in amperes. The product on the right-hand side of this equation is called the *Ohmic potential* or the *voltage drop* of the cell.

$$E_{ext} = E_{cell} + IR \qquad (10)$$

where E_{ext} is the externally applied voltage, and E_{cell} is the thermodynamic potential of the cell. E_{ext} and I are positive for an electrolysis process [39-40].

The above discussion occurred similarly in copper decoration process. As illustrated in Fig. 2.1 (a), the anode and cathode is separated with a gap of around 0.5cm. This gap is filled with methanol during copper decoration process. Assuming that the voltage lost due to electrical contacts are negligible, the voltage on oxide surface (V_{ox}) that actually used to stress the oxide layer is smaller than the applied voltage (V_{app}). Equation (10) can be modified

$$\begin{aligned} V_{drop} &= V_{app} - V_{ox} \\ &= IR \qquad (11) \end{aligned}$$

In copper decoration technique, it is important to know the V_{ox} or more accurately the applied field that uses to stress the oxide layer. This is because number of

copper dots grows on oxide surface of the wafer depending on the magnitude of applied field. Consequently, V_{ox} or stressed field is one of the important parameters to obtain repeatability and reproducibility results in copper decoration technique [5]. The V_{ox} can be measured during the copper decoration by using V_{ox}/V_{app} ratio measurement technique.

2.2 Gate oxide integrity

2.2.1 Oxide breakdown in Metal-Oxide-Semiconductor (MOS) structure

When an oxide layer is subjected to an electric field, it is considered to be breakdown if the current exceeds a certain pre-selected level e.g. 10^{-4} A/cm^2. The process of dielectric breakdown of capacitors often occurs at weak spots. The weak spots can have a much smaller area than the electrode area of the capacitors. Weak spots may consist of any feature, which lowers the injection barrier, enhances the field or by other means lowers the dielectric strength. Dislocations, stacking faults, space charge, traps, aspirates, contamination, etc., all can govern locally the dielectric strength of the whole capacitor. Defect is referred to any feature that changes locally the dielectric properties of the capacitor. The unchanged properties are referred to as intrinsic properties. When a capacitor contains more than one weak spot, the weakest of all spots will determine its dielectric strength.

Intrinsic breakdown or defect related breakdown can occurr at the oxide layer that has been subjected to electric field. Theoretically, intrinsic breakdown

indicates the maximum dielectric breakdown field or maximum total injected charges per unit area that can be tolerated by the oxide layer without breakdown. In practical, intrinsic breakdown is considered to occur when the breakdown field (E_{bd}) exceeds 10 MV/cm for thermally grown silicon dioxide layer. At this field, electrons can tunnel through the energy barriers at the electrode interfaces. On the other hand, the samples with defect-related breakdown will have E_{bd} or total injected breakdown charges (Q_{bd}) values lower compared to intrinsic breakdown.

2.2.2 The mechanism of oxide breakdown

Dielectric breakdown is the result of charge injection. When the injected charges are trapped in the charge traps, energy released by the charges might be able to damage the silicon lattice. Damaging a lattice takes at least the energy for its formation. The heat of SiO_2 formation is ΔH = 909 kJ/mole = 33 kJ/cm^3. The damages induced by this charge injection are permanent. At the moment of breakdown, the displacement charge provides the energy that causes the destruction of the capacitor. At breakdown, part of the capacitor is gasified and a larger part is melted [3, 9].

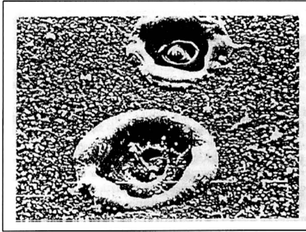

Figure 2.10: A SEM image of a breakdown in a poly-silicon gates of MOS devices. Oxide thickness was 40 nm. The gate was negatively biased. The wafer was n-type Si with capacitor area of 0.2 mm^2. The diameter of the gasified area was around 4 - 5 μm [3].

The breakdown model can be divided into four stages.

(i) The driving force for the generation of damage

The erosion of pathway is produced by the injection of charge into the wide energy gap of SiO_2 layer. Electrons injected over the high energy barrier in the conduction band have a large potential energy of 4 to 5 eV above the Fermi level. This energy is lost when these electrons are captured in deep traps or emitted into one of the electrodes. Their potential energy has to be transferred to the atomic and electronic species of the trap (and its environment) or to those of the electrodes. The energy of 4 to 5 eV is sufficiently large to break bonds, ionize atoms, etc. In conclusion, it is the number of electrons that causes oxide breakdown.

(ii) The capacitors' memory for injection

The abrupt change in potential energy must be found at the electrodes and at deep traps. Charge centers influence the pattern of conduction, and hence that of the erosion. When injected electrons are trapped, this results a negative space charge. Therefore, the subsequent injected electrons will be repelled. This will confine the current to a small area. In the opposite case of positive space charge present in dielectric, injection of electrons will be concentrated at the same spot. The local injection density will be high. The damage, leading to a short-circuiting path, takes much less Q_{bd}. Therefore, one can claim that the capacitor "memorizes" the previous stress.

iii. The growth of the discharge pattern

(a) (b)

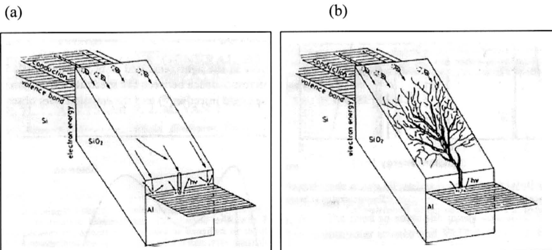

Figure 2.11: The waterfall model proposed by Wolters *et. al* [3]. The electron energy is plotted along the z-axis. (a) The growth of a discharge pattern until breakdown. (b) Breakdown occurs when the damage path reaches the other side of cathode.

Figure 2.11 schematically depicts the growth of a "discharge" pattern. The channels are assumed to contain positive charges acting as a local potential minimum for injected electrons. These form deep traps for the electrons by their Coulomb attraction. They have high local fields and large capture cross sections. The growth of the channels is in the direction of maximum discharge of the injected electrons. This may be different from the direction of the applied field. When injection and trapping is homogeneously distributed over a layer, a tree-shaped discharge pattern is formed as shown in Fig.2.11 (b).

iv. The final collapse

At the final collapse, one of the channels has reached the vicinity of the opposite electrode and the erosion is accelerated. The channel is heated when the energy of the charged capacitor is dissipated. Temperatures can reach 3000 – 4000k and a hole is burnt in the electrode as shown in Fig.2.10. Depending on the energy released during the collapse, parts of the capacitor and substrate are evaporated and often erupted over the area of the capacitor.

2.2.3 Gate Oxide Integrity (GOI) measurement

GOI measurement is a conventional technique uses to determine oxide quality. Prior to GOI measurement, hundred of polycrystalline silicon gates are fabricated on top of an oxidized wafer as shown in Fig. 2.12.

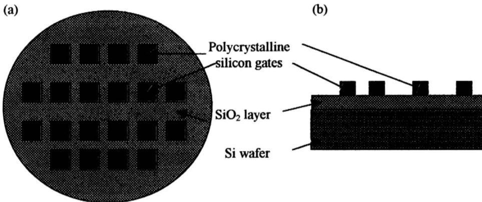

Figure 2.12: (a) Top view (b) side view of GOI samples. Basically, it consists of Metal-Oxide-Silicon (MOS) structure.

There are two main methods normally used in GOI measurement technique. In Time Zero Dielectric Breakdown (TZDB) method, a ramp up field is applied to the gates. On the other hand, a constant current is used to stress the gates in Time Dependent Dielectric Breakdown (TDDB-I) method.

2.2.3.1 Time Zero Dielectric Breakdown (TZDB) measurement method

In TZDB measurement, a ramp up DC voltage is applied to the gates through a test probe touching on the gate (Fig. 2.13 (a)). The gate is declared breakdown when the current density flowing through the circuit exceeds $1x10^{-4}$ A/cm^2 (Fig. 2.13 (b)). The breakdown voltage (V_{bd}) or more accurately the breakdown field (E_{bd} = V_{bd}/ t_{ox}, where t_{ox} is oxide thickness) is recorded down. These measurement steps are then applied to other selected gates on the wafer surface. After the measurement completed, a graph of number of gates breakdown versus breakdown field is plotted as shown in Fig. 2.13 (c).

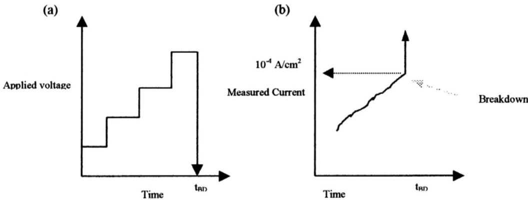

Figure 2.13: (a) A ramped up voltage is applied to the gates. (b) Current density is measured as a function of time. When J > $1x10^{-4}$ A/cm^2, oxide breakdown occurs. The breakdown voltage (V_{bd}) of this gate is then recorded down.

(c)

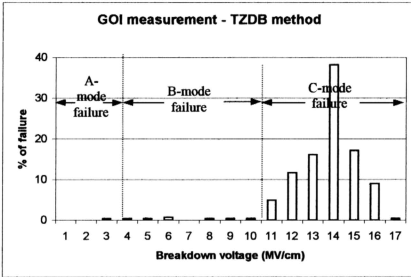

Figure 2.13: (c) A graph of percentage of failure (or number of gates) is plotted as a function of breakdown field (E_{bd}).

As shown in Fig. 2.13 (c), the number of breakdown spots increases as a function of stressed field. This is because the defects that integrated in the oxide layer cause different degree of damages on the oxide layer during oxide growing. Depending on the breakdown field (E_{bd}), the researches categorized the graph into three failure modes [9]. A & B mode failures are referred to defect-related breakdown, whereas C mode failure is intrinsic breakdown [1,3-4]. Defects such as pinholes and heavy metallic contamination are believed to causes A-mode failure at $E_{bd} < 3$MV/cm. In B-mode failure, gates will fail at the range of 3 –10 MV/cm. Defects contribute to this failure mode mainly from D-defects [39-45]. Intrinsic breakdown is achieved when $E_{bd} > 10$ MV/cm.

2.2.3.2 Time Dependent Dielectric Breakdown (TDDB-I) measurement method

In this method, a constant current is applied to stress the gate (Fig. 2.14 (a)). Breakdown occurs when the applied voltage to maintain constant current in the circuit is decreased more than 15% of the initial applied voltage (Fig. 2.14 (b)). The breakdown time, t_{bd} (or more accurately the total injected charges to cause breakdown, $Q_{bd} = \int I \, dt$) is recorded down. The measurement result can be presented in Weibull plot [9] (or accumulation of percentage failure of gates in logaritma scale) as shown in Fig. 2.14 (c).

Since oxide breakdown is due to the total number of injected charges, the results obtain in TDDB-I is more representative the oxide quality in GOI measurement.

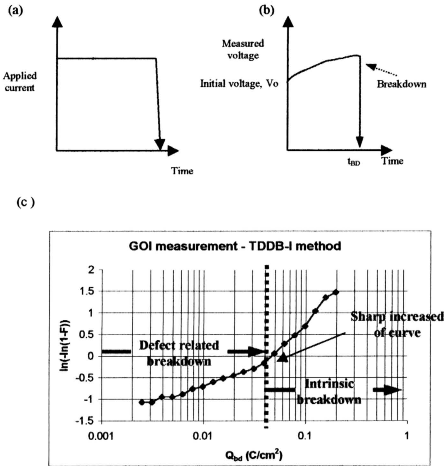

Figure 2.14 (a) A constant current with selected magnitude is applied to the gates. (b) The corresponding applied voltage to maintain the constant current is measured as a function of time. When $V < 0.85V_o$, oxide breakdown occurs. The breakdown time (t_{bd}) of this gate is then recorded down. (c) A Weibull plot (or accumulation % of gates failure in logaritma scale) is plotted as a function of total injected charges to cause breakdown (Q_{bd}).

Similarly, one can divide the TDDB-I result into intrinsic breakdown and defect related breakdown. Intrinsic breakdown is said to be happened when there is a sharp increased of curve in the plot.

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2.3 Aim of this project

Decoration methods are especially useful if an enlargement of the defects is desired for visualizations, photographic recording or automated counting for statistical evaluation. In fact, researchers have used the combination of copper decoration technique, and TEM or AFM to observe D-defects directly [5, 10, 16, 20, 28-36]. These papers shown that those copper dots are formed on top of the defects. However, there is lack of details discussion on formation of copper dots in their report.

Furthermore, Shanon [5] found that the dielectric film integrity is exponentially dependent upon the field and therefore on the dielectric surface voltage, V_{ox}. The weakest parts of the dielectric film decorate initially. Then, the less weak sites become decorated with copper as the electric field is increased. He claimed that for a meaningful application of this technique, the conditions should therefore be fixed or varied in a standardized manner. Anyway, he never mentions the method to measure the V_{ox} accurately in his report.

Besides, Shanon also pointed that the reproducibility of the decoration method was found to be dependent on the electrolytic conductivity, the electric field distribution and the dielectric surface potential. Similarly, no data is shown in his report [5] to explain the way electrolytic conductivity can affect the copper decoration result.

Consequently, this project is carried out to further understand the copper decoration technique. The first portion of the project will report on the investigation

results of copper dots formation. Formation of dots involves of oxide breakdown as a result of applied field and deposition of copper atoms via electrolysis process. In deposition of copper atoms, evident will be shown that copper ions are dissolved form the anode (copper plate). Then, the relationship of copper concentration in methanol as a function of time and magnitude of current will be discussed. This is followed by Time-Of-Flight Secondary Ion Mass Spectroscopy (TOF-SIMS) analysis to identify the cations that deposited as "dots" on wafer surface. On the other hand, evident to support that damages are created/ extended to wafer surface during oxide breakdown will be given in the report. Although these damages cannot visualize using naked eyes, preferential etching can be used to enlarge the size of damages in order to observe under low magnification of microscope (50X). In addition, the relationship of defect density with stressed field will be reported too. This will follow with the investigation on the relationship between the size of copper dots and size of D-defects. Since formation of the copper dots is attributed to the discharging of cations (mainly copper ions) at the defect region, a model is proposed to explain the shape of copper dot.

The second section of the report discusses proper method to determine stress field correctly. The results show that the V_{ox} measurement is affected by the exposed (non-insulated) length of the probe. As a result, the V_{ox}/V_{app} ratios should plot as a function of exposed probe lengths and extrapolate to the y-axis intersect (zero exposed length) to accurately determine the V_{ox} value.

Finally, the effects of copper concentration in methanol on copper decoration result are reported. Experimental results show that the copper concentration will affect the size of copper dots and conductivity of methanol.