DESIGN OF ULTRA LOW VOLTAGE, HIGH EFFICIENCY CMOS RADIO FREQUENCY ENERGY HARVESTING SYSTEM

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DESIGN OF ULTRA LOW VOLTAGE, HIGH EFFICIENCY CMOS RADIO FREQUENCY ENERGY HARVESTING SYSTEM

ABSTRACT

Wireless Sensor Networks (WSNs) have emerged as a pivotal technology for various IoT applications, driven by advancements in 5G (5^{th} Generation) technology and cloud computing. For stable and continuous operation, Radio Frequency Energy Harvesting (RFEH) is considered an optimal energy source for WSNs to achieve self-power capabilities, alleviating the need for a battery. The rectifier and charge pump (CP) plays a crucial role within the Radio Frequency Energy Harvesting (RFEH) system. However, the performance is significantly impacted by high conduction and reversion loss in subthreshold operation. Despite the existence of dynamic gate biasing (DGB) techniques that aim to mitigate both conduction and reversion losses, these losses cannot be entirely eliminated, resulting in the low performance of the rectifier and CP circuit. Furthermore, the broad range of scavenged input power from the RFEH system can result in elevated output voltage levels that may pose a risk of damaging the WSN load. This thesis presents a comprehensive review of recent rectifier and CP improvement techniques and provides a thorough analysis of the characteristics of the state-of-the-art rectifier and CP circuit. By considering the trade-offs, several enhancements are proposed to optimize these components specifically for subthreshold operation, aiming to improve its power conversion efficiency (PCE). This work proposes a novel advance dynamic gate-biasing technique that focuses on reducing forward conduction loss and reverse current leakage loss in the rectifier and CP. Specifically, the advanced DGB is combined with an NMOS-PMOS dual-switch transistor pair which acts as a secondary switch to further reduce the losses. By implementing this combination, the proposed architecture achieved an ultra-low-voltage input (0.1 V) subthreshold operation CP with a PCE of 43.4 %. Additionally,

a novel reconfigurable series-parallel CP employing a dynamic source-fed oscillator with 62 % PCE is introduced. Finally, an integrated RFEH featuring a low-power voltage monitoring unit with 3.3 V bounded output cater is designed to cater to WSN applications. The research contributes to the understanding and advancement of rectifiers and CPs, and the design of a fully integrated RFEH system, enabling more efficient energy utilization in WSNs.

Keywords: radio frequency energy harvesting, CMOS charge pump, DC-DC converter, power conversion efficiency, subthreshold operation

REKA BENTUK SISTEM PENUAIAN TENAGA RADIO CMOS VOLTAN ULTRA RENDAH DAN KECEKAPAN TINGGI

ABSTRAK

Rangkaian Penderia Tanpa Wayar (WSN) telah muncul sebagai teknologi penting untuk pelbagai aplikasi IoT, didorong oleh kemajuan dalam teknologi 5G (Generasi Ke-5) dan pengkomputeran awan. Untuk operasi yang stabil dan berterusan, Penuaian Tenaga Frekuensi Radio (RFEH) dianggap sebagai sumber tenaga optimum untuk WSN untuk mencapai keupayaan kuasa diri, mengurangkan keperluan untuk bateri. Pam penerus dan pengecas (CP) memainkan peranan penting dalam sistem Penuaian Tenaga Frekuensi Radio (RFEH). Walau bagaimanapun, prestasi terjejas dengan ketara oleh kehilangan pengaliran dan pengembalian yang tinggi dalam operasi subambang. Walaupun wujudnya teknik pincang get dinamik (DGB) yang bertujuan untuk mengurangkan kedua-dua kehilangan pengaliran dan penbalikan, kerugian ini tidak dapat dihapuskan sepenuhnya, mengakibatkan prestasi rendah penerus dan litar CP. Tambahan pula, julat luas kuasa input terkumpul daripada sistem RFEH boleh mengakibatkan paras voltan keluaran tinggi yang mungkin menimbulkan risiko merosakkan beban WSN. Tesis ini membentangkan ulasan komprehensif mengenai teknik penerus dan penambahbaikan CP terkini dan menyediakan analisis menyeluruh tentang ciri-ciri penerus terkini dan litar CP. Dengan mempertimbangkan pertukaran, beberapa peningkatan dicadangkan untuk mengoptimumkan komponen ini khusus untuk operasi subambang, bertujuan untuk meningkatkan kecekapan penukaran kuasa (PCE). Kerja ini mencadangkan teknik pincang pintu dinamik maju baru yang memfokuskan pada mengurangkan kehilangan pengaliran hadapan dan kehilangan kebocoran arus songsang dalam penerus dan CP. Khususnya, DGB pendahuluan digabungkan dengan pasangan transistor dwi-suis NMOS-PMOS yang bertindak sebagai suis sekunder untuk mengurangkan lagi kerugian.

Dengan melaksanakan gabungan ini, seni bina yang dicadangkan mencapai CP operasi subambang input ultra-rendah (0.1 V) dengan PCE sebanyak 43.4 %. Selain itu, CP selari siri yang boleh dikonfigurasikan semula menggunakan pengayun disuap sumber dinamik dengan 62 % PCE diperkenalkan. Akhir sekali, RFEH bersepadu yang menampilkan unit pemantauan voltan kuasa rendah dengan kater keluaran sempadan 3.3 V direka bentuk untuk memenuhi aplikasi WSN. Penyelidikan ini menyumbang kepada pemahaman dan kemajuan penerus dan CP, dan reka bentuk sistem RFEH bersepadu sepenuhnya, membolehkan penggunaan tenaga yang lebih cekap dalam WSNs.

Kata Kunci: penuaian tenaga frekuensi radio, pam caj CMOS, penukar DC-DC, kecekapan penukaran kuasa, operasi subambang

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LIST OF SYMBOLS AND ABBREVIATIONS

AC	:	Alternating Current
AM	:	Amplitude Modulation
BTRO	:	Bootstrapped Ring-Voltage Controlled Oscillator
CCCP	:	Cross-Coupled Charge Pump
CCDD	:	Cross-Couple Differential Drive
CMOS	:	Complementary Metal-Oxide-Semiconductor
CP	:	Charge Pump
CTS	:	Charge Transfer Switch
dBm	:	decibel-milliwatts
DC	:	Direct Current
DGB	:	Dynamic Gate Biasing
DRC	:	Design Rule Check
EM	:	Electromagnetic
F	:	Farad
FCC	:	Federal Communications Commission
FM	:	Frequency Modulation
GSM	:	Global Systems for Mobile
IC	:	Integrated Circuit
IMN	:	Impedance Matching Network
IoT	:	Internet Of Things
IRS	:	Input-Representing-Signal
LVS	:	Layout Vs. Schematic
LVT	:	Low-Voltage-Threshold
MCMC	:	Malaysian Communications and Multimedia Commission
MIM	:	Metal-Insulator-Metal
MOM	:	Metal-Oxide-Metal
MOS	:	Metal–Oxide–Semiconductor
NMOS	:	N-Channel Metal-Oxide Semiconductor

NOC	:	Non-Overlapping Clocks
OVC	:	Oscillator Voltage Controller
PCE	:	Power Conversion Efficiency
PEX	:	Parasitic Extraction
PFM	:	Pulse Frequency Modulation
PMOS	:	P-Channel Metal-Oxide Semiconductor
PMU	:	Power Management Unit
PWM	:	Pulse Width Modulation
RF	:	Radio Frequency
RFEH	:	RF Energy Harvesting
R_{ON}	:	on-Resistance
RVCO	:	Ring Voltage Controlled Oscillator
SoC	:	System-on-A-Chip
TSMC	:	Taiwan Semiconductor Manufacturing Company
V	:	Volt
VCE	:	Voltage Conversion Efficiency
VCO	:	Voltage Controlled Oscillator
VCR	:	Voltage Conversion Ratio
V_{DS}	:	Drain-To-Source Voltage
V_{GS}	:	Gate-To-Source Voltage
VOSC	:	Oscillator's Input Voltage
V_{TH}	:	Threshold Voltage
W	:	Watt
WSN	:	Wireless Sensor Network
WTP	:	Wireless Power Transfer
Φ	:	Clock Signal
Ω	:	Ohm

CHAPTER 1 : INTRODUCTION

This chapter of the thesis introduces the research work, including a comprehensive background study and an overview of the topic. It identifies and discusses the problem statement and motivation behind the research and sets out the research objectives as well as the research methodology employed in the study. The chapter concludes by highlighting the contributions of the work and presenting the overall thesis outline.

1.1 Background Study and Motivation

Wireless Sensor Networks (WSN) have emerged as a key technology for monitoring and collecting physical environmental conditions through wireless links in recent years due to the advancement in Internet of Things (IoT) and cloud computing technology. Based on Morgan Stanley Research (Stanley, 2016), WSN is anticipated to be the highest number count of electronic gadgets within the IoT infrastructure due to the explosive growth of electronic devices and its wide use of applications. WSN is a type of network that consists of numerous wireless sensors distributed in a particular area or environment. It is designed to collect and transmit data from the sensors to a central location or server for processing and analysis. Due to its versatile nature, WSN finds ubiquitous use in various applications throughout modern society. Some of its broad range of applications include healthcare monitoring, environment monitoring, industrial monitoring and pandemic monitoring (Ali et al., 2017; Xu et al., 2014). Table 1.1 delineated the detail WSN application and the type of sensors used.

Table 1.1: Application of WSN in Recent Work (Ali et al., 2017)

Application	References	Uses	Sensors	City Deployed in
Environmental monitoring	(Jiang et al., 2016)	Air Quality	NO2 Sensors	Amsterdam, The Netherlands
	(Hasenfratz et al., 2015)	Air Pollution Maps	Particles (UFPs), Temperature, Humidity	Zurich, Switzerland
	(Mao et al., 2012)	CO2 Monitoring	CO2, Temperature, Light Sensors	Wuxi, China
	(Boustani et al., 2011)	Waste Removal	Global System for Mobile (GSM) Tracking Sensors	New York, Seattle
Biomedical	(Hii & Chung, 2011)	Ubiquitous Healthcare Solution	Electrocardiogram (ECG) Sensor Node, 3G, Code Division Multiple Access (CDMA), GSM	Busan, Korea
	(Kakria et al., 2015)	Real time health monitoring System	Wearable Biosensors, Android Device, Smart Phone	Pathum Thani, Thailand
	(Yan et al., 2017)	Structural Health Monitoring System	Wireless Smart Aggregate sensor, RF Module, Sampling Module, Gateway	Shenyang, China
Wireless Body Area Network	(Wu et al., 2017)	Monitoring of Body Temperature, Heartbeat	Internet of Things	-
	(Kantoch et al., 2014)	Monitoring of Temperature, Heart Rate, Skin Humidity	Computer, Bluetooth	-
	(Woon-Sung et al., 2013)	Fall detection	Accelerometer, gyroscope, video camera, Infrared sensor	-
Vehicle and traffic monitoring	(Dagher et al., 2014)	UNS—Ubiquitous Navigation System	RF based, Google Maps	Lille, France
	(Srinivasan et al., 2016)	FWI—Fire Weather Index	Internet of Things, GPS Sensors	Oman

At present, batteries serve as the primary power source for WSNs. However, the currently available battery in the market (Sudevalayam & Kulkarni, 2011) poses several limitations such as size, weight, and the need for frequent replacements and maintenance. The labour-intensive nature of frequent replacing and maintaining bulky batteries for sensor nodes deployed over a wide region renders it impractical to use them as the primary energy source for WSNs in IoT applications. Therefore, there is a pressing need to explore alternative energy sources such as energy harvesting to extend their functionality.

Energy harvesting is a process of capturing and storing energy from various sources, such as light, heat, motion, or vibration, and converting it into electrical power to sustain the operations of electronic devices or systems. Harvesting energy source is categorized into different categories based on their controllability and predictability (Kansal et al., 2007). As WSNs require a constant energy source 24/7 to operate, uncontrollable energy such as solar energy is not suitable due to its unavailability at night. Unpredictable energy such as kinetic and wind are also deemed to be impractical for their inconsistent availability. Ambient radio frequency (RF) energy is a viable and sustainable solution for powering WSNs (Soyata et al., 2016). It is available through Electromagnetic (EM) wave transmission by Television towers, Global systems for mobile (GSM) towers, Radio networks, Wi-fi, etc. Despite having a lower power density than other sources such as solar and kinetic energy, recent surveys conducted between 2016 and 2021 have shown that the power density of RF energy ranges between 0.06 to 0.57 $\mu W/cm^2$ globally, thus confirming the feasibility of harvesting ambient RF energy for WSN applications (Ho et al., 2022). As WSN requires a constant cellular internet connection to operate for IoT applications, the presence of RF energy for harvesting is assured. Hence, RF energy harvesting (RFEH) is the ideal energy solution for powering WSNs.

Furthermore, the cost-effective nature of complementary metal-oxide-semiconductor (CMOS) technology enables a system-on-a-chip (SoC) design solution for RFEH systems, facilitating the creation of fully integrated, small form factor RF-powered WSNs. Previous works on RFEH have demonstrated the generation of stable direct current (DC) power through RF energy harvesting (Abouzied et al., 2017; Ramalingam et al., 2021). However, these RFEH circuits experience significant power losses, particularly when transistors operate in the subthreshold region due to the low operational voltage obtained from the harvested RF energy. This study aims to enhance the efficiency of RFEH systems, specifically in the design of the charge pump (CP) block, in order to minimize power losses in RFEH systems with low input voltages.

1.2 Problem Statement

Figure 1.1 shows the general RFEH system block diagram. It consists of an RF antenna to harvest ambient RF energy, an Impedance Matching Network (IMN) to match the impedance of the antenna and the RFEH system for maximum power transfer, a rectifier to convert the scavenged alternating current (AC) power to a usable DC power, a CP to step-up the rectified power and a control unit to manage the output voltage to ensure the compatibility with the WSN application. Designing an RFEH system poses a significant challenge primarily due to the low voltage obtained from the scavenged RF, which causes high conduction and reversion losses in the rectifier and charge pump blocks, ultimately leading to a low-efficiency RFEH system. The primary focus of this work is to improve the design topology of a low-voltage CP for WSN application.

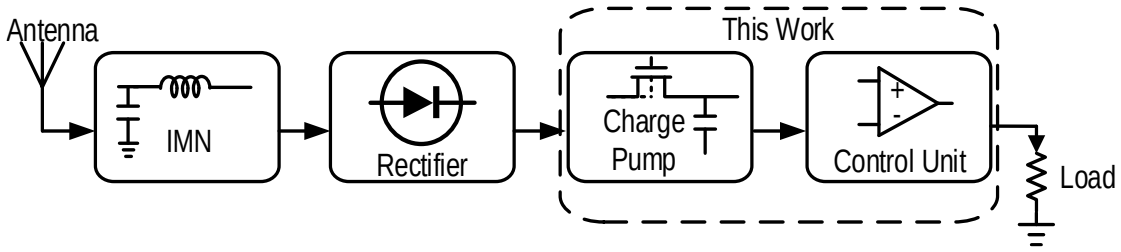

Figure 1.1: General System Diagram of an RF-Based Energy Harvesting System

The two most common CP architectures are Dickson and cross-coupled topology. The diode-connection transistor in Dickson topology offers the advantage of zero reverse current leakage at the cost of high threshold voltage (V_{TH}) drop.

In the recently published works, many have explored a variety of techniques and architecture to improve the CP performance. Yet, only a few works focus on the low input voltage scenarios that are relevant to the RFEH application. The power harvested from ambient RF is relatively low compared to other energy harvesters such as solar and piezoelectric. Conventional CP architectures are not suitable for RFEH applications due to their low scavenged input voltage. This is because the transistors in the CP are working in the subthreshold region and are not able to be fully turned ON/OFF. This leads to a massive forward conduction and reversion-leakage loss which greatly deteriorates the RFEH performance. Therefore, a novel CP and rectifier architecture that aims to reduce the forward conduction and reverse-leakage loss is required to design a high-efficiency RFEH system at low input voltage.

Another challenge in RFEH systems is the fluctuating input voltage. Existing CP topologies are typically designed and optimized for a specific voltage level. However, in energy harvesting applications, the input voltage can vary significantly, ranging from 0.2 V to 0.6 V. This wide voltage fluctuation makes it difficult for conventional CPs to maintain high efficiency across the wide input voltage range. To address this limitation, a reconfigurable CP that can adapt to these input voltage variations is crucial.

Furthermore, a notable challenge arises in maintaining a consistent output voltage within the RFEH system due to the inherent fluctuations in the harvested input power. Presently, state-of-the-art voltage limiters rely on external power sources to establish a voltage reference or to drive the control switches, rendering them ill-suited for self-sustaining energy harvesters. Additionally, the existing batteryless voltage limiter works consume substantial power, rendering them unsuitable for application in low-power RFEH systems.

1.3 Research Objectives

The objective of this research is to develop a novel highly efficient subthreshold operation CP topology and a fully integrated RFEH system with an output voltage monitoring unit tailored for WSN applications. The existing state-of-the-art CMOS CP topologies are geared toward high-voltage applications that are not suitable for RFEH systems (Feng et al., 2006; Shin et al., 2010; Yu et al., 2017). Furthermore, the-state-of-the-art improvement in low-voltage CP designs continue to grapple with high conduction and reversion losses, hindering their power conversion efficiency (PCE) from surpassing the 40% barrier (A. Ballo et al., 2020b; Chen et al., 2012; Fuketa et al., 2017). Besides that, the high unregulated scavenged output voltage poses the risk of damaging the WSN load (Wang & Kose, 2018). Therefore, this research seeks to develop innovative techniques and investigate novel topologies to enhance the performance of ultra-low voltage CP for RF energy harvesting with output voltage limiting capability.

The objectives of this research are listed below.

i. To design and develop a novel high-efficiency ($>$ 40 %) subthreshold operation CMOS DC-DC converter for low input voltage energy harvesting application.

ii. To engineer and fabricate a reconfigurable CP with output voltage limiting capability across a broad input voltage spectrum spanning from 0.26 V to 0.64 V.

iii. To design and develop a novel dynamic source-fed oscillator to achieve frequency modulation for reconfigurable CP, accommodating a wide input voltage variation.

iv. To design and implement a novel low-power voltage monitor and voltage limiter to effectively constrain the output voltage of the RFEH system under a boundary threshold of 3.3 V, catering specifically towards WSN applications.

1.4 Research Methodology

Figure 1.2 illustrates the comprehensive research methodology of this thesis. The process commences with an extensive background study and literature review of conventional subthreshold operation rectifiers and CP topologies, reconfigurable CP, frequency modulation, and the voltage limiter for RFEH systems. Subsequently, the process advances to the identification of problems and research gaps, as well as the delineation of the research scope drawing from the earlier literature review. Following this, the methodology proceeds with the development of an innovative CP design that leverages the dynamic gate biasing (DGB) technique to achieve high PCE during subthreshold operation. A rigorous simulation process is conducted to validate the circuit's performance, ensuring its effectiveness under subthreshold conditions. Upon completion of circuit optimization, the design will proceed to fabrication if it attains the target performance threshold of over 40 % PCE. In case the target is not met, a redesign of the circuit will be initiated.

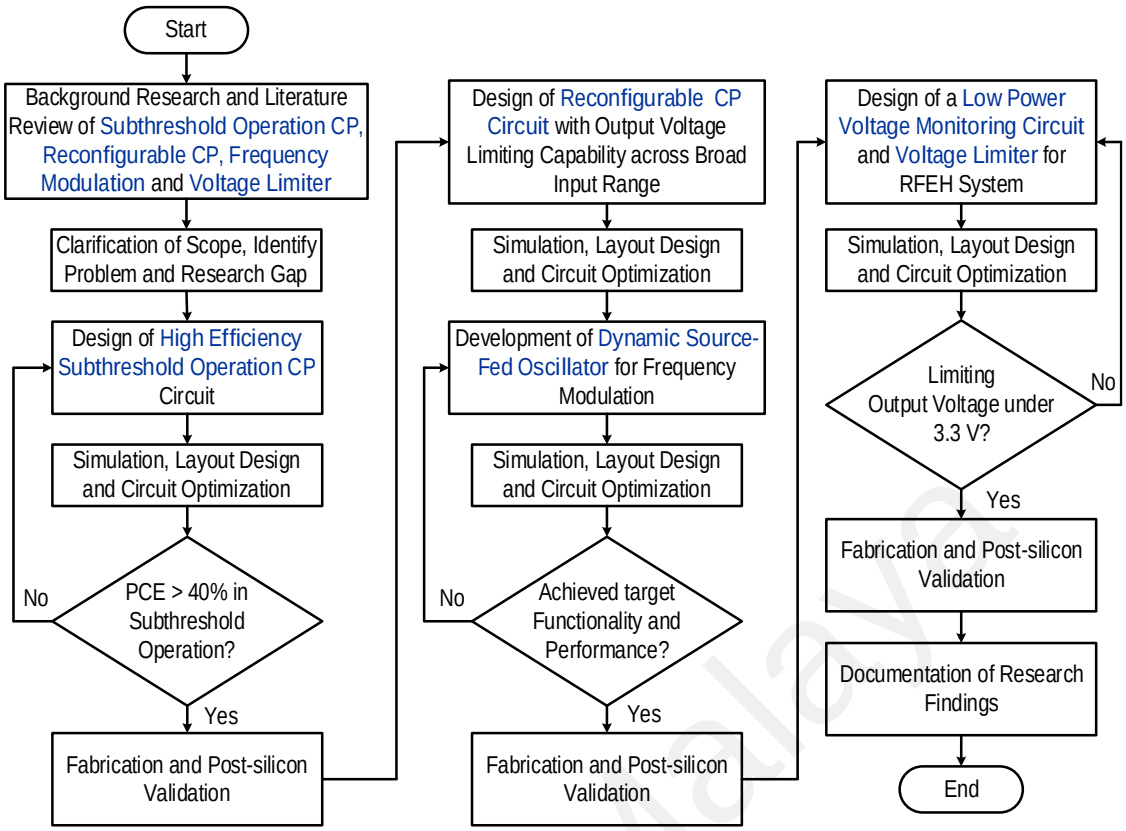

Figure 1.2: Research Methodology Flow Chart

Subsequently, a series-parallel reconfigurable CP circuit with output-limiting capability is designed using an ideal clock with a fixed frequency. Following an iterative simulation and testing phase, the work enters the next design phase to develop a dynamic source-fed oscillator to perform frequency modulation to accommodate the fluctuating wide input voltage. The iterative simulation and testing of the reconfigurable CP circuit are once again performed with the inclusion of the dynamic source-fed oscillator. The design advances to the fabrication stage once satisfactory results have been attained.

Next, the project explores an alternative output voltage limiting technique with the design of a novel low-power voltage monitoring unit and a voltage limiter calibrated to maintain a consistent output voltage under 3.3 V. Extensive design and layout simulations are conducted, and the design will be sent for fabrication once it satisfies the predefined design constraints.

The circuit layout of the designed circuits is constructed based on the circuit schematics. The layout undergoes two essential rule checks: the Design Rule Check (DRC) to ensure compliance with fabrication requirements and the Layout vs. Schematic (LVS) check to verify layout consistency with the schematic. Following the successful completion of these checks, a Parasitic Extraction (PEX) is performed to account for parasitic losses, enabling post-layout verification.

All the designed circuits are realized using Cadence software and fabricated under Taiwan Semiconductor Manufacturing Company's (TSMC) 65 nm CMOS technology. Upon fabrication, post-silicon validations are conducted to obtain the measurement result of the designs' performance. The acquired results are meticulously analyzed and compared with recently published works to emphasize the research contributions. Finally, the research findings are compiled and thoroughly documented for research publications.

1.5 Contributions of the Research Work

The contributions of this work are highlighted as shown below.

i. A novel CP architecture for low-power RFEH system with high Power Conversion Efficiency (PCE) in subthreshold operation with chip verification.

ii. A reconfigurable series-parallel CP with output voltage limiting capability across a broad input voltage spectrum spanning from 0.26 V to 0.64 V.

iii. A novel dynamic source-fed oscillator with frequency modulation ability to adapt to a wide input voltage range.

iv. SoC solution capabilities of the CCCP topology for system integration for ambient RFEH and WSN application.

v. A novel low-power voltage monitoring circuit and voltage limiter to maintain a boundary voltage of 3.3 V for IoT WSN applications.

1.6 Scope of Work

The primary focus of this study is to design a highly efficient RFEH system. As illustrated in Figure 1.1, the RFEH system comprises an IMN, rectifier, CP, and logic control unit. However, this investigation is solely centred on the design of the RFEH backend system, which is the CP and the output voltage control unit. To simulate the frontend section of the RFEH, a DC source with a series resistor is employed to supply the Thevenin voltage to the CP, allowing for an accurate evaluation of its performance. A comprehensive outline of the experimental setup will be presented in Chapter 3.4.1. It is noteworthy that since the CP and rectifier share the same topology, all the enhancement methods outlined in this work can be implemented on the rectifier unless otherwise specified.

1.7 Thesis Outline

This thesis comprises five chapters that cover various aspects of the research. Chapter 1 introduces the research background and presents the problem statement and motivation behind the study. It also outlines the research objectives and highlights the contributions of the research work. Chapter 2 provides a comprehensive literature review, focusing on RF power availability, CMOS RFEH circuit overview, and the latest advancements in rectifier and charge pump improvement techniques for high-efficiency operation. This review serves as a foundation for the subsequent chapters. In Chapter 3, the thesis delves into the proposed advanced DGB technique for CP design. The chapter also includes a comparison of the research findings with recent publications, highlighting the novelty and effectiveness of the proposed technique. Chapter 4 presents a novel reconfigurable series-parallel CP with output-limiting capabilities featuring a novel dynamic source-fed oscillator for frequency modulation. Chapter 5 delves into the design of an integrated

RFEH system with a novel low-power voltage monitoring unit capable of limiting the output voltage under a boundary level of 3.3 V for WSN applications. Finally, Chapter 6 concludes the thesis and explores the future work for the research.

CHAPTER 2 : LITERATURE REVIEW

2.1 Chapter Overview

This chapter delves into a comprehensive literature review of the RFEH system, starting with an investigation of the RF power availability for energy harvesting. It is followed by an in-depth overview of the conventional CMOS rectifier and CP architecture, providing valuable insights into the existing designs and their operation principles. Furthermore, it provides a comprehensive literature review on the state-of-the-art rectifier and CP improvement techniques with a discussion of their strengths and limitations. The chapter concludes with a summary of the key findings and contributions of the literature review.

2.2 RF Energy

2.2.1 Background

RF energy is an electromagnetic wave propagating in a free space medium for information transformation (Visser & Vullers, 2013; Vullers et al., 2009). The RFEH system can be classified into two categories, namely Near-field and Far-field, based on the propagation distance. The boundary between these two types of RFEH is determined by the Fraunhofer distance (Selvan & Janaswamy, 2017). A Near-field RFEH is commonly known as Wireless Power Transfer (WTP). It is achieved by transmitting energy through two magnetic-coupled coils placed in close proximity (S. Kim et al., 2014). In contrast, a Far-field RFEH system is designed to collect residual electromagnetic RF energy that is propagated through the air. This form of energy is generated by radio transmission antennas found in devices such as base stations, Wi-Fi routers, and Bluetooth-enabled devices. The power density harvested by a Far-field RFEH system is comparatively lower than that of a Near-field RFEH system due to the

increased propagation distance, which is explained by the Friis transmission equation, showing in the equation (2.1) below. (Friis, 1946).

$$\boldsymbol{P_{ANT} = \frac{P_T G_T G_R c^2}{(4\pi D f)^2}} \tag{2.1}$$

where P_{ANT} is the received power, P_T is the transmitted power, G_T is the antenna gain of the transmit antenna, G_R is the antenna gain of the receive antenna, c is the speed of light, f is the RF wave frequency and D is the distance of RF transmission between the transmit and receive antennas.

The scope of this thesis is centered around Far-field RFEH systems, with a specific focus on the application in low-power WSN. It is important to note that the term RFEH as denoted in this thesis exclusively refers to Far-field RFEH systems.

2.2.2 RF Availability

Ambient RF energy is widely available as it is designated for specific uses in data transmission in telecommunication, such as Amplitude Modulation (AM) radio, Frequency Modulation (FM) radio, television, cellular communications, Wi-Fi, and Bluetooth. These RF bands are allocated by the International Telecommunication Union and are regulated by the regulatory bodies, such as the Federal Communications Commission (FCC) in the United States, and Malaysian Communications and Multimedia Commission (MCMC) to avoid interference and ensure efficient use of the radio spectrum (Hesser & Hamburg, 1995).

Table 2.1 tabulates the measured RF power density at different frequency bands from various locations (Adam et al., 2017; Pinuela et al., 2013; Roy et al., 2021; Zeng et al., 2017). From Table 2.1, it is evident that the prospect of harvesting RF energy from ambient sources, including TV, GSM, and WLAN base stations, holds great promise, as these signals are omnipresent in urban environments. Nevertheless, it is important to

Table 2.1: Measured RF Power Density at Different Frequency Bands from Various Locations

Band	Frequency	Location	Average Power	Peak Power
Digital TV	470 MHz – 610 MHz	[a]Underground Station	0.89 nW/cm^2	460 nW/cm^2
GSM 900 (2G)	800 MHz – 915 MHz	[a]Underground Station	36 nW/cm^2	1930 nW/cm^2
	880 MHz – 960 MHz	[c]Semi-urban/ urban Areas	-34.9/-26.65 dBm	-22.66/-7.65 dBm
	925 MHz – 960 MHz	[d]University	n.a.	-22.5 dBm
	935 MHz – 960 MHz	[b]Shopping Center	-50/-56 dBm	-45/-52 dBm
GSM 1800 (2G)	1.805 GHz – 1.88 GHz	[a]Underground Station	84 nW/cm^2	6390 nW/cm^2
		[d]University	n.a.	-17.8 dBm
	1.805 GHz – 1.85 GHz	[b]Shopping Center	-55/-48 dBm	-54.9/-39 dBm
UMTS (3G)	1.92 GHz – 2.2 GHz	[c]Semi-urban/ urban Areas	-43.27/-13.33 dBm	-29.09/-10.65 dBm
	2.11 GHz – 2.17 GHz	[a]Underground Station	12 nW/cm^2	240 nW/cm^2
	2.11 GHz – 2.23 GHz	[d]University	n.a.	-23 dBm
WiFi	2.32 GHz – 2.575 GHz	[b]Shopping Center	-70/-65 dBm	-61/-60 dBm
	2.39 GHz – 2.4 GHz	[d]University	n.a.	-25.6 dBm
	2.4 GHz – 2.5 GHz	[a]Underground Station	0.18 nW/cm^2	6 nW/cm^2
		[c]Semi-urban/ urban Areas	-43.19/-24.8 dBm	-29.92/-15.56 dBm
LTE (4G)	2.5 GHz – 2.7 GHz	[d]University	n.a.	-26.5 dBm

[a]London Underground stations, UK; [b]Shunde shopping center/ residential area, China; [c]Kedah and Perlis (semi-urban area)/ Penang (urban area), Malaysia; [d]Multimedia University, Selangor, Malaysia

acknowledge that the harvested RF power is relatively lower compared to the other renewable energy sources such as solar, wind, and kinetic energy. As a result, its feasibility is confined to a restricted range of WSN applications. There has been a notable surge in research interest surrounding the development of high-efficiency RFEH systems specifically tailored for low-power operations to resolve the mentioned issue.

2.3 RFEH Circuit

Figure 2.1 illustrates the block diagram of an RFEH system, compromising two distinct components. The front-end circuit serves the purpose of harvesting ambient RF energy and converting it into DC power. On the other hand, the back-end circuit is responsible for the management and step-up of the harvested DC power to a higher voltage level suitable for the intended output WSN application.

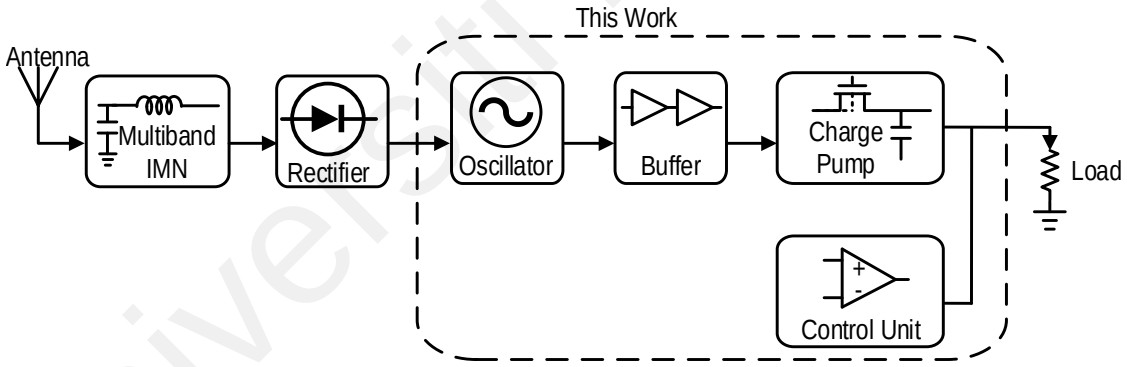

Figure 2.1: Block Diagram of an RF-DC Energy Harvester

2.3.1 RFEH Front-End Circuit

The front-end circuit consists of a receiving antenna, an IMN, and a rectifier. The antenna captures the ambient and transfers it to the rectifier for voltage rectification. The IMN resides between the antenna and the rectifier to resonate the impedance of the antenna to the RFEH system for maximum power transfer.

Conventionally, a 50 Ω antenna is widely utilized in RF applications to correlate a balance between low loss and power handling capabilities, particularly for coaxial connections (Gilmour, 1986). The harvested RF voltage from the antenna can be determined by equation (2.2) (Karthaus & Fischer, 2003):

$$\boldsymbol{V_{ANT}} = \sqrt{\boldsymbol{8 \times R_{ANT} \times P_{ANT}}} \tag{2.2}$$

where $\boldsymbol{V_{ANT}}$ is the receive antenna's peak input voltage, $\boldsymbol{R_{ANT}}$ is the receive antenna's radiation resistance, and $\boldsymbol{P_{ANT}}$ is the harvested ambient RF power from the antenna.

The scavenged voltage from the antenna is particularly low, in the range of milli-Volts due to the lower ambient RF power as mentioned in section 2.2.2 previously. The lower voltage will deteriorate the performance of the subsequent RFEH block. Therefore, many RFEH works have proposed techniques and topologies to improve the rectifier and CP performance in low input voltage applications.

The RF-DC rectifier serves as the central component within the front-end RFEH system. Its primary role involves the conversion of harvested RF power into usable DC power, which is then transmitted to the back-end circuit for subsequent management and processing. The utilization of CMOS-based rectifiers is widely preferred in RFEH systems, primarily due to their ability to be implemented on-chip. These rectifiers consist of a series of rectifying transistors and flying capacitors that work in tandem to ensure the conversion of AC into a unidirectional current flow, thereby achieving the desired rectification effect. Multiple stages of rectifiers can be cascaded in series to increase the voltage gain for voltage multiplication.

2.3.2 RFEH Back-End Circuit

The RFEH back-end circuit is further divided into two parts, the DC-DC converter for voltage boosting and the Power Management Unit (PMU) for ensuring a stable and reliable output voltage is delivered to the load. Although the rectifier can achieve voltage boosting by cascading multiple rectifier stages, the high switching frequency inherent in the RF waves can result in substantial switching losses within the rectifying transistors. To mitigate these losses, numerous prior RFEH designs have incorporated a dedicated DC-DC converter (Colella et al., 2016; Seong et al., 2016; You et al., 2011; Zhang & Lee, 2010). The utilization of a DC-DC converter offers flexibility in frequency operation and enables output voltage regulation using techniques such as Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM). By operating at a lower frequency than the RF wave, the DC-DC converter allows for precise control over the output voltage while minimizing switching losses. This enhances the overall performance and efficiency of the energy harvesting system.

There are two basic types of DC-DC converter namely inductive boost converter and switch capacitor converter. While inductor-based boost converter exhibits superior performance in power conversion and can achieve high efficiencies at very low input voltages (Goeppert & Manoli, 2016; Ramadass & Chandrakasan, 2010; Wens et al., 2007), the necessity of bulky off-chip inductor hinders its implementation in monolithic design (Shih & Otis, 2011). Consequently, a capacitive DC-DC converter emerges as the preferred choice in an integrated RFEH system for WSN application.

A switch capacitor converter, commonly referred to as a CP, operates on the fundamental principles of charge transfer and charge conservation (Rodriguez et al., 2016). The switch capacitor converter stores charge in a flying capacitor during the initial

pumping cycle and transfer them to the subsequent stages of the CP to achieve voltage boosting. The pumping operation is governed by two complementary clocks generated by the ring oscillator and the buffer circuit.

Ring oscillators are widely used in CP operations as clock signal generators due to their compact design and ease of implementation. It compromises a series of cascading inverters in an odd number of stages. The sinusoidal waveform generated by the oscillator will subsequently be directed into a buffer circuit to shape it into a square wave clock signal. Generally, the buffer circuit will generate two complementary clock signals for the CP operation.

There are different types of complementary clock signals for CP as depicted in Figure 2.2. According to the research conducted by Feng et al. (2006), non-overlapping clocks (NOC) have been identified as the optimal choice for CP operations, primarily due to the ability to reduce reversion loss across the pumping transistors. The type-I clock scheme is typically preferable for N-channel Metal-Oxide Semiconductor (NMOS) transistors in charge pump circuits because it includes a period where both clocks are low. This ensures that the NMOS transistors are turned off before a significant potential difference is established, thus preventing reversion loss and undesired charge transfer. Conversely, the non-overlap type-II clock scheme is more suitable for P-channel Metal-Oxide Semiconductor (PMOS) transistors in charge pump circuits, as it provides a period where both clocks are high, effectively preventing reversion loss by ensuring that the PMOS transistors remain turned off during that time.

The NOC generator can be constructed using either NAND gates (Bose et al., 2019; Kim et al., 2015) or NOR gates (Yu et al., 2017; Zhang & Lee, 2013) as shown in Figure 2.3. It consists of two components: the logic gate, which ensures the generation of non-

overlapping clock signals, and the buffer series, which facilitates the generation of square wave clock signals.

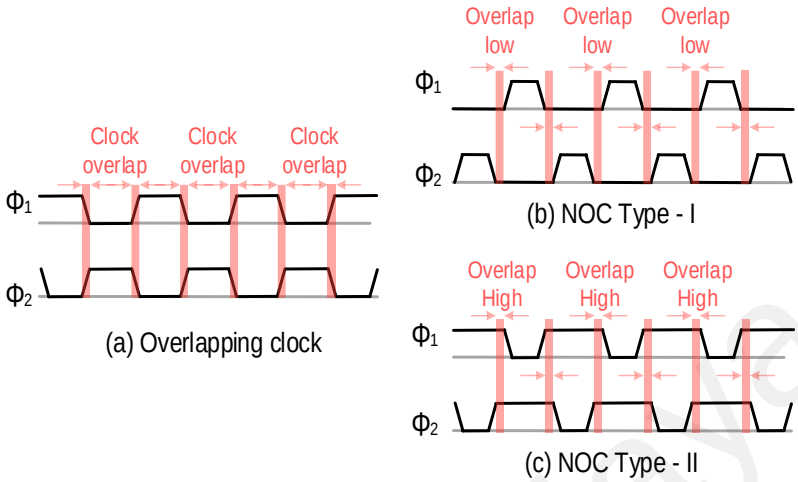

Figure 2.2: Different Types of Complementary Clock Signals for CP Operation (a) Conventional Overlapping Clock Scheme (b) Non-Overlap Type-I Clock Scheme (c) Non-Overlap Type-II Clock Scheme

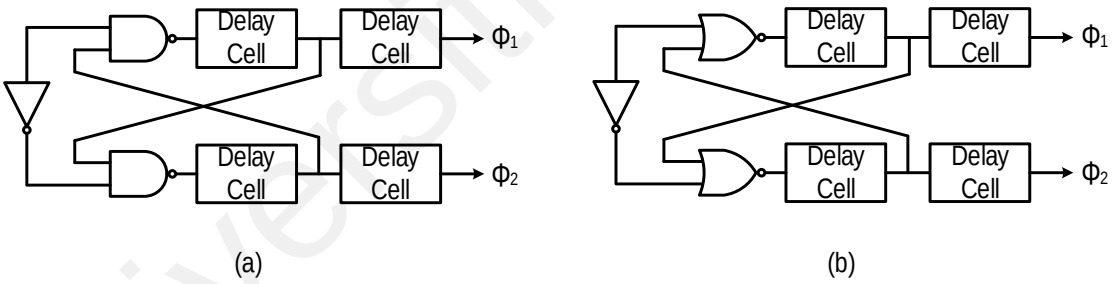

Figure 2.3: Schematic Block Diagram of Non-Overlap Clock Generator using (a) NAND Gates and (b) NOR gate.

2.3.3 Performance Evaluation Parameters

In assessing the performance of RFEH systems, several indicators are utilized to evaluate their effectiveness. Key indicators commonly employed for RFEH performance evaluation include:

a) Sensitivity

Sensitivity refers to the ability of an RFEH system to capture and convert RF energy. It is the measure of the minimum input power required for the RFEH system to produce a 1 V DC output voltage at the desired condition. The representation of the RFEH sensitivity is given in equation (2.3) below (Chong et al., 2018):

$$\boldsymbol{P_{dBm} = 10\log_{10}(P_{mW})} \tag{2.3}$$

Where P_{mW} is the input power in milli-Watt. The sensitivity is evaluated in dBm as the RF power received is in the range of milli or micro-watts.

b) Power Conversion Efficiency

Power Conversion Efficiency or PCE, is an indicator that measures the ability of the RFEH system to convert harvested RF power into usable DC power. The PCE is calculated by dividing the output DC power by the input RF power, expressing the efficiency of energy conversion shown in equation (2.4) (Poo et al., 2021):

$$\boldsymbol{PCE_{RFEH} = \frac{P_{OUT}}{P_{IN}} = \frac{V^2{}_{OUT} \times R_{LOAD}}{P_{IN}}} \tag{2.4}$$

where P_{OUT} and P_{IN} is the output power of the RFEH respectively, V_{OUT} is the output voltage and R_{LOAD} is the load resistance.

PCE is also an important indicator to evaluate the DC-to-DC power conversion efficiency for the back-end RFEH circuit. It is a measure of the ratio of the boosted DC output power to the input DC power as in equation (2.5) (Churchill et al., 2020):

$$\boldsymbol{PCE_{CP} = \frac{P_{OUT,CP}}{P_{IN,CP} + P_{PERI}}} \tag{2.5}$$

where $P_{OUT,CP}$ is the output power of CP, $P_{IN,CP}$ is the input power of CP and P_{PERI} is the power consumption of the peripheral circuits.

c) Voltage Conversion Efficiency

The voltage conversion efficiency, VCE, is an indicator for the RFEH backend evaluation parameter which measures the ability of the DC-DC converter to amplify the harvested DC voltage to a higher output voltage level (Churchill et al., 2020):

$$\boldsymbol{VCE_{CP}} = \frac{\boldsymbol{V_{OUT,CP(actual)}}}{\boldsymbol{V_{OUT,CP(ideal)}}} \tag{2.6}$$

where $V_{OUT,CP(actual)}$ is the actual measured output voltage of CP while $V_{OUT,CP(ideal)}$ is the ideal output voltage of CP without losses.

2.3.4 Subthreshold Operation

2.3.5 Types of Power Losses in Rectifier and CP

Efficient identification and mitigation of power losses in transistors play a crucial role in optimizing the performance of RFEH systems. These losses, encompassing forward conduction losses, reverse current losses, and switching losses, are typically observed in key components such as the rectifier and the DC-DC converter, necessitating careful attention for improving overall system efficiency.

a) Forward Conduction Loss

Forward conduction loss refers to the power dissipated when current flows through a transistor during the forward conduction phase due to the internal resistance of the transistor as shown in equation (2.7) (Jung et al., 2014):

$$\boldsymbol{P_{conduction}} = \boldsymbol{C} \times \Delta^{\boldsymbol{2}} \times \boldsymbol{f_{SW}} \tag{2.7}$$

where C is the pumping capacitance, f_{SW} is the switching frequency and Δ is the voltage drop due to the on-resistance of the transistor. The forward conduction loss can also be expressed in terms of current loss as in equation (2.8) (Ling & Dongsheng, 2008):

$$\boldsymbol{P_{conduction} = R_{ON} \times f_s \int_0^{DT} i^2(t)dt} \tag{2.8}$$

where the on-resistance (R_{ON}), which is the internal resistance of a conducting transistor given by equation (2.9) (Churchill et al., 2020):

$$\boldsymbol{R_{ON} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}} \tag{2.9}$$

The parameter μ represents the mobility of electrons or holes in a semiconductor material, while C_{ox} denotes the oxide capacitance, which is a technology-dependent parameter related to the capacitance of the insulating oxide layer. It is evident from the expression that increasing the gate-to-source voltage (V_{GS}) and the width of the transistor (W) can help reduce the on-resistance and, consequently, minimize conduction losses.

b) Switching Loss

Switching loss is the total dynamic power loss due to the switching transitions of a transistor. It occurs when the device undergoes rapid changes in its conducting or non-conducting state. During switching, there is a brief period where the device is neither fully OFF nor fully ON, resulting in a temporary overlap between the current flows. The expression of switching loss is given by equation (2.10) (Prado et al., 2022):

$$\boldsymbol{P_{Switching} = \frac{1}{2}(t_{ON} V_{DS} I_{ON} + t_{OFF} V_{DS} I_{OFF}) \times f_{SW}} \tag{2.10}$$

where V_{DS} is the drain-to-source voltage of the CMOS transistor, and I_{ON}, I_{OFF}, t_{ON}, t_{OFF} are the respective current and overlap duration of the transistor turn-on and turn-off phases. Equation (2.10) demonstrates the significant impact of switching frequency on the switching loss, emphasizing the need to minimize the frequency for effective reduction of overall switching losses. Furthermore, the switching loss is inversely proportional to the conduction loss. This correlation implies that mitigating switching losses may lead to an increase in conduction losses, and vice versa. Hence, achieving an

optimal balance between these two losses becomes essential in order to optimize the performance of the system and maximize energy efficiency.

c) Reverse Current Loss

Reverse current loss, also known as reverse charge leakage, pertains to the undesired leakage or backflow of charge from the subsequent rectifier or CP stages to the preceding stages. The expression of reversion loss is given by equation (2.11) (Ling & Dongsheng, 2008):

$$\boldsymbol{P_{reverse} = \frac{1}{2}\left(\frac{C_b C_L (V_{OUT} - V_b)^2}{C_b + C_L}\right) \times f_{SW}} \tag{2.11}$$

where C_b is the pumping capacitance, C_L is the load capacitance, V_{OUT} is the output voltage, V_b is the pumping voltage and f_{SW} is the switching frequency. The phenomenon of reversion loss occurs when the pumping transistors fail to effectively turn OFF during the reverse conduction phase, leading to a diminished transfer of charges to the output. Several factors can contribute to the improper turn-off of transistors, including variations in the V_{TH}, inadequate V_{GS} drive, and dissipation from short circuits (Eid & Rodriguez-Villegas, 2017; Kim et al., 2009; J. Y. Kim et al., 2014). However, it is important to note that the strategies employed to reduce reversion loss may lead to an increase in conduction loss. Therefore, careful consideration of design strategies is necessary to obtain the optimal balance point that enhances the overall efficiency and performance of the rectifier or charge pump circuit.

2.4 Conventional Rectifier and CP Topologies

Rectifiers and CPs share a similar circuit topology but with different input sources. The Dickson architecture, as depicted in Figure 2.4, represents the fundamental topology for both rectifiers and CPs (Dickson, 1976). A single stage of Dickson topology consists

of two diode-connected transistors M_{Dn}, M_{Dn+1}, and a coupling capacitor, C_n. For the rectifier, the Dickson topology takes a single RF voltage as input while CP has three DC inputs, which are V_{DD}, and two oscillating clocks, Φ_1 and Φ_2. Given the shared topology between the rectifier and CP circuits and the focus of this work on the backend RFEH circuit, this thesis will solely delve into the operation of the CP circuit from this point onwards.

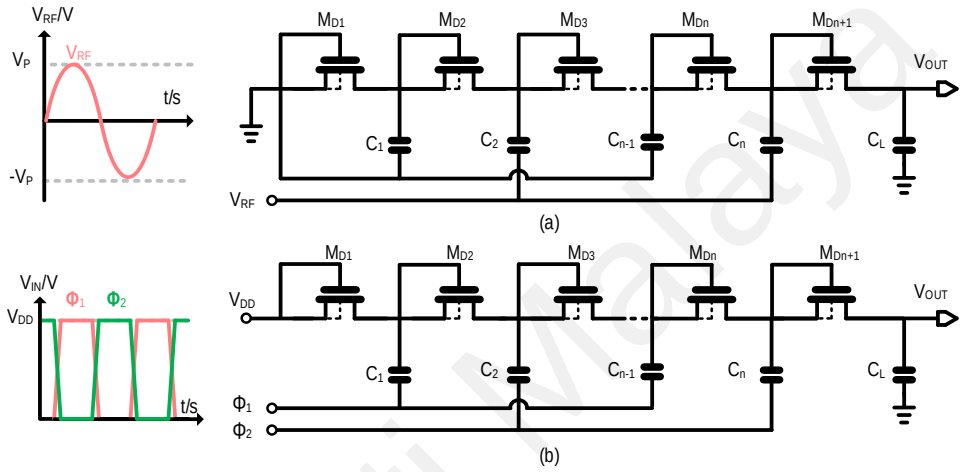

Figure 2.4: Conventional Dickson Topology of (a) Rectifier and (b) Charge Pump

During the second-half clock cycle, the first stage of the Dickson CP is operating in the reverse conduction phase with M_{D2} conducting in reverse-bias mode and M_{D3} conducting in forward-bias mode as depicted in Figure 2.5. During this phase, the low amplitude of the clock Φ_1 creates a potential difference with the DC input voltage, V_{DD}, causing the charge to pass through M_{D1} from the CP input. This results in the charging of C_1 to a voltage level equivalent to V_{DD}. At the same time, the reverse bias on M_{D2} prevents the charges from C_2 from backflowing into the preceding stage.

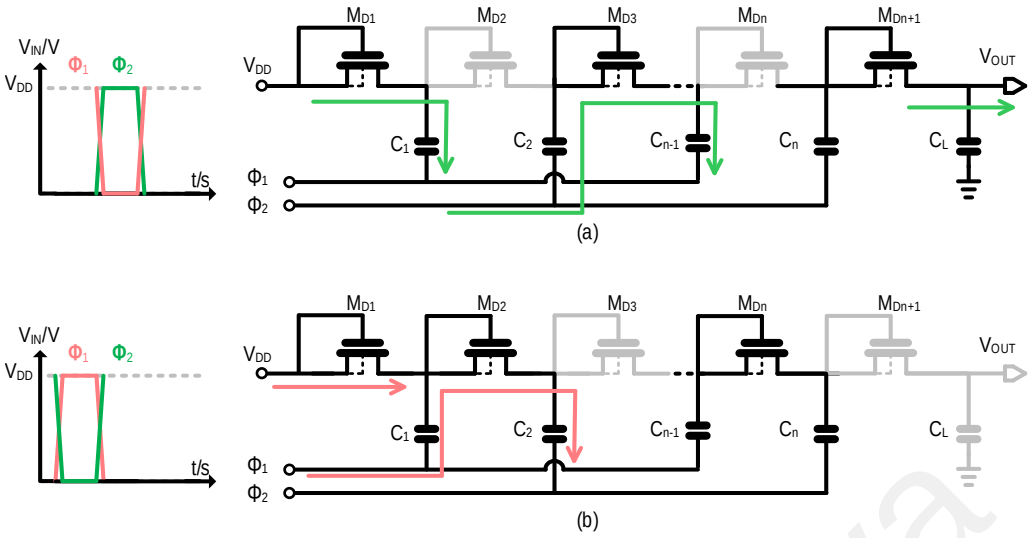

Figure 2.5: The Operation of Dickson CP at (a) The Second-Half Clock Cycle and (b) the First-Half Clock Cycle

During the first-half clock cycle, $\boldsymbol{\Phi_1}$ swings from low to high while $\boldsymbol{\Phi_2}$ swings from high to low. This causes transistor M_{D2} to conduct in forward bias and M_{D3} conducts in reverse bias condition. The high voltage amplitude from $\boldsymbol{\Phi_1}$ pushes the charges from C_1 through the M_{D3} to charge the C_2 to a voltage level of $\boldsymbol{V_{\Phi 1} + V_{C1}}$, which corresponds to $\boldsymbol{2\,V_{DD}}$. The process of altering charging and discharging the coupling capacitor over the two-half clock cycle enables voltage boosting in the CP circuit. The output voltage of a Dickson CP is formulated as in equation (2.12) (Ho et al., 2022):

$$\mathbf{V_{OUT} = V_{DD} - V_{th} + N\left(\frac{C}{C + C_{par}} \times V_{\Phi} - V_{TH} - V_{loss}\right)} \tag{2.12}$$

where V_{TH} is the threshold voltage of the diode-connected transistor, N is the number of CP stages, C is the pumping capacitance, C_{par} is the parasitic capacitance at the bottom plate of the pumping capacitor, V_{Φ} is the clock amplitude and V_{loss} is the voltage loss. The equation (2.12) reveals a significant V_{TH} drop in the Dickson CP due to the diode-connected transistor. Given the typically low voltage scavenged from RFEH, this

substantial V_{TH} drop renders the Dickson topology unsuitable for RFEH applications. Consequently, a switch-based CP topology was introduced as an alternative solution.

Figure 2.6 illustrates the rectifier and CP cross-coupling architecture which utilized switch-connected transistors to eliminate reverse current loss (Ballo et al., 2021). The cross-coupling architecture comprises two complementary charge-transferring paths, Path A and Path B, which enable voltage transfer to the output during both half cycles. Each path consists of a pair of cross-connecting NMOS-PMOS transistor pair and a coupling capacitor.

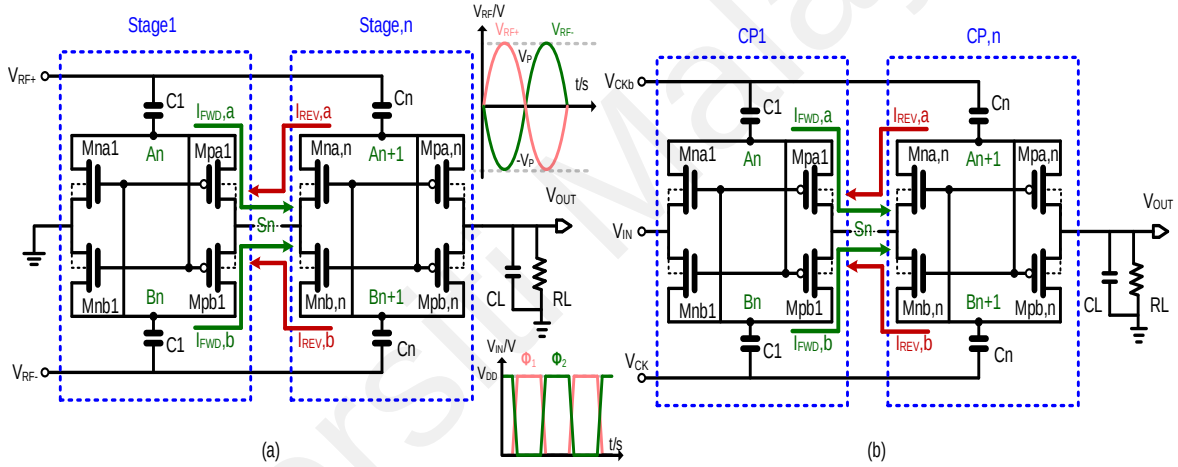

Figure 2.6: Conventional Cross-Coupled Topology of (a) Rectifier and (b) Charge Pump

Figure 2.7 illustrates the operation of cross-coupled CP topology. When Φ_1 transitions from high to low and Φ_2 transitions from low to high during the second half clock cycle, Path A of the Cross-coupled Charge Pump (CCCP) operates in reverse conduction mode while Path B operates in forward conduction mode. As a result, transistor M_{na1} in Path A turns ON while transistor M_{pa1} turns OFF. The charges from the input voltage, V_{IN}, flow through M_{na1} to charge the capacitor C_1 to the voltage level of V_{DD}. Conversely, $\Phi_1$transitions from low to high while Φ_2 transitions from high to low during the first-half

clock cycle. As a result, Path A of the CCCP enters the forward conduction mode, while Path B enters the reverse conduction mode. The high voltage amplitude from the clock Φ_1 drives the transfer of charges from capacitor C_1 to the subsequent CP stage, resulting in the charging of the pumping capacitor in the next stage to a voltage level of 2 V_{DD}. The operation of Path B is identical to that of Path A, except it occurs in the alternate clock cycle.

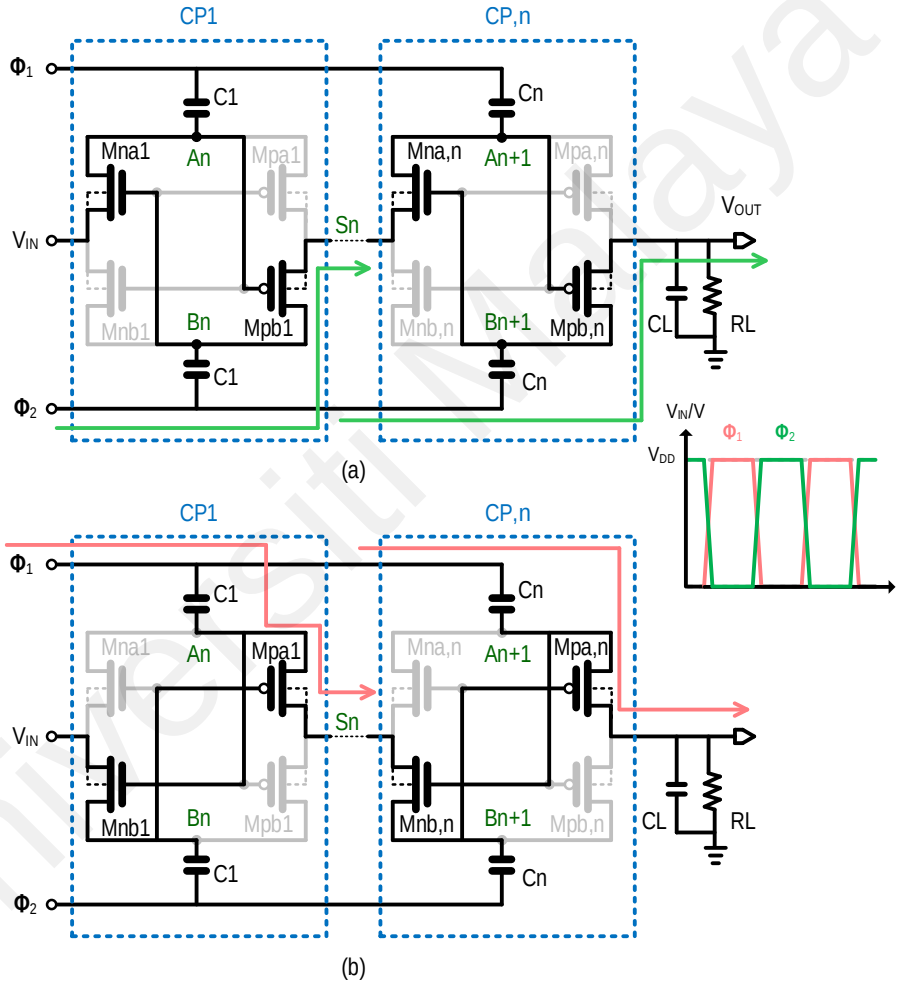

Figure 2.7: The Operation of Cross-coupled CP at (a) The Second-Half Clock Cycle and (b) The First-Half Clock Cycle

The CCCP overcomes the drawback of high V_{TH} loss associated with diode-connected transistors in the Dickson topology. Moreover, the dual branch connection in the CCCP

allows charge delivery to the output during both the charging and discharging phases. This can effectively suppress the output voltage ripples (Jiang et al., 2018).

While the CCCP architecture offers several advantages, it also exhibits setbacks, especially when it comes to reversion loss. Consequently, considerable research efforts which will be discussed in the following section have been devoted to overcoming this issue by devising enhancement methods specifically tailored for low-input voltage CCCP circuits.

2.5 Rectifier and CP Topologies Improvement Method

2.5.1 Gate Biasing Technique

a) V_{TH} Compensation

The gate bias technique refers to the practice of applying a specific voltage bias to the gate terminal of a transistor to change its R_{ON} for nullifying the V_{TH} drop across a transistor. The most common gate biasing technique is V_{TH} compensation for Dickson topology where a voltage level of V_{TH} is applied to the V_{GS} of a transistor to compensate for the voltage drop across the diode-connected transistor.

Le et al. (2008) proposes a floating gate threshold voltage compensation technique. This technique utilized the behavior of charge trapping in a floating gate PMOS transistor which acts as a capacitor. The floating gate PMOS is connected between the drain and the gate terminal of the diode-connected transistor to passively reduce the effective threshold voltage of the transistor as shown in Figure 2.8. This method however requires accurate pre-charging to avoid excessive extra potential, which can lead to negative turn-on voltages. Moreover, the pre-charging process requires an external battery which is not suitable for autonomous solutions. Chouhan and Halonen (2015) put forth a V_{TH} compensation scheme that eliminates the need for external manual pre-charging. This

scheme accomplishes V_{TH} compensation by utilizing capacitors as pumping storage to nullify the impact of V_{TH}. The C_{bat} is charging during the positive cycle and discharging during the negative cycle, thereby providing the necessary bias voltage for transistor P1.

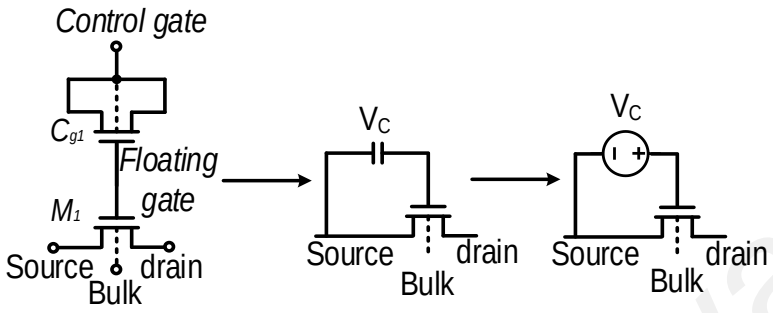

Figure 2.8: Floating Gate Threshold Voltage Compensation Technique (Le et al., 2008)

The work on Palumbo and Pappalardo (2010) and Umezawa et al. (1992) improves the Dickson topology with a bootstrap CP using an additional transistor and capacitor to bias the gate terminal of the charge-transferring transistor as illustrated in Figure 2.9. The capacitor provides the biasing voltage for V_{TH} compensation while the additional transistor acts as the gate control switch for voltage biasing.

Alternative V_{TH} compensation techniques employ external circuitry to generate and supply the required biasing voltage for precise compensation of V_{TH} variations. Umeda et al. (2006) proposed an external V_{TH} cancellation circuit to compensate V_{TH} drop. The V_{TH} cancellation unit is compromises of three parts, a V_{bth} generator, a V_{bth} distributor, and the capacitors for voltage biasing as shown in Figure 2.10. The V_{bth} generator utilizes the V_{TH} of an NMOS transistor as a reference to generate a voltage level that matches the threshold voltage of the rectifying transistor, V_{bth} for precise compensation. Subsequently, the V_{bth} distributor, comprising two pairs of pass transistors, receives the V_{bth} voltage and transfers it to the capacitor, enabling the biasing of the rectifying transistor to achieve the V_{TH} compensation.

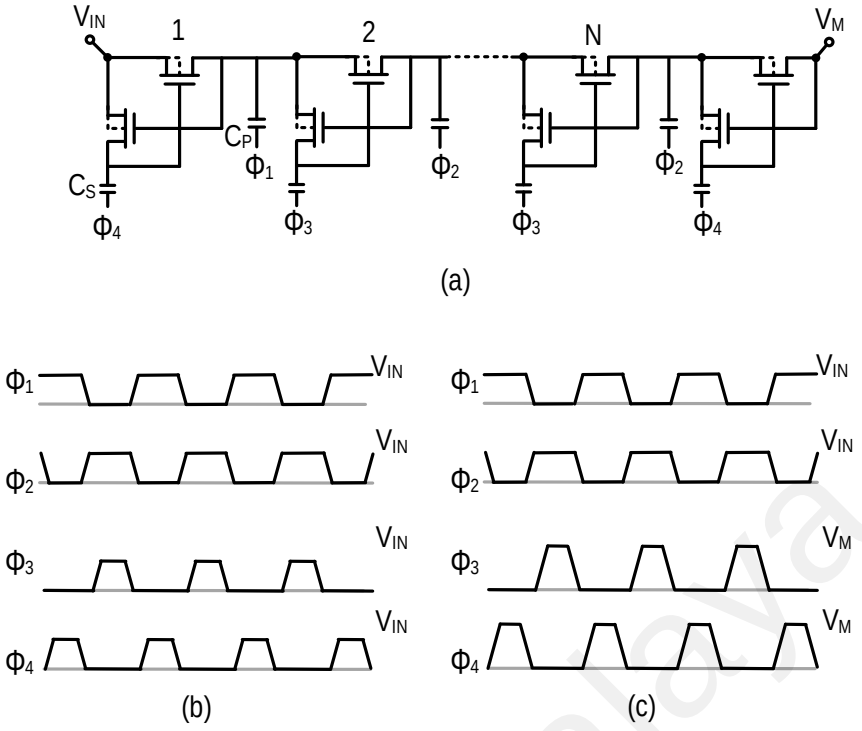

Figure 2.9: A Bootstrap CP's (a) Schematic Diagram (b) Conventional Clock Scheme (c) Gate-Boosted Clock Scheme (Fuketa et al., 2017)

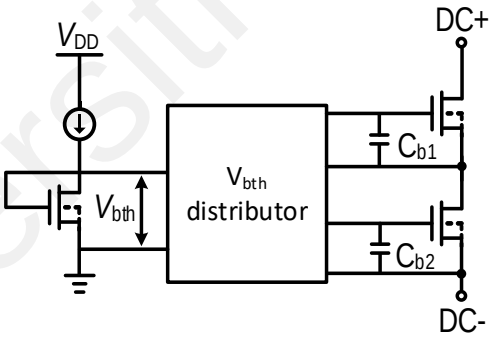

Figure 2.10: A Schematic Diagram of the V_{TH} Cancellation Unit (Umeda et al., 2006)

In the work of Nakamoto et al. (2007), an internal V_{TH} cancellation circuit was introduced for the mirror-stacked rectifier, aiming to accurately track and compensate for process and temperature variations in the rectifying diodes. This circuit ensures precise V_{TH} compensation in the rectifier by addressing the impact of variations caused by changes in process parameters and temperature conditions.

b) Self-Bias

The self-compensation concept presents a straightforward and highly effective embodiment of V_{TH} compensation. It involves the direct connection of a transistor's gate to the source of subsequent transistors within a multistage architecture. The voltage level of the rectifier and CP circuit increases in each subsequent stage. By connecting the gate terminal of NMOS in the next cascaded stage, a higher node voltage will be tapped into the V_{GS} of the transistor, achieving forward V_{TH} compensation.

Hameed and Moez (2013) proposes a forward-compensation self-biasing technique for the NMOS transistor where the gate terminal is connected to the next cascaded stage and a back-compensation self-biasing technique where the gate of the PMOS transistor is connected to the preceding stage. The schematic of the self-bias circuit is shown in Figure 2.11. Hameed and Moez (2014) further presented a level 3 forward and backward compensation technique whereby the gate of transistors are connected three stages away to further improve the current conductivity.

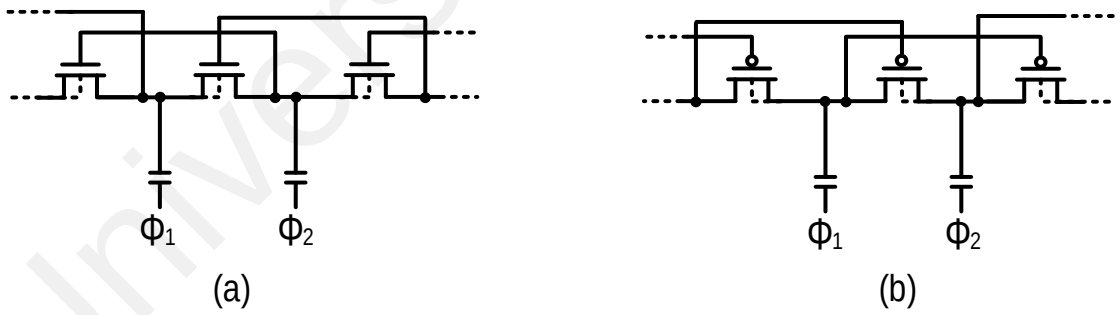

Figure 2.11: Self-Bias Technique with (a) Forward-Compensation using NMOS (b) Back-Compensation using PMOS (Hameed & Moez, 2013)

Papotto et al. (2011) presented an RFEH featuring a fully passive threshold self-compensation scheme with multiple "orders." The rectifier was designed with 17 stages and incorporated an additional cascade "dummy" chain. This chain generates a high DC

voltage to facilitate compensation voltage at multiple levels, enabling effective V_{TH} compensation in the circuit.

As discussed in section 2.3.5, there exists a trade-off between reversion loss and conduction loss. Therefore, in certain scenarios such as driving a large load current or handling a high input power, it may be necessary to increase the threshold voltage in order to enhance efficiency. In this context, L. Xia et al. (2014) introduce a harvesting tracking loop tunable V_{GS} technique, which involves the utilization of two time-interleaved sample-and-hold circuits, a comparator, and a digital decision block. This combination allows for dynamic tuning of the V_{TH} compensation. By employing this approach, the V_{GS} can be actively adjusted to optimize the compensation process in accordance with varying operational conditions, thereby further improving the overall efficiency of the system.

2.5.2 Gate Boosting Technique

Gate boosting technique is a method used to enhance the performance and efficiency of transistors by increasing the V_{GS} of the transistor. As discussed in equation (2.9), the R_{ON} of a transistor depends on the V_{GS}. By applying an additional voltage to the gate terminal of a transistor, the V_{GS} can be increased, resulting in a lower R_{ON} and improved conductivity of the transistor.

Wang et al. (2014) introduced an RFEH rectifier featuring a gate-boosting scheme that amplifies the input RF voltage at the gate of the transistors. The circuit employs an in-phase passive voltage multiplier to increase the V_{GS} swing in phase with the driving drain-to-source voltage (V_{DS}) swing. This approach offers several advantages, including a reduction in the effective V_{TH}, forward resistance, and reverse leakage current of the rectifier. Consequently, the efficiency and sensitivity of the rectifier are enhanced, leading to improved performance and energy harvesting capabilities.

In a similar vein, Fuketa et al. (2017) enhanced the conventional bootstrap CP circuit by incorporating the gate-boosting technique, as depicted in Figure 2.9 (c). The schematic of the CP topology remains unchanged from the conventional bootstrap CP, but the switch signals Φ_3 and Φ_4 are boosted to a higher amplitude equivalent to the output voltage.

Level shifter is an auxiliary circuit commonly used in CP to facilitate the implementation of gate boosting technique. Favrat et al. (1998) implemented a level shifter in his voltage doubler circuit to drive the gate of the load switches. The level shifter, as shown in Figure 2.12 (a), provides a higher driving gate voltage that ranges from 0 to $2\,V_{DD}$, in contrast to the conventional driving gate voltage of 0 to V_{DD}. This increased voltage range helps reduce the R_{ON} of the dual series load switches, enhancing their performance in the circuit. Kim et al. (2013) introduced further enhancements to the voltage doubler circuit by incorporating a negative CP in addition to the level shifter. The inclusion of the negative CP facilitates the generation of a negative voltage, thereby allowing the gate voltage to oscillate between $-V_{DD}$ and $2\,V_{DD}$. This negative voltage plays a crucial role in ensuring the proper turn-off of the NMOS load switch during the reverse conduction phase, effectively mitigating power loss resulting from current leakage.

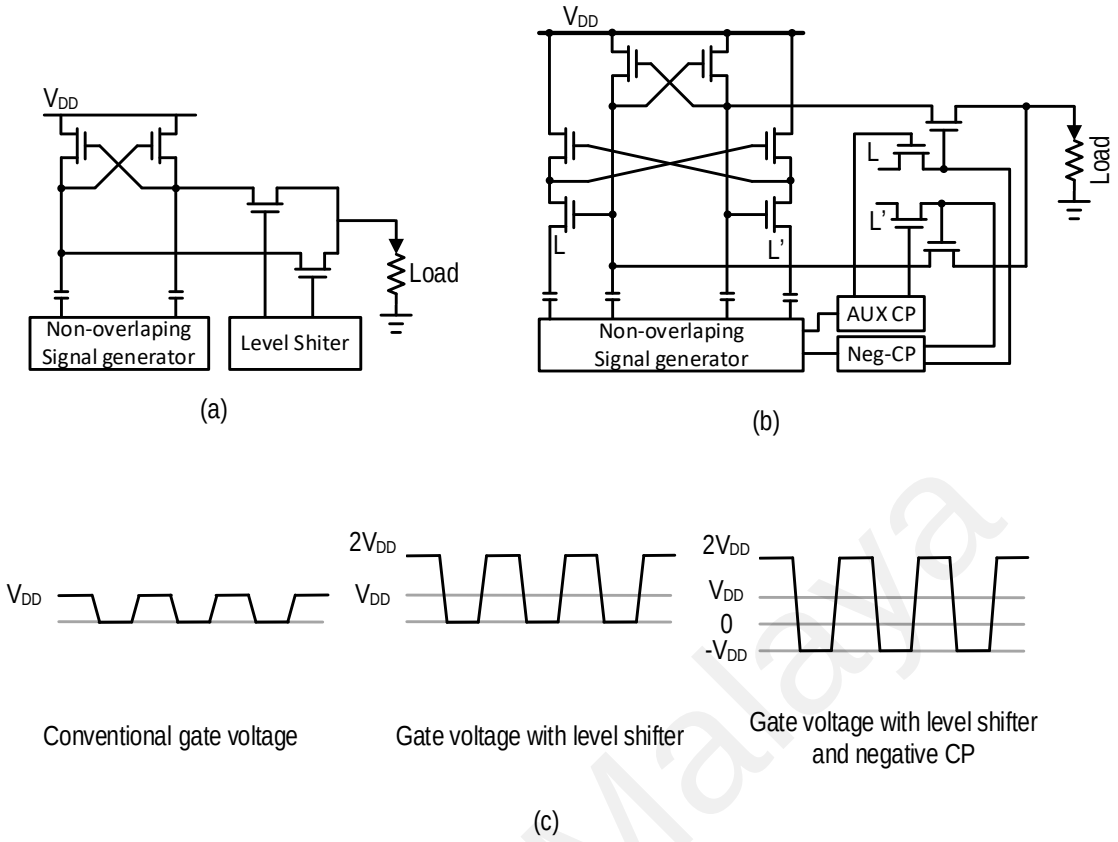

Figure 2.12: Schematic of a Voltage Doubler with (a) Level Shifter (b) Level Shifter and a Negative CP and (c) Different Gate Voltage Signals for the Charge Transferring Transistor

The previously highlighted level shifter serves the purpose of providing gate driving voltage for NMOS load switches in the voltage doubler circuit. However, CCCP topology compromises a set of NMOS and PMOS cross-coupling pairs, the same level shifter cannot be utilized for both switches. Tsuji et al. (2017) presented a low-leakage driver that incorporates two separate level shifters: one for the NMOS switch and another for the PMOS switch as depicted in Figure 2.13. This approach ensures that each switch receives the appropriate gate-boosted signal from its dedicated level shifter, catering to the specific requirements of the CCCP topology. The most recent gate-boosting technique incorporating a level shifter and negative CP was recorded in 2019 when Bose et al. (2019) integrated a gate booster for a 14-stage ultra-low voltage CP. The gate booster in the work

utilized positive and negative CP to provide the necessary boosting signals for the linear CP, achieving high PCE at ultra-low input voltage.

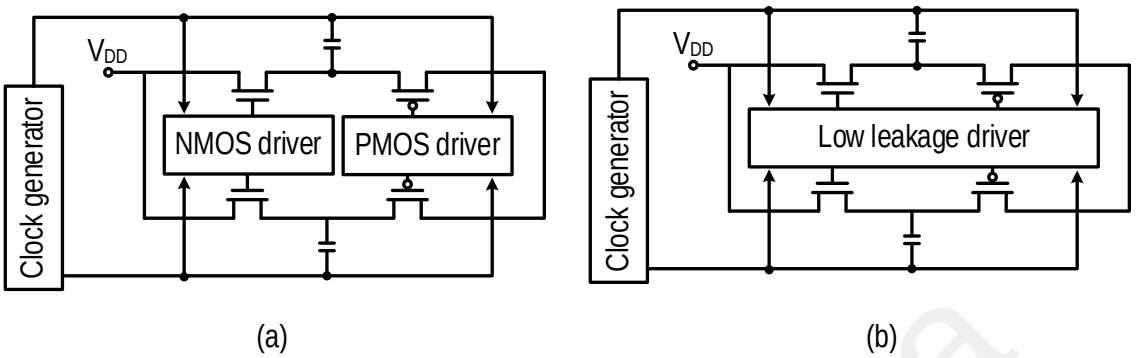

Figure 2.13: The Schematic of (a) Level-Shifter for the NMOS and PMOS in CCCP and (b) its Equivalent Block Diagram

The gate-boosting technique plays a crucial role, particularly in subthreshold operation, where the input voltage is insufficient to enable a complete turn ON/OFF of the transistor, leading to significant conduction and reversion losses. While the gate-boosting technique has the potential to significantly reduce forward conduction and reverse current losses, it has the limitation of requiring a significant amount of external circuitry for the implementation of the technique. Specifically, each CP requires an individual level shifter or negative CP. This demand for additional circuitry can become substantial, considering the number of CPs involved in energy harvesting systems.

2.5.3Dynamic Gate Biasing Technique

The DGB technique was initially proposed by Chi-Chang and Jiin-Chuan (1997). This technique aims to dynamically adjust the gate voltage of the charge transfer switch (CTS) in order to minimize the forward conduction loss during the forward conduction phase and the reverse current loss during the reverse conduction phase. Unlike the previously mentioned approach that solely focuses on reducing conduction loss through an increase in the V_{GS} of the transistor, DGB provides a comprehensive solution to not only minimize

conduction loss but also mitigate the trade-off of increased reversion loss. This makes DGB particularly noteworthy as it offers a more balanced and effective approach to optimizing the performance of the system.

During the forward conduction phase, the application of a higher V_{GS} effectively decreases the R_{ON} of the NMOS transistor. On the other hand, the application of lower V_{GS} in the reverse conduction phase will increase the R_{ON} of NMOS to stop the reverse current leakage. This is achieved by utilizing an NMOS-PMOS inverter pair that acts as a gate control switch to pull a higher node voltage from the subsequent CP stage and a lower node voltage from the preceding CP stage as shown in Figure 2.14. The approach of employing an NMOS-PMOS inverter pair to implement DGB is widely adopted in CP circuit design, evidently adopted in various design solutions (Feng et al., 2005; Mui et al., 2014; Ulaganathan et al., 2012).

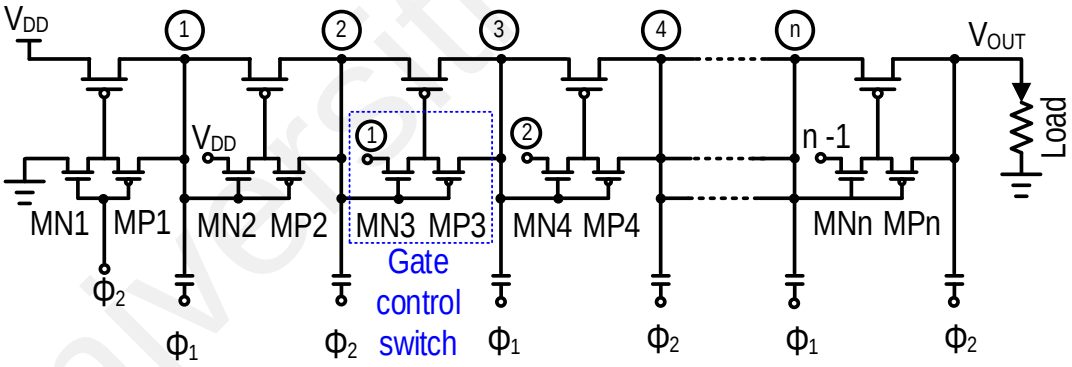

Figure 2.14: Conventional Dynamic Gate Biasing Technique on CTS CP (Chi-Chang & Jiin-Chuan, 1997)

In the DGB circuit, the gate terminal of the gate control switch is connected to the same node as the control signal, causing both gate control switches to turn ON simultaneously for a brief duration. This simultaneous activation leads to the occurrence of a reverse current through the gate control switch during the initial clock cycle. The issue is further exacerbated in the subsequent clock cycle when the gate control switch

experiences a delay in turning OFF, resulting in increased reverse current leakage. To resolve the aforementioned issue, a comprehensive investigation was conducted to evaluate the impact of different gate drive voltages on the gate control switch in the DGB technique, with the objective of determining the optimal combination that minimizes current leakage (Feng et al., 2006).

Jiang et al. (2018) introduce an advanced DGB wherein the gate terminal of the gate control switch is not interconnected. The different control signals enable the gate control switch to have independent switching states, preventing current backflow due to the simultaneous conduction. The approach demonstrates significant effectiveness in mitigating reversion loss during both clock cycles. Despite the implementation of non-simultaneous turning on of the gate control switch in the advanced DGB, the reversion loss still persists. A detailed analysis and proposed improvement method for the advanced DGB will be discussed in CHAPTER 3.

2.5.4 Bulk Biasing Technique

Bulk biasing, also known as body-biasing or substrate biasing is another exciting technique employed to enhance the performance of the rectifier and CP through the V_{TH} reduction. Similar to the gate-biasing technique, bulk biasing involves the application of voltage bias to alter the R_{ON} of a transistor to reduce its V_{TH}. However, the key distinction lies in the target terminal for biasing. While gate biasing focuses on the gate terminal, bulk biasing applies voltage bias to the bulk or substrate terminal of the transistor. As the expression of V_{TH} is given as in equation (2.13) (Gao et al., 2016):

$$\boldsymbol{V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\varphi_F - (V_{BIAS} - V_S)|} - \sqrt{|2\varphi_F|}\right)} \tag{2.13}$$

The V_{TH} can be reduced by increasing the bulk voltage, where V_{TH0} is the threshold voltage at zero bias, γ is the body effect coefficient, φ_F is the Fermi potential, V_{BIAS} is the bulk biased voltage and V_S is the source voltage.

Chen et al. (2015) and Po-Hung et al. (2010) implemented a forward body-biasing technique in their conventional CCCP circuit. To address the challenge of lacking a suitable control signal with the appropriate biasing voltage in the first and last CP stages, an additional stage was introduced to bias the last CP stage. In the case of the first CP stage, the work simply connects the bulk to the ground.

Jongshin et al. (2000) introduces a CP circuit with controllable body voltage, allowing the body terminal of the CTS to be connected either to its drain or source. This configuration enables dynamic control of the V_{TH} of the CTS. Similarly, Kim et al. (2015) propose a dynamic body biasing technique for the CCCP circuit. This technique effectively suppresses both conduction and reversion losses by decreasing the V_{TH} during the forward conduction phase and increasing it during the reverse conduction phase. The concept of dynamic body biasing is similar to DGB where an NMOS-PMOS inverter pair is used to drive higher and lower node voltage to the body terminal of CTS. To further enhance the performance of the CP circuit and reduce conduction and reversion losses, Zhang and Lee (2013) implemented a combination of dynamic gate and substrate biasing techniques on the CTS. This approach involved applying dynamic voltage signals to both the gate and substrate terminals of the CTS, allowing for simultaneous control of the threshold voltage and body effect.

2.5.5 Parallel Architecture

Parallel architecture is a design approach where multiple rectifiers or CP stages are cascoded in a sequential manner, allowing simultaneous operation of multiple stages.

This configuration is capable of reducing the equivalent resistance and improving the overall efficiency of the system.

Flores and Espinosa (2018) investigated and compared the power efficiency of various CP configurations for energy harvesting applications. It was found that increasing the number of cascading stages in a CP led to a higher voltage conversion ratio. However, this was accompanied by lower efficiency due to increased power losses caused by the higher effective resistance. On the other hand, connecting CP in parallel offers the advantage of higher efficiency due to the lower equivalent resistance, despite there being no increase in voltage boosting ratio with an increase in CP stages. Due to the aforementioned characteristics, multiple cascading CP stages are often connected in parallel to reduce the high effective resistance (Jiang et al., 2020; Vaisband et al., 2015). However, it is important to note that the parallel architecture comes with the cost of additional circuitry, which consumes more silicon area.

2.5.6 Clock Boosting Technique

Clock boosting is a technique specifically used in CP circuits to increase the amplitude of the clock signal. As the control signals (V_{GS}) for transistors in CP come from the clock signals, boosting the clock amplitude can achieve the same effect as the gate-boosting technique. In addition, the clock boosting technique will enhance the voltage-boosting capability of CP, leading to an increase in the voltage conversion ratio without the need for additional cascading CP stages. It's important to note that clock boosting applies only to CP circuits, as the process involves increasing the amplitude of the clock signal, which is not available in rectifier circuits.

To realize the clock boosting technique, a clock booster circuit is required to amplify the CP's clock amplitude as shown in Figure 2.15 (a). The clock booster circuit operates in a similar manner to a CP, utilizing charge storing and charge transferring methods. In

the first clock cycle where CK is low and CK_b is high, transistor N2 and N3 turn on while P1 turns off. The charge flows from V_{DD} through N2 to charge the capacitor C1. In the next clock cycle, N2 and N3 are off while P1 is one. This allows charges from CK to push the charges in C1 to flow into CK_b, yielding a clock amplitude of 2 V_{DD} to achieve the clock-boosting effect.

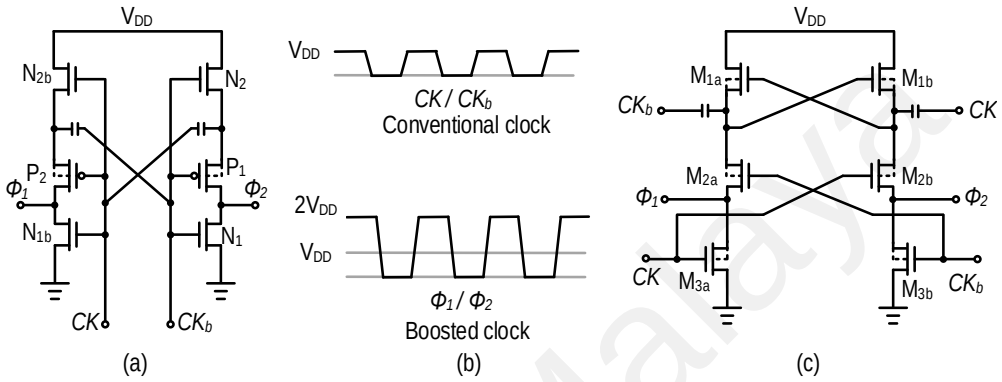

Figure 2.15: Clock Booster: (a) Conventional Circuit Schematic (b) Conventional and Boosted Clock Amplitude (c) All-NMOS Configuration

Clock boosting technique is widely popular in CP circuits due to its advantage in improved performance and voltage-boosting capability (Abdelaziz et al., 2011; Ballo et al., 2018; Chen et al., 2015). A. Ballo et al. (2020b) introduces an All-NMOS clock booster circuit by replacing the PMOS transistor with NMOS. This substitution was made based on the lower V_{TH} of NMOS transistors. While the clock booster circuit plays a crucial role in the overall performance of the CP circuit, the existing research did not specifically address its optimization or enhancement. This indicates a potential research direction for future studies to explore and improve the performance of the clock booster circuit, considering its significant impact on the overall performance of the CP circuit.

Ho et al. (2011) designed a novel ring oscillator with clock-boosting capability. This oscillator is composed of a series of odd-numbered cascaded bootstrapped delay cells, which are designed to generate a boosted oscillating clock signal with an amplitude

ranging from $-V_{DD}$ to $2\,V_{DD}$. The bootstrapped CMOS delay cell consists of two inverters, two capacitors, and several transistors. The top part of the circuit represents the clock booster, responsible for generating the 2-fold positive amplitude of the clock signal. On the other hand, the bottom part of the circuit functions as the negative CP, generating the negative clock amplitude.

Some recent works (Jiang et al., 2019; Yi et al., 2018a) made advancements in the design of bootstrapped delay cells and introduced a bootstrapped ring-voltage controlled oscillator (BTRO). The BTRO is specifically designed to generate multi-phase clock signals with a boosted swing amplitude ranging from $-\,V_{DD}$ to $2\,V_{DD}$ which can be directly used by the CP operation. The BTRO has a limitation in the frequency range as the number of delay cells depends on the number of CP stages.

2.5.7 Adiabatic Clock Scheme

The adiabatic clock scheme is a special clock scheme that aims to reduce power loss during charge transfer operations. During charge transfer in CP pumping operation, the current flows over the R_{ON} of CTS and generates Joule heat, E_J was given as in equation (2.14) (Wang et al., 2017):

$$\boldsymbol{E_J = C\Delta V^2} \tag{2.14}$$

where ΔV^2 represents the voltage increment of a single-stage CP in the charge transfer operation. From the equation, it is evident that the voltage increment contributes of majority Joule heat loss during charge transfer. To resolve the issue, Wang et al. (2017) proposes a split merge CP where the one big voltage increase in ΔV^2 is divided into several smaller voltage increment across multiple smaller flying capacitors. These smaller voltage increments are then merged at the end of the CP circuit to complete the voltage-boosting operation.

Lauterbach et al. (2000) proposed a charge-sharing method to mitigate the Joule heat loss associated with charge transfer. This method involves a specific clocking scheme and two pumping capacitors. The forward conduction phase of the charge transfer operation is divided into three parts, using the adiabatic clock scheme where the first part involves charging the first capacitor to $\frac{1}{2}\ V_{DD}$. In the second part, the two pumping capacitors will be connected in parallel to facilitate charge sharing. Lastly, the second capacitor will be charged for another $\frac{1}{2}\ V_{DD}$ to complete the full pumping operation. By dividing the full V_{DD} charge transfer into two parts and incorporating charge sharing, this method effectively reduces the Joule heat loss associated with the large voltage increment. A similar adiabatic clocking scheme was adopted by Ulaganathan et al. (2012) for his ultra-low voltage CP.

2.6 Comparative Recent Research Evaluation of Low Input Voltage Charge Pumps

Table 2.2 provides a summary of the performance characteristics of state-of-the-art CPs designed for low input voltage subthreshold operation. To address the trade-offs associated with CP design, recent research studies have focused on performance enhancements, as discussed earlier. These enhancements primarily involve techniques such as threshold voltage compensation, gate and body biasing, and clock boosting, aiming to reduce forward conduction and leakage current. It is generally observed that CPs experience significant conduction and reversion losses at low input voltages. However, as the input voltage increases, the performance of the CPs improves accordingly.

2.7 Effect of Fluctuating Input Power on RFEH System

In energy harvesting applications, the input voltage of the CP varies due to the fluctuation in the harvested power, which is an external influence on the system. For instance, the changes in the strength of the RF signal and the distance between the transmitter source and the receiving antenna of the RFEH system will significantly impact the harvesting input power. There are several problems accommodated with a wide input power range in the RFEH system.

Firstly, the PCE of a CP cannot remain high over a wide input voltage range, as the CPs are typically optimized for a specific input voltage range. Additionally, different CP topologies have defined input voltage operation ranges tailored to their characteristics. Secondly, the frequency generated by the oscillator is influenced by the input voltage. Higher input voltage levels can lead to an increase in the oscillator's oscillation frequency, resulting in elevated switching losses within the CP, ultimately affecting its performance. Moreover, the wide input power range can potentially lead to the RFEH system producing higher output voltages, which may pose a risk of damaging the connected output load.

To address these challenges, various approaches have been proposed in existing works. These include the development of frequency modulation techniques, reconfigurable CP topologies, and output voltage monitoring schemes aimed at mitigating the aforementioned issues.

Table 2.2: Performance Overview of Recent Subthreshold Operation Charge Pumps.

Author	Tech. (nm)	Key Technique	Input Voltage (V)	No. of Stages	Pumping capacitance (pF)	VCE (%)	Frequency (MHz)	PCE (%)	Area (mm^2)
(Fuketa et al., 2017)	65	Bootstrap CP + Gate boosting	0.1	10	1001	76@ $0.1V_{IN}$	1	33	1.32
(Tsuji et al., 2017)	65	CCCP: low leakage driver	0.1	3	300	90.5@$0.1V_{IN}$	-	12.7	-
(Chen et al., 2012)	65	Dual mode: CTS + Dickson	0.12	10	-	58	1	38.8	0.78
(Ulaganathan et al., 2012)	130	Adiabatic clock + DGB	0.125	3 / 7	130	80@3stages, 70@7stages	0.125	65@3stages / 59@7stages	0.1 / 0.5
(Jung et al., 2014)	180	Self-oscillating reconfigurable CP	0.14	4	654	-	70 ~ 19	50@ 0.45 V_{IN}	0.86
(Yi et al., 2018a)	28	BTRO (3x clock boost)	0.15	3	22.5	80@$0.15V_{IN}$	15.2	38.8	0.032
(Jongshin et al., 2000)	130	DBB	0.15	3	[b]60,000	86@$0.18V_{IN}$	0.25	34	0.066 w/o cap
(Kim et al., 2015)	130	dynamic body biasing + dead time control	0.15	3	0.006	86	0.25	34@$0.18V_{IN}$	0.006

Table 2.2, continued

(Po-Hung et al., 2010)	65	FBB	0.18	3	6*12.3 + 2*0.4	69@0.18V_{IN}	10	-	0.296
(Abdelaziz et al., 2011)	[a]250	CLK boost + DGB	0.3	6	-	-	1MHz	66	-
(Abdelaziz et al., 2012)	[a]250	CLK boost + DGB	0.3	3 / 6	-	-	1MHz	68.15@3stage 66.36@6stage	-
(Peng et al., 2014)	180	DGB	0.32	6	288	89@320mV	0.45	-	0.14
(Ozaki et al., 2016)	180	MVG / HVG	0.35	2	1920 / 1440	79.7@0.59V 60.5@2.5V	-	49.1@MVG 75.8@HVG	1.75
(A. Ballo et al., 2020a)	[a]65	CC-CP	0.4	4	10*8	99.2	4	87.7	0.021
(Liu et al., 2016)	180	Reconfigurable	0.455	4	4*62.7	89@0.45V_{IN}	0.286~1	-	4
(Wang et al., 2017)	130	Split merge CP	0.5	5	-	93	0.8~2.5	78.6	0.98
(Mahmoud et al., 2018)	65	Dickson CP + DGB	0.55	4	4*40	98@0.7V_{IN}	0.5~1.8	66	0.17

Table 2.2, continued

(A. Ballo et al., 2020b)	[a]28	CCCP + CLK Boost	0.05 / 0.1	2	15	80	1	38.9@0.1V_{IN}	0.0116
(Shih & Otis, 2011)	130	Bootstrap CP (no regulation) / With output regulation	0.27 / 0.4	3	150	65@0.45V_{IN}	0.8 (nominal) / 0.6~1 (tunable)	58	0.42

[a]Simulated work; [b]Off-chip components

2.7.1 Conventional Reconfigurable CP

The primary objective of a reconfigurable CP is to enhance efficiency and control the Voltage Conversion Ratio (VCR) to limit the output voltage. In a study by Gupta et al. (2013), a power-efficient reconfigurable CP was introduced, switching between linear CP and Fibonacci CP in high and low voltage ranges, respectively. However, this work primarily focuses on maximizing efficiency, without addressing the need to limit the output voltage to prevent transistor overstress and load breakdown.

In another work by Palumbo et al. (2006), an adaptive VCR reconfigurable CP was implemented, capable of switching between 1, 2, and 3 stages to achieve maximum efficiency. However, its diode-based design restricts its applicability in low-voltage energy harvesting scenarios. A reconfigurable soft transition VCR CP was proposed in Jiang et al. (2022), but it is designed for step-down CP.

Tsai et al. (2014) introduced a hybrid Dickson and Cockcroft-Walton CP, configurable between 4 and 6 stages. However, this work was only tested within a narrow input voltage range of 0.9, 1, and 1.1 V. Similarly, Zhang and Lee (2010) proposed a reconfigurable CP with VCR options of 2 and 3, while Luo et al. (2019) proposed a stage selection CP that can configure between 1 to 3 stages. However, these CPs were primarily evaluated at high input voltage ranges. In addition to adaptive VCR for limiting output voltage, Luo et al. (2019) also considered transistor electrical overstress and gate-oxide unreliability in the design for the 1.8 V/3.3 V CMOS process.

Ballo et al. (2022a) presented a unique output voltage regulation method using the transconductive loop implemented through the bulk terminal of the PMOS transistor in a CCCP. However, this work did not account for the impact of variable frequency within a wide input voltage range, as it maintained a constant 1MHz clocking frequency throughout the input voltage range.

An alternative approach to altering the VCR is by controlling the clock amplitude of the CP. Ballo et al. (2021) implemented a clock amplitude reducer to halve the VCR in conjunction with a reconfigurable CCCP capable of switching between 2 and 4 stages. Jung et al. (2014) introduced a novel self-oscillating CP that supplied different levels of source voltage to achieve an adaptive VCR. While the self-oscillating CP eliminates the need for an external oscillator, its frequency cannot be independently adjusted, necessitating an external frequency modulation block.

2.7.2 Frequency Modulation

Frequency modulation plays a crucial role in wide-input reconfigurable CPs because high oscillating frequencies can lead to increased switching losses, ultimately degrading CP performance. Surprisingly, this aspect has been frequently overlooked in previous reconfigurable CP research. For example, some recent works (Ballo et al., 2022a; Andrea Ballo et al., 2020) directly supply two non-overlapping clocks with constant frequency for the CP with a wide input voltage range. However, this approach is not suitable for accurately assessing the CP performance.

An oscillator plays a crucial role in generating the oscillating clock signal necessary for CP operation and is a critical component in frequency modulation. The generated oscillation frequency is determined by the quantity of inverter cells and the associated delay time, as indicated in equation (2.15) (Ho et al., 2022; Kishore K. Pakkirisami Churchill et al., 2022):

$$\boldsymbol{f_{osc} = \frac{1}{2 \cdot N \cdot t_d}} \tag{2.15}$$

where N represents the number of delay cell stages and t_d represents the delay time for each stage. The delay time is influenced by the oscillator's input voltage (V_{OSC}) and transistor size (Kishore Kumar Pakkirisami Churchill et al., 2022). Given that the

oscillator's input voltage varies with the circuit's input voltage (V_{DD}), the output clock frequency range of the RVCO is consequently affected by V_{DD} variations. This effect becomes particularly significant in energy harvesting applications where a wide input voltage range is typical. Furthermore, high frequencies contribute to elevated switching losses in the charge pump. Given that switching loss is inversely proportional to conduction loss (Churchill et al., 2020), achieving an optimal frequency is essential to strike a balance between switching loss and conduction loss for efficient charge pump performance.

The oscillation frequency can be reduced by either increasing the number of delay cell stages or lowering the oscillator's input voltage (V_{OSC}). However, expanding the number of delay cell stages is not a viable method for frequency regulation because it increases the oscillator's power consumption, which is evident from equation (2.16) (Kishore K. Pakkirisami Churchill et al., 2022):

$$\boldsymbol{P_C = N \cdot f_{osc} \cdot C_L \cdot V_{osc}^2} \tag{2.16}$$

While lowering V_{OSC} might initially seem like a favorable approach to simultaneously reduce oscillation frequency and power consumption, it's important to note that decreasing V_{OSC} will also result in a reduced amplitude swing of the oscillating signal. This, in turn, diminishes the conduction capabilities of the CP. Typically, the amplitude of the CP's clock signals aligns with the amplitude of the oscillating signal. A diminished amplitude significantly compromises CP performance and its VCR. This occurs due to the resultant increase in the R_{ON} of the charge transfer transistors.

Several approaches have been explored in previous studies to achieve frequency modulation in wide-input CPs. For instance, a subtraction-mode CP was proposed with the capability of handling high switching frequencies in the range of 60 MHz to 100 MHz

(Jiang et al., 2020). However, this frequency range is too limited for wide-input energy harvesting applications. In another study by Carreon-Bautista et al. (2016), frequency modulation was implemented in a 9-stage CP, where each stage could be deactivated using a stage control block. The modulation was achieved through a variable delay cell configuration, but this approach introduced high power consumption. Fanori and Andreani (2013) introduced a high efficient class – C CMOS voltage controlled oscillator (VCO) with fine-tuning capabilities. However, the narrow frequency range of 3.4 GHz to 4.5 GHz is not sufficient to cover the range of CP operation for RFEH system.

2.7.3 Output Voltage Monitoring

Ensuring appropriate power delivery to the load is crucial to meet the specific voltage requirements of IoT systems. These devices typically include low-power microcontrollers, sensors, and wireless communication modules, which can become damaged if supplied with excessively high voltage levels (Wang & Kose, 2018). To address this concern, some studies have proposed limiting the output voltage to ensure the long-term reliability of the circuit (Moghaddam et al., 2022; Moghaddam et al., 2017; Yi et al., 2018b). The use of a voltage monitor (Colella et al., 2016) is one approach to maintain the output voltage within an acceptable range, providing a stable and reliable power source for IoT devices while safeguarding sensitive components against potential damage. This can be achieved by adjusting the equivalent output load resistance or disconnecting the load when the output voltage exceeds a predefined threshold (Colella et al., 2016). Typically, a voltage regulator or limiter is employed for this purpose. Despite the importance of maintaining a bounded output voltage, only a limited number of RFEH studies have addressed this concern (Abouzied et al., 2017; Scorcioni et al., 2012; Scorcioni et al., 2013), emphasizing the need for further research in this area.

In the past, power-intensive circuit components like voltage and current sensors (Vaisband et al., 2015) or a bandgap reference and comparator (Shih & Otis, 2011) were utilized for output voltage regulation, resulting in increased power consumption and making them unsuitable for micro-scale energy harvesting systems (Rawy et al., 2016). Furthermore, these circuit elements required a stable voltage reference to function properly. Existing voltage reference generation circuits typically consumed significant power and relied on bulky resistive components, rendering them unsuitable for on-chip applications. Some previous works attempted to supply a constant reference voltage externally to the voltage regulation unit (Jung et al., 2014; Liu et al., 2016; Lingli Xia et al., 2014). However, evaluating energy harvesters with the use of external sources is not a fair assessment of their performance.

2.8 Summary

In this chapter, a comprehensive literature review that encapsulates the RF power availability for energy harvesting, the overview of the RFEH circuit, and the recently published rectifier and CP improvement techniques are presented. Based on the findings, the literature review conducted on subthreshold operation CPs reveals a predominant focus on addressing the issues of forward conduction and reversion loss. These two aspects have been identified as the major drawback to the CPs' efficiency in subthreshold operation. It is imperative to acknowledge that exclusively targeting the reduction of a single loss while disregarding the other proves impracticable due to an inherent trade-off between conduction and reversion loss. In this context, clock boosting, and DGB techniques emerge as favourable options, as they can simultaneously address both losses. While the clock-boosting technique is applicable specifically to CP circuits and requires additional clock-boosting circuitry, DGB has proven to be a superior choice for subthreshold operation RFEH circuits.

Subsequently, the chapter delves into the impact of a wide input power range on the RFEH system, which encompasses inconsistent PCE across the wide input range, high oscillating frequencies leading to increased switching losses, and potential overshooting of the output voltage, which could pose a risk of damaging the WSN load. In response to these challenges, existing works have proposed reconfigurable topologies to adapt to the broad changes in input voltage and have introduced voltage monitoring units to limit the output voltage within a specified range. However, there is still a notable research gap in designing a high-efficiency reconfigurable CP topology and a low-power voltage monitoring unit tailored specifically for WSN RFEH applications.

CHAPTER 3 : ADVANCED DYNAMIC GATE BIASING

3.1 Chapter Overview

In this chapter, a CP topology utilizing advanced DGB with a dual switch configuration is introduced to enhance the CP's PCE in subthreshold operation. The chapter commences by providing an overview of related work and addressing the existing challenges in dynamic gate biasing. Subsequently, the operating principle of the proposed charge pump is presented, highlighting its distinctive features and advantages. Next, a capacitive optimization technique is presented for effective silicon area utilization. The design is validated through experimental results, demonstrating the effectiveness of the proposed approach. Furthermore, the research findings are thoroughly discussed and analyzed, with a comparative evaluation of the performance against prior works in the field. Finally, a summary wraps up the chapter, summarizing the key insights and contributions of the proposed CP topology.

3.2 Proposed Subthreshold Operation Charge Pump

3.2.1 Related Work on Dynamic Gate Biasing

The first gate control strategy was introduced by Jieh-Tsorng and Kuen-Long (1998) where each CTS in the CP is controlled by a CMOS inverter composed of transistor MNi and MPi which acts as a gate control switch as depicted in Figure 2.14. The main concept of the gate control strategy is to utilize the lower voltage from the previous stage to effectively turn ON the PMOS CTS during the conduction phase, thereby reducing the threshold voltage drop in the CTS.

However, the topology suffers a shortcoming of undesired charge transfer. Taking the third stage of the CP circuit as an example, the reversion charge phenomenon can be observed as illustrated in Figure 3.1. As shown in Figure 3.1 (a), M3 is the PMOS CTS

while MN3 and MP3 are the gate control switches for M3. During the forward conduction phase, Φ_2 transitions from 0 V to V_{DD} while Φ_1 transitions from V_{DD} to 0 V. This results in a drop in node voltage 1 ($V1$) from 2 V_{DD} to V_{DD}, an increase in node voltage 2 ($V2$) from 2 V_{DD} to 3 V_{DD}, and a drop in node voltage 3 ($V3$) from 4 V_{DD} to 3 V_{DD}. In this scenario, MP3 remains turned on until $V2$ reaches $V3 - |V_{THp}|$, while MN3 starts turning on as soon as $V2$ reaches $V1 + V_{THn}$. Consequently, MN3 and MP3 are turned on simultaneously for a brief period T. Due to the higher voltage at V3 compared to $V1$ during this period, reverse charge occurs from node 3 back to node 1 through the gate control switch MN3 and MP3.

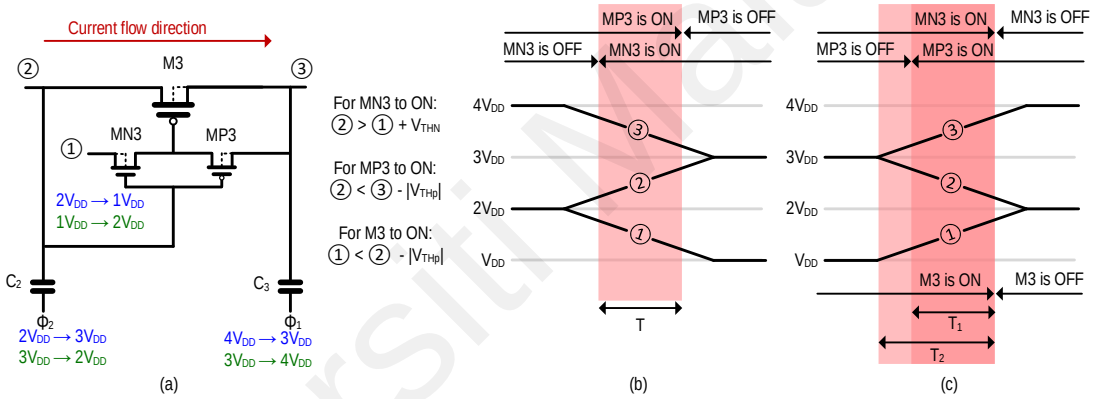

Figure 3.1: The Third Stage of a Conventional DGB's (a) Node Voltage Behavior and its Switching Waveforms at (b) Forward Conduction Phase (c) Reverse Conduction Phase

In the reverse conduction phase, Φ_1 transitions from 0 V to V_{DD} while Φ_2 transitions from V_{DD} to 0 V. The node voltage $V1$ rises from V_{DD} to 2 V_{DD}, $V2$ dropped from 3 V_{DD} to 2 V_{DD}, and V3 rises from 3 V_{DD} to 4 V_{DD} as shown in Figure 3.1 (b). In a similar manner to the forward conduction phase, MN3 continues to remain on until its gate voltage $V2$ decreases below $V1 + V_{THn}$. This leads to a period (T1) where both gate control switches are simultaneously on, allowing current to flow in the reverse direction from $V3$ to $V1$.

Furthermore, since the operation of M3 is dependent on the gate control switch, it cannot be turned off until MN3 is turned off to disconnect the gate terminal of M3 from node 1. This will result in an undesirable charge transfer from node 3 back to node 2.

Jiang et al. (2018) proposes an innovative advanced dynamic gate biasing technique where the gate terminal of the gate control switches is not interconnected as shown in Figure 3.2. This design ensures that the gate control switches have independent control signals, eliminating the possibility of both switches being activated simultaneously.

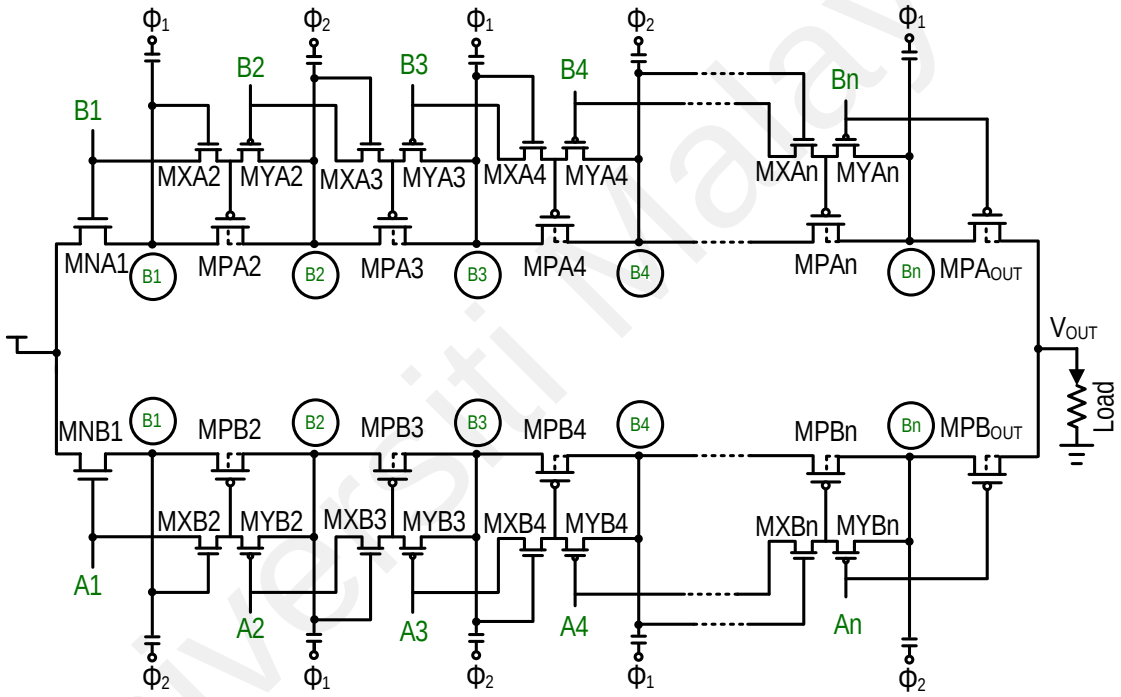

Figure 3.2: Dual branch CP employing advanced dynamic gate biasing technique (Jiang et al., 2018)

Taking the third stage of the advanced DGB CTS CP-1 configuration (Jiang et al., 2018) as an example, the transistors MXA3 and MYA3 serve as the gate control switches as shown in Figure 3.3 (a). The gate control switches are responsible for pulling a higher voltage from node A3 and a lower voltage from node A2 to the CTS MPA3. During the first clock cycle, as Φ_1 decreases from V_{DD} to 0 V and Φ_2 increases from 0 V to V_{DD}, the

node voltages at A3 and A2 change from $4\,V_{DD}$ to $3\,V_{DD}$ and from $2\,V_{DD}$ to $3\,V_{DD}$, respectively. MYA3 turns off when the voltage at $VB3$ is no longer lower than the voltage at node VA2 minus the threshold voltage V_{THp}. On the other hand, MXA3 turns on when the voltage at A2 is greater than the voltage at B2. As a result, there is a period when both gate control switches are off, as shown in Figure 3.3 (b). Consequently, no reverse current flows through MYA3 and MXA3, in contrast to the conventional DGB configuration.

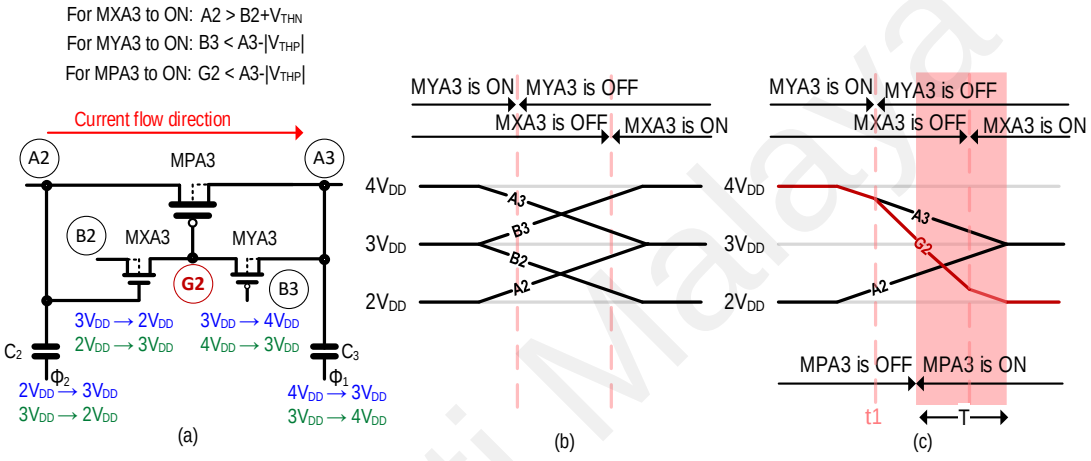

Figure 3.3: Forward Conduction Phase of the Third Stage of Advanced DGB CP-1's (a) Node Voltage Behavior (b) Switching Waveforms (c) Switching Waveform of MPA3's Gate Terminal

Despite the reduction in reverse current flowing through the gate control switch, some reversion current leakage still occurs on the CTS MPA3. Node G2 serves as the output of the gate control switch and is also the gate of transistor MPA3, as depicted in Figure 3.3 (c). In the first phase (before t1) when both MYA3 and MXA3 are ON, the voltage at node G2 is equal to the voltage at node A3. As both gate control switches turn off, the voltage at G2 gradually decreases until MXA3 is turned on. Eventually, with MYA3 off and MXA3 on, the voltage at G2 becomes equal to the voltage at node B2.

As transistor MPA3 will turn on when the voltage at node G2 is lower than $VA3 - |V_{THp}|$, the MPA3 turns on before the node voltages $VA3$ and $VA2$ stabilize at 3 V_{DD}. As the current goes from a higher potential to a lower potential, the reversion current flows from A3 to A2 through MPA3 for the period (T) where MPA3 is ON and the voltage of A3 is larger than that of A2.

Despite the improvements in mitigating the effect of undesired charge transfer during the forward conduction phase using advanced DGB in CP-1, the issue persists during the reverse conduction phase. As illustrated in Figure 3.4 (b), MPA3 won't be turned off until MYA3 is turned on to increase the gate control voltage of MPA3 regardless of the OFF state of MXA3. During this transition, as the voltage $VA3$ is greater than $VA2$, the delayed turning off of MPA3 results in undesired charge transfer from node A3 back to node A2 through MA3, as represented by the time period T in Figure 3.4 (b).

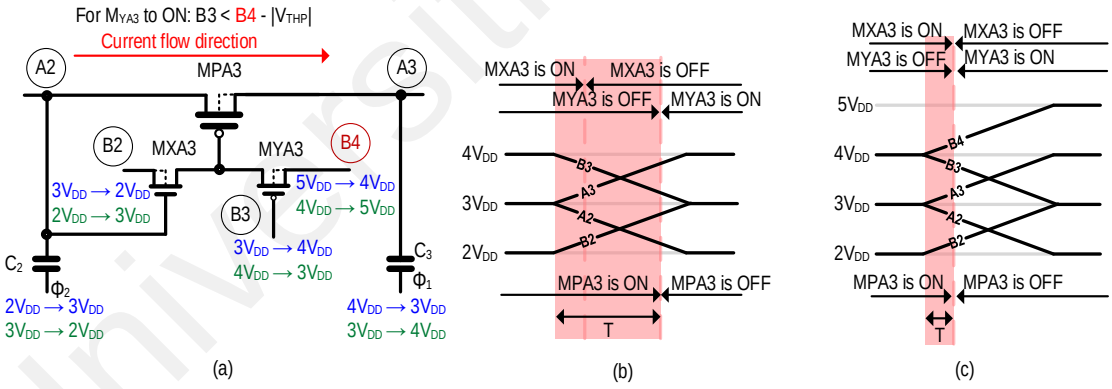

Figure 3.4: The Improved Advance DGB's (a) Schematic Diagram of CP-2's (b) Switching Waveform of CP-1 (c) Switching Waveform of CP-2

To resolve this issue, Jiang et al. (2018) introduced advanced DGB CP-2 where the PMOS in the gate control switch is pulling a higher voltage from two stages away as depicted in Figure 3.4 (a). Taking the third stage in Branch A as an example, the source terminal of MYA3 is connected to node B4 instead of node A3 in CP-1. With this

configuration, the turn-on criteria of MYA3 changed to B2 < B4 − $|V_{THp}|$ which allows it to turn ON earlier than in CP-1. This enables MPA3 to turn OFF in time, effectively reducing the reverse charge flow as shown in Figure 3.4 (c). The CP-2 advanced DGB technique encounters an issue as it necessitates a higher node voltage two stages away from the targeted CP stage. This poses a problem since there is no accessible node to tap the voltage at the last stage of the CP. Prior-art work (Abdelaziz et al., 2012; Po-Hung et al., 2010) suggests an additional CP stage to address the voltage requirement in the conventional DGB technique. However, applying the CP-2 topology would necessitate two extra CP stages for the advanced DGB technique which is not recommended for subthreshold application due to the increased losses from the additional stage which outweigh the reverse current reduction achieved by the last CP stage.

3.2.2 Proposed CP circuit

The proposed 3-stage CP, depicted in Figure 3.5, incorporates advanced DGB technique, dual switch configuration, and capacitance optimization. It consists of two parallel charge transfer paths (Path A and Path B) to parallelly transfer charges to the output during both forward and reverse conduction phases. The use of a dual path results in a smaller output ripple compared to the Dickson CP topology, which only has a single path. Moreover, the proposed dual-branch design features an independent connection, a departure from the conventional CCCP where the output of each stage is shorted together. This design prevents the reversion loss from one branch from affecting the performance of the current charging path in the other branch. In conventional CCCP as depicted in Figure 2.6, the net current flowing from one stage to another during one of the charging phases is represented by equation (3.1):

$$\boldsymbol{I_{OUT(net)} = I_{FWD} - I_{REV,a} - I_{REV,b}} \tag{3.1}$$

When the output path is split, the forward current becomes independent of the reverse current in the alternate path, as in Figure 3.5 which is also described in the equation (3.2) below:

$$I_{OUT(net,a)} = I_{FWD,a} - I_{REV,a} \tag{3.2}$$

This distinction is essential because, despite implementing the DGB technique, complete elimination of reversion loss is not achievable in subthreshold applications.

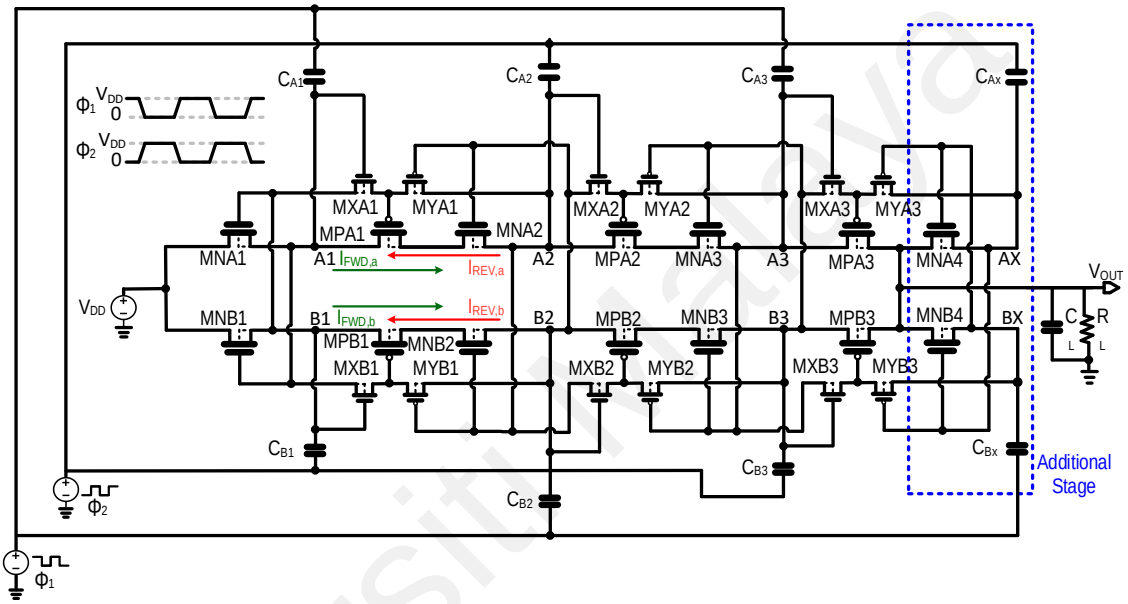

Figure 3.5: Proposed 3-stage CCCP Topology with Advanced DGB

Each stage of the proposed CP compromises NMOS (MNA,n, and MNB,n) and PMOS (MPA,n, and MPB,n) pairs for charge transfer. Additionally, each charge-transfer PMOS is accompanied by a set of gate control switches (MXA,n, and MXB,n) to implement the DGB technique. The distinct control signals from the NMOS-PMOS pair enable them to function as two-level control switches, effectively reducing the reversion current.

Figure 3.6 (a) presents the schematic of the 3rd-stage first-charging branch of the proposed CP. In this design, an enhancement is introduced to (Jiang et al., 2018)'s advanced DGB by incorporating an additional NMOS in each pumping stage. The inclusion of the NMOS acts as an extra control switch, effectively mitigating reversion current. The operation of MPA3, MXA3, and MYA3 remains consistent with the CP in Figure 3.3 (b).

Furthermore, MNA4, the additional NMOS, is triggered to turn ON when the voltage at node B3 surpasses $VA3 + V_{THn}$. As depicted in Figure 3.6 (b), MNA3 remains OFF until it fulfills its turn-on condition, which effectively reduces reversion loss during this period. Once MNA3 is activated, the path between A2 and A3 becomes fully accessible for charge transfer. It is worth noting that although reversion loss still occurs briefly during T when the voltage at node A3 exceeds that at node A2, this reversion loss is comparatively lower than that observed in the conventional advance DGB CP topology shown in Figure 3.3 (c).

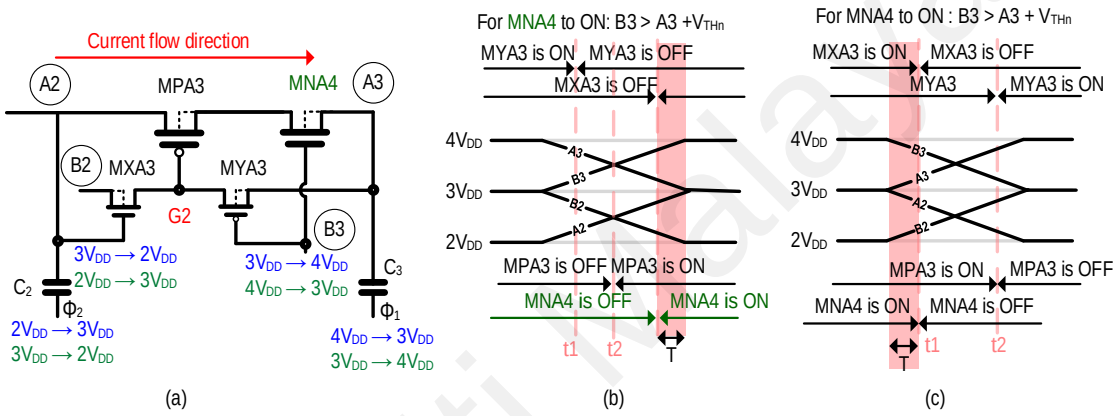

Figure 3.6: The Third Stage Proposed CP's (a) Schematic Representation (b) Switching Waveform During Forward Conduction Phase (c) Switching Waveform During Reverse Conduction Phase

During the reverse conduction phase, Jiang et al. (2018) addressed the issue of reverse current reduction by tapping the gate voltage from 2 stages away. However, this approach necessitates the addition of two extra auxiliary stages at the output as mentioned earlier. The proposed topology achieves the same reverse current reduction as CP-2 with only one additional CP stage. In Figure 3.6 (a), it is evident that MXA3, MYA3, and MPA3 exhibit behavior similar to the CP in the work of Jiang et al. (2018) during the second phase. The corresponding switching waveforms can be observed in Figure 3.4 (b). The addition of MNA4 significantly reduces the duration of the reversion current without the need to tap voltage from node B4. This is due to the turn-on criteria of MNA4 ($VB3 > VA3 + V_{THn}$),

which acts as a secondary switch to prevent reverse currents. While MPA3 turns OFF after t_2, as shown in Figure 3.6 (c), MNA4 turns OFF earlier at t_1, effectively stopping the reverse current leakage from A3 to A2. This optimized configuration results in improved reverse current reduction by using only one additional auxiliary CP stage.

3.3 Capacitance Optimization

Capacitance optimization is a technique of minimizing silicon area consumption of CP by leveraging the effect of pumping capacitance and CP performance to effectively allocate the pumping capacitance in CP.

3.3.1 Effect of Pumping Capacitance on Charge Pump

a) Single Stage Charge Pump

Figure 2.6 illustrates the conventional CCCP topology. The output voltage of the CP can be calculated using the following equation (3.3) (Ballo et al., 2019; Dickson, 1976):

$$\boldsymbol{V_{OUT} = (V_{IN} - V_{TH}) + N\left(\frac{V_{CK}}{1+\alpha_T}\right) - N\frac{I_{OUT}}{f_{CK}(1+\alpha_T)C'}} \tag{3.3}$$

In this equation, V_{IN} represents the input voltage, V_{CK} denotes the clock voltage, V_{TH} is the threshold voltage, I_{OUT} is the load current, f_{CK} represents the clock frequency, and α_T represents the ratio between the stray capacitance C_S and the pumping capacitance C_P. The value of α_T can be determined as the following equation (3.4):

$$\boldsymbol{\frac{1}{1+\alpha_T} = \frac{C_P}{C_P + C_S}} \tag{3.4}$$

The stray capacitance refers to the parasitic capacitance associated with the bottom plate of a pumping capacitor. As evident from the aforementioned equations, a larger pumping capacitor can mitigate the adverse impact caused by the stray capacitor. Consequently, an

increased pumping capacitance has the potential to enhance the PCE of the charge pump. The PCE can be calculated using the formula in equation (3.5) (Churchill et al., 2020):

$$\boldsymbol{PCE} = \frac{\boldsymbol{P_{OUT}}}{\boldsymbol{P_{IN}} + \boldsymbol{P_{CK}}} \times \mathbf{100}\% \tag{3.5}$$

where P_{OUT}, P_{IN}, and P_{CK} are the output power, input power, and the power consumption of the clock respectively.

An in-depth investigation into the impact of pumping capacitance is conducted by analyzing the node voltage at N_{a1} and N_{b1}. Figure 3.7 illustrates the variation in node voltage with different pumping capacitance values of a conventional CCCP. The energy stored in a smaller capacitor ($10\ pF$) is lower compared to larger capacitors ($30\ pF$ and $80\ pF$). When the clock amplitude is high, a portion of the charge stored in the capacitor is transferred to the next stage, causing a slight inclination in the node voltage N_{b1}. Node voltage Nb1 serves as the control signal for transistors M_{Na1} and M_{Pa1}. If N_{b1} is low, it results in high forward resistance and increased reversion loss on $M_{Na}1$ and M_{Pa1}. A similar issue arises at the complementary node N_{a1} (Churchill et al., 2020). When a larger pumping capacitor stores higher energy, the node voltage exhibits a square wave with minimal slope. Consequently, the high forward resistance and reversion loss are mitigated.

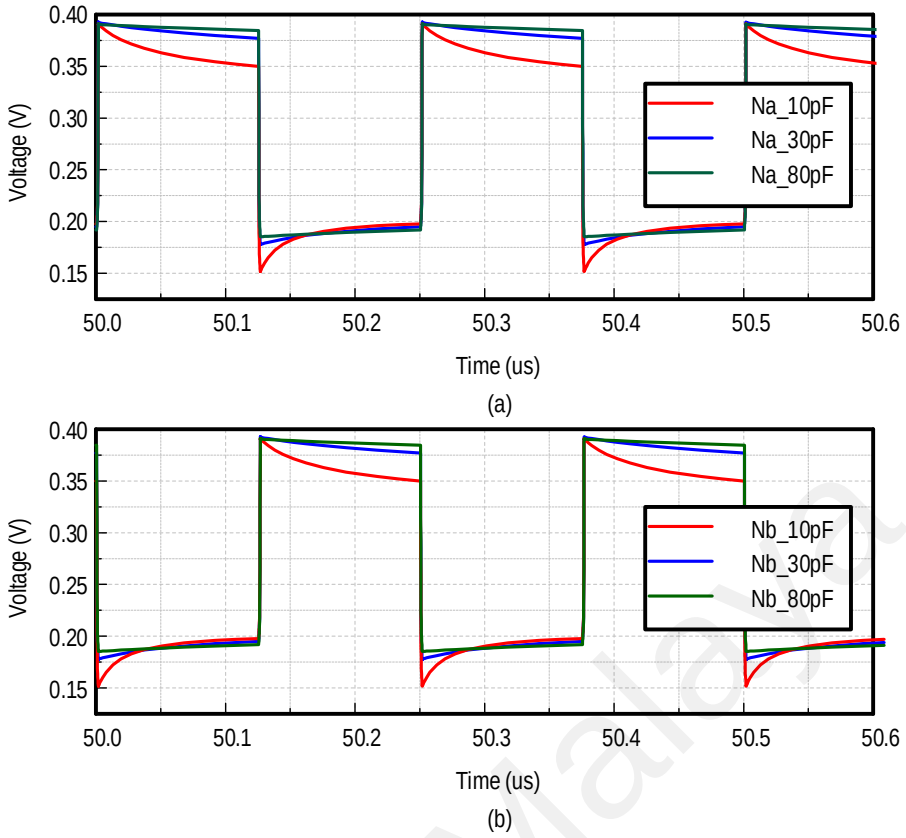

Figure 3.7: Node Voltage of CCCP at (a) First Pumping Branch (CLK) (b) Second Pumping Branch (CLKB) with Different Pumping Capacitance

The graph in Figure 3.7 demonstrates the relationship between capacitance and PCE at various input voltages. It reveals that increasing the pumping capacitance enhances the PCE. However, the impact on PCE becomes less significant as the pumping capacitance reaches higher values. This behavior aligns with the findings in equation (3.4). As the capacitor size directly affects silicon area and manufacturing cost, it is crucial to carefully select the appropriate pumping capacitance for optimal performance in the given charge pump application.

b) Cascading Charge Pump

In cascading the charge pumps, multiple stages are connected to generate a higher output voltage. Each stage can be considered as an independent charge pump, with the

input voltage obtained from the preceding stage. This relationship is expressed by equation (3.6) below:

$$\boldsymbol{V_{OUT,n+1} = V_{OUT,n} + V_{CK} - V_{loss,n}} \tag{3.6}$$

where $V_{OUT,n+1}$ and $V_{OUT,n}$ is the output voltage from current and previous charge pump stage respectively while $V_{loss,n}$ is the total voltage loss in one charge pump stage.

If the initial stage of a charge pump exhibits low efficiency and generates a lower voltage, it can have a cascading effect on the subsequent stages. This domino effect occurs as each stage relies on the output voltage of the previous stage as its input voltage. Consequently, if the first stage performs poorly, it impacts the overall efficiency of the entire charge pump. The relationship between PCE and input voltage is also depicted in Figure 3.8. When the charge pump operates in the weak inversion region, the PCE demonstrates an increasing trend with higher input voltages. This illustrates that raising the input voltage can positively influence the efficiency of the charge pump.

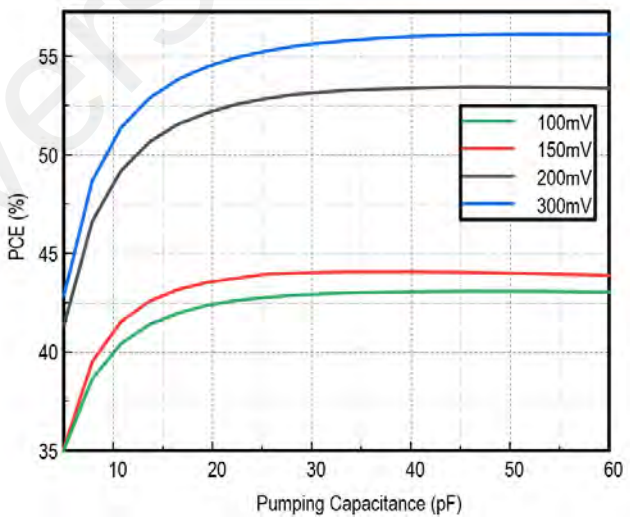

Figure 3.8: PCE of Single-Stage CCCP with Different Pumping Capacitance at Different Input Voltage Levels

Take a four-stage charge pump as an example, the performance of each stage is interdependent, with the first stage (CP1) influencing the subsequent stages (CP2, CP3,

and CP4). Specifically, CP1 affects the performance of CP2, which in turn affects CP3 and CP4. However, the last stage, CP4, does not impact the performance of any other charge pump stages. This hierarchical relationship highlights the importance of optimizing the earlier stages to ensure efficient operation and desired output voltage levels throughout the charge pump circuit.

c) Capacitance Optimization

Capacitance optimization utilized two key theories discussed in the previous section. First, the PCE of a CP increases with the size of the pumping capacitance until it reaches a saturation point. However, increasing the capacitance also leads to higher utilization of silicon area, resulting in increased manufacturing costs. Second, considering the domino effect, improving the performance of the initial charge pump stage is crucial. Given these considerations, this study places emphasis on optimizing the performance of the earlier charge pump stages by allocating a greater amount of capacitance to the initial stage.

Capacitance optimization is achieved by adjusting the sizing of the capacitors such that the earlier charge pump stages have higher pumping capacitance compared to the later stages. Figure 3.9 presents the simulation results of a 4-stage charge pump with various capacitance sizing combinations. In the conventional CCCP configuration, the capacitance is equivalent across all stages. In the D1-CCCP combination, the early stage has higher capacitance, while the subsequent stages have slightly lower capacitance. Conversely, the D2-CCCP configuration features high capacitance in the first stage, low capacitance in the last stage, and moderate equivalent capacitance in the middle stage. The A1-CCCP and A2-CCCP configurations are the direct opposite of the D1-CCCP and D2-CCCP configurations, respectively. An example of the capacitance scaling in this different configuration is shown in

Table 3.1.

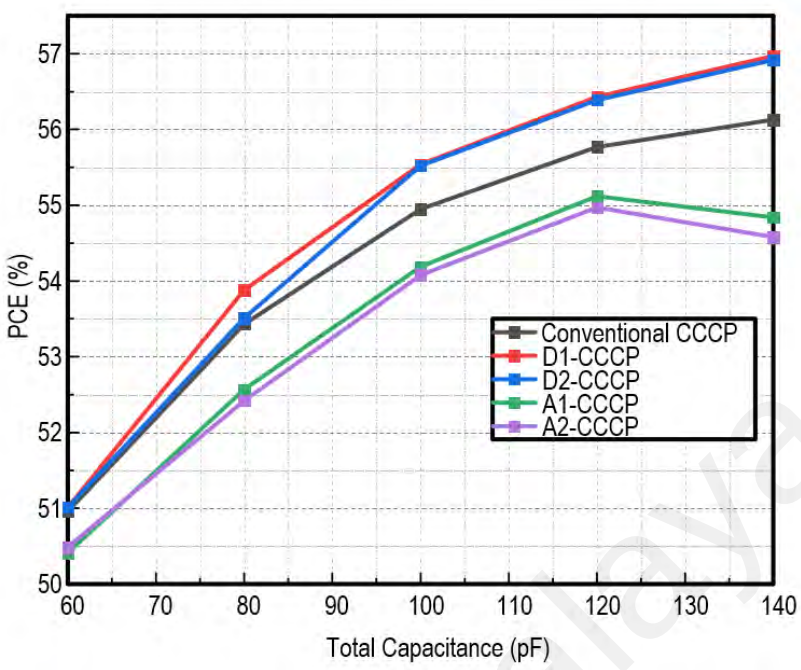

Figure 3.9: PCE of Different Capacitor Size Combinations

The simulation results depicted in Figure 3.9 reveal that both D1-CCCP and D2-CCCP configurations outperform the conventional charge pump, despite having the same total capacitance. In contrast, A1-CCCP and A2-CCCP exhibit lower PCE due to the smaller capacitance used in the early stage. It is important to notice that the improvement in PCE is more prominent when the total capacitance is higher, as there is a larger capacitance pool available for allocation to the early stage.

Table 3.1: Capacitance Scaling Configuration for Capacitive Optimization

Total Capacitance		60 pF	80 pF	100 pF	120 pF	140 pF
CCCP	C1 (pF)	15	20	25	30	35
	C2 (pF)	15	20	25	30	35
	C3 (pF)	15	20	25	30	35
	C4 (pF)	15	20	25	30	35
D1-CCCP	C1 (pF)	17	24	30	35	45
	C2 (pF)	16	22	27	33	40
	C3 (pF)	14	18	23	27	30
	C4 (pF)	13	16	30	25	25
D2-CCCP	C1 (pF)	17	14	30	35	45
	C2 (pF)	15	20	25	30	35
	C3 (pF)	15	20	25	30	35
	C4 (pF)	13	16	20	25	25
A1-CCCP	C1 (pF)	13	16	20	25	25
	C2 (pF)	14	18	23	30	35
	C3 (pF)	16	22	27	30	35
	C4 (pF)	17	24	30	35	45
A2-CCCP	C1 (pF)	13	16	20	25	25
	C2 (pF)	15	20	25	27	35
	C3 (pF)	15	20	25	33	40
	C4 (pF)	17	24	30	35	45

*C1,C2,C3,C4 represent the first, second, third and fourth stage of pumping capacitor respectively

3.4 Experimental Set Up and Result

3.4.1 Experimental and Measurement Set Up

This study adopts the experimental setup introduced by Ballo et al. (2022b), which is widely utilized in other works by the same author (A. Ballo et al., 2020a, 2020b; Ballo et al., 2022a). Figure 3.10 describes the measurement setup of this work. The fabricated chip is positioned on a probe station, where two measurement probes with the configuration of G, S, G, S, and G are connected to the bond pads of the chip die. To drive the circuit, a Keysight E8267D waveform generator is utilized, generating two asynchronous clock

signals with a 180-degree phase difference, corresponding to Φ_1 and Φ_2. Two 100 Ω series resistors are connected to the waveform generator to emulate the ring oscillator. Additionally, a Keysight 4156C DC voltage generator is employed to provide a stable input voltage (V_{DD}) to the chip. Similarly, a 100 Ω series resistor is placed at the CP's input to model the energy harvester's input (Ballo et al., 2018; A. Ballo et al., 2020b). On the output side of the setup, an off-chip adjustable resistor fabricated on a PCB serves as the load resistance of the circuit, while the output is measured with a digital multimeter.

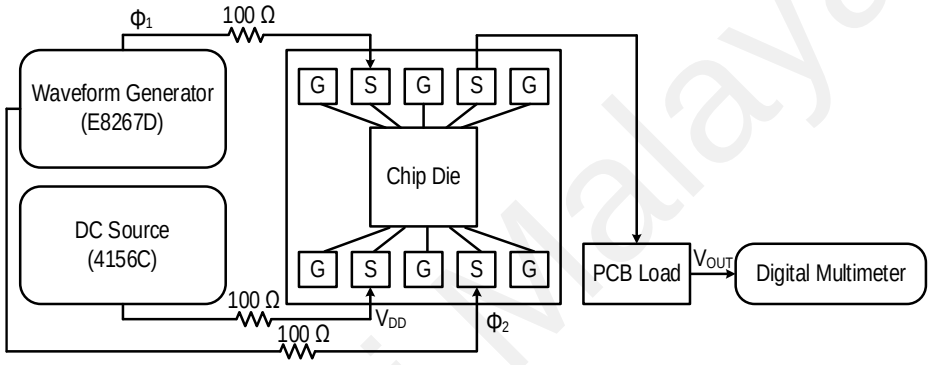

Figure 3.10: Schematic of the Measurement Set Up for the Proposed CP

Figure 3.11 showcases the chip micrograph of the proposed 3-stage subthreshold CP fabricated using TSMC 65 nm CMOS technology. The chip occupies an active area of 0.34 × 0.67 mm^2 where the majority area is dominated by the pumping capacitor. As capacitance optimization is applied, the pumping capacitance of the CP is scaled to 15, 13, and 12 pF respectively, with a pair of 1 pF auxiliary capacitors for DGB. This work incorporates MIM capacitors and Low-Voltage-Threshold (LVT) transistors with V_{TH} values of 370 mV (NMOS) and 360 mV (PMOS). LVT transistors are used in this work as they offer a lower threshold voltage which is suitable for subthreshold operation. By iterative simulation, the optimal pumping frequency of the work is set at 4MHz. To balance the free electron-to-hole ratio for efficient charge transfer, the size of the PMOS is twice that of the NMOS in the circuit design. Specifically, the NMOS CTS has a width of 66 μm, while the PMOS

CTS has a width of 96 µm. A smaller device is used for the gate control switch whereby NMOS has a width of 3.6 µm and PMOS is 7.2 µm. Additionally, the auxiliary NMOS at the last stage has a size of 4.8 µm.

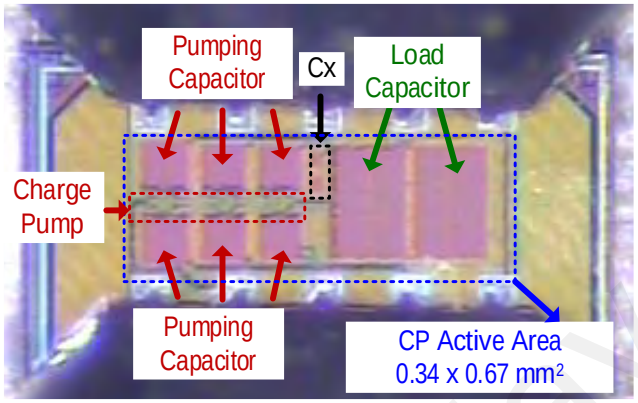

Figure 3.11: Chip Micrograph of the Fabricated Charge Pump Circuit

3.4.2 Experimental Results

Figure 3.12 presents a comparison of the measured PCE of the proposed CP with the performance of conventional Dickson CP and CCCP across the input voltage range from 0.04 V to 0.1 V. The data on the conventional CP's performance is extracted from the work (A. Ballo et al., 2020b). As depicted in the graph, there is a noticeable increase in PCE as the input voltage, V_{IN}, rises. This is attributed to the fact that at low input voltages, transistors may not turn ON/OFF effectively, leading to higher conduction and reversion losses, as elucidated in Chapter 2. The proposed CP exhibits a PCE of 10.49 % at 0.04 V and achieved 43.41 % at 0.1 V surpassing the conventional Dickson CP and CCCP at all input voltage ranges. These compelling results demonstrate the superior performance of the proposed CP and underscore its potential for low-voltage energy harvesting applications.

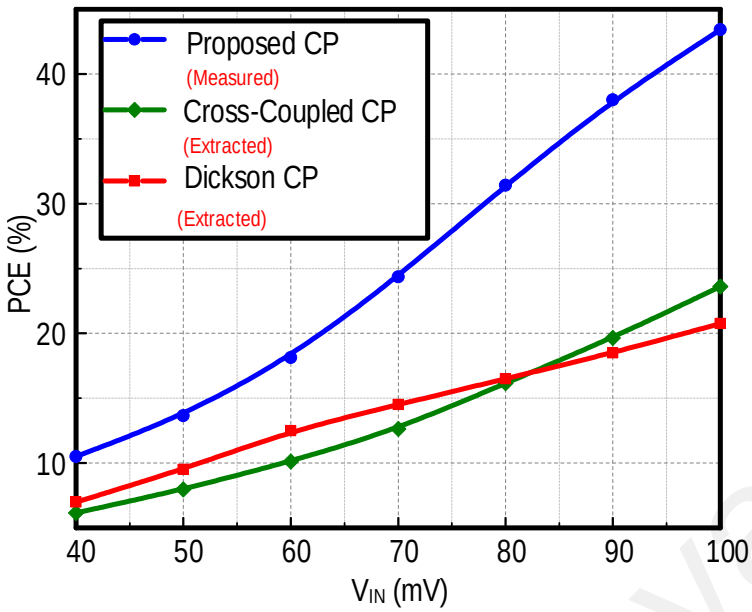

Figure 3.12: The Measured Power Conversion Efficiency of the Proposed CP Across Input Voltage Under 150 kΩ Load Condition

The transient response of the proposed CP is analysed with varying load conditions ranging from 50 kΩ to 250 kΩ with a resolution of 50 kΩ, as depicted in Figure 3.13. The graph shows the output voltage rises in correspondence with the increasing output load. It reaches a maximum of 0.346 V output at an open load with 0.1 V input voltage. Based on the equation (2.6), the proposed circuit achieved a peak VCE of 86.5 %. Additionally, the circuit demonstrates a start-up time of 0.02 ms.

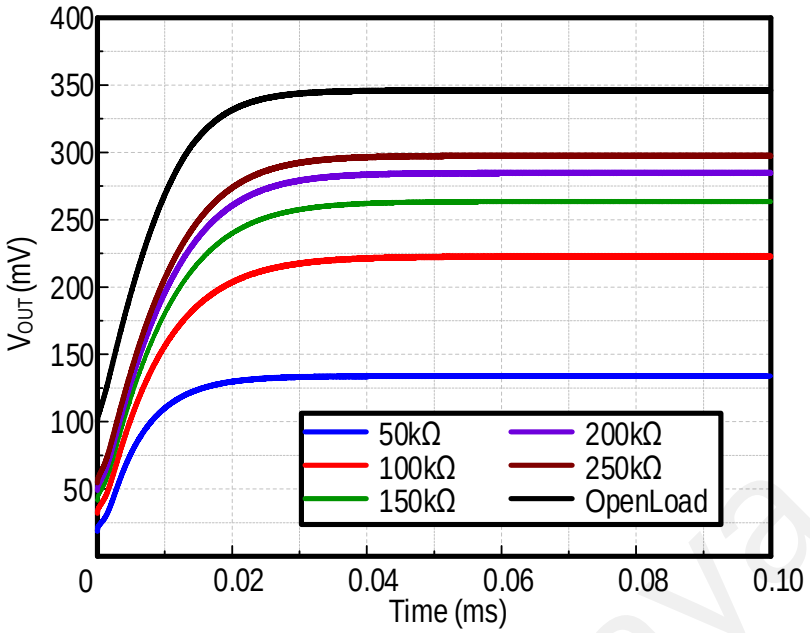

Figure 3.13: Transient Behaviour of Proposed CP Under Various Load Conditions at V_{IN} = 0.1 V.

Figure 3.14 illustrates the performance of the charge pump at various output currents with different input voltages. The circuit achieves a maximum output current of 2.664 µA at 100 mV input voltage with a PCE of 27.61 %. The peak PCE of the circuit is achieved at an output current of 1.744 µA with 100 mV input.

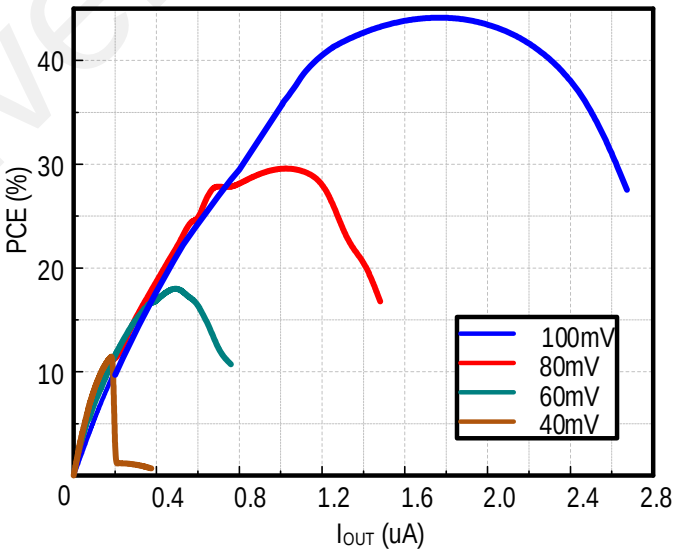

Figure 3.14: The Plot of Measured Power Conversion Efficiency Versus Output Current of the Proposed Charge Pump

A 3-dimensional plot of P_{OUT}, R_{OUT}, and PCE is presented in Figure 3.15. The plot demonstrates that the circuit achieves a maximum output power (P_{OUT}) of 490.7 nW at a load resistance of 100 kΩ. Moreover, the peak PCE is attained at 150 kΩ load condition with the output power of 457.9 nW.

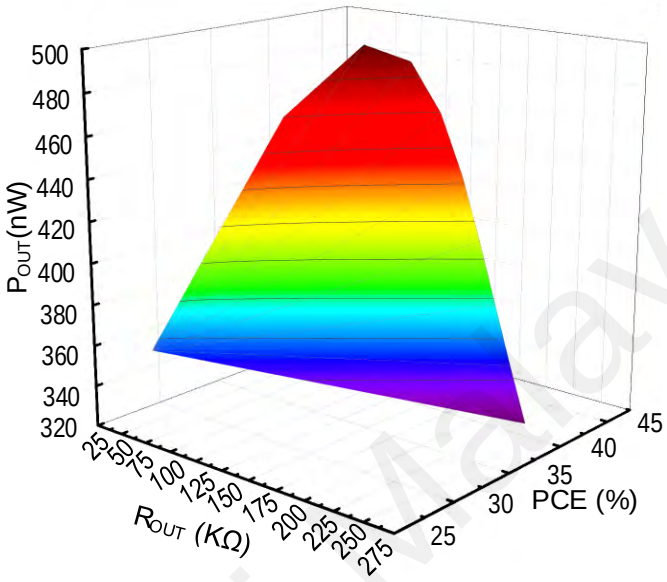

Figure 3.15: A 3-Dimensional Plot of Output Power Versus PCE of the Proposed Circuit Under Various Load Conditions

Table 3.2 presents a comparison of the proposed CP with the state-of-art low voltage subthreshold operation CP within a similar input voltage. The table highlights the CP's performance in terms of PCE, VCE, and the total capacitance used. Fabricated and measured with TSMC 65 nm CMOS technology with input voltage 0.1 V at a pumping frequency of 4 MHz, the proposed CP outperforms its counterparts with the highest peak PCE at 43.4 % and the highest peak VCE at 86.5 %.

3.5 Discussion

The experimental findings demonstrate the performance of the proposed 3-stage CP topology, showcasing its capability to achieve a 4-fold voltage boosting with ultra-low input voltages. Operating within a minimum startup voltage of 0.04 V and up to an

operational range of 0.1 V, the CP effectively delivers a steady and boosted DC output voltage to the load. The CP can produce a 0.346 V output voltage with a power of 457.9 nW at 0.1 V input under 50 to 275 kΩ load conditions. The achieved output voltage and power characteristics make this CP well-suited for various IoT applications. This included the source voltage for timer circuits in IoT devices, the start-up circuit for high-voltage DC-DC converter, and the power source for low-power wireless sensor networks.

The novel advanced DGB technique in conjunction with the dual switch configuration effectively mitigates the effect of reverse current loss. Moreover, the circuit harnesses the advantage of the dual branch switch connection CP to further enhance its performance in ultra-low input voltage. This combination of techniques contributes a superior performance as compared to the state-of-art low voltage CP as reported in Table 3.2. With the same input voltage of 0.1 V, (A. Ballo et al., 2020b) and (Fuketa et al., 2017) only achieved a PCE of 38.9 % and 33 % with the hybrid CP and gate-boosted CCCP respectively. While (Bose et al., 2019) reported a higher PCE with the same input voltage of $0.1\ V$ in the CP work, it is crucial to note that their circuit necessitates an inductive boost converter to kick-start the pumping operation. In order to maintain a fair comparison of low-voltage capacitive DC-DC boost converters, the work is not included in Table 3.2.

Table 3.2: Performance Comparison with the State-of-art Charge Pump

Author	This work	(A. Ballo et al., 2020b)	(Fuketa et al., 2017)	(Yi et al., 2018a)	(Chen et al., 2012)	(Kim et al., 2015)
CMOS Technology	65 nm	28 nm	65nm	65 nm	65 nm	130 nm
Number of Stages	3	2	10	3	10	3
CP Topology	CCCP	CCCP	CCCP	CCCP	CTS	CCCP
Proposed Technique	Advance DGB	Hybrid topology	Gate Boosting	BTRO, 3x Clock boost	Adaptive dual mode CP	Adaptive dead time + Dynamic bulk biasing
Input Voltage	100 mV	100m V	100 mV	150 mV	120 mV	180 mV
Peak PCE	43.4 %	[a]38.9 %	33 %	38.8 %	38.8 %	34 %
Peak VCE	86.5 %	[a]80 %	76 %	80 %	58 %	85.97 %
Maximum Output Power	480 nW	[a]6800 nW	6600 nW	1500 nW	3000 nW	-
Frequency	4 MHz	1 MHz	1 MHz	15.2 MHz	1 MHz	0.25 MHz
Total Capacitor	82 pF	120 pF	1001 pF	22.5 pF	286 pF	[b]60,000 pF
Load Capacitor	120 pF	120 pF	100 pF	30 pF	-	[b]10,000 pF

[a]Simulation result, [b]Off-chip

On the other hand, Yi et al. (2018a) introduce a novel bootstrap ring oscillator, which is able to generate non-overlap clock signals with a clock boosting effect. However, the main CP circuit implemented in the work follows a conventional CCCP topology, which is known to suffer from high reversion loss as discussed in Chapter 2. Consequently, the work only achieved a peak PCE of 38.8 %. In the study by Chen et al. (2012), a dual-mode CP is introduced, which can be configured into a hybrid Dickson topology for start-up and transformed into a conventional CTS CP topology during operational mode. Similar to the earlier mentioned work by Yi et al. (2018a), this work also employs conventional CP topology without any improvement to mitigate the reverse leakage loss in the switch connection transistor. In the work by Kim et al. (2015), a low-voltage CP adopting a dynamic body biasing technique with adaptive dead time control is implemented. However, the dynamic body biasing technique used in the work shares a similar principle with the conventional DGB in the work of Jieh-Tsorng and Kuen-Long (1998), leading to the same problem discussed in Chapter 3.2.1. Despite incorporating an adaptive dead time control circuit to mitigate the reversion loss, this additional circuit consumes a significant amount of power. As a result, the work reported a peak PCE of 34 % at 0.15 V.

3.6 Summary

A novel subthreshold operation dual branch CP employing an advanced DGB technique is presented in this chapter. Similar to the conventional DGB technique, the advanced DGB proposed in this work draws a higher voltage from the subsequent CP stage to turn off the PMOS CTS during the reverse conduction phase and draws a lower node voltage from the preceding CP stage to effectively turn ON the PMOS in forward conduction phase. The circuit further combines the advanced DGB technique with an NMOS-PMOS dual switch configuration to mitigate the reversion loss observed from the

conventional DGB's gate control switch. Moreover, a capacitance optimization technique for CP is introduced, leveraging the correlation of pumping capacitance and CP performance to optimize the silicon area used. Finally, a comprehensive performance comparison between the proposed 3-stage subthreshold operation CP and state-of-the-art CP architectures is presented at the end of the chapter, along with a thorough discussion of the experimental results.

CHAPTER 4 : RECONFIGURABLE SERIES-PARALLEL CHARGE PUMP

4.1 Chapter Overview

This chapter explores the series-parallel reconfigurable CP architecture to accommodate the wide voltage range from the RFEH input. The chapter begins with the charge pump reconfiguration concept and its main objective of reconfiguration. Then, it follows the operation principle, design, and control logic of the proposed reconfigurable CP. Subsequently, the chapter delves into the novel dynamic source-fed oscillator, integrated with the aim of achieving frequency modulation for the reconfigurable CP. This is followed by a comprehensive discussion and analysis of the research findings, including performance comparisons with previous studies. Finally, the chapter draws to a close with a succinct summary.

4.2 Proposed Reconfigurable Charge Pump

4.2.1 CP Reconfiguration Concept

The concept of reconfigurable CP is to modify the configuration of a CP such as topology or number of stages to achieve dynamic adaptation to the fluctuations in input voltage. Reconfigurable CPs are generally used for improving the PCE (Choo, Lee, et al., 2023; Choo et al., 2022; Choo, Ramiah, et al., 2023) and to constrain a bounded output voltage (Jiang et al., 2022) over a wide range of input voltages. As shown in Figure 4.1, the reconfigurable CP focusing on improving PCE of wide input voltage involves the combination of two CP configurations with distinct PCE curves to achieve a wide PCE range. Conversely, in the case of a reconfigurable CP aimed at limiting the output voltage, multiple CPs with distinct Voltage Conversion Ratios (VCR) are employed as in Figure 4.2. This dynamic alteration of the VCR ensures the maintenance of a bounded output voltage. In the scope of this thesis, the proposed reconfigurable CP primarily emphasizes the reconfiguration of VCR to confine the output voltage within desired bounds.

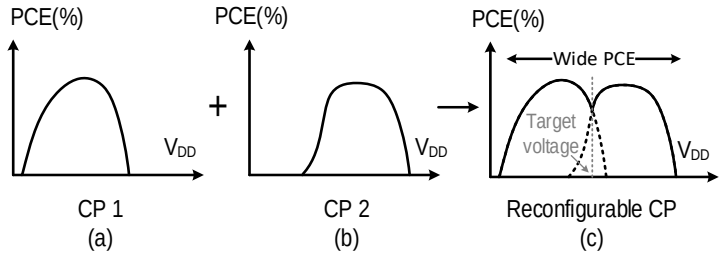

Figure 4.1: The PCE vs Input Voltage Curve of (a) Individual CP1 (b) Individual CP2 (c) Reconfigurable CP by Combining CP1 and CP2.

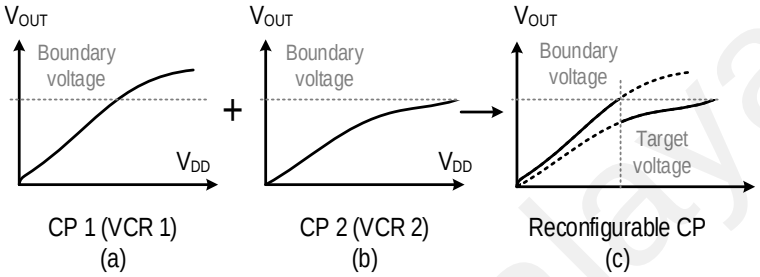

Figure 4.2: The Output Voltage of (a) Individual CP1 (b) Individual CP2 (c) Reconfigurable CP by Combining CP1 and CP2

4.2.2Proposed Series-Parallel Reconfigurable CP

The proposed CP scheme is illustrated in Figure 4.3. It achieves variable VCE by reconfiguring the number of stages, either in series or in parallel, based on the input voltage (V_{DD}). The scheme comprises three primary circuit blocks. Firstly, the clock generation unit generates two non-overlapping clock signals with a modulated frequency. Secondly, the logic control unit furnishes the CP with control signals. Lastly, the reconfigurable CP is responsible for boosting the output voltage.

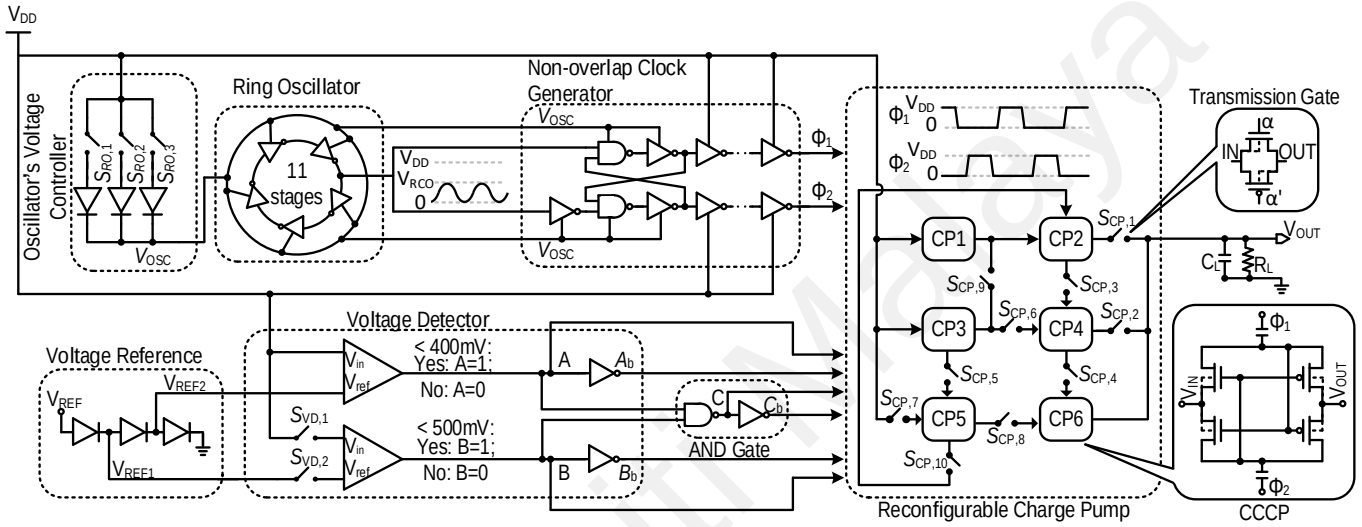

Figure 4.3: Top Architecture of the Proposed Series-Parallel Reconfigurable CP.

Table 4.1: Control Logic High Signal for Stage Reconfigurable CP

V_{DD} State	$S_{CP,1}$	$S_{CP,2}$	$S_{CP,3}$	$S_{CP,4}$	$S_{CP,5}$	$S_{CP,6}$	$S_{CP,7}$	$S_{CP,8}$	$S_{CP,9}$	$S_{CP,10}$	$S_{VD,1}$	$S_{VD,2}$	$S_{RO,1}$	$S_{RO,2}$	$S_{RO,3}$
$V_{DD} < 0.4$ V	0	0	1	1	0	0	1	0	1	1	0	0	1	0	0
$0.4 \text{ V} \leq V_{DD} < 0.5$ V	0	1	1	0	1	0	0	1	0	0	1	1	0	1	0
$V_{DD} \geq 0.5$ V	1	1	0	0	0	1	1	1	0	0	1	1	0	0	1
Control HIGH Signal	**C**	**Ab**	**Cb**	**A**	**B**	**C**	**Bb**	**Ab**	**A**	**A**	**Ab**	**Ab**	**A**	**B**	**C**

Within the reconfigurable CP, there are six individual CCCPs, each capable of configuring into 4 stages, 3 stages, or 2 stages depending on the detected input voltage. The CP's configuration is controlled by the transmission gates, denoted as SCP,1-SCP,10, which function as control switches for the reconfigurable CP. The primary advantage of employing a series-parallel reconfigurable CP is that every CP cell remains fully operational across all input voltage scenarios. Furthermore, the parallel CP configuration exhibits lower conduction loss due to its reduced equivalent circuit resistance, resulting in significantly reduced power loss during the charge-transfer phase (Flores & Espinosa, 2018).

As depicted in Figure 4.4, the proposed CP operates in three distinct modes. When the input voltage V_{DD} from the EH source falls below 0.4 V (V_{DD} <0.4 V), SCP,3,4,7,9,10 are turned activated while the remaining gates are OFF. Thus, the CP reconfigures to a 4-stage CP with a VCR of 5. In this configuration, CP1, CP3, and CP5 are connected in parallel in the first stage, boosting the voltage from V_{DD} to 2 V_{DD}; Subsequently, CP2 in the second stage boosts the voltage to 3 V_{DD}, CP4 operates in the third stage, and CP6 in the fourth stage as shown in Figure 4.4 (a). For V_{DD} between $0.4\,V$ and $0.5\,V$, SCP,2,3,5,8 are turned ON while the rest are deactivated. The CP is then reconfigured into a 3-stage configuration with 2 parallel paths. In this arrangement, CP1, CP2, and CP4 constitute the first CP path, and CP3, CP5, and CP6 form the second pumping path. Specifically, CP1,3 boosts voltage from V_{DD} to 2 V_{DD}; CP2,5 boosts 2 V_{DD} to 3 V_{DD} and CP4,6 boosts 3 V_{DD} to 4 V_{DD}. When V_{DD} exceeds 0.5 V ($V_{DD} > 0.5$ V), SCP1, SCP2, SCP6, SCP7, and SCP8 are activated, while the others are deactivated. The CP is reconfigured into 2 stages with 3 parallel paths. The first path comprises CP1 and CP2, the second path comprises CP3 and CP4, and the last path comprises CP5 and CP6. In this configuration, CP1, CP3, and CP5 form the first CP stage, boosting V_{DD} to 2 V_{DD},

while CP2, CP4, and CP6 constitute the second stage, responsible for boosting 2 V_{DD} to 3 V_{DD}.

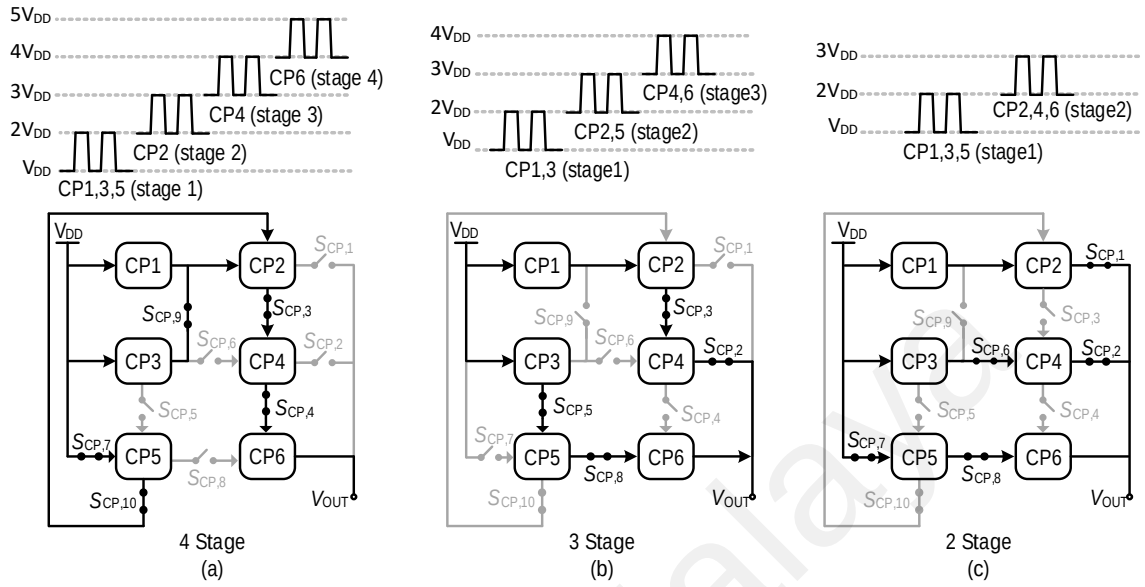

Figure 4.4: Proposed Reconfigurable CP (a) Scenario I, 4 Stages (b) Scenario II, 3 Stages (c) Scenario III, 2 Stages

4.2.4 Logic Control Unit

The logic control unit plays a pivotal role in furnishing the necessary control signals for managing the configuration of the CP. Table 4.1 presents a comprehensive breakdown of these control signals for each transmission gate, where logic 1 signifies the activation of the transmission gate, and logic 0 indicates that the switch is turned OFF. Examining the table reveals that the circuit relies on three distinct control signals (A, B, C) and their corresponding complements (Ab, Bb, Cb) to facilitate topology reconfiguration. For instance, when the CP is configured into 2, 3, and 4 stages, SCP4, SCP9, and SCP10 share the same logic signal sequence of 0, 0, and 1, respectively. In contrast, SCP2 and SCP8 exhibit the inverse of control signal A, with logic values of 1, 1, and 0.

To generate these essential control signals, a voltage detection unit is employed, consisting of two Op-amp-based comparators designed to identify three distinct voltage

levels: below 0.4 V, between 0.4 V and 0.5 V, and above 0.5 V. This work adopts the comparator design outlined in Yuen et al. (2019) for voltage detection. Two reference voltages (V_{REF1}, V_{REF2}) are derived from an external source (V_{REF}) using diode-connected transistors functioning as a voltage divider. V_{REF} can be sourced from a battery in a battery-assisted energy harvesting system. These reference voltages are then fed into the comparator within the voltage detection unit for voltage comparison.

The first comparator compares V_{DD} with V_{REF2}, set at 0.4 V, and returns a logic value of $A = 1$ if V_{DD} is less than V_{REF2}, or $A = 0$ if V_{DD} exceeds V_{REF2}. While signal A is high, SVD1 and SVD2 are deactivated, preventing the second comparator from consuming unnecessary power and keeping signal B low. When V_{DD} surpasses 0.4 V, signal A becomes LOW, activating the second comparator. This comparator compares V_{DD} with V_{REF1}, set at 0.5 V, and returns a logic value of $B = 1$ if V_{DD} is below V_{REF1} or $B = 0$ if V_{DD} exceeds V_{REF1}.

The circuit efficiently discerns the three distinct input voltage ranges (below 0.4 V, between 0.4 V and 0.5 V, and beyond 0.5 V) by relying solely on the two control signals derived from the comparators, namely, signals A and B. Nevertheless, signals A and B, when considered independently, do not provide a complete control solution for configuring the CP, as illustrated in Table 4.1. Consequently, an additional signal (C and Cb) is derived by applying an AND logic gate to signals A and B. The truth table outlining the AND logic operation for generating signals C and Cb is elucidated in Table 4.2. Using two comparators in conjunction with an AND logic gate, the circuit yields six distinct control signals, encompassing all conceivable logic combinations. This expanded control signal set lays the groundwork for potential future reconfigurable CP works, enabling configurations with varying numbers of stages.

Table 4.2: Truth Table for Reconfigurable CP's Control Signals

Scenario	V_{DD} State	No. stage	A	Ab	B	Bb	C	Cb
III	$V_{DD} \geq 0.5$ V	2 stages	0	1	0	1	1	0
II	$0.4\ V \leq V_{DD} < 0.5$ V	3 stages	0	1	1	0	0	1
I	$V_{DD} < 0.4$ V	4 stages	1	0	0	1	0	1
-	-	-	1	0	1	0	x	x

4.2.5 Dynamic Source-Fed Oscillator

a) Pumping Clock Generation

As highlighted in the literature review presented in Chapter 2, the utilization of frequency modulation proves indispensable within the context of RFEH systems, due to the broad spectrum of input voltage variations. In response to this challenge, this work proposes a dynamic source-fed oscillator as the clock generation unit which provides a dynamically adjustable input voltage that remains independent of the source voltage used for generating non-overlapping clock signals. The proposed approach achieves frequency regulation by modulating V_{OSC} (the oscillator's input voltage) while preserving the amplitude of the output clock signal, V_{Φ}.

The proposed clock generation unit comprises three key components: an Oscillator Voltage Controller (OVC), a Ring Voltage-Controlled Oscillator (RVCO), and a Non-Overlap Clock (NOC) generator. The OVC plays a pivotal role by extracting a lower voltage from V_{DD}, which serves as a dynamic input voltage for the RVCO. As illustrated in Figure 4.5 (a), (b), the OVC incorporates three distinct voltage divider paths, each characterized by varying effective resistances. Activation of these paths is accomplished through the control of transmission gates denoted as SRO1, SRO2, and SRO3, respectively, governed by signals A, B, and C. It's worth noting that the gate voltage for all transmission gates is sourced from V_{REF}, boasting an amplitude of 1.5 V.

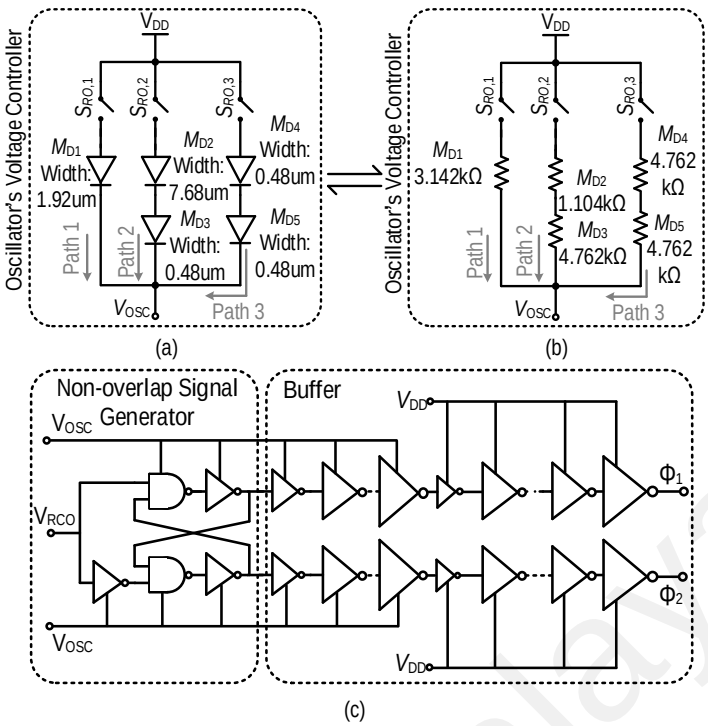

Figure 4.5: Proposed Oscillator's Voltage Controller Unit: (a) Schematic Diagram (b) Equivalent Resistant Model (c) Block Diagram of a Non-Overlap Clock Generator. The Size of the Inverters Represents the Transistors' Width.

Path 1 features a single diode-connected NMOS transistor with a large size, yielding an effective resistance of 3.142 kΩ. Path 2 comprises two diode-connected transistors with widths of 7.68 μm and 0.48 μm, resulting in a cumulative effective resistance of 5.806 kΩ. Meanwhile, Path 3 exhibits the highest total effective resistance, standing at 9.524 kΩ, originating from two small-sized transistors, each boasting a width of 0.48 μm.

The operational principle is elucidated through three distinct scenarios, akin to Section II-B. In scenario I, when V_{DD} is at a low level (V_{DD} <0.4 V), the activation of SRO1 initiates the first voltage divider path, characterized by a relatively lower effective resistance. This path's resistance reduces the V_{DD} voltage from the range of 0.26 V to 0.4 V down to the range of 269 mV to 240 mV, thereby providing a lower V_{OSC} for the oscillator. Moving to scenario II, the activation of the second path via SRO2 occurs. This

path, with its 5.806 kΩ resistance, further lowers V_{OSC} to a range between 180.5 mV and 201 mV, originating from a V_{DD} range of 0.4 V to 0.5 V, as illustrated in Figure 4.6. In scenario III, the engagement of SRO3 activates the path with the highest resistance, such as 9.524 kΩ. This path produces a V_{OSC} in the range of 207 mV to 257 mV. The three voltage divider paths collectively ensure the stable regulation of V_{OSC} for the RVCO, facilitating the generation of a modulated frequency.

This work incorporates an RVCO derived from the work in Bose et al. (2019) for clock frequency generation, which exhibits superior performance in comparison to conventional oscillators during subthreshold operation. However, instead of utilizing the supply node V_{DD}, this approach employs the previously generated V_{OSC} from the OVC as the voltage supply node. V_{OSC} is constrained within the bounds of 169 mV to 257 mV through the control signals A, B, and C. Consequently, the oscillator's generated frequency remains within the range of 4.3 MHz to 24 MHz, as portrayed in Figure 4.6. It's worth noting that an unbounded V_{OSC}, spanning from 168 mV to 384 mV, would lead to an unmodulated frequency surge from 4 MHz to 148 MHz, as delineated in the same figure.

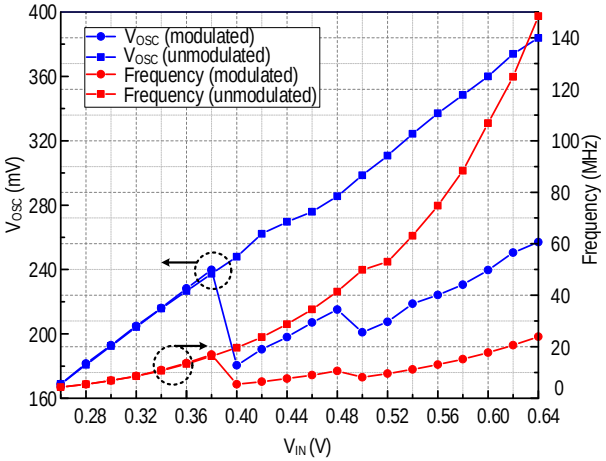

Figure 4.6: Plots of the Relationship Between Input Voltage, Oscillator Source Voltage, and the Modulated and Unmodulated Oscillating Frequencies

b) Non-overlap clock generator

The non-overlap clock generator is composed of two interconnected components, as illustrated in Figure 4.5 (c). The initial component features two cross-connected NAND gates, tasked with generating two non-overlapping signals essential for the operation of the CP. The subsequent component comprises a succession of cascading inverters, forming a buffer chain that refines the sinusoidal wave originating from the RVCO. It's noteworthy that this series of buffers is powered by V_{DD} as the supply voltage, rather than V_{OSC}. This design choice ensures that the final output clock maintains its amplitude at V_{DD}, thereby remaining independent of the lower amplitude V_{OSC} produced by the RVCO.

4.3 Experimental Result

The proposed reconfigurable CP is fabricated with TSMC 65 nm technology with an active area of 0.36 × 0.96 mm^2 as shown in Figure 4.7. To enhance performance during subthreshold operation (Chong et al., 2019), this work incorporated low-voltage threshold (LVT) devices for all charge transfer transistors, thereby reducing forward conduction losses. Meanwhile, other circuit blocks, such as the OVC and the comparator, employ standard threshold (SVT) transistors. In each CP stage of the circuit, two 20 pF MIM capacitors are employed to facilitate the pumping process.

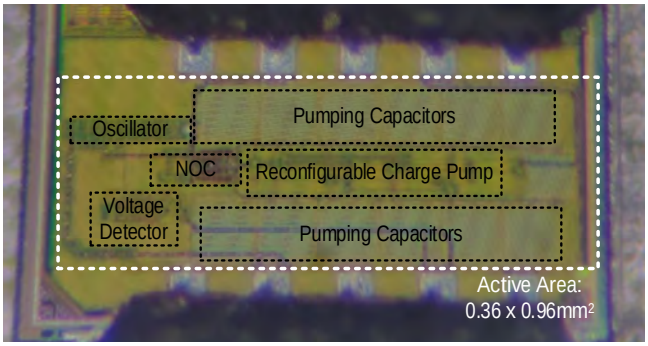

Figure 4.7: Photomicrograph of the Proposed Reconfigurable CP.

The measurement PCE and VCE results of the reconfigurable CP are portrayed in Figure 4.8. Figure 4.8 (a) shows the CP performance in different scenarios under various loads. The performance of the CP is peak at scenario II with the highest recorded at 62% PCE achieved under 50kΩ load condition. The proposed reconfigurable CP also exhibit over 85% VCE in every scenario as portrayed in Figure 4.8 (b). Figure 4.8 (c) illustrates the capability of the proposed CP to confine the output voltage across a wide input voltage range from 0.26 to 0.64 V by changing its VCR.

Similarly, Figure 4.9 showcases the performance of the circuit and its output voltage limiting capability under various input currents. Finally, the key performance of the proposed reconfigurable CP is recorded in Table 4.3. with the comparison with the state-of-the-art related reconfigurable CP work.

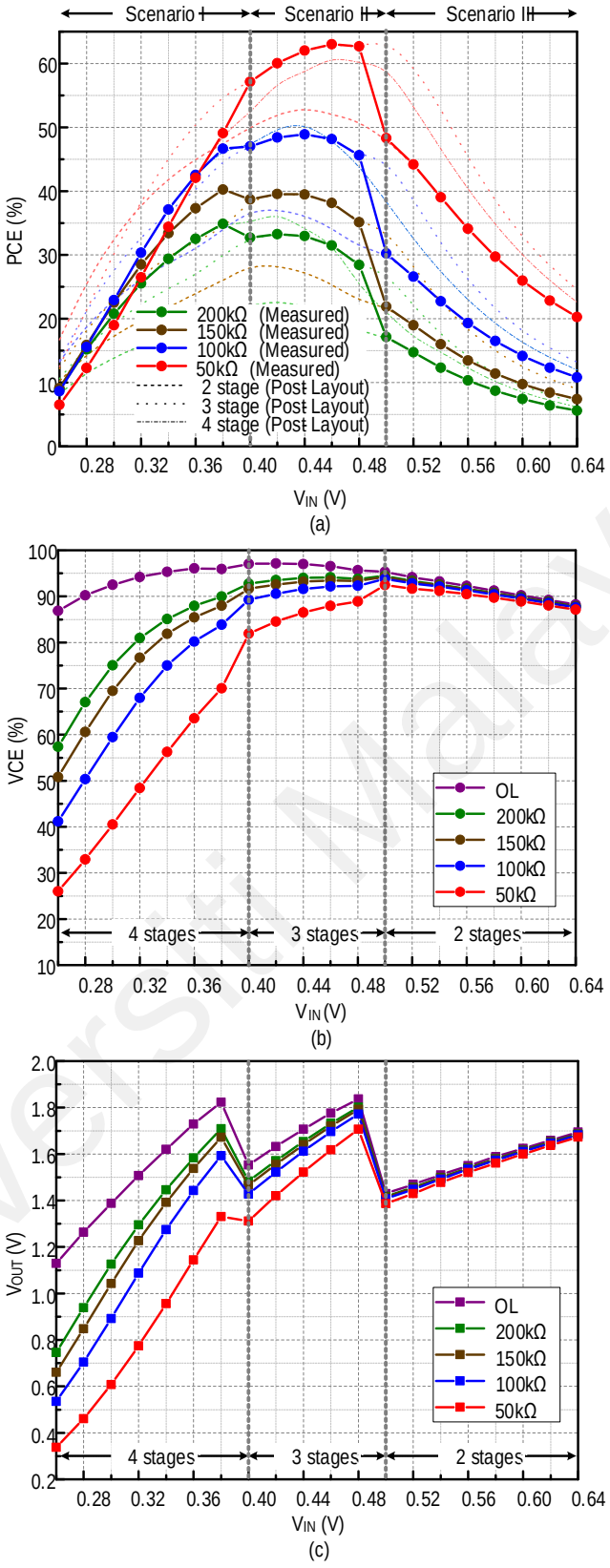

Figure 4.8: Measured Performance of (a) PCE vs V_{IN} (b) VCE vs V_{IN} (c) V_{OUT} vs V_{IN} at Various Output Load Conditions

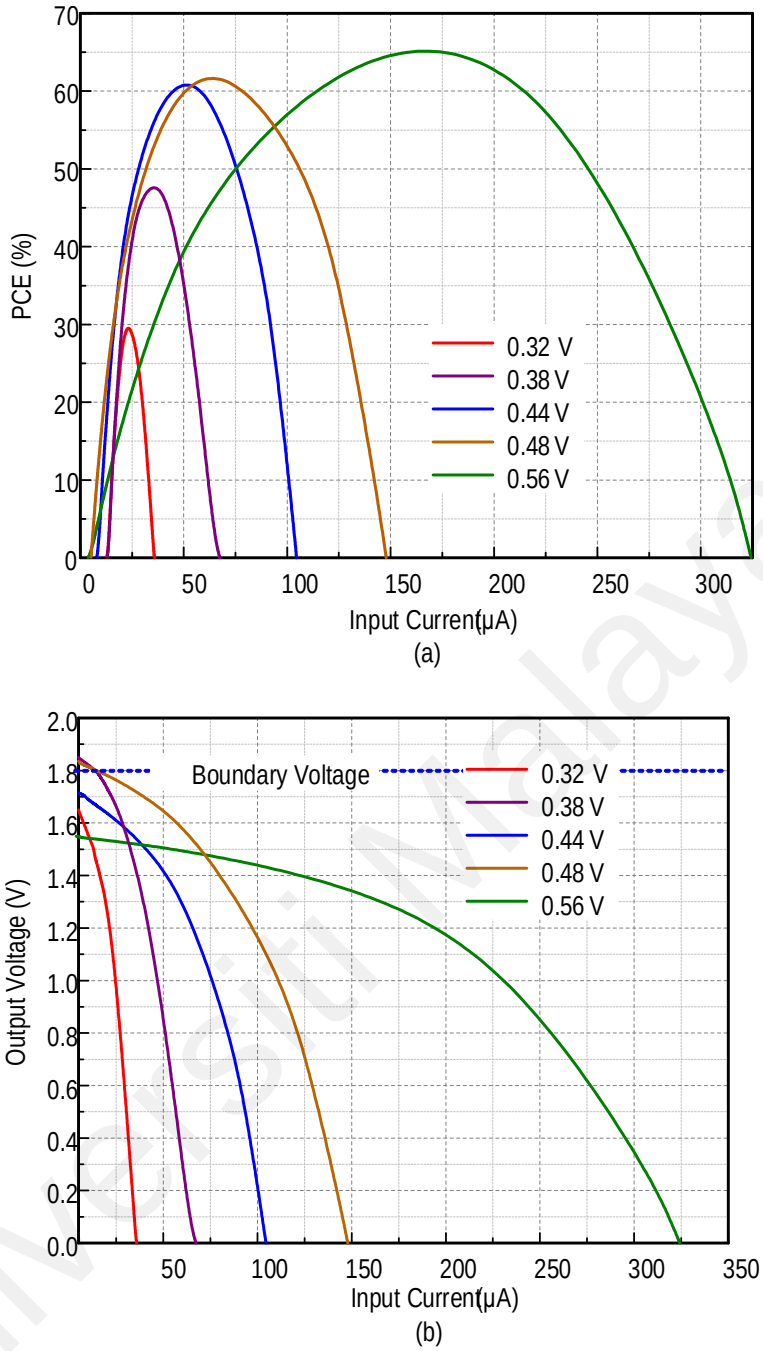

Figure 4.9: (a) Graph of PCE vs Input Current (b) Graph of Output Voltage vs Input Current at Various Input Voltage Under 100 kΩ Condition

Table 4.3: Performance Summary and the State-of-art Comparison of the Reconfigurable Charge Pump

Parameters	**This work**	(Carreon-Bautista et al., 2016)	(Shih & Otis, 2011)	(Tsai et al., 2014)	(Jung et al., 2014)	(Kim & Kim, 2023)	(Ballo et al., 2021)
CMOS	**65 nm**	180 nm	130 nm	180 nm	180 nm	180 nm	65 nm*
No. of Stage	**2,3,4**	1~9	4	4~6	4	4	2 ~ 4
Output Voltage Regulation Technique	**Series-Parallel CP**	Variable stage selection	Resistive voltage divider	Variable stage selection	Variable cascaded stage	Fast-transient dynamic reconfigure	Variable stage selection + clock amplitude reduction
Frequency Modulation Technique	**Dynamic source-fed oscillator**	Variable delay cell stage	Test register	Dynamic voltage for delay blocks	Dynamic voltage for delay blocks	TFM	-
Input Voltage (V)	**0.26~ 0.64**	0.25~ 1.1	0.27~ 1.4	1	1.2	2	0.45 ~ 0.7
Regulated Voltage (V)	**1.8**	1.8	1.4	3~6	2.2	6~10	1.2 ~ 3
Frequency (MHz)	**4.3~24**	0.75~7.5	0.6~1	0.01~20	$70x10^{-6}$ ~19	-	10
Peak PCE (%)	**62**	57	58	58	75	69.8	73*
Area (mm^2)	**0.346**	-	0.42	0.5	0.069	0.66	0.023**

*simulation result ** oscillator not included

4.4 Discussion

The experimental results show that the proposed reconfigurable CP can efficiently adapt its VCR to limit the output voltage while maintaining a high PCE. As shown in scenario I of Figure 4.8 (V_{DD} < 0.4 V), the combination of LVT devices and the parallel CP configuration allows the reconfigurable CP to achieve a high PCE in subthreshold operation. Moving to scenario II, the CP reconfigures into 3 stages with 2 parallel paths, effectively reducing its effective resistance and consequently achieving a high PCE. Notably, the CP's performance in scenario II surpasses that of scenario I because the transistors are no longer operating in the subthreshold region, thanks to the higher input voltage. The peak PCE is recorded in scenario II, reaching 62 % at 0.48 V when driving 50 kΩ loads. However, despite having three parallel pumping paths, the CP's performance deteriorates in scenario III. This decline is attributed to the fact that the CP is optimized for low input voltage operation. In high-voltage conditions, the CP experiences significant reverse current leakage across the LVT transistors. Furthermore, the utilization of a 2-stage CP results in a circuit mismatch, leading to an inefficient transfer of power to the output load. To limit the bounded output voltage, the CP's performance is sacrificed in scenario III.

The VCE of the proposed reconfigurable CP is depicted in Figure 4.8 (b). The CP consistently exhibits VCE values of over 80 % across all voltage ranges, with the highest VCE reaching 97% observed under open load conditions at an input voltage of 0.4 V. Notably, the proposed circuit effectively limits the output voltage under 1.8 V across various load conditions, spanning an input voltage range of 0.26 V to 0.64 V, as demonstrated in Figure 4.8 (c). As the input voltage increases from 0.26 V to 0.4 V, the circuit dynamically reconfigures into 3 stages, reducing its VCR to 4 and ensuring that

V_{OUT} remains below 1.8 V. A similar behaviour is observed at 0.5 V, where the circuit configures into 2 stages, as illustrated in the same figure.

The plot in Figure 4.9 (a) shows the measured performance of the CP as a function of the input current. Notably, the peak PCE shifts to the right as the input voltage increases, indicating that lower-stage configurations perform better with higher input currents. The proposed CP has been subjected to testing with various input currents, encompassing a range of up to 325 μA. Figure 4.9 (b) illustrates the relationship between the input current and the output voltage of the proposed circuit. This figure clearly illustrates the circuit's effective maintenance of the output voltage within the specified boundary for most input current levels, except when the input voltage approaches the configuration switching points at 0.48 V and 0.38 V. However, it's worth highlighting that the circuit can still uphold the boundary voltage even at very low input current levels, as low as 15 μA.

Table 4.3 serves as a comprehensive summary and comparison of our proposed system with state-of-the-art reconfigurable CP solutions. In (Shih & Otis, 2011), an output feedback mechanism is employed to limit the output voltage to 1.4 V. This technique relies on a resistive voltage divider that adapts its division ratio based on a comparison between the output voltage and a bandgap reference voltage. However, this approach incurs power losses due to voltage absorbed by the resistive voltage divider. Meanwhile, other related works (Carreon-Bautista et al., 2016; Jung et al., 2014; Tsai et al., 2014) regulate the output voltage by adjusting the number of CP stages in operation, akin to our proposed method. However, they deactivate CP stages instead of connecting them in parallel. This choice negates the advantage of low equivalent circuit resistance achieved through parallel CP connections, potentially reducing harvesting efficiency.

In terms of frequency regulation, Carreon-Bautista et al. (2016) employ a variable delay cell configuration for frequency modulation, involving multiple stages of delay

cells to generate the desired frequency. Nevertheless, as depicted in equation (2.16), the use of numerous delay stages increases power consumption in the clock generation circuit. Conversely, (Jung et al., 2014) and (Tsai et al., 2014) perform frequency modulation by varying the voltage source of the delay cell, similar to our approach. However, the work used the CP output as the dynamic source for the delay stages, leading to high power losses in the delay cells due to the elevated voltage levels. Table 4.3 illustrates that the proposed reconfigurable CP outperforms other state-of-the-art reconfigurable CPs in low-voltage energy harvesting applications (Carreon-Bautista et al., 2016; Shih & Otis, 2011; Tsai et al., 2014), achieving a peak PCE of approximately 58 %. While some recent works (Jung et al., 2014; Kim & Kim, 2023) achieved slightly higher PCE values, these were achieved at higher input voltages. Additionally, Ballo et al. (2021) reported a 73 % PCE, but it was based solely on simulation results and did not consider the power consumption of the oscillator. Moreover, the proposed solution boasts the lowest circuit complexity, occupying a modest silicon area of only 0.346 mm^2.

4.5 Summary

A novel series-parallel reconfigurable CP employing a dynamic source-fed oscillator is presented in this chapter. Operating within an input voltage range of 0.26 V to 0.64 V, the CP effectively sustains a stable output voltage through dynamic VCR adjustments. In low input voltage scenario (input voltage < 0.4 V), the proposed CP reconfigures into 4 stages configuration, yielding a higher voltage boosting effect; when input voltage is in the range of 0.4 V to 0.5 V, the CP reconfigures into 2 parallel, 3 stages configuration; when the input voltage is higher than 0.5 V, the CP reconfigures into 3 parallel, 2 stages configuration, lowing its voltage conversion ratio. The low internal resistance of the parallel configuration in the proposed CP contributes to its higher performance. Moreover, the dynamic source-fed oscillator achieves frequency modulation with

superior power efficiency compared to prior implementations. The performance of the proposed CP is summarized in a table of comparison, and the experimental results are discussed.

CHAPTER 5 : FULLY INTEGRATED CMOS AMBIENT RFEH SYSTEM

5.1 Chapter Overview

This chapter delves into the design of a novel low-power output voltage monitoring unit for RFEH systems, showcasing an alternative voltage-limiting strategy without the use of reconfigurable CP. The output voltage monitoring unit and voltage limiter are designed and optimized to limit a boundary voltage of 3.3 V, catering towards WSN applications. The chapter begins with elucidation of the operational principles governing the novel voltage sensing circuit. Then, the operation of the output voltage limiter is discussed. The chapter later proceeds with the implementation of the proposed voltage monitor on RFEH systems. This is succeeded by the presentation and analysis of research findings with the performance benchmarking relative to prior works. Lastly, the chapter draws to a close with a summary.

5.2 Proposed RFEH System with Output Voltage Limiter

Figure 5.1 illustrates the proposed fully integrated RFEH system, which is composed of two main components: the RF-DC energy harvesting blocks and the voltage monitoring unit. The front-end RF harvesting block incorporates the IMN, a primary rectifier, and an auxiliary rectifier which are responsible for converting the scavenged AC power into usable DC power. On the other hand, the voltage monitoring unit consists of a voltage sensing circuit and a voltage limiter to maintain the output voltage under a boundary level of 3.3 V suitable for WSN applications.

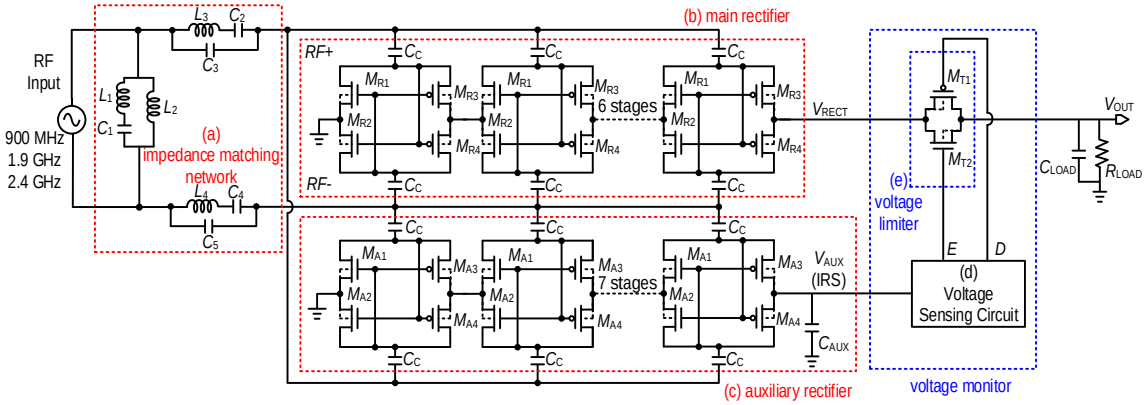

Figure 5.1: The Schematic of RF-DC Energy Harvesting Circuit with Output Limiting Capabilities: (a) IMN (b) Main Rectifier (c) Auxiliary Rectifier (d) Voltage Sensing Circuit (e) Voltage Limiter

5.2.1 RF-DC Rectifier

Cross-couple differential drive (CCDD) is implemented as the main rectifier as delineated in Figure 5.1 (b). It serves the dual purpose of converting and elevating the harvested AC RF energy into a stable DC power source, denoted as V_{RECT}. Prior to supplying this power to the load, it undergoes scrutiny by the voltage monitor. As discussed in CHAPTER 2 The output voltage, of the RFEH system, V_{OUT} is directly proportional to the input power, P_{IN}. If the P_{IN} is high, the RFEH will produce a high boosted V_{OUT}, potentially damaging the connected load. To prevent this, the system employs an auxiliary rectifier and a voltage monitor to constrain V_{OUT} within a specified voltage boundary.

The auxiliary rectifier operates within the secondary path, generating an independent voltage, denoted as V_{AUX} which has a higher voltage compared to V_{RECT}. V_{AUX} assumes the role of an Input-Representing-Signal (IRS) which signifies the scavenged input power level. Since P_{IN} fluctuates due to its AC nature, IRS provides a more stable alternative for voltage detection. Thanks to its linear correlation with P_{IN}, the voltage monitoring unit can track the IRS voltage level to enact voltage constraints effectively. Additionally,

V_{AUX} serves as the source voltage for the voltage sensing circuit, enabling the generation of control signals that facilitate the voltage monitoring unit's operation.

The decision to use a seven-stage auxiliary rectifier, which is one stage higher than the main rectifier, was made to generate a higher amplitude of V_{AUX} compared to V_{RECT}. The rationale behind this choice lies in the control signal for the transistors within the voltage limiter, which relies on V_{AUX}. By employing a control signal with a higher amplitude than the output from the main rectifier, the voltage limiter gains the capability to efficiently regulate the output voltage.

5.2.2 Voltage Monitor

a) Voltage Sensing Circuit

Figure 5.2 (a) depicts the proposed voltage sensing circuit, which incorporates two voltage divider paths, (VDP1, VDP2) and an inverter chain equipped with current-limiting gate-ground transistors. This circuit represents an enhancement over (Kim et al., 2015)'s V_{TH} sensing circuit. Rather than relying on diode-connected NMOS, as seen in some state-of-art work (Mostafa et al., 2011; Olivieri et al., 2005), the proposed voltage sensing circuit utilizes CMOS inverters to perform voltage detection. Furthermore, the integration of a voltage divider network enhances the circuit's capacity to detect voltages across a broader range, extending beyond the V_{TH} threshold of a transistor.

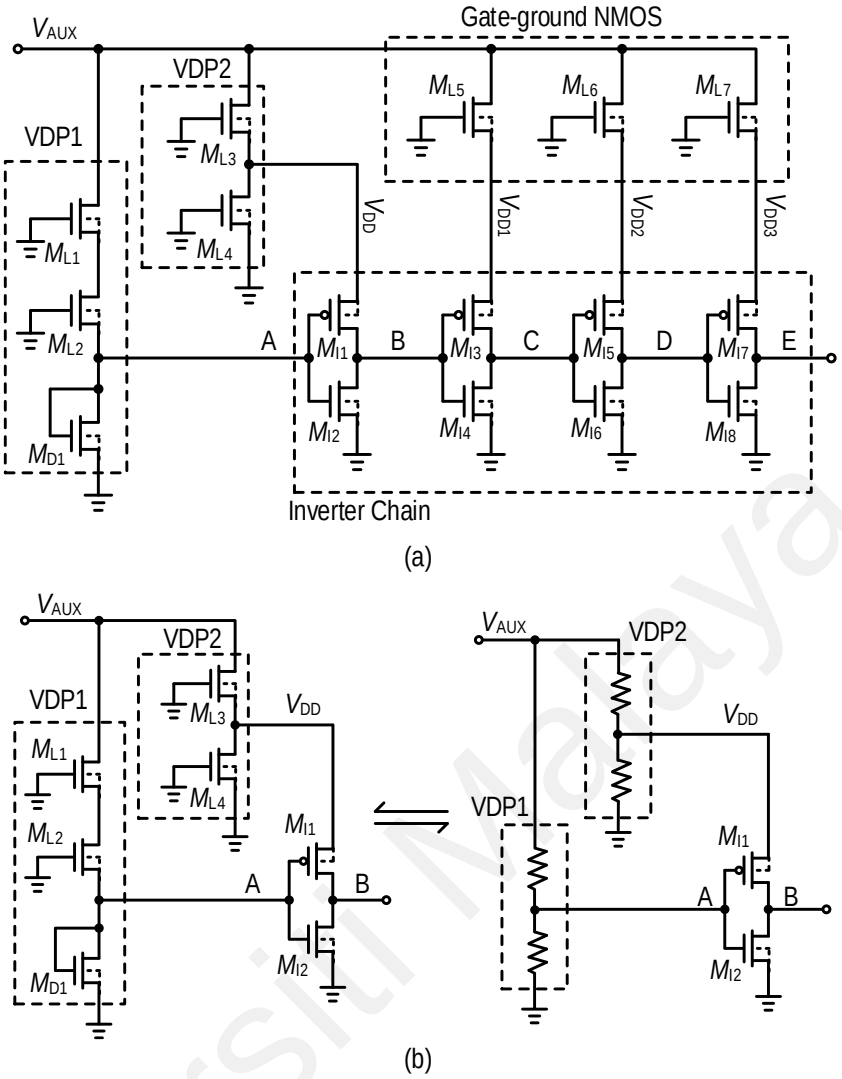

Figure 5.2: The Schematic Diagram of (a) The Proposed Voltage Sensing Circuit. (b) The Voltage Divider Path for the CMOS Inverter Voltage Sensing Unit and its Equivalent Resistance Ratio Model

1) CMOS Inverter as a Voltage-Sensing Unit:

A conventional CMOS inverter takes a control signal (signal A) as input and produces the inverted source voltage of the inverter (V_{DD}) as its output. To clarify the operation of a CMOS inverter, it's important to note that the turn-on criterion for NMOS is $V_{GS} > V_{TH}$, while for PMOS, it's $V_{GS} \leq |V_{TH}|$. The operation mode of a CMOS inverter is summarized in Table 5.1. When V_{DD} falls below the threshold voltage of both NMOS and PMOS (assuming equal V_{TH} values), the inverter fails to perform its intended operation

of signal inversion, resulting in a logic-low output, regardless of the input signal A. Conversely, when V_{DD} exceeds V_{TH}, the inverter operates normally and produces a high output voltage only when signal A meets the criteria outlined in scenario 1. This unique characteristic allows a CMOS inverter to serve as a V_{TH} voltage sensing unit for signal A.

Table 5.1: Operation Mode of a Conventional Inverter

Operating Mode		$V_{DD} \leq V_{TH}$ (Inverter fails to operate when V_{DD} is too low)	$V_{DD} > V_{TH}$
$A < V_{DD} - V_{TH}$	$A \leq V_{TH}$	**Scenario 4** NMOS OFF PMOS always OFF Output = 0	**Scenario 1** NMOS OFF PMOS ON Output = V_{DD}
	$A > V_{TH}$	**Scenario 5** NMOS ON PMOS always OFF Output = 0	**Scenario 2** NMOS ON PMOS ON Output = 0
$A \geq V_{DD} - V_{TH}$	$A > V_{TH}$	**Scenario 6** NMOS ON PMOS always OFF Output = 0	**Scenario 3** NMOS ON PMOS OFF Output = 0

To enable the detection of voltage levels other than V_{TH}, two voltage divider paths are employed to generate both V_{DD} and signal A for the inverter. The first voltage divider path (VDP1) comprises two gate-ground transistors at the top and a diode-connected transistor at the bottom, effectively representing a series resistance, as depicted in Figure 5.2 (b). Similarly, the diode-connected NMOS at the bottom can be regarded as a lower-resistance component. At the top of voltage divider path 1 (VDP1), two gate-ground

transistors are connected in series to increase the resistance ratio compared to the lower part. This arrangement is employed to extract signal A from V_{AUX}. Conversely, voltage divider path 2 (VDP2) consists of two gate-ground transistors designed to extract V_{DD} from V_{AUX}.

As V_{AUX} increases with the harvested input power, both V_{DD} and signal A also experience increments. However, due to the distinct resistance ratios, VDP2 exhibits a higher rate of voltage increment compared to VDP1. When designing the circuit, it is essential to configure the resistance ratio of VDP2 in such a way that when V_{AUX} reaches the target voltage ($V_{AUX} = 3$ V), the extracted V_{DD} equals the V_{TH} threshold. This alignment ensures that signal B initiates an upward trend when V_{AUX} surpasses the target voltage, as illustrated in Figure 5.3. It is apparent that the inverter fails to perform its signal inversion operation when the voltage at V_{AUX} falls below the 3 V target voltage. This occurs because V_{DD} remains below the threshold voltage (V_{TH}), resulting in a low voltage output for signal B. Once the voltage at V_{TH} exceeds the target voltage, the inverter transitions to scenario 1, generating an output voltage that matches V_{DD}.

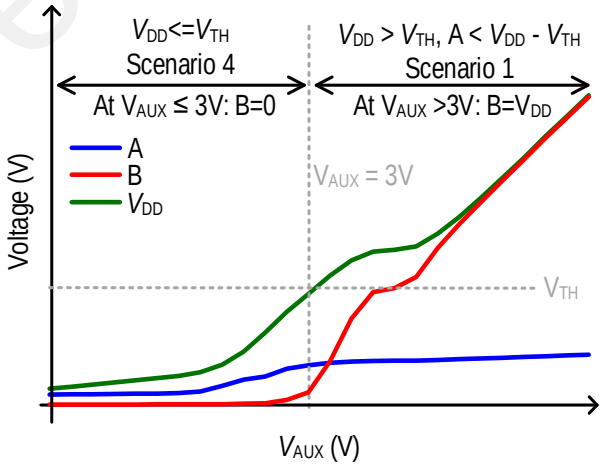

Figure 5.3: The Two-Operating Region of a CMOS Inverter Voltage Sensing Unit (Scenario 1 and 4) with Voltage Divider Paths Detecting a Target Voltage of 3 V.

The design of a voltage sensing circuit capable of detecting voltage at any specified target level entails the incorporation of two voltage divider paths and a CMOS inverter. However, this voltage-sensing topology faces two challenges. Firstly, the voltage output from the CMOS inverter may not be sufficiently high to drive transmission gates or support control logic operations, as V_{DD} undergoes attenuation by VDP2. Secondly, the circuit's output exhibits excessive hysteresis, making it unsuitable for use as a voltage detector.

2) Inverter Chain

To address the previously mentioned issues, an inverter chain consisting of multiple cascading inverters can be employed. Each inverter within this chain receives power from a distinct voltage source, whereby each subsequent inverter has a voltage level incrementally higher than its predecessor. This is achieved by incorporating current-limiting transistors with varying widths for each inverter in the chain. As depicted in Figure 5.4 (a), transistors ML3, ML5, ML6, and ML7, with widths of 0.24 µm, 0.6 µm, 7.2 µm, and 8.4 µm, are responsible for providing voltages V_{DD}, V_{DD1}, V_{DD2}, and V_{DD3}, respectively.

Figure 5.4 (b) illustrates the output voltage graph of inverter 1, where the hysteresis of the graph can be described by the equation: $B = -m(A) + V_{TH}$, with m representing the gradient of the hysteresis. Since the second inverter takes the output of the first inverter as its input, its hysteresis graph can be expressed as $C = m^2A - mV_{TH} + V_{TH}$. Similarly, signal *C* serves as the input for the third inverter, producing an output of signal *D*, which becomes the input of the fourth inverter. The expressions for *D* and *E* are as follows: $D = -m^3A + m^2V_{TH} - mV_{TH} + V_{TH}$ and $E = m^4A - m^3V_{TH} + m^2V_{TH} - mV_{TH} + V_{TH}$.

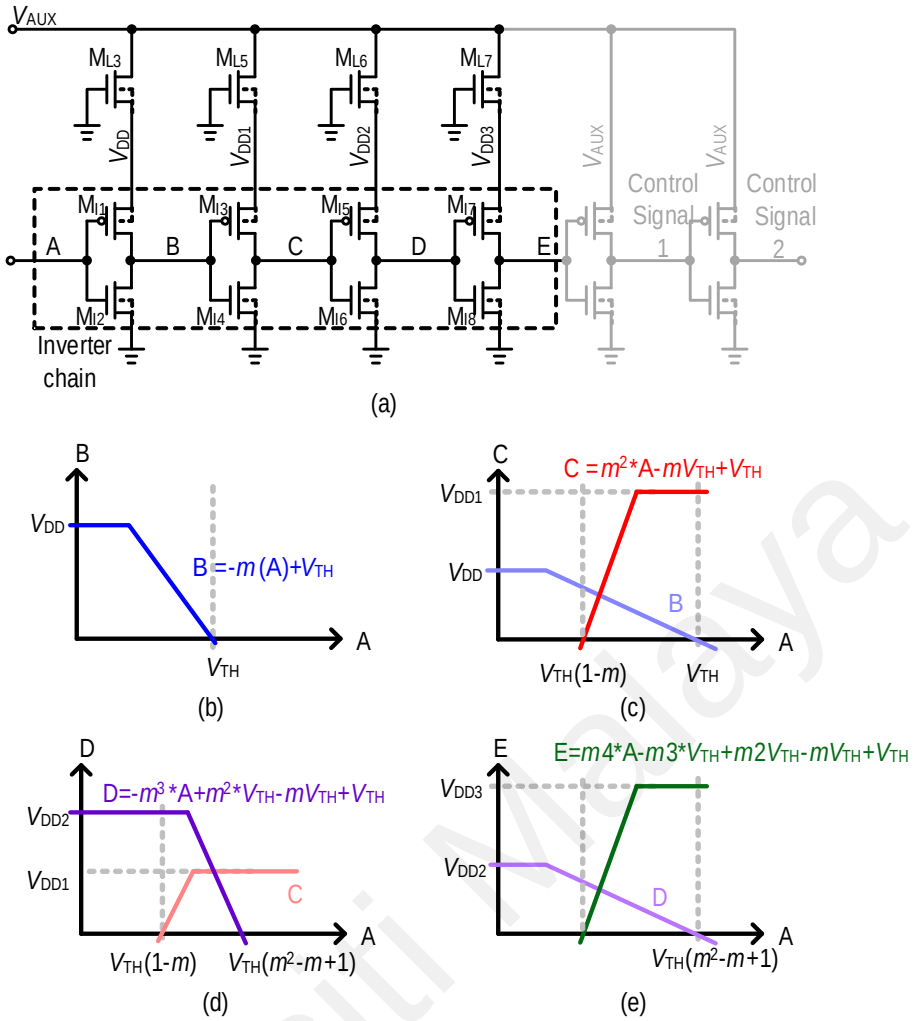

Figure 5.4: Inverter Chain's (a) Schematic Diagram and the Output Hysteresis of (b) First Inverter (c) Second Inverter (d) Third Inverter (e) Fourth Inverter

The equations reveal that the gradient increases by a factor of m with each inverter, resulting in a reduction in hysteresis for each successive inverter within the chain. Furthermore, the gradual increase in V_{DD} for each inverter in the chain allows the final output voltage to surpass that of its predecessors, providing a higher voltage control signal for the output voltage-limiting function.

3) Low Power Voltage Sensing Circuit

In order to minimize power consumption in the voltage sensing circuit, a gate-ground transistor is incorporated into each stage of the inverter as a current regulator. This gate-

ground transistor is an NMOS transistor with its gate tied to the ground (Fassio et al., 2021), causing it to function in the subthreshold region. The drain current of an NMOS transistor in the subthreshold region can be expressed as in equation (5.1) and (5.2) (A. Ballo et al., 2020b),

$$\boldsymbol{I_{SUB} = I_0 \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nV_T}\left(1-e^{-\frac{V_{DS}}{V_T}}\right)}} \tag{5.1}$$

$$\boldsymbol{V_{TH} = V_{TH0} - \lambda_{DS} V_{DS} - \lambda_{BS} V_{BS}} \tag{5.2}$$

where I_0 represents a technology-specific constant, V_T stands for the thermal voltage (kT/q), $\frac{W}{L}$ denotes the transistor's aspect ratio, V_{DS} is the drain-to-source voltage, V_{GS} is the gate-to-source voltage,V_{BS}represents the bulk-to-source voltage, and V_{TH} corresponds to the threshold voltage. When the transistor experiences a negative gate-to-source voltage, its current is notably lower than that of a typical transistor's leakage current. As seen in equation (5.1), the presence of the negative exponential term in the drain current equation results in an extremely reduced current. The utilization of gate-ground transistors effectively decreases the current consumption of the voltage sensing circuit from the milliampere range to the microampere range.

In addition to the inverter chain, gate-ground transistors used as resistive components in the voltage divider path also serve as current limiters. This significantly reduces the overall current within the voltage divider path, resulting in decreased power consumption for the voltage divider path. As illustrated in Figure 5.5 (a), the proposed voltage sensing circuit exhibits minimal power consumption in the nano ampere range when the voltage source (V_{AUX}) falls below 1.5 V. It maintains a power consumption of under 1 µA. However, as the voltage source surpasses 3.5 V, power consumption increases exponentially and peaks at 23 µA at 4.3 V for input power levels ranging from -20 dBm to 5 dBm.

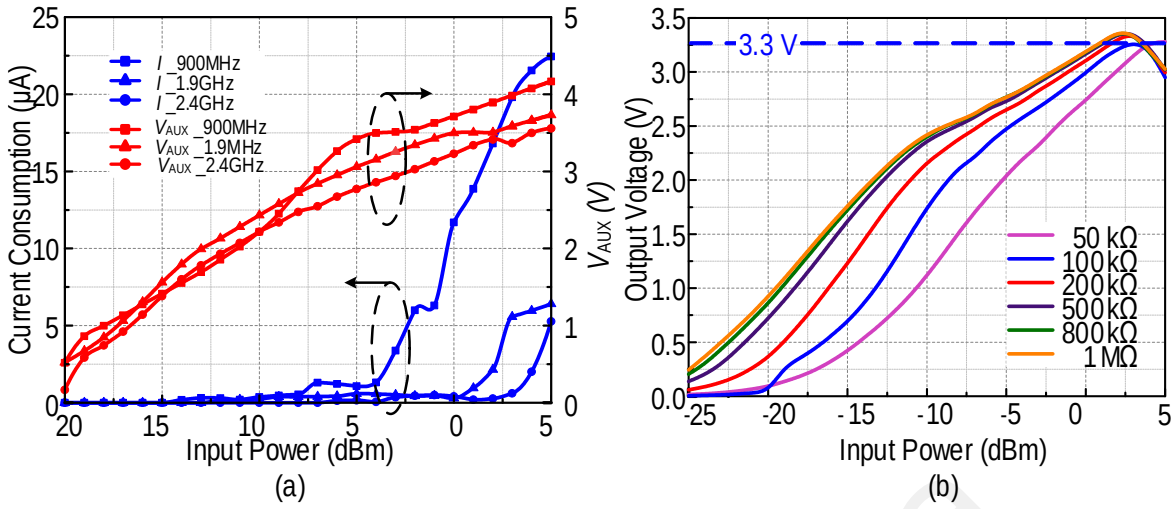

Figure 5.5: Graph of (a) Current Consumption of the Proposed Low Power Voltage Sensing Circuit under Different Voltages (b) Output Voltage of the Proposed Circuit under Various Load Conditions at 2.4 GHz

b) Output Voltage Limiter

The voltage limiter plays a critical role in safeguarding and maintaining the output voltage within the circuit's operational limits. This is especially vital in energy harvesting circuits, given the wide range of fluctuating voltages scavenged, which could otherwise lead to the failure of connected load devices. Typically, energy harvesting circuits for IoT sensors are regulated to maintain an output voltage of 3.3 V (Liu et al., 2016; Wong & Chen, 2019; Yang et al., 2020). This work implemented Switched Resistor Modulation (SRM) to ensure a bounded output voltage of 3.3 V. This technique is achieved by dynamically altering the on-resistance of power switches to adjust the equivalent output load resistance (Wong & Chen, 2019). This modulation is achieved by modifying the V_{GS} of the power switch, changing its ON/OFF periods (Lee & Mok, 2007), or adjusting the transistor's width (Jain et al., 2014). In SRM, a pass transistor acts as a variable resistor and is connected in series with the output load, as illustrated in Figure 5.6 (a). In this work, SRM is implemented by regulating the R_{ON} of the pass

transistor through precise control of its V_{GS}. This control allows for fine-tuning of the circuit's equivalent output resistance.

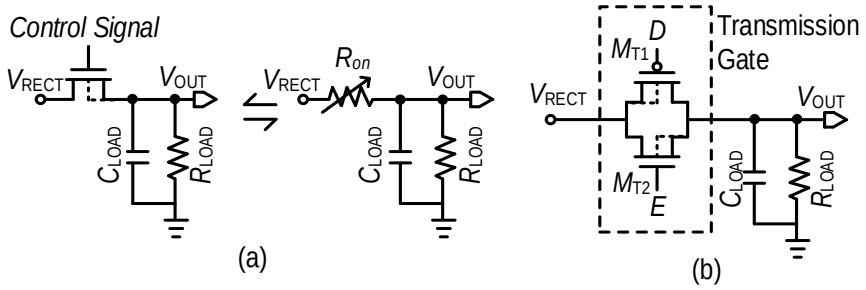

Figure 5.6: The Schematic of a Switch-Resistance Modulation Technique using (a) a Pass Transistor and its Equivalent Variable Resistor Model and (b) Transmission Gate.

In this work, an NMOS-PMOS transistor pair is configured as the pass transistor for SRM, as illustrated in Figure 5.6 (b). To control the V_{GS} of the PMOS and NMOS transistors within the transmission gate, two control signals, D and E, are employed. As shown in Figure 5.7, these control signals adapt as V_{AUX} varies to regulate the R_{ON} of the transmission gate, thereby constraining the output voltage to remain below 3.3 V. Specifically, when the P_{IN} is below -2 dBm (V_{AUX} =3.42 V), signal D is low while E is high, reducing the effective resistance of the transmission gate and allowing for a higher output voltage. Conversely, when the P_{IN} exceeds -2 dBm, signal D becomes high, while E goes low, thereby increasing the effective resistance of the transmission gate to ensure the output voltage remains below 3.3 V.

It is worth noting that the target voltage set at 3 V at the first inverter of the voltage sensing circuit. However, at the third and fourth inverters within the chain, this target voltage is adjusted to 3.42 V, as shown in Figure 5.7. This adjustment is a result of variations in transistor sizing within the inverter chain. Additionally, it's important to

mention that the transistor size within the transmission gate can be modified to set a different boundary voltage level if needed.

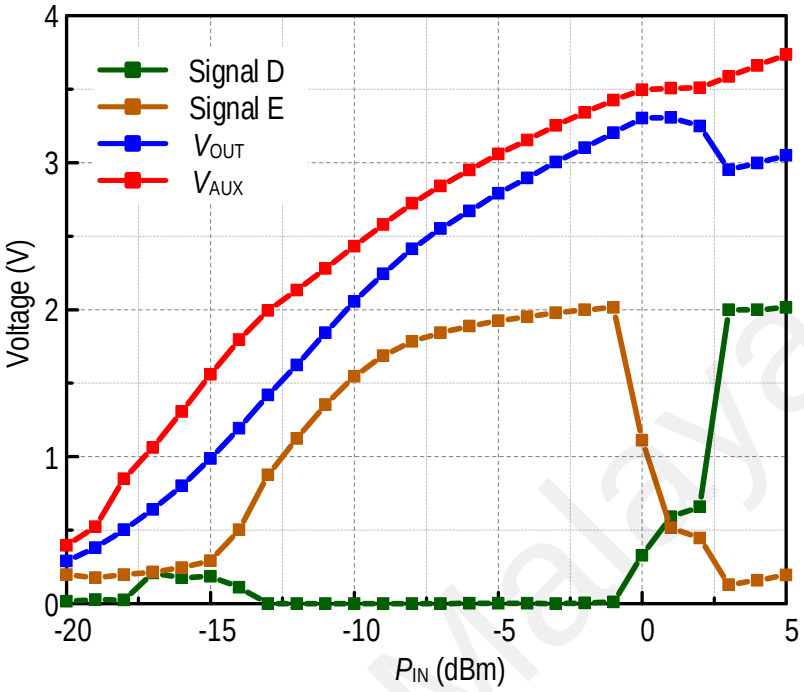

Figure 5.7: The Bounded Output Voltage of the Main Rectifier under 3.3 V by Control Signals D and E.

5.3 Experimental Result

The proposed tri-band RF energy harvesting system was designed and fabricated using 65-nm CMOS technology, as depicted in Figure 5.8. The chip has a compact footprint of 0.37mm2, with the IMN occupying majority of the area (0.24 mm^2) and rectifier and voltage monitor consuming the remaining area of 0.056 mm^2.

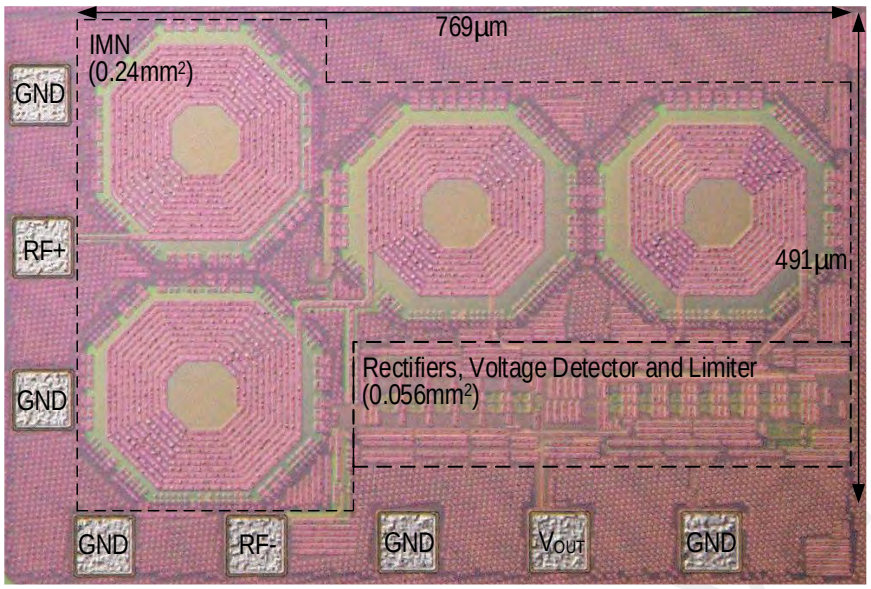

Figure 5.8: Chip Micrograph of Proposed Tri-band RFEH System

In Figure 5.9 (a), the transient output voltage of the proposed system is depicted at 1.9 GHz with a 100 kΩ load condition. At low P_{IN} levels (-20, -16, -12, -8, -4 dBm), the voltage limiter remains inactive, allowing for a gradual increase in output voltage until it reaches a steady state. Conversely, at higher P_{IN} levels (-2, 0, 2, 5 dBm), the transmission gate within the voltage monitoring unit becomes active and limits the output voltage to stay below 3.3 V, causing a decrease in output voltage before reaching a stable state. Figure 5.9 (b) illustrates the switching points of the voltage monitoring unit, which are 1 dBm, -3 dBm, and 4 dBm for 900 MHz, 1.9 GHz, and 2.4 GHz, respectively. The output voltage increases with increasing P_{IN} values until it reaches the respective switching point, after which it decreases as P_{IN} continues to rise. This mechanism effectively maintains the output voltage below 3.3 V for a wide range of P_{IN} levels, spanning from -25 dBm to 5 dBm.

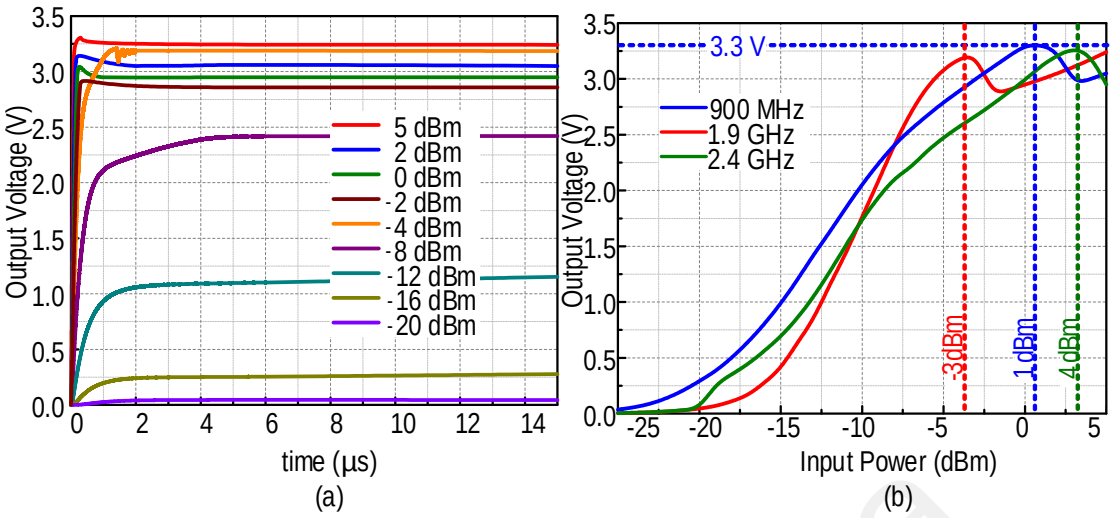

Figure 5.9: The Graph of (a) Transient Output Voltage Bounded below 3.3 V under Various Input Power at 100 kΩ, 1.9 GHz, and (b) Output Voltage vs Input Power Showing the Switching Point of the Voltage Monitor.

The proposed RFEH is later tested at three distinct frequency bands at 900 MHz, 1.9 GHz, and 2.4 GHz to showcase the performance of the RFEH system compromising the proposed voltage monitor. Its respective performance plot is presented in Figure 5.10. Figure 5.10 (a) illustrates the circuit's output power at a 100 kΩ load. The maximum output power attained for frequencies of 900 MHz, 1.9 GHz, and 2.4 GHz is 109.3 µW, 105 µW, and 107.3 µW, respectively. Contour plots in Figure 5.10 (b) to (d) display the relationship between input power and PCE at various load conditions for these frequencies. These plots reveal peak PCE values of 42.8 %, 37.1 %, and 30.4 % for 900 MHz, 1.9 GHz, and 2.4 GHz, respectively. Among the three frequencies, 900 MHz yields the highest PCE, followed by 1.9 GHz and 2.4 GHz. This hierarchy is attributed to increased switching losses in the rectifying transistors as the frequency rises, resulting in superior performance at 900 MHz. From the same figure, all three frequencies portrayed the same characteristics where there is a sweet spot of input power and output load to achieve the peak PCE. This is because the IMN is can only match the impedance at only

a certain range for the maximum power transfer and the input power determines the gate voltage of transistor which in turns affected the impedance of each transistor in the circuit.

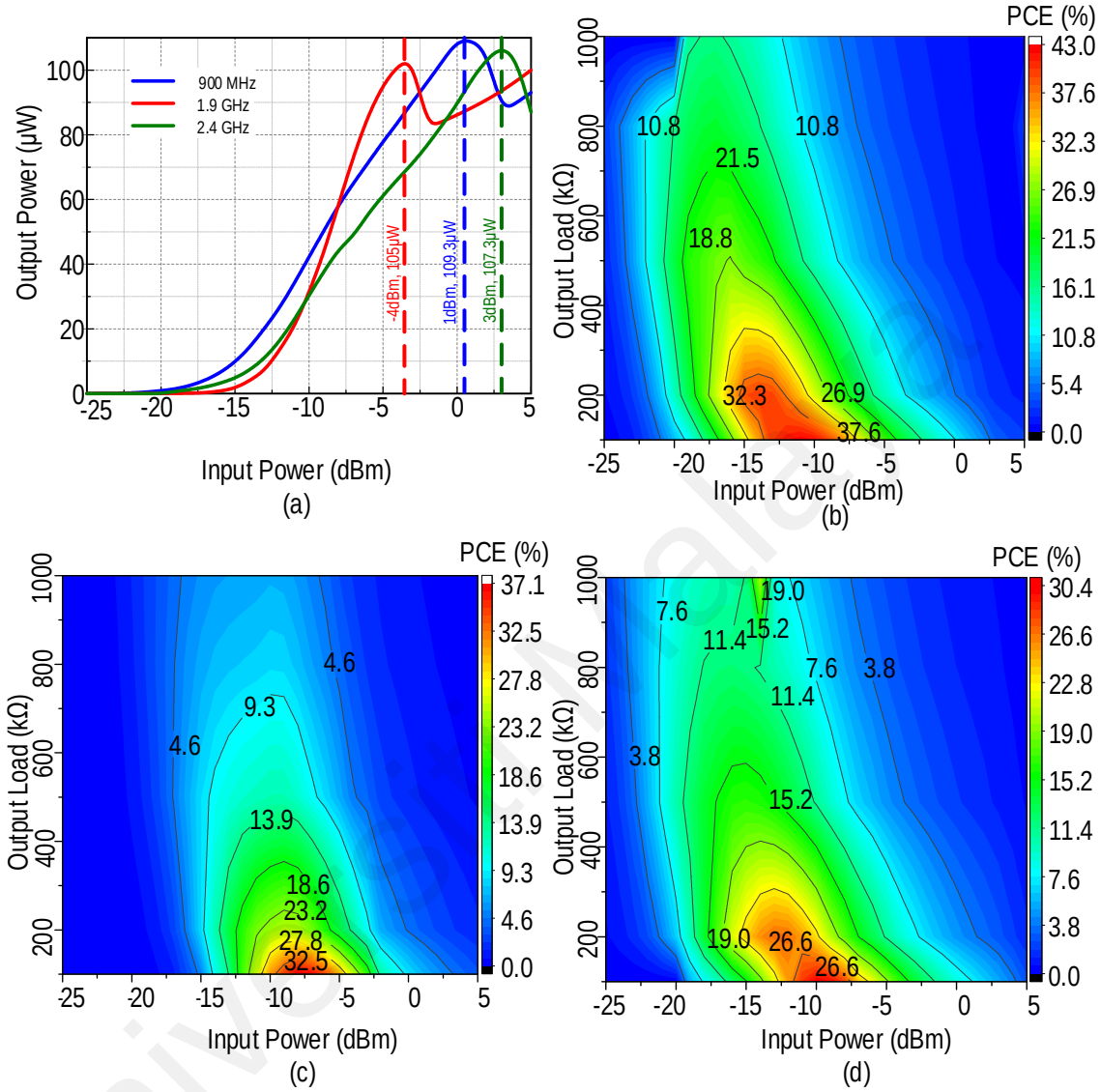

Figure 5.10: The Performance of Proposed RFEH System: (a) The Plot of P_{OUT} vs P_{IN} at 100 kΩ Load Condition and the Contour Plots of the Proposed RFEH System under Various Load Conditions and Input Power at (b) 900 MHz (c) 1.9 GHz and (d) 2.4 GHz

Table 5.2 presents the performance comparison with the existing output voltage controller works. Additionally, Table 5.3 records the performance summary of the

proposed fully integrated RFEH system and the comparison with the state-of-art multi-band RFEH works.

Table 5.2: Performance Comparison with the State-of-Art Output Voltage Controller

	This Work	**(Shih & Otis, 2011)**	**(Yang et al., 2020)**	**(Carreon-Bautista et al., 2016)**
Process (nm)	**65**	130	180	130
Controller	**Voltage sensing circuit + Voltage limiter**	Comparator + bandgap	bandgap + hysteresis control circuit + LDO	CMOS voltage reference circuit + LDO
Key technique	**Switch resistance modulation**	Resistance divider	Voltage divider	Resistance divider
Bounded output voltage (V)	**3.3**	1.4	3.3	1.8
Controller's Power Consumption	**< 0.021µW (@< 1.5V)**	1.158 µW (@450mV)	4.656 µW	10.148 µW

Table 5.3: Performance Comparison with the State-of-art RFEH System

Parameters	This work	(Li et al., 2017)	(Li et al., 2013)	(Abouzied et al., 2017)	(Papotto et al., 2011)	(Soltani & Yuan, 2010)
Technology (nm)	**65**	180+IPD	130	180	90	180
Frequency (GHz)	**0.9, 1.9, 2.4**	0.93, 2.36	0.9, 2.0	0.915	0.915	3.53
Peak PCE (%)	**42.8, 37.1, 30.4**	22.5, 23.3	9.1, 8.9	25	11.2[#]	<3[#]
Sensitivity at 1V (dBm)	**-20, -16, -19 (@800kΩ)**	-15.4, -15.4 (@500 kΩ)	-19.3[*], -19[**] (@1.5 MΩ, 1 MΩ)	-14.8(@1 MΩ)	-22.4 (No load)	-5 (1MΩ)
Rectifier Scheme	**Cross-couple differential drive**	Native NMOS Dickson	Dickson with Off-chip Biasing Network	Reconfigurable Dickson	Threshold Compensated Dickson	Dual half-wave rectifier
IMN	**Tri-Band On-Chip LC**	Dual-band IPD Band Pass/ Stop Filter	Two On-chip LC for Each Frequency (With Antenna Co-Design)	Single Band On-chip LC	Single Band On-Chip LL	Single Band On-chip LC
Bounded Output Voltage	**Yes**	Not bounded	Not bounded	Yes	Not bounded	Not bounded
Area (mm^2)	**0.37**	11.6	4	0.47	1.34	0.053[!]

5.4 Discussion

The experimental outcomes demonstrated the ability of the proposed voltage monitoring unit to uphold an output voltage boundary of 3.3 V with low power consumption. Additionally, the voltage limiter is tested with an RFEH system, showcasing its capability of generating usable DC power in the range of hundreds of micro-watts across three distinct frequency bands of 900 MHz, 1.9 GHz, and 2.4 GHz. This range of rectified power, coupled with the constrained output voltage suffices to serve as a dependable power source for IoT Wireless Sensor Network (WSN) applications.

In this study, the selection of a 3.3 V boundary voltage aligns with the prevalent voltage specification for IoT sensor applications in energy harvesting circuits. The novel voltage sensing circuit utilizes the CMOS inverter characteristics to detect any voltage level without requiring additional external supply. This allows the realization of truly wireless self-sustaining RFEH design. Besides that, the use of gate-ground transistors effectively limits the current consumption of the voltage sensing circuit, thus, greatly reducing the power consumed by the voltage monitoring unit.

Table 5.2 presents a performance comparison between this study and previous energy harvesting research. Notably, all the studies listed in Table 5.2 operate without an external power source. This work introduces a low-power voltage sensing circuit that achieves voltage detection with remarkable efficiency, consuming only $0.021\ \mu W$ at low voltage. This performance surpasses recent research efforts that rely on alternative reference circuits (Carreon-Bautista et al., 2016; Shih & Otis, 2011; Yang et al., 2020).

Additionally, this study incorporates a switch resistance modulation technique to limit the output voltage, eliminating the need for a large resistive component.

Table 5.3 provides a performance comparison between the proposed system and existing multiband RFEH systems. Unlike current on-chip multiband RFEH systems, the proposed system incorporates a tri-band on-chip IMN, enhancing its practicality by enabling energy harvesting from a broader spectrum of frequency bands. This versatility ensures continuous energy harvesting even when one or two desired frequencies are unavailable due to geographical variations. In this study, the proposed system achieves outstanding performance, surpassing recent works with a PCE exceeding 30 % across all three frequencies. This achievement can be attributed to a comprehensive assessment of the on-chip L-network, particularly the evaluation of losses associated with the IMN's inductor and the minimum power loss from the output voltage limiter.

5.5 Summary

A novel low power voltage monitoring unit capable of limiting a boundary output voltage of 3.3 V is presented in this chapter. The voltage monitoring unit leverages the behaviour of CMOS inverter operation to achieve voltage detection and utilizes gate-ground transistors to ensure minimal power consumption of less than 0.021μW under 1.5 V input. Moreover, the voltage limiter in the voltage monitoring unit capitalizes the SRM technique to achieve the voltage limiting capabilities.

The voltage monitoring unit is incorporated into a fully integrated RFEH system and tested with three distinct frequency bands, ranging from input powers of -25dBm to 5dBm, catering to IoT WSN applications. The voltage monitoring unit allows the realization of a truly wireless self-sustaining RFEH design without any external voltage supply sources.

CHAPTER 6 : CONCLUSION

6.1 Conclusion

A comprehensive literature review on RFEH circuit blocks was undertaken, with particular emphasis on rectifier and charge pump blocks. The review extensively covers the conventional rectifier and CP architectures, evaluating their respective strengths, weaknesses, and the trade-offs involved in their circuit design. In the context of ultra-low-voltage subthreshold operation, the performance of rectifier and CP circuits is primarily influenced by forward conduction and reversion loss. These aspects present a trade-off, wherein improvements in one may affect the other. The DGB technique has shown promising results in mitigating both losses simultaneously. However, the conventional DGB technique still experiences some reverse leakage issues. Thus, this research aims to further improve on the current DGB technique and present a high-efficiency subthreshold operation CP circuit for WSN application.

Furthermore, the work explored the implications of a wide input power range on RFEH systems, including challenges such as inconsistent PCE across the input range, high oscillating frequencies causing increased switching losses, and the potential for overshooting the output voltage, which could damage the WSN load. To address these challenges, existing works proposed reconfigurable topologies and voltage monitoring units to adapt the input voltage changes for limiting the output voltage. Despite these efforts, there remains a research gap in the design of high-efficiency reconfigurable CP topologies and low-power voltage monitoring units tailored specifically for WSN RFEH applications.

This research has yielded three major significant contributions aligned with the research objectives. The first major contribution of this thesis is the development of a

high-efficiency subthreshold operation CMOS DC-DC converter for low input voltage energy harvesting applications. This is achieved with the novel advanced DGB technique in conjunction with the dual switch configuration to mitigate the reversion loss in the CP architecture, yielding a 43.4 % peak PCE at ultra-low input voltage. The second major contribution pertains to the development of a series-parallel reconfigurable charge pump with output voltage limiting capability across a broad input voltage spectrum of 0.26 V to 0.64 V. The proposed reconfigurable CP capitalizes on the low internal resistance inherent in parallel CP configurations to augment its performance while adaptively changing its stage configurations to achieve dynamic VCR for limiting a bounded output voltage. The proposed CP achieves a bounded output voltage with a wide input range of 0.26 V to 0.64 V with a peak PCE of 62 %.

The third contribution is the design and development of a novel dynamic source-fed oscillator that aims to achieve frequency modulation for reconfigurable CP. The novel oscillator features an independent source for the ring oscillator and the non-overlap clock generator, achieving frequency modulation without affecting the generated clock amplitude. The proposed dynamic source-fed oscillator achieved frequency modulation ranges of 4.3 MHz to 24 MHz with a wide input voltage range spanning from 0.26 V to 0.64 V.

The final contribution revolves around the development of a low power voltage monitoring unit. The voltage monitoring unit features a voltage sensing circuit to detect the input voltage and a voltage limiter to constrain a boundary voltage of 3.3 V for WSN application. The experiment result validates the effectiveness of the proposed circuit tested on a fully integrated RFEH system, achieving a PCE exceeding 30% across all three frequency bands: 900MHz, 1.9GHz, and 2.4GHz. Moreover, the voltage sensing circuit within the monitoring unit harnesses the operational principles of CMOS inverters

to enable voltage detection without the need for external voltage sources. The inclusion of gate-ground transistors further diminishes the power consumption of the voltage monitoring unit, registering a power consumption of less than 0.021μW under 1.5 V input. Finally, the voltage limiter adopts the SRM technique to effectively limit a bounded output voltage of 3.3V.

To fulfill the final research objective, the proposed circuit underwent comprehensive validation, fabrication, measurement, and characterization. The utilization of low-cost CMOS technology enables a monolithic system-on-chip solution well suited for WSN application.

6.2 Future Work

One significant area for future research is the implementation of the advanced DGB technique in rectifier circuits. The current research primarily focused on the design and improvement of charge pumps, leaving room to explore the potential benefits of applying the advanced DGB technique to rectifiers. Moreover, future work can also implement a self-powered ultra-low voltage CP mentioned in Chapter 3 to demonstrate its performance and characteristics when it is power by on-chip oscillator generated clock signals.

The second future work suggestion is the implementation of the advanced DGB technique in clock booster circuits. Clock booster circuits operate using charge storing and charge transferring principles, much like CPs. As a result, the same circuit improvement method that enhances CPs can be applied to clock boosters. Given that a clock booster circuit effectively boosts the clock signal, its performance can have a direct domino effect on each CP stage in the main CP circuit. Enhancing the clock booster circuit's performance could, therefore, contribute to the overall efficiency and reliability

of the entire energy harvesting system. It is worth noting that none of the current research has focused on optimizing the clock booster circuit, making it a promising avenue for future investigations.

Another future work suggestion is to improve the first stage of the advanced DGB. While DGB effectively operates by pulling a higher node voltage from the subsequent CP stage to optimize PMOS CTS performance during the reverse conduction phase and tapping a lower node voltage from the preceding CP stage to improve PMOS conductivity during the forward conduction phase, the current DGB technique encounters limitations in the first CP stage. The lack of available lower voltage from the first CP stage poses a challenge to the implementation of the DGB technique. While a negative CP could potentially provide the required negative voltage control, its considerable power consumption renders it unsuitable. Therefore, exploring methods to improve the DGB technique for the first CP stage represents a compelling area of future research. Addressing this challenge could pave the way for achieving even higher efficiency and performance in energy harvesting systems utilizing the advanced DGB technique.

The last future work suggestion is the integration of a complete RFEH system, encompassing a reconfigurable rectifier, an IMN, a CP, and the voltage monitor, into the scope of the research. The reconfigurable rectifier can be designed to adaptively adjust its configuration to achieve high PCE with a wide dynamic range, while the voltage monitoring unit can limit the output voltage. This comprehensive RFEH system will facilitate real-environment prototype testing, providing valuable insights into the system's practical performance and its suitability for its implementation in WSN applications.

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