

**DESIGN OF FAST START-UP HIGH-Q OSCILLATOR
FOR
WIRELESS SENSOR NODES TRANSCEIVER
FREQUENCY REFERENCE**

ABDOLRAOUF RAHMANI

**FACULTY OF ENGINEERING
UNIVERSITI MALAYA
KUALA LUMPUR**

2025

**DESIGN OF FAST START-UP HIGH-Q OSCILLATOR
FOR
WIRELESS SENSOR NODES TRANSCEIVER
FREQUENCY REFERENCE**

ABDOLRAOUF RAHMANI

**DISSERTATION SUBMITTED IN
FULFILMENT OF THE
REQUIREMENTS FOR THE DEGREE OF
MASTER OF ENGINEERING SCIENCE**

**FACULTY OF ENGINEERING
UNIVERSITI MALAYA
KUALA LUMPUR**

2025

UNIVERSITI MALAYA

ORIGINAL LITERARY WORK DECLARATION

Name of Candidate: **Abdolraouf Rahmani**

Matric No: **S2148321/1**

Name of Degree: **Master of Engineering Science**

Title of Project Paper/Research Report/Dissertation/Thesis ("this Work"): **DESIGN OF FAST START-UP HIGH-Q OSCILLATOR FOR WIRELESS SENSOR NODES TRANSCEIVER FREQUENCY REFERENCE**

Field of Study:

ELECTRONICS (NEC 520: ENGINEERING AND ENGINEERING TRADES)

I do solemnly and sincerely declare that:

- (1) I am the sole author/writer of this Work;
- (2) This Work is original;
- (3) Any use of any work in which copyright exists was done by way of fair dealing and for permitted purposes and any excerpt or extract from, or reference to or reproduction of any copyright work has been disclosed expressly and sufficiently and the title of the Work and its authorship have been acknowledged in this Work;
- (4) I do not have any actual knowledge nor do I ought reasonably to know that the making of this work constitutes an infringement of any copyright work;
- (5) I hereby assign all and every rights in the copyright to this Work to the Universiti Malaya ("UM"), who henceforth shall be owner of the copyright in this Work and that any reproduction or use in any form or by any means whatsoever is prohibited without the written consent of UM having been first had and obtained;
- (6) I am fully aware that if in the course of making this Work I have infringed any copyright whether intentionally or otherwise, I may be subject to legal action or any other action as may be determined by UM.

Candidate's Signature

Date: **17/08/24**

Subscribed and solemnly declared before,

Witness's Signature

Date: **17/08/24**

Name:

Designation:

DESIGN OF FAST START-UP HIGH-Q OSCILLATOR FOR WIRELESS SENSOR NODES TRANSCEIVER FREQUENCY REFERENCE

ABSTRACT

With the prevalence of wireless sensor networks and the Internet of Things (IoT), optimizing power in battery-powered wireless nodes is crucial due to the inconvenience and cost of replacing batteries in remote areas. Synchronized power modulation between "Sleep" and "Active" states, known as burst mode activation, allows nodes to conserve power. However, frequent transitions between these states consume significant energy, highlighting the need to reduce the start-up time of the slowest component, the high- Q crystal oscillator. Additionally, to ensure improved synchronization within the network and a cost-effective IoT device manufacturing, the device should be produced with low start-up time variations and without the need for post-manufacture trimming respectively. This report introduces Zero-phase Lock Injection, a novel method based on resonance lock chirp injection to reliably reduce start-up time. It features Zero-phase Cross Detection, a low-power, variation-tolerant resonance frequency detection technique. Unlike previous detectors, this method does not require the variation-prone voltage reference and utilizes low power digital circuits. Additionally, Zero-phase adaptive chirp is proposed to advance resonance lock chirp injection by allowing for motional current phase correction which increases variation tolerance of start-up time while further reducing the start-up time. Both techniques have demonstrated start-up times that are robust against voltage, and temperature and even process variations. Post-layout simulations with Cadence Virtuoso on a 38.4 MHz crystal resonator with 1.0 V supply and 65-nm CMOS process confirms the feasibility of Zero-phase lock and Zero-phase adaptive chirp to effectively reduce and achieve start-up times of 175 μ s and 170 μ s respectively. This is achieved with state-of-art minimal temperature variations of 3% and

3.8% respectively. The results demonstrate the promising potential of Zero-phase Lock and Zero-phase Adaptive Chirp as viable variation-tolerant techniques, enabling enhanced synchronization without the need for costly post-manufacture trimming.

Keywords: CMOS, Internet-of-Things (IoT), Crystal oscillator (XO), Start-up Time, Energy injection

Universiti Malaysia

REKABENTUK PERMULAAN PANTAS PENGAYUN Q TINGGI UNTUK RUJUKAN KEKERAPAN PENGURUS NOD PENDERIA WAIR

ABSTRAK

Dengan kelaziman rangkaian penderia tanpa wayar dan *Internet of Things (IoT)*, pengoptimuman kuasa dalam nod tanpa wayar berkuasa bateri adalah penting disebabkan oleh kesulitan dan kos menggantikan bateri di kawasan terpencil. Modulasi kuasa yang disegerakan antara keadaan "Tidur" dan "Aktif", yang dikenali sebagai pengaktifan mod pecah, membolehkan nod menjimatkan kuasa. Walau bagaimanapun, peralihan yang kerap antara keadaan ini menggunakan tenaga yang ketara, menonjolkan keperluan untuk mengurangkan masa permulaan komponen paling perlahan, pengayun kristal Q tinggi. Selain itu, untuk memastikan penyegerakan yang dipertingkatkan dalam rangkaian dan pembuatan peranti IoT yang kos efektif, peranti itu harus dihasilkan dengan variasi masa permulaan yang rendah dan tanpa memerlukan pemangkasan selepas pembuatan. Laporan ini memperkenalkan Suntikan Kunci Fasa Sifar, kaedah baru berdasarkan suntikan kicauan kunci resonans untuk mengurangkan masa permulaan dengan pasti. Ia menampilkan Pengesanan Silang Fasa Sifar, teknik pengesanan frekuensi resonans bertoleransi variasi kuasa rendah. Tidak seperti pengesanan sebelumnya, kaedah ini tidak memerlukan rujukan voltan terdedah kepada variasi dan menggunakan litar digital kuasa rendah. Selain itu, kicauan adaptif fasa sifar dicadangkan untuk memajukan suntikan kicauan kunci resonans dengan membenarkan pembetulan fasa arus pergerakan yang meningkatkan toleransi variasi masa permulaan sambil mengurangkan lagi masa permulaan. Kedua-dua teknik telah menunjukkan masa permulaan yang teguh terhadap variasi proses, voltan dan suhu. Simulasi pasca susun atur pada resonator kristal 38.4 MHz dengan bekalan 1.0 V dan proses CMOS 65-nm mengesahkan kebolehlaksanaan kunci fasa sifar dan kicauan penyesuaian fasa sifar untuk mengurangkan dan mencapai

masa permulaan 175 μ s dan 170 μ s secara berkesan masing-masing. Ini dicapai dengan variasi suhu minimum terkini masing-masing 3% dan 3.8%. Hasilnya menunjukkan potensi menjanjikan Kunci Fasa Sifar dan Kicauan Penyesuai Fasa Sifar sebagai teknik toleransi variasi yang berdaya maju, membolehkan penyegerakan yang dipertingkatkan tanpa memerlukan pemangkasan pasca pembuatan yang mahal.

Keywords: CMOS, Internet-of-Things (IoT), Crystal oscillator (XO), Masa Permulaan, Suntikan tenaga

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to several individuals whose support and guidance were instrumental in the completion of this thesis. First and foremost, I am profoundly thankful to Prof. Harikrishnan for his continuous mentoring and unwavering encouragement, pushing me to excel throughout this journey. My sincere appreciation goes to Dr. Ka-Meng Lei for his invaluable technical guidance, which has been crucial to the progress of my research. I would also like to extend my gratitude to Dr. Chee Cheow Lim for his technical support and assistance.

Special thanks go to all my Postgraduate peers at the Analog, Digital & RF Research group. Your strategies to overcome both personal and career challenges have been a source of inspiration and support. I am also grateful to the University of Malaya Faculty of Engineering office staff for their administrative support, which greatly facilitated my work.

Lastly, I want to extend my heartfelt thanks to my family for their unwavering love, patience, and encouragement. Your belief in me has been a constant source of strength throughout this journey. Thank you all for your contributions, support, and encouragement.

TABLE OF CONTENTS

Abstract	ii
Abstrak	iv
Acknowledgements	vi
Table of Contents	vii
List of Figures	x
List of Tables.....	xiii
List of Symbols and Abbreviations.....	xiv
List of Appendices	xvi
 CHAPTER 1: INTRODUCTION.....	 1
1.1 Motivation.....	1
1.2 Problem Definition and Research Questions.....	3
1.3 Objective and Report Organization	6
 CHAPTER 2: BACKGROUND AND LITERATURE REVIEW.....	 8
2.1 Sinusoidal Oscillators and Piezoelectric Crystal Resonator	8
2.2 The Slow Start-up Pierce Oscillator	12
2.3 XO Start-up Reduction Techniques.....	14
2.3.1 Constant Frequency Injection (CFI).....	15
2.3.2 Chirp-Injection (CI).....	17
2.3.3 Dithering Injection (DI).....	18
2.3.4 Feedback-Based Injection	18
2.4 Research Gap and Report Layout	23

CHAPTER 3: ANALYSIS AND DESIGN OF ZERO-PHASE LOCK AND ZERO-PHASE ADAPTIVE CHIRP.....24

3.1	Zero-Phase Lock (ZL) Injection	26
3.1.1	Zero-phase Resonance Frequency Detection Analysis	26
3.1.2	Zero-Phase Resonance Frequency Detection Macro-Model Implementation.....	30
3.1.3	Zero-Phase Lock Macro-Model Implementation	32
3.2	Zero-Phase Adaptive Chirp (ZAC) Injection	35
3.2.1	Zero-Phase Adaptive Chirp (ZAC) Injection Analysis	35
3.2.2	Zero-Phase Adaptive Chirp (ZAC) Macro-Model Implementation.....	37
3.3	Transistor Level ZAC and ZL XO Start-up Implementation	40
3.3.1	Implementation Workflow	41

CHAPTER 4: POST-LAYOUT SIMULATION RESULTS AND DISCUSSION .43

4.1	Determination of C_{L2} for ZAC and ZL	43
4.2	Determination of t_{NR} for ZAC and ZL based on Process Corners.....	46
4.3	Simulated Performance of ZAC and ZL Start-up Techniques	50
4.4	Discussion and Comparison to Other Proposed Works.....	53
4.5	Future Works	54

CHAPTER 5: CONCLUSION.....58

REFERENCES 61

LIST OF PUBLICATIONS AND PAPERS PRESENTED 70

APPENDIX 71

Appendix A: Derivation of (3.3).....	71
Appendix B: Verilog-A of Macro-model Blocks.....	72
VCO: Voltage Control Oscillator	72
Other Blocks	72
Appendix C: Curve Fitting of Figure 3.5(b) onto Equation (3.3)	73
Appendix D: D-FF's Metastability	79
Appendix E: Leakage Current Considerations in Voltage Sweep Gen. Circuit	81

LIST OF FIGURES

Figure 1.1: (a) Power profiles of two IoT nodes pre- and post- wake-up timer synchronization and (b) close-up of sleep, start-up and active modes indicating the importance of T_{start} reduction on E_{start} and consequentially node's overall power reduction.	2
Figure 1.2: Crystal Resonator (black) connected in Pierce oscillator (grey), negative resistance boosting start-up (red), and Injection start-up (blue).	3
Figure 2.1: Basic structure of a sinusoidal oscillator. A positive feedback loop is formed by an amplifier and a frequency selective network. V_{in} is the thermal noise that exists in all electronic circuits as white noise.....	8
Figure 2.2: Phase response of resonators with Q_1 (where $Q_1 > Q_2$) showing how higher quality factor resonators are desired for frequency generation because lower change in oscillation frequency, Δf_0 , is produced for a given phase perturbation, $\Delta \phi$	10
Figure 2.3: An illustration depicting the crystal resonator encased within its packaging, accompanied by the circuit symbol and equivalent model (<i>Piezoelectric Effect</i> , n.d.). .	11
Figure 2.4: Crystal resonator connected in Pierce oscillator configuration whereby a basic implementation of the amplifier is illustrated	12
Figure 2.5: Crystal resonator connected in Pierce oscillator (grey, ϕ_3), negative resistance boosting start-up (red, ϕ_2), and Injection start-up (blue, ϕ_1).	15
Figure 2.6: Crystal resonator's $i_{M,env}$ against time for different injection frequency mismatch, Δf . (Luo et al., 2022).....	16
Figure 3.1 Research workflow diagram to achieve the 3 objectives.....	25
Figure 3.2: (a) Frequency response of motional branch (Z_M) of crystal resonator, exhibiting both capacitive ($\Delta f < 0$) and inductive ($\Delta f > 0$) characteristics, and (b) the circuit used to derive the frequency response.	27
Figure 3.3: Block diagram of proposed zero-phase resonance detection highlighting the zero-phase-cross detection unit.	28
Figure 3.4: Resonance frequency difference between (3.3) and simulations for different C_{L2} values with and without ADL loading - where loading is from the transistor implemented Zero-phase cross detection block.	29
Figure 3.5: Evaluating the relationship between C_{L2} and f_{01} , where f_{01} represents the frequency at which phase rapidly shifts relative to its steady-state value, using: (a) phase	

against time for a 1.2MHz/ μ s down-chirp, (b) C_{L2} against $|f_{INJ}-f_0|$ at Phase=-30ps for different down-chirp rates. 31

Figure 3.6: Zero-Phase Lock XO start-up macro-model block diagram and timing diagram..... 32

Figure 3.7: Comparison of conceptual operation between Impedance lock and the proposed adaptive chirp (fixed peak-to-peak frequency toggling of 30,000 ppm around the resonance) in terms of frequency, phase and motional current envelop profiles. 36

Figure 3.8: Zero-Phase Adaptive Chirp XO start-up macro-model and its timing diagram. 37

Figure 3.9: Illustration of the phase and frequency correction properties demonstrated by the Zero-Phase Adaptive Chirp (ZAC) injection macro-model. (a) displays the frequency response of ZAC, (b) shows the phase response of the D-FF inputs, (c) presents the injection phase mismatch, and (d) depicts the motional current profile. 38

Figure 3.10: Transistor level implementation workflow with PEX verifications across PVT corners 42

Figure 4.1: Physical Layout of the XO-start-up systems 43

Figure 4.2: The $\theta_{DFF}(t)$ versus Δf for different (a) C_{L2} and (b) different delay line sizing at chirping rate of 2MHz/ μ s in the simulations for worst case delay drop. 44

Figure 4.3: Monte-Carlo simulated Δf (at D-FF trigger) given $C_{L2}=14$ pF, and 2x W_1/W_2 under 2 MHz/ μ s down chirp. 45

Figure 4.4: Frequency profile of the zero-phase adaptive chirp injection and the output from the D-FF 45

Figure 4.5: The growth of $|i_M|$ using ZAC and ZL. Based on shown results, we set t_{NR} 519 cycles and 70 cycles after the first zero-phase detection respectively. 46

Figure 4.6: Phase correction property exhibited by Zero-Phase Adaptive Chirp injection macro-model implementation. Signals i_M and V_{XO+} during (a) positive interference and (b) during negative interference; (c) gives the injection phase mismatch, and (d) is the motional current profile..... 47

Figure 4.7: Motional current growth of 38.4 MHz resonator without start-up (left), Zero-Phase lock (middle) and the Zero-phase adaptive chirp (right). 50

Figure 4.8: Simulated T_{start} , $|i_M(t_{NR})|$ and average frequency error against temperature variations. 51

Figure 4.9: Simulated T_{start} , $ i_M(t_{\text{NR}}) $ and average frequency error against voltage variations.	52
Figure 4.10: Simulated T_{start} , $ i_M(t_{\text{NR}}) $ and average frequency error against process corners.	52
Figure 4.11: A 90° phase shifter using D-FFs.....	56
Figure 4.12: ZAC with periodic 90° phase compensation to ensure continuous motional current growth despite the phase offset error by Zero-phase cross detection unit.	56
Figure 1D: Zoomed in image of Figure 4.2(b) near zero-phase cross. The pink highlighted box around Zero-phase cross is the metastable window with span of 32ps.	75
Figure 2D: Zoomed in image of Figure 2 for Adaptive chirp's frequency and phase response. The metastable window is illustrated in pink.....	76
Figure 1E: Zoomed in image of Figure 4.2(b) near zero-phase cross. This resonance detection unit, just like resonance detections in (Luo et al., 2022), has a significant error of -0.5MHz.....	78

LIST OF TABLES

Table 2.1: Tabulated comparison of XO start-up techniques (1/3).....	20
Table 3.1: Crystal resonator and injection parameters used for analysis	27
Table 3.2: Design Considerations developed using the implemented macro-model XO-start-up.....	33
Table 3.3: Zero-Phase Adaptive Chirp design considerations developed using the implemented macro-model XO-start-up	39
Table 4.1: Performance summary and comparison with prior arts.	53
Table 1C: Non-linear Curve fitting of macro-model simulation result from Figure. 3.5(b) with rate 10MHz/ μ s onto Equation (3.3). Highlighted in red are the relevant outputs. .	69
Table 2C: Non-linear Curve fitting of macro-model simulation result from Figure. 3.5(b) with rate 14MHz/ μ s onto Equation (3.3). Highlighted in red are the relevant outputs ..	71
Table 3C: Non-linear Curve fitting of macro-model simulation result from Figure. 3.5(b) with rate 18MHz/ μ s onto Equation (3.3). Highlighted in red are the relevant outputs ..	73

LIST OF SYMBOLS AND ABBREVIATIONS

IoT	:	Internet of Things
T_{start}	:	IoT node start-up time which is dominated by $T_{\text{XO-start}}$
E_{start}	:	Energy consumption during crystal oscillator start-up
$T_{\text{XO-start}}$:	Crystal Oscillator start-up time
Tx/Rx	:	Transceiver/Receiver
XO	:	Crystal Oscillator
Q	:	Quality factor of a resonator
PVT	:	Process, voltage and temperature
i_M	:	Motional current inside crystal resonator
APEC	:	Automatic phase error correction
f_0	:	Fundamental series resonance frequency of resonator
$R_{M,i} L_{M,i} C_{M,i}$:	Motional passive resistor, capacitor, and inductor, at branch i of crystal resonator
$Z_{M,i}$:	Motional impedance of branch i of crystal resonator
$i_M(0)$:	The motional current when core Pierce Oscillator amplifier is connected
R_N	:	Negative resistance seen by the motional branch of crystal resonator
C_L	:	Load Capacitance
CFI	:	Constant frequency injection
Δf	:	Frequency difference between injection frequency and resonance frequency ($\Delta f = f_{\text{INJ}} - f_0$)
T_{INJ}	:	Duration when crystal oscillator is under constant frequency injection
ϕ	:	Phase Error between motional current and injection signal ($\phi(t) = \angle i_M(t) - \angle V_{\text{INJ}}(t)$ or $\phi(t) = \angle i_M(t) - \angle V_{\text{XO+}}(t)$)
CI	:	Chirp injection – a signal whose frequency varies linearly with time
IGCI	:	Impedance Guided Chirp Injection

PEX	:	Post layout extraction/verification
ZL	:	Zero-Phase Lock
ZAC	:	Zero-Phase Adaptive Chirp
f_{01}	:	The series resonance frequency seen by buffer looking into resonator with the presence of C_{L2}
θ	:	Phase error between V_{XO-} and V_{XO+} ($\theta = (\angle V_{XO-} - \angle V_{XO+})$)
V_D	:	Voltage at D input of D-FF
V_{CLK}	:	Voltage at CLK input of D-FF
θ_{DFF}	:	Phase error between V_D and V_{CLK} ($\theta_{DFF} = (\angle V_D - \angle V_{CLK})$)
V_{ctrl}	:	Control voltage of VCO
VCO	:	Voltage Control Oscillator
A_p	:	Amplifier to sustain crystal oscillator oscillators
V_{XO}	:	Steady state voltage swing of crystal oscillator

LIST OF APPENDICES

Appendix A: Derivation of (3.3).....	71
Appendix B: Verilog-A of Macro-model Blocks.....	72
Appendix C: Curve Fitting of Figure 3.5(b) onto Equation (3.3)	73
Appendix D: D-FF's Metastability	79
Appendix E: Leakage Current Considerations in Voltage Sweep Gen. Circuit	81

CHAPTER 1: INTRODUCTION

1.1 Motivation

Amidst the prevalence of wireless sensor networks and Internet of Things (IoT), wireless nodes play a crucial role in gathering and transmitting data from remote locations. The technological facilitators for remote and extended wireless node operation are device miniaturization and ultra-low power nodes respectively. As a consequence of device miniaturization small sized batteries or energy harvesting power sources attributed with lower energy capacities are utilized. Hence, there is a continued scientific interest in power optimization (Rout & Ghosh, 2013).

The ongoing interest lies in average power reduction of wireless transceiver — the most power-hungry block which is constituted of low-noise amplifiers, phase-locked loops, and data converters. Literature has proposed synchronized power modulation of transceivers, alternating between "Sleep" and "Active" states to reduce average power. Such burst mode of activation allows nodes to conserve power in periods of inactivity, while being available to transmit and receive data when activated (Oller et al., 2016).

To facilitate burst mode of operation, wake-up timers (Loo et al., 2017) are used to trigger the bursts at predefined intervals while wake-up receivers (Rohde & Poddar, 2010) are event-based and are activated by wake-up signals. However, the burst mode technique puts the hardware into an inherent energy-consuming start-up mode with duration and energy costs of T_{start} and E_{start} respectively (Figure 1.1).

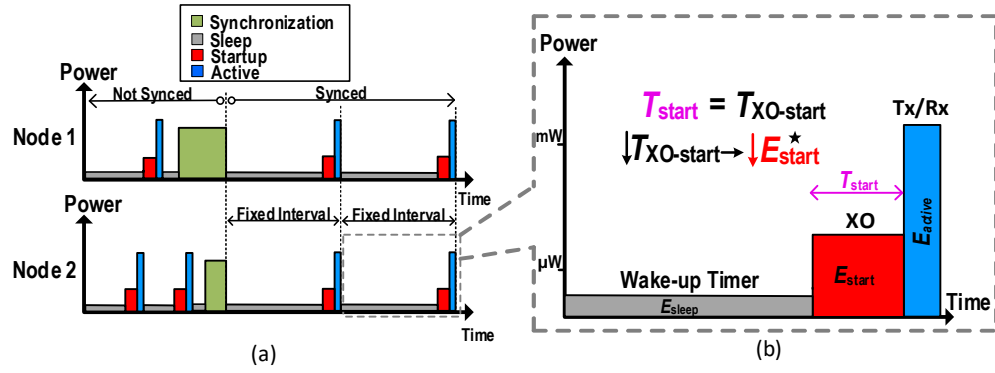


Figure 1.1: (a) Power profiles of two IoT nodes pre- and post-wake-up timer synchronization and (b) close-up of sleep, start-up and active modes indicating the importance of T_{start} reduction on E_{start} and consequentially node's overall power reduction.

As indicated in Figure 1.1 a significant reduction on power consumption of a duty cycling wireless node is achieved by reducing system start-up, T_{start} , which is dominated by start-up time of the High- Q MHz ranged crystal oscillator, $T_{XO-start}$. Furthermore, a reliable and consistent start-up time across devices, despite variations, would ensure that active states are aligned for longer periods without using the power-hungry synchronization method.

Lei et al (2018) demonstrates that this start-up loss accounts for a significant portion, approximately 42%, at each operational cycle of a transceiver at heavy duty cycling of 0.1%. Consequently, achieving additional power savings through heavy duty cycling necessitates a reduction in T_{start} via $T_{XO-start}$ reduction.

Overall, the reduction of power consumption in an IoT node can be significantly facilitated by the reliable reduction of crystal oscillator (XO) start-up time therein, this research project aims to reduce the start-up time consistently across process, voltage and temperature (PVT) variations for a 38.4MHz crystal resonator using a 65nm technology node.

1.2 Problem Definition and Research Questions

The start-up time of a crystal oscillator refers to the duration required to reach steady-state operation, which varies depending on the application. For instance, frequency synthesis for a transceiver may target a frequency stability of 20 ppm (Karimi-Bidhendi et al., 2019; Megawer et al., 2019) while duty cycling applications typically aim to achieve 90% of steady state's motional current (Esmaealzadeh & Pamarti, 2018). This research will henceforth use motional current, i_M , as metric for start-up. For a traditional XO in Pierce oscillator configuration (Figure 1.2) the motional current in the core of the quartz crystal (i_M) grows exponentially — provided that the amplifier can promote the growth of oscillation.

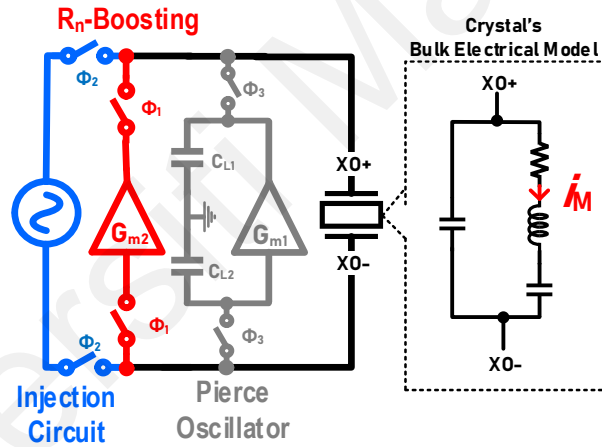


Figure 1.2: Crystal Resonator (black) connected in Pierce oscillator (grey), negative resistance boosting start-up (red), and Injection start-up (blue).

However, this growth is slow and results in long T_{start} , within milliseconds for a MHz crystal. Thereby literature has proposed R_n -boosting and energy injection start-up systems (Ding et al., 2019; Karimi-Bidhendi et al., 2019; Miyahara et al., 2018; Rusznyak, 1987). Figure 1.2 illustrates a crystal oscillator circuit with both these start-up techniques, where typical sequence of connection is injection unit, Φ_1 , R_n -boosting, Φ_2 , and then Pierce oscillator, Φ_3 . Current trend in literature is increasing i_M via injection techniques so that Pierce oscillator starts with higher initial motional current.

For an optimal injection, the injected frequency has to match the resonance frequency of crystal (Karimi-Bidhendi et al., 2019) and the injection phase must remain in-phase to i_M . Due to the high- Q of crystal oscillator, energy injection techniques focus on safeguarding the robustness of the phase and frequency of injected signal amid PVT variations (Cai et al., 2023; Griffith et al., 2016; Iguchi et al., 2016; H. Li et al., 2024; H. Li, Lei, Martins, et al., 2023; Luo et al., 2022; Megawer et al., 2019; Zhou et al., 2024). While techniques such as two-step injection (Megawer et al., 2019) offer strong frequency injection and hence start-up time tolerance against VT variations, compensating for the process variation necessitates costly post-fabrication calibrations, namely trimming¹ (Antonopoulos et al., 2019).

Chirp injection on the other hand guarantees the performance of the start-up by sweeping the injection frequency to cover the frequency deviation of the auxiliary oscillator due to voltage, temperature and even process variations. Therefore, chirp injection does not require specific calibration/trimming on the start-up circuit to guarantee the operation, thereby significantly reducing the manufacturing costs of the XO. The reduction in chip area, achieved by eliminating the need for trimming, along with the elimination of associated labor costs, leads to the savings.

A drawback of the typical PVT-tolerant chirp injection method, however, is the low energy injection efficiency since the power is spread to a wide frequency band, thereby the energy injected into the crystal core is low compared with constant frequency injection (Luo et al., 2022) or dithering (Karimi-Bidhendi et al., 2019). To this end (Luo et al., 2022) proposed a resonance locking technique where the chirping frequency is locked near crystal's resonance frequency. However, the proposed technique is power-hungry and remains susceptible to process variations, as the resonance detection circuit relies on

¹ Trimming in CMOS technology refers to the process of fine-tuning certain on-chip parameters, such as resistance or capacitance, to achieve desired electrical characteristics and improve performance.

a power-hungry comparator and a variation-prone voltage reference. Furthermore, since the frequency locked onto is not precisely the resonance frequency, any small frequency mismatch would cause additional variation in start-up time. Thereby, this research project (1) pursues the design of a PVT tolerant power efficient resonance detector without a voltage reference (2) a start-up system that provides variation tolerant start-up times without locking onto the exact resonance frequency.

In the pursuit of the aforementioned tasks, below research questions are to be answered:

How to detect resonance while chirping without a comparator referencing to a voltage reference?

In Luo et al (2022), with the aid of a comparator the injection unit is locked at a low crystal impedance magnitude, by referring to a voltage reference, and assumed to lock at resonance frequency. Alternatively, based on the frequency response of crystal resonator, the injection unit could lock at zero-phase impedance which doesn't require a voltage reference. This brings about the question, as to what behavior should be exploited to detect resonance, zero-phase or otherwise, and how to implement such detection circuit.

How to compensate for the imprecise frequency locked and further reduce start-up time variation?

The imprecise frequency locking in Impedance Guided Chirp Injection (Luo et al., 2022) results i_M to dampen after a growth duration whereby the extent of growth and damping for high- Q resonators is very sensitive to frequency mismatch. Karimi (2020) introduces a phase correcting technique whereby despite a frequency error, the motional current does not dampen and instead grows with small deviation against PVT. Thereby a similar phase correcting technique added to resonance locking could further excite the crystal and reduce start-up time variations across PVT.

1.3 Objective and Report Organization

Because of the problems listed above, three objectives have been developed for this research, namely:

- a) To formulate analysis that describe the characteristic of the proposed high-Q XO start-up technique towards start-up-time.

The start-up behavior of the proposed XO start-up systems will be analyzed using a dynamic differential equivalent model. This mathematical analysis involves formulating the mechanisms of the proposed system, facilitating systematic implementation. Additionally, the results from macro-model implementation of the systems are used to further verify this analysis.

- b) To design and implement a transistor-level XO start-up system based on low power resonance detection without a voltage reference.

Resonance locked injection is a promising PVT tolerant system, with the drawback of high-power detector referencing to a variation-tolerant voltage reference for detection. The Researcher aims to design and implement a XO start-up system with a low power resonance detector without a voltage reference. The proposed design is to be verified thorough extensive transistor-level² post-layout verification.

- c) To design and implement a transistor-level phase-error correcting XO start-up

As of writing this document, two phase error correcting techniques have been proposed, namely multi-phase injection (Karimi-Bidhendi & Heydari, 2020) and automatic-phase error correction (APEC) (Cai et al., 2023). However, neither can be implemented for the variation tolerant resonance locked based injection. Hence, a novel phase-error correction

² This report utilizes multiple implementations, ranging from macro-models to transistor-level schematics, and finally to transistor-level post-layout designs with parasitics, to extensively verify the proposed systems.

built upon resonance detecting start-up is pursued by the researcher and further verified with transistor-level post-layout results.

This report details researcher's findings into achieving the given objectives. Chapter 2 provides a literature review, with mathematical theories, into existing start-up solutions and narrows down into the research gaps that made up objectives two and three. In Chapter 3, Section 1 the Zero-phase Lock injection with the novel low power and reference-less Zero-phase Cross Detection unit is introduced to address objective two. Furthermore, in Section 2 the Zero-Phase Adaptive Chirp is proposed to address objective three. Lastly, Chapter 3 analyses the proposed techniques and verifies the analysis through mathematics and macro-model simulations thereby accomplishing objective one. Lastly, Chapter 3 discusses the transistor implementation work-flow for the proposed techniques. Whereby in chapter 4 the transistor level implemented results are discussed to show how the proposed techniques have accomplished objectives two and three. Finally, the report is concluded with its findings in chapter 5.

CHAPTER 2: BACKGROUND AND LITERATURE REVIEW

In pursuit of improving average power consumption of a wireless node via design of crystal oscillator (XO) with T_{start} (and hence E_{start}) reduction circuitry, we aim to comprehend fundamental concepts of existing solutions via fundamental studies. The studies will cover characterization of oscillators and quartz crystal as piezoelectric resonators. Following the studies on fundamental concepts, the conventional crystal oscillator in form of Pierce oscillator is analyzed and studied for its start-up time. Subsequently, existing start-up solutions are reviewed to identify the research scope—variation-tolerant fast start-up systems without trimming—and to further identify two research gaps within this scope.

2.1 Sinusoidal Oscillators and Piezoelectric Crystal Resonator

Oscillator circuits use a DC signal to generate a periodic signal. Such converter circuits use relaxation techniques to generate non-sinusoidal signals (e.g. square, sawtooth, and triangular signals) or frequency-selective network, also called resonator, to generate sinusoidal signals. XO are sinusoidal oscillators whose resonator is the piezoelectric crystal. Figure 2.1 shows the basic structure of such sinusoidal oscillators.

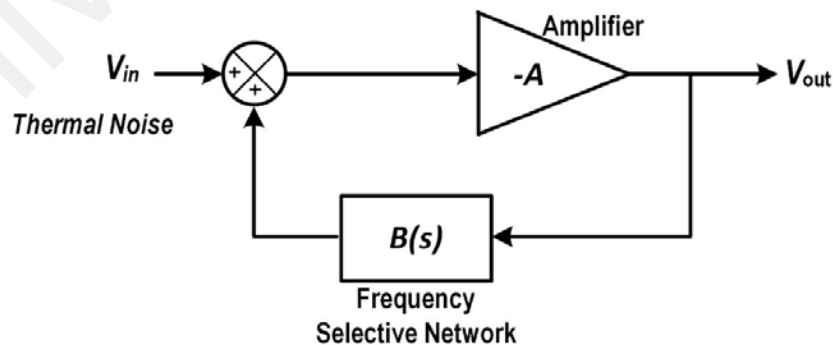


Figure 2.1: Basic structure of a sinusoidal oscillator. A positive feedback loop is formed by an amplifier and a frequency selective network. V_{in} is the thermal noise that exists in all electronic circuits as white noise.

The oscillator consists of an inverting amplifier with gain $-A$ ³ and resonator with gain $\beta(s)$ connected in a positive feedback-loop.

Using the basic structure, we derive for the closed loop gain, A_f , as:

$$A_f(s) = \frac{-A}{1 + \beta(s) \cdot A} \quad (2.1)$$

For this structure to exhibit as an oscillator, we need to consider a case whereby despite a zero-input signal, a value is produced at the output. This occurs when A_f is infinity, which requires the steady state⁴ loop gain product, $\beta(j\omega) \cdot A$, to be -1 (Sedra & Smith, 2015). This occurs when the steady state feedback selective network, $\beta(j\omega)$, is contributing 180° phase shift corresponding to a $\beta(j\omega)$ value with only negative real component. The frequencies at which resonators produce such real components are called resonance frequencies, f_0 . This real component requirement of loop gain is one part of the Barkhausen criterion for sustained oscillation. The second criterion to enable sustained oscillation is for A to compensate the losses of β at f_0 thereby producing an overall loop gain of -1 and enabling sustained oscillations.

To allow the circuit to produce a precise frequency with tolerance to change in phase (e.g. due to temperature (B. Kim et al., 2008) or noise (Leeson, 2016)), a sharp phase shift transition with respect to frequency, $\frac{d\phi}{df}$, would be desired as it would reduce change of resonance frequency, Δf_0 , for a given change of phase since $\Delta f_0 \approx \frac{\Delta\phi}{d\phi/df}$ (Sedra & Smith, 2015).

³ For practical cases amplifiers are also frequency dependent and they contribute to loop gain's phase response. In this section we reasonably assume a zero-phase gain as amplifiers tend to operate in lower frequencies.

⁴ A complete transfer function is expressed in $s = j\omega + \sigma$ while the steady state transfer function is considered when we use $s = j\omega$ (Nise, 2020)

The property corresponding to slope of phase transition through zero-phase or 180°-phase is the quality factor, Q , of the resonator.

Figure 2.2 illustrates how higher resonator quality factor, Q , corresponds to lower frequency change, Δf_0 , for a given phase change/noise, $\Delta\phi$ ⁵.

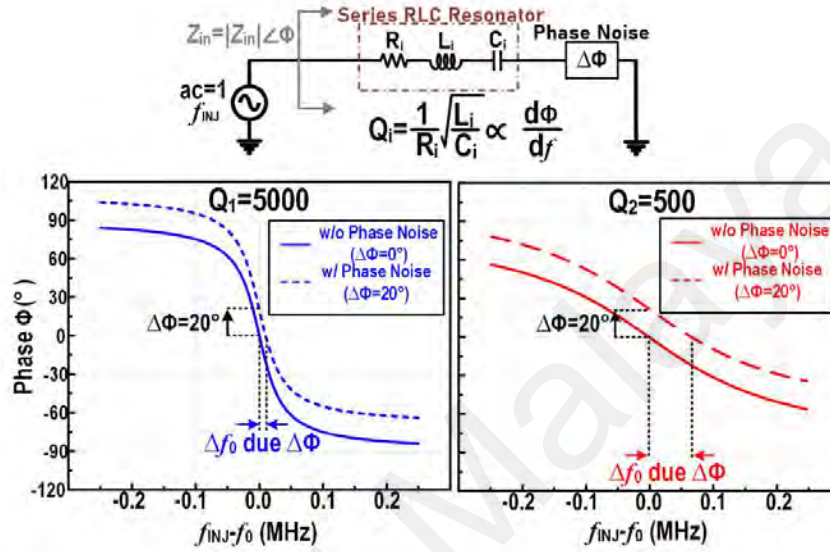


Figure 2.2: Phase response of resonators with Q_i (where $Q_1 > Q_2$) showing how higher quality factor resonators are desired for frequency generation because lower change in oscillation frequency, Δf_0 , is produced for a given phase perturbation, $\Delta\phi$.

Thereby a resonator with high quality factor is desired for a low noise frequency reference generation that is used in IoT transceivers.

Resonators can be designed from electrical components such as series or parallel RLC resonators. However, to produce a reasonable quality factor of 10^6 for a low noise reference generation, extremely large sized inductors would be required⁶. In turn, mechanical resonators are used. Furthermore, interfacing the mechanical resonator with

⁵ An alternative relationship between phase deviation/noise and quality factor Q is given by Leeson's phase noise equation (Leeson, 2016).

⁶ Since the inductance is proportional to inductor size and $Q = \frac{1}{R} \sqrt{L/C}$

the amplifying unit requires the mechanical resonator to have piezoelectrical property. An example of such piezoelectric resonators is ceramic or quartz crystals (Figure 2.3).

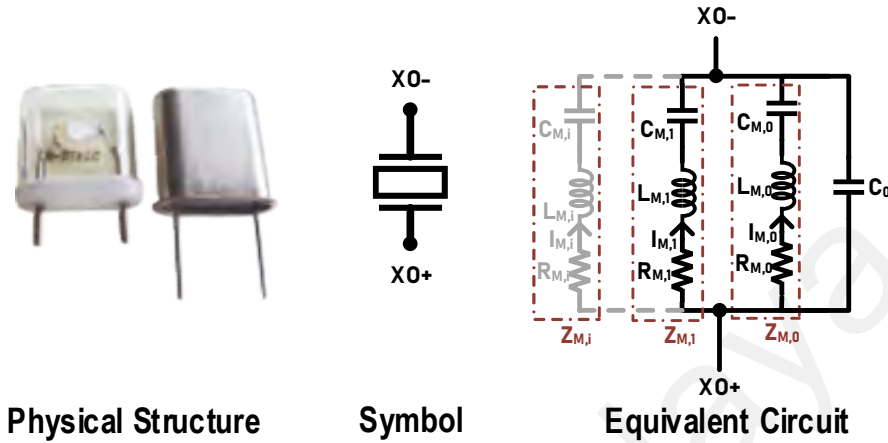


Figure 2.3: An illustration depicting the crystal resonator encased within its packaging, accompanied by the circuit symbol and equivalent model (*Piezoelectric Effect*, n.d.).

Mechanical resonators, unlike their electrical counterparts, exhibit multiple resonance frequencies corresponding to different modes of oscillation. Therefore, the electrical equivalent model of crystal resonators consists of multiple series $R_{M,i} \cdot L_{M,i} C_{M,i}$ branches each corresponding to a resonance frequency- see Figure 2.3.

Each possible mode of oscillation i of the resonator corresponds to a motional impedance $Z_{M,i}$ formed by the series resonant circuit $R_{M,i} L_{M,i} C_{M,i}$. Each branch or mode has an associated series resonance frequency $f_i (=1/2\pi\sqrt{L_{M,i}C_{M,i}})$. Once oscillation has taken place at one branch, the other branches can be ignored. Manufactured crystals such as (YXC, n.d.) cut the crystal so that a particular branch resonates more over the others. In the case where the “wanted” branch is the lowest resonance frequency, index i is 0, the series resonance frequency is referred to as the fundamental frequency, f_0 .

For this research, the conventional Pierce oscillator utilizing a high Q -crystal resonating at the fundamental frequency f_0 is studied for improvement of its start-up time

whereby the large $\frac{d\phi}{df}$ at f_0 is a mechanism utilized for our proposed resonance detector, Zero-Phase Cross Detection unit.

2.2 The Slow Start-up Pierce Oscillator

The most common XO arrangement is the Pierce oscillator (Figure 2.4).

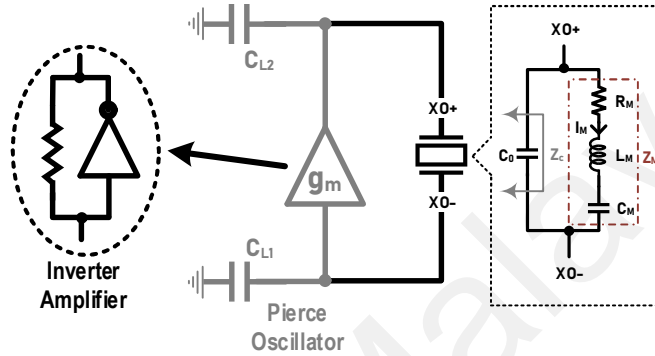


Figure 2.4: Crystal resonator connected in Pierce oscillator configuration whereby a basic implementation of the amplifier is illustrated

The lumped electrical model showing the fundamental motional branch for the crystal resonator is depicted in Figure 2.4, where R_M , C_M , and L_M represent the fundamental motional branch resistance, capacitance, and inductance of the crystal resonator, respectively, and C_0 represents the collection of electrical capacitances, and parasitic capacitance due to the package.

Pierce oscillator provides a great frequency stability (Bahai, 2016) attributed to improved quality factor in this configuration due quadratic contribution of large C_{L2} (Ohira, 2005):

$$Q_L \propto \omega_0^3 L_M C_{L2}^2 \quad (2.2)$$

where C_{L2} is the load capacitance at the output of the amplifier (see Figure 2.4).

The small-signal impedance, Z_c , that the motional branch of the crystal unit sees can provide insights into the properties and functionality of the XO. We may express Z_c

by considering a lossless condition (no loss in amplifier and capacitors) as (Lei et al., 2021):

$$Z_c = Re(Z_c) + Im(Z_c)j$$

$$Re(Z_c) = -\frac{g_m C_{L1} C_{L2}}{(g_m C_0)^2 + \omega^2 (C_{L1} C_{L2} + C_{L2} C_0 + C_0 C_{L1})^2}, \quad (2.3)$$

where the stable oscillation angular frequency is given as ω . The negative resistance, here denoted as $R_N \triangleq -Re(Z_c)$, is a crucial component of XO specially in regards to its start-up time, T_{start} .

T_{start} is made up of the addition of two variables: $T_{pre-energ}$, and T_{core} . $T_{pre-energ}$ is given as the amount of time the crystal is pre-energized before the core Pierce Oscillator is connected. On the other hand, T_{core} is the amount of time current grows until 90% of steady-state level by the core Pierce Oscillator. T_{start} is then mathematically expressed as (Rusznyak, 1987):

$$T_{start} = T_{pre-energ} + T_{core},$$

$$T_{core} = \frac{Q}{\pi f_0} \cdot \frac{1}{\alpha} \cdot \ln \left(\frac{0.9 i_M(t_{ss})}{i_M(0)} \right) \quad (2.4)$$

Where Q is the crystal resonator's quality factor, $i_M(0)$ is the motional current when core Pierce Oscillator amplifier is connected at time $T_{pre-energ}$, f_0 is the resonance frequency of crystal, $i_M(t_{ss})$ is steady state motional current and α is i_M growth factor given as (Rusznyak, 1987):

$$\alpha \approx \frac{|R_n| - R_m}{2L_m} \quad (2.5)$$

Analyzing (2.4) hints the following to reduce T_{start} :

- a) More R_N contributes to increase in α , thereby leading to decrease in T_{core} .
- b) Increasing $i_M(0)$ can reduce T_{core} .

Although T_{core} can be reduced by boosting α of Pierce Oscillator core, this is undesirable as it would increase oscillator phase noise resulting in the undesirable noise frequency generation (Iguchi et al., 2017). Therefore, recent start-up techniques focus on increasing $i_M(0)$.

2.3 XO Start-up Reduction Techniques

Literature presents two main categories of T_{start} and E_{start} minimization via T_{core} minimization: (1) energy injection and (2) R_N -boosting, which both increase $i_M(0)$ before sustaining amplifier starts its operation. Table 2.1 (page 20) compares the most relevant fast start-up techniques in literature.

As the name implies, R_N -boosting technique temporarily increases the negative resistance of the Pierce oscillator thereby increasing α and reducing T_{start} . This may be done via introduction of parallel gain stages (Iguchi et al., 2017) or reduction of C_L at start-up (Ding et al., 2019). Regardless of implementation, this technique suffers from low motional current increase at low i_M values due to i_M 's exponential relationship to R_N as given by (2.6) (Rusznyak, 1987).

$$i_M(t) \propto I_M(t = 0) \cdot e^{\alpha t} \quad (2.6)$$

Additionally, R_N -boosting techniques have matured, and no recent advances have been made. In contrary, there is an ongoing research interest into energy injection techniques as justified by 10 publications in last 2 years (Chen et al., 2023; Kruiskamp, 2022; Kundu et al., 2022; Lechevallier et al., 2021; Lei et al., 2021; H. Li, Lei, Mak, et al., 2023; Luo et al., 2022; Park et al., 2021; Wang et al., 2021; Zhang et al., 2022). Furthermore, as energy injection raises $i_M(0)$, it has the potential to achieve the theoretical minimum T_{start} via raising of $i_M(0)$ to $i_M(t_{\text{ss}})$. Hence, this project utilizes energy injection to reduce T_{start} and in conjugation E_{start} (since $E_{\text{start}} = P_{\text{startup}} \times T_{\text{start}}$ where P_{startup} is power loss at start-up).

In order to identify research gap, energy injection techniques are categorized and reviewed in the following sub-sections.

2.3.1 Constant Frequency Injection (CFI)

Constant Frequency injections (CFI) are simplest of energy injection techniques whereby a square wave with voltage V_{INJ} and frequency f_{INJ} is applied between the two crystal ports (Figure 2.5).

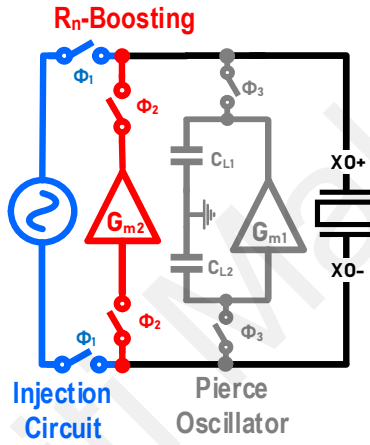


Figure 2.5: Crystal resonator connected in Pierce oscillator (grey, ϕ_3), negative resistance boosting start-up (red, ϕ_2), and Injection start-up (blue, ϕ_1).

Under such excitation and zero initial condition for a high Q crystal, i_M is expressed as (Karimi-Bidhendi et al., 2019):

$$i_M(t) \propto e^{-t} \sin(2\pi f_0 t) \times \left[\int_0^t e^x \cos(2\pi(f_0 - f_{INJ})x) dx \right] + e^{-t} \cos(2\pi f_0 t) \times \left[\int_0^t e^x \sin(2\pi(f_0 - f_{INJ})x) dx \right] \quad (2.7)$$

Under the ideal condition of zero resonance and injection frequency error, $\Delta f = (f_{INJ} - f_0)$, the maximum motional current growth occurs whereby

$$i_M(t) \approx i_{M,env}(t) \sin(2\pi f_0 t)$$

where $i_{M,env}(t)$ is the envelop of i_M and it is calculated to be

$$i_{M,env}(t) = \frac{2V_{DD}}{\pi R_M} \left(1 - e^{-\left(\frac{R_M}{2L_M}\right)t} \right). \quad (2.8)$$

To achieve theoretical minimum start-up under resonance frequency injection, the injection duration, T_{INJ} , is tuned so that i_M growth stops at steady state motional current $i_M(t_{ss})$. This is because any further i_M increase would require the motional current to drop to the steady state operation as per equation (2.4) (Esmaelzadeh & Pamarti, 2017).

Practically, the CFI approach faces two challenges: (1) to properly select T_{INJ} given PVT variations and (2) to ensure Δf is close to zero. Due to the inherent circuit variations from PVT, the creation of the injection signal with a frequency of f_0 — specially without calibration/trimming to compensate for process variation — is not possible. Therefore, any injection circuit will have a non-zero frequency error Δf . This results in a periodic damped driven oscillation behavior of motional current envelop, $i_{M,env}$, whereby $i_{M,env}$ periodically grows to a maximum value followed by subsequent damping. For V_{INJ} of 1 V, $i_{M,env}$'s rate of growth and its maximum is dependent on Δf as illustrated in Figure 2.6 (Luo et al., 2022).

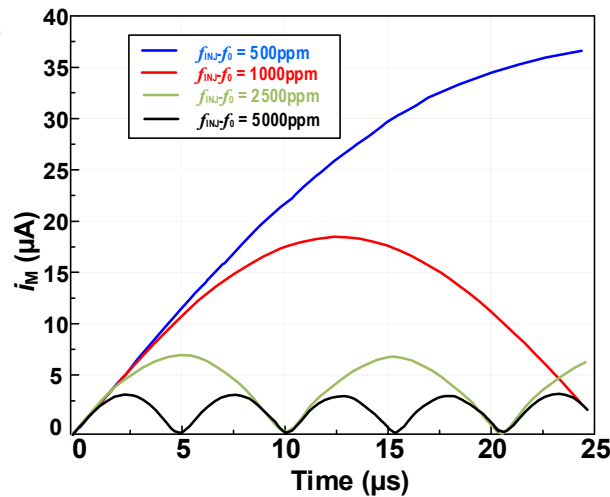


Figure 2.6: Crystal resonator's $i_{M,env}$ against time for different injection frequency mismatch, Δf . (Luo et al., 2022)

Karimi-Bidhendi et al (2020) has qualitatively explained the behavior as follows: at start of injection, the phase error, ϕ , between i_M and V_{INJ} is zero, thereby injection oscillator constructively builds up the motional current. However, due to Δf , the phase error accumulates and when ϕ reaches $\pi/2$, the injecting signal counteracting the crystal resonance, i.e., damping the oscillation⁷.

Furthermore as illustrated in Figure 2.6, $i_{M,env}$ varies significantly with Δf , presenting substantial challenges in designing for a reliable start-up time across variations.

All-in-all, CFI shows a promise for energy injection to fasten XO start-up, however non-calibration-based CFI techniques are constrained by the short comings of the inherent damped driven oscillation to reliably produce fast start-up.

2.3.2 Chirp-Injection (CI)

CI seeks to cover the frequency mismatch between the injection source and f_0 by injecting a chirping signal that sweeps through the resonance frequency (Iguchi et al., 2016; Lei et al., 2018; Luo et al., 2022). The chirping pulse's frequency varies linearly with time, and it is modeled as:

$$V_{INJ} = \sin \left(f_1 t + \frac{f_2 - f_1}{t_{INJ}} t^2 \right), \quad (2.9)$$

where the chirping pulse's beginning and ending frequencies are f_1 and f_2 , respectively.

CI guarantees the performance of the start-up by sweeping the injection frequency to cover the frequency deviation of the auxiliary oscillator due to PVT variation. It does not require specific trimming on the start-up circuit to guarantee the operation, thereby significantly reducing the manufacturing and operating costs of the XO. A drawback of

⁷ Note that the destructive interference starts when $|\phi| > \pi/2$ while the most destructive interference is at $|\phi| = \pi$.

the typical chirp injection method is low energy injection efficiency; since the power is spread to a wide frequency band, the energy injected into the crystal core is low compared with CFI (Luo et al., 2022).

2.3.3 Dithering Injection (DI)

Just as CI covers the frequency mismatch between the injection source and f_0 , a dithering signal provides injecting signal with band of frequency that consists of the resonance frequency. Unlike chirping where the injecting signal has a continuous linear change in frequency with time, dithering involves a signal that toggles between frequencies. For such injection technique the injection duration, injection frequency patterns, and the deviation of the frequencies from the resonance frequency determines the effectiveness of i_M excitation (Lei et al., 2021).

An excellent benefit of dithering is the possible enabling of phase correction and hence improved excitation given that the toggling occurs about the resonance frequency. However, designing a dithering injection circuit about resonance is not effective given large PVT variation of injection frequency band, thereby for an effective dithering designers make use of the costly post fabrication trimming/calibration (Karimi-Bidhendi et al., 2019).

2.3.4 Feedback-Based Injection

A high Q resonator such as crystal is a good frequency reference in and of itself, therefore its reaction to injection may be used as the input to a feedback loop to improve the injection source. Li et al (2023) and Megawer et al (2019) use a 2-step injection strategy, namely injection and frequency calibration of phase locked loop based injector, to calibrate the energy injector for minimal Δf . The initially injected signal is expected to be within 5000ppm of f_0 and this is not possible due to high process variations, thereby requiring calibration or trimming. On the other hand Luo et al (2022) utilizes CI with a

droop detection circuit to detect and lock at f_0 . This chirp injection with feedback allows for higher PVT tolerance. On the downside, the design of Luo et al (2022) suffers from high power consumption due to use of comparator and still requires tuning of voltage reference to effectively compensate for the process variation. An absolute voltage reference generation is especially difficult at lower technology nodes (M.-Y. Kim et al., 2012). At the same time the comparator implementation for lower technology nodes would be difficult due to low voltage, higher parasitic, higher noise and higher variations (Vertregt, 2006) for these nodes. Hence an alternative digital based resonance detection technique that doesn't use a voltage reference would improve the power and PVT performance of such feedback-based approach. Additionally, even with the use of such resonance locked injection, there is Δf due to imperfect locking⁸ and consequently damped driven oscillation as result of the accumulated phase error (Karimi-Bidhendi & Heydari, 2020).

⁸ Any practical circuit has errors in its operation, and this is also true for any resonance lock injection. Since crystal resonator excitation is very sensitive to Δf , even a slight mismatch of locked frequency would greatly reduce the growth rate and the maximum of i_M .

Table 2.1: Tabulated comparison of XO start-up techniques (1/3).

Technique	Ref.	Technique	Problem Addressed	Proposed Solution
R_N Boosting	(Rusznyak, 1987)	Conventional Pierce Osc.	The crystal is solely driven by a single self-biased inverter for start-up and sustained oscillation.	
	(Iguchi et al., 2017)	Stacked-Amplifier	R_N boosting with a single amplifier result in high power consumption	Reduced E_s for the same R_N is achieved with additional decoupled amplifiers in parallel to the core amplifier.
	(Miyahara et al., 2018)	Reconfigurable Multi-stage Amplifier	R_N is reduced at higher frequencies	R_N at higher oscillation frequency is boosted via addition of multiple voltage amplifiers with a feedforward frequency compensation
	(Ding et al., 2019)	Autonomous Dynamically Adjusted C_L	R_N is proportional to $1/C_L^2$ while required g_m to achieve this R_N is proportional to C_L^2 creating a tradeoff between E_s and T_{start} for a given C_L	By dynamically adjusting from a low to a high C_L as oscillator transitions from start-up to steady state operation, both low E_s and T_{start} is achieved.
	(Karimi-Bidhendi et al., 2019)	Active Inductance	C_0 is a limiting factor in maximum R_N achieved	The effect of C_0 is reduced via active inductor which increases maximum R_N and hence reduce T_{start}

Table 2.1 Continued: Tabulated comparison of XO start-up techniques (2/3).

Technique	Ref	Technique	Problem addressed	Proposed Solution
Energy injection (1/2)	(Iguchi et al., 2016)	Chirp Injection	The energy injections are PVT intolerant and such T_{start} reduction requires costly calibration/trimming to make f_{INJ} close to f_0 .	Designed a no trimmed PVT tolerant injection by sweeping frequency, chirping, from $f_{INJ} > f_0$ to $f_{INJ} < f_0$ across all PVT corners to reduce T_{start} and E_s
	(Esmaealzadeh & Pamarti, 2018)	Precisely Time Injection	Energy injection under or beyond optimum T_{INJ} increases T_{start}	Systematic design of precisely timed injector was designed to reduce T_{start}
	(Lei et al., 2018)	Self-Reference Chirp Injection	(Iguchi et al., 2016) uses an area hungry RC voltage sweep to chirp VCO's frequency	VCO's frequency is chirped via digitally controlling the ring osc.'s cap-banks whereby its control is referenced on the number of cycles produced by the VCO itself. This digital approach reduced chip area.
	(Verhoef et al., 2019)	Synchronized Signal Injection	With Δf damped sinusoidal oscillation occurs due to ϕ accumulation.	Start-up system involves injection of signal that is periodically synchronized for $\phi=0$ after a preset drive delay producing a linear $ i_M $ growth.
	(Griffith et al., 2016)	Dithering Signal Injection	There is an stringent Δf requirement for reliable T_{start} across temperature and voltage variations	By toggling f_{INJ} above and below f_0 , temperature and voltage variations are compensated thereby producing more reliable T_{start} across these variations.
	(Lechevallier et al., 2019)	Self-Timed Injection	All injection techniques make use of the power hungry VCO to produce f_{INJ}	By detecting the zero crossings of i_M a signal with very low Δf and in phase is produced and injected thereby reducing E_s and T_{start} without a VCO.

Table 2.1 Continued: Tabulated comparison of XO start-up techniques (3/3).

Technique	Ref	Technique	Problem addressed	Proposed Solution
Energy injection (2/2)	(Megawer et al., 2019)	Two-step injection	Constant frequency, dithered, and chirp injection cannot provide a precise f_{INJ} thereby not achieving close to minimum theoretical T_{start}	A precise f_{INJ} is produced by self-calibration of VCO using a DPLL after an initial energy excitation.
	(Karimi-Bidhendi & Heydari, 2020)	Multi-phase injection	Synchronized signal injection used manual adjusting of delay between phase correction stages	The phase accumulation is rigorously studied to evaluate the appropriate delay between phase correction stages at the simulation level.
	(Lechevallier et al., 2021)	Stepwise charging	A portion of E_s is lost to charging and discharging of capacitors such as C_L	Instead of charging the caps until rail-to-rail voltage, they are charged in N small steps thereby saving E_s by N times.
	(Luo et al., 2022)	Impedance Guided Chirp Injection	While chirp injection effectively excites crystal across PVT, its power is wasted due to the spread across a wide frequency	f_{INJ} is detected and locked near resonance frequency by droop detector, made up of envelop detector, comparator and FSM, thereby improving effective injection.
	(Cai et al., 2023)	Automatic Phase Error Correction	Multi-phase and synchronized signal phase corrections use a preset delay and require a low Δf for effective injection	Proposed system automatically corrects ϕ despite a large Δf to achieve a low T_{start}
	(H. Li, Lei, Mak, et al., 2023)	Binary-Search-Assisted Two-Step Injection	Due to use of DPLL, two-step injection requires first f_{INJ} to have stringent requirement of $\Delta f < 5000\text{ppm}$	Utilizing assistance from binary-search algorithm the frequency calibration of PLL is done across a larger Δf of $< 10,000$ while also reducing PLL's locking time.

2.4 Research Gap and Report Layout

To address the variation tolerant and power consuming resonance detection as well as the phase error accumulation, this research project proposed two PVT tolerant CI based fast start-up systems with lower frequency spread to improve XO start-up without calibration or trimming. The first design is dubbed Zero-Phase Lock and it is a resonance lock injection based on impedance guided chirp injection (Luo et al., 2022) with an enhancement of low power digital resonance detector without any variation-prone voltage reference. The second design, dubbed as Zero-Phase Adaptive Chirp, enhances the first by dynamically correcting the phase of the injection source through the detection of the phase difference between the injection source and i_M . Both systems make use of the novel Zero-Phase Cross Detecting unit to enable their core functionally, namely resonance detection and phase error correction. The designs are validated with post layout simulation results in the CMOS 65-nm process.

The report is outlined to accomplish objective one in the 3rd Chapter and objectives two and three in the 4th Chapter. By analysing the proposed fast XO start-ups via steady state mathematical analysis along with the transient macro-model simulations, Chapter 3 accomplishes objective one. Furthermore, the systematic methodology to design the proposed techniques is highlighted. For a complete verification of the proposed techniques and thereby accomplishment of objectives two and three, Chapter 4 discusses the transistor-level post-layout results. Finally, the report is concluded in chapter 5.

CHAPTER 3: ANALYSIS AND DESIGN OF ZERO-PHASE LOCK AND ZERO-PHASE ADAPTIVE CHIRP

Crystal resonator is remarkable to offer an exceptionally high Q for excellent spectral purity. Yet, a drawback to this high Q is its slow start-up behaviour. For a fast start-up solution using energy injection, a stringent requirement on the frequency mismatch between the resonance and injection frequency for a robust i_M growth is necessary (Lei et al., 2021). In light of this, PVT-tolerant energy injection techniques such as chirp injection are attractive as they allow the auxiliary injection circuit to inject energy at resonance frequency amid PVT variation without any trimming thereby reducing costs. Yet, as the injection energy is distributed to a wide frequency band, the energy delivered to the crystal is limited thereby the XO needs additional time to reach the steady state after the injection. Alternatively, resonance searching techniques such as impedance-guided chirp injection, IGCI (Luo et al., 2022), has been proposed to lock the injection frequency near the resonance frequency by use of a droop detector, which is compromised of power-hungry comparator and a variation-prone voltage reference. Based on impedance-guided injection (Luo et al., 2022), we propose the zero-phase resonance lock injection which utilises power efficient digital blocks and doesn't use the variation-prone voltage reference. Furthermore, to introduce phase correction to locked injection techniques, adaptive chirp is proposed. Figure 3.1 illustrates the research workflow to achieve the three objectives.

This chapter will discuss the working principles of the proposed techniques, Zero-Phase Lock (ZL) and Zero-phase Adaptive Chirp (ZAC). The hypothesized steady state working principles will be validated through macro-model simulation, and successful correspondence will mark the completion of objective 1. Additionally, this simulation will establish the design considerations and specifications for the transistor-level implementation.

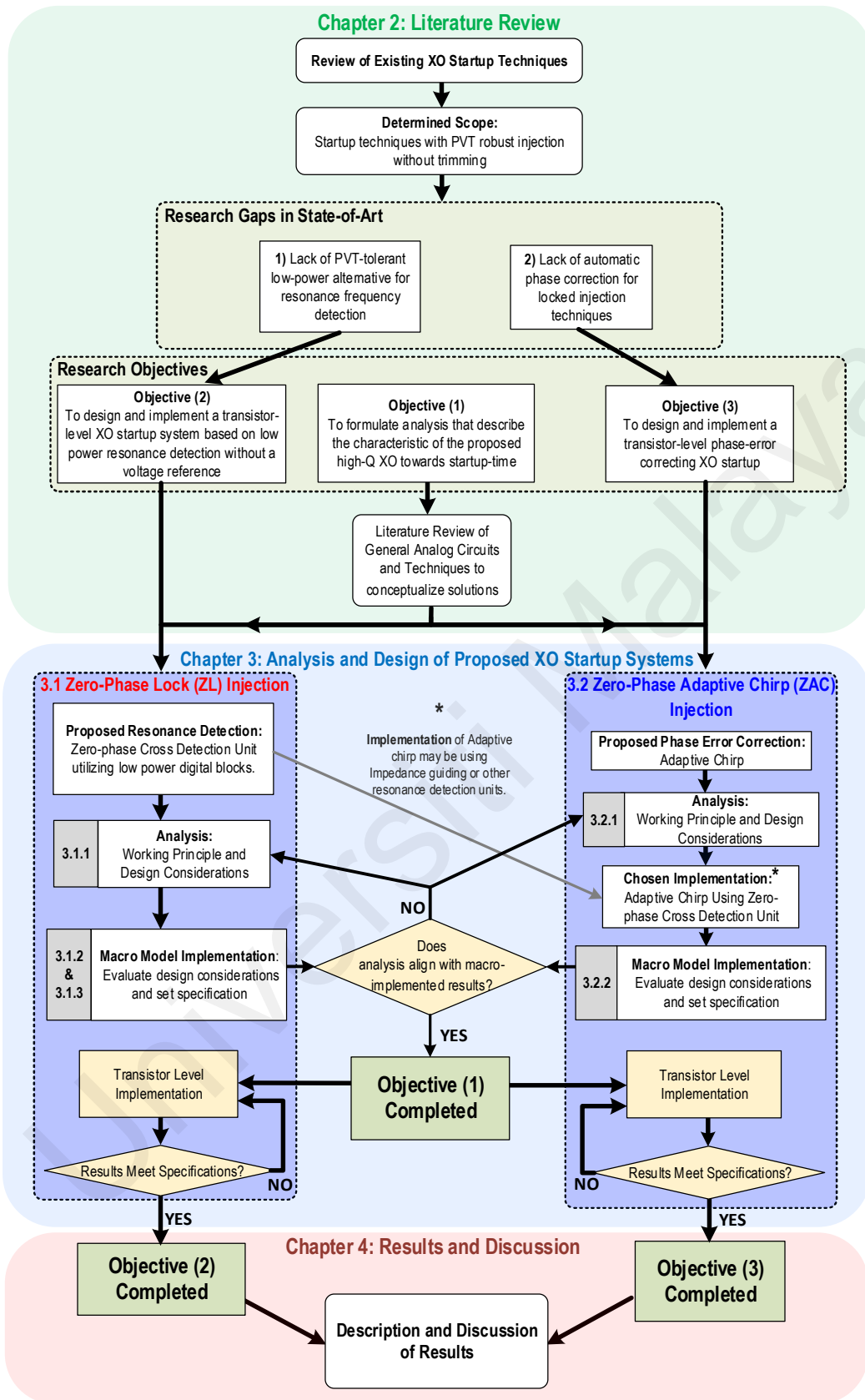


Figure 3.1 Research workflow diagram to achieve the 3 objectives.

3.1 Zero-Phase Lock (ZL) Injection

The proposed resonance lock injection start-up technique utilizes the novel approach of resonance detection using the zero-phase cross by the Zero-Phase Cross Detection unit.

We will analyse this resonance detector block using quantitative steady state analysis in subsection 3.1.1, after which the analysis is validated via macro-model implementation of Zero-phase Cross detection in subsection 3.1.2. Building upon the resonance detector by adding the control logic blocks, the macro-model of Zero-phase Lock (ZL) injection is further built to set the design consideration and specifications for the transistor level implementation in subsection 3.1.3.

3.1.1 Zero-phase Resonance Frequency Detection Analysis

Resonance detection techniques such as IGCI (Luo et al., 2022), utilize the motional impedance characteristic of crystal resonator at series resonance frequency. The series resonance frequency of a quartz resonator is characterized by the frequency with minimum resistance and zero reactance.

Using the equivalent quartz crystal model with fundamental motional components (as illustrated in Figure 2.4), the motional impedance of the resonator is:

$$Z_M(s) = R_M + sL_M + \frac{1}{sC_M}. \quad (3.1)$$

For a linear system such as this series RLC circuit, the solution to $Z_M(s)$ includes a transient and a steady state component. The steady state component is obtained by considering the imaginary component of s while neglecting its real component. Hence the steady state response of Z_M , also known as frequency response, is obtain by having $s = j\omega = 2\pi fj$ giving

$$Z_M(2\pi fj) = R_M + 2\pi fjL_M + \frac{1}{j2\pi fC_M}. \quad (3.2)$$

Furthermore, using Equation (3.2) the magnitude and phase response of Z_M against $\Delta f (= f_{INJ} - f_0)$ for parameters in Table 3.1 is illustrated graphically in Figure 3.2.

Table 3.1: Crystal resonator and injection parameters used for analysis

f_0	L_M	C_M	R_M	C_0	$V_{INJ} (ac)$
38.4 MHz	2.865m H	6f F	60 Ω	2p F	1 V

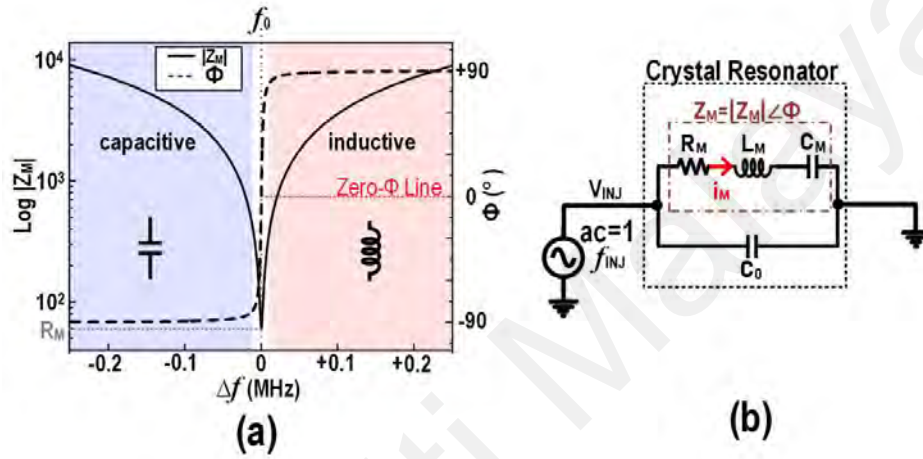


Figure 3.2: (a) Frequency response of motional branch (Z_M) of crystal resonator, exhibiting both capacitive ($\Delta f < 0$) and inductive ($\Delta f > 0$) characteristics, and (b) the circuit used to derive the frequency response.

Resonance detecting techniques in IGCI (2022) and by Cai (2023) use the dip in impedance magnitude at f_0 (shown in Figure 3.2) to represent f_0 . Such dip detection requires the use of the power-hungry comparator. While there has been on-going research in power reduction of comparators, e.g using dynamic comparators (Babayan-Mashhadi & Lotfi, 2014), there is still a significant current consumption due to the biasing tail current. Additionally, in IGCI, a voltage reference is required. This chapter presents a novel approach to resonance detection using zero-phase at f_0 (Figure 3.2) detected by D-flip flop, which is a low power and simple circuit without any reference voltage in contrary to the comparator, allowing for lower power consumption and reduced performance variation.

where f_{01} is the new resonance frequency seen by the buffer in the presence of C_{L2} given no loading from the amplifier. Equation (3.3) evinces that when $C_{L2} \gg C_M$ then $f_{01} \approx f_0$.

Utilizing the crystal parameters in Table 3.1, Figure 3.4(a) shows how increasing C_{L2} brings f_{01} closer to f_0 thereby theoretically proving that zero-phase cross detection is an alternative means to reasonably detect f_0 .

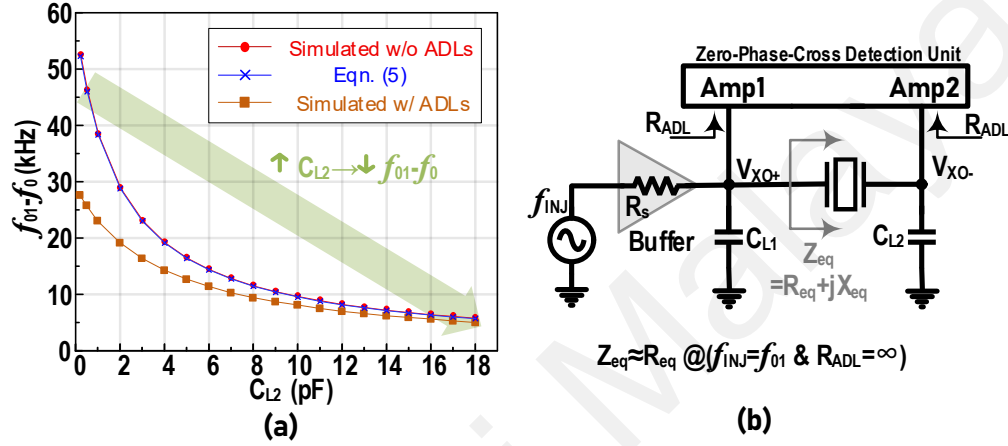


Figure 3.4: Resonance frequency difference between (3.3) and simulations for different C_{L2} values with and without ADL loading - where loading is from the transistor implemented Zero-phase cross detection block.

By addition and increase of C_{L2} we have modified the equivalent circuit seen by buffer so that the resonance frequency f_{01} is closer to the resonance frequency f_0 of the crystal. Unlike resonator's resonance frequency we can detect f_{01} without using a current detector. This can be accomplished by detecting the zero-phase cross between signals V_{XO+} and V_{XO-} .

Since the combination of crystal and C_{L2} induce zero-phase at f_{01} and a grounded capacitor provides a -90° phase shift, the steady-state phase $\theta(\omega)$ at V_{XO-} with respect to V_{XO+} is $(\angle V_{XO-} - \angle V_{XO+}) = -90^\circ$, which is validated by considering the voltage division at V_{XO-} :

$$V_{XO-}(j\omega) = V_{XO+}(j\omega) \cdot \frac{1/j\omega C_{L2}}{Z_{eq}(j\omega)} \quad (3.4)$$

From Equation (3.4), we can obtain phase $\theta(\omega)$ as:

$$\begin{aligned}\theta(\omega) &= \angle V_{XO-}(j\omega) - \angle V_{XO+}(j\omega) \\ \theta(\omega) &= \angle(1/j\omega C_{L2}) - \angle Z_{eq}(j\omega),\end{aligned}\tag{3.5}$$

where Z_{eq} is the impedance seen by the buffer, and it is equivalent to the impedance of crystal added to the impedance of C_{L2} . Equation (3.5) shows that when $\angle Z_{eq}(j\omega)=0$, which occurs when $\omega \approx \omega_{01}(=2\pi f_{01})$, $\theta(\omega)$ becomes -90° . Additionally studying (3.5) for frequencies from just above f_{01} to just below it, we observe that the phase changes from 0° to -90° and then to -180° which indicates a sharp phase transition through f_{01} . This sharp transition is detected by the AC-coupled amplified D-FF thereby detecting f_{01} .

Thus far using steady state analysis we have quantitatively analysed how the zero-phase cross detection unit detects for f_{01} by using the easily sampled voltage signals V_{XO+} and V_{XO-} over current signals. Note that this behaviour is observed for the steady state response which forms a part of the transient response of the voltage difference between V_{XO+} and V_{XO-} . therefore for a complete analysis the transient response will be analyzed in upcoming macro-model implementation sub-section to provide a complete analysis of zero-phase cross detection circuit.

3.1.2 Zero-Phase Resonance Frequency Detection Macro-Model Implementation

The macro-model circuit in Figure 3.4, implemented in Verilog-A using Cadence Virtuoso and the Specter simulator¹⁰, verifies the analysis. The macro-model demonstrates that for a crystal under down-chirp injection, increasing C_{L2} would reduce $|f_{01}-f_0|$.

¹⁰ Simulation details including the VerilogA code has been placed in Appendix B: Verilog-A of Macro-model Blocks.

Herein we evaluate the f_{01} based on the phase transition whereby as the frequency goes through f_{01} the phase between V_{XO+} and V_{XO-} is expected to rapidly change from its steady value.

Amplifiers were tuned for a gain that provides peak-to-peak digital outputs while providing an equal delay. The results of phase between V_D and V_{CLK} ¹¹ (corresponding to V_{XO+} and V_{XO-} respectively) for different capacitor values are given in Figure 3.5(a).

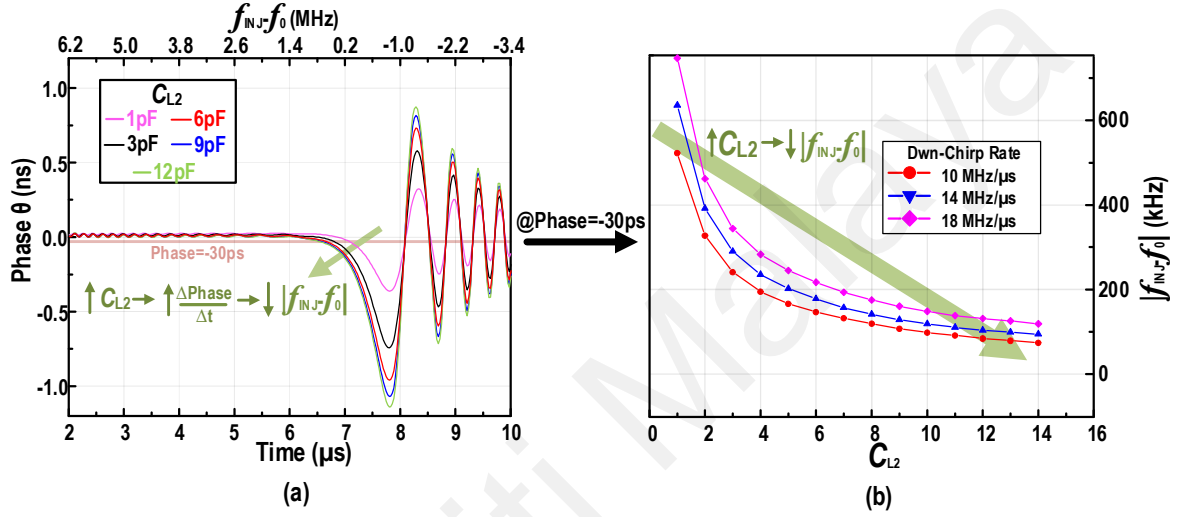


Figure 3.5: Evaluating the relationship between C_{L2} and f_{01} , where f_{01} represents the frequency at which phase rapidly shifts relative to its steady-state value, using: (a) phase against time for a 1.2MHz/μs down-chirp, (b) C_{L2} against $|f_{INJ}f_0|$ at Phase=-30ps for different down-chirp rates.

Studying Figure 3.5(a), it can be observed that with increase in C_{L2} the rate of change of phase $\frac{\Delta Phase}{\Delta t}$ is higher which in turn results in earlier crossing of -30ps phase thereby indicating a decrease in resonance frequency seen by buffer.

The relationship which was observed in Figure 3.4 for steady state analysis is also observed in Figure 3.5(b)'s transient analysis regardless of chirp rate, thereby evidencing that the analysis developed with Equations (3.5) and (3.3) is sound. To further validate the relationship as given by Equation (3.5) the results of Figure 3.5(b) are curve fitted to Equation (3.5) from

¹¹ Phase is calculated as the time difference between positive edges of V_D and V_{CLK} .

which we have obtained an average r^2 of 99.96%¹². Thereby we can state with a high degree of certainty that the developed analysis describes the developed system. This marks the part completion of objective 1, whereby the remainder of the objective is accomplished by analyzing for the proposed Adaptive Chirp concept in the future section.

3.1.3 Zero-Phase Lock Macro-Model Implementation

The Zero-phase lock macro-model in Figure 3.6 was developed to establish the system level design considerations and set specifications for each block. Crystal parameters in Table 3.1 was used for this simulation.

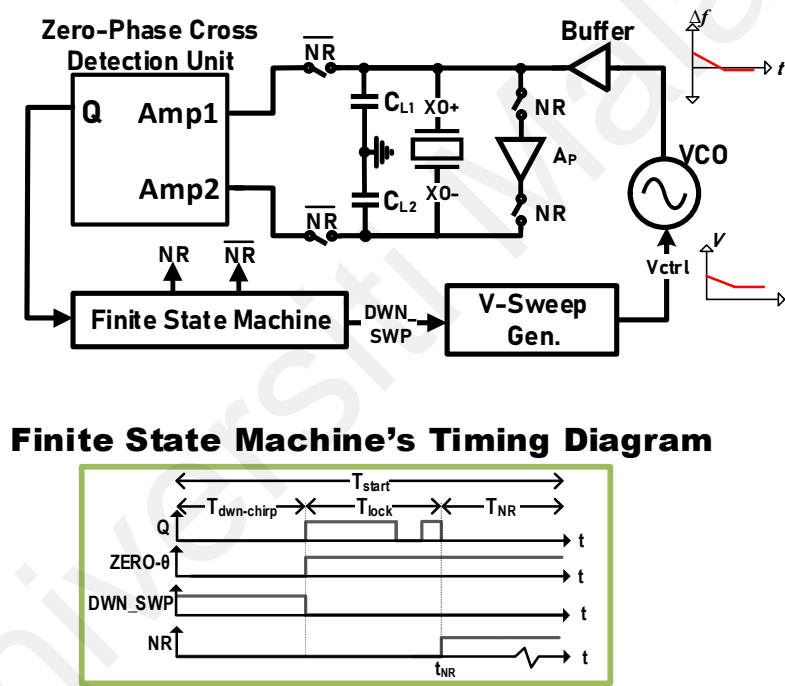


Figure 3.6: Zero-Phase Lock XO start-up macro-model block diagram and timing diagram.

In addition to Zero-phase cross detection unit, the ZL block diagram consists of C_{L1} ¹³ and amplifier A_p for pierce oscillator, and finite state machine for system control.

¹²The curve fitting report is provided in Appendix C: Curve Fitting of Figure 3.5(b) onto Equation.

¹³ C_{L1} is added for the effective operation of Pierce Oscillator.

Upon detection of positive edge trigger on Q the FSM's ZERO- θ will latch as one and consequently stop down sweep of voltage V_{ctrl} and hold injected frequency permanently. The buffer injects energy with a preset duration of T_{lock} after which NR state becomes 1, which signals the buffer and Zero-phase cross detection unit to detach while it signals the pierce oscillator to attach at time t_{NR} ¹⁴. This transition allows i_M to reach steady state condition.

Table 3.2 lists design considerations that was derived by studying the system's macro-model.

Table 3.2: Design Considerations developed using the implemented macro-model XO-start-up

Block	Considerations When Designing the Block
Zero-Phase Cross Detection Unit	<p>Amplifier Gain:</p> <ul style="list-style-type: none"> - Must be high enough to produce accurate digital representation of V_{XO+} and V_{XO-} phase difference at V_D and V_{CLK} respectively - Must be low enough to reduce power consumption. <p>Amplifier Delay:</p> <ul style="list-style-type: none"> - The delay difference between Amp1 and Amp2 can be used to fine tune to obtain more accurate resonance frequency detection. - Accurate delays are difficult especially due to process variation. - Large delays would increase transistor count and hence power consumption. <p>Amplifier Loading:</p> <ul style="list-style-type: none"> - Reducing the loading by amplifier on the buffer will help increase crystal excitation and reduce the required gain by the amplifiers Amp1 and Amp2. <p>AC coupling Cap Size:</p> <ul style="list-style-type: none"> - large enough to completely decouple the DC - Have a small enough $\tau(=R_{Bias}C)$ to reduce the charge required to charge the ac coupling cap to steady state thereby reducing D-FF errors. <p>R_{Bias} Size:</p> <ul style="list-style-type: none"> - Large enough to only pass DC and reduce AC loading of buffer - Have a small enough $\tau(=R_{Bias}C)$ to allow the ac coupling capacitor to charge to steady state thereby reducing D-FF errors. <p>D-Flip Flop Metastability Window:</p> <ul style="list-style-type: none"> - a lower metastability window would result in lower frequency error.

¹⁴The duration T_{lock} and time of detachment of injection unit is discussed in section 4.2.

C_{L1} and C_{L2}	C_{L1} and C_{L2} size: <ul style="list-style-type: none"> - C_{L1} is to be made equal to C_{L2} for a typical pierce oscillator configuration. - High C_{L2} would increase resonance frequency detection accuracy. - High C_{L1} and C_{L2} would mean higher loading of buffer and hence lower signals passed to the zero-phase cross detection thereby demanding more amplification. Concurrently this causes lower V_{XO+} and V_{XO-} which would mean lower excitation of crystal. - Larger C_{L1} and C_{L2} at steady state would improve phase noise of the oscillator as well as improving the frequency accuracy.
Amplifier A_P	Amplifier Gain: <ul style="list-style-type: none"> - The gain of the amplifier affects R_N thereby the excitation of i_M after time t_{NR}. - Higher the gain, the higher the power consumption.
V Sweep Gen. and VCO	The Rate of Sweep: <ul style="list-style-type: none"> - frequency sweep affects the peaks of phase θ therefore, for a given delay a high rate may cause the D-FF not to get triggered. Initial Frequency Across Corners: <ul style="list-style-type: none"> - Since larger frequencies would cause larger power consumptions, the initial frequency is to be designed as PVT tolerant and not too far away from resonance frequency. - To reduce start-up time the initial frequency across corners should be very close to f_0
Switches	Size of Switch (W/L): <ul style="list-style-type: none"> - For minimal power consumption, the loading from buffer to Zero-phase cross detection unit is to be reduced by increasing the switch size. - Leakage and loading on amplifier A_P are to be reduced for improved excitation after time t_{NR}.
Buffer	Driving Strength of Buffer: <ul style="list-style-type: none"> - Buffer is to be large enough to produce sufficient inputs to the zero-phase cross detection when Zero-θ is 0 - Buffer is to be large enough to produce large excitation when Zero-θ is 1. - The buffer should be small enough to reduce power consumption.

3.2 Zero-Phase Adaptive Chirp (ZAC) Injection

Although resonance lock injection techniques such as ZL can improve the injection efficiency over chirp injection via focusing of injection frequency, their inherent phase error, ϕ , accumulation reduces the reliability of i_M excitation across PVT variations. To this end, Adaptive chirp is proposed to automatically correct injection phase thereby improving reliability across PVT variations.

This subsection will analyse adaptive chirp injection and validates the phase correction property via macro-model implementation. Furthermore, the macro-model is used to set design considerations, and specifications for the transistor level implementation of ZAC.

3.2.1 Zero-Phase Adaptive Chirp (ZAC) Injection Analysis

In conventional resonance locked injection techniques such as in Luo et al's IGCI (2022), the injection unit is locked at near f_0 . However, to ensure an effective injection, the frequency mismatch after locking must be below 530 ppm to establish a maximum motional current for given crystal parameters in Table 4.1, $C_{L1}=C_{L2}=14$ pF, and $V_{XO+}=0.9$ V as obtained below (Lei et al., 2021):

$$\frac{\Delta f}{f_0} = \mp \frac{4V_{INJ}/\pi}{V_{XO}} \cdot \frac{C_M}{(C_{L1} + C_{L2})/2 + C_0}, \quad (3.6)$$

where V_{XO} is the steady-state oscillating amplitude, V_{INJ} is the amplitude of the injection signal, C_{L1} and C_{L2} are the load capacitances to two ends of the crystal, and C_0 is crystal's shunt capacitance. Locking within 530 ppm of f_0 requires a delicate design consideration accounting in the chirping sweep rate, VCO noise, and delay in resonance detection under PVT variations. Consequently, due to Δf and uncorrected phase error, ϕ , the injection has to be disabled by a short duration when the maximum i_M , $|i_M|_{Max}$, has been reached (see Figure 3.7).

In light of this challenge, we proposed adaptive chirp to relax such strict design requirements and enable ϕ correction under PVT variation. Adaptive chirp is an enhancement to the

resonance lock injection techniques by allowing for continuous Δf and ϕ correction. In principle, the chirping circuit sweeps the output signal's frequency, f_{INJ} , up and down about f_0 to correct the ϕ accumulated due to injection with Δf (Figure 3.6¹⁵).

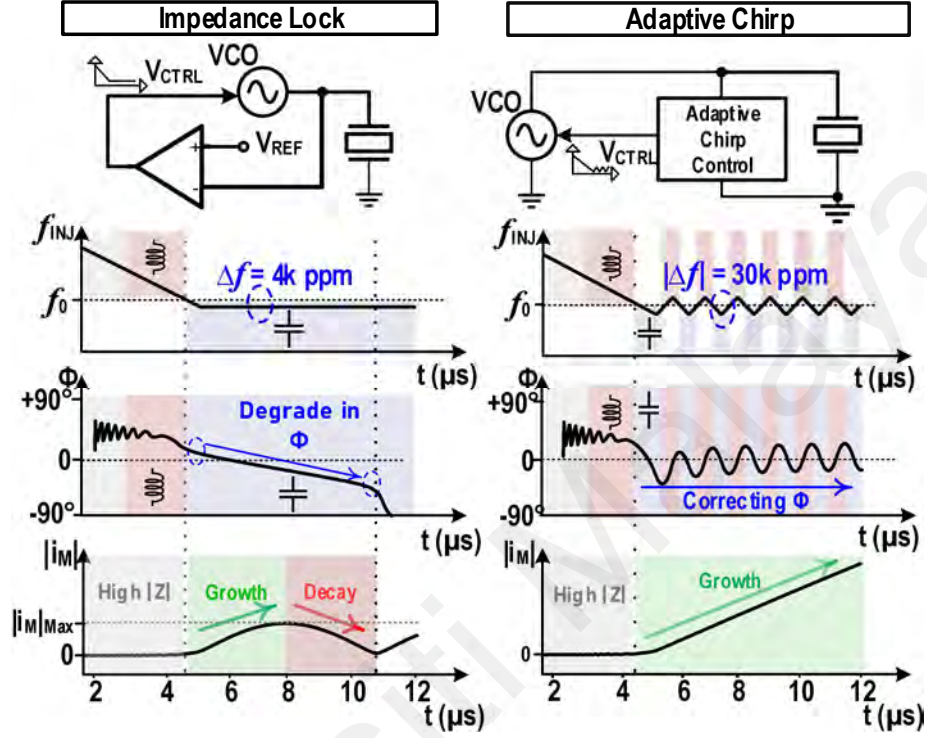


Figure 3.7: Comparison of conceptual operation between Impedance lock and the proposed adaptive chirp (fixed peak-to-peak frequency toggling of 30,000 ppm around the resonance) in terms of frequency, phase and motional current envelop profiles.

Initially, the chirping signal starts its operation with a frequency significantly higher than f_0 similar to that of ZL injection. As f_{INJ} approaches f_0 (entering low- Z_m region), due to the positive Δf (initial $f_{\text{INJ}} > f_0$), the resonator exhibits an inductive impedance (shown as red background), resulting in a pulling of ϕ towards the positive. As f_{INJ} continues to decrease below f_0 , the resonator transfers from inductive to capacitive. This transition leads to a pulling of ϕ towards the negative. Therein, the ϕ crosses the zero value. Upon the detection of zero-phase cross the chirping direction is inverted (from down-chirping to up-chirping) to effectively correct the

¹⁵ The results are from macro-model simulations whereby Impedance Lock locks at frequency of $\Delta f = 4\text{k ppm}$ while Adaptive Chirp's frequency linearly goes up and down about f_0 with $|\Delta f| = 30\text{k ppm}$ for the same duration of up-chirp and down-chirp-see the frequency of injection in Figure 3.6.

new ϕ ¹⁶. Similarly, upon reaching the up-chirping operation, the ϕ also crosses the zero again, where we can again detect this point and invert the chirping direction. Hence, the circuit will generate an alternative up- and down-chirping sequence centred around f_0 to enable a continuous correction of ϕ . This coordinated approach facilitates sustained $|i_M|$ growth.

For our implementation, the zero-phase detector used is the Zero-phase Cross Detection unit thereby making the adaptive chirp injection as Zero-Phase Adaptive Chirp (ZAC). To verify the functionality of Zero-Phase Adaptive Chirp in terms of phase error correction, we will utilize macro-models using AHDL for digital and analogue blocks.

3.2.2 Zero-Phase Adaptive Chirp (ZAC) Macro-Model Implementation

ZAC may be built upon ZL injection whereby upon each detection of zero-phase cross, the VCO switches between up- and down- chirp. The macro-model of ZAC is shown in Figure 3.8.

Note that the primary difference to Figure 3.6's ZL implementation is the change in FSM.

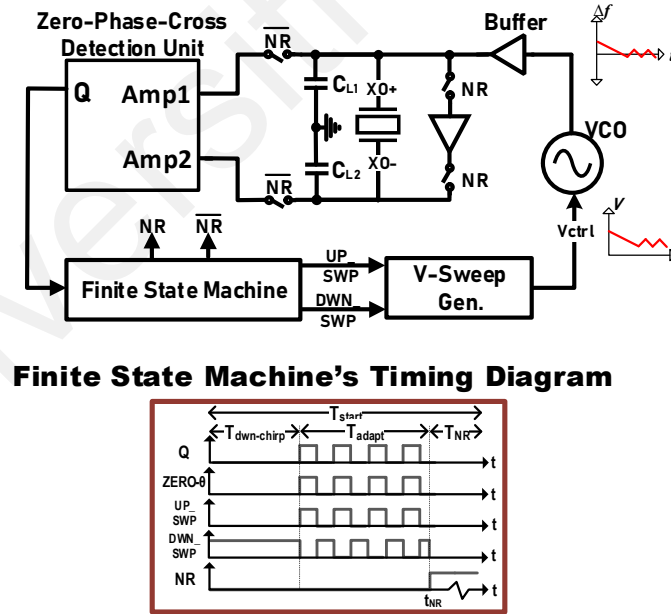


Figure 3.8: Zero-Phase Adaptive Chirp XO start-up macro-model and its timing diagram.

¹⁶ In the simulation the duration of up- and down-chirp is tuned to ensure this transition upon zero-phase cross.

The FSM change involves addition of UP_SWP state to allow for up chirping of frequency when it is equal to 1. The timing diagram of ZAC's macro-model implementation is also given in Figure 3.8.

This macro-model is used to (1) verify the analysis in terms of phase correction property and (2) establish the system level design considerations and specifications for each block.

Figure 3.9(a) shows how the macro-model implementation of ZAC exhibits frequency correction as the f_{INJ} goes up- and down- about f_0 . Furthermore, the phase correction is shown in Figure 3.9(c) by preventing the injection phase mismatch, ϕ , to continuously accumulate.

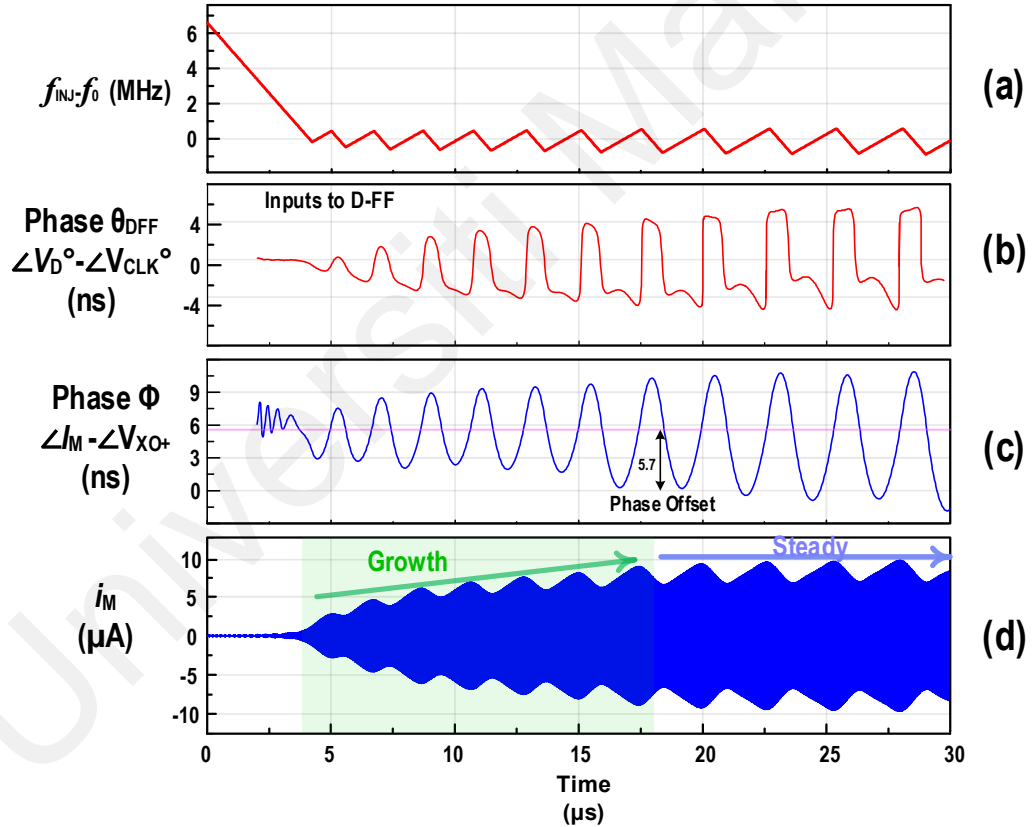


Figure 3.9: Illustration of the phase and frequency correction properties demonstrated by the Zero-Phase Adaptive Chirp (ZAC) injection macro-model. (a) displays the frequency response of ZAC, (b) shows the phase response of the D-FF inputs, (c) presents the injection phase mismatch, and (d) depicts the motional current profile.

The effect of the frequency and phase correction showcases how the motional current initially grows as hypothesized (green background in Figure 3.9(d)). Notably, although the growth

period is very long, it is not indefinite, and this is because of the offset phase of 5.7ns – the effect of this is to be discussed further in Chapter 4.

Herein, the macro-model simulation results have verified the hypothesized phase and frequency correction properties of ZAC thereby marking the completion of the first objective - namely to formulate analysis that describes the characteristics of both ZAC and ZL techniques.

The macro-model results were also used to lists design considerations for each block that will be used for transistor level implementation of Zero-Phase adaptive chirp Injection (listed in Table 3.3).

Table 3.3: Zero-Phase Adaptive Chirp design considerations developed using the implemented macro-model XO-start-up

Block	Considerations when selecting parameters
Zero-Phase cross detection unit	<p><i>(Same considerations as ZL in Table 3.2)</i></p> <p>D-Flip Flop Metastability Window:</p> <ul style="list-style-type: none"> - The window must be small enough for detection, for the given L_M and sweep rate, to prevent the injection frequency to escape – explanation provided in Appendix D: D-FF's Metastability.
C_{L1} and C_{L2}	<i>(Same considerations as ZL in Table 3.2)</i>
Amplifier X1	<i>(Same considerations as ZL in Table 3.2)</i>
V Sweep Gen and VCO	<p><i>(Same considerations as ZL in Table 3.2)</i></p> <p>The Rate of Sweep:</p> <ul style="list-style-type: none"> - frequency sweep effects the peaks of phase θ after the initial chirp inversion therefore a high up-chirp rate may cause the D-FF not to get triggered again.
Switches	<i>(Same considerations as ZL in Table 3.2)</i>
Buffer	<i>(Same considerations as ZL in Table 3.2)</i>

3.3 Transistor Level ZAC and ZL XO Start-up Implementation

Using the design considerations from Table 3.2 and Table 3.3, the transistor level ZL and ZAC XO start-up systems has been designed (Figure 3.9).

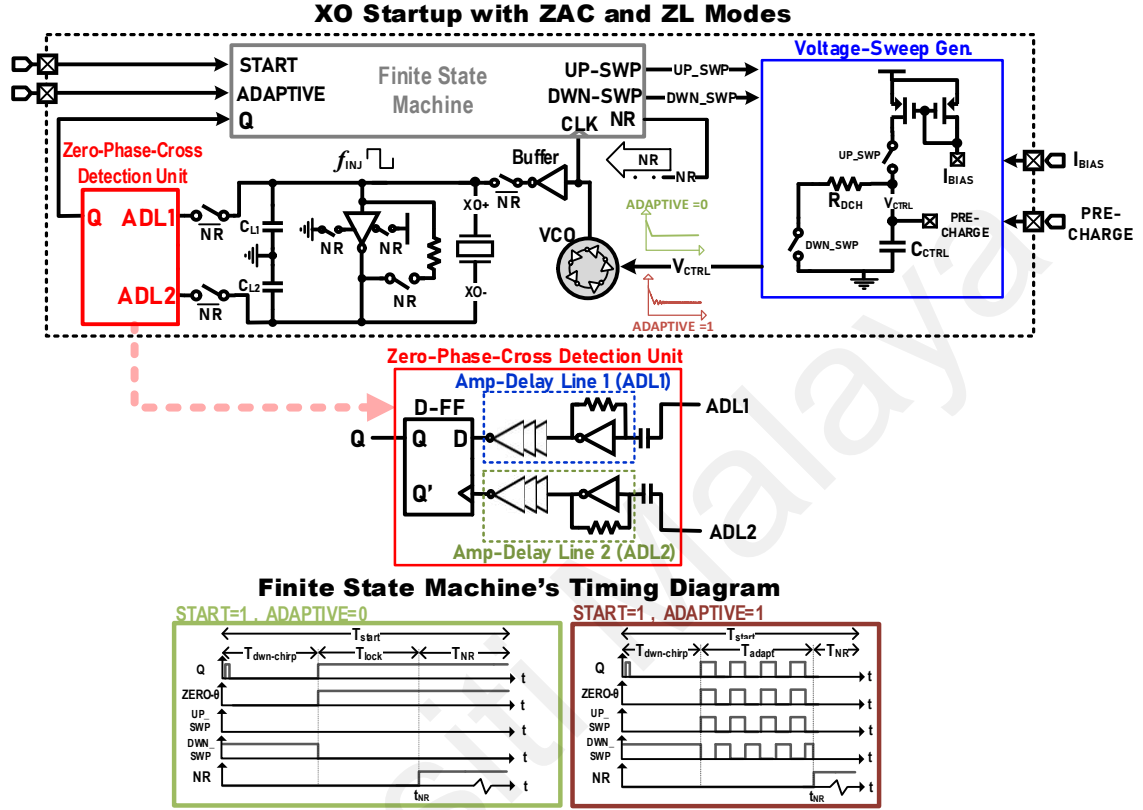


Figure 3.9: Transistor-level architecture of the proposed crystal oscillator with zero-phase lock and zero-phase adaptive chirp start-up modes.

The system includes primarily a digital CMOS finite state machine, voltage sweep generator, 5-stage voltage-controlled ring oscillator, zero-phase cross-detection unit with digital CMOS D-FF, self-biased inverter as amplifiers and inverter lines as delay lines, a weak inverting buffer to excite the crystal and a self-biased inverting amplifier for Pierce oscillator configuration.

The start-up sequence and operation of ZL and ZAC injection (Figure 3.9) is as follows:

- The initial voltage of the sweep voltage generator, V_{CTRL} , is set by charging its capacitor, C_{CTRL} , using the PRECHARGE port.

- b) When the start-up is enabled, the V_{CTRL} starts to drop according to $\Delta V = V_{CTRL}(t=0) \times \exp(-\Delta t / R_{DCH}C_{CTRL})$. Hence, the VCO's frequency starts to decrease.
- c) The zero-phase cross-detection unit detects the relative phase between V_{XO+} and V_{XO-} . To overcome the error due to the random noise, the FSM only accepts transition when the results from 3 periods are identical. The FSM uses the VCO's clock signal to count this duration using a digital counter.
- d) When the f_{INJ} drops below f_{01} , the zero-phase cross-detection unit detect this zero-phase point.
- e) For ZL injection (at ADAPTIVE=0), when the crossing point is detected (zero- θ becomes 1 V), the DWN_SWP state turns to 0 V and consequently locks the injection frequency. The injection then continues until it reaches a preset duration, T_{lock} .

For the ZAC injection (when ADAPTIVE=1), upon inversion of zero- θ , the DWN_SWP and UP_SWP states become 0 V and 1 V, respectively, leading to the charging of C_{CTRL} according to $\Delta V = I_{BIAS} \times \Delta t / C_{CTRL}$. This results in an up-sweep of V_{CTRL} and an up-chirp of f_{INJ} . Another inversion of zero- θ inverts UP_SWP and DWN_SWP states again, causing a down-chirp of f_{INJ} . This process continues for a preset injection duration, T_{adapt} . After the injection durations for both ZL and ZAC injections, the NR state changes to 1 V at time t_{NR} (where this value will be discussed in sub-chapter 4.2).

- f) With NR state at 1 V, the injecting unit and zero-phase cross-detection unit are disabled, while the core amplifier unit, made from a self-biased inverter, is in place to sustain the oscillation in the steady state.

3.3.1 Implementation Workflow

The systematic transistor-level optimization with post-layout verification (PEX) is provided as in workflow diagram in Figure 3.10.

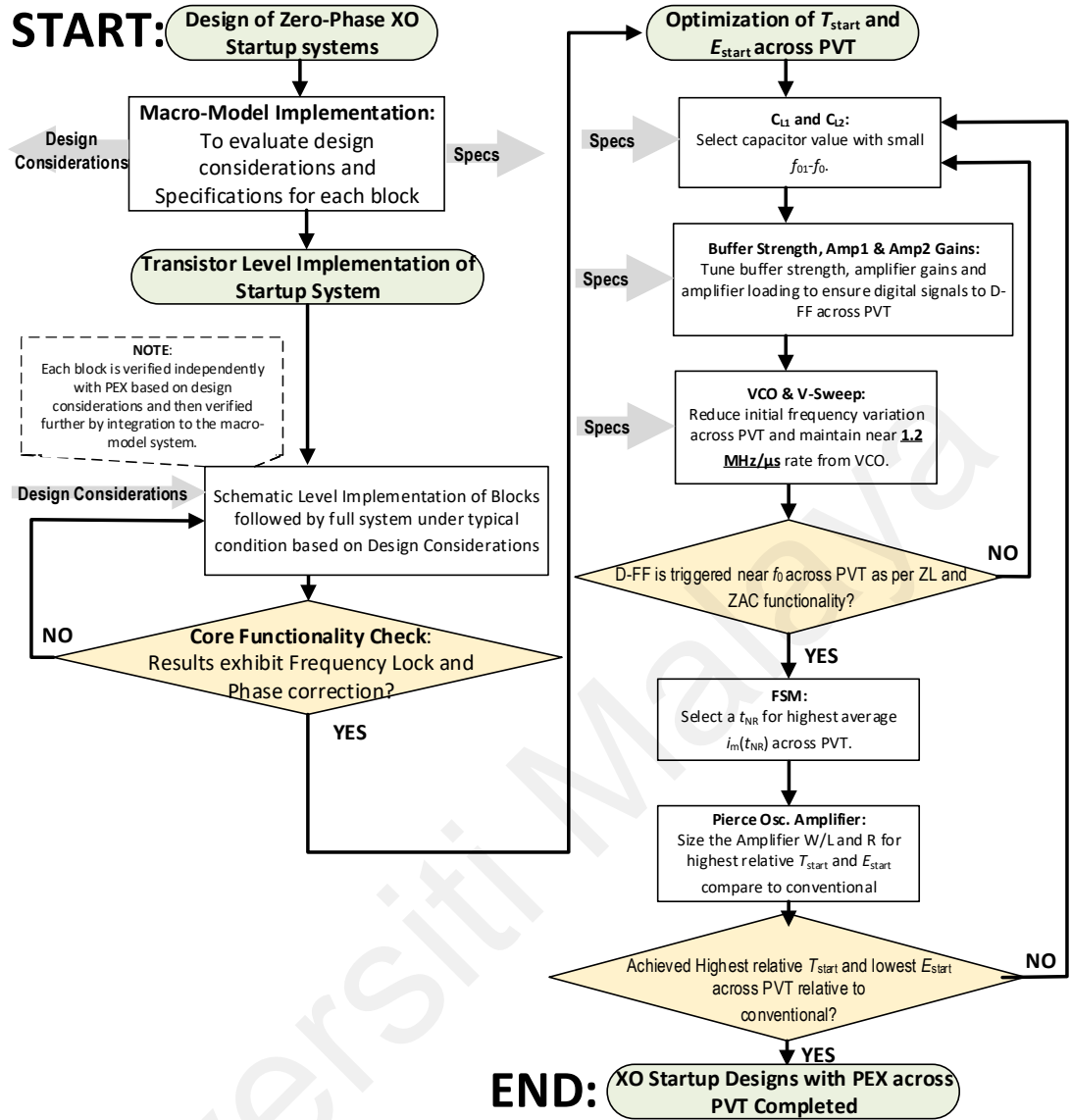


Figure 3.10: Transistor level implementation workflow with PEX verifications across PVT corners

The proposed system is compact and utilizes mostly digital blocks leading to more rapid implementations by the designers. This can be especially useful as most injection type start-up oscillator circuits, aside from chirp injection, are fairly complex and would require longer implementation period which would lead to increased cost and longer time to market.

CHAPTER 4: POST-LAYOUT SIMULATION RESULTS AND DISCUSSION

We implemented and simulated the proposed fast start-up XOs in the 65-nm CMOS process with voltage supply of 1 V (layout shown in Figure 4.1). The work showcasing the variation tolerance of the proposed injection techniques in reducing XO start-up time is the core contribution of this project.

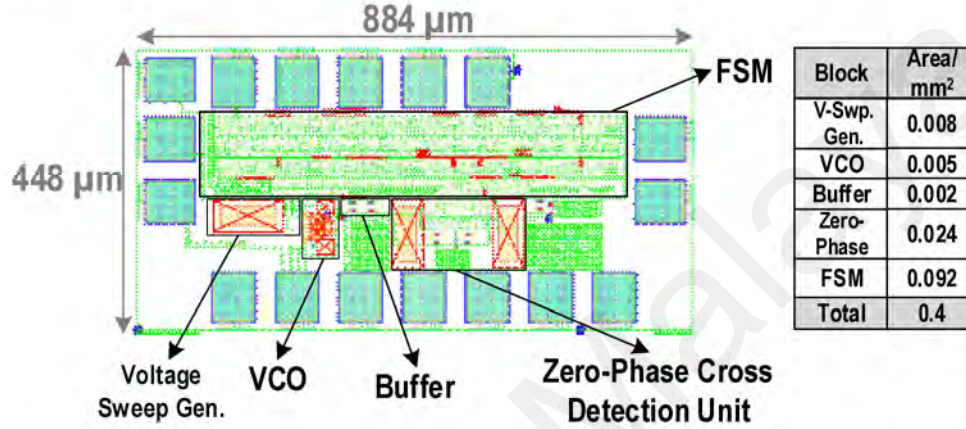


Figure 4.1: Physical Layout of the XO-start-up systems

Before delving into the results, subsections 4.1 and 4.2 provide a detailed analysis of the systematic approach used to determine the optimal values for C_{L2} and t_{NR} . Following this, subsection 4.3 evaluates the performance of the start-up techniques under various PVT variations, highlighting their robustness. Subsection 4.4 offers a comparative analysis of the proposed methods against the current state-of-the-art techniques, emphasizing the advancements. Finally, subsection 4.5 outlines the proposed future directions for further research and development in this area.

4.1 Determination of C_{L2} for ZAC and ZL

Detection of f_0 using zero-phase cross detection requires the design of C_{L2} and the relative delay difference between amplifier-delay lines 1 and 2, as they will affect the zero-crossing point (as illustrated by Figure 4.2).

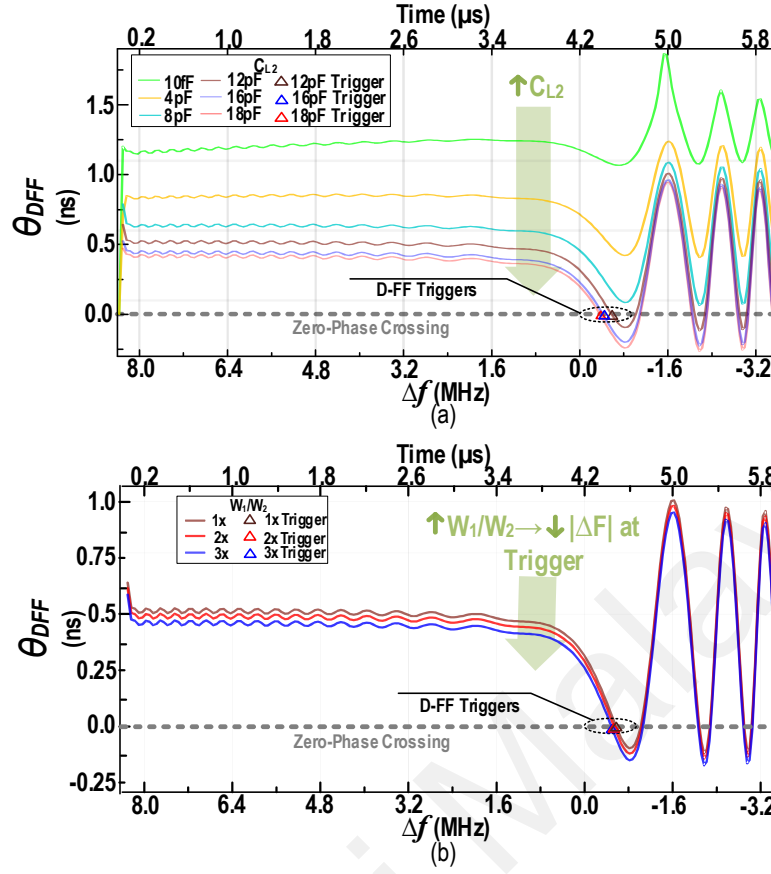


Figure 4.2: The $\theta_{DFF}(t)$ versus Δf for different (a) C_{L2} and (b) different delay line sizing at chirping rate of 2MHz/ μ s in the simulations for worst case delay drop.

Figure 4.2(a) shows how increasing C_{L2} of a transistor level implementation brings zero-phase cross frequency (shown as D-FF Trigger) closer to resonance frequency, $\Delta f = 0$; which was hypothesized and tested with macro-model simulation. To ensure the first zero-crossing with tolerance to D-FF's metastability¹⁷ and PVT variations, given crystal resonator parameters in Table 3.1, C_{L2} of 14 pF is selected as the transient phase goes well below zero-phase (shown in Figure 4.2(a)). Furthermore, the delay difference between the lines is adjusted via width ratio (W_1/W_2) and it is sized as 2x by a trade-off between consistent PVT operation and reduced footprint. Indeed, we utilized these two parameters to achieve coarse and fine-tuning on $\theta_{DFF}(t)$ such that $\theta_{DFF}(t) = 0^\circ$ when $\Delta f = 0$ [Figure 4.2(a) and (b)].

¹⁷ D-FF's metastability is discussed in Appendix D: D-FF's Metastability

The Monte-Carlo simulated Δf (at D-FF trigger) in Figure 4.3 proves zero-phase cross-detection unit's core functionality robustness against process variation.

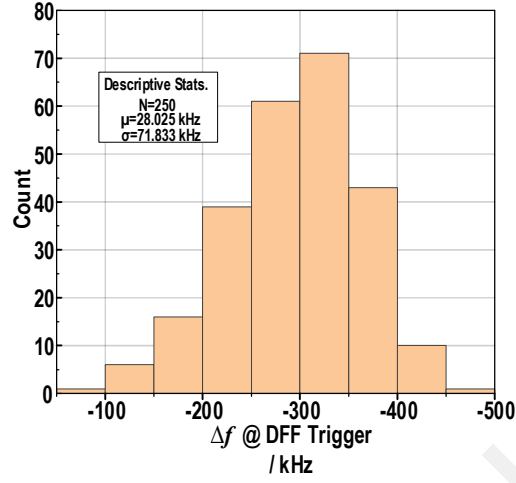


Figure 4.3: Monte-Carlo simulated Δf (at D-FF trigger) given $C_{L2}=14\text{pF}$, and $2\times W_1/W_2$ under $2\text{ MHz}/\mu\text{s}$ down chirp.

Figure 4.4 illustrates the operation of zero-phase cross-detection for ZAC showcasing how upon adaptive inversions of Q the frequency converges about $f_{01}(\approx f_0)$. This results in a lower frequency mismatch error compared to ZL. The adaptive frequency correction property also reduces the impact of variations on the injected frequency and crystal excitation. Additionally, the proposed adaptive injection provides phase correction, further enhancing variation tolerance (where phase correction is further discussed in subsection 4.2)

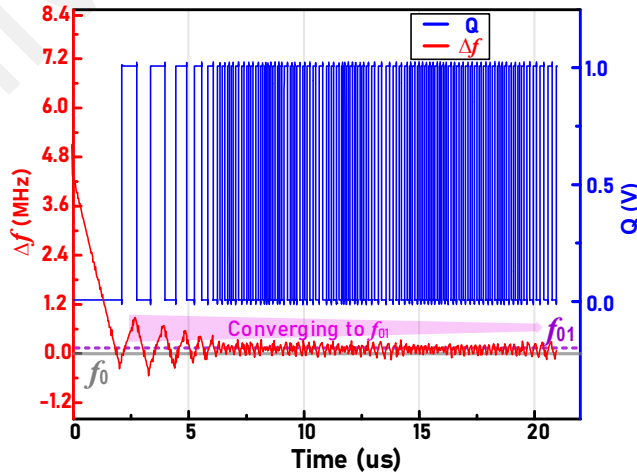


Figure 4.4: Frequency profile of the zero-phase adaptive chirp injection and the output from the D-FF

4.2 Determination of t_{NR} for ZAC and ZL based on Process Corners

We have selected a crystal resonator with f_0 of 38.4 MHz driven by a small buffer ($V_{XO+}=150\text{mV}$ peak to-peak). To cover the PVT variations, the initial V_{CTRL} is set such that VCO's initial frequency is above f_0 in all corners. This is done via simulation sweep of V_{CTRL} and selecting a single V_{CTRL} that will provide frequencies that are higher than f_0 across all PVT corners. This V_{CTRL} is selected to be 520 mV. Furthermore, the ring-VCO exhibits the fastest and slowest frequency down-sweep rates of $1.6\text{ MHz}/\mu\text{s}$ and $0.8\text{ MHz}/\mu\text{s}$ for the FF and SS corners, respectively whereby these rates are lower than the worst case considered ($2\text{ MHz}/\mu\text{s}$) which ensures the first detection of zero-phase cross.

Figure 4.5 shows $i_{M,env}$ for all process corners to highlight the phase-error correction property of ZAC relative to ZL.

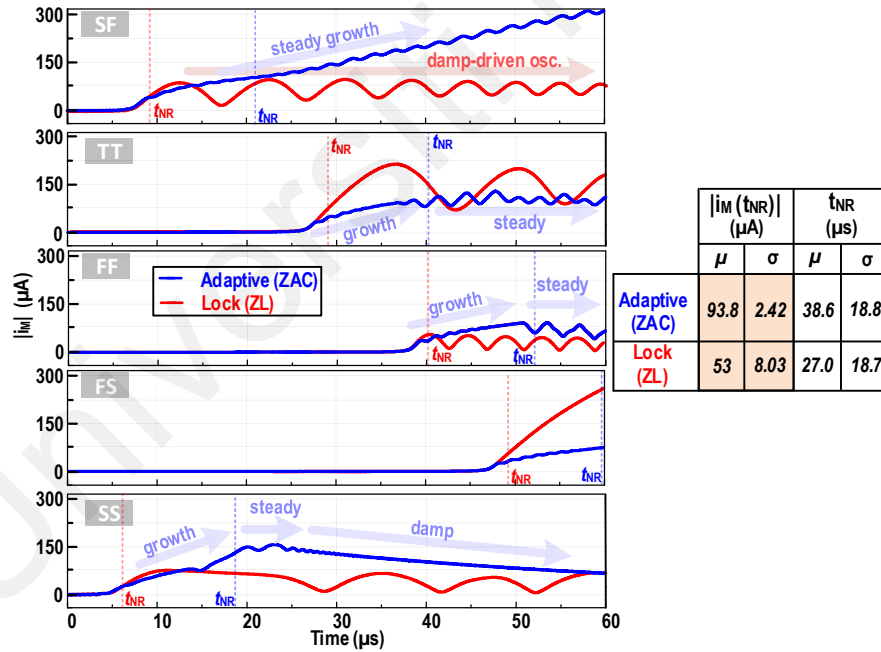


Figure 4.5: The growth of $|i_M|$ using ZAC and ZL. Based on shown results, we set t_{NR} 519 cycles and 70 cycles after the first zero-phase detection respectively.

ZL consistently shows the undesirable damped driven oscillation which is the result of phase error accumulation. This is a trend that is exhibited across all resonance locked injection including Impedance Guided Chirp Injection (Luo et al., 2022). This trend makes it especially

hard to select a t_{NR} to achieve a variation tolerant $i_{M,env}$ and hence a variation tolerant T_{start} . While ZL only exhibits damped driven oscillation, ZAC shows (1) $i_{M,env}$'s continuous growth (at SF), (2) growth and sustain (at TT and FF), and (3) growth, sustain and gradual damping (at SS) corresponding to broad effectiveness of adaptive chirp in terms of phase correction property.

This broad effectiveness is attributed to the offset of phase error correction. Figure 4.6 uses the macro-model simulations results to explain the various effectiveness of adaptive chirp due to this phase offset value. Note that Figure 4.6 is an elaboration on results from Figure 3.9, whereby the concept of positive and negative interference and degree of occurrence will be used to explain the results in Figure 4.5.

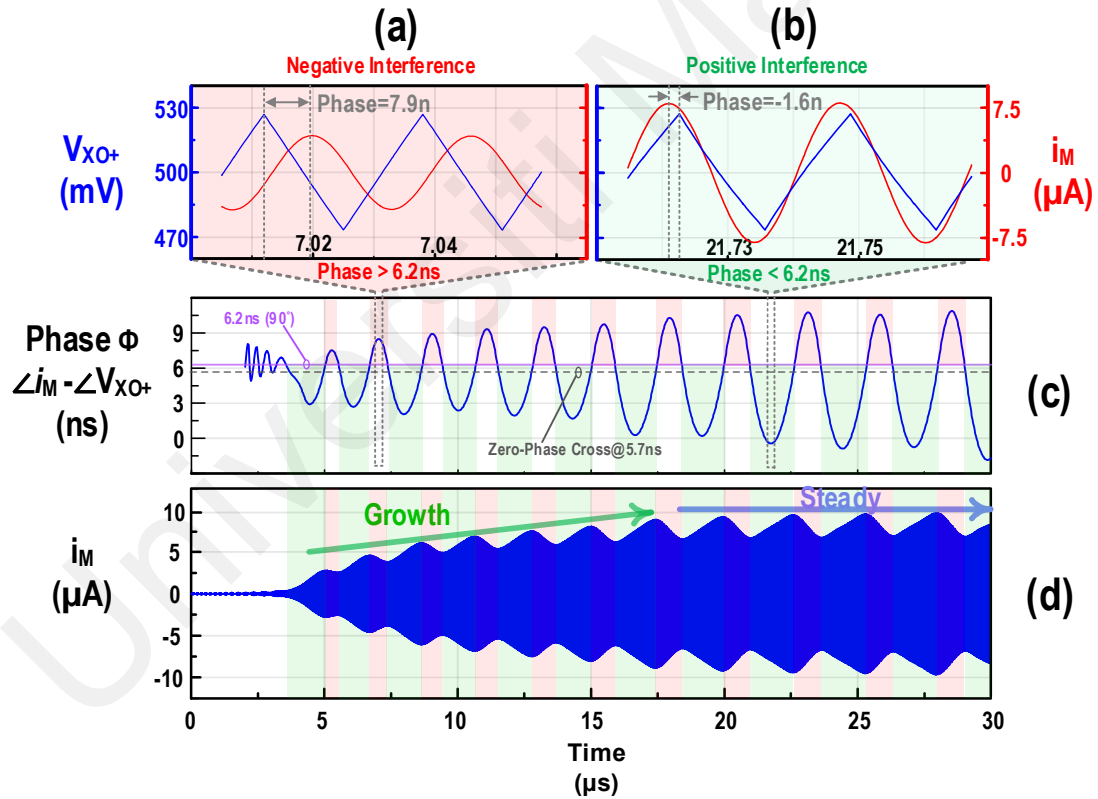


Figure 4.6: Phase correction property exhibited by Zero-Phase Adaptive Chirp injection macro-model implementation. Signals i_M and V_{XO+} during (a) positive interference and (b) during negative interference; (c) gives the injection phase mismatch, and (d) is the motional current profile.

The positive interference, which causes increase in envelop of $|i_M|$, occurs when $\phi < 90^\circ$ or $\phi < 6.2ns$. On the other hand, negative interference, which causes drop in $|i_M|$ envelop, occurs when $\phi > 90^\circ$ or $\phi > 6.2ns$. These positive and negative interference regions are illustrated in Figure 4.6 as green and red backgrounds respectively.

Note that the existence of negative interference is due the ϕ offset of $5.7 ns$ ¹⁸ instead of $0 ns$. Considering the case of an ideal adaptive chirp, the ϕ offset is $0 ns$, shown in Figure 3.7, whereby this zero offset causes only positive interference. The proposed Zero-phase implementation of adaptive chirp however provides an offset that is near to $6.2 ns$ (90°) instead, thereby causing the injection phase to change between positive and negative interference.

The $|i_M|$ behaviour in Figure 4.6(d) can be divided into overall growth of $i_{M,env}$, shown with green arrow, and then steady value of $i_{M,env}$, shown with blue arrow. The overall $i_{M,env}$ growth occurs when the relative positive interference is more than the negative interference.

With time there is an increase in the amplitude of ϕ and this causes the growth duration in positive interference to become negligible in relative to the damp in negative interference thereby resulting in $i_{M,env}$ to appear as steady.

Based on the above discussion, we conclude that in the case of SF, continuous $i_{M,env}$ growth is observed due to the phase offset being significantly lower than 90° . This ensures continuous correction of the phase error. On the other hand, for TT, FF, and SS, they transition into a steady state $i_{M,env}$ because ϕ is close to 90° ($6.2 ns$ for $38.4 MHz$). During this period, the growth and damping of $i_{M,env}$ are approximately equal.

¹⁸ Note that the $5.7 ns$ crossing of $(\angle i_M^\circ - \angle V_{XO}^\circ)$ corresponds to the zero-phase crossing of $(\angle V_D^\circ - \angle V_{CLK}^\circ)$, shown in Figure 3.9; whereby this phase cross is detected by the Zero-phase cross detection unit.

The last $|i_M|$ behaviour of ZAC to be discussed is the damp in SS. As is the case with the phase of ϕ , the phase of ϕ_{DFF} also gradually increases with time. This increases to a point where after a zero-cross detection, an incorrect zero-phase (corresponding to 180°) is detected which then causes the frequency to get further away from f_0 instead of getting closer to it. The outcome of this is an $i_{M,env}$ drop that is also observed when a simple chirp injection's frequency gets very far from f_0 .

Despite ZAC's various effectiveness across process corners, it can be configured to produce a low average T_{start} with low variation by leveraging the closed-loop property for the selection of t_{NR} ¹⁹.

Studying Figure 4.5 for both a low $|i_M(t_{NR})|$ variation and high average $|i_M(t_{NR})|$ across process corners, 519 and 70 clock cycles after first Zero-phase cross are selected for ZAC and ZL respectively. Whereby the clock is that of VCO's which is near 38.4 MHz at first zero-phase cross. These values equate to approximately 13.5 μs and 1.8 μs after the first zero phase cross detection. The extended average injection duration of 38.6 μs by ZAC relative to 27 μs by ZL, demonstrates ZAC's ability for longer in-phase injection. Additionally, ZAC demonstrates a higher average $|i_M(t_{NR})|$, by 1.75x, and lower $|i_M(t_{NR})|$ deviation, by 3.3x.

On the other hand, open loop injections, such as chirp injections, have to preset t_{NR} with respect to the start time which would result in both high $|i_M(t_{NR})|$ variation and low average $|i_M(t_{NR})|$ across corners.

All in all, Figure 4.5 proves that ZAC ensures a more reliable $i_{M,env}$ behaviour which ensures a lower $|i_M(t_{NR})|$ variation and higher average $|i_M(t_{NR})|$ across process corners whereby based on Equation (2.4) these theoretically result to lower T_{start} variation and higher average T_{start} with

¹⁹ Note that the large phase offset shortcoming, and zero-phase detection of 180° of Zero phase implementation chirp and large t_{NR} of adaptive chirp is improved by techniques discussed in future research works in section 4.5.

respect to ZL. Additionally, it must be noted that these benefits are enabled by the phase and frequency correction properties of ZAC.

4.3 Simulated Performance of ZAC and ZL Start-up Techniques

The start-up time of the XO with ZAC and ZL compared with that of without start-up aid is shown in Figure 4.7. These results are produced at SF at 1 V and -20°C . The system start-up times decrease from $326\text{ }\mu\text{s}$ without start-up to $175\text{ }\mu\text{s}$ with the ZL start-up technique and further to $170\text{ }\mu\text{s}$ with the ZAC start-up technique.

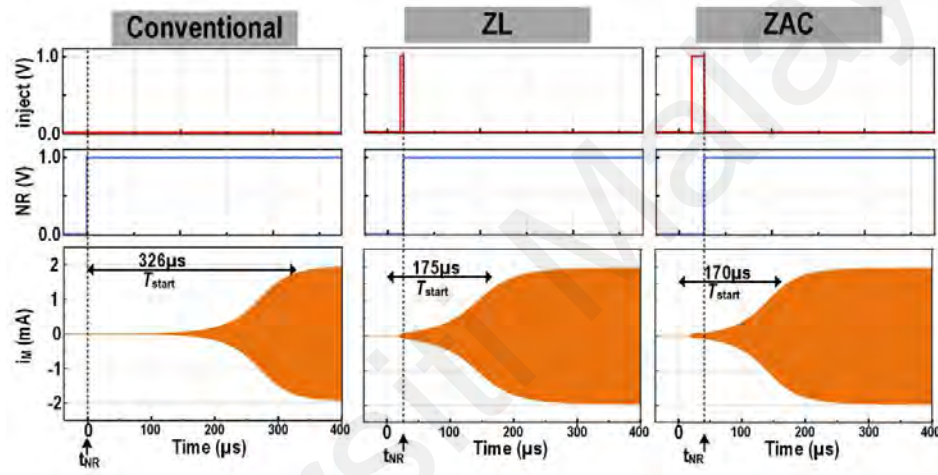


Figure 4.7: Motional current growth of 38.4 MHz resonator without start-up (left), Zero-Phase lock (middle) and the Zero-phase adaptive chirp (right).

The correlation between start-up time and $|i_M(t_{NR})|$, as expressed in Equation (2.4), informs the injection unit's efficiency. Herein, $|i_M(t_{NR})|$ will be used to assess the performance of ZAC and ZL energy injection techniques across PVT variations, while T_{start} will be used to evaluate the effectiveness of both the injection start-up reduction (for times $t < t_{NR}$) and the negative resistance start-up reduction (for times $t > t_{NR}$) when combined.²⁰

²⁰ Note that the key contribution of this thesis is the variation tolerant injection technique, namely PVT tolerance of ZAC and ZL. This is why $|i_M(t_{NR})|$ will be shown and discussed here.

Figure 4.8 illustrates ZAC's $|i_M(t_{NR})|$ across -20 to 80 °C, demonstrating a relative variation coefficient of 10.3%, with maximum and minimum $|i_M(t_{NR})|$ of 90 μA and 71 μA at -20°C and 50°C, respectively. Moreover, ZAC offers a lower average $|f_{01}-f_0|^{21}$ by 157% with respect to ZL (from 90 kHz to 35 kHz).

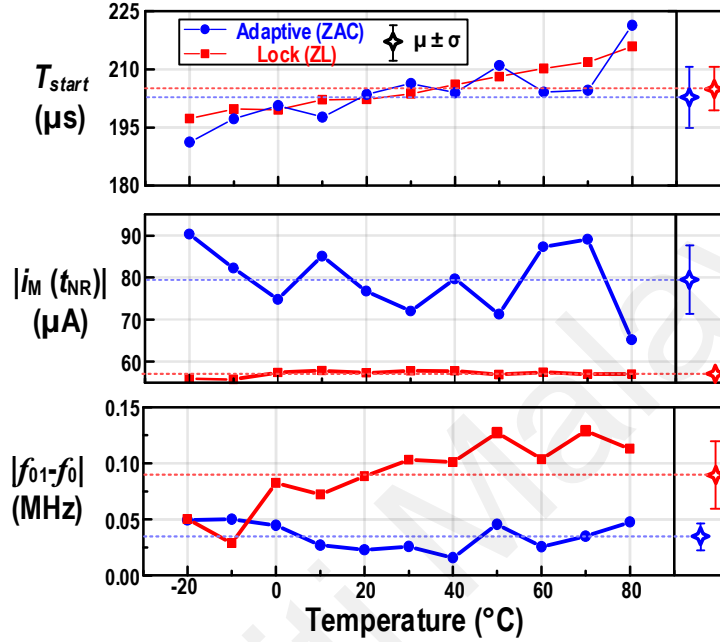


Figure 4.8: Simulated T_{start} , $|i_M(t_{NR})|$ and average frequency error against temperature variations.

The improved frequency accuracy of ZAC across temperature variations is attributable to its longer convergence duration toward f_{01} . This extended convergence duration significantly enhances ZAC's frequency detection variation tolerance by compensating for detection delays.

Figure 4.9 illustrates the start-up performance of the XO with ZAC and ZL against voltage variations (0.9 V to 1.1 V). The XO with ZAC shows a 14% relative change in $|i_M(t_{NR})|$ when the supply voltage varies by 10%, whereas that with ZL displays a higher relative variation of 18%. In addition to $|i_M(t_{NR})|$, the XO with ZAC also exhibits a lower average Δf of 35 kHz, in contrast to 113 kHz from that with ZL.

²¹ This performance parameter is further discussed in Future Works.

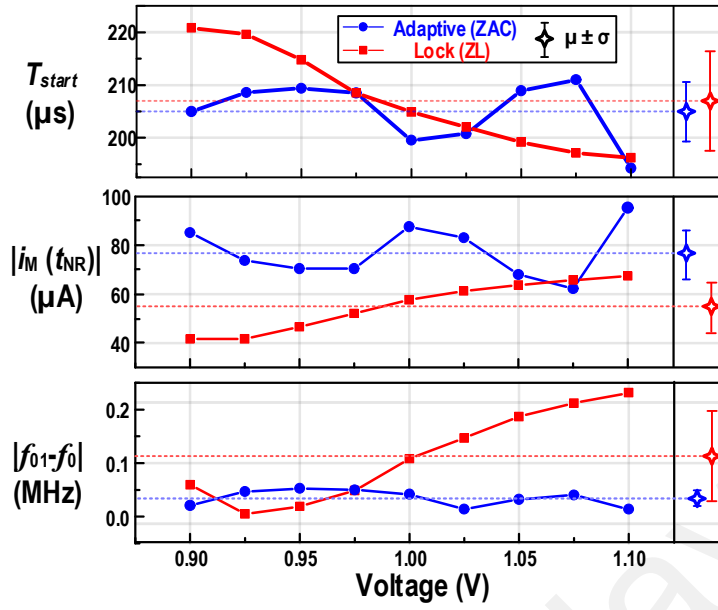


Figure 4.9: Simulated T_{start} , $|i_M(t_{NR})|$ and average frequency error against voltage variations.

The $|i_M(t_{NR})|$ response for the XOs with ZAC and ZL across process corners yields an average value of 94 μA and 54 μA , with 219 μs and 233 μs average start-up times, respectively (Figure 4.10); the fastest and slowest start-up of the XO with ZAC are at the SF and SS corners (178 μs and 308 μs). At FS despite starting with the highest initial frequency of 80 MHz (corresponding to 1.1×10^6 ppm- Δf) ZAC retains its correction property achieving 221 μs .

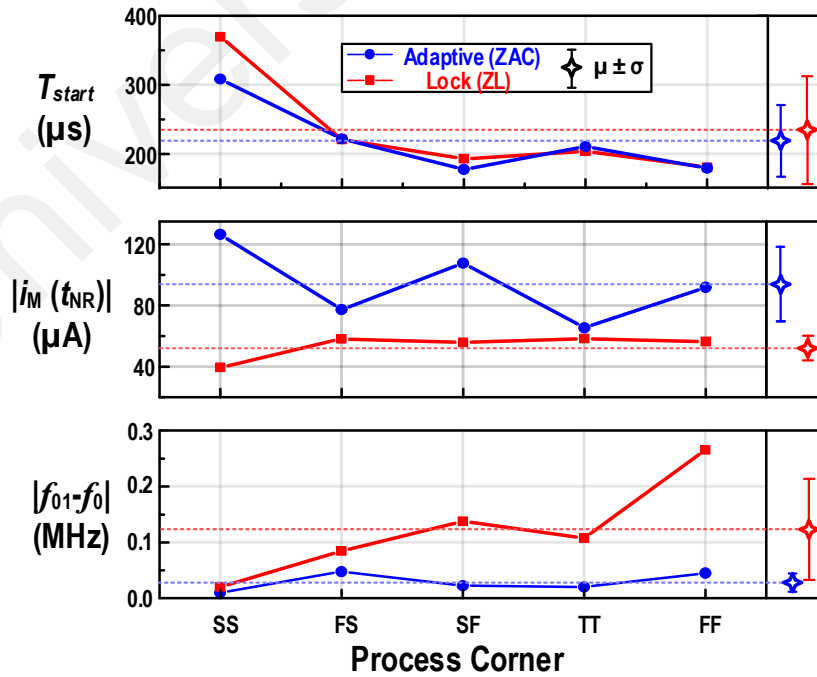


Figure 4.10: Simulated T_{start} , $|i_M(t_{NR})|$ and average frequency error against process corners.

The PVT results consistently show a higher mean (μ) of $|i_M(t_{NR})|$ for ZAC compared to ZL, indicating an improvement in ZAC's injection method. While ZL exhibits lower variation (σ) in $|i_M(t_{NR})|$ at some points, this is due to the selection of a much smaller t_{NR} , which results in a lower $|i_M(t_{NR})|$ mean. Additionally, the consistently lower mean and variation in T_{start} for ZAC suggests that its start-up function is more efficient than ZL's resonance lock injection.

Even though ZL's performance falls short of ZAC, it still shows significant enhancement over alternative resonance lock techniques as will be discussed in 4.4. These findings align with the hypothesis, demonstrating the successful achievement of all three objectives.

4.4 Discussion and Comparison to Other Proposed Works

Table 4.1 summarizes and compares the performance with prior architectures.

Table 4.1: Performance summary and comparison with prior arts.

Technique	JSSC'19 Megawer et al	ISSCC'23 Cai et al	JSSC'22 Luo et al	JSSC'16 Iguchi et al	Proposed #	
	2-step PLL Injection	Automatic Phase-Error Correction	IGCI + Boosted R_n	Chirp + Boosted R_n	Zero-Phase Lock	Zero-Phase Adaptive Chirp
Technology (nm)	65	40	22	180	65	
Resonator Frequency (MHz)	54	16	38.4	39.25	38.4	
Steady state Voltage/ Supply voltage (V)	0.5/1.0	0.25/1.0 [†]	0.8/1.0	1.4/1.5	0.95/1.0	
PVT Tolerant Injection	NO	NO	YES	YES	YES	YES
Frequency Mismatch Tolerance (ppm- Δf)	5×10^3	10^4	4.7×10^4 [†]	1.25×10^6 [*]	1.1×10^6 [*]	
$\Delta T_{start}/T_{start}$ over Temp _{range}	1.25%	4.5%	26% [†]	7%	3% [*]	3.8%
Load Cap (pF)	6	6	3.75	6	14	
T_{start} (μs)	19	17.5	58	158	175	170
E_{start} (nJ)	34.9	9.2	45.6	349	107	99
Steady State Power (μW)	198	84	800	181	450	
Temperature Range ($^{\circ}C$)	-40 to 85	-20 to 85	-40 to 40 [†]	-30 to 125	-20 to 80	

Simulated Results.

[†] Value obtained from visual inspection of figures.

^{*} Value obtained for corner case with highest value.

^{*} Achieved low variation at cost of lower $|i_M(t_{NR})|$

simulation results for best corner (SF@-20 $^{\circ}C$)

The proposed zero-phase adaptive chirp injection technique supplements the PVT tolerant injection XO start-up methods by Luo et al (2022) and Iguchi et al (2016), enhancing them by providing an exceptional frequency mismatch tolerance of 1.1×10^6 ppm- Δf . While the proposed technique falls 12% short of the frequency mismatch tolerance achieved by the

technique cited by Iguchi (2016), it compensates with superior $3.5\times$ lower start-up energy consumption (E_s). The robustness from Iguchi (2016) and the proposed injection are attributed to the inherent chirping mechanism used. IGCI (Luo et al., 2022), also employing a chirping mechanism, enables quicker PVT-tolerant start-up with respect to ZAC by utilizing a reduced C_L and lower steady-state voltages. However, with reduced C_L and steady state voltage the IGCI technique would entail an inherently higher oscillator phase noise cost (Vittoz et al., 1988), whereas the proposed design could demonstrate a superior performance. Moreover, owing to ZAC's correction property, which mitigates the error induced by the resonance frequency detector, the start-up variation across the temperature range is $7\times$ superior to that of IGCI's. Lastly and most importantly, despite the use of variation tolerant chirping, IGCI relies on a variation prone voltage reference for resonance detection. In contrast, the proposed resonance detector, namely zero-phase cross detection unit, is tolerant to variations as is evident from Figure 4.3.

Regardless of the higher power consumption and longer start-up relative to other techniques, this investigative work proposed and verified ZAC's Δf and ϕ correcting injection which showcases potential in PVT robust start-up time reduction.

4.5 Future Works

While the current implementation of ZAC and ZL successfully delivers the promised PVT-tolerant injection, there is still room for further improvements as will be discussed below.

Increase Injection Voltage Swing: For full exploitation of ZAC and ZL with higher resonator excitation, optimization for system with higher injection voltage swing may be planned. For a given supply voltage, enhancing the injection voltage swing can be achieved by reducing the buffer output impedance, R_s , or by detaching C_{L1} after the first zero-phase detection. The increased voltage swing is to be enabled after the first zero-phase detection to ensure lower power consumption before this event as well as ensuring a large delay for the zero-phase cross-detection unit's trigger. The relationship between effectiveness of proposed resonance detector with injection voltage swing is a similar relationship as that of the resonance

detector in IGCI (Luo et al., 2022). Note that while ZL can fully benefit from peak-to-peak voltage swing after first zero-phase cross detection due to its open loop nature, ZAC on the other hand would require a slightly lower voltage swing to ensure enough delay between V_{XO+} and V_{XO-} to be detected by the zero-phase cross detection unit. Nevertheless, the current implementation uses 150 mV peak-to-peak whereby based on macro-model simulations, 800mV peak-to-peak will still permit effective operation of the zero-phase cross detection.

Additionally, instead of constant frequency injection of ZL or closed loop injection of adaptive chirp upon zero-phase cross detection, we may utilize the open loop dithering injection – namely zero-phase dithering. Unlike typical dithering injection, zero-phase dithering would ensure that the toggled frequencies are close to and about the resonance frequency ensuring an effective excitation of i_M . Similar to ZL, the open-loop nature of dithering injection enables the utilization of the full voltage swing for injection without the power losses associated with the zero-phase cross detection unit. Additionally, zero-phase dithering, akin to the ZAC method, can facilitate phase correction, provided that the design carefully considers the toggling frequencies and the duration of their injection.

It must be noted that ZAC has the ability to correct phase and frequency even at such low voltages as 150mV peak-to-peak. Such feature may be utilized for lower supply voltage systems to effectively and reliably reduce the start-up time. Such technique may be an improvement in the variation tolerant start-up techniques such as the self-reference chirp injection (Lei et al., 2018) operating at as low as 0.5 V.

Lower Steady State Power Consumption: A lower steady-state power consumption can be achieved via optimization for a system with lower bias current Pierce oscillator and/or utilizing of amplitude control circuitry to reduce the oscillation voltage swings (Esmacelzadeh & Pamarti, 2017, 2018; Luo et al., 2022; Verhoef et al., 2019).

Phase Offset: As previously discussed, in the context of ZAC, the near 90° phase offset causes the growth of i_M to diminish due to the decreasing positive interference relative to

negative interference. To address this issue, the phase offset can be periodically corrected using a 90° phase shifter (illustrated in Figure 4.11).

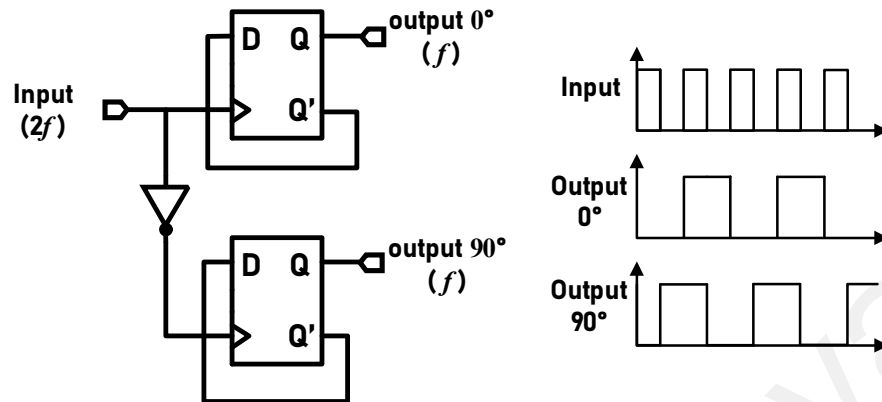


Figure 4.11: A 90° phase shifter using D-FFs

The periodic compensation mechanism, as illustrated in Figure 4.12, operates by detecting when the current i_M reaches a steady state, which is identified using a preset counter. Upon reaching this steady state, the injection buffer shifts by 90° , effectively correcting the near 90° phase error.

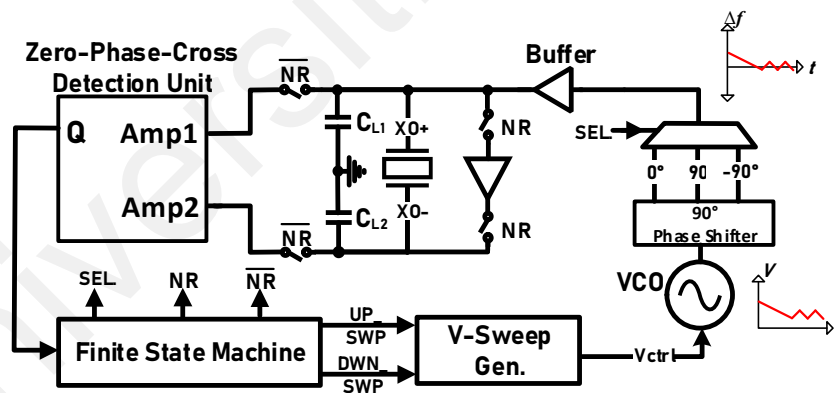


Figure 4.12: ZAC with periodic 90° phase compensation to ensure continuous motional current growth despite the phase offset error by Zero-phase cross detection unit.

This technique is similar to multi-phase injection (Karimi-Bidhendi & Heydari, 2020) with the enhanced feature of using a “detector” to determine the phase shift timing instead of a predetermined time with respect to the starting of injection.

An alternative approach to compensate for this near 90° phase offset error is by only responding to every second zero-phase cross instead of every single zero-phase cross. This

approach would cause oscillation between 90° and -90° phases difference. This approach in contrast to the precious mentioned approach would ensure continuous adaptive chirp without any concerns regarding detection of the “wrong” zero-phase cross.

Lower Zero-phase Cross Detection Power Consumption: The two self-biased inverter amplifiers in zero-phase cross detection unit may be replaced with dynamic comparators biased by resistors. The comparators would compare the V_{XO+} and V_{XO-} signals to the bias voltage. This implementation would reduce the PVT variations of the amplifier gain as well as reduce the power consumption.

Utilizing ZAC’s Low Frequency Mismatch for Subsequent Start-ups: as is evident from results in Figure 4.8 to Figure 4.10, the injection frequency of ZAC becomes very close to that of resonance at the end of injection. Given that the injection frequency is stored as voltage in a capacitor and that the IoT nodes are expected to have heavy duty cycling, the stored “frequency” may be used for subsequent start-up events. This approach would reduce the start-up time associated with process variation. To ensure that this stored frequency retains near resonance despite a change in voltage or temperature, the charge redistribution technique (Kugelstadt, 2000) may be used to increase the stored voltage, and hence increase the frequency, before the next start-up event is started.

CHAPTER 5: CONCLUSION

The rapid increase in battery-powered wireless sensor nodes necessitates reducing both operational and manufacturing costs. To minimize battery replacement expenses associated with operational cost, these devices operate in burst mode to conserve power and increase operation life. However, frequent power cycling can still cause significant energy consumption, primarily due to the slow start-up of the crystal oscillator (XO). Therefore, for an effective burst mode operation, a fast XO start-up is required. Additionally, cost-effective manufacturing demands a consistent and process variation-tolerant XO start-up without relying on costly post-fabrication trimming. To ensure transmission reliability between wireless sensor nodes, aside from process variation, it is also important to minimize the impact of voltage and temperature variations on start-up, ensuring that nodes awaken for transmission at similar times during bursts.

This thesis addresses these challenges by designing and analyzing two fast-start-up XO techniques with minimal PVT (Process, Voltage, Temperature) variations and no post-fabrication trimming: Zero-Phase Lock (ZL) and Zero-Phase Adaptive Chirp (ZAC). Both techniques employ chirp injection to ensure PVT tolerance. ZL reduces start-up time compared to conventional chirp injection by using a zero-phase cross detection unit to lock onto the resonance frequency. ZAC further reduces start-up time by using the same unit for phase correction through adaptive chirping around the resonance frequency. Unlike conventional chirp injection methods, which suffer from low energy injection efficiency due to wide frequency band coverage, these proposed techniques improve energy injection efficiency by targeting the resonance frequency. This approach enhances energy injection efficiency while preserving the trim-less operation characteristic of chirp injection. The reduction in the chip area, achieved by eliminating the need for trimming,

along with the elimination of associated labor costs, leads to the savings in manufacturing expenses.

The operation of both ZL and ZAC has been theoretically validated through mathematical analysis and macro-model implementations, fulfilling the first objective of this thesis. Post-layout simulations in a 65-nm CMOS process were conducted to verify their operation. The results demonstrate that ZL effectively functions as a low-power resonance lock injection method without a variation-prone voltage reference, meeting the second objective. ZL is more power-efficient compared to its Impedance Guided Chirp Injection (IGCI) counterpart, as it eliminates the need for a power-hungry comparator or voltage reference. ZAC successfully implements the proposed phase correction on top of the resonance lock injection technique, consistently reducing start-up time across variations, thus fulfilling the third objective.

Both ZL and ZAC exhibit state-of-the-art performance, achieving fast start-up times of 175 μs and 170 μs , respectively, and exceptional temperature variation tolerance with start-up time variations of just 3.8% and 3.0%, respectively, without post-fabrication trimming.

Despite the successes of ZL and ZAC in achieving PVT-tolerant fast start-up, there is still potential for improvement. For instance, increasing the injection swing voltage could enhance the motional current magnitude $|i_M(t_{NR})|$, further reducing start-up time (T_{start}). Additionally, the growth stage of the motional current under ZAC could be optimized through injection phase offset correction, potentially using a 90° phase shifter or varying the injection phase between -90° and 90° . A further promising aspect of ZAC is its potential to reduce the impact of process variations in subsequent start-up events due to minimal injection frequency mismatch and capacitive storage of the injection frequency.

These innovative approaches represent significant advancements in crystal oscillator start-up, offering enhanced robustness to PVT variations.

Universiti Malaya

REFERENCES

- Antonopoulos, A., Volanis, G., Lu, Y., & Makris, Y. (2019). Post-Production Calibration of Analog/RF ICs: Recent Developments and A Fully Integrated Solution. *2019 16th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, 77–80. 2019 16th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD). <https://doi.org/10.1109/SMACD.2019.8795278>
- Babayan-Mashhadi, S., & Lotfi, R. (2014). Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 22(2), 343–352. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. <https://doi.org/10.1109/TVLSI.2013.2241799>
- Bahai, A. (2016). Ultra-low Energy systems: Analog to information. *2016 46th European Solid-State Device Research Conference (ESSDERC)*, 3–6. <https://doi.org/10.1109/ESSDERC.2016.7599575>
- Brown, S. D., & Vranesic, Z. G. (2014). *Fundamentals of digital logic with Verilog design* (Third edition). McGraw-Hill Higher Education.
- Cai, Z., Wang, X., Wang, Z., Yin, Y., Zhang, W., Xu, T., & Guo, Y. (2023). 3.7 A 16MHz X0 with 17.5 μ s Startup Time Under 104ppm- Δ F Injection Using Automatic Phase-Error Correction Technique. *2023 IEEE International Solid- State Circuits Conference (ISSCC)*, 2–4. <https://doi.org/10.1109/ISSCC42615.2023.10067675>
- Chen, C.-W., Hung, C.-C., & Hsueh, Y.-L. (2023). A Fast-Startup 80MHz Crystal Oscillator with 96x/368x Startup-Time Reductions for 3.0V/1.2V Swings Based

on Un-interrupted Phase-Aligned Injection. *2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 113–116.
<https://doi.org/10.1109/RFIC54547.2023.10186129>

Ding, M., Liu, Y.-H., Harpe, P., Bachmann, C., Philips, K., & Van Roermund, A. (2019). A Low-Power Fast Start-Up Crystal Oscillator With an Autonomous Dynamically Adjusted Load. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 66(4), 1382–1392. <https://doi.org/10.1109/TCSI.2018.2880282>

Esmaelzadeh, H., & Pamarti, S. (2017). A precisely-timed energy injection technique achieving 58/10/2 μ s start-up in 1.84/10/50MHz crystal oscillators. *2017 IEEE Custom Integrated Circuits Conference (CICC)*, 1–4.
<https://doi.org/10.1109/CICC.2017.7993605>

Esmaelzadeh, H., & Pamarti, S. (2018). A Quick Startup Technique for High- Q Oscillators Using Precisely Timed Energy Injection. *IEEE Journal of Solid-State Circuits*, 53(3), Article 3. <https://doi.org/10.1109/JSSC.2017.2766208>

Ginosar, R. (2011). Metastability and Synchronizers: A Tutorial. *IEEE Design & Test of Computers*, 28(5), 23–35. *IEEE Design & Test of Computers*.
<https://doi.org/10.1109/MDT.2011.113>

Griffith, D., Murdock, J., & Roine, P. T. (2016). 5.9 A 24MHz crystal oscillator with robust fast start-up using dithered injection. *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 104–105.
<https://doi.org/10.1109/ISSCC.2016.7417928>

Iguchi, S., Fuketa, H., Sakurai, T., & Takamiya, M. (2016). Variation-Tolerant Quick-Start-Up CMOS Crystal Oscillator With Chirp Injection and Negative Resistance

Booster. *IEEE Journal of Solid-State Circuits*, 51(2), 496–508.
<https://doi.org/10.1109/JSSC.2015.2499240>

Iguchi, S., Sakurai, T., & Takamiya, M. (2017). A Low-Power CMOS Crystal Oscillator Using a Stacked-Amplifier Architecture. *IEEE Journal of Solid-State Circuits*, 52(11), 3006–3017. *IEEE Journal of Solid-State Circuits*.
<https://doi.org/10.1109/JSSC.2017.2743174>

Karimi-Bidhendi, A., & Heydari, P. (2020). A Study of Multi-Phase Injection on Accelerating Crystal Oscillator Start-Up. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 67(12), 2868–2872.
<https://doi.org/10.1109/TCSII.2020.2978097>

Karimi-Bidhendi, A., Pu, H., & Heydari, P. (2019). Study and Design of a Fast Start-Up Crystal Oscillator Using Precise Dithered Injection and Active Inductance. *IEEE Journal of Solid-State Circuits*, 54(9), Article 9.
<https://doi.org/10.1109/JSSC.2019.2920084>

Kim, B., Hopcroft, M. A., Candler, R. N., Jha, C. M., Agarwal, M., Melamud, R., Chandorkar, S. A., Yama, G., & Kenny, T. W. (2008). Temperature Dependence of Quality Factor in MEMS Resonators. *Journal of Microelectromechanical Systems*, 17(3), 755–766. *Journal of Microelectromechanical Systems*.
<https://doi.org/10.1109/JMEMS.2008.924253>

Kim, M.-Y., Lee, H., & Kim, C. (2012). PVT Variation Tolerant Current Source With On-Chip Digital Self-Calibration. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 20(4), 737–741. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. <https://doi.org/10.1109/TVLSI.2011.2109971>

- Kruiskamp, W. (2022). A Fully Differential 40 MHz Switched-Capacitor Crystal Oscillator with Fast Start-Up. *ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC)*, 397–400.
<https://doi.org/10.1109/ESSCIRC55480.2022.9911475>
- Kugelstadt, T. (2000). The operation of the SAR-ADC based on charge redistribution. *CC*.
- Kundu, S., Huusari, T., Luo, H., Agrawal, A., Alban, E., Shahraini, S., Xiong, T., Lake, D., Pellerano, S., Mix, J., Kurd, N., Abdel-moneum, M., & Carlton, B. (2022). A 2-to-2.48GHz Voltage-Interpolator-Based Fractional-N Type-I Sampling PLL in 22nm FinFET Assisting Fast Crystal Startup. *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, 144–146.
<https://doi.org/10.1109/ISSCC42614.2022.9731560>
- Lechevallier, J. B., Bindra, H. S., van der Zee, R. A. R., & Nauta, B. (2021). Energy Efficient Startup of Crystal Oscillators Using Stepwise Charging. *IEEE Journal of Solid-State Circuits*, 56(8), 2427–2437.
<https://doi.org/10.1109/JSSC.2021.3061032>
- Lechevallier, J. B., Van Der Zee, R. A. R., & Nauta, B. (2019). Fast & Energy Efficient Start-Up of Crystal Oscillators by Self-Timed Energy Injection. *IEEE Journal of Solid-State Circuits*, 54(11), Article 11.
<https://doi.org/10.1109/JSSC.2019.2933143>
- Leeson, D. B. (2016). Oscillator Phase Noise: A 50-Year Review. *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, 63(8), 1208–1225. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control.
<https://doi.org/10.1109/TUFFC.2016.2562663>

Lei, K.-M., Mak, P.-I., Law, M.-K., & Martins, R. P. (2018). A Regulation-Free Sub-0.5-V 16-/24-MHz Crystal Oscillator With 14.2-nJ Startup Energy and 31.8- μ W Steady-State Power. *IEEE Journal of Solid-State Circuits*, 53(9), 2624–2635.
<https://doi.org/10.1109/JSSC.2018.2849012>

Lei, K.-M., Mak, P.-I., & Martins, R. P. (2021). Startup Time and Energy-Reduction Techniques for Crystal Oscillators in the IoT Era. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 68(1), 30–35.
<https://doi.org/10.1109/TCSII.2020.3040419>

Li, D., Chuang, P., & Sachdev, M. (2010). Comparative analysis and study of metastability on high-performance flip-flops. *2010 11th International Symposium on Quality Electronic Design (ISQED)*, 853–860.
<https://doi.org/10.1109/ISQED.2010.5450482>

Li, H., Lei, K.-M., Mak, P.-I., & Martins, R. P. (2023). 3.6 A 12/13.56MHz Crystal Oscillator with Binary-Search-Assisted Two-Step Injection Achieving 5.0nJ Startup Energy and 45.8 μ s Startup Time. *2023 IEEE International Solid- State Circuits Conference (ISSCC)*, 64–66.
<https://doi.org/10.1109/ISSCC42615.2023.10067401>

Li, H., Lei, K.-M., Martins, R. P., & Mak, P.-I. (2023). A 12-/13.56-MHz Crystal Oscillator With Binary-Search-Assisted Two-Step Injection Achieving 5.0-nJ Startup Energy and 45.8- μ s Startup Time. *IEEE Journal of Solid-State Circuits*, 1–12. *IEEE Journal of Solid-State Circuits*.
<https://doi.org/10.1109/JSSC.2023.3300589>

Li, H., Lei, K.-M., Martins, R. P., & Mak, P.-I. (2024). A 12-/13.56-MHz Crystal Oscillator With Binary-Search-Assisted Two-Step Injection Achieving 5.0-nJ

Startup Energy and 45.8- μ s Startup Time. *IEEE Journal of Solid-State Circuits*, 59(2), 464–475. IEEE Journal of Solid-State Circuits. <https://doi.org/10.1109/JSSC.2023.3300589>

Loo, M. H.-W., Ramiah, H., Lei, K.-M., Lim, C. C., Mak, P.-I., & Martins, R. P. (2017). *Fully-Integrated Timers for Ultra-Low-Power Internet-of-Things Nodes – A Review*. 15.

Luo, H., Kundu, S., Huusari, T., Shahraini, S., Alban, E., Mix, J., Kurd, N., Abdel-Moneum, M., & Carlton, B. (2022). A Fast Startup Crystal Oscillator Using Impedance Guided Chirp Injection in 22 nm FinFET CMOS. *IEEE Journal of Solid-State Circuits*, 57(3), 688–697. <https://doi.org/10.1109/JSSC.2021.3136237>

Manuzzato, A., Campi, F., Rossi, D., Liberali, V., & Pandini, D. (2013). Exploiting body biasing for leakage reduction: A case study. *2013 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 133–138. <https://doi.org/10.1109/ISVLSI.2013.6654635>

Megawer, K. M., Pal, N., Elkholy, A., Ahmed, M. G., Khashaba, A., Griffith, D., & Hanumolu, P. K. (2019). A Fast Startup CMOS Crystal Oscillator Using Two-Step Injection. *IEEE Journal of Solid-State Circuits*, 54(12), 3257–3268. <https://doi.org/10.1109/JSSC.2019.2936296>

Miyahara, M., Endo, Y., Okada, K., & Matsuzawa, A. (2018). A 64 μ s Start-Up 26/40MHz Crystal Oscillator with Negative Resistance Boosting Technique Using Reconfigurable Multi-Stage Amplifier. *2018 IEEE Symposium on VLSI Circuits*, 115–116. <https://doi.org/10.1109/VLSIC.2018.8502281>

Nise, N. S. (2020). *Control Systems Engineering*. John Wiley & Sons.

- Ohira, T. (2005). Rigorous Q-factor formulation for one- and two-port passive linear networks from an oscillator noise spectrum viewpoint. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 52(12), 846–850. *IEEE Transactions on Circuits and Systems II: Express Briefs*. <https://doi.org/10.1109/TCSII.2005.853343>
- Oller, J., Demirkol, I., Casademont, J., Paradells, J., Gamm, G. U., & Reindl, L. (2016). Has Time Come to Switch From Duty-Cycled MAC Protocols to Wake-Up Radio for Wireless Sensor Networks? *IEEE/ACM Transactions on Networking*, 24(2), 674–687. <https://doi.org/10.1109/TNET.2014.2387314>
- Park, J.-H., Shin, Y., Choi, J., & Kim, S.-J. (2021). A 5.02nW 32-kHz Self-Reference Power Gating XO With Fast Startup Time Assisted by Negative Resistance and Initial Noise Boosters. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 68(11), 3386–3390. <https://doi.org/10.1109/TCSII.2021.3077589>
- Piezoelectric Effect*. (n.d.). Retrieved May 6, 2024, from <https://reviseomatic.org/help/e-components/Piezoelectric%20Effect.php>
- Rohde, U. L., & Poddar, A. K. (2010). Electromagnetic interference and start-up dynamics in high frequency crystal oscillator circuits. *2010 IEEE Sarnoff Symposium*, 1–9. <https://doi.org/10.1109/SARNOF.2010.5469744>
- Rout, R. R., & Ghosh, S. K. (2013). Enhancement of Lifetime using Duty Cycle and Network Coding in Wireless Sensor Networks. *IEEE Transactions on Wireless Communications*, 12(2), 656–667. <https://doi.org/10.1109/TWC.2012.111412.112124>

- Rusznay, A. (1987). Start-up time of CMOS oscillators. *IEEE Transactions on Circuits and Systems*, 34(3), 259–268. IEEE Transactions on Circuits and Systems. <https://doi.org/10.1109/TCS.1987.1086137>
- Sedra, A. S., & Smith, K. C. (2015). *Microelectronic circuits* (Seventh edition). Oxford University Press.
- Verhoef, B., Prummel, J., Kruiskamp, W., & Post, R. (2019). 18.6 A 32MHz Crystal Oscillator with Fast Start-up Using Synchronized Signal Injection. *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, 304–305. <https://doi.org/10.1109/ISSCC.2019.8662338>
- Vertregt, M. (2006). The analog challenge of nanometer CMOS. *2006 International Electron Devices Meeting*, 1–8. <https://doi.org/10.1109/IEDM.2006.346834>
- Vittoz, E. A., Degrauwe, M. G. R., & Bitz, S. (1988). High-performance crystal oscillator circuits: Theory and application. *IEEE Journal of Solid-State Circuits*, 23(3), Article 3. <https://doi.org/10.1109/4.318>
- Wang, L., Arnold, A., Meier, J., Scholl, M., Wunderlich, R., & Heinen, S. (2021). A 55 MHz Integrated Crystal Oscillator with Chirp Injection Using a 28-nm Technology. *SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME*, 1–4.
- YXC. (n.d.). *YSX1210SL Small Size Crystal*. YSX1210SL. Retrieved May 6, 2024, from <https://image.seapx.com/mall/yangxin/3/20240301/YXC-YSX1210SL-datesheet-V2-573167.pdf>
- Zhang, Z., Yang, S., Liu, Y., Zhu, Z., Lin, J., Bao, R., Xu, T., Yang, Z., Zhang, M., Liu, J., Zhou, X., Yin, J., Mak, P.-I., & Li, Q. (2022). On the DC-Settling Process of

the Pierce Crystal Oscillator in Start-up. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 1–1. IEEE Transactions on Circuits and Systems II: Express Briefs. <https://doi.org/10.1109/TCSII.2022.3209025>

Zhou, B., Li, Y., & Wang, Z. (2024). A Fast Startup Crystal Oscillator with Digital SAR-AFC Based Two-Step Injection. *Chinese Journal of Electronics*, 33(5), 1147–1153. Chinese Journal of Electronics. <https://doi.org/10.23919/cje.2023.00.043>

Universiti Malaysia