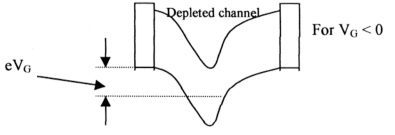


Figure 2.18 (c): The energy band profile when the gate bias is negative, so the channel is depleted. [16,18]

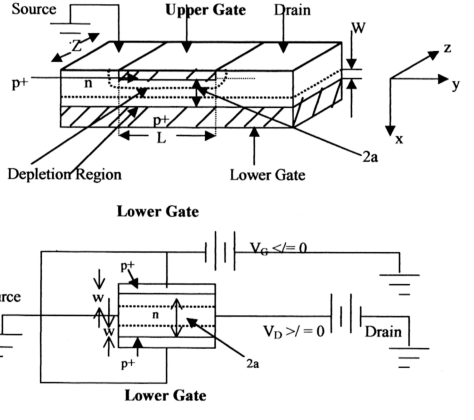


Figure 2.18 (d): The rearranged FET structure from (a). [16,18]

is shown in Figure 2.1.

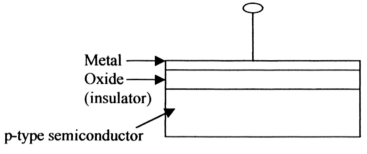
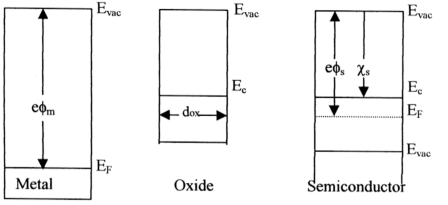


Figure 2.1: MOS capacitor structure (ideal case). [16]

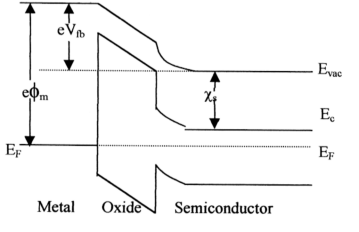
The oxide layer (e.g SiO_2) is grown on the top of p-type, n-type or polysilicon thin film and a metal contact is then deposited on the oxide. With such structure, the MOS device or MOS capacitor acts as a solid state device where a gate is isolated from semiconductor, Si by an insulator layer, SiO_2.

2.2.2 Energy Band Profile of MOS Junction

Figure 2.2 presents the band profiles of the isolated metal, oxide and semiconductor and the MOS junction. The metal and semiconductor vacuum work functions are represented by ϕ_m and ϕ_s respectively. The barrier energies of the metal and semiconductor are $e\phi_m$ and $e\phi_s$ respectively is measured from the Fermi level, E_F to the vacuum level, E_{vac}. χ_s is the semiconductor electron affinity measured from the conduction band edge, E_c to the vacuum level, E_{vac}. The flat band voltage of the MOS junction is represented by V_{fb} and d_{ox} is the thickness of oxide.



(a)



(b)

Figure 2.2: (a) Band Profiles of the isolated metal, oxide, and semiconductor. (b) Band profile of p- type MOS junction. [16]

When the metal of a MOS structure is shorted out to the semiconductor, electrons will flow from the metal to the semiconductor or vice-versa until a potential will be built up between the two which will counterbalance the different in the work function. When equilibrium is reached, the Fermi level in the metal is lined-up with the Fermi level in the semiconductor. Therefore, there will be a electrostatic potential variation from one

region to the other as illustrated in Figure 2.2 (b) for the case of an alluminium/silicon dioxide/p-type silicon junction.

When just enough gate voltage is applied to counterbalance the work function difference, ϕ_{ms}, a flat-band condition is maintained in the semiconductor. The gate voltage required to bring about the flat-band condition is called the flat-band voltage, V_{fB}. The flat-band condition can be established if $eV_{fb} = e\phi_m - \chi_s - E_c + E_F$. Thus $V_{fb} = \phi_m - \phi_s = \phi_{ms}$ (2.1)

The effects of various applied gate voltages on the energy band of an ideal p-type MOS capacitor are shown in the Figure 2.3 (a), (b) and (c).

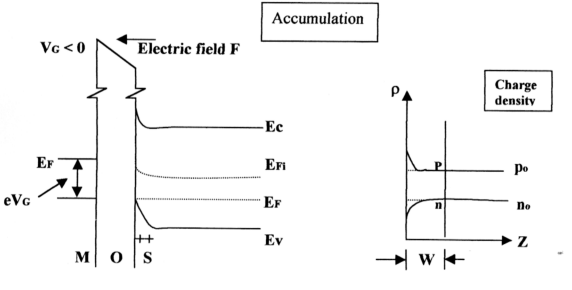


Figure 2.3 (a): Effects of a negative gate voltage on an ideal p-type MOS capacitor. [16,18]

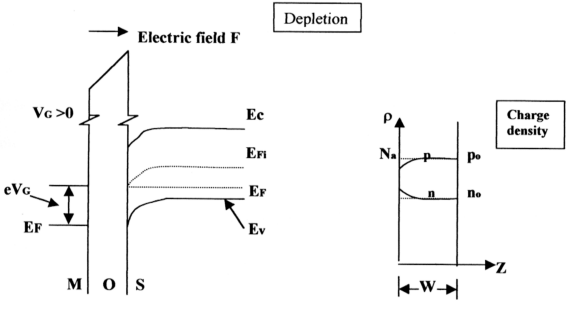


Figure 2.3 (b): Effects of a positive gate voltage on an ideal p-type MOS capacitor. [16,18]

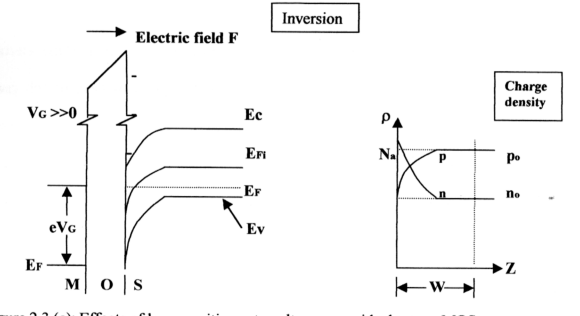


Figure 2.3 (c): Effects of large positive gate voltage on an ideal p-type MOS capacitor. [16,18]

If negative bias voltage is applied on the gate of MOS capacitor with respect to substrate, the majority carriers will "accumulate" near to semiconductor-oxide interface or channel. For p-type MOS capacitor case, the holes as a majority carrier will be attracted due to negative charges deposited on the gate. The semiconductor valence band will bend-up closer to Fermi level, causing an accumulation of holes at the interface as shown in Figure 2.3 (a). The different between the Fermi level in the metal and semiconductor is equal to eV_G, where V_G is the applied bias voltage. The holes concentration depends exponentially on the energy difference $E_i - E_F$ as in the expression below:

$$p_p = n_i e^{(E_i - E_F)/k_B T} \tag{2.2}$$

where E_i is the intrinsic level, E_F is the Fermi level, n_i is the intrinsic electron concentration, k_B is the Boltzmann constant and T is the temperature.

When a positive bias is applied on the gate of MOS capacitor, the majority carriers will "deplete" in the channel. For p-type MOS capacitor, the holes will be pushed away due to positive charges deposited on the gate. The Fermi level in the metal is lowered by eV_G with respect to the Fermi level of the semiconductor causing the valence band to move away from the semiconductor Fermi level (Figure 2.3 (b)). As a result, the density of holes near interface (or channel) falls below the bulk value in the p-type MOS. The space charge per unit area Q_{sc} in the semiconductor is given by the charge in the depletion region

$$Q_{sc} = -qN_A W \tag{2.3}$$

where W is a width of the surface depletion region.

If positive voltage is increased further, the layer of minority carriers forms an inversion surface charge. In terms of band energy, the conduction band at the oxide-semiconductor will bend down further close to the Fermi level in the semiconductor as shown in Figure 2.3 (c). The significant increase in the electron density will result in an electrical property of n-type semiconductor. For the case of p-type MOS, the electron density (minority carriers) will increase until the n-channel is formed. The width of the inversion region is typically from 10A° to 100A°. The electron concentration depends exponentially on the energy difference $E_F - E_i$ as in the expression below:

$$n_p = n_i e^{(E_F - E_i)/k_B T} \tag{2.4}$$

Under strong inversion condition the charge per unit area in the semiconductor is given by

$$Q_s = Q_n + Q_s \tag{2.5}$$

and, $$Q_{sc} = -qN_A W_m \tag{2.6}$$

where W_m is the maximum width of the surface depletion region.

It is important to note here that, the n-type behavior is not produced by doping the semiconductor but is produced by "inverting" the bands using an external bias. A very high carrier density can be induced if an insulator has a large band gap and has a good quality interface with the semiconductor.

Inversion regime is important in the gate switching of active devices such as MOSFET, power MOSFET, etc. As such, the quantitative details will be examined here. The band bending is described by the quantity $e\phi_s$, which measures the position of the

intrinsic Fermi level with respect to the bulk intrinsic Fermi level as shown in Figure 2.4. Therefore, when surface potential $e\phi_s = 0$, the band are flats. When $e\phi_s > 0$, the interface is in depletion and when $e\phi_s >> 0$, the interface is in inversion for the p-type MOS structure. The interface potential for inversion must satisfy the condition $\phi_s = 2\phi_F$ as illustrated in Figure 2.4.

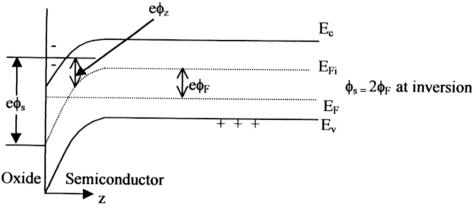


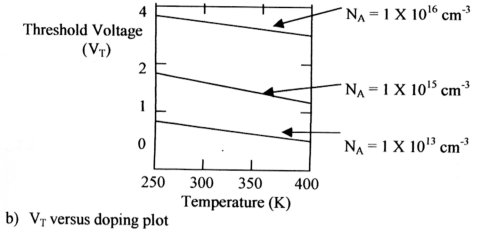
Figure 2.4: The band bending of semiconductor in inversion mode where the interface potential for inversion is given by this condition, $\phi_s = 2\phi_F$. [20,23]

2.2.3 MOS Characteristics

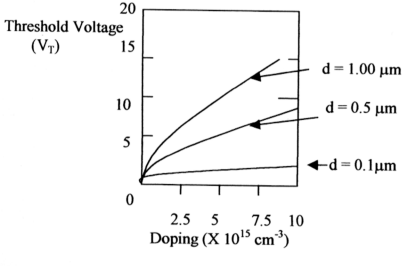
2.2.3-1 Threshold Voltage

The threshold voltage is the value of gate voltage which current just starts to flow between the drain to source in the MOSFET [17] or the gate voltage needed to cause inversion in the channel of MOS capacitor.

a) V_T versus temperature plot



b) V_T versus doping plot



c) V_T versus insulator thickness.

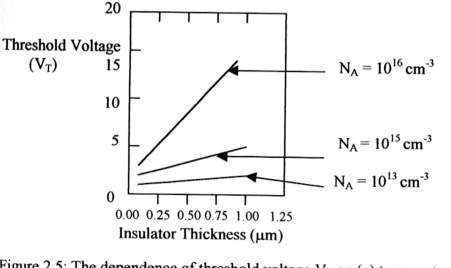


Figure 2.5: The dependence of threshold voltage V_T on (a) temperature, (b)doping level, and (c) insulator thickness. [17]

The presence of interface traps (due to defects) has significant effects on the threshold voltage (V_T). The traps will have an additional charge and will cause a voltage drop across an insulator. The voltage drop will cause a shift in the threshold voltage.

2.2.3-2 Capacitance-Voltage (C-V_G)

The measurement of capacitance-voltage is done by applying the dc bias and plus a small ac signal about 5-10 mV super imposed [5,15] to the gate of MOS device to obtain the capacitance at the bias voltage. The C-V characteristics provide an important characterization tool to check on the quality of the MOS structure [1]. The capacitance of the MOS structure is the series combination of the oxide capacitance C_{ox} and the semiconductor capacitance C_s as shown in Figure 2.6.

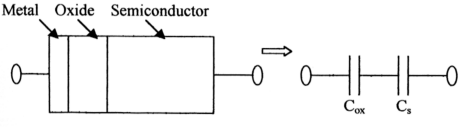


Figure 2.6: An equivalent simple circuit for MOS device. [16,17]

The semiconductor capacitance is

$$C_s = dQ_s / dV_s \tag{2.7}$$

and the total MOS capacitance is

$$C_{mos} = C_{ox} C_s / [C_{ox} + C_s] \tag{2.8}$$

where the capacitance values discussed are capacitance per unit area.

The three important regimes of accumulation, depletion, and inversion (as discussed in earlier section 2.2.2) are reflected in the C-V characteristics as shown in Figure 2.7. In the accumulation region ($-V_G$), the holes accumulate at the surface and C_s is much larger than C_{ox}. This is because a small change in bias causes a large change in Q_s in the accumulation regime. The MOS capacitance in equation 2.38 then become

$$C_{mos} \cong C_{ox} = \varepsilon_{ox} / d_{ox} \tag{2.9}$$

When the bias voltage is positive, the channel is depleted of holes. The depletion capacitance is given by ε_s / W, and total MOS capacitance in equation 2.8 becomes

$$C_{mos} = C_{ox} / [1 + C_{ox} / C_s] = \varepsilon_{ox} / [d_{ox} + \varepsilon_{ox} W / \varepsilon_s] \tag{2.10}$$

where W is a depletion width of the channel.

The value of C_{mos} in equation 2.10 decreases as more holes are depleted when the positive biasing applied increases (Figure 2.7) to a point zero free carrier density.

When the depletion width reaches a maximum value, the minimum capacitance is given by the equation

$$C_{mos}\,(min) = \varepsilon_{ox} / [d_{ox} + \varepsilon_{ox} W_{max} / \varepsilon_s] \tag{2.11}$$

where W_{max} is the maximum depletion width.

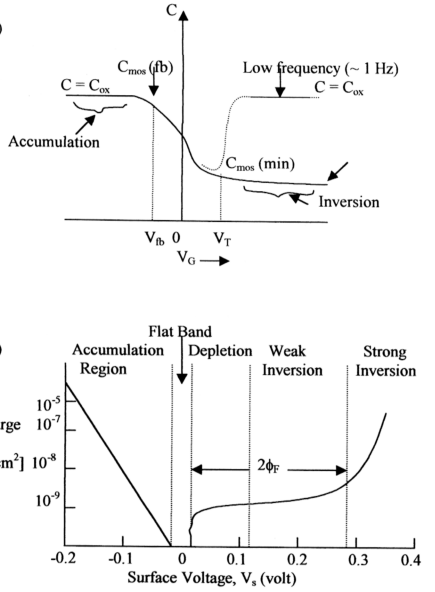


Figure 2.7: (a) The MOS capacitance dependence on bias voltage. The curve (i) is for low frequency measurement and the curve (ii) is for high frequency measurement.
(b) The MOS charge density $|Q_s|$ dependence on the surface potential V_s in various regions i.e Accumulation, Flat Band, Depletion, Weak Inversion and Strong Inversion. [16]

If the bias voltage is further increased i.e V_G is equal or larger than V_T, the electrons start to collect in inversion region and the depletion width, W_{max} remains unaltered with bias. For low frequency measurement (1 Hz), the small change in surface voltage, V_s causes a large change in Q_s and the total MOS capacitance is returned towards the same value of C_{ox}

$$C_{mos}(inv) = C_{ox} = \varepsilon_{ox} / d_{ox} \tag{2.12}$$

While for high frequency measurement (1 kHz), the total capacitance C_{mos} remains at the value $C_{mos}(min)$ as in equation 2.11.

At flat band region, the small change $\delta V(z)$ of potential produces charge density

$$\delta(z) = p_o [\exp (e\delta V(z)/k_B T) - 1] \sim e\delta V(z)\, p_o / k_B T \tag{2.13}$$

where p_o is the hole density at the flat band. After solving the Poisson equation, this result the semiconductor capacitance

$$C_s = \varepsilon_s / [(k_B T/e) \times (\varepsilon_s / e N_a)]^{1/2} \tag{2.14}$$

Therefore, the MOS capacitance at flat band is given by

$$C_{mos}(fb) = \varepsilon_{ox} / \{ d_{ox} + \varepsilon_{ox} / \varepsilon_s [(k_B T/e) \times (\varepsilon_s / eN_a)] \} \tag{2.15}$$

2.2.3-3 Non-Ideal MOS Structure

Figure 2.8 shows the different charges present in the non-ideal MOS gate structure. All these charges such as Mobile Ionic Charge, Fixed Oxide Charge, Interface Trap Density and Oxide Trapped Charge are defects in MOS gate structure. Mobile Ionic Charges (Q_m), is an ionic contamination of monovalent ions such as Na+, K+, etc are able to move in the oxide layer at various temperatures. Fixed oxide charges Q_f, normally

located at or near the silicon-silicon dioxide interface. Interface Traps Density (interface states or interface trapped-charges) Q_{it}, can exchange charge with silicon as a function of applied gate bias. Oxide Trapped Charges, Q_{ot} which are created by radiation of X-Ray or hot electron injection will be distributed inside the oxide layer.

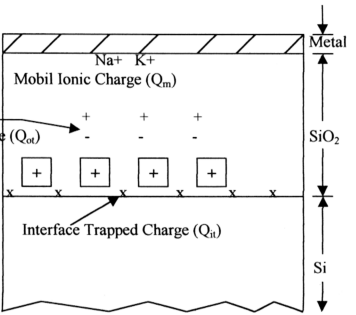


Figure 2.8: The terminology for charges associated with thermally oxidized silicon. [18,19]

(a) Mobile Ionic Charge, Q_m

The main influence of sodium ions Na+ on MOSFET characteristic is to alter the threshold voltage [18,20,24]. The effects is more pronounced in n-channel devices than p-channel because the gate bias for n-channel is positive, driving sodium ions from the metal-SiO_2 to Si-SiO_2 interface (or channel). Sodium ions, Na+ in the gate oxide will cause a shift in Capacitance-Voltage signals. The amount of ions is variable from device to device and it moves around in the oxide, causing a long-term instability in the device threshold.

The flat-band shift due to an arbitrary charge density distribution can be calculated from the expression

$$V_{FB},shift = -1/\varepsilon_{ox} \int_0^{t_{ox}} x\ \rho(x)\, dx \qquad (2.16)$$

where $\rho(x)$ is an arbitrary charge density (charges cm^{-3}) , x is the charge distance inside of gate oxide from the metal-oxide interface , t_{ox} is the gate oxide thickness i.e distance from metal-oxide interface to oxide-semiconductor interface, and ε_{ox} is the gate oxide permeability constant.

From the above equation 2.16, if a negative bias is applied to the gate, all positives ions in the oxide will be pushed to the metal-oxide interface (i.e x = 0), the flat band voltage is zero. If positive biased is applied to the gate, all positive sodium ions will be moved to Si-SiO_2 interface (i.e $x = t_{ox}$).

Other alkali ions such as lithium and potassium can also results in ionic contamination but sodium ions are the most common one. The sodium ions [20] can be introduced into the oxide during gate processing or contact metallization, oxidation and high temperature annealing, high temperature processes such as diffusion and photoresist bake, chemical reagents used in cleaning and general handling of samples either direct or indirect contact with body salt.

(b) Fixed oxide charge, Q_f

The fixed oxide charge Q_f is located within approximately 30A° of the Si-SiO_2 interface [18]. This charge is fixed and cannot be charged or discharged over a wide variation of surface potential ϕ_s. Generally, Q_f is positive and depends on oxidation and

annealing conditions and on silicon orientation. It has been suggested that when the oxidation is stopped, some ionic silicon is left near the interface. These ions, along with uncompleted silicon bonds (e.g Si-Si or Si-O bonds) at the surface, may result in the positive fix oxide charge Q_f. Q_f can be regarded as a charge sheet located at the $Si-SiO_2$ interface. Typical fixed oxide charge densities for carefully treated $Si-SiO_2$ systems are about 10^{10} cm^{-2} for a <100> surface and about 5 X 10^{10} cm^{-2} for a <111> surface. The <100> orientation is preferred for silicon MOSFETs [20] due to its lower Q_{it} and Q_f values. In Capacitance-Voltage measurement, for positive Q_f, the C-V curve will shift to more negative value of gate bias with respect to ideal C-V curve and for negative Q_f the C-V curve will shift to more positive gate voltage regardless of p-type or n-type as shown in Figure 2.9.

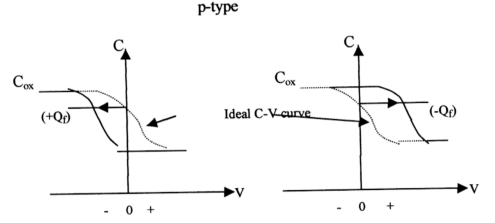


Figure 2.9: The influence of Q_{f+} and Q_{f-} on p-type semiconductor C-V curve. [20]

The amount of C-V shift can be calculated as

$$dV_f = Q_f / C_{ox} \tag{2.17}$$

where dV_f is the amount voltage shifted, Q_f is the fix oxide charge, and C_{ox} is the capacitance of oxide.

(c) Interface Traps Density, Q_{it}

Interface Traps are electronic states located at oxide-semiconductor interface due to impurity ions may be incorporated during the oxide (SiO_2) fabrication process and the non-ideal nature of the Si-SiO_2 interface [16,18,20,24,32]. Three "interface models" have been proposed in literature [20] on interface trap charges in MOS structure. The "Coulombic Model" proposed by Goetzberger et al [25] says that charges in the oxide induce potential wells in the silicon and quantum levels within these wells are identified with interface trap levels. The "Bond Model" proposes that the interface trap level distribution is produced by a distribution of bond angles or by stretched bonds at the silicon surface. Finally, the "Defect Model" proposes that defects within or near the interfacial region caused interface trap levels. Such defect range from stacking faults and micro pores to various atomic or molecular fragments left as a residue of imperfect oxidation.

Interface traps can be produced [20] in several different ways. (i) thermal oxidation in dry oxygen or steam, (ii) plasma oxidation, (iii) avalanche injection of electrons or holes into the SiO_2, (iv) the diffusion of metals such as chromium to the Si-SiO_2 interface, and (v) the exposure of the gate MOS to ionizing radiation.

The amount of interface traps, Q_{it} in normal MOS gate fabrication is about 10^{10} charges cm^2 ev^{-1}. The crystal silicon <100> orientation is the best in thermal oxidized silicon [18]. The interface charge trap depends upon the applied bias but the fix oxide charge is not dependent upon the gate bias. As such, the interface trap charges have

ifferent effects on C-V characteristics. In ideal case, there are no allowed electron states n the band gap of semiconductor. Since the Si-SiO_2 interface is not ideal, a certain lensity of interface traps will reside in the band gap region. In contrast to the fixed harge, electrons can flow into and out of these interface states depending upon the osition of Fermi level.

The character of the interface states is defined as "acceptor like" and "donor-like". An acceptor state is neutral if the Fermi level is below the state (i.e the state is unoccupied) and becomes negatively charged if the Fermi level is above it (i.e the state is occupied) and positively charged when it is empty. As a result, when the position of the Fermi level is altered, the charges at the interface change. When the interface is positive, the C-V curve shifts towards negative voltages, while when it is negative, the curve shifts towards positive voltages as shown in Figure 2.10.

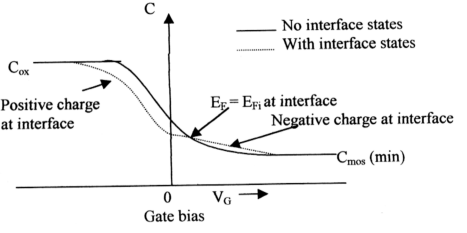


Figure 2.10: Shows the effect of the interface states is to smear out the C-V curves. [16]

The C-V curve is "smeared out" due to interface states present. In modern high quality MOS structure, the interface state density is maintained below 10 X 10^{10} cm^{-2}, so the effect is negligible.

(d) Deep Depletion

The deep depletion occurs in high frequency C-V measurement whenever the gate voltage is applied so rapidly that the build-up of an inversion layer is impossible. Capacitance decreases with gate bias until the avalanche breakdown point in the silicon is reached. Then, the capacitance saturates, but at lower value than the curve at normal equilibrium C_{min}, as shown in Figure 2.11.

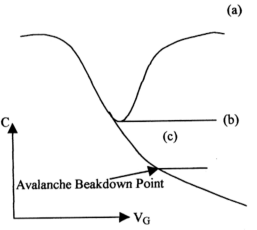


Figure 2.11: The MIS capacitance-voltage curve at (a) low frequency, (b) high frequency, and (c) deep depletion case. [20]

This non-equilibrium condition is called "deep depletion" because the silicon surface is depleted to a greater depth than it would be in thermal equilibrium. The minority carriers cannot generate fast enough to balance the changing of ac gate voltage

2.3 Field-Effect Transistors (FET)

The field-effect transistor (FET) is a three-terminal device where the current flowing from the gate to source is controlled by the gate terminal (Figure 2.12). In contrast with the bipolar-junction transistors (BJT), the field-effect devices use voltage at the gate terminal rather than current. Other than that, FET is a unipolar device, only majority carrier. The way of the gate isolation from the channel current flow is very important to avoid it from drawing a lot of current, and leading a poor gain i.e the ratio of output power or current to input power or current. Generally, the field effect transistor, FET can be categorized into three different categories depending on how the gate is isolated. The first category of FET, the gate isolation can be achieved by using an insulator between the gate and channel such as MOSFET, c-MOS, power MOSFET, etc. The second category of FET, is where the gate isolation can be achieved by using depletion region of reverse p-n junction such as JFET. In the last category of FETs, the gate isolation is achieved by using a Schottky barrier such as MESFET and MODFET. In this section, a detail discussion focused on the gate isolation as in the MOSFET and JFET is presented in terms of their structure, energy band, principal of operation and its characteristics such as current-voltage (I-V) output, equivalent circuit and frequency respond, types, etc.

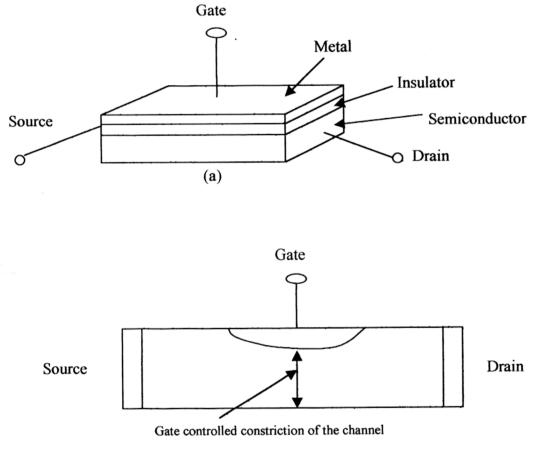


Figure 2.12: The principal of FET involves the use of gate to control the charge/current in the channel by voltage application in (a) 3-dimensional, and (b) 2-dimensional. The source and drain terminals are biased in such a way electron flow from source to drain. Both source and drain terminals are ohmic contact. [16,17]

2.3.1 Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

Metal-oxide-semiconductor field-effect transistor (MOSFET) is one member of the FET family [16,18,26]. Other members of FET family are JFET, MESFET, MODFET, etc. In MOSFET, the metal gate terminal is separated from the channel by an insulator. As such, the MOSFET also can be named as MISFET (metal-insulator-semiconductor) or IGFET (insulated-gate field-effect transistor) or MOST (metal-oxide-semiconductor transistor).

MOSFET is the most important device for very-large-scale integrated circuit such as microprocessor and semiconductor memories [16,18]. By some modification on its structure from planar to vertical [1,2,22], it can become the high power handling capability device i.e power MOSFET which will be discussed in section 2.4.3. Basically, MOSFET is one of the members of field-effect-transistor (FET).

2.3.1-1 MOSFET Structure

MOSFET structure is shown as in Figure 2.13. It consists of MOS structure at the gate terminal, and another two n+ regions as source and drain. Here, the case of n-channel for Si-SiO_2 system is being considered. The device parameters are channel length (L), channel width (Z), oxide thickness (d) and substrate doping (A).

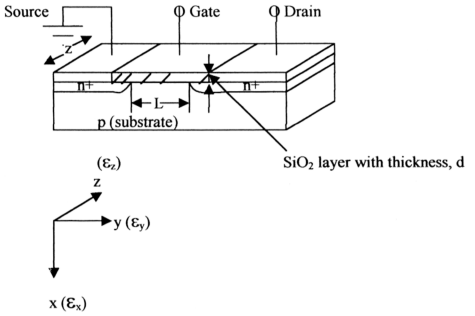


Figure 2.13: The MOSFET structure. [18]

2.3.1-2 Energy Band Profile and Principal of Operation

The energy band of MOSFET is similar with MOS energy band as in Figure 2.2. If bias voltage V_G is greater than V_T ($V_G > V_T$) is applied at the gate (Figure 2.14), the MOS structure gate will change the density of free electrons at the oxide interface where p-type material is inverted to n-channel. The n-channel will connect the two n+-regions. If a bias is applied between the source and drain, a current will flow in the channel. As such it meet the essential features of an active device [18].

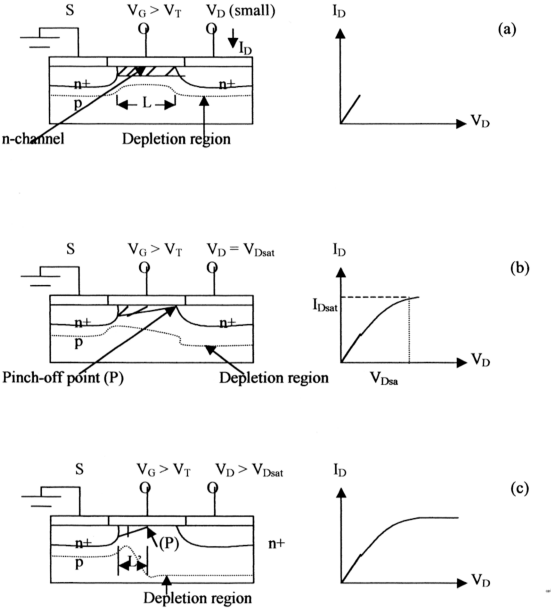


Figure 2.14: Show the principal operation and output I-V characteristics of MOSFET. (a) Low drain voltage, (b)onset of saturation. P is pinch-off point, and (c) beyond saturation. [18]

2.3.1-3 Current-Voltage Characteristic

The current-voltage characteristics of MOSFET (Figure 2.15) are based on the seven assumptions. First, the gate structure is assumed an ideal MOS structure. Second, only the drift current is considered here. Third, the mobility of the carrier in the channel is constant. Fourth, the channel doping is uniform. Fifth, the reverse-leakage current is small and negligible. Sixth, the transverse field εx is perpendicular with the longitudinal field ε_x and ε_x is much greater than ε_y. Finally, the gradual channel approximation is assumed usually true for long channel MOSFET.

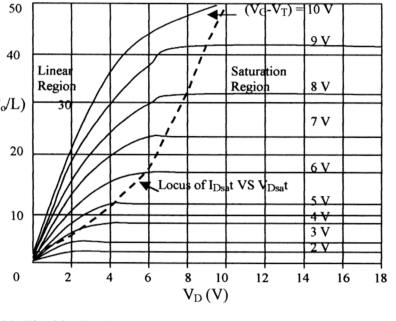


Figure 2.15: The idealized I-V characteristics of n-channel MOSFET. The drain current increases with higher gate-source voltage bias. For V_D =/> $V_D$sat, the drain current is constant. [18]

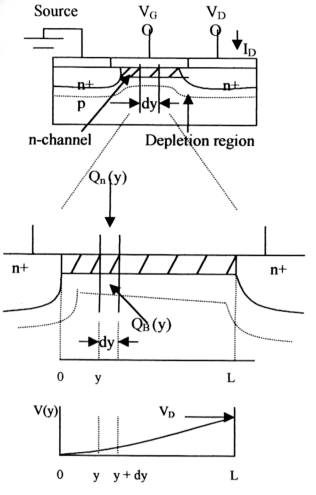


Figure 2.16: (a) MOSFET operated in the linear region, (b) Enlarged of the channel region, and, (c) Drain voltage drop along the channel. [18]

Considering an ideal MOSFET operating in the linear region shown in Figure 2.16 (a). Total charge induced (Figure 2.16 (b)) in the semiconductor at any distance y from the source

$$Q_s(y) = - [V_G - \psi_s(y)] C_o \qquad (2.18)$$

where $\psi_s(y)$ is the surface potential at y and $C_o = \epsilon_{ox} / d$ is the gate capacitance per unit area. Under strong inversion condition ($Q_s = Q_n + Q_{sc}$) and from equation 2.18 it yield the total charge in the inversion layer (or n-channel)

$$Q_n(y) = Q_s(y) - Q_{sc}(y)$$

$$= - [V_G - \psi_s (y)] C_o - Q_{sc}(y) \quad (2.19)$$

The surface potential ψ_s (y) at inversion is equivalent to $2\psi_B + V(y)$, where V(y) as shown in Figure 2.16 (c) is in the reverse bias between the point y and the grounded source terminal. The surface charge within the surface depletion region Q_{sc} is given by

$$Q_{sc}(y) = - qN_A W_m \cong - \{2\epsilon_s qN_A [V(y) + 2\psi_b]\}^{1/2} \quad (2.20)$$

By substituting equation 2.20 into equation 2.19, it result

$$Q_n(y) \cong - [V_G - V(y) - 2\psi_b]C_o + \{2\epsilon_s qN_A [V(y) + 2\psi_b]\}^{1/2} \quad (2.21)$$

The conductivity of the channel at any point y

$$\sigma(x) = q_n (x) \mu_n(x) \quad (2.22)$$

As constant mobility is assumed, so the channel conductance

$$g = Z/L \int_0^{x_i} \sigma (x)\, dx = Z\mu_n / L \int_0^{x_i} qn (x)\, dx \quad (2.23)$$

where the intergral at the right hand side is equal to the total charge per unit area. So equation 2.23 can be rewritten as

$$g = Z\mu_n/L \; |Q_n| \quad (2.24)$$

The channel resistance of an element section dy,

$$dR = dy/gL = dy/\{Z\mu_n |Q_n(y)|\} \quad (2.25)$$

and at the same time, the voltage drop across this section dy can be calculated as,

$$dV = I_D\, dR = I_D\, dy/ \{ Z\mu_n |Q_n(y)| \} \quad (2.26)$$

where I_D is the drain current which independent of y.

Substituting equation 2.21 into equation 2.20 and integrating from the source terminal (y = 0, V = 0) to the drain terminal (y = L, V = V_D), the drain current, I_D can be expressed as

$$I_D \cong Z/L\ \mu_n C_o \{[V_G - 2\psi_B - V_D/2]\ V_D - 2/3\ [2\in_s qN_A]^{1/2}/\ C_o \{[V_D + 2\psi_B]^{3/2} - (2\psi_B)^{3/2}\}\} \quad (2.27)$$

Linear Region

For small $V_D << (V_G - V_T)$, equation 2.27 become

$$I_D \cong Z/L\ \mu_n C_o\ (V_G - V_T)\ V_D$$

where the threshold voltage V_T is given by

$$V_T = \{2\in_s qN_A(2\psi_B)\}^{1/2}/\ C_o + 2\psi_B \quad (2.28)$$

The threshold voltage can be deduced from linearly extrapolated value at the V_G axis from I_D versus V_G (for given small V_D) plot. In linear region, the channel conductance g_D and transconductance g_m are derived as

$$g_D \cong \partial\ I_D/\ \partial V_D \Big|_{V_G = const} = Z/L\ \mu_n C_o(V_G - V_T) \quad (2.29)$$

$$g_m \cong \partial\ I_D/\ \partial V_D \Big|_{V_D = const} = Z/L\ \mu_n C_o V_D \quad (2.30)$$

2.3.1-4 Types of MOSFET

The different types of MOSFET are defined according to the way the "inversion layer" is formed in the channel. There are four types of MOSFET i.e n-channel enhancement (normally off), n-channel depletion (normally on), p-channel enhancement (normally off) and p-channel depletion (normally on) as shown in Figure 2.17. For an example, the n-channel enhancement is normally off. When gate bias is zero, current flow is minimum (or no current for ideal case). To produce an inversion in the channel, the gate needs a positive bias voltage [18].

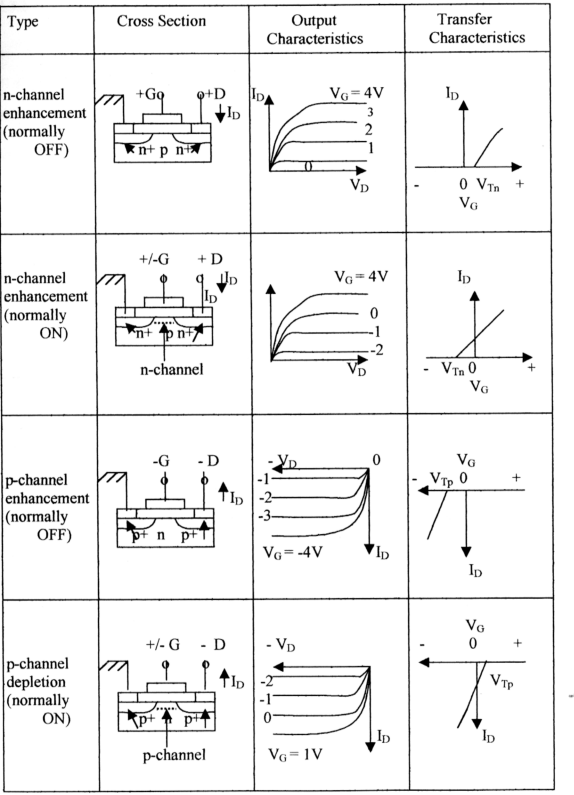


Figure 2.17: Different types of MOSFET, cross section, output characteristics and transfer characteristics. [18]

2.3.2 Junction Field Effect Transistor (JFET)

The JFET approach of the gate isolation is used for material in which it is difficult to get a large Schottky barrier height. The JFET acts as a voltage-controlled resistor. The device having reverse-biased p-n junction which acts as a "gate" to control the resistance and thus the current flow between two ohmic contacts. JFET is important in the high performance application such as microwave and digital applications. It can be operated in the frequency range from 10 to 100 GHz. JFET is also used in the high power application devices i.e in the vertical structure of power MOSFET such as n-channel enhancement power MOSFET which will be discussed in section 2.4.3.

2.3.2-1 JFET Structure

The JFET structure is shown in Figure 2.18 (a). In this structure, a double sided device with the two p+ layers are introduced at the left and right sides of the n-type semiconductor which act as the gate terminal. The source is at top of n-type semiconductor and the drain is at the bottom of n-type semiconductor. Both source and drain are ohmic contacts. As usual the source is negatively biased with respect to the drain to enable electrons to flow from the source to the drain. Both the gate terminals (i.e p+ layers at the left and right of the n-type semiconductor) have a common negative bias.

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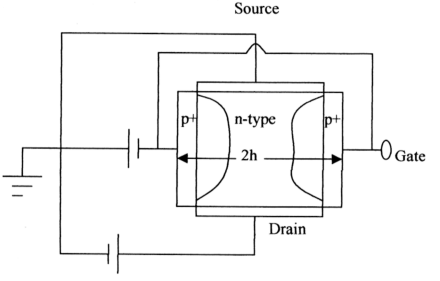


Figure 2.18 (a): A schematic JFET structure showing the source, drain and gate. [16,18]

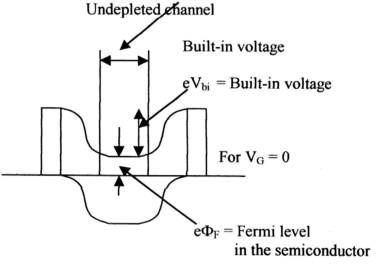


Figure 2.18 (b): The energy band profile for zero gate bias. [16,18]

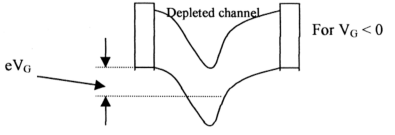


Figure 2.18 (c): The energy band profile when the gate bias is negative, so the channel is depleted. [16,18]

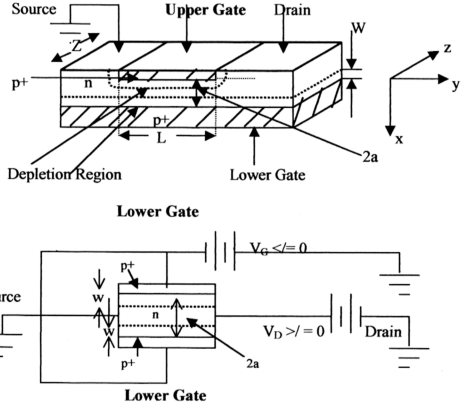


Figure 2.18 (d): The rearranged FET structure from (a). [16,18]

.3.2-2 Energy Band Profile and Principal of Operation

The energy band of JFET under equilibrium i.e $V_G = 0$ is shown in Figure 2.18 (b) where the n-channel is undepleted. Whenever the gate bias, $V_G < 0$, p+-n junction is nder reverse bias and the n-channel is depleted. The band diagram of the depleted hannel is shown in Figure 2.18 (c).

For the easier illustration, the orientation of the JFET structure in Figure 2.18 (a) s changed as shown in Figure 2.18 (d). The resistance of the channel in JFET is derived sing the relationship

$$R = \rho L / A = L / (q \mu_n N_D A) = L / \{2 q \mu_n N_D Z (a - W)\} \quad (2.31)$$

where N_D is the donor concentration, A is the cross-sectional area for current flow (A = Z (a – W), W is the width of depletion region at the top and bottom of the p+-n unctions, L is the channel length, Z is the channel width, 2a is the channel depth and μ_n s the electron mobility. Under normal operation, the gate is zero or reverse-biased (i.e V_G 0) and the drain is zero or forward- biased (i.e $V_D \geq 0$).

The effects of these bias voltages on the depletion width, current flow and drain current ersus drain voltage are explained as following:

a) When $V_G = 0$ and V_D is small ($V_D > 0$) (Figure 2.19 (a)), the drain current I_D is flowing with small value. As V_D increases, the drain current increases linearly with the magnitude of the V_D / R ratio. Please take note here, the voltage in the channel path is zero at the source and increases to V_D at the drain. As such the reverse bias of p+-n junctions at both top and bottom will increase as moving from source to drain. If V_D is increase, the reverse biased on p+-n-junction will increase and caused the increases of depletion width W and the effective cross-sectional area, A will reduce. Hence the

resistance R will increase and the magnitude of current flow (i.e V_D / R) is increased at slower rate.

b) When $V_G = 0$ and $V_D = V_{dsat}$ (Figure 2.19 (b)). If V_D is increased further (but bias gate stills $V_G = 0$), the depletion width is increasing until the two depletion regions are met each other at drain). The drain voltage at this stage (i.e W = a) is called saturation voltage, V_{dsat}

$$V_{dsat} = q N_D a^2 / (2\varepsilon_s) - V_{bi} \qquad (\text{for } V_G = 0) \tag{2.32}$$

where the V_{bi} is the built-in potential of the gate p+-n-junction.

At this saturation voltage V_{dsat}, the source and drain is separated by reverse biased depletion region. The drain current is called as saturation current Id_{sat} and the location P is called pinch-off point.

c) When $V_G = 0$ and $V_D > V_{dsat}$ (Figure 2.19 (c)). If V_{Dsat} is increased further, the depletion region will expand and the point P will move to towards the source. However, the voltage point of P remains the same magnitude of V_{dsat} (unaltered). Therefore, an amount of electrons per unit time from source to point P are remained same. As such the amount of I_{dsat} is same, independent of V_D for the case $V_D > V_{dsat}$.

d) When $V_G < 0$ (the gate is negative biased) and V_D is small ($V_D > 0$) (Figure 2.19 (d)). The negative bias voltage is caused the depletion width W increase, higher resistance and reduce the drain saturation current I_{dsat} and drain saturation voltage V_{dsat}. The amount of V_{dsat} is reduced by amount equal with bias voltage applied at the gate as given below

$$V_{dsat} = q N_D a^2 / (2\varepsilon_s) - V_{bi} - V_G \quad (\text{for } V_G = \text{negative bias}) \tag{2.33}$$

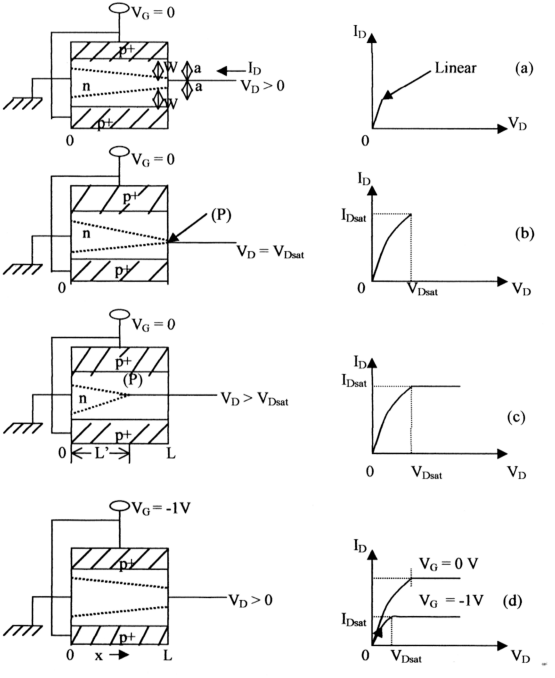


Figure 2.19: Shows the variation of depletion layer and output characteristics of JFET under different bias voltages. (a) $V_G = 0$ and small V_D, (b) $V_G = 0$ and at pinch-off, (c) $V_G = 0$ and post pinch-off ($V_D > V_{Dsat}$) and (d) $V_G = -1V$ and small V_D. [18,23]

2.3.2-3 Current-Voltage Characteristics

The Current-Voltage characteristics consist of three regions namely the linear region, the pinch-off region and the saturation region as shown in Figure 2.20.

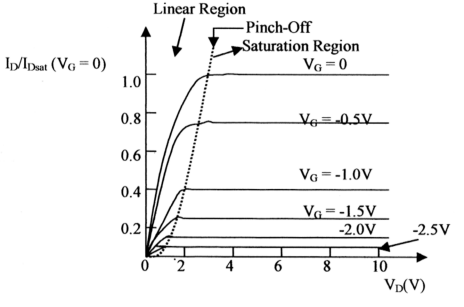


Figure 2.20: The normalized I-V Characteristics of JFET: linear, pinch-off and saturation regions. [16]

a) The Pinch-Off Region

Figure 2.21 (a) shows the expanded channel of the JFET while Figure 2.21 (b) shows the drain voltage drop along the channel.

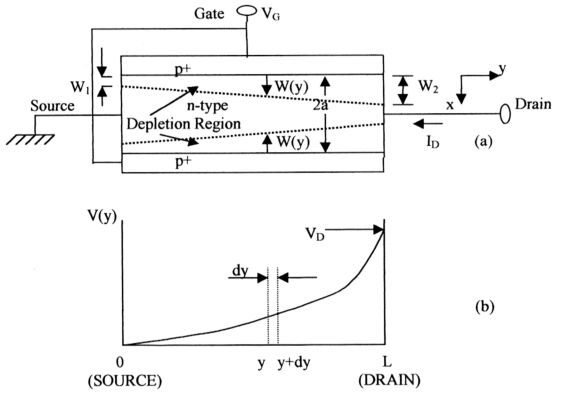


Figure 2.21: (a) An expanded channel of JFET, and (b) drain voltage drop along the channel of the JFET. [18]

Considering the I-V characteristics before the pinch-off region, the voltage drop across ly of the channel

$$dV = I_D\,dR = I_D\,dy\,/\,\{2\,q\,\mu_n\,N_D\,Z\,[a - W(y)]\} \tag{2.34}$$

Where dR can be obtained from equation 2.31 and replaced L by dy. The depletion width t distance y from the source is derived as

$$W(y) = \{2\varepsilon_s[\,V(y) + V_G + V_{bi}\,]\,/\,[qN_D]\}^{1/2} \tag{2.35}$$

Since the drain current I_D is a constant, the equation 2.34 can be rewritten as

$$I_D\,dy = 2q\mu_n\,N_D\,Z\,[a - W(y)]\,dv \tag{2.36}$$

From equation 2.35, the differentiation of the drain voltage dV is expressed as

$$dV = qN_D/\varepsilon_s \, W \, dW \tag{2.37}$$

Substituting equation 2.37 into equation 2.36 and integrating from y = 0 to y = L

$$I_D = 1/L \int_{W_1}^{W_2} 2q\mu_n N_D Z (a - W) (qN_D/\varepsilon_s) W \, dW$$

$$= (Z \mu_n q^2 N_D{}^2) / (\varepsilon_s L) [a (W_2{}^2 - W_1{}^2) - 2/3 (W_2{}^3 - W_1{}^3) \tag{2.38}$$

$$= I_p \{V_D/V_p - 2/3[(V_D + V_G + V_{bi})/V_p]^{3/2} + 2/3 [(V_G + V_{bi})/V_p]^{3/2} \} \tag{2.39}$$

where pinch-off current is given by

$$I_p \equiv Z \mu_n q^2 N_D{}^2 a^3 / (\varepsilon_s L) \tag{2.40}$$

and

$$V_p \equiv q N_D a^2 / (2\varepsilon s) \tag{2.41}$$

where V_p is the pinch-off voltage ($\equiv V_D + V_G + V_{bi}$) whenever $W_2 = a$.

b) The Linear Region

The drain voltage in the linear region is small where $V_D << V_G + V_{bi}$, the equation 2.40 can be expanded as following

$$I_D \cong I_p/V_p \{1 - [(V_G + V_{bi})/V_p]^{1/2} \} V_D \tag{2.42}$$

The channel conductance g_D (or drain conductance) is given by

$$g_D \equiv \partial I_D/\partial V_D \,|_{V_G=\text{constant}} = I_p/V_p \{1 - [(V_G + V_{bi})/V_p]^{1/2} \} \tag{2.43}$$

and the JFET transconductance g_m is defined as

$$g_m \equiv \partial I_D/\partial V_G \,|_{V_D=\text{constant}} = I_p/2V_p{}^2 \{V_p/(V_G + V_{bi})\}^{1/2} V_D \tag{2.44}$$

) The Saturation region

From equation 2.39, the drain current can be obtained by substituting $V_p = V_D + V_G + V_{bi}$

$$I_{Dsat} = I_p \{1/3 - [(V_G + V_{bi})/V_p] + 2/3 [(V_G + V_{bi})/V_p]^{3/2} \} \quad (2.45)$$

The saturation voltage is given by

$$V_{Dsat} = V_p - V_G - V_{bi} \quad (2.46)$$

The conductance is zero at saturation region.

The transconductance g_m is derived from equation 2.44 and equation 2.45,

$$g_m = I_p/V_p \{1- [(V_G + V_{bi})/V_p]^{1/2} \}$$

$$= (2Z \mu_n q N_D a) / L \{1- [(V_G + V_{bi})/V_p]^{1/2} \} \quad (2.47)$$

2.4 Power Semiconductor Devices

The Power Semiconductor Devices can be classified into three groups based on the degree of controllability as a switch, namely Diodes, Thyristors and Controllable Switches [1]. The on and off states for the "Diodes" are controlled by a power circuit. While for the "Thyristors", the on state is latched on by a control signal but must be turned off by the power circuit. As for the "Controllable Switches", the switches are turn-off and on by control signals.

The Controllable Switches group consist of several types of power device namely bipolar junction transistor (BJT), metal-oxide-semiconductor field effect transistor (MOSFET), gate turn off (GTO) thyristor, insulated gate bipolar transistor (IGBT) and MOS-controlled thyristor (MCT).

In this section, the "power MOSFET device" is explained in detail in terms of its tructure, principal of operation, current-voltage characteristic, etc. The other two power evices i.e Thyristor and power Bipolar Junction Transistor (BJT) are also presented but iscussions are limited more onto their structures. This will give an insight of how the ther power device structures are designed when compared to the power device of nterest which is studied in this work i.e power MOSFET (or n-channel enhancement node power MOSFET). Some modifications on the structure of simple low power evices are needed to make them suitable for high power application. Finally, the scope nd applications of Power Semiconductor Devices are presented.

.4.1 Thyristors

Thyristor which is sometimes referred to as SCR (i.e semiconductor-controlled ectifier) has the highest power handling capabilities in solid-state power device 1,21,27]. The vertical cross section of a thyristor is shown in Figure 2.22. It consists of a our-layer construction of alternating p-type and n-type regions i.e p-n-p-n [1,21]. If xamined, the vertical structure of a thyristor, it is similar with BJT including some of the lensity and layer thickness. The gate location of a thyristor is similar with the base ocation of the BJT. Also the cathode location of a thyristor is similar with the emitter ocation of the BJT. The n- region is a drift region in the thyristor to absorb the depletion ayer of the junction that blocks the applied voltage when the thyristor is in the off–state. The function of this n- region is also similar as the n- collector drift region of BJT.

The difference in a thyristor is the p layer that forms anode. This anode is not present in a BJT and this result in the different characteristic of the thyristor.

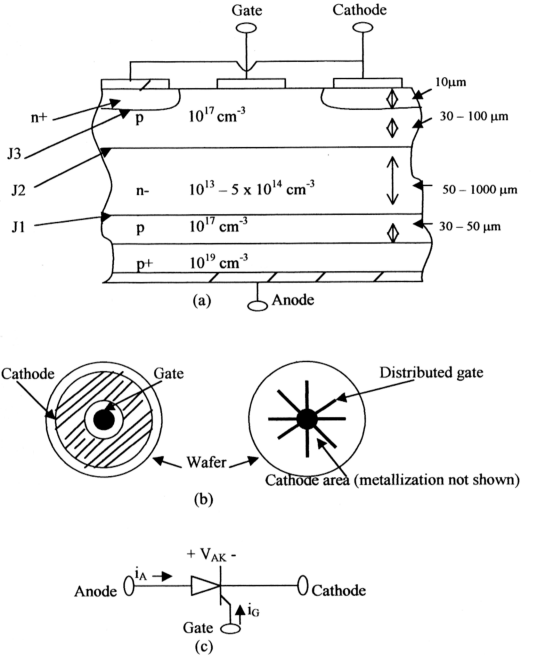


Figure 2.22: (a) Vertical cross-section structure of thyristor, (b) gate and cathode layouts, and (c) circuit symbol. [1,27]

4.2 Power Bipolar Junction Transistor (BJT)

The power BJT needs a large blocking voltage in the off state and high current apability if compared with conventional planar BJT. The modified structure has nproved significantly its I-V characteristics and switching properties as will be xplained in this section for both power BJTs and monolithic Darlington-connected evices.

The vertical cross section of a typical npn power BJT is shown in Figure 2.23. he n-p-n configuration is more widely used than p-n-p for power BJT. The vertical ructure is used in power BJT to maximizes the cross sectional area for current flow and is will reduce thermal resistance. The base and emitter terminals are on the top and the ollector terminal is at the bottom of the device structure. The doping level and its ickness can influence the device characteristics. The emitter and collector are similarly gh doped with n+ regions typically 10 X 10^{19} cm^{-3}. The base p-semiconductor is oderate doped 10 X 10^{16} cm^{-3}. The base thickness is designed small 5-20 μm to achieve e high amplification. The n- region termed as collector drift region. The power BJT reakdown voltage is determined by this collector drift region.

The current gain i.e the ratio $\beta = I_c / I_B$ for power BJT as a single structure alone is nall typically 5-10. As such, to achieve the higher gain, it is connected with Darlington onfiguration on a single chip as in Figure 2.24. The current gain in this Darlington onfiguration is given as in the equation below

$$\beta = \beta_M \beta_D + \beta_M + \beta_D \qquad (2.48)$$

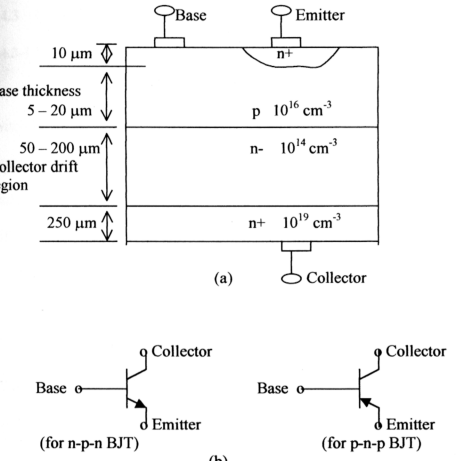


Figure 2.23: (a) the vertical cross section of a typical n-p-n power BJT, and (b) circuit symbols. [1]

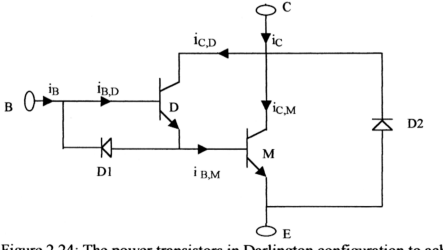


Figure 2.24: The power transistors in Darlington configuration to achieve higher current gain, beta. Two diodes used to help turn-off (D1) and full bridge application (D2). [1]

4.3 Power MOSFET

4.3-1 Structure

Power MOSFET belongs to the controllable switches group has the fastest witching speed among its group [1]. It can be turned on and off by applying control gnals. Power MOSFET operates on different physical mechanisms than power BJT. nderstanding its design structure will lead to an effective understanding in their ilization. Due to its high speed, the power MOSFET device has wide applications such s switching regulator, switching converter, motor driver and relay driver [1,8,9].

A power MOSFET has vertically oriented four-layer structure of alternating n- pe and p-type doping shown in Figure 2.25 (a). For the case of an enhancement mode -channel power MOSFET, its structure consists of n+/p/n-/n+ structure [1]. The two n+- gions are the source and drain of MOSFET structure. Both the source and drain are ighly doped with about similar doping typically 10^{19} cm^{-3}. The p-type semiconductor is lentified as the body and doped at 10^{16} cm^{-3}. The n- layer is the drain drift region doped ghtly at 10^{14} to 10^{16} cm^{-3}. The device breakdown voltage is determined by drain drift gion.

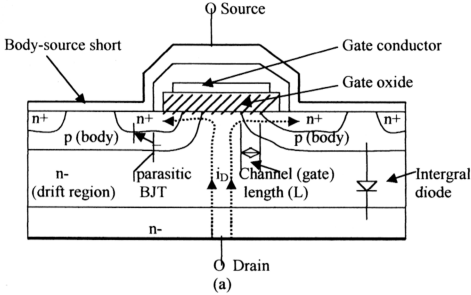
The gate terminal consists of the MOS structure (or MOSFET) laterally and JFET tructure vertically (Figure 2.26) [22]. JFET forms by the drift region (n-) and p-type emiconductor (body-source short). The depletion layer of JFET contributes significantly n the switching speed in today's power MOSFET.

The structure of power MOSFET normally is fabricated by using vertical double- iffused process namely VDMOS or simply DMOS [9]. Thousands of cells (e.g 240 quare mil silicon chip contains about 5,000) are packed parallel to reduce turn-on drain-

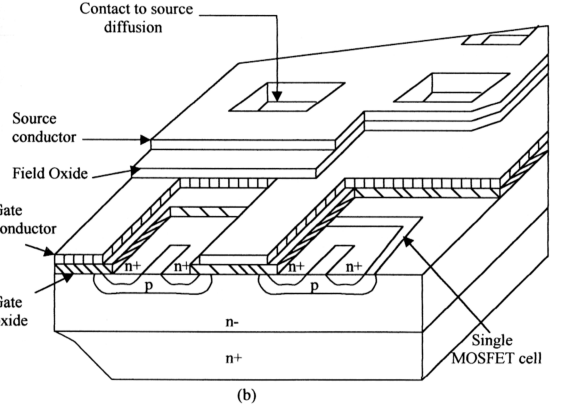
ource resistance $r_{DS}(on)$, hence improving the current handling capability. The amount f current flow at the given gate-source voltage (bias) [1,9], are determined by some her factors such as thickness of the gate oxide, the width of the gate and the number of te/source regions connected electrically in parallel (figures 2.25 (b) and 2.26).

Referring to Figure 2.25 of the power MOSFET structure, the geometrical shape f the source which are connected in parallel can reduce the turn-on drain-source sistance. The device designer can either select the polygon-shape (Figure 2.25) or exagonal-shape (Figure 2.26) or other geometrical shapes for the source terminal igure 2.27). The power MOSFET under study uses an enhancement n-channel power IOSFET with a hexagonal-shape source as illustrated in Figure 2.26.

Also, there is a parasitic n+/p/n- bipolar junction transistor (BJT) between the ource and drain (Figure 2.25 (a)). To ensure the BJT is always off condition, the p-type ody region is shorted to the source region by overlapping the source metallization onto -type body. The gate metallization overlaps across the n- drift region. This will enhance onductivity of the drift region at n- - SiO_2 interface by creation of accumulation layer in ne on state. Also, it acts as a field plate in the off state whereby the depletion layer of /n- junction will be not be too small which can result in decreasing the breakdown oltage.



(a)



(b)

Figure 2.25: Shows (a) vertical cross section, (b) perspective view of n-channel power MOSFET. Many thousand of cells are connected in parallel to reduce on-state resistance, hence improve power capability. [1]

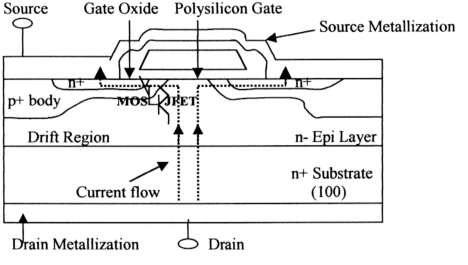


Fig. 2.26: An enhancement-mode n-channel power MOSFET, device under studies has a hexagonal shape source. It structure is a combination of lateral MOSFET and vertical JFET superimposed. [22]

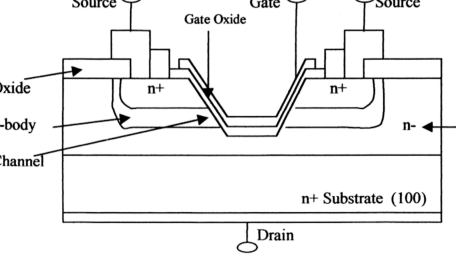


Fig. 2.27 (a)

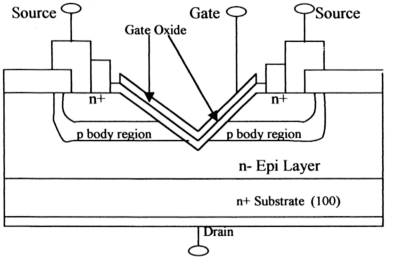


Fig. 2.27 (b)

igure 2.27: The other shapes of power MOSFET source, (a) n-channel trench V-Groove, and (b) n- channel truncated V-Groove. [2]

.4.3-2 Principle of Operation

The n-channel enhancement mode power MOSFET is a "normally-off " device 18]. It is turned on by application of sufficiently large gate-source voltage (V_{gs}> V_T) to nduced an inversion layer in the channel region and shorts the drain to source current [1]. An electron is moved from n+ source to the inversion layer laterally and then it move own vertically to n- drift region and lastly to n+ drain region as shown in figures 2.25 a) and 2.28. For current, the direction is opposite of an electron direction i.e it will flow rom drain to source.

Since the power MOSFET devices consist of two basic device structures i.e MOSFET structure at the gate terminal and JFET structure (formed by p-type body and - drift region), it is important to understand their role in this power MOSFET operation.

rst, the V_{gs} bias effect (or field effect) on the MOS gate structure is discussed (Figure 28). When a small positive bias (Vgs>0) is applied on the gate with respect to source, ositive charges are induced on the upper metal and equal quantity of negative charges at e SiO_2- p-type semiconductor interface are induced. The majority carrier holes are ushed away forming a depletion layer. When the positive gate bias is increased further $Vgs > V_T$), the electron density increases significantly forming an inversion layer in the hannel region. The p-type in the channel region is inverted to n-channel by minority arriers i.e electron. The n-channel is highly conducting, as such it shorts the drain to the ource. Next, the effect of applying a fixed voltage across the gate and source (V_{gs}) while he drain-source bias voltage (V_{ds}) is varied is discussed (V_{ds}). When the both bias are resent, the JFET is activated and starts to function [1]. The p-type semiconductor (i.e ody) receives a negative bias (i.e body-source short), so that the junction p-type body/ n-rift region is under reverse bias condition. The JFET is basically a voltage-controlled esistor [18] and will control the amount of current flowing vertically between the two hmic contacts i.e drain to source.

The resistance during on-state from drain to source [9] is minimized by putting many thousand units in parallel as discussed earlier. The higher number of units in parallel, the on-state drain to source resistance becomes smaller and this will achieve the large gain or high current handling capability of power MOSFET.

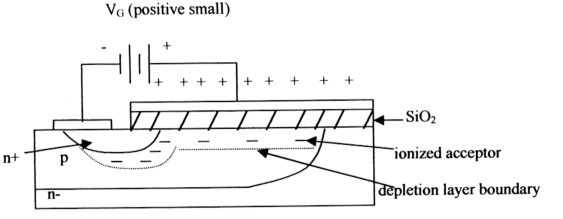


Figure 2.28 (a): The effects of increasing gate-source bias in power MOSFET during depletion layer (V_g positive small). [1]

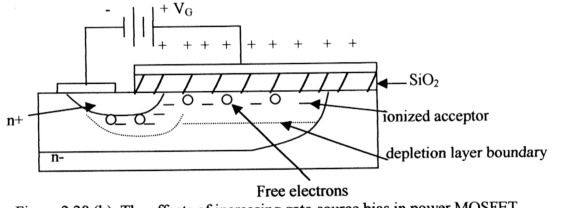


Figure 2.28 (b): The effects of increasing gate-source bias in power MOSFET during depletion layer ($0 < V_g < V_{th}$). [1]

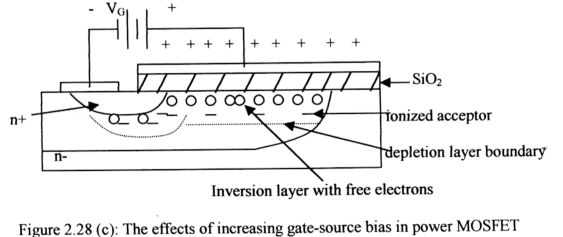
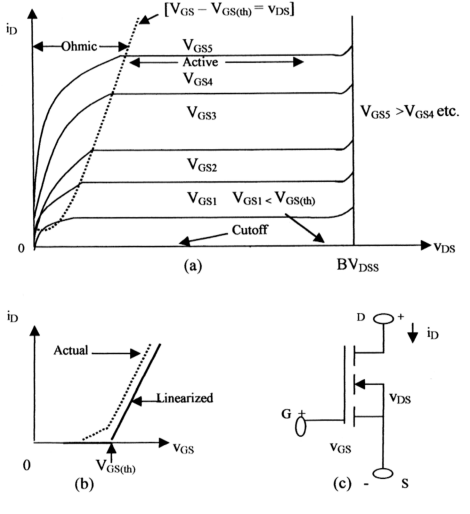


Figure 2.28 (c): The effects of increasing gate-source bias in power MOSFET during inversion layer ($V_g >/= V_{th}$). [1]

4.3-3 Current-Voltage Characteristics

The I-V characteristic of power MOSFET (i.e vertical structure) is similar to the onventional planar structure of MOSFET being discussed earlier. The I-V haracteristics, drain current i_D as a function of drain-to- source voltage v_{DS} with gate-to ource voltage V_{GS} as a parameter. Unlike of BJT, it is a voltage-controlled device as ndicated in Figure 2.29 (a) and (d) for n-channel power MOSFET. The idealized haracteristics of the device operating as a switch are shown in Figure 2.29 (e).



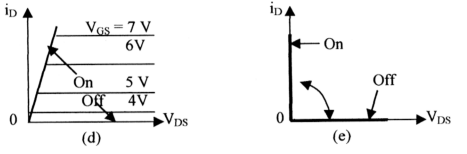


Figure 2.29: The n-channel power MOSFET (a) and (d) I-V characteristics (i_D – V_{DS}), (b) transfer curve, (c) symbol and, (e) idealized I-V characteristics operating as a switch. [1,21,27]

4.4 Importance and Applications of Power Semiconductor Devices

The scope and applications of Power Semiconductor Devices is discussed in this ction. It starts off with the comparison of "controllable switches" group in the power evice in term of their power capability and switching speed. For switching speed, power evice has the fastest speed among its group (controllable switches) [1,5,6]. Then, llowed by the general capability of all Power Semiconductor Devices in term of rrent, voltage and frequency. Finally, the scope in the power electronic system and pplications of these power semiconductor devices are presented.

4.4-1 Comparison of Controllable Switches Group (i.e second group of Power Semiconductor Devices)

Below is the qualitative comparison on the Controllable Switches Group of Power emiconductor Devices as discussed in the previous sections (Section 2.4.1 to 2.4.3) in rm of power handling capability (current/voltage) and switching speed.

Table 2.1: Relative Properties of the Controllable Switches Power Device. [1]

Power Device	Power Capability	Switching Speed
BJT/MD	Medium	Medium
MOSFET	Low	Fast
GTO	High	Slow
IGBT	Medium	Medium
MCT	Medium	Medium

2.4.4-2 Power Semiconductor Device Capability

The summary of Power Semiconductor Device capabilities in term of current, voltage and frequency are shown as in Figure 2.32.

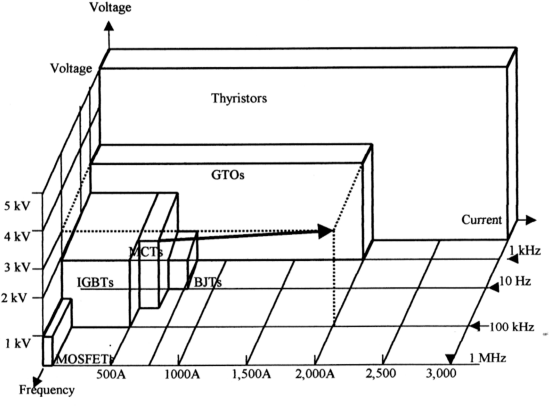


Figure 2.30: The summary of power semiconductor device capabilities. All device except MCT have relatively mature technology. MCT technology is under rapid expansion (see arrow). [1]

4.4-3 Applications of Power Semiconductor Devices

The application scope of Power Semiconductor Devices which is used as a switch the power electronic system is as shown in Figure 2.33 below.

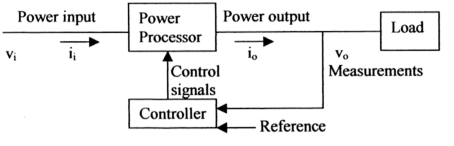


Figure 2.31: The block diagram of a power electronic system. [1]

he task of power electronics is to process and control the flow of electric energy by upplying voltages and currents in a form that is optimally suited for user loads. The ower input will be processed by Power Processor Unit and supply power output as esired by load (voltage, current, frequency, and the number of phases). The feedback ontroller will compare the output of the power processor unit and compared with the eference value. Any errors are minimized by the controller.

The advancement of microelectronic fabrication which causes the new evelopment of equipment such as computers, communication equipment and consumer lectronic which require regulated dc power supply and uninterrupted power supplies is he first factor influencing the increase in the demand of Power Semiconductor Devices. he demand to conserve energy such as adjustable-speed drive for motor pump, ompressor system, air conditioner, etc. is also an important factor contributing to this

demand. The need of process control and factory automation, for an example, the usage of robot powered by electric servo (adjustable speed and position) drives also result in the increase in demand for this device. The advance in the transportation sector to reduce smog and pollution such as electric vehicles which require battery charger and the increase in the electro-technical application such as equipment for welding, electroplating and induction heating which need high power for operation make power devices as an important device in these sector. The increase in the utility-related application such as high voltage dc transmission (HVDC), energy storage system, etc. and an improvement in the semiconductor technology of Power Semiconductor Devices itself have led to the higher current or voltage handling capability, faster switching speed and lower cost will result in more systems use these power devices.

Table 2.2 shows the various applications of Power Semiconductor devices from different sectors namely residential, commercial, industrial, transportation, utility systems, aerospace and telecommunication.

ble 2.2: Various Applications of Power Semiconductor Devices. [1]

RESIDENTAL
Refrigeration and freezers
Space heating
Air conditioning
Cooking
Lighting
Electronics (personal computers, other entertainment equipment)
COMMERCIAL
Heating, ventilating and air conditioning
Central refrigeration
Lighting
Computers and office equipment
Uninterruptible power supplies (UPS)
Elevators
INDUSTRIAL
Pumps
Compressors
Blowers and fans
Machine tools (robots)
Arc furnace, induction furnaces
Lighting
Industrial lasers
Induction heating
Welding
TRANSPORTATION
Traction control of electric vehicles
Battery chargers for electric vehicles
Electric locomotives
Street cars, trolley buses
Subways
Automotive electronics including engine controls
UTILITY SYSTEMS
High-voltage dc transmissions (HVDC)
Static var compensation (SVC)
Supplementary energy sources (winds, photovoltaic), fuel cells
Energy storage systems
Induced-draft fans and boiler feed water pumps
AEROSPACE
Space shuttle power supply systems
Satellite power systems
Aircraft power systems
TELECOMMUNICATION
Battery charges
Power supplies (dc and UPS)