hapter 3

igh Frequency Characterization of the n-Channel Enhancement lode Power MOSFET Device

1 Introduction

Device characterization is important in order to determine the idealized condition r device performance and also to determine the limitation to the operation of the device. ie ideal n-channel enhancement mode power MOSFET which usually termed as ontrollable switches" should be able to block arbitrarily large forward and reverse ltages with zero current flow when off, conduct arbitrarily large currents with zero ltage drop when on, can switch from on to off or vice-versa instantaneously when ggered and require vanishingly small power from control source to trigger the switch 0,31,34,35]. Capacitance-Voltage and Conductance-Voltage measurement of devices e used widely in determining various important parameters in devices [1,6]. Shifts in e capacitance-voltage and conductance-voltage curves provide evidence of the quality materials used in the device fabrication [16,20,24,32].

In this chapter, the experimental details involved in the high frequency pacitance-Voltage and Conductance-Voltage measurement techniques that have been opted in this work are presented. The device studied in this work i.e n-channel nancement mode power MOSFET is introduced in section 3.2. The device structure is

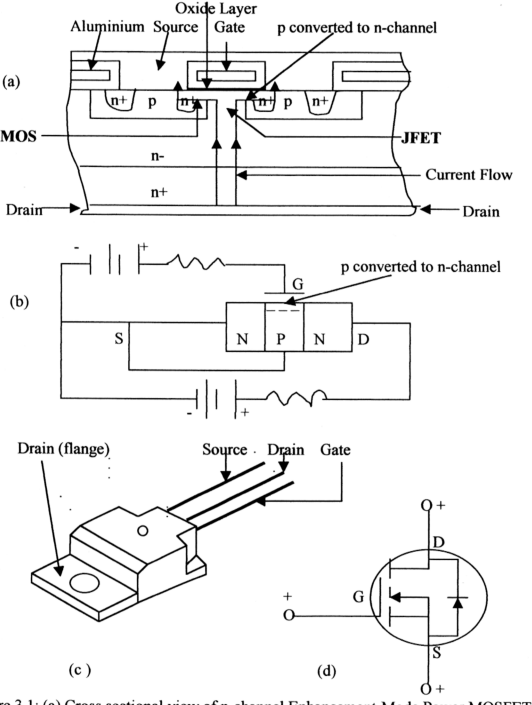
lso detailed in this section. The experimental set-up for the device for the device haracterization is presented in section 3.3. The design for the Test Fixture which enable igher capacitance range to be measured is detailed in section 3.4. Section 3.5 provides etails on the Capacitance-Voltage and Conductance-Voltage measurement techniques. Ieasurement techniques at elevated temperatures are presented in section 3.6. The last ection in this chapter previews the annealing procedures carried out on the device.

2 Power MOSFET Device Structure

The power semiconductor devices can be classified into three groups based on the egree of controllability as a switch, namely diodes, thyristors and controllable switches ,20]. The power MOSFET device is belongs to the controllable switches group has the stest switching speed among its group [1]. In this work, a set of commercially packaged -channel enhancement-mode power MOSFET device was studied. The structure of this evice and how the device is accommodated for measurement purposes are documented detail in this section.

The device studied in this work is an "n-channel Enhancement Mode Power IOSFET device" with a hexagonal shape source, manufactured by the Harris emiconductor industry (Figure 3.1). This power MOSFET is one of the members of ower Devices family under "Controllable Switches" group which also has the fastest witching speed among its group and is capable of handling high power (i.e high current high voltage handling capability). As a switch in application, its can be in the turn-on nd turn-off modes by the control signals [1]. This device structure actually is a ombination of MOSFET and JFET superimposed [6]. It has a p-type MOS gate and a versed biased field induced p/n junction (formed during inversion process) laterally at

ıe surface and a JFET structure vertically (Figure 3.1(a)). The cross sectional structure, ircuit connection, package layout and electrical symbol for this power MOSFET is ıown in Figure 3.1.



gure 3.1: (a) Cross sectional view of n-channel Enhancement-Mode Power MOSFET, (b) circuit connection, (c) package layout (source, drain and gate) and,

(d) electrical symbol. [8,14]

It is manufactured by using a vertical double-diffused process call VDMOS or imply DMOS [14]. Through this process, a single silicon chip structured with a large umber of closely pack, hexagonal cells in parallel. A 240 mil square chip for example as more than 25,0000 cells. As such, it can produce high current about 14A with the low urn-on drain-source resistance, $r_{DS}(ON)$ is about 0.1 ohm. The minimum Drain-Source reakdown Voltage of this power device is 50.0 Volt, and the Gate Threshold Voltage is etween 2.0 Volt and 4.0 Volt [8]. It can operate in the temperatures ranging from -55°C o 175°C [8]. Switching speed during turn-on is less than 60 ns and less than 100 ns uring turn-off. The oxide thickness is 500 A°, the channel length is 2 um and the gate rea is 200 um. The high frequency maximum capacitance, Cmax is about 8.45 nF and ie minimum capacitance, Cmin is about 5.2 nF while the high frequency maximum onductance, Gmax is about 341 mili-Siemen and minimum conductance, Gmin is about 28 mili-Siemen. They were designed for use in widely application such as switching egulators, switching converter, motor drivers, and relay drivers [1,8].

For electrical characterization, each pin of the power MOSFET sample is soldered o a hard wire. Then the soldered hardwire is winding with another hard wire acts as round wire (Figure 3.2(a)). Both hard and ground wires are insulated, so they are not horted each other (Figure 3.2(b)). All the ground wires are connected to the similar round earth. The proper grounding is important to avoid any stray capacitance pick-up uring measurement is carried out [15].

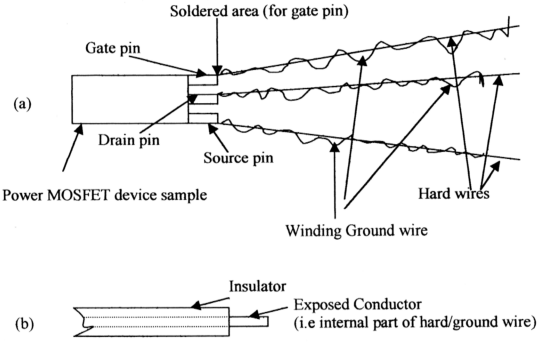


Figure 3.2: Shows (a) how the power MOSFET sample being prepared for C-V_G and G-V_G measurements to avoid any stray capacitance pick-up during measurement and easier connection, and (b) cross sectional view of hard wire (or ground wire). [8]

.3 Experimental Set-up for Device Characterization

Figure 3.3 (a) shows the experimental set-up for the high frequency C-V and G-V measurements done in this work. The experimental set-up consist of a Keithley 590 C-V Analyser, a personal computer, a test fixture, a temperature chamber and a set of n-channel enhancement mode power MOSFET device as the device under test (DUT). The Keithley 590 C-V Analyser is the main equipment in this work to perform the high frequency capacitance-voltage (C-V_G) and conductance–voltage (G-V_G) measurements on the power MOSFET devices. The equipment is interfaced to a personal computer and

easurements are done using a KI590CV-Model82 software provided by the anufacturer.

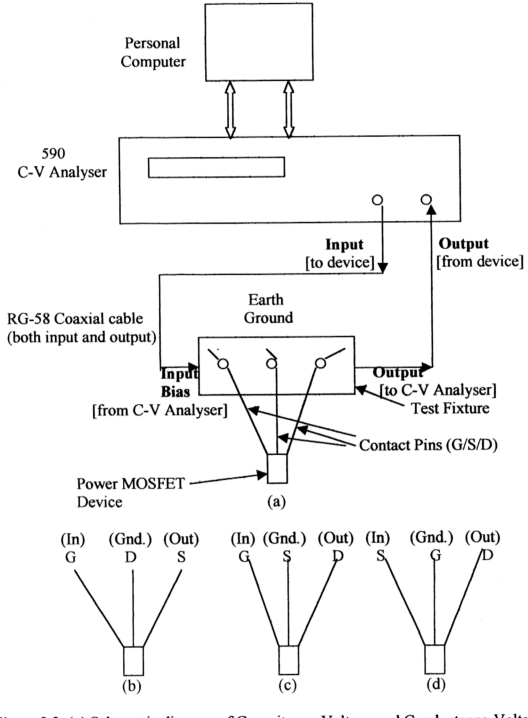
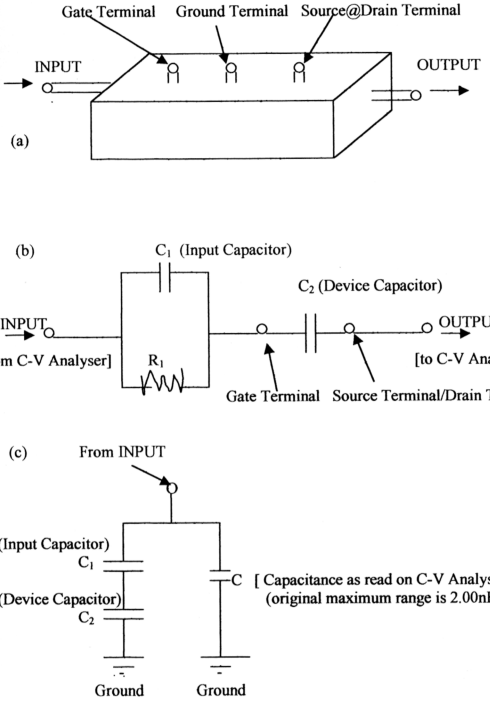


Figure 3.3: (a) Schematic diagram of Capacitance-Voltage and Conductance-Voltage measurement set-up. Pin connections to C-V Analyser for measurement across (b) gate-source , (c) gate-drain and (d) source-drain. [15]

The test fixture is needed to increase the upper limit range of the present Keithley 90 C-V Analyser from 2.0nF to 20.0 nF. So that the commercially packaged device om the industry which has a higher range than 2.0 nF can be measured. The test fixture as three terminal jacks, where the ground, gate and either the source or drain pin of the evice are connected during measurement. The temperature chamber is for Capacitance-oltage and Conductance-Voltage measurements at elevated temperatures. Figure 3.3), (c) and (d) show the pin connection from the device to the C-V Analyser for C-V and -V measurements across the gate-source, gate-drain and source-drain terminals spectively.

.4 Test Fixture Design

In order to characterize the n-channel enhancement mode power MOSFET tudied in this work, a test fixture was designed and built to facilitate measurement using he Keithley 590 C-V Analyser. The upper limit of capacitance measurement range of his C-V Analyser is only up to 2.0 nF while the capacitance of the MOSFET power evice ranges from 5.0 nF to 10.0 nF. The test fixture enables the capacitance neasurement range of the C-V Analyser to be expanded. Also the test fixture is designed uch that the device pin contacts such as the gate, source and drain can be connected irectly to the terminals of the test fixture and the RG-58 coaxial cables can be connected irectly from the input and output of the C-V Analyser to the test fixture.



igure 3.4: (a) External view of test fixture with contacts to the device under test (DUT) and the C-V Analyser.
(b) Circuit design of connections from the output to the input of the C-V Analyser.
(c) Equivalent circuit design of (b) excluding resistor, R_1 which does not correspond to high frequency.

To increase the maximum capacitance range of the C-V Analyser, a small internal rcuit consisting of the input capacitor, C_1 and input resistor, R_1, which are connected in arallel with each other is inserted between the connections of the INPUT and GATE rminal of the test fixture. The values of the input capacitor, C_1 and input resistor, R_1 etermines the maximum capacitance range of the C-V Analyser and the d.c. voltage weep biased during measurements.

In order to increase the capacitance range of the C-V Analyser to accommodate apacitance measurement of the device studied in this work, the exact value of the input apacitance, C_1 has to be determined. The capacitance across the input capacitor, C_1 and e device capacitor, C_2 which is the capacitance read on the C-V Analyser (refer Figure 4 (c)) can be expressed by the equation [27,28,29]:

$$1/C = 1/C_1 + 1/C_2 \tag{3.1}$$

y simple mathematical manipulation below

$$1/C_1 = 1/C - 1/C_2$$

$$= [C_2 - C]/ CC_2$$

$$C_1 = CC_2 / [C_2 - C] \tag{3.2}$$

In this case, the value for C is 2.0 nF which the maximum range of the C-V nalyser. If the capacitance range of this C-V Analyser (taken to be C_2) to be increased 20 nF, by inserting these values into equation 3.2, the value of input resistance C_1 must e 2.222 nF. With the new capacitance range, C-V measurements are not confined to apacitance less than 2nF only. The capacitance reading displayed on the equipment anel now must be multiplied by ten.

The input resistance, R_1 (refer Figure 3.4 (b)) must be carefully selected so that he required d.c. voltage sweep is used during measurement. In this work, the process of etermining R_1 value is also done to calibrate the C-V Analyser to measure accurate hreshold values of the power device. This process is done by performing normal C-V nd G-V measurements on the power MOSFET device studied in this work using esistors with different values for R_1. The resistor value for R_1 which gives the most ccurate reading of threshold voltage for this device is then used. The accuracy is ompared with to the threshold voltage value as measured using a standardized industrial ester which measures threshold value of devices. In this case, a resistance of 0.82 kOhm s selected as the input resistance which measures accurately the threshold voltage of the ower device as 3.096 Volt. The value of the threshold voltage read using this resistance alue is also consistent with the value given from the data sheet of specification of the evice parameters. Also with this resistance value, the required d.c. voltage sweep is btained.

.5 Capacitance-Voltage and Conductance-Voltage Measurement Techniques

The Capacitance-Voltage and Conductance-Voltage measurements were neasured at 1 MHz frequency using a Keithley 590 C-V Analyser. The equipment needs o be warmed-up at least for about two hours before any measurement can be carried out 15]. The source, drain and gate contacts were soldered with hard wires and connected to he test fixture mentioned previously. The C-V and G-V measurements across the ifferent structures of the power MOSFET is as illustrated in Figure 3.3 (b), (c) and (d). The connection from the drain contact grounded and voltages are measured with

eference to this contact. The gate contact is biased with a d.c voltage sweep from –7V to 7V and output signal from the source contact is recorded.

In order to operate the C-V Analyser to perform the C-V and G-V measurements, software supplied by Keithley Instrument to run the C-V Analyser is utilized. The perational procedure to start off the measurement begins with the opening of the main enu, "Device Measurement Analysis". From this main menu, select the "Manual Start weep Measurement" as illustrated in Figure 3.5 [15]. The measurement parameters hould then be set by pressing the "M" button. These parameters are the start and stop weep voltages, bias voltage, time delay and step voltage. Any leakage capacitance and ystem stray capacitance need to be suppressed by pressing the "Z" button with the probe-up" condition. In the "probe-up" condition the power MOSFET should not be onnected to the test fixture. After this procedure, the measurement parameters still emains as in the earlier set-up but the system strays are automatically zeroed. Once this eroing process is done the terminals of the power MOSFET should be properly onnected to the test fixture. The RG-58 coaxial cable is used to connect the input and utput terminals of the C-V Analyser to the contacts of the power MOSFET via the test ixture. Once everything is connected and already in the "probe down" condition, the neasurement is started by pressing "S" button. The voltage will sweep from negative to ositive or vice versa depending on the start voltage and stop voltage that has been set-p. The data obtained from the measurement is saved in the computer memory. The data an be retrieved for analysis. By pressing the "R" button "suppress" is removed and to uit the "Q" button should be pressed.

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      ** Manual Start Sweep Measurement **

press 'M'  to set measurement parameters
press 'Z'  to suppress Cq, Ch, G (probe-up)
press 'R'  to remove suppress
press 'S'  to start sweep
press 'Q'  to Quit

(note: Keyboard respond time is affected by delay time)

 Suppress is OFF                Sweep will take = 2.0 minutes

          Gain, offset and Rseries COMPENSATED READINGS
 High freq :  Ch (pF)      G (uS)          Start Vgs
               -0.5     -3.0000E+00          -7.000
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Figure 3.5: Shows the Manual Sweep Menu in the software of C-V Analyser to perform auto sweep during high frequency Capacitance-Voltage and Conductance-Voltage measurements. [15]

.6 Capacitance-Voltage and Conductance-Voltage Measurement at Elevated Temperatures.

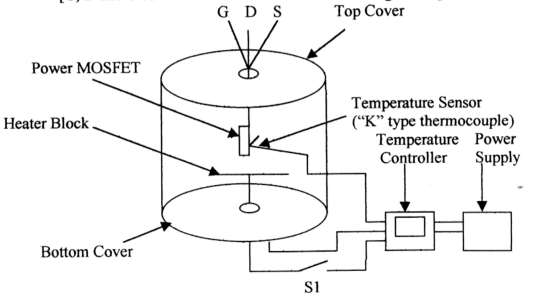

Figure 3.6: Schematic drawing of the Temperature Chamber which used for C-V and G-V measurements at elevated temperatures.

Figure 3.6 shows the schematic diagram of Temperature Chamber where C-V and -V measurements of the power MOSFET at elevated temperatures are done. The aximum measurement temperature in this work is 175°C. This to comply with the anufacturer recommendation for the highest operating temperature. The power OSFET was placed inside the temperature chamber by opening the top cover. A "K" pe thermocouple which is used as a temperature sensor is placed at the back of the ower MOSFET to monitor the measurement temperature. The power MOSFET is heated the Temperature Chamber to a required temperature and then the measurements are rried out when a stable temperature is achieved. The measurement temperature is aintained by a Sigma MDCAS temperature controller. The power MOSFET is heated convection processed by the Heater Block. Once a C-V or G-V measurement is ompleted at a particular temperature, the Temperature Controller is reset to a higher mperature to obtain measurement at this temperature.

.7 Annealing Process

When the n-channel enhancement mode power MOSFET is annealed at a articular temperature, it undergoes a heat treatment process and is exposed to this levated temperature for a certain time duration and is then cooled down gradually to oom temperature. This process is known to especially effect the oxide layer of the power IOSFET [5,11,20]. C-V and G-V measurements are repeated after each annealing rocess.

7.1 Calibration of Furnace

In this work, annealing is done in a Carbolyte Furnace model CFN1271. A hromel-Alumel thermocouple is used as a temperature sensor. This thermocouple is ecially designed so that it can go all the way into the tube of the furnace. The ceramic sulator on the thermocouple is marked into 1 cm divisions all the way from the tip to e end that protrudes out of the furnace. This enables the temperature and distance of the ermocouple tip in the furnace to be measured. The thermocouple is connected by K-pe wires to a digital thermometer model TR2112A. The experimental set-up for the nnealing process is illustrated in Figure 3.7.

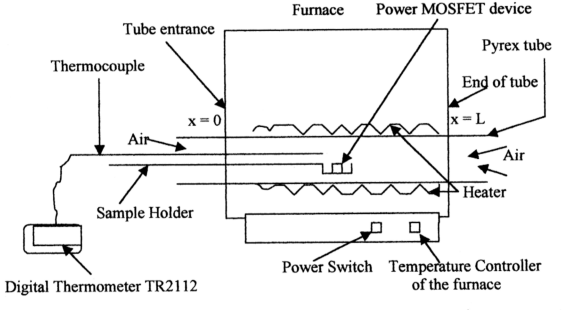

Figure 3.7: Set-up for Annealing Process

The calibration procedure starts with determining the variation of temperature in he tube furnace with the distance from the tube entrance, marked x = 0 to the end of the ube, marked x = L. The thermocouple is fixed at a particular position until a stable

mperature is achieved. A calibration curve of temperature versus distance is then chieved. Figure 3.8 shows the calibration curve of furnace at set temperature of 150°C. rom this curve, the plateau region between 21 cm to 24 cm inside the furnace tube is etermined as the position when the power MOSFET is to be placed during annealing.

The next calibration procedure is to calibrate the set temperature of the furnace ith the temperature as detected by the temperature sensor and measured by the digital ermometer at the position determined from the calibration procedure described in the revious paragraph. The thermocouple is positioned at this position and furnace is set to he required temperatures. The maximum stable temperature obtained is recorded as the ctual temperature at this position when set at this temperature. Figure 3.9 shows the alibration curve obtained. Table 3.1 and 3.2 presents the data as of calibration curves in igures 3.8 and 3.9 respectively.

Table 3.1: Data for Figure 3.8.

Furnace Distance [+/- 0.1 cm]	**Reading Temperature** [+/- 0.1°C]
16.0	133.0
17.0	136.0
18.0	140.0
19.0	142.0
20.0	144.0
21.0	146.0
22.0	146.0
23.0	146.0
24.0	146.0
25.0	145.0
26.0	142.0
27.0	138.0
28.0	132.0

Table 3.2: Data for Figure 3.9.

Temperature of Furnace Controller [+/- 0.1°C]	**Reading Temperature** [+/- 0.1°C]
100.0	98.0
150.0	146.0
200.0	196.0
250.0	248.0
300.0	297.0
350.0	348.0
400.0	397.0

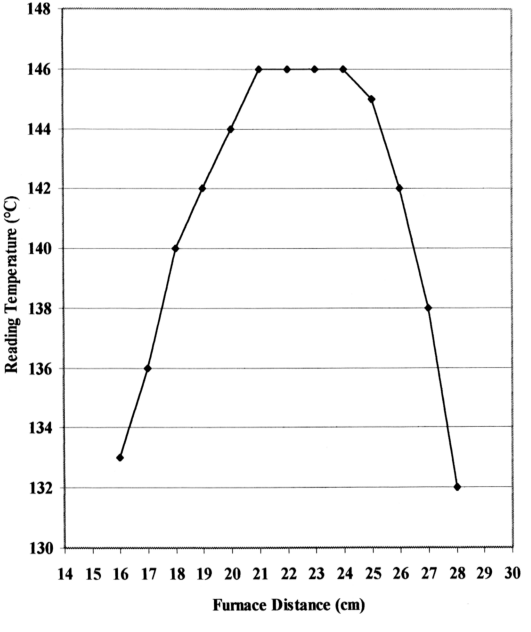

Figure 3.8: Calibration Curve of Tube Furnace; Temperature versus Distance at set temperature of 150°C.

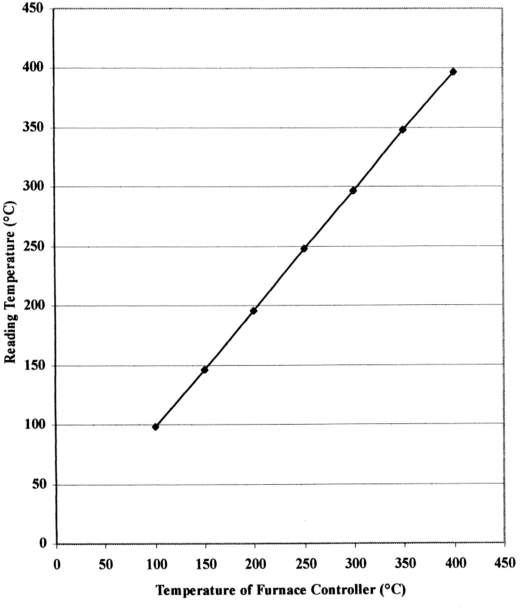

Figure 3.9: Calibration Curve of Temperature at position where device is to be placed with set temperature of the furnace.

3.7.2 Annealing Process

The furnace is set to the required temperature using the calibration curves in Figures 3.8 and 3.9. When the required temperature is achieved, the power MOSFET device which is placed in a sample holder is pushed into the furnace at the required position as determined in the calibration procedure. The device is left in the furnace at this temperature for 30 minutes. The furnace is then turned off and the device is left in the furnace to cool down gradually to room temperature. In this work, the device is annealed in air at temperatures of 100°C, 200°C, 300°C, 350°C and 400°C. C-V and G-V measurements are repeated after each annealing process.