Chapter 4

High Frequency Capacitance-Voltage Measurements On The n-Channel Enhancement Mode Power Device: Results and Analysis

.1 Introduction

The High Frequency Capacitance-Voltage (C-V) measurement results of the n-hannel Enhancement Mode Power MOSFET device studied in this work are presented, iscussed and analyzed in this chapter. This chapter begins with section 4.2.1 with the resentation and analysis of the C-V_G characteristics of the device across the Gate-Source G-S) structure. The measurement across the G-S structure is further studied in section .3 with measurement done at different temperatures ranging from 25°C to 175°C. Since he switching properties of the device is strongly determined by electrical characteristic f the G-S structure [2,6,9,14], measurements are done across the G-S structure only. The ffects of measurement temperature on the C-V_G characteristic across this structure are lso analyzed. Exposing the device high temperature is expected to produce some ignificant effects on the performance of the device. High Frequency C-V_G results btained across the G-S structure of this device annealed at temperatures of 100°C to 00°C are presented and studied in section 4.4. Finally, the C-V_G results of device nnealed at 400°C at different measurement temperatures are presented and analyzed.

2 High Frequency Capacitance-Voltage Characteristics of Device

2.1 Measurements across Gate-Source Structure

Figure 4.1 shows the high frequency C-V_G curve across the gate-source of the n-hannel enhancement mode power MOSFET at room temperature 25°C. In the negative iased region, the capacitance remains constant at approximately 8400 pF and decreases ıddenly to approximately 8059 pF when the voltage is about –2.0 volts and decreases gain to approximately 5260 pF when the voltage is zero . In the positive biased region, ıe capacitance gradually decreases to approximately 5079 pF when the voltage is about .5 volts and then the capacitance increases slightly to approximately 5577 pF when the oltage is about 2.0 volts, then remains fixed at this capacitance until the voltage is about .0 volts. The capacitance increases suddenly to approximately 8400 pF when the voltage bout 3.0 volts. The capacitance remains constant at this magnitude with the further ıcrease in voltage. The maximum high frequency capacitance depicted in the both the egative and positive biased regions is of same magnitude (i.e 8400 pF).

This high frequency C-V_G curve depicted here is unique and different from the ormal high frequency measurement for the MOS structure [16,18,20] although the G-S tructure is similar to a MOS structure (refer to Figure 4.2). The C-V curve for of p-type MOS or n-type MOS at high frequency (in this case 1MHz) would result only in one naximum either in the negative or positive biased region respectively [16,23]. The ollowing paragraphs will present a detailed analysis of the C-V_G curve of the n-channel nhancement power MOSFET device.

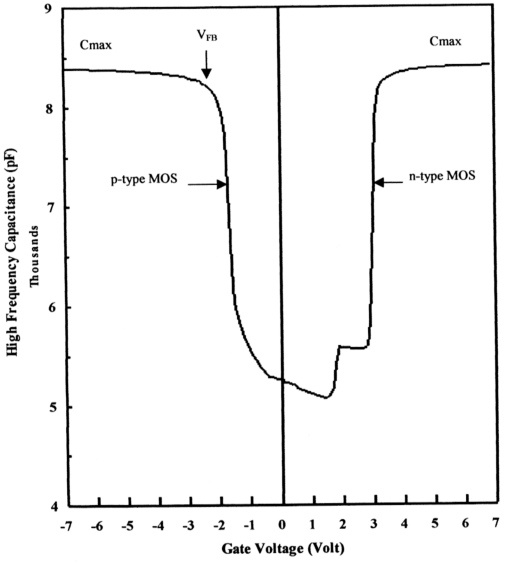


Figure 4.1: High Frequency Capacitance-Voltage ($C\text{-}V_G$) measurement results across **Gate-Source structure** of the n-channel enhancement mode power MOSFET device at room temperature 25°C.

where X_o is the oxide thickness. The electric field at the silicon surface, from Gauss's law equals

$$\varepsilon_s = -Q_s/k_s\varepsilon_o \tag{4.4}$$

Thus, from these three equations

$$V_o = -X_o/(k_o\varepsilon_o) \times Q_s \tag{4.5}$$

where $Co = k_o\varepsilon_o/X_o$ is the capacitance per unit area of the oxide layer. The gate voltage then can be related to the characteristics of the surface space charge region by

$$V_G = -Q_s/C_s + \Phi_s \tag{4.6}$$

If Q_G is the charge per unit area on the gate, the capacitance across the MOS structure is

$$C = dQ_G/dV_G = -dQ_s/dV_G = -dQ_s / [(-dQ_s/C_o) + dQ_s] \tag{4.7}$$

or $$C = 1/ [1/C_o + 1/C_s] \tag{4.8}$$

where $C_s = -dQ_s / \Phi_s = k_s\varepsilon_o / X_d$ (4.9)

is the capacitance per unit area of the surface space charge region in the semiconductor where X_d is the depletion width. Thus the capacitance of the MOS structure is given by the series combination of C_o and C_s. By eliminating X_d, the capacitance formula can be expressed as

$$C/C_o = 1/ [1 + (2k_o^2\varepsilon_o/qN_Ak_sX_o^2)\, V_G]^{1/2} \tag{4.10}$$

which predicts that the capacitance will fall with the square root of the gate voltage while the surface is being depleted.

When a large negative bias is applied to the gate, holes, being the majority carrier in a p-type semiconductor are attracted towards the semiconductor-oxide interface creating an accumulation region (Figure 4.3 (a)). As a result, no depletion region exists, thus the formula derived for capacitance across the MOS structure is not applicable.

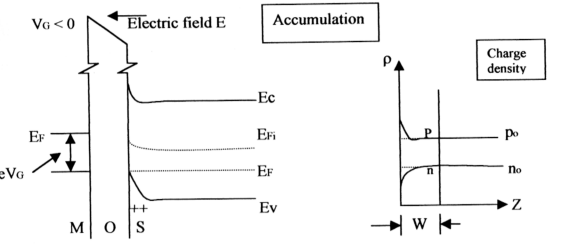


Figure 4.3 (a): Effects of applied large negative gate voltage (V_G = -7V to –3.5V) on the p-type MOS Gate-Source structure of the n-channel enhancement mode power MOSFET device. [16,23]

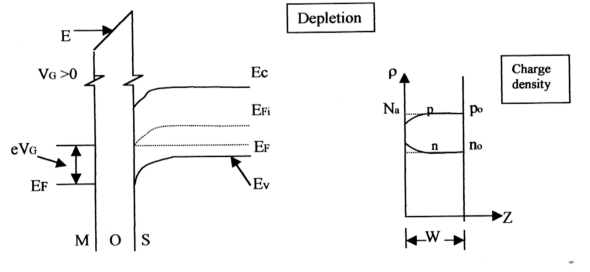
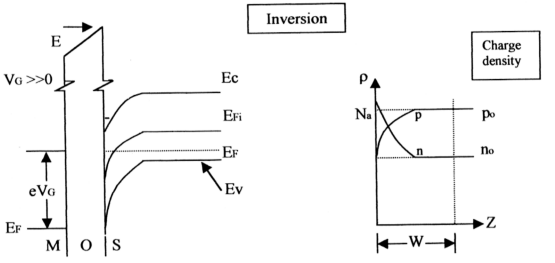


Figure 4.3 (b): Effects of applied relatively more positive biased gate voltage (V_G = -3.5V to 0V) on the p-type MOS Gate-Source structure of the n-channel enhancement mode power MOSFET device. [16,23]



igure 4.3 (c): Effects of positive biased (V_G >0) on the p-type MOS Gate-Source structure of the n-channel enhancement mode power MOSFET device. [16,23]

However, the capacitance can be readily obtained by considering that when the surface is in accumulation, the semiconductor acts as a resistor in series with the oxide capacitance. Thus the measured capacitance will just be the oxide capacitance (Equation 4.8) which is the maximum capacitance observed in the large negative biased region.

When a relatively small positive bias is applied to the gate (less than 2V), holes are depleted from the oxide-semiconductor interface resulting in a depletion region. The capacitance across the gate-source structure then is in agreement with equation 4.10 where the value decreases with the square root of the gate voltage.

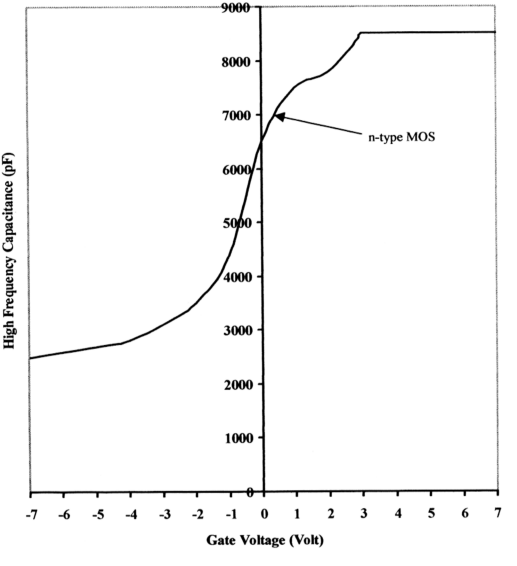
The sudden decrease in the capacitance occurs when V_G is equal to the flat-band voltage and beyond this voltage, the gradual decrease in the negative biased region before depletion indicates presence of fast surface state in the forbidden gap concentrated at the surface [5,9,16,18-20,24,32].

When the positive potential applied to the gate is increased, the width of the depletion region will first increase. Correspondingly, the total electrostatic potential variation in the silicon will also increase which result in the energy band bending towards the Fermi level at the interface (Figure 4.3b). However, when the bands are bent further, the conduction band will come close to the Fermi level. At this point, the concentration of electrons near the interface will increase sharply. Then, most of the additional negative charge induced in the semiconductor will be charge, Q_n due to electrons in a very narrow n-type inversion layer or n-channel. However, the onset of this inversion layer, produces a reverse bias p-n junction between the source and gate at the surface of the semiconductor [1,6,9,13,26,27,30,31]. This result in the generation of electron-hole pairs and the electrons are immediately attracted to the surface below the gate. Accumulation

negative charges in this region reduces depletion width at the interface to zero. Again, mentioned earlier the semiconductor can be considered as just a resistor in series with ide capacitance. Thus the capacitance value increases and saturate at the oxide pacitance value.

2.2 Measurements Across Gate-Drain Structure

Figure 4.4 present the high frequency Capacitance-Voltage ($C\text{-}V_G$) measurement sults across Gate-Drain structure (Figure 4.5) of the n-channel enhancement power OSFET device at room temperature. The C-V plot across the Gate-Drain structure oduces a plot typical of n-type MOS structure [15,18,20]. Referring to Figure 4.5, it is early justified since measurement is done across the oxide and n-type silicon substrate. o the surface under the gate accumulates with electrons when the gate is biased with a rge positive voltage (Figure 4.6 (c)). Majority carrier in the n-type silicon which are ectrons accumulates at the oxide-semiconductor interface. The surface under the gate oes into depletion when V_G is negative pushing away electrons from the surface. When $_G$ is large and negative the surface inverts but the capacitance remains at the value when was in depletion since the conductance in this case is not at the surface but through the ulk.



igure 4.4: High Frequency Capacitance-Voltage ($C\text{-}V_G$) measurement results across **Gate-Drain structure** of the n-channel enhancement mode power MOSFET device at room temperature 25°C.

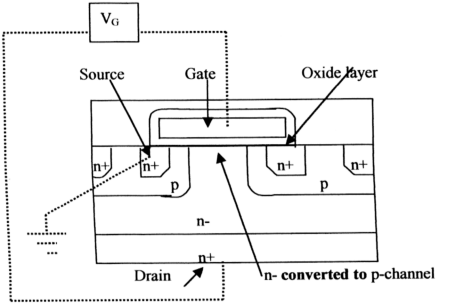
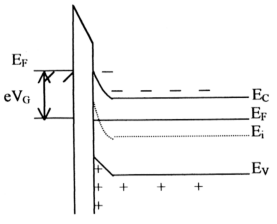
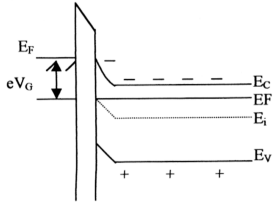


Figure 4.5.: Shows the cross sectional of the gate to drain structure of n-channel enhancement mode power MOSFET. [6,9]

(a) $V_G << 0$



(b) $V_G < 0$



c) $V_G > 0$

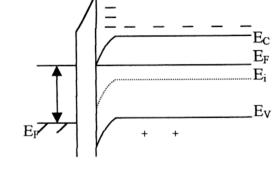


Figure 4.6 : Energy Band Profiles of the n-/n+ type MOS of the power device at different gate voltages; (a)$V_G << 0$, (b) $V_G < 0$ and (c) $V_G > 0$. [18]

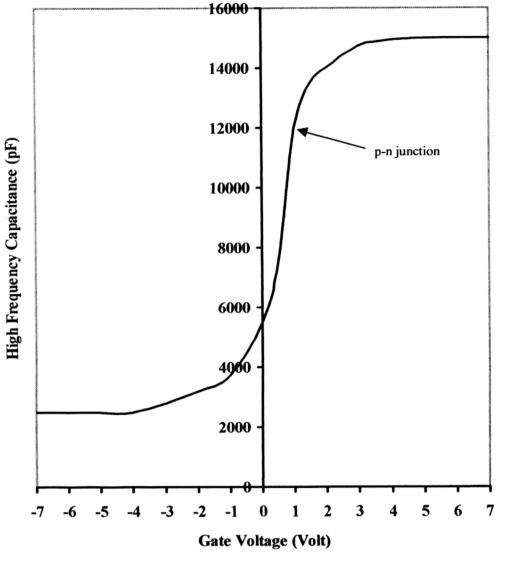


Figure 4.7: High Frequency Capacitance-Voltage ($C\text{-}V_G$) measurement results across **Source-Drain structure** of the n-channel enhancement mode power MOSFET device at room temperature 25°C.

Figure 4.7 shows the high frequency Capacitance-Voltage ($C\text{-}V_G$) measurement sults across Source-Drain structure of the n-channel Enhancement Power MOSFET evice at room temperature 25°C. The C-V curve is typical of a p-n junction C-V haracteristic [16-18,33].

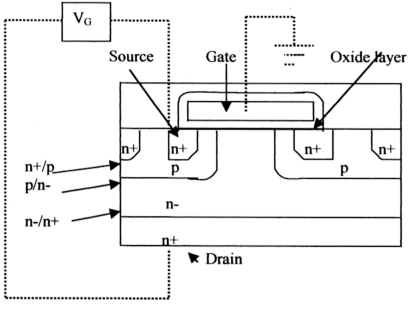


Figure 4.8: Shows the cross sectional of the source to drain structure of n-channel enhancement mode power MOSFET. [6,9]

Referring to Figure 4.8, this observation is clearly justified as measurements are ne across a p-n junction type of structure. When a negative voltage is applied to the urce, the majority carriers of the p-type silicon which are holes are pushed towards the nction and the electrons in the n-type silicon are also pushed towards the junction. A pletion region is created at the junction, producing a reversed biased condition in the p- junction resulting in the small capacitance value. As the source is biased increasingly positive, a forward biased condition is produced and this results in the increase in pacitance to maximum value and saturating at this value.

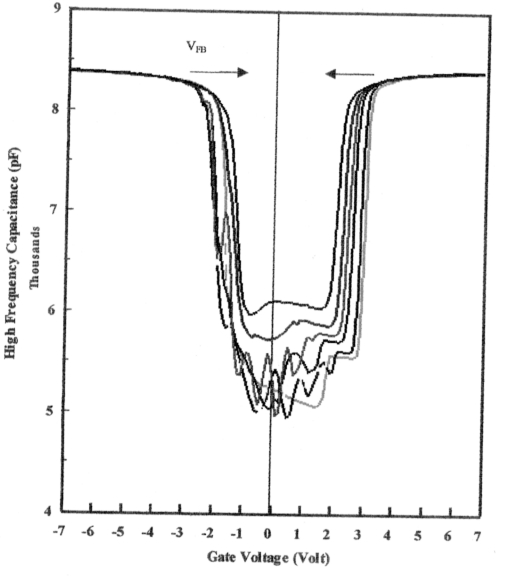
3 High Frequency Capacitance-Voltage Measurement Results At Different Measurement Temperatures Across Gate-Source Structure

Figure 4.9 shows the high frequency Capacitance-Voltage ($C\text{-}V_G$) measurement sults across Gate-Source structure of the n-channel Enhancement Mode Power OSFET device at different measurement temperatures ranging from 25°C to 175°C. he $C\text{-}V_G$ curves shift towards zero gate voltage both in the positive and negative biased gions as the measurement temperature increases. The minimum capacitance is also bserved to increase with the increase in measurement temperature. The maximum pacitance in the negative and positive bias regions does not change with measurement mperature.

The shift in the $C\text{-}V_G$ curves in the negative biased region towards zero gate oltage with increase in measurement temperature correspondingly results in the shift in e flat-band voltage (V_{FB}) in the same fashion. This shift is most obvious when the easurement temperature is above 100°C. Shift in V_{FB} is known to be due to surface ate charges present in the oxide because of excess ionic silicon presence in the oxide uring oxidation process [16,18,19,20,24,32]. The relationship between the flat-band oltage and these charges is well established by the equation

$$V_{FB} = -Q_{SS}/C_O \tag{4.11}$$

here C_o is is the oxide capacitance. Thus, measurement temperature above 100°C result a decrease in the surface state charge, Q_{SS} since the maximum capacitance which rresponds to the oxide capacitance, C_o does not vary with measurement temperature. his indicates that, excess ionic silicon are reduced as the measurement temperature creases above 100°C.



gure 4.9: High Frequency Capacitance-Voltage ($C\text{-}V_G$) measurement results across Gate-Source structure of the n-channel enhancement mode power MOSFET device at different measurement temperatures ranging from 25°C to 175°C.

From literature [24], annealing a MOS structure in oxygen produces similar ffects. Thus measurement temperatures above 100°C results in excess ionic silicon ecreasing by reacting with oxidizing species present in the oxide. In the positive biased egion, the shift in C-V_G curve towards zero gate voltage with increasing measurement emperatures is in a uniform manner. As the measurement temperature increases electron-ole pairs are generated in the semiconductor [16,18]. This produces no effect in the shift n the negative biased region but produces significant effect in the positive biased region. Electrons produced from the generation of electron hole pairs due to increase in emperature are attracted towards the surface below the gate. This results in accumulation f electrons in this region. Thus with increasing temperature, threshold voltage, V_{th} is eached at lower voltage due to this effect [8,17,18]. Measurement at room temperature V_{th} occurs at higher gate voltage since accumulation of electrons are only due to nversion layer under the gate and induced reversed p-n junction below the gate.

The increase in the minimum capacitance is also due to the generation of electron ole pairs with the increase in measurement temperature. The increase in electrons and oles result in a reduction in the depletion width thus increasing the capacitance value.

Another significant observation is the reduction in fluctuations of the capacitance n the "turn-off" voltage region when the measurement temperature is above 125°C. luctuations are also small in this region for the C-V_G plot measured at room emperature. When C-V_G measurements are done at temperatures of 50°C, 75°C, 100°C nd 125°C, thermal generation of electron-hole pairs results in increase in capacitance owever recombination process is also occurring at these temperatures [18,24] thus ausing these fluctuation.

4.4 High Frequency Capacitance-Voltage Characteristics of Device: Effects of Annealing on Device

Figure 4.10 shows the high frequency C-V_G curve measured across the Gate-Source structure of the n-channel enhancement mode power MOSFET at different annealing temperatures. The effect of annealing temperature on the Figure 4.10 differs from the effects of measurement temperature on the C-V_G characteristics. The results strongly confirms earlier results that the shift in the C-V_G curve only observed in the negative biased region when annealed at 400°C towards zero gate voltage is due to the surface state charges, Q_{SS} present in the oxide [16,18,20,24,32]. These surface states as mentioned earlier are due to excess ionic silicon in the oxide. No effect on the C-V_G curve in the positive biased region is observed since after annealing, the device is cooled to room temperature and measurements are done at room temperature. Thus, generation of holes and electron due to thermal effects is not present.

Annealing the device at 400°C results in broken Si-O bonds at the surface [10,11,18,24]. This results in interruption in the periodicity of the lattice at the surface, creating fast surface state. These states present in the forbidden gap are dependent on the bending of energy bands. When the energy band bend up wards away from the Fermi level, the probability of occupation of these states is zero thus has no effect on the capacitance of the p-type MOS structure. However, when the energy band bends down ward towards the Fermi level, the probability of occupation of these states increases to unity thus increasing the capacitance. This explains the significant increase in the capacitance at voltages beyond the flatband voltage and before the surface goes into inversion for the device annealed at 400°C.

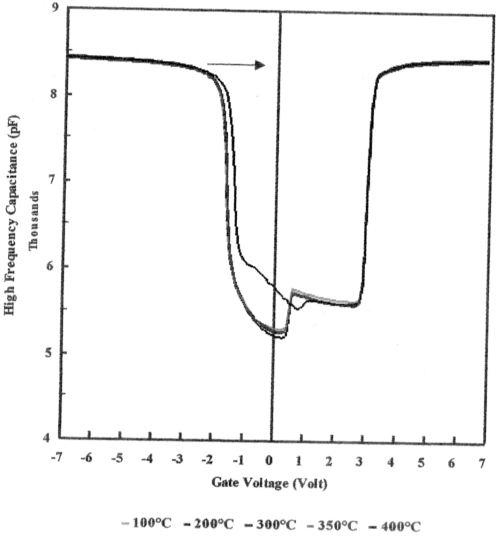


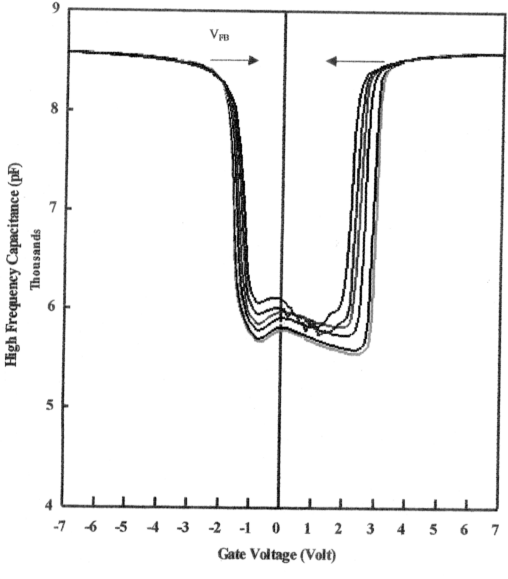
Figure 4.10: High Frequency Capacitance-Voltage ($C\text{-}V_G$) measurement results across Gate-Source structure of the n-channel enhancement mode power MOSFET device: Effects of Annealing on Device.

Also, the shift towards zero gate voltage when annealed at 400°C, although very small, is due to reduction in excess ionic silicon in the oxide. Since annealing is done in air, oxygen in the air are able to diffuse into the silicon dioxide structure and reduce these excess ionic silicon which contribute to the decrease the concentration of surface states in the oxide. This effect is also observed when a MOS structure is annealed in oxygen [24].

5 High Frequency Capacitance-Voltage Measurement Results of Device Annealed at 400°C at Different Measurement Temperatures

Figure 4.11 shows the high frequency Capacitance-Voltage ($C\text{-}V_G$) measurement sults across Gate-Source structure of the n-channel enhancement mode power OSFET device annealed at 400°C. These $C\text{-}V_G$ curve characteristics for the device nealed at 400°C (Figure 4.11) shows a similar trend as the $C\text{-}V_G$ curves of the non-nealed device (Figure 4.9) measured at different measurement temperatures. However, e shift of $C\text{-}V_G$ curves towards zero gate voltage is uniformly gradual both in the gative and positive bias region. For the non-annealed device, the shift is only gnificant in the negative biased region when the measurement temperature is above 0°C. The capacitance measured at zero gate voltage increases with measurement mperature. Beyond the zero gate voltage the capacitance decreases to minimum before creasing significantly to a maximum at threshold voltage but for measurement at 150°C d 175°C, the capacitance decrease to minimum but a slight increase is observed before aching threshold voltage.

The shift in the $C\text{-}V_G$ curves in the negative region, as in the non-annealed device due to surface state charges in the oxide [18,20,24,32]. However, these charge ecreases uniformly with measurement temperature resulting in the uniform shift of the rve towards zero gate voltage. The shift in the positive bias region is similar to the non-nealed device due to similar reasons quoted earlier. However, the presence of fast rface states increases with measurement temperature and most obvious when annealing temperature of 150°C and 175°C. This is deduced from the dominant increase the C-$_G$ plot at zero gate voltage. These effects show that, thermal generation of electrons and le pairs in this annealed device also result in disruption of the lattice structure.



gure 4.11: High Frequency Capacitance-Voltage ($C\text{-}V_G$) measurement results across Gate-Source structure of the n-channel enhancement mode power MOSFET device annealed at 400°C at different measurement temperatures.

In this annealed device, fluctuations in the capacitance values in the "turn-off" voltage region are observed at measurement temperatures of 150°C and 175°C which is reversed of the non-annealed device (Figure 4.9). The increase in concentration of fast surface states at the interface in the annealed device results in lower probability of recombination of the thermally generated electron-hole pairs, thus capacitance values are stable in this region. However, when the measurement temperature is high (150°C and 175°C), the generation of electron-hole pairs is higher thus recombination process increases as the number of electrons produced are larger than the number of fast surface states at the interfaces.

Figure 4.12 shows the variation of capacitance value at zero gate voltage with measurement temperature of the non-annealed device and the device annealed at 400°C. Generally, the capacitance in the device annealed at 400°C is higher than capacitance in the non-annealed device. This is due to the presence of broken Si-O bonds at the interface when device is annealed at 400°C. Dangling bonds which results from the broken Si-O bonds causes disruption of the lattice periodicity [16,18,10,11]. These results in more fast surface states being formed at the interface. In both cases, the capacitance across the gate-source terminal increase with measurement temperature with exception of the non-annealed device when annealed at 100°C where a decrease in the capacitance value is observed. Referring to Figure 4.12, the capacitance-voltage plots of the non-annealed device at measurement temperatures below 125°C fluctuates noticeable in the "turn-off" voltage region where the capacitance decrease in value and this includes the capacitance at zero gate voltage. Thus the error is larger and this could be the explanation in the inconsistency of the trend. However, with the increase in measurement temperature,

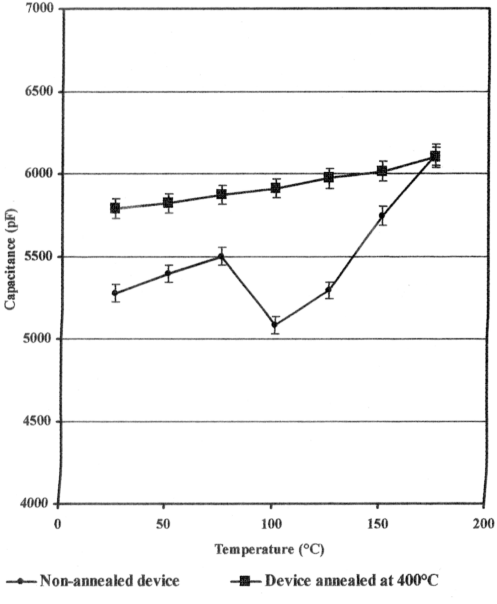


Figure 4.12: Capacitance at zero biased gate $V_G = 0$ versus temperature.

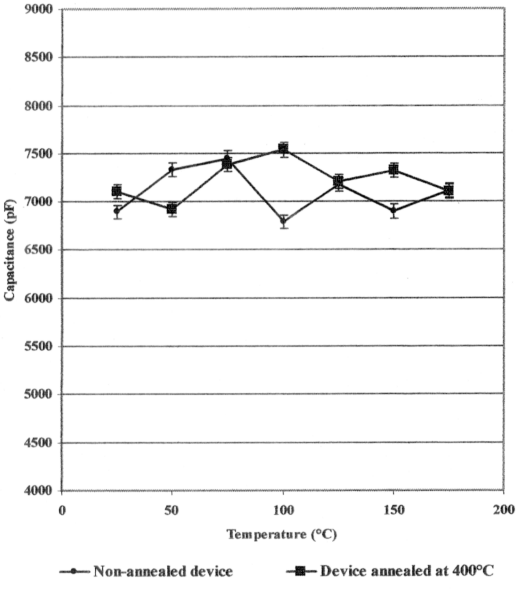


Figure 4.13: Capacitance at $V_G = V_p$ (peak voltage) versus temperature.

thermal generation of electron-hole pairs results in electrons being trapped in the fast surface states thus increasing the capacitance.

Figure 4.13 shows the variation of capacitance at $V_G = V_P$ (peak conductance voltage) at different measurement temperatures for the non-annealed and annealed devices. No significant variation is observed in both cases. Thus, annealing does not have any significant effect at the "turn-on" voltage of the device