# Chapter 5

# High Frequency Conductance-Voltage Measurements On The n-Channel Enhancement Mode Power Device: Results and Analysis

## 5.1 Introduction

The High Frequency Conductance-Voltage (G-V) measurement results of the n-channel Enhancement Mode Power MOSFET device studied in this work are presented, discussed and analyzed in this chapter. This chapter begins with section 5.2.1 with the presentation and analysis of the G-$V_G$ characteristics of the device across the Gate-Source (G-S) structure. The measurement across the G-S structure is further studied in section 5.3 with measurement done at different temperatures ranging from 25°C to 175°C. Since the switching properties of the device is strongly determined by electrical characteristic of the G-S structure [1,6,8,21], measurements are done across the G-S structure only. The effects of measurement temperature on the G-$V_G$ characteristic across this structure are also analyzed. Exposing the device to high temperatures is expected to produce some significant effects on the performance of the device. High frequency G-$V_G$ results obtained across the G-S structure of this device annealed at temperatures between 100°C and 400°C are presented and studied in section 5.4. Finally, the G-$V_G$ results of device annealed at 400°C at different measurement temperatures are presented and analyzed.

## 5.2 High Frequency Conductance-Voltage Characteristics of Device

### 5.2.1 Measurements across Gate-Source Structure

Figure 5.1 shows the gate to source (Figure 5.2) high frequency G-$V_G$ curve for the n-channel enhancement mode power MOSFET device. The conductance value saturates at 340 mS at voltages larger than 3V to 1.5V in the positive and negative biased region respectively. In the positive biased region, a conductance peak is observed between 2V and 3V. This voltage is referred to as the peak conductance voltage ($V_p$) in the positive biased region. The G-$V_G$ characteristics in the positive biased region shows that the device is a normally off n-channel device [5,18,26].

When a large negative voltage is applied to the gate, the surface of the p-type semiconductor region goes into accumulation, accumulating holes at the surface below the gate. In the n-type semiconductor region, the large negative bias result in the surface being inverted. In the accumulation region of p type semiconductor region, generation current is contributed by centers which are within the depletion region of the metallurgical p-$n^+$ junction while in the inversion region, generation current is contributed by centers within the surface depletion region, i.e the depletion region of the field-induced junction [24]. The contribution of generation current in the p-$n^+$ metallurgical junction is related to the surface depletion region, $X_d$. When the surface is accumulated, the depletion region is zero, thus, generation current due to this contribution is minimal. However, when the surface is depleted, and $X_d$ increases with the increase in gate voltage, this current component increases. Once the surface is inverted, $X_d$ reaches its maximum value and hence there will be no further increases in this current component. However, while the surface is depleted, recombination-generation centers at the oxide-silicon interface provides another contribution to the generation current. This

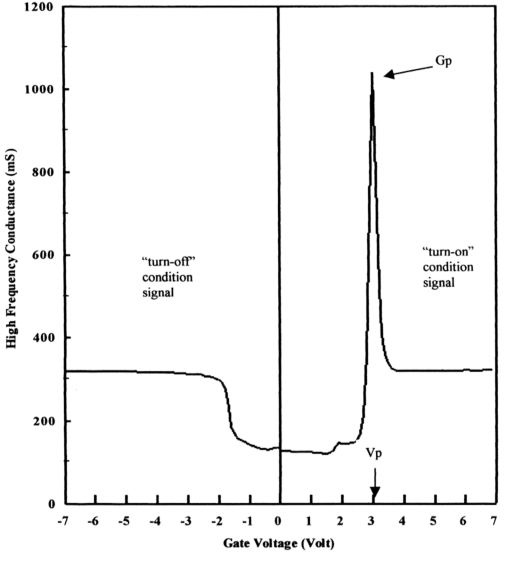



Figure 5 .1: High Frequency Conductance-Voltage ($G\text{-}V_G$) measurement results across **Gate-Source structure** of the n-channel enhancement mode power MOSFET device at room temperature 25°C.

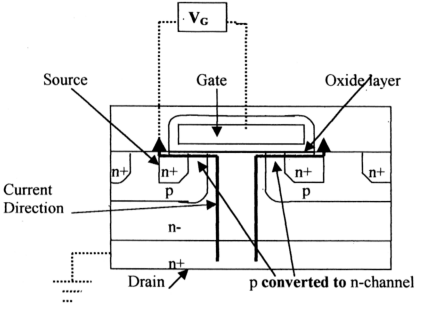



Figure 5.2: Shows the cross sectional of the gate to source structure of n-channel enhancement mode power MOSFET. [6,22]

ontribution results in a peak in positive bias region of the gate voltage. The constant onductance observed in the large negative biased region is thus contributed by the field nduced junction at the surface of the n⁻ type semiconductor region.

In the n- type semiconductor region, a reverse phenomena is observed. When a arge positive biased voltage is applied to the gate, the surface of this region is ccumulated with electrons, the contribution of generation current due to metallurgical p-+ junction is minimal since the depletion region at the surface of the n+ type emiconductor is minimal. The constant conductance in this large positive biased region s contributed by the field induced junction at the surface of the p type semiconductor

egion. When the n-type semiconductor surface is depleted of electrons, the depletion egion at this surface increases and reaches a maximum when the surface under the gate s inverted. This current thus increases and stops increasing when the surface inverts. The combination effects of the depletion regions of the n- and p type semiconductor surfaces esults is constant minimum voltage on the both sides of the zero gate voltage. When a arge negative voltage is applied to the gate the surface of the n- region is inverted esulting in the constant conductance due to generation current of the field induced unction at this surface.

Figure 5.3 presents a model explaining the characteristic high frequency G-V curve of the n-channel power MOSFET device measured across the source and the gate. gen.A represents the generation current produced by the field induced junction at the surface of the n- type semiconductor region. While Igen.B represents the generation current of the metallurgical p-n+ junction which increases as the depletion region at the surface of the p-type semiconductor increases and reaches a maximum in the positive biased region as shown by a broken line marked G. Igen.C is the generation current of the metallurgical p-n+ junction which increases as the depletion region at the surface of the n-type semiconductor increases and reaches a maximum in the negative biased region as shown by a broken line marked H. Igen.D is the generation current of the field induced unction at the surface of the p-type semiconductor. While Igen.E is the generation current at the oxide-silicon interface. Igen.F shows the combination effects of B and $\bar{C}$ which results in a constant minimum conductance in this region.

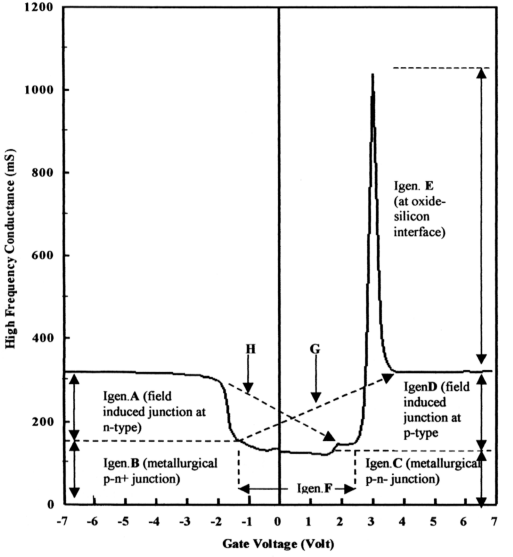



Figure 5 .3: Model explaining the variation of high frequency conductance with gate voltage.

## 2.2 Measurement across Gate-Drain Structure

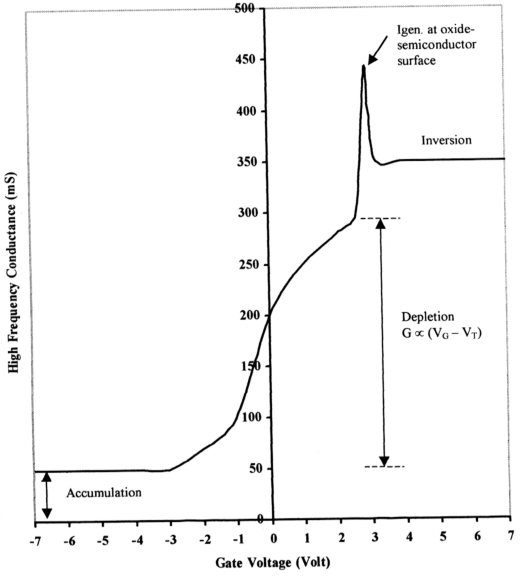



Figure 5 .4: High Frequency Conductance-Voltage ($G\text{-}V_G$) measurement results across **Gate-Drain structure** of the n-channel enhancement mode power MOSFET device at room temperature 25°C.

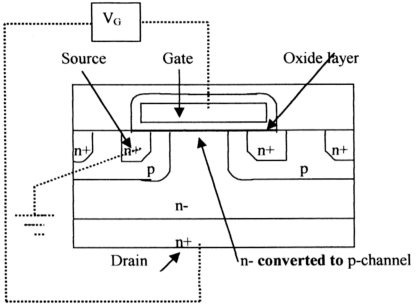



Figure 5.5: Shows the cross sectional of the Gate-Drain structure of n-channel enhancement mode power MOSFET. [6,22]

Figure 5.4 shows the G-$V_G$ curve characteristics across Gate-Drain structure of the n- channel enhancement mode power MOSFET (Figure 5.5) at room temperature 25°C. The magnitude of the peak conductance here is very small when compared with the peak conductance has been occurred in the G-$V_G$ curve across gate-source structure in Figure 5.1. It suggests that the gate-drain structure is not suitable for fast gate switching and high current handling capability in the n-channel enhancement mode power MOSFET.

When a large negative biased is applied to the gate, conductance is small. Generation of holes and electrons in the depletion region of the field induced junction due to the surface of the n type semiconductor going into inversion is the only contributor to the conductance in this case. When the gate voltage is large and positive, conductance is

due to generation of holes and electrons in the depletion regions of the field induced junction at the surface of the p type semiconductor and also of metallurgical p/n+ junction [18,24]. When the surface under the gate goes into depletion (at low negative and positive gate voltages) conductance increases with increase in depletion width of the metallurgical p/n+ junction since conductance is contributed by generation of holes and electrons in the depletion region. Generation of holes and electrons in the depletion region at the oxide-semiconductor surface contributes to the peak conductance as in the Gate-Source conductance-voltage characteristics.

### 5.2.3 Measurement across Source-Drain Structure

Figure 5.6 shows the High Frequency Conductance-Voltage measurement results across Source-Drain structure (Figure 5.7) of the n-channel Enhancement Mode Power MOSFET device at room temperature 25°C. The conductance minimum in the negative biased region because the p/n-/n+ junction was under reverse biased mode [16,18]. The conductance is increasing gradually with the higher application of positive voltages. At higher positive voltages, the electron-hole pairs recombination rate is increased and produced higher density of carries in this junction. A significant increased of conductance was observed at positive biased region roughly about 0.6 V biased. This is the "turn-on" potential of the junction. The conductance then saturates beyond this turn-on potential.

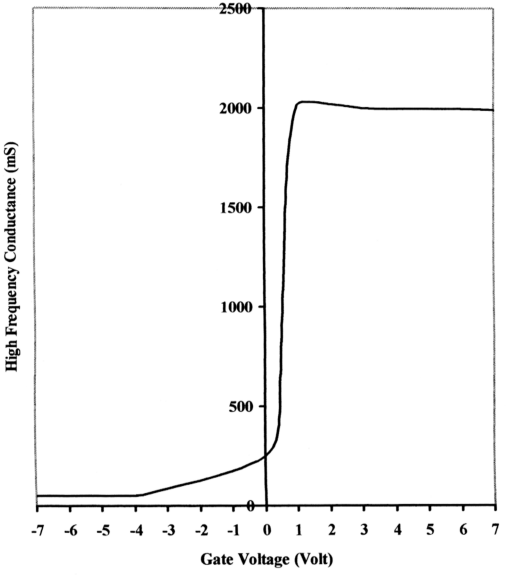



Figure 5 .6: High Frequency Conductance-Voltage ($G\text{-}V_G$) measurement results across **Source-Drain structure** of the n-channel enhancement mode power MOSET device at room temperature 25°C.

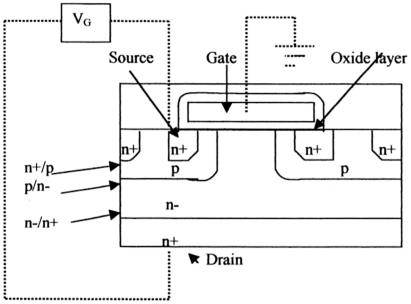



Figure 5.7: Shows the cross sectional of the Source-Drain structure of n-channel enhancement mode power MOSFET. [6,22]

## 5.3 High Frequency Conductance-Voltage Measurement Results At Different Measurement Temperatures across Gate-Source Structure

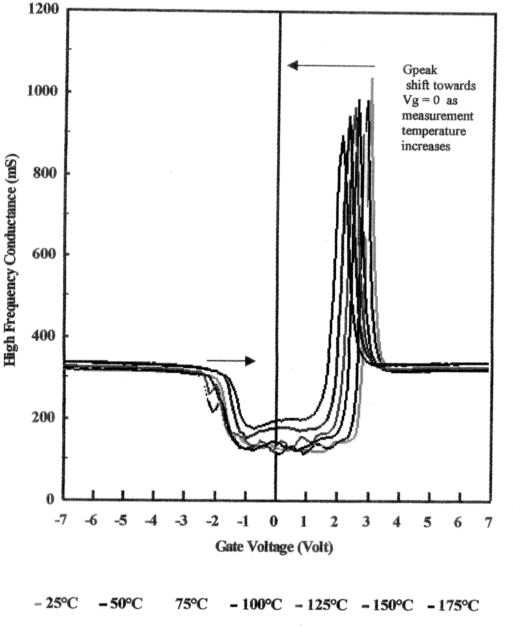



Figure 5 .8: High Frequency Conductance-Voltage ($G\text{-}V_G$) measurement results across Gate-Source structure of the n-channel enhancement mode power MOSFET device at different temperatures.

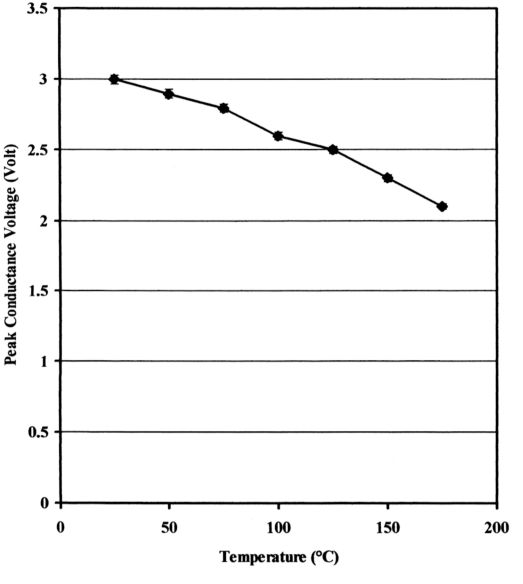



Figure 5 .9: Variation of Peak Conductance Voltage with measurement temperature.

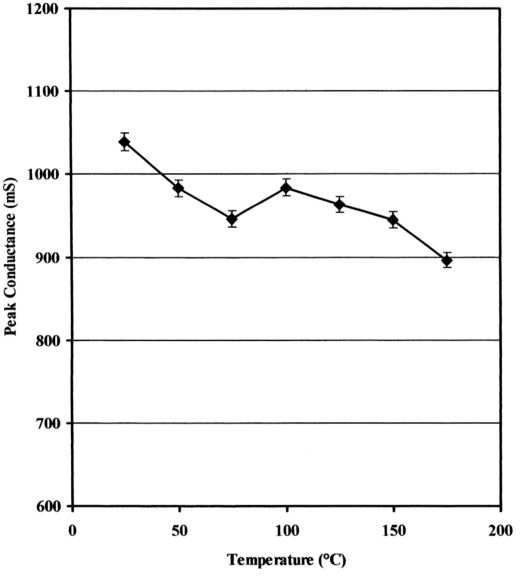



Figure 5 .10: Variation of Peak Conductance with measurement temperature.

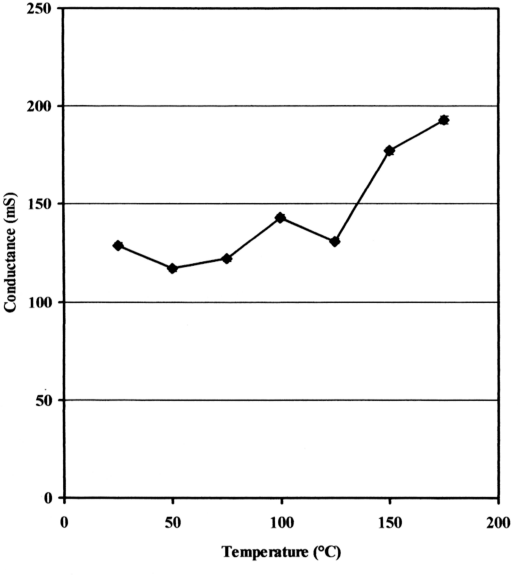



Figure 5 .11: Variation of conductance value at zero gate voltage with measurement temperature.

Figure 5.8 shows the G-$V_G$ across Gate-Source structure of the n-channel enhancement mode power MOSFET device at different temperatures. The conductance increases with the measurement temperatures especially at 150°C and 175°C in the both large negative and positive biased regions. This is supported by the results in the Figure 5.11 where the variation of conductance value at zero gate voltage showed that the conductance increased with these two measurement temperatures. It is because at higher temperatures the rate of thermal generation holes and electrons is higher and this results in the increase of conductance [16-18].

The G-$V_G$ curve shifts towards zero gate voltage at measurement temperatures 150°C and 175°C in the small negative biased region. As in the C-$V_G$ at different temperatures, increasing measurement temperatures result in the decrease in surface state charges and this result the flat band voltage shifting towards low negative voltage [20,24,32]. The G-$V_G$ curve which include the conductance peak voltage, $G_p$ shifts towards zero gate voltage at different measurement temperatures in the small positive biased region. It is because at higher temperatures, the thermal generation of electron and hole pairs is higher resulting in faster rate of increment in depletion width, thus inversion occurs at lower positive voltage (Figure 5.9).

In addition to this, there is a uniform shift of G-$V_G$ towards zero gate voltage in the positive biased region as compared to the negative biased region as the measurement temperature increases. The concentration of donor ions is higher in the p-n+ junction than in the p-n- junction. The former and the latter effect the voltage at which the junction goes into depletion in the negative and positive biased region respectively. Thus with lower concentration of donor ions, the junction goes into depletion at lower gate voltage

which is observed in the positive biased region at even the lower measurement temperatures. The shift in the G-$V_G$ curve is observable at lower temperatures in the positive biased region while the G-$V_G$ shift in the negative biased region is significant at only temperatures 150°C and 175°C.

Figure 5.10 shows the peak conductance decreases with measurement temperature. The peak conductance is dependent on the recombination of holes and electrons at the oxide-silicon interface (refer Figure 5.3) before the surface of the p-type semiconductor goes into inversion [24]. Since the peak conductance voltage decreases with increasing temperature, the lower voltage results in lower recombination generation centers thus decreasing the peak conductance. The "turn-on" current is thus reduced with increase in temperature.

Figure 5.11 shows the variation of conductance value at zero gate voltage with the measurement temperature. This conductance represents the "turn-off" current of the device. An increase in the conductance value with increase in temperature is observed when the measurement temperature is 150°C and 175°C. At these temperatures significant number of electrons are excited into the conduction band thus increasing the "turn-off" conductance.

## 5.4 High Frequency Conductance-Voltage Characteristics of Device: Effects of Annealing on Device

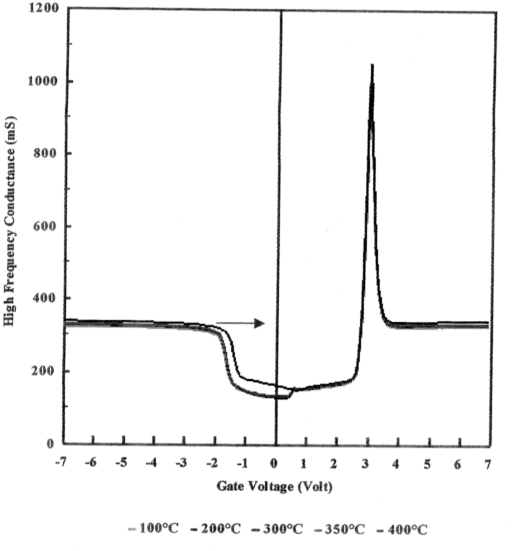



Figure 5.12: High Frequency Conductance-Voltage Characteristics of Device: Effects of Annealing on Device.

Figure 5.12 shows the high frequency conductance-voltage characteristics of evice at different annealing temperatures. An increase in conductance is observed in the egative biased region and where the gate voltage is slightly less than 1 volt. In the ositive bias region, at gate voltage larger than 1 volt, the G-$V_G$ plots showed almost no hange. When annealed at 400°C, some Si-O bond breaks leaving behind dangling bonds ithin the oxide and at the interface [5,10,11,20,24,32]. This results in disruption of the eriodicity of the lattice at the surface. A high density of states called fast surface states eintroduced into the forbidden gap near the semiconductor surface. These states can act s a generation recombination centers for electrons and holes [18,24]. In the negative iased region, these states increases the generation of holes and electron pairs. This is ecause fast surface states are dependent on energy band bending. In the negative biased egion, the surface of the p-type semiconductor is in accumulation, the energy band is ent upwards away from the fermi level. The fast surface states are also bent in the same manner [24], thus the probability of electron occupation is zero. However, in n-type semiconductor surface which is in inversion, the energy band is bent towards the fermi evel, thus probability occupation of electrons is unity. This result in these states ecoming active centers for generation of electron-hole pair thus increase conductance. In the positive biased region, the surface of the p-type semiconductor is in inversion mode, the n-type in accumulation mode. Thus, probability of fast surface states in the p-type semiconductor surface is unity but zero for the n-type semiconductor surface. The majority carriers of p-type semiconductor is holes, thus annealing shows no significant effect in the positive biased region.

## 5.5 High Frequency Conductance-Voltage Measurement Results of Device Annealed at 400°C at Different Measurement Temperatures.

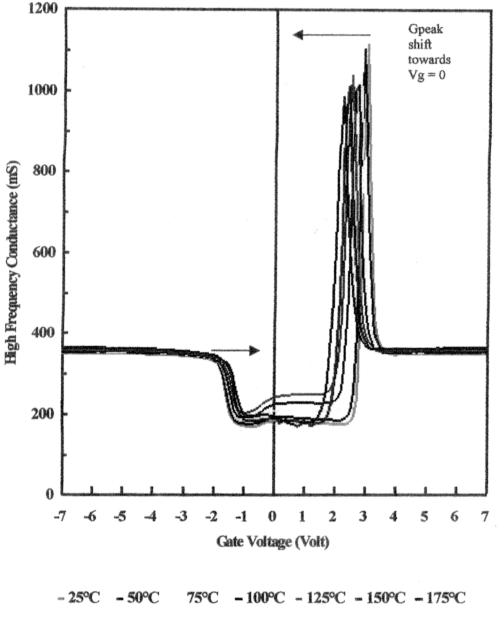



Figure 5 .13: Variation of G-$V_G$ for device annealed at 400°C at different temperatures.

Figure 5.13 shows the variation of conductance-voltage across Gate-Source structure of device annealed at 400°C at different measurement temperatures. The G-$V_G$ curves of the device annealed at 400°C show similar trend as the G-$V_G$ curve of the non-annealed device in the large positive and negative biased regions. Both the G-$V_G$ curves shift towards zero gate voltage in the positive and negative biased regions as the measurement temperature increases. The G-$V_G$ plot within the region where the surface depletes (conductance is lowest) shows a significant decrease in conductance when the measurement temperature is above 125°C. This trend is contrasting to trend observed in the non-annealed device.

For clarification, Figures 5.14, 5.15 and 5.16 are plotted. Figure 5.14 shows the variation of the peak conductance voltage with measurement temperature for the non-annealed device and the device annealed at 400°C. The trends are almost paralleled for both devices. With thermal generation and recombination of holes and electrons, the maximum depletion width is reduced as the surface inverts at a lower gate voltage [5,18,24]. Thus the peak conductance shifts towards low gate voltage as the measurement temperature increases.

Figure 5.15 shows the variation of peak conductance with measurement temperature for both the unannealed device and device annealed at 400°C. The peak conductances are generally higher for the unannealed device due to the present of fast surface states in the forbidden gap at the interface. The peak conductances in both cases decrease with the increase in measurement temperature. Increase in measurement temperature increases the rate of thermal generation of holes and electrons and this reduces the maximum depletion width thus decreasing the peak conductance [18,24].

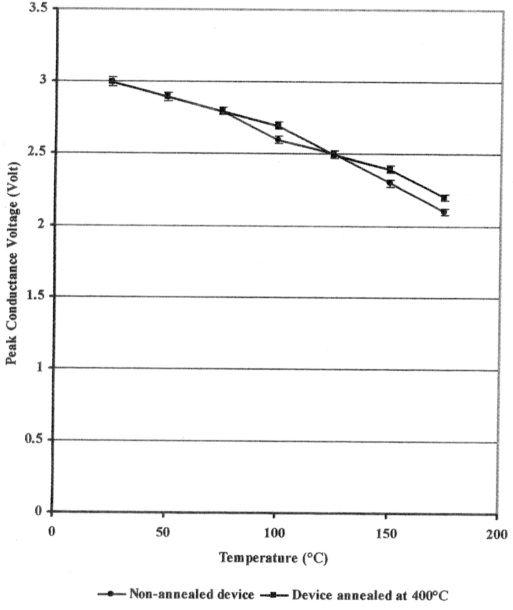



Figure 5 .14: Variation of Peak Conductance Voltage ($V_p$) for non-annealed device and device annealed at 400°C with measurement temperature.

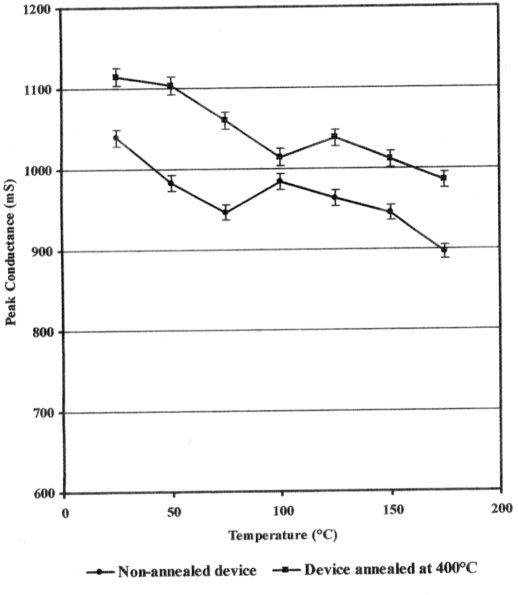
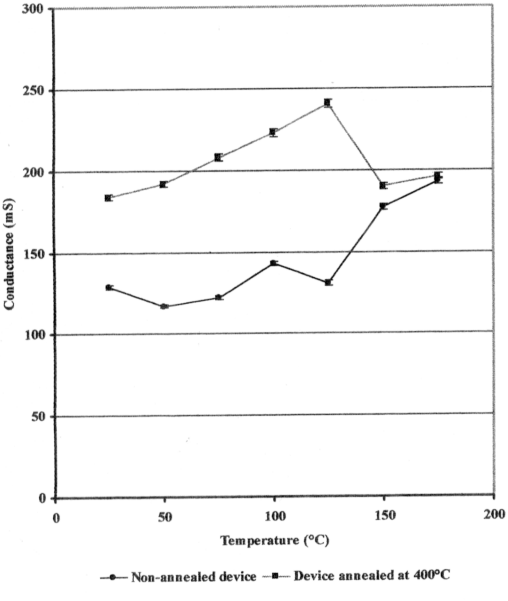



Figure 5 .15: Variation of Peak Conductance ($G_p$) for non-annealed device and device annealed at 400°C with measurement temperature.




igure 5 .16: Variation of conductance value at zero gate voltage for non-annealed device and device annealed at 400°C with measurement temperature.

Figure 5.16 shows the variation of conductance value at zero gate voltage with measurement temperature. The conductance for reasons explained earlier are always higher for the device annealed at 400°C. For the annealed device the conductance increases with the increase in measurement temperature at measurement temperature of 125°C and below. However, a significant drop in conductance is observed when the measurement temperature is 150°C and stabilizes at 175°C. At these temperatures, diffusion of oxygen atoms to the surface and passivating the dangling bonds result in decrease of fast surface states within the gap [20,24]. This phenomena could have resulted in the decrease in conductance at these temperatures.