Chapter 6

Conclusion and Suggestion for Further Works

6.1 Conclusion

Power semiconductor devices are used mainly as switches in power electronic systems and have vast applications in residential, commercial, industrial, transportation, utility systems, aerospace and telecommunication sectors. The power MOSFET device, compared to other controllable switches group of power Semiconductor devices has a low power capability but has the highest switching speed. In this work, the power semiconductor device studied is a commercially packaged n-channel enhancement mode power MOSFET device manufactured by Harris Semiconductor. The objective of this work is to study the high frequency Capacitance-Voltage (C-V) and Conductance-Voltage (G-V) characteristics of this device. Since fast switching speed is the most important advantage of power MOSFET device over other controllable switches group, the measurements in this work are mostly concentrated on the gate-source structure of this device as this structure determines the efficiency of the switching property of this device. The effects of higher operational temperatures on this device are studied by analyzing the C-V and G-V characteristics across this structure at different temperatures above room temperature within the recommended temperature range suggested by the manufacturer. The tolerance of the device components to extreme temperatures are also

studied from the effects of high temperature annealing on the C-V and G-V characteristics across the gate-source terminals of this device.

The room temperature high frequency C-V plot across the gate-source structure of the device demonstrated a p-type MOS characteristic in the negative biased region and an n-type MOS characteristic in the positive biased region. The high frequency G-V plot produce a switching property of a "normally OFF" n-channel device. The "turn-off" mode of the device was observed in the vicinity of the zero gate voltage and the "turn-on" mode was triggered when a small positive voltage close to 3 volts was applied across the gate-source terminals. At this voltage, the conductance peaked at a significantly high conductance relative to the "turn-off" conductance value. The insignificant difference between the peak conductance voltage and the threshold voltage demonstrate the fast and efficient switching property of this device.

Increasing the measurement temperature resulted in the shift of the C-V curves across the gate-source structure towards zero gate voltage both in the positive and negative biased regions. The presence of excess ionic silicon which behaved as surface state charges, Q_{ss} in the oxide was evident from the shift of the C-V curve in the negative biased region. These excess ionic silicon in the oxide were usually formed during the oxidation process. The reduction of these excess ionic silicon by reacting with oxidizing species present in the oxide as the measurement temperature increased resulted in the shift of the C-V curve towards zero gate voltage in the negative biased region especially when the measurement temperature exceeded 100°C. The generation of electron-hole pairs in the semiconductor produced the uniform shift of the C-V curves in the positive biased region towards zero gate voltage as the measurement temperature increased.

The high frequency G-V curves also shifted towards zero gate voltage in the positive and negative biased regions as the measurement temperature increased. The peak conductance voltage or, in this high performance switching device is equivalent to the threshold voltage decreased with the increase in measurement temperature. Thus, this lowers the "turn on" voltage of the device. The peak conductance value also decreased with increasing measurement temperature and combined with the lowering of the "turn-on" voltage indirectly reduced the power output of the device. The conductance value at zero gate voltage increased with increasing measurement temperature most significantly at measurement temperatures exceeding 100°C. This conductance representing the "turn-off" current of the device could be a measure of leakage current. Thus, operating the device at these elevated temperatures could result in higher leakage current.

The tolerance of this device to extreme temperatures was investigated by annealing the device at temperatures ranging from 100°C to 400°C for 30 minutes. The high frequency C-V curve measured at room temperature showed significant changes only when annealed at 400°C. Changes were only observed in the negative biased region when the p-type semiconductor surface was in depletion. In this region the curve shifted towards zero gate voltage and the capacitance was significantly higher. Broken Si-O bonds at the surface due to annealing at 400°C resulted in interruption in periodicity at the lattice creating fast surface states. These states in the forbidden gap are dependent on the bending of the energy band. When the energy band bend downwards towards the Fermi level, the probability of occupation of these states increased to unity thus increasing the capacitance. Increase in the number of electron hole-pairs generated resulted in more electrons being trapped in the fast surface states thus increasing the

capacitance as the measurement temperature was increased. The fast surface states also contributed to the shift towards zero gate voltage and higher conductance value in the G-V curve within the same bias voltage region when the device was annealed at 400°C. The increase in concentration of these states also increased the generation recombination centers for electrons and holes thus increasing the conductance. However, when the measurement temperature exceeded 100°C, these fast surface states decreased as the broken Si-O bonds were passivated by oxygen atoms in the oxide thus resulting in the decrease in the conductance. Annealing the device at 400°C had no effect on the peak conductance voltage at all measurement temperature. However, the peak conductance values were significantly higher for the device annealed at 400°C for all measurement temperatures due to the increase in concentration of fast surface states. The peak conductance value also decreased with increasing measurement temperature as in the non-annealed device but the rate of decrease was smaller as the measurement temperature exceeded 100°C for similar reasons quoted above. Thus, even though annealing at 400°C destroyed the casing of the device but the switching property of the device was not effected and the output power appeared to increase at the expense of a higher leakage current.

6.2 Suggestion for Further Works

Further studies on the properties of the n-channel enhancement mode power MOSFET device can be done. In this work, most of the studies are based on the high frequency C-V and G-V characteristics across the gate terminal of the device. High frequency C-V and G-V measurements across the source-drain and gate-drain structure of

the device at different measurement temperatures would produce interesting results to optimize the applications of this device. Low frequency C-V and G-V measurements also could produce interesting results to enhance further understanding of the device.

In this work, the effects of annealing of the device up to 400°C were analyzed. However, at this extreme temperature the casing was destroyed even though the device was still functioning. More work can be done on the material suitable for the device casing so that it can be used at extreme temperatures.

The effect of high frequency radiation on the device is another important aspect to be seriously considered. This device when used in power supply systems in satellites and space shuttles could be exposed to high frequency radiation in outer space. Studies on making these devices operational when exposed to this harsh environment would certainly be of great important to mankind.