

CHAPTER 4

READOUT CONTROL AND HALOMUONS

4.1 CAL Readout control (ROC) of the ZEUS Detector

The readout control of the calorimeter of ZEUS detector was extensive and fragmented in design. A Field Programmable Gate Array (FPGA) version of the readout control will give advantage over the old design as it will be single-board and compact, and easier to improve in the future. The FPGA-based readout control for the calorimeter of the ZEUS detector was developed on an Altera Cyclone with Verilog as the hardware description language and with Quartus II as the tool for software testing and simulation. The old circuit diagrams of the readout control modules were used to form basic building blocks of the readout control. This chapter will discuss how the system was developed and simulated for lab-scale testing before being downloaded onto the FPGA hardware for implementation.

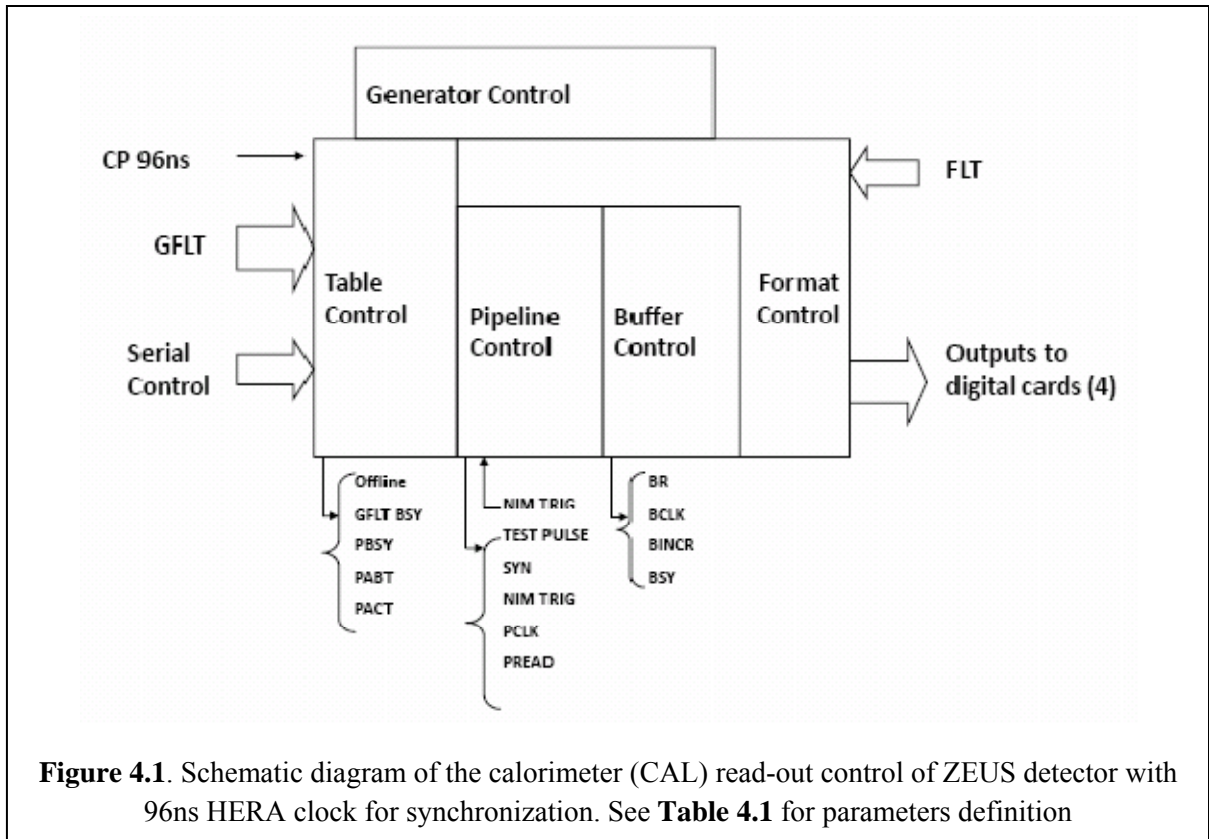
4.1.1 The Readout Controlling Modules

In the high energy physics experiment at HERA (Hadron-Electron Ring Accelerator), the proton beam with 920 GeV energy collided with an electron/positron beam (at 30GeV). As a result of the collision, quarks interactions within the accelerated protons and incoming electron/positron were observed and recorded by ZEUS detector, synchronized by the HERA clock at 96 ns or 10MHz. The read-out system controlling the data-taking of the calorimeter part of the detector consists of five analogue modules i.e. table, pipeline, buffer, format and generator modules, with more than 140 input and output signals interconnected to each other. **Figure 4.1** shows the schematic diagram of the calorimeter readout control of the ZEUS detector.

4.1.1.1 The Functions

In this project the analogue circuit diagrams, as well as the block diagram of the table, pipeline, buffer and format modules were used as bass to form the building blocks of a Field-Programmable Gate Array (FPGA) -based readout control, using Verilog as the hardware description language.

The readout electronics were ‘data driven’, i.e. the operation of the components was completely determined by the context provided by the data themselves [52]. The table module gave preset controlling data to the readout system; the pipeline selected which particular cell out of 96 samples [53], to trigger; the buffer keep interim data storage from the pipeline; and the format set the timing for the digitization of the output.



4.1.2 FPGA programming

The table module accepts 8-bit serial data from the universal computer interface card i.e. from table, format, pipeline, generator for its RAM (random access memory) data. The controller bits in the table module were synchronized with the 10MHz serial clock. Here, the readout control system was first isolated by giving flag 0, before each subsequent byte pushed the prior byte onto the next register in the chain [52]. Once set, the readout control was put on-line again, where the signals from GFLT (Global First Level Trigger) would determine the controlling sequence of the readout control. In the table module, an FPGA 16-bit shift and 8-bit shift register were design with Verilog to accept serial data and serial clock and compare them with the GFLT signals.

In the pipeline module, the signals from table control would determine which data in the 96 samples of the physics events for accept (ACT) or abort (ABT). While the ACT was true, the buffer controller would continue taking the physics data event and forward them to format controller for digital outputs. On receiving the ABT signal from the table module, the pipeline controller would notify the buffer to reject the current data taking.

Figure 4.2 gives the sequence of the readout control development; the table, pipeline, buffer and format modules were integrated into one FPGA-based module with Verilog.

4.1.3 Coding with Verilog

The converting of the modules was carried out based on the logic block diagram of the readout modules. Connecting inputs and outputs from/into each of the modules were identified. Smaller sub-modules i.e. shift register (8, 16-bits), multiplexers, JK, RS flip-flops, decoder, counter divider etc. were created and combined to form the four controlling i.e. modules table, pipeline, buffer and format, which were later, combined to form the main controlling module.

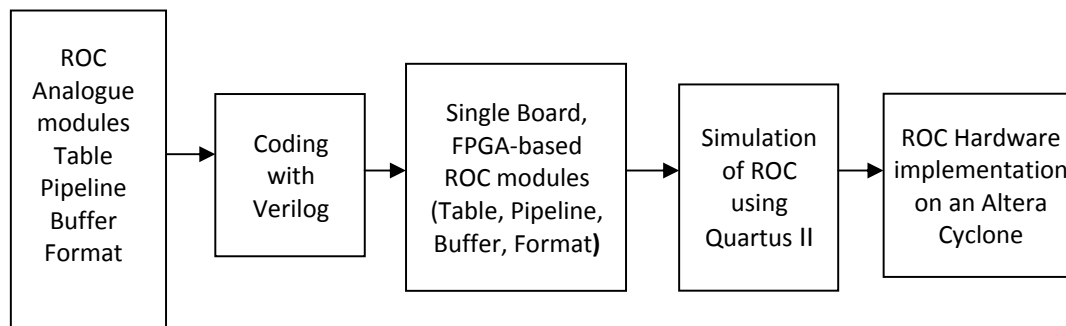


Figure 4.2 . The analogue modules of readout control (ROC) of the ZEUS detector were coded into single board, FPGA-based using Verilog before being simulated on Quartus II.

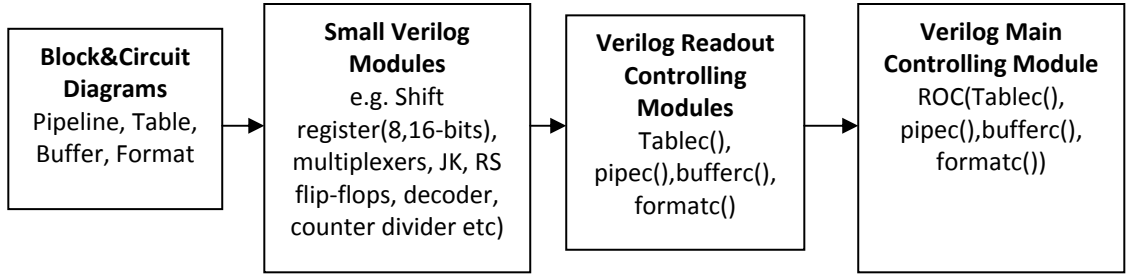
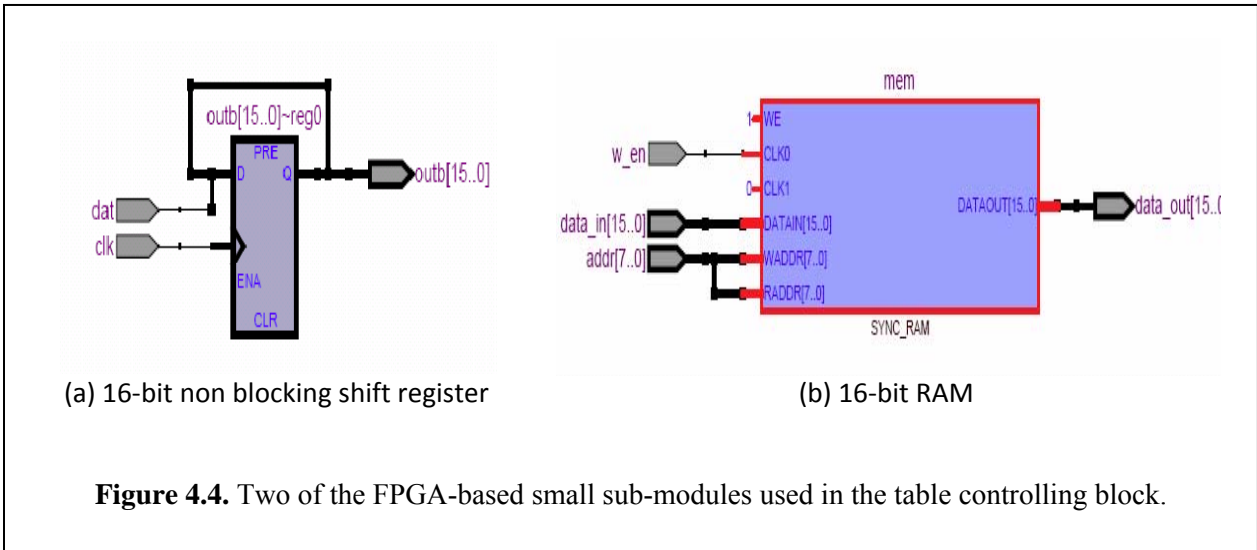


Figure 4.3. Coding sequence of the controlling analog read-out modules using Verilog. Coding were carried our starting with basic blocks, later combined to become the main controlling block

Figure 4.3 gives the coding sequence used in converting the analog table, pipeline, buffer and format modules into the FGGA-based read-out controlling module.

In **Figure 4.4**, two examples of the small FPGA sub-modules used in the ROC are given. Numerous sub-modules were build and combined together to form the controlling modules, which later integrated to form the main read-out control as given in **Figure 4.5**.

Figure 4.5, shows the RTL viewer of the FPGA-based readout control on Quartus II, with full layout of the CAL ROC main modules that integrated the pipeline, buffer, table and format modules to function as a single controlling block.



(a) 16-bit non blocking shift register

(b) 16-bit RAM

Figure 4.4. Two of the FPGA-based small sub-modules used in the table controlling block.

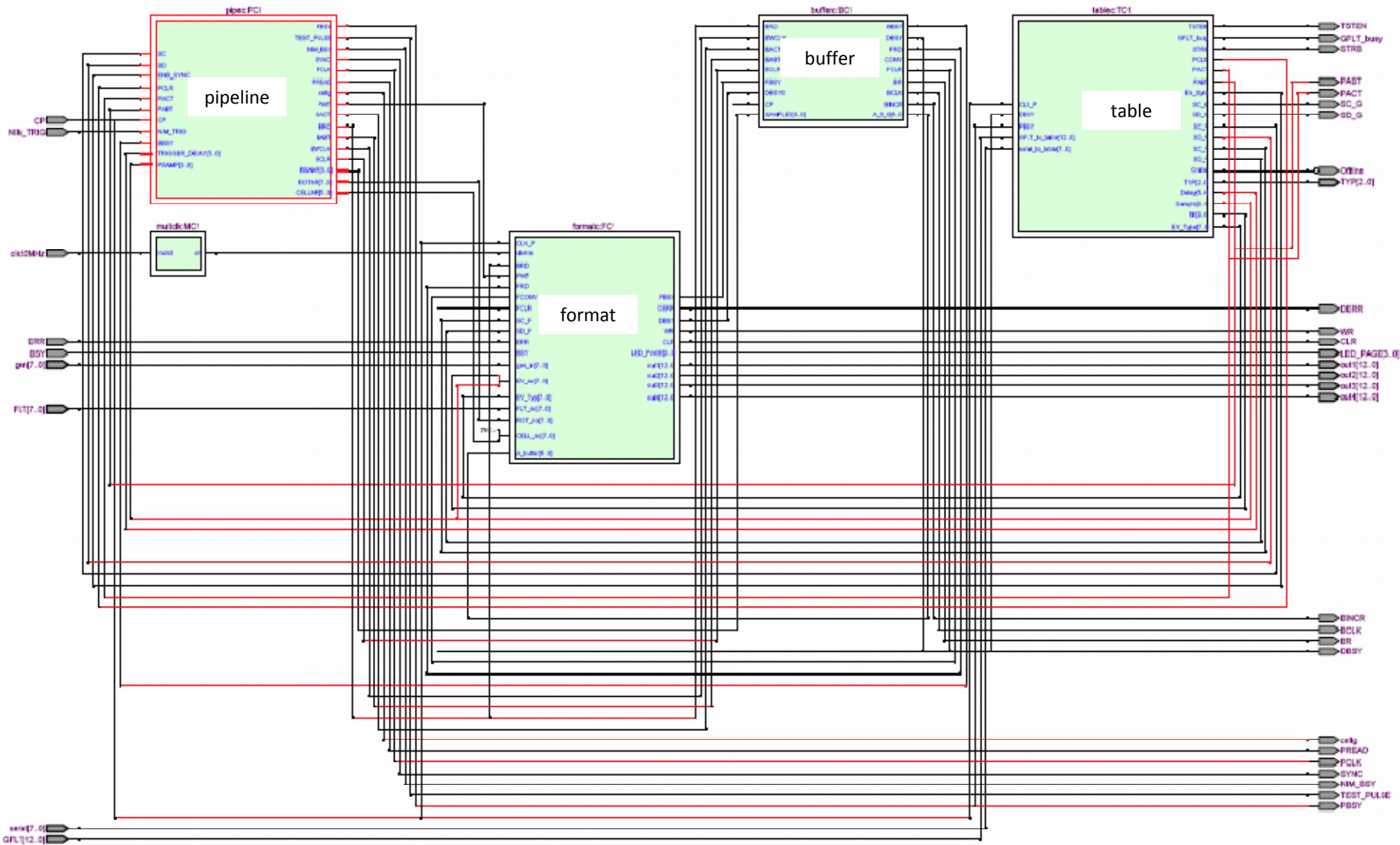


Figure 4.5 Full Quartus II RTL viewer of the FPGA-based readout control (ROC) for the calorimeter (CAL) of the ZEUS detector, showing the four main module i.e. pipeline, format, buffer and table, with inputs on the left and outputs on the right of the diagram.

4.1.4 FPGA Simulation and Results

The integrated FPGA-based modules in Verilog were simulated on Quartus II using the device settings of Altera Cyclone I. **Figure 4.6** shows the part of the vector waveform used in Quartus II for the simulation for serial data input. Each serial data consist of 4 bytes control data given to RAM in table module.

Each bit of the serial data is only counted on negative change of the clock edge, where subsequent byte pushes a prior byte up the 16-bit shift register.

In **Figure 4.7 (a)**, when the pipeline accept data PACT is triggered, the pipeline busy PBSY and the pipeline read PREAD are triggered with PCLK temporarily disabled. Here, the buffer read is flagged 0 and the BCLK is temporarily disabled. **Figure 4.7 (b)**, gives a closer look at the sequence of pipeline and buffer triggers upon abort ABT signal by GFLT. On a negative edge of ABT from GFLT, the pipeline abort PABT triggers and pipeline accept PACT is flagged down to 0. During the abort trigger, the buffer is still flagged 0 and only changes to 1 about 0.07 ms later, resulting in unused data being taken by the buffer instead of rejecting it.

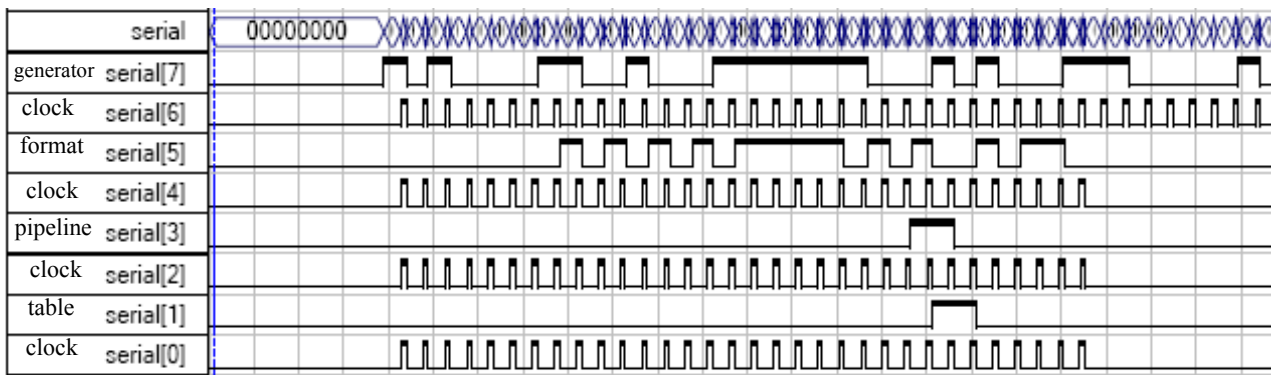


Figure 4.6 Serial data input to the FPGA-based readout control (serial[0] for table control, serial[3] for pipeline, serial[5] for format control, serial[7] for generator control; while serial[0],[2],[4],[6] were serial clock 10MHz)

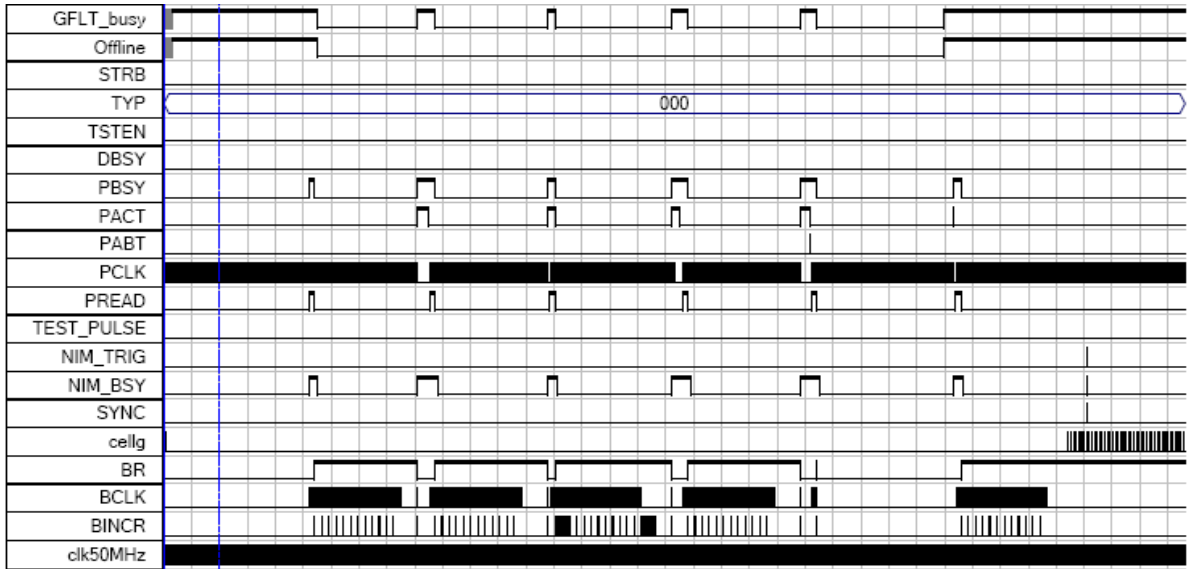


Figure 4.7a Output signals from the FPGA-based readout control

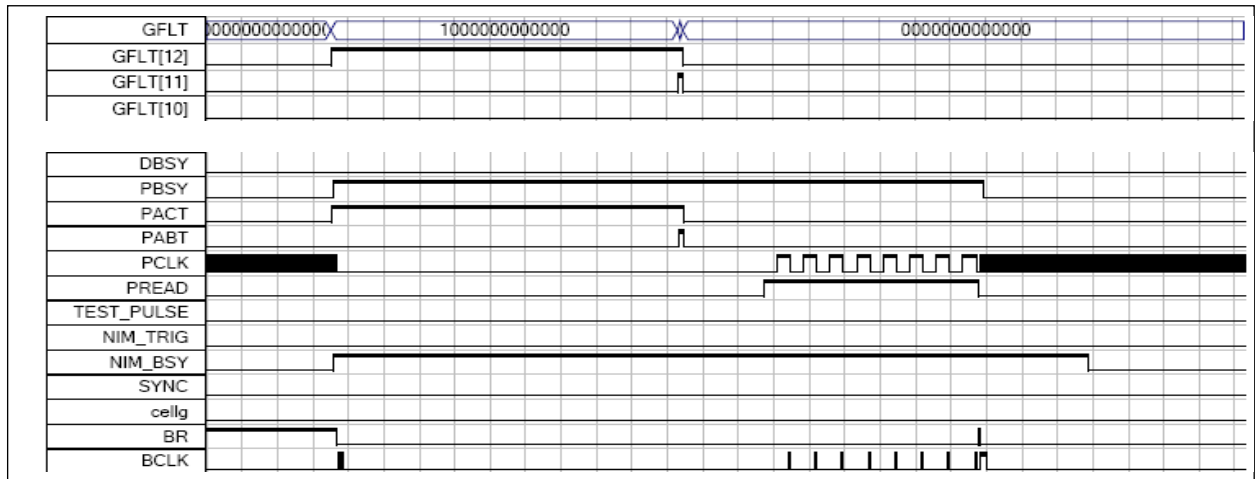


Figure 4.7b A close-up of the FPGA-based readout control showing the abort ABT signal from the pipeline control

Table 4.1 gives some of the output labels used the FPGA-based readout control (ROC) block, with the output waveform as given in **Figure 4.4 (a)** and **(b)**.

Table 4.1 Some of the output label from FPGA-based readout control (ROC) as shown in Figure 4.4a and its status

Output label	Output Status	Flag
GFLT_busy	GFLT busy	1
Offline	System is off-line	1
STRB	Strobe signal	0
TYP	Type of event	000
TSTEN	Test mode enable	0
DBSY	Data busy	0
PBSY	Pipeline busy	1
PACT	Pipeline accept data	1
PABT	Pipeline abort data	1
PCLK	Pipeline clock	counter
PREAD	Pipeline read	1
cellg	Number of bunch crossing	1
BR	Buffer read	1

4.1.5 FPGA-based ROC Power consumption

With the design FPGA-based readout control (ROC), simulation on Quartus II resulted in a total number of 123 input/output pins and 7,010 of logic elements used. In **Table 4.2**, the dissipated power calculated for the FPGA-based ROC is given, with a total of 189.61 mW of dissipated power expected for the design ROC. Of the three components, the core static power dissipation contributed the highest at 71% of the total power loss.

Table 4.2 Thermal dissipation of readout control block

Component	Power dissipated	percentage
Core dynamic power dissipation	35.73 mW	19%
Core static power dissipation	134.79 mW	71%
I/O power dissipation	19.09 mW	10%
Total thermal power dissipation	189.61 mW	100%

4.1.6 Hardware Development

The hardware of the readout control was carried out using Proteus software to design the PCB layout using an Altera Cyclone I FPGA chip, with a total of 37 chips i.e. 12 of the ECL-to-TTL type, 16 of the TTL-to-ECL type, 7 of the bus driver type and 2 of the for OR gate type.

In **Figure 4.8**, the fabricated printed circuit board (PCB) designed using Proteus software is shown. The figure, the FPGA kit with Altera Cyclone I chip is mounted in the middle of the PCB. The board was tested in laboratory using a -5.2V for V_{EE} and initial current I_{EE} supply of 0.5A and, a 5.0V for V_{CC} and initial current I_{CC} of supply 0.63A.

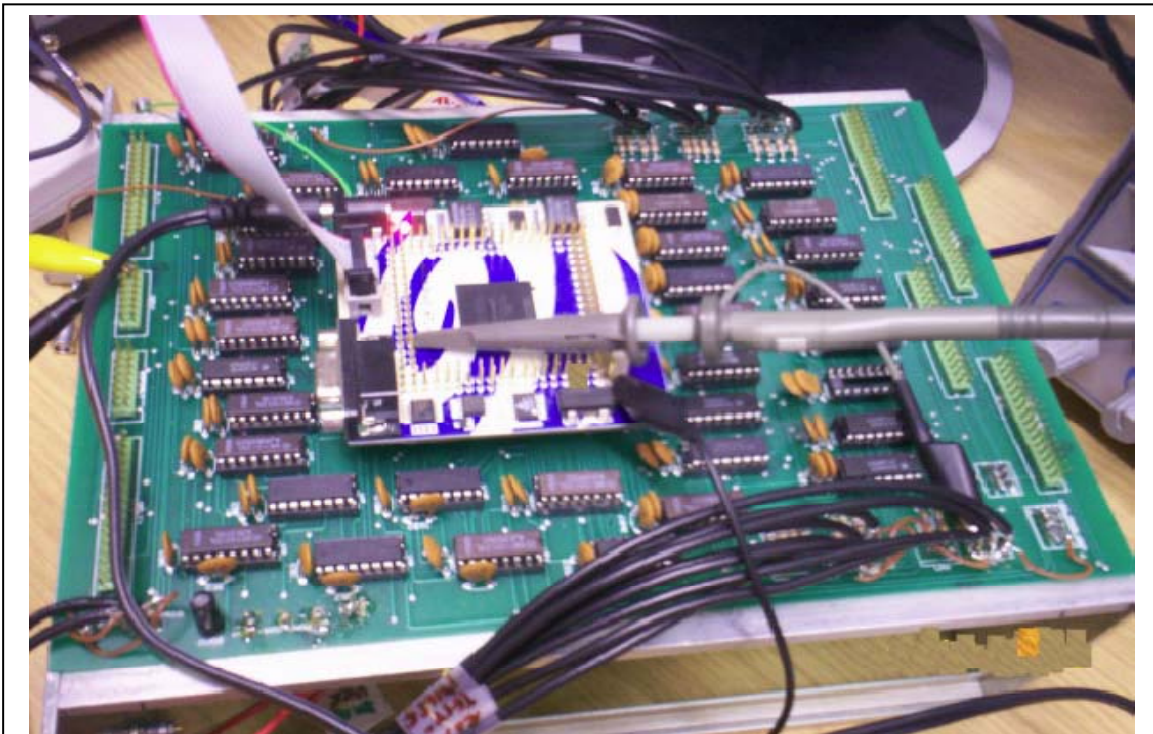


Figure 4.8 A 7inch by 11inch (17.5cm by 27.5cm) PCB designed using Proteus software, with the FPGA Altera Cyclone mounted in the middle and TTL-ECL, ECL-TTL and Quad Bus Driver chips mounted fully. The PCB was tested in laboratory using frequency generator and high current voltage supply

During laboratory test, the chips were mounted one by one on the PCB. Each time the voltage supply V_{EE} and V_{CC} dropped with mounted chips, the current adjusted again until the initial -5.2V and 5.0V respectively.

Figure 4.9 shows the plot of current I_{CC} (A) and I_{EE} (A) versus number of chips of TTL-ECL quad translator type, while **Figure 4.10** shows the same plot for quad bus driver type. In both figures, the currents increases I_{CC} and I_{EE} increased with the number of chips mounted on the PCB, after an initial plateau. For TTL-ECL quad translator type both I_{CC} and I_{EE} show the same trend, but in quad bus driver type chip the currents is higher with I_{CC} dropped lower before increasing.

In quad bus driver type chip, the power dissipation was 575 mW or a total of 6.9 Watt power dissipation produced by 12 chips, thus higher bias current was need than the TTL-ECL quad translator type .

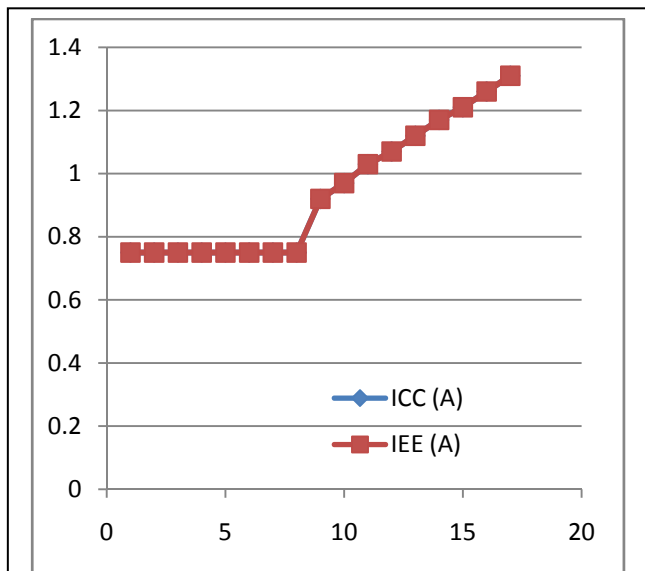


Figure 4.9 Plot of current I_{CC} (A) and I_{EE} (A) versus number of chips of TTL-ECL quad translator type (MC0124) showing the tendency the currents to increase with the number of chips

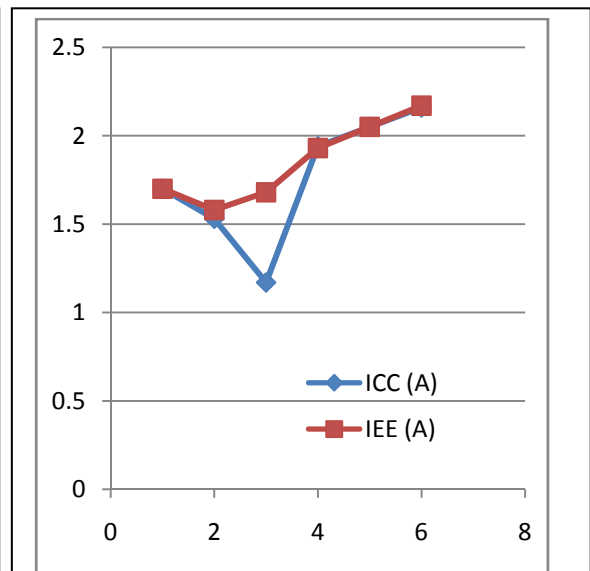
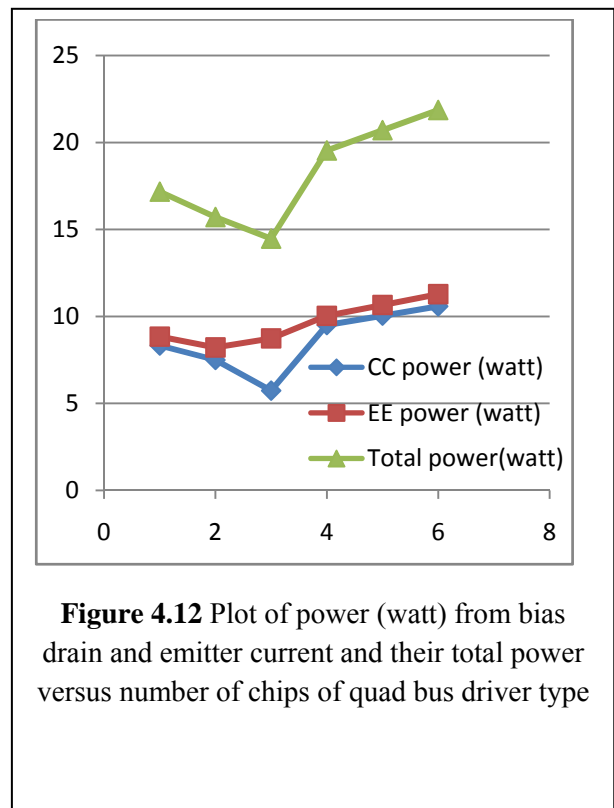
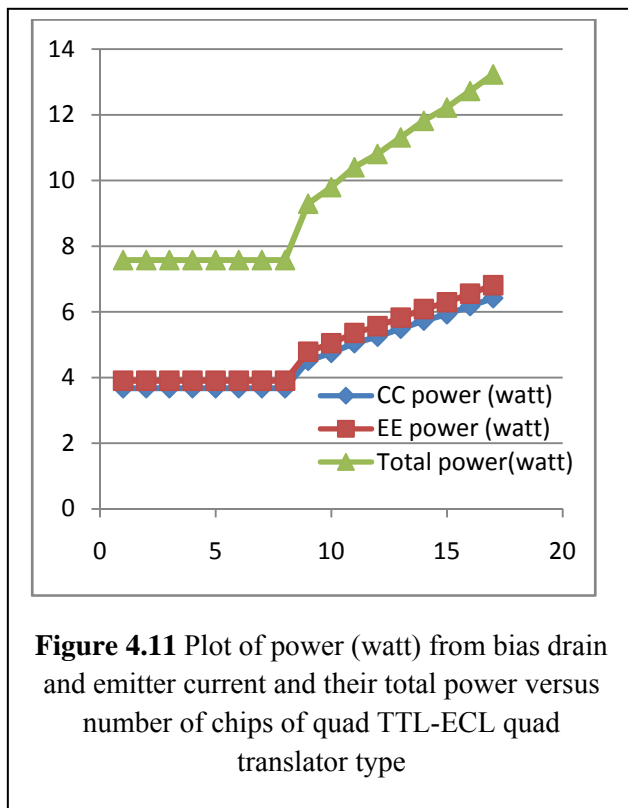


Figure 4.10 Plot of current I_{CC} (A) and I_{EE} (A) versus number of chips of quad bus driver type (MC0192) showing the tendency the currents to increase with the number of chips

In **Figure 4.11**, the plot of power (watt) from bias drain and emitter current and their total power versus number of chips for quad TTL-ECL quad translator driver is given, while **Figure 4.12** gives the same plot for quad bus driver. In both plots, the same trend as in **Figure 4.9** and **Figure 4.10** were observed. In these figures, the linear increase in bias currents and power after a certain number of chips mounted on the PCB indicates that improvisation of the PCB to remove excess heat dissipation is needed.



4.1.7 Summary

In this project, the four controlling modules of the analog readout control of the calorimeter of the ZEUS detector have been integrated into single FPGA-based readout controlling module on a single chip. The integrated FPGA-based module on a single chip besides compact is easier to modify in future. More work would have to be carried out to overcome glitches of the timing sequence of the present readout control

While the power consumption of the FPGA-based readout control on a single chip is quite high, nevertheless we have demonstrated that an FPGA-based readout control for at 96ns synchronized clock is feasible but needs more work to improve its performance especially on power dissipation.

4.2 The Halomuons in the ZEUS detector

In a high energy physics experiment, the cosmic muons and halomuons were normally used to calibrate the energy scale of the detector especially in the lower range. The properties of the halomuons that moves in a straight path i.e. from rear to the front end of the detector makes it a convenient entity to calibrate both ends of the detector in the range of 1GeV and for alignment purposes. The identification of halomuons will help to reduce background contamination during physics experiment, by its elimination from event selection.

In the ZEUS detector, the halomuons were produced upstream of the detector when the proton beam interacted with the rest gas during its acceleration prior to entering the detector, to produce π^+ (mean life of 2.6×10^{-8} s) that later decayed into μ^+ . The hard muons μ^+ travelled along with proton beam accelerated towards the RCAL become soft when hitting the veto wall prior to entering the ZEUS detector.

While the transversing halomuons may contribute to the background signals, it is particularly useful for alignment and calibration of the endcap region of the detector [57], as compared with cosmic muons used for the energy calibration of the barrel region of the detector. The halomuons were also used to determine if the energy scale of the calorimeter was correct in absence of dead material in front of the calorimeter, where the measurement of electron and hadron deteriorated substantially [57]. It was also used to study the long-term stability of muon response in each longitudinal section of the FCAL and RCAL, relative to the UNO signal [58].

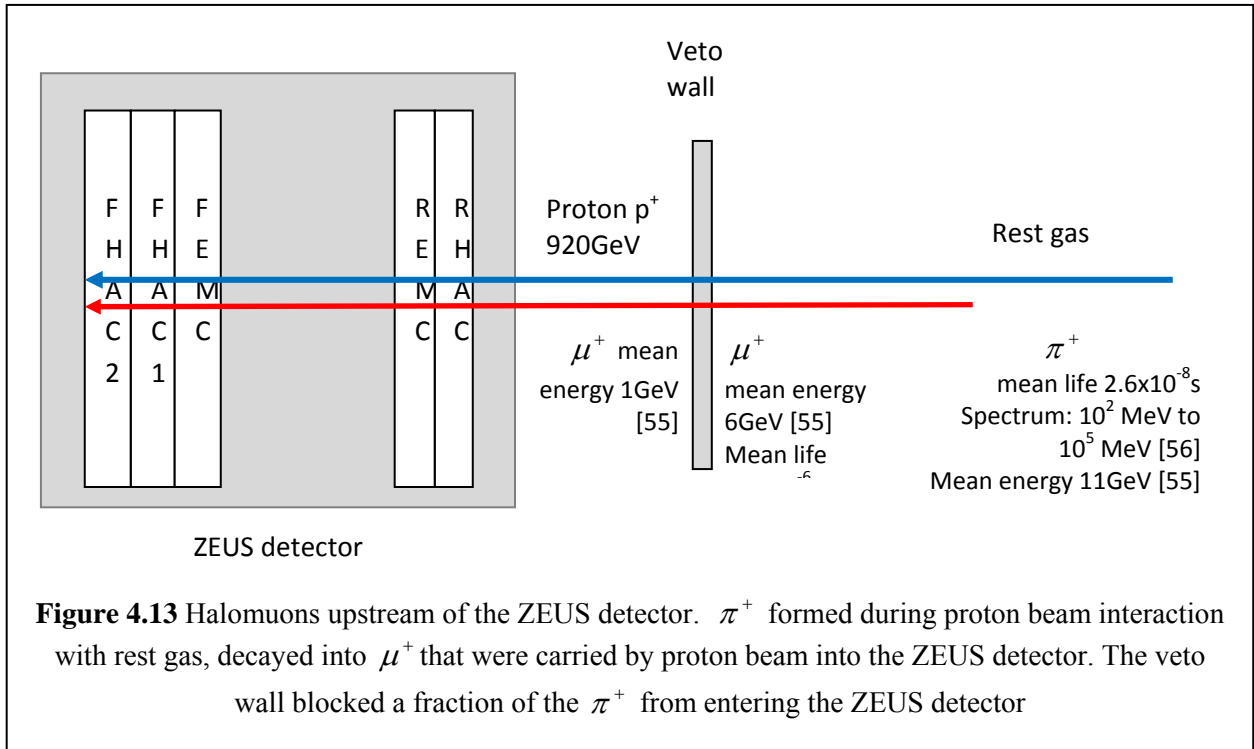
In this section, energies the soft muons traversing the ZEUS detector from RCAL to FCAL were identified using ORANGE and Fortran PAW routines.

4.2.1 Halomuons production upstream of ZEUS detector

Muon is the second heaviest charged lepton with electric charge of ± 1 and is 200 times more massive than electron (mass $m = 105.658369 \pm 0.000009$ MeV). It has mean life $\tau = 2.19703 \pm 0.00004) \times 10^{-6}$ s. The halomuons crossed the ZUES detector almost horizontally from RCAL to FCAL, depositing some of its energy in the electromagnetic calorimeter (EMCs) and hadronic calorimeter (HACs) of the detector ZEUS. The halomuons might also gave higher pulse rate to a physics event and contribute to global muons sampling along its trajectory in the detector.

In the ZEUS detector, the veto wall located at 7.5 m upstream of the interaction point, protected the central detector against the particles from the beam halo accompanying the proton bunches [13]. The halomuons from the decayed pions, were absorbed by the iron wall in the Veto Wall. Halomuons which were not absorbed by the iron wall transverse through the RCAL to FCAL.

Figure 4.13 shows the transversing of halomuons from the pion decay and moving along with the proton beam right into the ZEUS detector. Previous study has shown that the mean value of pion momentum spectrum of was about 11 GeV became softer to a mean 8GeV after hitting the shield. Here, the mean muon energy decaying from the pion was about 6GeV. The halomuons mean energy 6 GeV became soft to about 1GeV after hitting the veto wall prior to entering the ZEUS detector [55].



4.2.2 The EMCs and HACs in F/RCALs

Figure 3.9 in **Chapter 3** shows the layout of the electromagnetic calorimeter (EMC) and hadronic calorimeter (HAC) in the F/RCAL. In FCAL, there are two HACs i.e. HAC1 and HAC2, and one EMC i.e. FEMC. In RCAL, there is one EMC i.e. REMC and one HAC i.e. RHAC.

In **Figure 3.10a**, the direction of modules and towers of the RCAL as seen from the interaction point, is shown, with 23 modules in the i^{th} direction and 23 towers in the j^{th} direction. At position (12, 12) of RCAL, the beam hole will be visible.

As HERA tunnel was not centred with respect to the main detector, but shifted about +1 m in x-direction and +0.5 m in y-direction, more events in the upper-right corner of F/RCAL than lower left would be expected, where more low energy halomuons would be absorbed by a significantly bigger shielding material in front of the detector [59].

4.2.3 The Algorithm for halomuon analysis

In calorimeter reconstruction program, the identification of particles or group of particles is performed using the particular shower properties of the particle and the segmentation of the calorimeter. Here, the muons are defined as isolated tracks of minimum ionizing energy passing through the full depth of the calorimeter [9]. In case of the halomuons, its transverse path from RCAL to FCAL could be detected from the energy deposits in the HAC1, HAC2 and FEMC cells of the FCAL and the corresponding (origin) halomuons in HAC and RMEC cells of the RCAL.

In selecting the halomuon candidates from the F/R CAL cells, the following conditions were used [60]:

- (i) Halomuon trigger bits should be fulfilled

In 2004, trigger logic bit FLT 37 was used to associate potential halomuon candidate's transversing the ZEUS detector. In 2006, the slot 56 is used to store trigger logics for halomuons. This GFLT slot was moved to 17 in 2007 (from run 62595 onwards).

- (ii) There should be energy deposits above the background level, in both FCAL and RCAL cells

In selecting potential candidates from Caltru table, a minimum energy of 0.15GeV was required to eliminate background noise.

- (iii) Time difference between FCAL and RCAL should be within 5-18 ns from interaction point

For each halomuon candidates reaching the RCAL a time of ~ 5 ns from the interaction would be recorded and on reaching FCAL, a time of ~ 18 ns be recorded. This would ensure that only candidates tranversing from RCAL to FCA would be selected.

(iv) The selected F/RCAL tower should be isolated, i.e

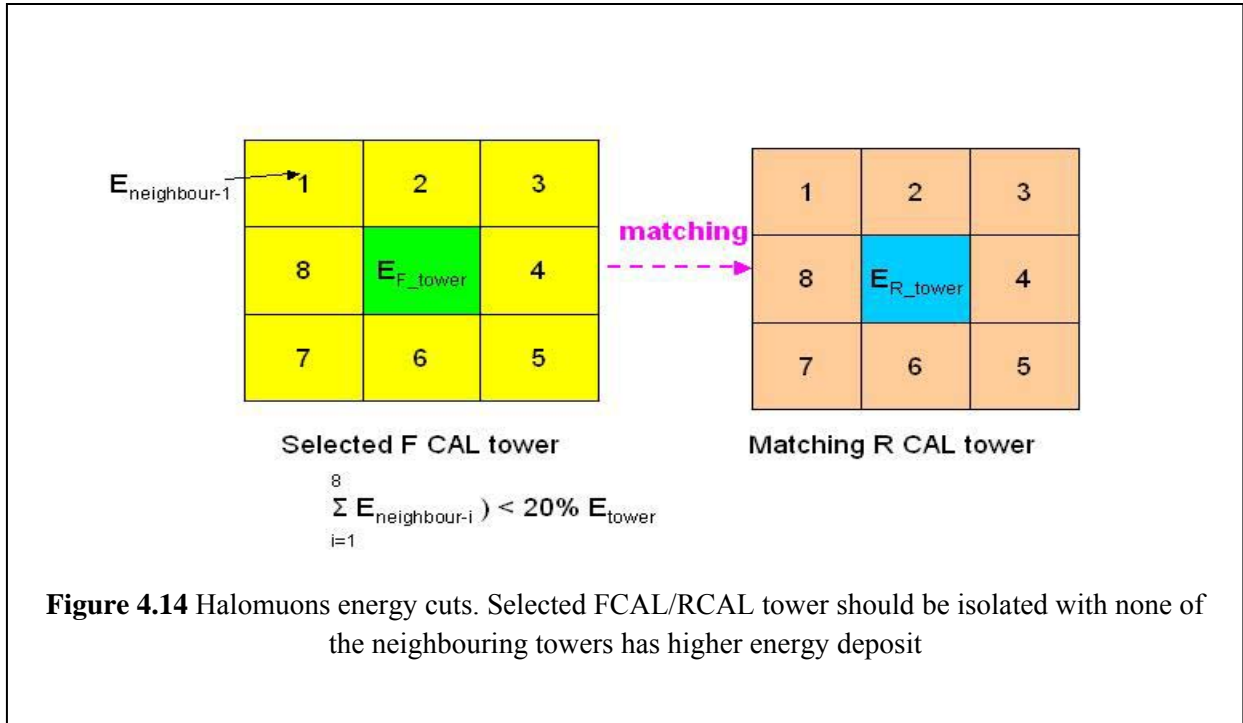
None of the neighboring eight towers should have an energy deposit higher than that of the selected tower. The energy sum of the eight neighboring towers should be less than 20% of the energy of the selected tower [63].

(v) The selected FCAL tower should have one matching tower in RCAL (and vice versa)

If there is an energy deposit in one FEMC and either or both HAC1 and HAC2 cells of the FCAL, then there should also be a (corresponding) energy deposits in REMC and HAC cells of the RCAL

For a given halomuon energy deposit in a FCAL cell, there should be a matching cell in RCAL. A matching of RCAL tower should be isolated i.e. it should have more than 80% of the sum of energy of its surrounding eight neighboring cells. The matched RCAL tower shall be one the nine selected towers with the same tower and module numbers of the selected FCAL tower and its neighboring towers. This cut would throw away halomuon events not parallel to the beam axis [61], [62].

Figure 4.14 shows the scheme for matching the halomuons in FCAL tower to RCAL tower.



4.2.4 Results

Figure 4.15 shows the time difference (ns) between FCAL and RCAL for the halomuon candidate's transversing the detector, fulfilling time requirements between 8 and 15 ns from interaction point. These data were from the CALCAL files collected as background to the physics event in the ZUES detector. In this analysis, the magnetic effect of the detector was neglected (but in case of calibration with a precision at a few percent levels [58] the effect might be significant).

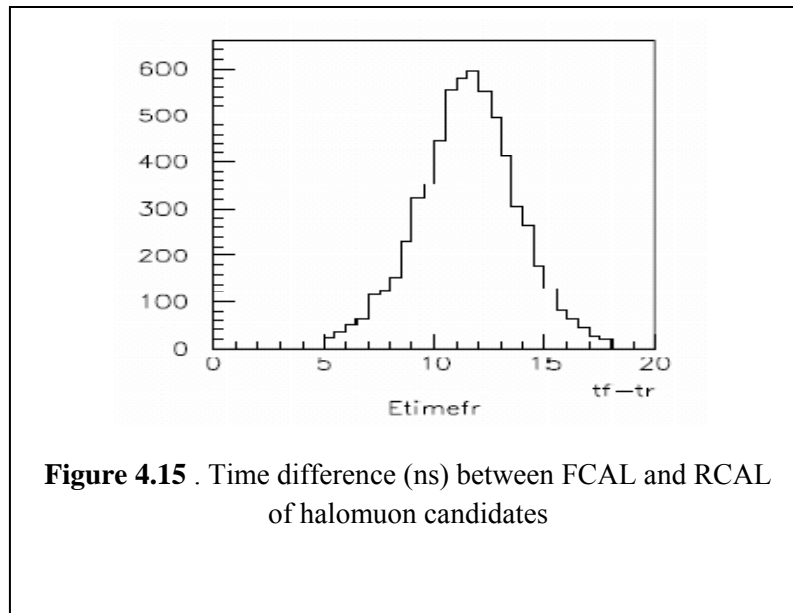


Figure 4.16 compares the halomuon hits before and after event selections and matching of towers for FCAL and RCAL towers with box plot of isoenergy. The size of the boxplots were significantly reduced before and after event selections and matching of towers in both the FCAL and RCAL towers. For both FCAL and RCAL, the isoenergy boxplots after event selections and matching of towers were more or less of the same size, indicating the success of the event selection and matching of towers for the halomuons.

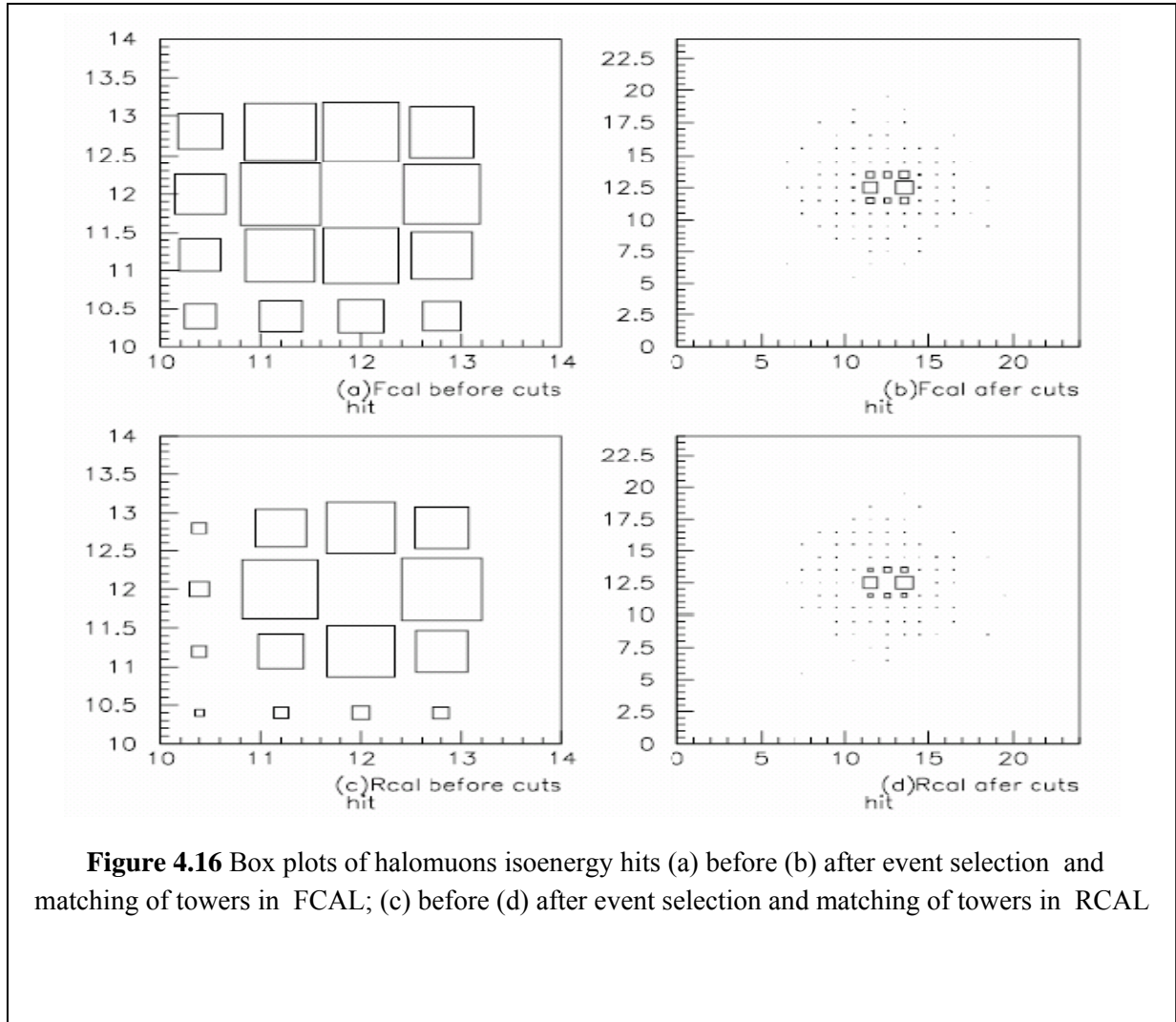
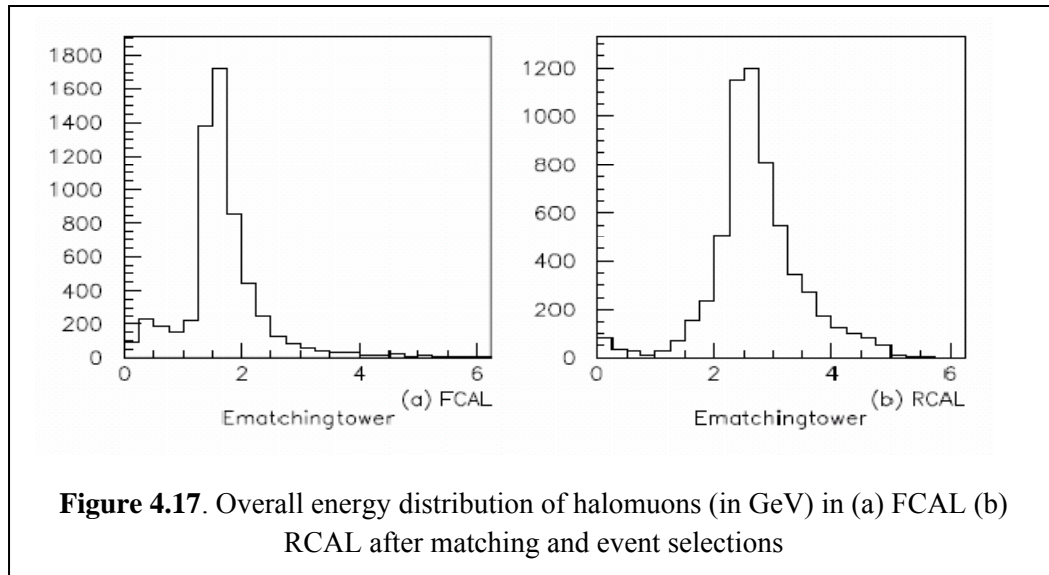
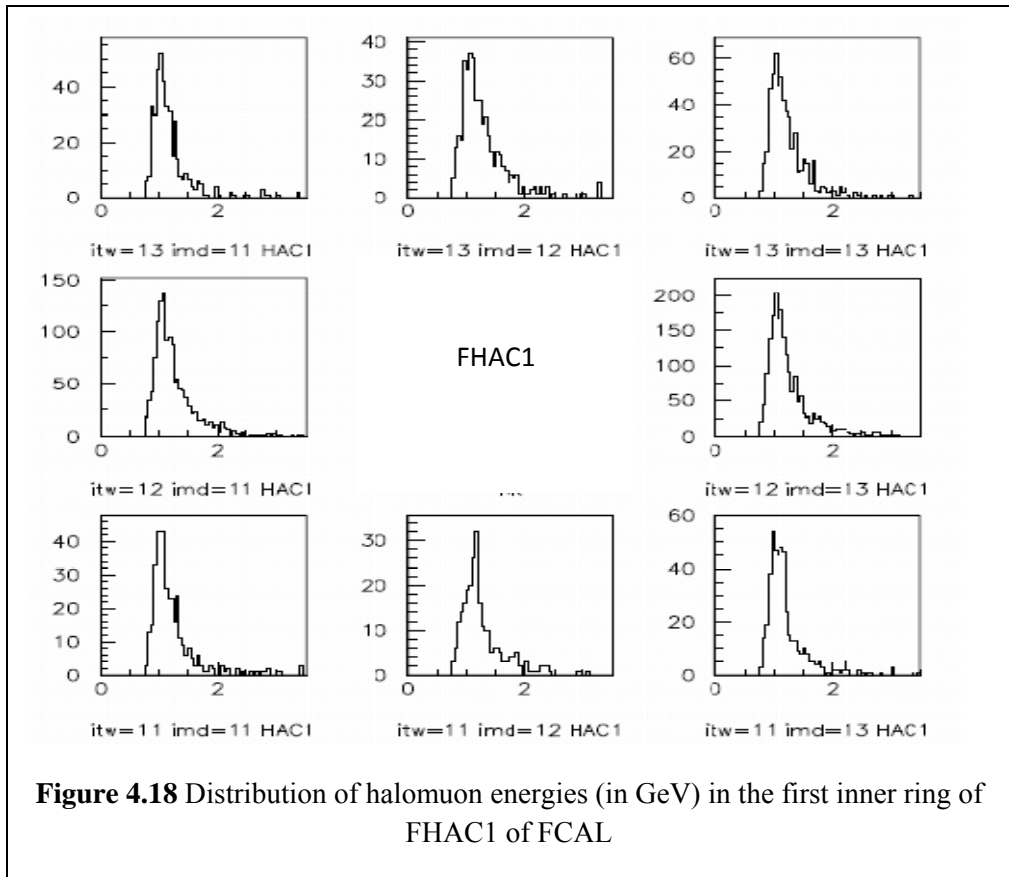
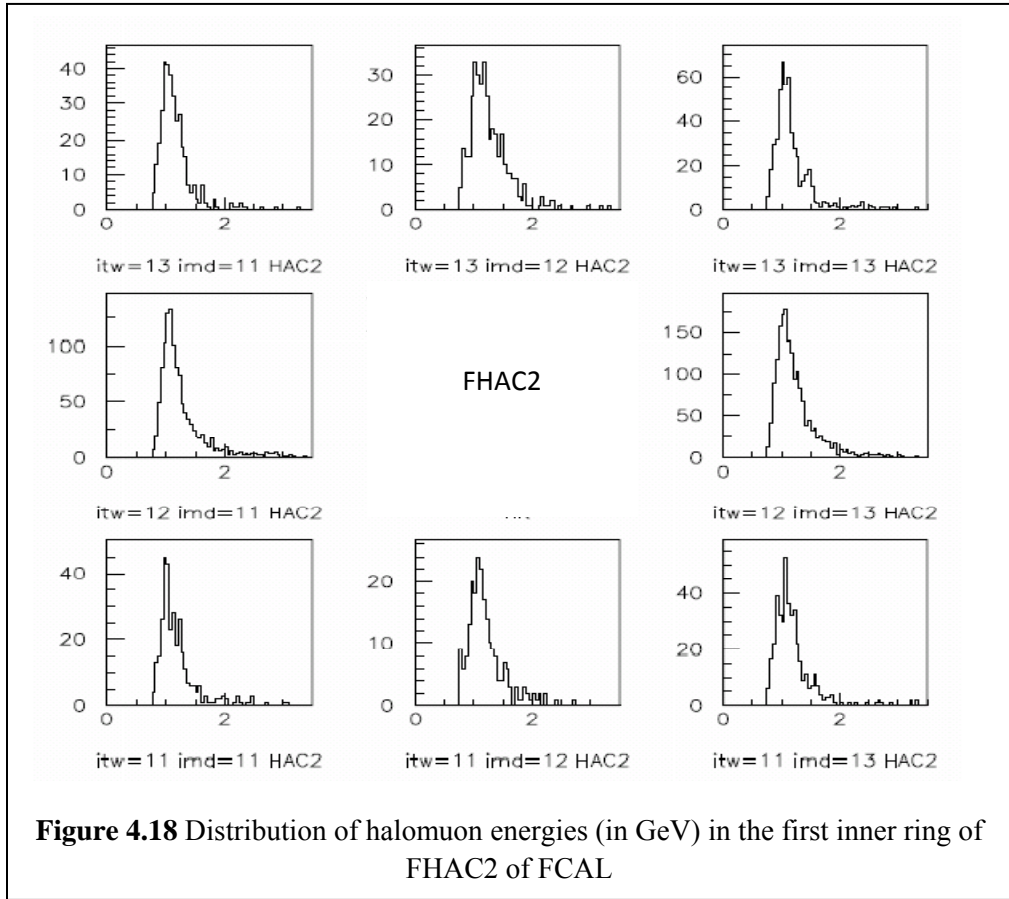


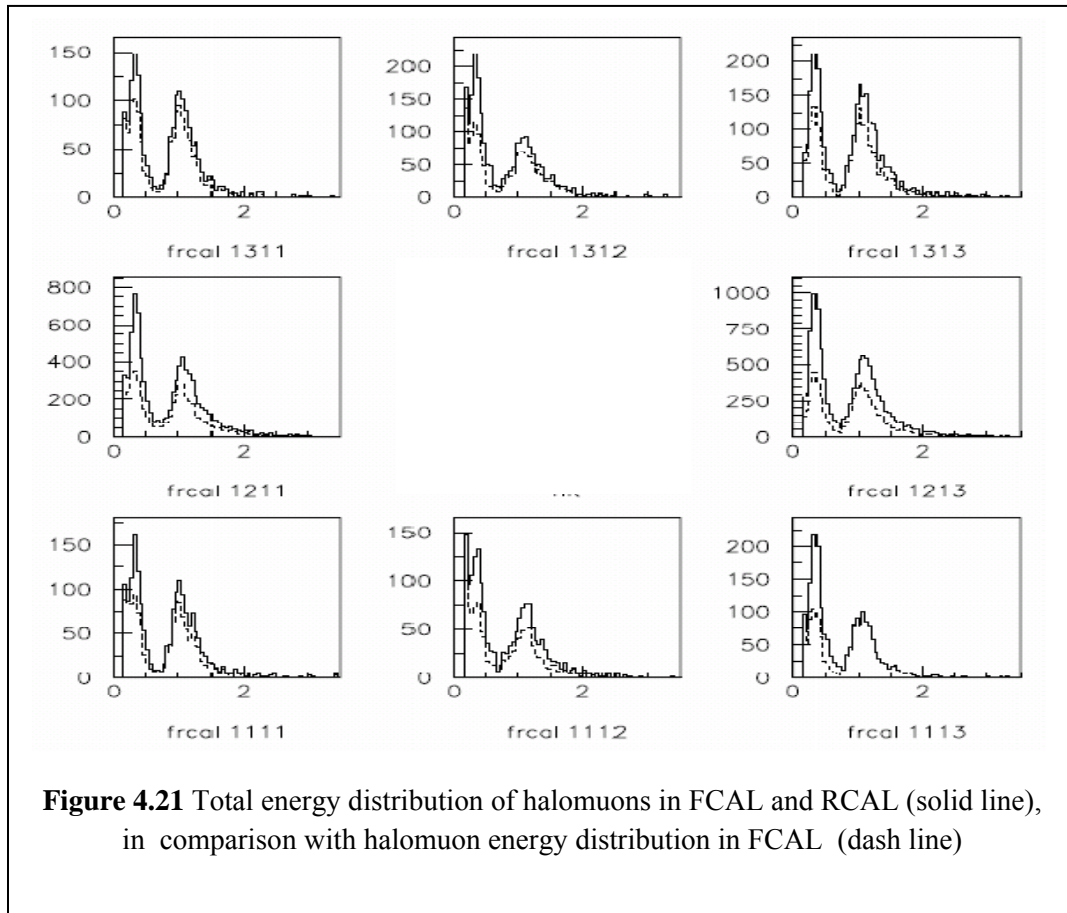
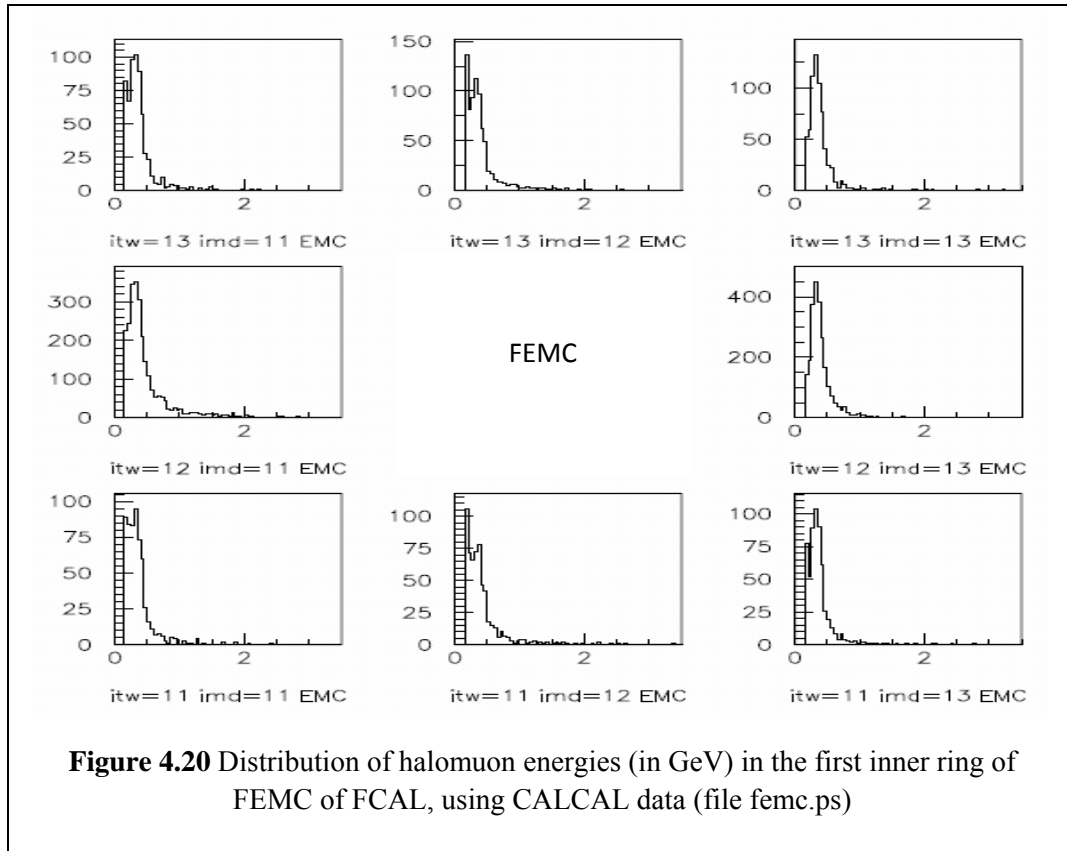
Figure 4.16 Box plots of halomuons isoenergy hits (a) before (b) after event selection and matching of towers in FCAL; (c) before (d) after event selection and matching of towers in RCAL

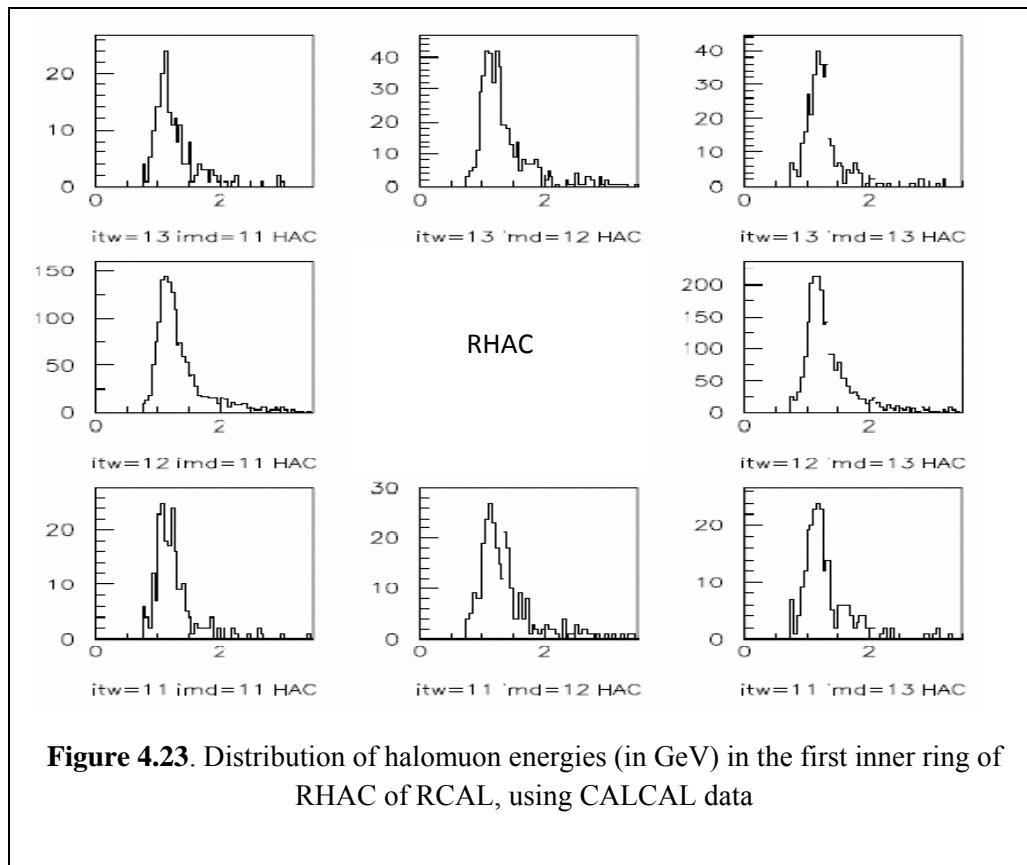
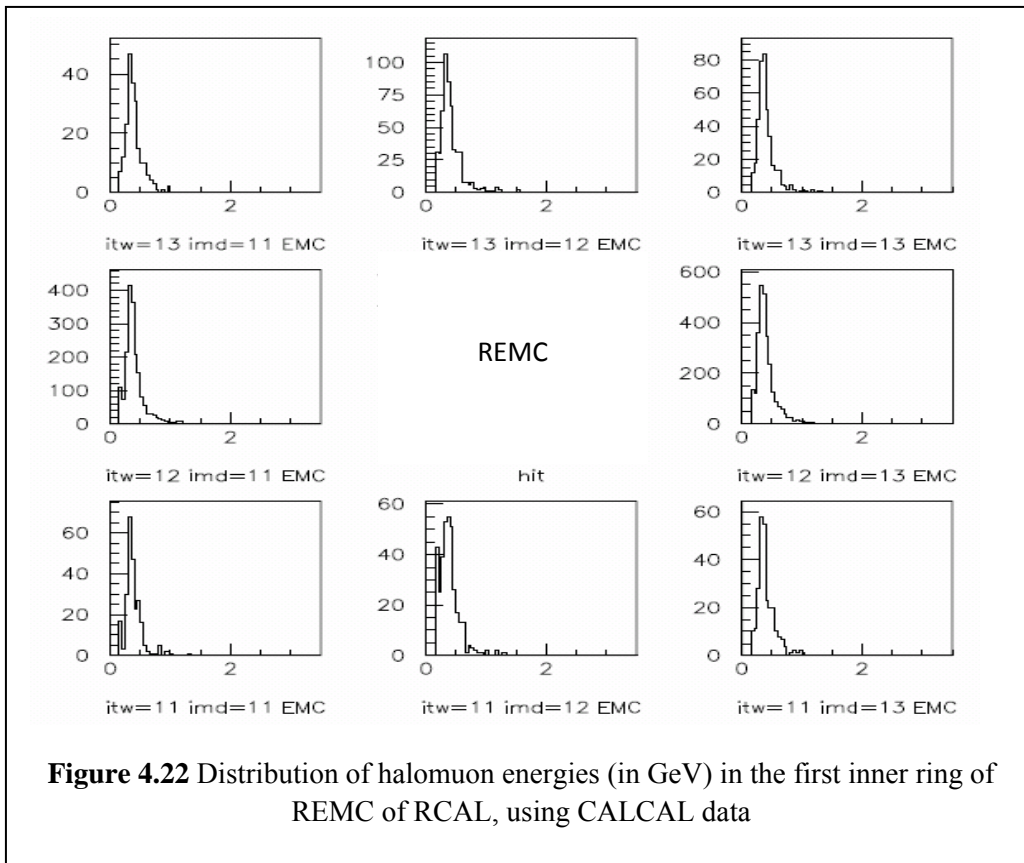
In **Figure 4.17**, the overall energy distribution (in GeV) in FCAL and RCAL towers after event selection and matching of towers is given. In the FCAL, there two overall energy peaks could be observed i.e. $\sim 0.5\text{GeV}$ and $\sim 1.8\text{GeV}$. Similarly in RCAL but at peaks $\sim 0.2\text{GeV}$ and $\sim 2.5\text{GeV}$. The difference in overall energy peaks between FCAL and RCAL might due to the energy loss as the halomuons transverse the ZEUS detector from RCAL to the FCAL, with small fraction of the energy being deposited in FEMC and REMC regions.

In **Figure 4.18**, **Figure 4.19** and **Figure 4.20**, the halomuons energy distributions for FHAC2, FHAC1 and FEMC are given for towers 11,12, 13 and modules 11,12, 13, with **Figure 4.21** giving the comparison between total halomuons energy (sum of energy both FCAL and RCAL) distributions and the energy distribution halomuons in FCAL (sum of FHAC2, FHAC1 and FEMC) . In **Figure 4.18** and **Figure 4.19**, the halomuons energy peaked at ~ 1 GeV in FHACs, while in **Figure 4.20** the halomuons energy peak at ~ 0.2 GeV in FEMC. But in RHAC the halomuons energy peaked at ~ 1.2 GeV showing that it loss ~ 0.2 GeV of energy as it transverse to the FHACs.









4.2.5 Summary

In **Section 4.2**, the algorithm for identifying halomuons in the ZEUS detector has been described. The halomuons which transverse the ZUES detector from the RCAL to the FCAL show reasonably good Landau distribution in the first inner ring (FIR) of the F/RCAL as part of physics event, with energy range of $\sim 1\text{GeV}$ in the hadronic calorimeter and $\sim 0.5\text{ GeV}$ in the EMC. As muons decay length is large (658.654 m), the halomuons retains most of its energy as its travels from rear to the front end of the ZEUS detector.