APPENDIX

Appendix 1: *MISR outputs from C program*

r252=10001001
r251=00101101
r250=00100101
r249=10110100
r248=10011010
r247=11010001
r246=01011010
r245=01000110
r244=01101000
r243=00011001
r242=10100011
r241=01100111
r240=10001100
r239=10011100
r238=00110011
r237=01110011
r236=11001110
r235=11001111
r234=00111001
r233=00111100
r232=11100111
r231=11110001
r230=10011110
r229=11000110
r228=01111000
r227=00011011
r226=11100011
r225=01101100
r224=10001101
r223=10110000
r222=00110110
r221=11000010
r220=11011000
r219=00001000
r218=01100001
r217=00100010
r216=10000100
r215=10001011
r214=00010001
r213=00101110
r212=01000101
r211=10111010
r210=00010111
r209=11101011
r208=01011101
r207=10101111
r206=01110101
r205=10111101
r204=11010111
r203=11110110
r202=01011110
r201=11011011
r200=01111011
r199=01101111
r198=11101101
r197=10111110
r196=10110111
r195=11111000
r194=11011111
r193=11100001
r192=01111100

r191=10000110
r190=11110000
r189=00011010
r188=11000011
r187=01101001
r186=00001101
r185=10100110
r184=00110100
r183=10011010
r182=11010011
r181=01101011
r180=01001101
r179=10101101
r178=00110101
r177=10110110
r176=11010110
r175=11011010
r174=01011011
r173=01101010
r172=01101101
r171=10101000
r170=10110101
r169=10100000
r168=11010100
r167=10000010
r166=01010000
r165=00001001
r164=01000001
r163=00100111
r162=00000100
r161=10011101
r160=00010011
r159=01110110
r158=01001110
r157=11011001
r156=00111011
r155=01100100
r154=11101100
r153=10010010
r152=10110010
r151=01001001
r150=11001001
r149=00100110
r148=00100100
r147=10011000
r146=10010011
r145=01100000
r144=01001100
r143=10000001
r142=00110000
r141=00000111
r140=11000000
r139=00011101
r138=00000011
r137=01110100
r136=00001110
r135=11010010
r134=00111010
r133=01001000
r132=11101001
r131=00100011

r130=10100100
r129=10001110
r128=10010001
r127=00111000
r126=01000111
r125=11100010
r124=00011000
r123=10001000
r122=01110001
r121=00100000
r120=11000100
r119=10000000
r118=00010000
r117=00000010
r116=01000000
r115=00001011
r114=00000001
r113=00101100
r112=00000101
r111=10110001
r110=00010110
r109=11000111
r108=01011000
r107=00011110
r106=01100011
r105=01111010
r104=10001111
r103=11101000
r102=00111101
r101=10100001
r100=11110100
r99=10000111
r98=11010000
r97=00011111
r96=01000011
r95=01111111
r94=00001111
r93=11111110
r92=00111111
r91=11111001
r90=11111111
r89=11100100
r88=11111100
r87=10010000
r86=11110010
r85=01000010
r84=11001000
r83=00001010
r82=00100001
r81=00101001
r80=10000101
r79=10100111
r78=00010100
r77=10011111
r76=01010011
r75=01111101
r74=01001111
r73=11110101
r72=00111110
r71=11010101
r70=11111010
r69=01010101
r68=11101010
r67=01010111
r66=10101010
r65=01011100
r64=10101011
r63=01110000
r62=10101110
r61=11000001
r60=10111000
r59=00000110
r58=11100000
r57=00011000
r56=10000011
r55=01100010
r54=00001100
r53=10001010
r52=00110001
r51=00101011
r50=11000101
r49=10101100
r48=00010101
r47=10110011
r46=01010110
r45=11001100
r44=01011001
r43=00110010
r42=01100110
r41=11001011
r40=10011001
r39=00101111
r38=01100101
r37=10111111
r36=10010111
r35=11111101
r34=01011111
r33=11110111
r32=01111110
r31=11011110
r30=11111011
r29=01111001
r28=11101111
r27=11100110
r26=10111100
r25=10011011
r24=11110011
r23=01101110
r22=11001101
r21=10111011
r20=00110111
r19=11101110
r18=11011101
r17=10111001
r16=01110111
r15=11100101
r14=11011100
r13=10010101
r12=01110010
r11=01010100
r10=11001010
r9=01010010
r8=00101010
r7=01001010
r6=10101001
r5=00101000
r4=10100101
r3=10100010
r2=10010100
r1=10001001
r0=01010001

Appendix 2: *Partial pad report of "Baud_r.pad"*

```
PAR: Xilinx Place And Route C.16.
Copyright (c) 1995-1999 Xilinx, Inc.  All rights reserved.
Wed Jan 30 12:32:03 2002

Xilinx PAD Specification File
*****************************

Input file:       map.ncd
Output file:      baud_r.ncd
Part type:        xc4005e
Speed grade:      -1
Package:          pc84

Wed Jan 30 12:32:03 2002

Pinout by Pin Name:
```

Pin Name	Direction	Pin Number
bclkx16	OUTPUT	P68
hclk	INPUT	P13
n<0>	INPUT	P69
n<10>	INPUT	P65
n<11>	INPUT	P49
n<12>	INPUT	P48
n<13>	INPUT	P47
n<14>	INPUT	P46
n<15>	INPUT	P45
n<1>	INPUT	P67
n<2>	INPUT	P66
n<3>	INPUT	P57
n<4>	INPUT	P50
n<5>	INPUT	P58
n<6>	INPUT	P59
n<7>	INPUT	P62
n<8>	INPUT	P61
n<9>	INPUT	P60
reseth	INPUT	P44

Appendix 3: *Partial pad report of "bilbotst.pad"*

```
PAR: Xilinx Place And Route C.16.
Copyright (c) 1995-1999 Xilinx, Inc.  All rights reserved.
Wed Jan 30 11:46:15 2002

Xilinx PAD Specification File
*****************************

Input file:       map.ncd
Output file:      bilbotst.ncd
Part type:        xc4005e
Speed grade:      -1
Package:          pc84

Wed Jan 30 11:46:15 2002

Pinout by Pin Name:
```

Pin Name	Direction	Pin Number
bilbo_mode<0>	INPUT	P45
bilbo_mode<1>	INPUT	P46
bilboen	INPUT	P49
ce	INPUT	P47
hclk	INPUT	P13
q<0>	OUTPUT	P57
q<1>	OUTPUT	P50
q<2>	OUTPUT	P58
q<3>	OUTPUT	P59
q<4>	OUTPUT	P62
q<5>	OUTPUT	P61
q<6>	OUTPUT	P60
q<7>	OUTPUT	P65
reseth	INPUT	P44
si	INPUT	P48
so	OUTPUT	P67
z<0>	INPUT	P6
z<1>	INPUT	P7
z<2>	INPUT	P8
z<3>	INPUT	P9
z<4>	INPUT	P66
z<5>	INPUT	P69
z<6>	INPUT	P70
z<7>	INPUT	P77

Appendix 4: *Hwtst.ucf*

```
net reseth      loc=p44;
net addr<0>  loc=p45;
net addr<1>  loc=p46;
net addr<2>  loc=p47;
net rw          loc=p48;
net cs          loc=p49;

net data<0>  loc=p6;
net data<1>  loc=p7;
net data<2>  loc=p8;
net data<3>  loc=p9;
net data<4>  loc=p66;
net data<5>  loc=p69;
net data<6>  loc=p70;
net data<7>  loc=p77;

net hclk        loc=p13;
```

Appendix 5: *Full pad report of "Hwtst.pad"*

```
PAR: Xilinx Place And Route C.16.
Copyright (c) 1995-1999 Xilinx, Inc.  All rights reserved.
Fri Jan 25 14:34:39 2002

Xilinx PAD Specification File
*****************************

Input file:        map.ncd
Output file:       hwtst.ncd
Part type:         xc4005e
Speed grade:       -1
Package:           pc84

Fri Jan 25 14:34:39 2002

Pinout by Pin Name:
+-------------------------------------------+-----------+--------------+
|                 Pin Name                  | Direction |  Pin Number  |
+-------------------------------------------+-----------+--------------+
| ack                                       |  OUTPUT   | P68          |
| addr<0>                                   |  INPUT    | P45          |
| addr<1>                                   |  INPUT    | P46          |
| addr<2>                                   |  INPUT    | P47          |
| addr<3>                                   |  INPUT    | P24          |
| bilbo_mode<0>                             |  INPUT    | P20          |
| bilbo_mode<1>                             |  INPUT    | P3           |
| bilboen                                   |  INPUT    | P4           |
| cs                                        |  INPUT    | P49          |
| cts                                       |  INPUT    | P81          |
| data<0>                                   |  BIDIR    | P6           |
| data<1>                                   |  BIDIR    | P7           |
```

data<2>	BIDIR	P8
data<3>	BIDIR	P9
data<4>	BIDIR	P66
data<5>	BIDIR	P69
data<6>	BIDIR	P70
data<7>	BIDIR	P77
dcd	INPUT	P82
dsr	INPUT	P71
dtr	OUTPUT	P72
hclk	INPUT	P13
irq	OUTPUT	P67
ldareg	INPUT	P5
ldbreg	INPUT	P83
out1	OUTPUT	P80
out2	OUTPUT	P25
reseth	INPUT	P44
ri	INPUT	P78
rts	OUTPUT	P84
rw	INPUT	P48
rxd	INPUT	P41
rxdatest<0>	OUTPUT	P57
rxdatest<1>	OUTPUT	P50
rxdatest<2>	OUTPUT	P58
rxdatest<3>	OUTPUT	P59
rxdatest<4>	OUTPUT	P62
rxdatest<5>	BIDIR	P61
rxdatest<6>	BIDIR	P60
rxdatest<7>	BIDIR	P65
si	INPUT	P14
so	OUTPUT	P79
txd	OUTPUT	P40

Dedicated or Special Pin Name	Pin Number
/PROG	P55
CCLK	P73
DONE	P53
GND	P52
GND	P1
GND	P76
GND	P31
GND	P43
GND	P64
GND	P12
GND	P21
M0	P32
M1	P30
M2	P34
TDO	P75
TDO	TDO
VCC	P22
VCC	P11
VCC	P42
VCC	P2
VCC	P63
VCC	P33
VCC	P54
VCC	P74

Pinout by Pin Number:

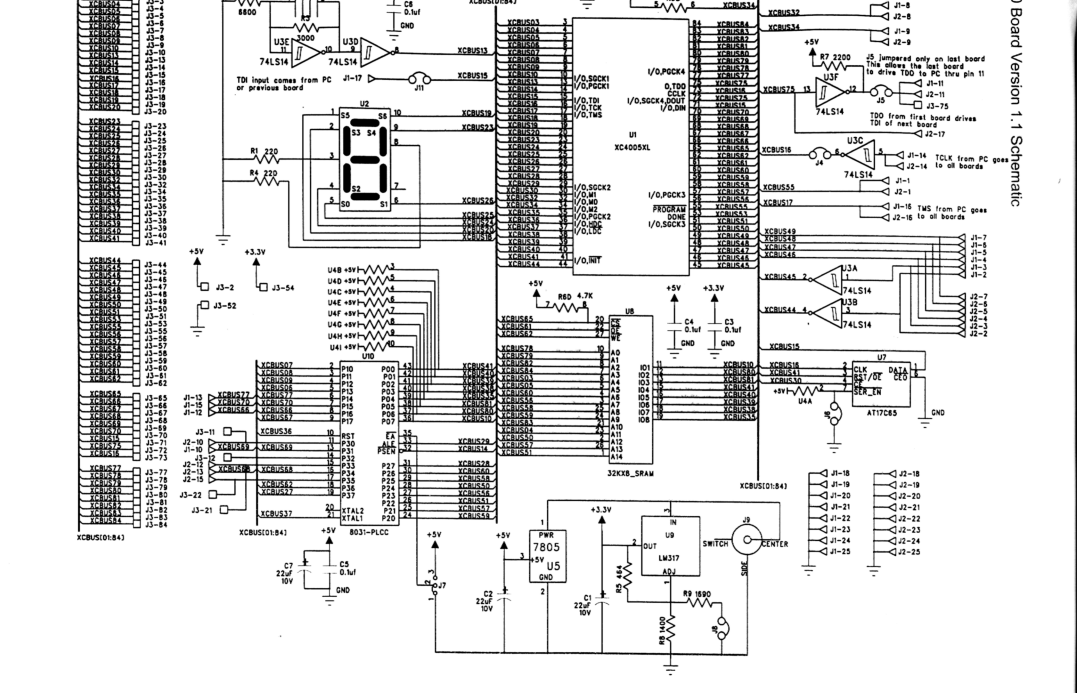
Pin Number	Pin Name	Direction	Constraint
P1	(GND)		
P2	(VCC)		
P3	bilbo_mode<1>	INPUT	
P4	bilboen	INPUT	
P5	ldareg	INPUT	

P6	data<0>	BIDIR	LOCATED
P7	data<1>	BIDIR	LOCATED
P8	data<2>	BIDIR	LOCATED
P9	data<3>	BIDIR	LOCATED
P10	---	UNUSED	
P11	(VCC)		
P12	(GND)		
P13	hclk		
P14	si	INPUT	LOCATED
P15	---	INPUT	
P16	---	UNUSED	
P17	---	UNUSED	
P18	---	UNUSED	
P19	---	UNUSED	
P20	bilbo_mode<0>	UNUSED	
P21	(GND)	INPUT	
P22	(VCC)		
P23	---		
P24	addr<3>	UNUSED	
P25	out2	INPUT	
P26	---	OUTPUT	
P27	---	UNUSED	
P28	---	UNUSED	
P29	---	UNUSED	
P30	(M1)	UNUSED	
P31	(GND)		
P32	(M0)		
P33	(VCC)		
P34	(M2)		
P35	---		
P36	---	UNUSED	
P37	---	UNUSED	
P38	---	UNUSED	
P39	---	UNUSED	
P40	txd	UNUSED	
P41	rxd	OUTPUT	
P42	(VCC)	INPUT	
P43	(GND)		
P44	reseth		
P45	addr<0>	INPUT	LOCATED
P46	addr<1>	INPUT	LOCATED
P47	addr<2>	INPUT	LOCATED
P48	rw	INPUT	LOCATED
P49	cs	INPUT	LOCATED
P50	rxdatest<1>	INPUT	LOCATED
P51	---	OUTPUT	
P52	(GND)	UNUSED	
P53	(DONE)		
P54	(VCC)		
P55	(/PROG)		
P56	---		
P57	rxdatest<0>	UNUSED	
P58	rxdatest<2>	OUTPUT	
P59	rxdatest<3>	OUTPUT	
P60	rxdatest<6>	OUTPUT	
P61	rxdatest<5>	BIDIR	
P62	rxdatest<4>	BIDIR	
P63	(VCC)	OUTPUT	
P64	(GND)		
P65	rxdatest<7>		
P66	data<4>	BIDIR	
P67	irq	BIDIR	LOCATED
P68	ack	OUTPUT	
P69	data<5>	OUTPUT	
P70	data<6>	BIDIR	LOCATED
P71	dsr	BIDIR	LOCATED
P72	dtr	INPUT	
P73	(CCLK)	OUTPUT	
P74	(VCC)		

```
| P75          | (TDO)                          |            |           |
| P76          | (GND)                          |            |           |
| P77          | data<7>                        | BIDIR      | LOCATED   |
| P78          | ri                             | INPUT      |           |
| P79          | so                             | OUTPUT     |           |
| P80          | out1                           | OUTPUT     |           |
| P81          | cts                            | INPUT      |           |
| P82          | dcd                            | INPUT      |           |
| P83          | ldbreg                         | INPUT      |           |
| P84          | rts                            | OUTPUT     |           |
| TDO          | (TDO)                          |            |           |
+--------------+--------------------------------+------------+-----------+

#
# To preserve the pinout above for future design iterations,
# simply run "Lock Pins..." from the Design Manager's Design
# menu, or invoke PIN2UCF from the command line. The location constraints
# above will be written into your specified UCF file. (The constraints
# listed below are in PCF format and cannot be directly used in the UCF file).
#
COMP "ack" LOCATE = SITE "P68" ;
COMP "addr<0>" LOCATE = SITE "P45" ;
COMP "addr<1>" LOCATE = SITE "P46" ;
COMP "addr<2>" LOCATE = SITE "P47" ;
COMP "addr<3>" LOCATE = SITE "P24" ;
COMP "bilbo_mode<0>" LOCATE = SITE "P20" ;
COMP "bilbo_mode<1>" LOCATE = SITE "P3" ;
COMP "bilboen" LOCATE = SITE "P4" ;
COMP "cs" LOCATE = SITE "P49" ;
COMP "cts" LOCATE = SITE "P81" ;
COMP "data<0>" LOCATE = SITE "P6" ;
COMP "data<1>" LOCATE = SITE "P7" ;
COMP "data<2>" LOCATE = SITE "P8" ;
COMP "data<3>" LOCATE = SITE "P9" ;
COMP "data<4>" LOCATE = SITE "P66" ;
COMP "data<5>" LOCATE = SITE "P69" ;
COMP "data<6>" LOCATE = SITE "P70" ;
COMP "data<7>" LOCATE = SITE "P77" ;
COMP "dcd" LOCATE = SITE "P82" ;
COMP "dsr" LOCATE = SITE "P71" ;
COMP "dtr" LOCATE = SITE "P72" ;
COMP "hclk" LOCATE = SITE "P13" ;
COMP "irq" LOCATE = SITE "P67" ;
COMP "ldareg" LOCATE = SITE "P5" ;
COMP "ldbreg" LOCATE = SITE "P83" ;
COMP "out1" LOCATE = SITE "P80" ;
COMP "out2" LOCATE = SITE "P25" ;
COMP "reseth" LOCATE = SITE "P44" ;
COMP "ri" LOCATE = SITE "P78" ;
COMP "rts" LOCATE = SITE "P84" ;
COMP "rw" LOCATE = SITE "P48" ;
COMP "rxd" LOCATE = SITE "P41" ;
COMP "rxdatest<0>" LOCATE = SITE "P57" ;
COMP "rxdatest<1>" LOCATE = SITE "P50" ;
COMP "rxdatest<2>" LOCATE = SITE "P58" ;
COMP "rxdatest<3>" LOCATE = SITE "P59" ;
COMP "rxdatest<4>" LOCATE = SITE "P62" ;
COMP "rxdatest<5>" LOCATE = SITE "P61" ;
COMP "rxdatest<6>" LOCATE = SITE "P60" ;
COMP "rxdatest<7>" LOCATE = SITE "P65" ;
COMP "si" LOCATE = SITE "P14" ;
COMP "so" LOCATE = SITE "P79" ;
COMP "txd" LOCATE = SITE "P40" ;
#

---------------------------------------------------------------------------------------------
```


Board Version 1.1 Schematic
XC4005XL
32KX8_SRAM
AT17C65
74LS14
74LS14
74LS14
74LS14
74LS14
74LS14
8031-PLCC
LM317
7805
TDI input comes from PC or previous board
TDO from first board drives TDI of next board
TCLK from PC goes to all boards
TMS from PC goes to all boards
J5 jumpered only on last board This allows the last board to drive TDO to PC thru pin 11
SWITCH
CENTER
SIDE