REFERENCES

[Cheng, 2001]	"DFT and Core-Based SOC Testing" Cheng-Wen Wu, Lab for Reliable Computing, Dept. Electrical Engineering, National Tsing Hua University, 2001.
[Edward, 1985]	"Bult-in Self Test Techniques", J. M. Edward, IEEE Design and Test, p.p. 21-28, April 1985.
[Fields, 2000]	"Improving Productivity with FPGA Design Reuse", Carol Fields, Design Methodologist, Xilinx Inc., Dec 2000.
[Frederick, 1993]	"A High-Level Synthesis Based VLSI Design Methodology" Lawrence Frederick Arnstein Electrical and Computer Engineering, Carnegie Mellon University Pittsburgh, Pennsylvania, December 1993
[Harvey, 1999]	"Generic UART Manual" M. S. Harvey, SiliconValley, December 1999.
[Hyungwon, 2001]	"Simulation-Based Generation of LFSR Seeds for Deterministic BIST" Hyungwon Kim and John P. Hayes, Advanced Computer Architecture Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan, May 1997
[Ibrahim, 1995]	"A Built in Self Testable Bit-Slice Processor" Ibrahim Abubakr M., Faculty of Computer Science & Information Technology, University of Malaya, May 1995.
[I-Cube 1997]	"JTAG UART for Controlling PSID" I-Cube Application Note, September 1997
[Koetr, 1996]	"What's an LFSR" John Koeter, Texas Instrument, December 1996.
[Kwanghyun, 1988]	"Automatic Insertion of BIST Hardware Using VHDL" Kwanghyun Kim Joseph G. front Dong S. Ha, Department of Electrical Engineering, Virginia Polytechnic Institute and State University Blacksburg, VA 24061, 1988
[Martin, 1989]	"A Comparison of the INS8250, NS16450 and NS16550AF Series of UARTs" Martin S. Michael, National Semiconductor Application Note 493, April 1989

[McCluskey, 1984]	"Verification Testing – A Pseudoexhaustive Test Technique", E.J. McCluskey, IEEE Trans. Computer, p.p. 541-546 June 1984.
[Monroe, 2001]	"Computing with Atoms and Molecules. Prospects of Harnessing Quantum Mechanics for Faster Computers", Christopher Monroe and David Wineland National Institute of Standards and Technology, Boulder, CO 80303, 2001.
[National, 1995]	"PC16550D Universal Asynchronous Receiver/Transmitter with FIFOs", National Semiconductor Application Note, June 1995.
[Navabi, 1991]	"VHDL Analysis and Modeling of Digital Systems", Zainalabedin Navabi, McGraw-Hill Inc. 1991.
[Oelsner, 2000]	"Digital UART Design in HDL" Thomas Oelsner, QuickLogic Europe, 2000.
[Peterson, 1972]	"Error Correcting Codes", W.W. Peterson and E.J. Weldon, Jr, MIT press, Cambridge, MA 1972.
[Roth, 1998]	"Digital System Design Using VHDL" Charles H Roth, Jr., PWS Publishing Company, 1998
[Schip, 2001]	"International Technology Roadmar For Semiconductors Accelerates Pace To Smaller Chip Dimensions", Semichips, Press Release, Nov 2001.
[Turino, 2000]	"RTL DFT Rule Checking - The Circuit Designer's Secret Weapon" Jon Turino, Integrated System Design Magazine, 2000
[Upadhyaya, 2001]	"VLSI Testing" Shambu J Upadhyaya, Department of Computer Science & Engineering, State University of New York, January 22, 2001.
[Williams. 2000]	"Design For Testability- A Survey" T. W. Wiliams and K. P. Parker, Proc. IEEE V. 71, No. 1, 2000.
[Wilson, 2001]	"FPGA-vsASIC panel reaches few conclusions", Ron Wilson, EE Times, 2001.
[XEng, 1997]	"XS40, XSP, and XS95 Board Manual" XESS Corporation, Copyright ©1997, 1998 by X Engineering Software Systems

Corporation.

[Xess, 1999]	"Xstend V1.3 Board Manual – How to install and use your new Xstend Board" XESS Corporation, May 7, 1999
[Xess, 2000]	"XSTOOLs Source Documentation 3.0 - Architecture of the XSTOOLs software" XESS Corporation. October 9, 2000
[Xilinx, 1999]	"XC4000E and XC4000X Series Field Programmable Gate Arrays" Xilinx's Product Specification. January 29, 1999 (Version 1.5)