LIST OF TABLES

Table 1.1: Future prediction towards semiconductors technologies
Table 2.1: Summary of test cost
Table 3.1: Feedback Combination to Generate LFSR
Table 4.1: UART Pins Description
Table 4.2: UART Registers Description
Table 4.3: LCR1 Description
Table 4.4: LCR2 Description
Table 4.5: Modem Control Register Description
Table 4.6: Line Status Register Description
Table 4.7: Modem Status Register Description
Table 4.8: Interrupt Mask Register Description
Table 4.9: VHDL Modules
Table 5.1: Script Files of a UART with BIST
Table 5.2: ADDR[3:0] and DATA[7:0] corresponds to the simulation result
Table 5.3: S_QOUT and S_DATA_IN in binary number
Table 6.1: Summary of Xilinx XC4005E FPGA Chip
Table 6.2: BILBO Operating Mode
Table 6.3: Test Procedure
Table 6.4: Summary of the selected ADDR[3:0] and DATA[7:0]
Table 7.1: Cost to Detect and Diagnose a Fault at Different Levels
LIST OF TABLES

Table 1.1 : Future prediction towards semiconductors technologies

Table 2.1 : Summary of test cost

Table 3.1 : Feedback Combination to Generate LFSR

Table 4.1 : UART Pins Description

Table 4.2 : UART Registers Description

Table 4.3 : LCR1 Description

Table 4.4 : LCR2 Description

Table 4.5 : Modem Control Register Description

Table 4.6 : Line Status Register Description

Table 4.7 : Modem Status Register Description

Table 4.8 : Interrupt Mask Register Description

Table 4.9 : VHDL Modules

Table 5.1 : Script Files of a UART with BIST

Table 5.2 : ADDR[3:0] and DATA[7:0] corresponds to the simulation result

Table 5.3 : S_QOUT and S_DATA_IN in binary number

Table 6.1 : Summary of Xilinx XC4005E FPGA Chip

Table 6.2 : BILBO Operating Mode

Table 6.3 : Test Procedure

Table 6.4 : Summary of the selected ADDR[3:0] and DATA[7:0]

Table 7.1 : Cost to Detect and Diagnose a Fault at Different Levels
LIST OF FIGURES

Figure 1.1 : Total transistor per chip 1

Figure 3.1 : Serial Data Transmission and Receive 18

Figure 3.2 : UART block diagram 18

Figure 3.3 : Transmitter sequence of UART 20

Figure 3.4 : Receiver sequence 22

Figure 3.5 : Generic BIST 24

Figure 3.6: n-bits Linear Feedback Shift Register 25

Figure 3.7: n stage LFSR Configured as a MISR 27

Figure 3.8: BILBO Operating Modes 29

Figure 3.9: UART with BILBO Register and Tester 29

Figure 3.10: Sampling data received with 16 clocks faster than transmitter bit clock 31

Figure 4.1 : Xilinx Foundation Series 2i design flow 36

Figure 4.2 : Design Implementation flow of Xilinx Foundation Series 2i 38

Figure 4.3 : UART with BIST Top Level Design Symbol 41

Figure 4.4 : Hierarchical Tree of UART with BIST 50

Figure 5.1 : UART Frame Format 56

Figure 5.2 : 8-bits Data Transmission Setup 58
Figure 5.3: Serial 8-bits Data Transmission at TXD

Figure 5.4: 5-bits Data Transmission Setup

Figure 5.5: Serial 5-bits Data Transmission at TXD

Figure 5.6: Transmitter Break Interrupt Setup

Figure 5.7: Transmitter Break Interrupt at TXD

Figure 5.8: Transmitter Even Parity Setup

Figure 5.9: Transmitter Even Parity Data Transmission at TXD

Figure 5.10: Transmitter CTS Enable Setup

Figure 5.11: TXD when CTS = '1' and tcstsen is enable

Figure 5.12: TXD when CTS = '0' and tcstsen is enable

Figure 5.13: Interrupt Mask Register setup

Figure 5.14: Interrupt Request (IRQ) when TXRDY Interrupt Mask is enable

Figure 5.15: Receiver 8-bits Setup

Figure 5.16: 8-bits Data Received at DATA[7:0] when Data Output Enabled.

Internal Data Received at S_RXDATA.

Figure 5.17: Receiver 5-bits Setup

Figure 5.18: 5-bits Data Received at DATA[7:0] when Data Output Enabled.

Internal Data Received at S_RXDATA.

Figure 5.19: Receiver Error and LSR setup

Figure 5.20: Results of Receiver Error and LSR

Figure 5.21: Results of Receiver Error and LSR (continued)

Figure 5.22: BIST Setup

Figure 5.23: BILBO Act as Shift Register

Figure 5.24: BILBO Act as LFSR and MISR
Figure 5.25: Final Value of MISR (S_QOUT) to be shifted out as serial signature

Figure 5.26: Serial Data Out Signature at "so"

Figure 6.1: XS40 Board V1.1

Figure 6.2: GXLOAD

Figure 6.3: GXSPORT

Figure 6.4: GXSTEST

Figure 6.5: GXSSETCLK

Figure 6.6: Test Setup

Figure 6.7: Hewlett Packard 54645D Mixed Signal Oscilloscope

Figure 6.8: XS40 test setup

Figure 6.9: External circuit to drive inputs to FPGA pins

Figure 6.10: Custom Implementation

Figure 6.11: Baud Rate Test Result

Figure 6.12: Measurement of BclkX16 using Mixed Signal Oscilloscope

Figure 6.13: Simulated waveform of BclkX16

Figure 6.14: Pseudo Random Pattern

Figure 6.15: Multiple Input Signature Register (MISR)

Figure 6.16: UART Internal Loop Test Result

Figure 7.1: Design Summary
CONTENTS

ACKNOWLEDGEMENTS i
LIST OF TABLES ii
LIST OF FIGURES iii
CONTENTS vi

CHAPTER 1: VLSI SUB-MICRON TECHNOLOGY

1.0 Introduction 1
1.1 Sub-micron Technology & FPGA 2
1.2 FPGA and Logic Testing 3
1.3 The Objectives 4
1.4 Scope 6

CHAPTER 2: SUB-MICRON TECHNOLOGY & LOGIC TESTING

2.0 Introduction 8
2.1 Tests and Manufacturer 9
2.2 VLSI Testing Problems 11
   2.2.1 Test Generation Problem 11
   2.2.2 The Input Combinatorial Problem 12
   2.2.3 The Gate to I/O Pin Ratio Problem 13
2.3 Built-in-Self-Test (BIST) 13
CHAPTER 3: UART with BIST

3.0 Introduction 16

3.1 Universal Asynchronous Receive/Transmit (UART) 17

3.2 UART Architecture 18

3.2.1 The Transmitter 19

3.2.2 The Receiver 21

3.2.3 Baud Rate Generator 22

3.3 BIST Consideration 24

3.3.1 Linear Feedback Shift Register (LFSR) 25

3.3.2 Multiple Input Signature Register (MISR) 27

3.4 UART with BILBO Register and Tester 28

3.5 UART Features 31

CHAPTER 4: VHDL IMPLEMENTATION

4.0 Introduction 35

4.1 Designing a Programmable logic 36

4.2 VHISC Hardware Description Language (VHDL) 38

4.2.1 VHDL as a Standard Language 39

4.2.2 Increase productivity 39

4.2.3 Better design 39

4.2.4 Reusability for new technology 39

4.2.5 Tools independence 40

4.2.6 Minimum cost and time 40
CHAPTER 5: SYNTHESIS & SIMULATION

5.0 Introduction 53
5.1 Simulation 53
5.2 UART Frame Format 55
5.3 Transmitter Simulation 57
   5.3.1 Transmitter 8-Bits Data Transmission 57
   5.3.2 Transmitter 5-Bits Data Transmission 61
   5.3.3 Transmitter Break Interrupt 62
   5.3.4 Transmitter Even Parity Mode 63
   5.3.5 Transmitter CTS Enable (txctsen) 64
   5.3.6 Interrupt Mask Register (INTMSK) 66
5.4 Receiver Simulation

5.4.1 Receiver 8-bit Mode 67
5.4.2 Receiver 5-bits Mode 69
5.4.3 Receiver Error and I.SR 70

5.5 BIST Simulation 73
5.5.1 BIST Mode 73

CHAPTER 6: HARDWARE TEST

6.0 Introduction 80
6.1 XS40 Prototyping Board Version 1.1 (XS40 V1.1) 81
6.2 Xilinx XC4005E FPGA Chip 82
6.3 XSTOOLs 83
6.4 Initial Test Setup 86
6.5 Baud Rate Generator Test 88
   6.5.1 User Constraint Files (*.ucf) 89
   6.5.2 Baud Rate Calculation 90
   6.5.3 External Circuit 91
   6.5.4 Download Bit Stream File 92
   6.5.5 Baud Rate Test Result 94
6.6 BILBO Test 96
   6.6.1 Pseudo Random Pattern Generation (PRPG) 96
   6.6.2 Multiple Input Signature Register (MISR) 98
6.7 UART Internal Loop Back Mode

CHAPTER 7: DISCUSSION AND CONCLUSION

7.0 Discussion

7.1 Conclusion

REFERENCES

APPENDIX

Appendix 1: MISR outputs from C program

Appendix 2: Partial pad report of “Baud_r.pad”

Appendix 3: Partial pad report of “bilbotst.pad”

Appendix 4: Hwtst.ucf

Appendix 5: Full pad report of “Hwtst.pad”

Appendix 6: XS40 Board Version 1.1 Schematic