CHAPTER 1

VLSI SUB-MICRON TECHNOLOGY

1.0 Introduction

Technological innovation is a critical factor for survival and growth. Thanks to physic-based simulation, advances in silicon technology are increasing. In the age of sub-micron technology, a single chip may contain tens or even hundreds of millions of transistors. According to Semiconductor Industry Association (SIA) projections [SChip, 2001], the number of transistors per chip and the local clock frequencies for high-performance microprocessors will continue to grow exponentially in the near future. The prediction is similar to Moore's law, which indicates that the number of transistors in an IC doubles every 18 months [Monroe, 2001]. **Figure 1.1** and **Table 1.1** show the future prediction researched by SIA towards semiconductor technologies. The improvement and evolution ensures that future microprocessors will become ever more complex.

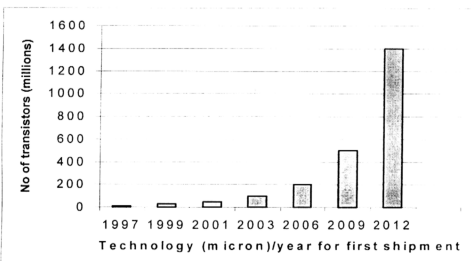

Figure 1.1: Total transistor per chip

Table 1.1: Future prediction towards semiconductor technologies

Specification/year	1997	1999	2001	2003	2006	2009	2012
Feature size (micron)	0.25	0.18	0.15	0.13	0.1	0.07	0.05
Supply voltage (V)	1.8-2.5	1.5-1.8	1.2-1.5	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6
Transistors/chip	11M	21M	40M	76M	200M	520M	1.4B
DRAM bits/chip	167M	1.07G	1.7G	4.29G	17.2G	68.7G	275G
Die size (mm 2)	300	340	385	430	520	620	750
Local clock freq. (MHz)	750	1,250	1,500	2,100	3,500	6,000	10,000
Global clock freq. (MHz)	750	1,200	1,400	1,600	2,000	2,500	3,000
Maximum power/chip (W)	70	90	110	130	160	170	175

1.1 Submicron Technology & FPGA

The increasing growth of sub-micron technology creates an opportunity for design and test engineers to play an important role to ensure better quality of their products. At this stage, programmable logic devices (PLD) are the most suitable devices for new technologies because of their capability to change and manipulate or store their logic characteristics through programming. One of the major programmable logic architecture available is called Field Programmable Gate Array (FPGA). FPGA contains hundreds (or thousands) of Configurable Logic Blocks (CLBs) to form complex logic implementation. It is one of the fastest growing components invented and has revolutionized the way many systems are designed. It also improves productivity with its design reusability [Fields, 2000][Wilson, 2001].

FPGAs are supported by a number of CAD/EDA tools (SYNOPSYS, AMBIT BuildGates, etc.) to generate a structural hardware implementation. This sophisticated software places and routes the logic on the device reducing the FPGA cost. The reduction is possible since the FPGAs do not provide 100% interconnection between their logic blocks (100% interconnection is prohibitively expensive). Although the cost of the FPGA itself is reduced, the main contribution to overall production cost (the test) still needs to be improved. The test of the FPGA should be investigated to ensure the quality and reliability of a product produced by the manufacturer.

1.2 FPGA and Logic Testing

An increasing number of transistors per chip from hundreds of thousands and lately in millions have resulted in an increase in the difficulty of testing. The difficulty of testing also affects the FPGA since there is no practical way of probing individual memory circuits on a chip with hundreds of thousands of gates compared to chips of early design. Therefore, the designer has to create design practices that will allow easier testing procedures. Design for testability techniques simplify the test development tasks by constraining the design such that will be easy to test structures, thereby making it easier to generate and apply tests that detect all the targeted failures. The introduction of internal test circuitry in the design to form self-testing steps can prove to be a useful approach.

One of the most widely accepted internal test circuitry is Built-In-Self-Test (BIST). This technique has long been recognized as a means to reduce system life cycle test and maintenance costs. However, the drawbacks when implementing BIST are the main problems of the limited use of this technique. The drawbacks as can be observed in a previous research [Upadhyaya, 2001] are the possibilities of performance or areas overhead and the needs of initial design investment. These drawbacks sometimes force the manufacturer to rethink before trying to implement BIST in their products.

1.3 The Objectives

The number of faulty chips that escapes detection during testing are serious issues in chip design and manufacturing. To increase reliability, manufacturers must be able to discover a high percentage of the defective chips during their testing procedures. This thesis will try to highlight the attention given by most customers who are expecting the designer to include testability features that will increase product reliability.

The focus of this thesis will be on designing a UART chip with embedded Built-In-Self-Test (BIST) architecture using FPGA technology. Universal Asynchronous Receive/Transmit (UART) is an integrated circuit, which plays the most important role in serial communication. It handles the conversion between serial and parallel data. Serial communication reduces the distortion of a signal, therefore makes data transfer between two systems separated in greater length possible (i.e. hundreds of feet and millions of miles apart). The embedded BIST architecture provides opportunities for the sharing of system and test logic. BIST is a method of self-testing on a system on chip

due to the complexity to determine stuck at logic error using conventional methods such as bed of nails. The technique proposed for BIST architecture in this thesis is Built-In-Logic-Block-Observer (BILBO). The BILBO technique has been recognized as a method that can help to reduce the test and maintenance cost of chip production. By implementing a BILBO architecture to a design, an external tester feature, such as Test Pattern Generator (TPG) and Output Response Analyzer (ORA) will be embedded into the part that contains the Circuit Under Test (CUT). This can be done since BILBO can act as a shift register, Linear Feedback Shift Register (LFSR) and Multiple Input Signature Register (MISR) depending on its operating mode. BILBO testability technique can provide shorter test time compared to an externally applied test and allows the use of low-cost test equipment during all stages of production. This technique will be described in more detail in chapters two and three.

Although BIST techniques are becoming more common in industry, the additional BIST circuit that increases the hardware overhead is often cited as a reason for the limited use of BIST. In this research, the test performance achieved with the implementation of BIST will prove to be adequate to cover the weakness of the hardware overhead produced by the additional BIST circuit. The BIST technique has the main objective of satisfying specified testability requirements and to generate the lowest-cost with the highest performance implementation.

The design will start by describing the behavior of UART circuit using VHISC Hardware Description Language (VHDL). In the implementation phase, the BIST technique has to be incorporated into the UART design before the overall design is

synthesized by means of reconfiguring the existing design to match testability requirements. Then both designs (UART and BIST) which are written in VHDL will be synthesized to obtain a Register Transfer Level (RTL) description. The next step is to verify the RTL and implement it on Xilinx's FPGA chip using "Xilinx Foundation Series Student Edition 2i" software. The design then will be downloaded to Xilinx FPGA chip using XS40 board and XSTOOLs provided by Xess Corporation to ensure its reliability in the real world application.

1.4 Scope

This thesis is intended for those who are interested in implementing a Built-In-Self-Test (BIST) technique in their design. Apart from this, the thesis will also present a special UART controller chip architecture to assure a proper function of serial ports, which has been an important input/output tool for decades. The organization of this thesis starts with the basic principles of logic testing followed by the implementation of BIST to the UART architecture. Next, the result achieved from the simulation and hardware test will be presented and discussed. The summary of each chapter is presented as follows:

Chapter 2: In this chapter, a discussion on VLSI Sub-micron technology and logic testing are conducted. Beginning with the issue of testability in the design and production stage, the issue is then followed by associated testing problems of VLSI circuit. A close study on the testing problems identified is to be solved with the implementation of Built-In-Self-Test architecture.

Chapter 3: The major topic of this chapter emphasizes on the architecture and features provided in the proposed design of the UART. The discussion continues with the implementation of BIST to the UART architecture to improve its testability feature.

Chapter 4: Xilinx Foundation Series 2i and VHISC Hardware Description Language (VHDL) play important role in the completion of this thesis. This chapter deals with the extensive use of the CAD tools and language based design to describe the structure and behavior of digital electronic hardware designs. The suitability of VHDL to design BIST is investigated. In addition, UART with BIST pin and register descriptions are presented throughout the rest of the chapter.

Chapter 5: This chapter focuses on the design implementation and verification of the UART with BIST design. The verification of the VHDL description is achieved through the correct simulation result of the intended implementation. The critical part of the generated waveform will be observed and discussed toward the end of the chapter.

Chapter 6: Chapter 6 guides the user on the hardware test to the real world application of UART with BIST design. The test is to assure that the designed circuit works as intended on the real FPGA chip since simulation results do not represent the real world. The implemented design to the FPGA will be tested using the tools and test boards provided by XESS Corporation.

Chapter 7: Overall discussion and conclusion of this thesis are given in this chapter.