CHAPTER 2

SUB-MICRON TECHNOLOGY & LOGIC TESTING

2.0 Introduction

The increasing growth of sub-micron technology has resulted in the difficulty of testing by many orders. Therefore, the designer and test engineers have no choice but to accept new responsibilities that have been performed by groups of technicians in the previous years. Manufacturers who thoroughly addressed the issue of testability at the device, board, and system levels have delivered more consistently reliable and cost-effective products to the marketplace. This means building in test capabilities in every phase of development including design verification, hardware (and software) integration and manufacturing must be ranked to a higher priority. Designers who do not design systems with full testability in mind open themselves to increased possibility of product failures and missed market opportunities.

This chapter will take the reader to the exploration of chip manufacturing and Design For Testability (DFT) techniques. The chapter will start with a discussion on problems that most VLSI chip manufacturers need to deal with before their products can be marketed. The discussion will be stressed on the issue of testability, which appears to be the main contributor to overall production cost. Next, an investigation on associated testing problems due to the complexity of VLSI component will be carried out. The

investigation will be followed by a Built-In-Self-Test technique to offer the solution to the VLSI testing problems.

2.1 Tests and Manufacturer

Nowadays Computer Aided Design (CAD) tools have been developed to help designers to design chips (or ICs) and verify their inputs and outputs by using simulation. However, it is not enough to just design and manufacture ICs without taking testability as a requirement. Manufacturing processes are extremely complex. They must make sure that designed circuits will function as intended. Therefore, to assure the reliability of each VLSI chip, they need to be tested. The cost of a test as in total production cost is shown in the formula [Upadhyaya, 2001] below:

Total production cost = Fabrication (**F**) + Packaging (**P**) + Assembly (**A**) + Testing (**T**)

As seen in the formula, total production cost consists of fabrication, packaging, assembly and test. A standard among people familiar with testing process says that the cost of '**F**', '**P**' and '**A**' would decrease per circuit. Nevertheless, this is not happening to the cost of test **(T)**. The reason why test cost does not decrease as '**F**', '**P**' and '**A**', is because the test can be further divided into three parts:

- Test Equipment Cost;
- Test Activity Cost; and
- Others.

Table 2.1: Summary of Test Cost

Test Equipment cost	Test Activity Cost	Others
• Test controller • Interface drivers + receivers • Cables and probe contacts	• Test pattern generator • Test design verification (fault simulation) • Documentation	• Test personnel

Furthermore, four stages to detect and diagnose a fault at different levels will also contribute to the total cost of a test. The levels are:

1. Circuit/Logic level;
2. Board level;
3. System level; and
4. Field level.

Due to denser integration at each level, the level of difficulty would go up and increase the cost on each level following the rule of 10 [Williams, 2000]. If it costs $0.30 to detect a fault at circuit level, it would cost $3.00 to test the same fault at board level, $30.00 at the system level and $300.00 if it to be tested in the field level. Therefore, if a fault can be detected at the lowest level (circuit/logic level), larger cost per fault can be avoided. The need of an early detection of fault has forced most designers to implement Built-In-Self-Test (BIST) technique to their designs. Therefore, further discussion on BIST technique will be carried out in the next section of this

chapter. Before proceeding to the discussion on BIST approach, it is appropriate to proceed with some of the main factors of VLSI testing problems.

2.2 VLSI Testing Problems

Today's highly integrated multi-layer boards with fine-pitch ICs are virtually impossible to access physically for testing. Traditional board test methods include functional test only accesses the board's primary I/Os, providing limited coverage and poor diagnostics for board-network fault. In circuit testing, another traditional test method works by physically accessing each wire on the board via costly "bed of nails" probes and testers. To identify reliable testing methods which will reduce the cost of test equipment, a research to verify each VLSI testing problems has been conducted. The major problems detected so far are:

- Test Generation Problems;
- The Input Combinatorial Problems; and
- The Gate to I/O Pin Ratio Problems.

2.2.1 Test Generation Problems

The large number of gates in VLSI (Very-Large-Scale-Integrated) circuits has pushed computer automatic-test-generation times to weeks or months of computation. The number of test patterns are becoming too large to be handled

by an external tester have resulted in high computation costs and have outstripped reasonable available time for production testing.

Another test generation problem is that computer algorithms providing Automatic Test Pattern Generation (ATPG) work well for combinatorial logic but rather poorly for sequential logic circuits. Sequential circuits demand too much computer memory and computation since many more time states must be evaluated [Ibrahim, 1995].

2.2.2 The Input Combinatorial Problem

A combinatorial logic circuit with N primary input nodes has a total set of 2^N possible input vectors. This is the number of test vectors required to exhaustively test a circuit for those functions that a customer might use. In contrast to MSI (Medium-Scale-Integrated) circuits, the number of test vectors needed to exhaustively examine a VLSI circuit such as 32-bits microprocessor is prohibitive. However, a finite number of test vectors still can be applied to an IC and follow the economic rules of production. The finite number of test vectors is much lesser than the full exhaustive test set of a VLSI circuit [Ibrahim, 1995].

2.2.3 The Gate to I/O Pin Ratio Problem

As ICs grow in gate counts, it is no longer true that most gate nodes are directly accessible by one of the pins on the package. This makes testing of internal nodes more difficult as they could no longer be easily controlled by signal from an input pin (controllability) nor easily observed at an output pin (observe ability). Pin counts go at a much slower rate than gate counts, which worsens the controllability and observe ability of internal gate nodes [Ibrahim, 1995].

VLSI testing problems described above have motivated designers to identify reliable test methods in solving these difficulties. An insertion of special test circuitry on the VLSI circuit that allows efficient test coverage is the answer to the matter. The need for the insertion has been addressed by the need for design for testability and hence the need for BIST.

2.3 Built-in-Self-Test (BIST)

Built-in-Self-Test (BIST) is a design technique that allows a circuit to test itself. This design technique will eliminate the VLSI logic problems that have been discussed in the previous section. It also eliminates the needs for ineffective and costly test methods. The use of BIST technique has long been recognized as means to reduce system life cycle test and maintenance costs. BIST provides shorter test times and allows

the use of low-cost test equipment during all stages of the product life: production test, acceptance test, field maintenance, and failure diagnosis.

BIST solves the problems associated with "Test Generation Problem" and "The Input Combinatorial Problem" by providing the circuit under test (cut) with Linear Feedback Shift Register (LFSR) and Multiple Input Signature Register (MISR). LFSR is a simple logic circuitry that generates pseudo random pattern test vectors for production testing. Since it is not practical to store all possible test data in a computer memory, LFSR uses its small circuitry to produce all the possible test data. The small circuitry of LFSR reduces the demand on a computer memory hence reduces the memory computation costs.

A large amount of data produced by LFSR at the input pins will generate large data output at the output pins. To observe each output pin each time the circuit under test produces result is not a practical approach to test a system. Because of this, MISR is added to the circuit under test to compress the data outputs into one signature, therefore the only value needs to be observed and compared is the signature. In spite of that, there is still weakness if MISR is applied alone. Applying MISR alone may lead to "The Gate to I/O Pin Ratio Problem" especially if the VLSI circuit using wide data bus (e.g. 32-bits data bus needed 32 extra pins). It is a waste to use most of the pins just to observe the test results of the circuit under test. This problem is solved by a scan register that will shift the parallel signature produced by MISR into serial data output signature that uses only one extra pin.

Implementing BIST technique to a design can save total production cost by reducing the needs for redesign because of system failure. Early detection of fault may avoid some significantly larger costs per fault. Furthermore, the user can minimize the purchase of expensive test equipment and still guarantee high-quality part for their application. To create a practical approach of this technique towards a real design, an implementation of BIST technique to a UART design will be described in the next chapter.