

CHAPTER 7

DISCUSSION AND CONCLUSION

7.0 DISCUSSION

The simulation and hardware tests have shown and ensured the capability and reliability of the designed UART chip. However, as discussed in the first and second chapters of this thesis, the reasons for the limited use of BIST is due to area overhead, performance degradation and increased design time. In this section, the reports after the optimization process will be used as a basis for comparing the UART design before and after the implementation of the BIST technique. **Figure 7.1** is the design and timing summary generated with and without the implementation of BIST technique. The summary is obtained from the implementation log file of XSE2i Project Manager software. By comparing these reports, it can be shown that the reliability of the chosen technique for the testable UART chip can be proven.

Design Summary:				
Number of errors:	0			
Number of warnings:	2			
Number of CLBs:		160 out of	196	81%
CLB Flip Flops:	133			
4 input LUTs:	279	(1 used as route-throughs)		
3 input LUTs:	49	(16 used as route-throughs)		
Number of bonded IOBs:		28 out of	61	45%
IOB Flops:	9			
IOB Latches:	0			
Number of clock IOB pads:		1 out of	8	12%
Number of primary CLKs:		1 out of	4	25%

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Number of secondary CLKs: 1 out of 4 25%
Number of TBUFs: 3 out of 448 1%
Number of startup: 1 out of 1 100%
Total equivalent gate count for design: 2789
Additional JTAG gate count for IOBs: 1344
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Timing summary:

Timing errors: 0 Score: 0

Constraints cover 2523 paths, 373 nets, and 1235 connections (100.0% coverage)

Design statistics:
Minimum period: 28.678ns (Maximum frequency: 34.870MHz)
Maximum combinational path delay: 33.437ns
Maximum net delay: 11.823ns

(a) UART without BIST Design Summary

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Design Summary:
Number of errors: 0
Number of warnings: 2
Number of CLBs: 190 out of 196 96%
  CLB Flip Flops: 158
  4 input LUTs: 342 (1 used as route-throughs)
  3 input LUTs: 54 (18 used as route-throughs)
Number of bonded IOBs: 35 out of 61 57%
  IOB Flops: 2
  IOB Latches: 0
Number of clock IOB pads: 1 out of 8 12%
Number of primary CLKs: 1 out of 4 25%
Number of secondary CLKs: 1 out of 4 25%
Number of TBUFs: 3 out of 448 1%
Number of startup: 1 out of 1 100%
  4 unrelated functions packed into 4 CLBs.
  (2% of the CLBs used are affected.)
Total equivalent gate count for design: 3289
Additional JTAG gate count for IOBs: 1680
```

Timing summary:

Timing errors: 0 Score: 0

Constraints cover 2848 paths, 443 nets, and 1498 connections (100.0% coverage)

Design statistics:

Minimum period: 31.270ns (Maximum frequency: 31.980MHz)

Maximum net delay: 13.626ns

(b) UART with BIST Design Summary

Figure 7.1: Design Summary

From the design summary, it can be observed that the number of CLBs used after the implementation of BIST technique is increased from 81% to 96%. The difference of 15% of the total CLBs area overhead will result in 1.803 ns (i.e. 13.626 ns - 11.823 ns) increment of the maximum net delay. The implementation of BIST technique also has resulted in the decrease of the maximum frequency from 34.87 MHz to 31.98 MHz. This shows that the UART with embedded BIST design may not work well if its host clock frequency exceeded the maximum frequency of 31.98 MHz. The reason why the design may not cater for high-speed clock is due to the possibility of a real time delay, which may be caused by temperature or the delay within the FPGA itself. The delay will limit the capability of data to be captured at some critical point. The faulty data captured may lead to errors at the output pins.

In spite of the hardware overhead obtained with BIST implementation, the overhead is somehow reasonable considering the test performance obtained. The thesis has proved that implementing BIST in a design has effectively satisfied on-chip test generation and evaluation. Although the technique was implemented on a low-end device, its usefulness as a testing process has been demonstrated. With the implementation of BIST, expensive tester requirements and testing procedures starting

from circuit or logic level to field level testing are minimized. The LFSR replaces the function of the external tester features such as a test pattern generator by automatically generating pseudo random patterns to give 100% fault coverage to the UART module. The MISR acts as a compression tool, compressing the output result when automatic pseudo random pattern is fed to the UART. The shift register minimized the input/output overhead by shifting the parallel signature produced by MISR into serial signature. The reduction of the test cost will lead to the reduction of overall production cost. Furthermore, the implementation of BIST provides a high-speed test result.

7.1 CONCLUSION

The main contribution of this thesis is to apply testing techniques and methods during the design phase in order to reduce the effort and cost of testing. In this thesis, a close study on the associated testing problems of VLSI circuit has been carried out. A Built-In-Self-Test technique using BILBO approach has been suggested to improve testability features of the designed UART circuits. BILBO has four modes such as normal function, shift register (scan in/out), Linear Feedback Shift Register (LFSR) and Multiple Input Signature Register (MISR). The discussion covered in chapter 2 has shown that the BILBO modes are suitable to replace expensive external tester requirements (e.g. Teradyne's Integera J750k test system would cost up to \$99,000). The BILBO also reduces significantly larger diagnosis costs per fault by an early detection of a fault at the lowest level (circuit/logic level (**Table 7.1**)). The level of difficulty would go up and increase the cost on each level following the rule of 10 [Williams, 2000].

Therefore, the minimization of expensive tester and diagnosis costs will reduce the overall production cost.

Table 7.1: Cost to Detect and Diagnose a Fault at Different Levels

CHIP LEVEL	\$0.30
BOARD LEVEL	\$3.00
SYSTEM LEVEL	\$30.00
FIELD LEVEL	\$300.00

The Universal Asynchronous Receiver Transmitter (UART) is the most widely used controller chip architecture to assure proper function of serial ports, which have been an important input/output tool for decades. In this thesis, the UART is designed to allow full duplex mode communication over serial communication links, increase accuracy, decrease the effect of noise and embedded with a testability feature. The UART was designed using National Semiconductor [National, 1995][Martin, 1989] and QuickLogic [Oelsner, 2000] standards and freely distributed modules of Generic UART [Harvey, 1999] with some modification to suite the implementation of BIST technique. The implementation of BIST technique to the UART design has been proven to provide opportunities for the sharing of system and test logic. The simulation and hardware tests conducted have ensured the capability and reliability of the design.

The thesis has proved that the implementation of BIST will reduce the computation effort and has guaranteed complete fault coverage for detectable faults in

high-speed test process. In the previous research, the possibility of performance or area overhead and the needs of initial design investment are the main reasons of the limited use of BIST. However, the overhead gain due to testable design technique in this thesis has been proven reasonable considering the test performance obtained.

The used of SRAM based FPGA technology has been proven to give the system designer a new degree of freedom and revolutionized the way systems are designed. The capability to change, manipulate, and store logic characteristics through programming (i.e VHDL) has helped to remove barriers between design and test engineers. VHDL has allowed quick design entry and the high degree of standardization makes it possible to have most testability features added to a design. This capability ensures for the manufacture of more quality and improved product to be created in the near future.

VHDL is also proven to be one of the most dominant language-based-tools, which allowed quick design-entry suites to describe the structure and behavior of digital electronic hardware designs. The wide usage of CAD tools will play an increasing important role in future products as complexity grows and shorter design times are required.