Chapter 1

.0 Introduction

MEMC was incorporated in 1984 under the name of Dynamit Nobel Silicon Holdings, Inc. (DNS). Huls AG, a subsidiary of VEBA AG, subsequently acquired ownership of DNS. In 1989, Huls AG, through DNS and other related companies, acquired the assets of Monsanto Company's electronic materials business. Huls AG changed the company's name to MEMC Electronic Materials, Inc.. MEMC sales for 1994 is US $ 660 million.

It is the second largest silicon wafer company with approximately 6,000 employees worldwide. It's headquarter is in St. Peters, MO. (USA). MEMC's products include Czochralski-grown silicon wafers; sold as-polished or with an epitaxial layer in diameter ranges from 4" to 8". The number of individually specified parameters leads to hundreds of unique products. Applications use ranges from discrete diodes to complex micro-processors and DRAM memories. Next generation use is silicon-on-insulator wafer (SOI) for high speed microprocessors, very high density memory, and low power applications.

MEMC produces silicon wafers ; the raw materials for device fabricators. The customers using wafers specify certain criteria or specifications for the wafers required.

Some of these specifications are :

1. Thickness of wafers.
2. Resistivity.
3. Flatness parameters : TTV, TIR, STIR
4. Surface-free defects : particles, chips, scratches, fracture, micro-roughness (haze)
5. Carbon and oxygen content.

Silicon, has been and will be the dominant material in semiconductor industry, which will carry us into the ultra-large-scale integration (ULSI) era. As the technology of integrated circuits (ICs) approaches ULSI, the performance of ICs is proving to be more sensitive to the characteristics of the starting materials. Although silicon is unarguably the most important material in the electronics and information era, no single source has covered the entire silicon crystal technology, from raw materials to silicon crystal modifications during the IC fabrication processes.

Currently, the device makers specify stringent requirement as the industry desires to make high speed and high density memory devices. Contamination in wafers, either formed during crystal growing process or wafer preparing processes, is a yield impacting factor to the IC device manufacturers. Therefore, the minority carrier's lifetime of the silicon wafers plays an important role on the device's performance. The impact of low minority carrier lifetime on negative device are :

1. Junction leakage.
2. Degraded refresh characteristic.
3. Early avalanche junction breakdown on high voltage devices.

This thesis is dedicated to the understanding of the importance of minority carrier lifetime of silicon wafers to the device makers which is in-line with the advancing IC technology towards ultra-large-scale integrated (ULSI) circuits ; understanding wafer manufacturing technology in relation to wafer minority carrier lifetime, various methods of lifetime measurement, real life examples of lifetime measurement data on manufacturing wafers and finally, discussion and conclusion on determining the critical steps within the wafer manufacturing processes in relation to wafer minority carrier lifetime. Normally, minority carrier wafer lifetime is known to be an average value. Therefore, for device fabricators, it is critical to understand the variation on minority carrier lifetime on silicon wafer surface. This thesis is also dedicated to understand this variation and the impact it has on device fabricators on production yield and device performance.

Silicon is the basic element used in solid-state electronic devices. The diffused interest in silicon properties is linked to the existence of transistor, that is the most extensively manufactured product. The estimate of 10^{15} transistors produced since its invention, in 1947 at Bell laboratories, is not far from reality. The date of invention of transistor, has usually been taken as December 23, 1947, when the point-contact transistor was demonstrated to the top executives of Bell Laboratories. The first public

announcement of their discovery and demonstration of their invention were not made until June 30, 1948 [1]. The extensive investigation and development in solid-state electronics led to invention of the " solid circuit ", which was eventually judged by the courts to be the first semiconductor integrated circuit (IC), by Kilby at Texas Instruments in 1958 [2].

Though the transistors were originally germanium - made, the set up of planar technology at Texas Instruments led to the sudden and almost complete replacement of germanium by silicon [3]. However, the narrow bandgap (0.66 eV) limits the operation of germanium-based devices to temperatures of approximately 90^{O}C due to the considerable leakage currents at higher temperatures. The wider bandgap of silicon (1.12 eV), on the other hand, results in electronic devices that are capable of operating up to around 200^{O}C [4]. A more serious problem than the narrow bandgap is that germanium does not readily provide a stable passivation layer on the surface. For example, germanium dioxide (GeO_2) is water-soluble and dissociates at approximately 800^{O}C [5]. Silicon, in contrast to germanium, readily accommodates itself to surface passivation by forming silicon dioxide (SiO_2), which provides a higher degree of protection to the underlying devices. Silicon has an advantage from the extraordinary masking qualities of SiO_2 against impurities and from the very low defectiveness of Si - SiO_2 interface, that allowed the development of metal-oxide-semiconductor (MOS) field-effect transistor. This advantage has been used to establish significant basic technologies, including the processes for diffusion doping and defining intricate patterns. In addition, other advantages of silicon from the environmental point of view are that silicon is entirely nontoxic, and that silica (SiO_2), the raw material of silicon, comprises approximately 60 % of the minerals in

the earth's crust. This implies that the raw material of silicon can be steadily supplied to the IC industry. Moreover, electronic-grade silicon can be obtained at less than one-tenth the cost of germanium [6]. Consequently, silicon has almost completely replaced germanium in the semiconductor industry.

The major achievements in MOS technology took place originally in the San Francisco bay area (the Silicon Valley) by Noyce at Fairchild [7]. Since the creation of the first IC, the density and complexity of electronic circuits manufactured on semiconductor chip have increased from small-scale integration (SSI), to medium-scale integration (MSI), to large-scale integration, to very large-scale integration (VLSI), and finally to ultra-large-scale integration (ULSI), which consists of 10^7 or more components per chip. Now the gap has been filled and the technological level is such that several industries have announced Mbit memories, i.e. semiconductor devices containing more than 1.5×10^6 MOS transistors in an area of about 30 mm^2.

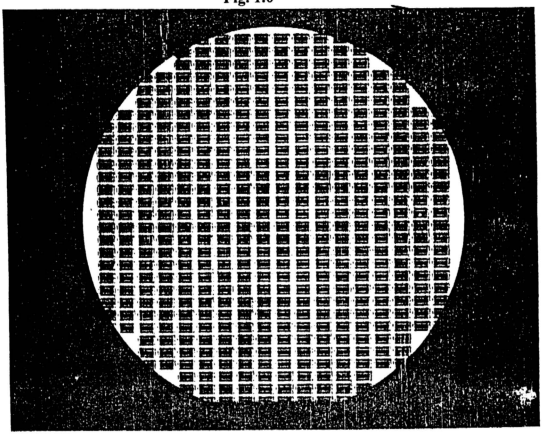
Table 1.0 shows the electronic evolution related to integrated circuits, since 1960 up to 1999, when a prevision can be done, about the number of transistors per chip, the chip size and the wafer diameter. A number of IC circuit chips are simultaneously fabricated on a silicon wafer through so-called batch processing. For example, Fig. 1.0 shows 1-Mbit dynamic random-access memory (DRAM) chips fabricated on a 150 mm diameter Czochralski silicon wafer. In order to attain more IC chips per wafer, silicon wafers of an ever larger diameter have been demanded by IC manufacturers. Fig. 1.1 shows the change in maximum diameter of float-zone and

Table 1.0

COMPLEXITY OF SEMICONDUCTOR INTEGRATED CIRCUITS

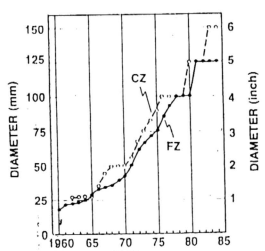
year	class	n° devices	litho (μm)	chip size mm^2	wafer size mm
60-68	SSI	2^1-2^7 (2-128)	> 10	1-15	25
65-75	MSI	2^6-2^{12} (64-4K)	3-10	10-25	50
72-83	LSI	2^{11}-2^{17} (2K-128K)	1 5-4	15-50	50-100
80-88	VLSI	2^{16}-2^{22} (64K-4M)	0 75-2	25- 75	100-125
85-93	ISI	2^{21}-2^{27} (2M-128M)	0 5-1	50-200	125-200
90-99	HSI	2^{26}-2^{32} (64M-4000M)	>0 5	100-400	>200

Fig. 1.0



DRAM chips (1 Mbit) fabricated on 150-mm-diameter Czochralski silicon wafer.

Fig. 1.1



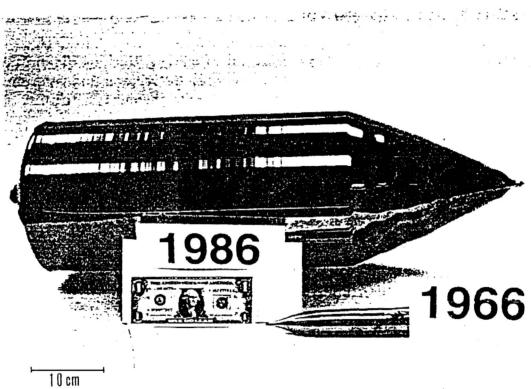
Change in the maximum diameter of float-zone and Czochralski silicon wafers used in the silicon industry from 1960 to 1985. (After Abe.)

Czochralski silicon wafers used in the silicon industry during the 25 years from 1960 to 1985 [8]. The difference in diameter of Czochralski silicon crystals is strikingly visualised in Fig. 1.2. The increased component density and device complexity, as well as the increased wafer diameter, are driving today's silicon wafers to ever more stringent specifications, since ICs and their fabrication processes are proving more sensitive to starting-material characteristics as IC technology approaches VLSI-ULSI. Therefore, considering the interrelationships among silicon material characteristics, IC fabrication and circuit performance are crucial to the successful fabrication of VLSI-ULSI circuits.

The presence of transitional metal impurities like Fe, Ni, Cu, Cr etc. are well known to influence semiconductor device parameters like leakage current, gate oxide breakdown voltage etc. The continuous decrease in dimensions makes present day integrated circuits even more sensitive to metal contaminations as they are recognized as a major yield limiting factor. As integration density increases the tolerable level of metallic impurities is decreasing ; most recent reports suggest that the minimal bulk contamination level should be below 10^{11} cm^{-3} . The control of such a low amount of contamination requires improved analytical techniques. Process control, requires fast, non-contact survey techniques. Minority carrier diffusion length or recombination lifetime measurements have been introduced for this purpose.

However, silicon is not an optimum choice in every respect. For example, compound semiconductors such as gallium arsenide (GaAs) [9], are superior to silicon in terms

Fig. 1.2



Commercial Czochralski silicon crystal ingots grown in 1966 and 1986. (Courtesy of R. A. Frederick and H-D. Chiou, Monsanto Electronic Materials Company.)

of electronic mobility, resulting in devices with reduced parasitics and improved frequency response. The most serious disadvantage of silicon might be that silicon cannot be applied to optoelectronic devices because of its indirect bandgap.

Some electronic and physical properties of germanium, silicon, and gallium arsenide are summarized in Table 1.1 [10]. However, it is certain that silicon will continue to be the dominant material in the semiconductor industry as a whole. In particular, single-crystalline silicon grown by the Czochralski method will steadily carry us into the ULSI era. In the next section, we will introduce and discuss the processes involved in the silicon wafering or shaping technology.

Table 1.1

Physicochemical Properties of Three Principal Semiconductors[a]

Properties	Ge	Si	GaAs
Atoms/cm^3	4.42×10^{22}	5.0×10^{22}	4.42×10^{22}
Atomic weight	72.60	28.09	144.63
Breakdown field (V/cm)	$\sim 10^5$	$\sim 3 \times 10^5$	$\sim 4 \times 10^5$
Crystal structure	Diamond	Diamond	Zincblend
Density (g/cm^3)	5.3267	2.328	5.32
Dielectric constant	16.0	11.9	13.1
Effective density of states in conduction band, N_c (cm^{-3})	1.04×10^{19}	2.8×10^{19}	4.7×10^{17}
Effective density of states in valence band, N_v (cm^{-3})	6.0×10^{18}	1.04×10^{19}	7.0×10^{18}
Effective mass, m^*/m_0			
Electron	$m_l^* = 1.64$ $m_t^* = 0.082$	$m_l^* = 0.98$ $m_t^* = 0.19$	0.067
Hole	$m_{lh}^* = 0.044$ $m_{hh}^* = 0.28$	$m_{lh}^* = 0.16$ $m_{hh}^* = 0.49$	$m_{lh}^* = 0.082$ $m_{hh}^* = 0.45$
Electron affinity (V)	4.0	4.05	4.07
Energy gap at 300 K (eV)	0.66	1.12	1.424
Intrinsic carrier concentration (cm^{-3})	2.4×10^{13}	1.45×10^{10}	1.79×10^6
Intrinsic Debye length (μm)	0.68	24	2250
Intrinsic resistivity (Ω cm)	47	2.3×10^{10}	1.79×10^8
Lattice constant	5.64613	5.43095	5.65.13
Linear thermal expansion coefficient (°C^{-1})	5.8×10^{-6}	2.6×10^{-6}	6.86×10^{-6}
Melting point (°C)	937	1420	1238
Minority carrier lifetime (sec)	10^{-3}	2.5×10^{-3}	$\sim 10^{-8}$
Mobility (drift) (cm^2/V sec)			
Electron	3900	1500	8500
Hole	1900	450	400
Optical-phonon energy (eV)	0.037	0.063	0.035
Specific heat (J/g °C)	0.31	0.7	0.35
Thermal conductivity at 300 K (W/cm °C)	0.6	1.5	0.46

1 Silicon wafering manufacturing technology

Semiconductor devices and circuits are fabricated through many mechanical, chemical, physical, and thermal processes. A typical flow diagram for semiconductor silicon preparation processes is shown below.

Silica (SiO_2)	
⇓	Silicon reduction process
Matallurgical-grade Silicon (MG-Si)	At ~ 2000 °C, carbon will reduce
⇓	SiO_2 into Si element. Si is converted
Trichlorosilane ($SiHCl_3$)	into $SiHCl_3$.
⇓	
Purification	$SiHCl_3$ reduced by hydrogenand purified
	by fractional distillation to remove other
⇓	complexes.
Polycrystal (polysilicon)	
⇓	
Crystal growing	By Czochrovski (CZ) or Float zone
⇓	(FZ) process.
Slicing	Special diamond saws are used.
⇓	
Lapping	Mechanical abrasions.
⇓	
Etching	
⇓	
Cleaning process	Cleaning process prior to annealing.
⇓	

Annealing ⇓ Annealing at 800 °C in a furnace.

Polished silicon wafer

⇓

(Gettering Treatment)

⇓

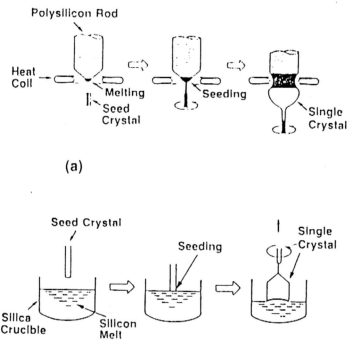
(Epitaxial Growth)

⇓

Microelectronic Circuit Fabrication

The preparation of silicon single-crystal substrates with mechanically and chemically polished surfaces is the first step in the long and complex device fabrication processing. The growth of single crystals of silicon from high-purity polysilicon (99.999999999 %) is a critical beginning step for electronic device fabrication. Although various techniques have been utilized to convert polysilicon into single crystals of silicon, two techniques have dominated the production of silicon single crystals because they meet the requirements of the microelectronics device technology. One is a zone-melting method commonly called the float-zone (FZ) method and the other is a pulling method traditionally called the Czochralski (CZ) method although it should be called more properly the Teal-Little method. The latter is widely being adopted by wafer manufacturer. So Fig. 1.3 illustrates the principles of these two crystal growth methods. In the FZ method, a molten zone is passed through a polysilicon rod to convert it into a single crystal ingot ; in the CZ method, a single crystal is grown by pulling from the melt contained in a quartz crucible. In

Fig. 1.3



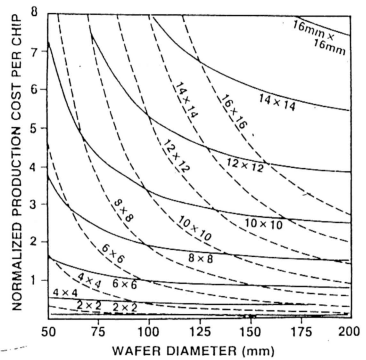
Principles of single-crystal growth by (a) float-zone method and (b) Czochralski method.

both cases, the seed crystal plays a very important role in obtaining the single crystal with a desired crystallographic orientation.

Since IC chips are produced through a " batch system ", the diameter of the silicon wafers used for device fabrication significantly affects the productivity and in turn the production cost. Fig. 1.4 shows the relationship between the normalized production cost per chip with different size and the diameter of the silicon substrates [11]. It is clearly observed that the electronic device industry has favorably used larger-diameter silicon wafers in order to reduce the production cost. Technologically, it is easier and less costly to increase the crystal diameter by the CZ method than by the FZ method. Although 200 mm diameter silicon wafer is the largest ones used for device fabrication, as far as the crystal growth technology is concerned, crystal of even larger diameter for example, 250 or 300 mm are available by the CZ method. The main problems that limit the practical use of the larger diameter wafers remain in the wafer shaping technology and device processing equipment. Fig. 1.5 shows a schematic view of typical Czochralski silicon crystal growing system and Fig. 1.6 is an example of a commercial crystal puller equipment.

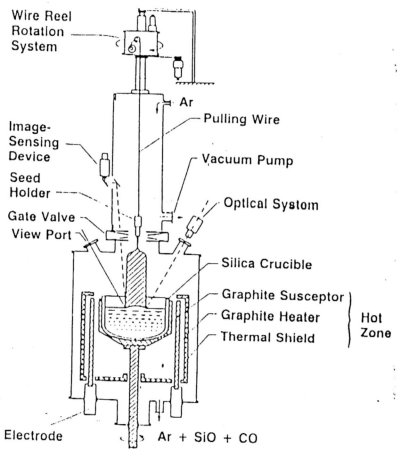
Semiconductor electronic devices are exclusively fabricated on polished wafers. Thus, the first step in device fabrication is the preparation of smooth, clean and damage-free surfaces. The requirements for geometrical tolerance of the polished wafer as well as their bulk crystal properties have become more stringent as the complexity of device design has increased. As the semiconductor device industry approaches the ULSI era, microelectronic circuits and their fabrication processes are proving more sensitive to the characteristics of starting material, which is the polished wafers. In this section,

Fig. 1.4



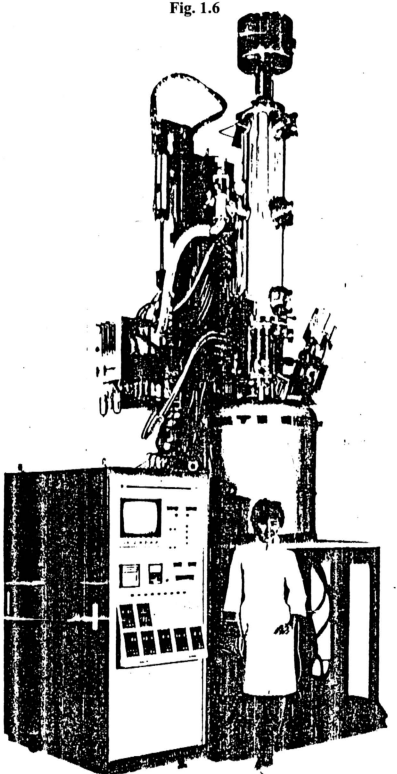
Relation between the normalized production cost per chip of different size and the diameter of silicon wafers. (After Takasu.[17])

Fig. 1.5



Schematic view of typical Czochralski silicon crystal growing system. (After Abe.[24] Reproduced with the permission of Academic Press, Inc.)

Fig. 1.6



Appearance of modern Czochralski silicon crystal growing equipment. (Courtesy of Kokusai Electric Co., Ltd)

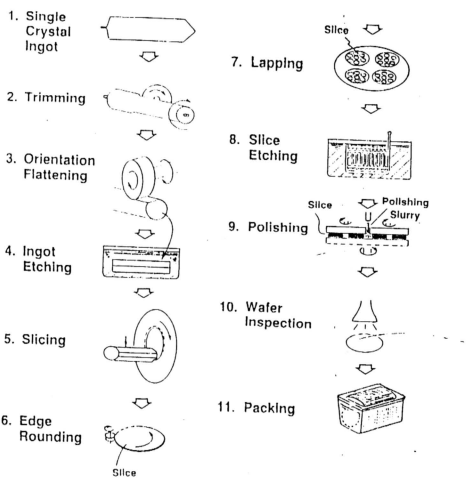
the wafer shaping processes and some important properties of silicon wafers are discussed.

Polished wafers are prepared through a complex sequence of shaping, polishing and cleaning steps after a single crystal ingot has been grown. Most of these processes referred to as wafer shaping are somewhat similar among silicon manufacturers; however, the details strongly depend on the know-how developed by each manufacturer. Therefore, the details of wafer shaping processes will not be elaborate since the competition among silicon suppliers is as extreme as that among the device manufacturers. Thus, the wafer shaping procedure presented below, according to Fig. 1.7, shall be generic.

1.1.1 Trimming

The single crystal ingot first passes through routine evaluation of properties such as resistivity and crystal perfection. The seed and tail ends are cut off and then the ingot is ground to a cylindrical shape of precise diameter since the ingot does not grow perfectly round nor with sufficiently uniform diameter. At this point the diameter is slightly larger than the final one since the diameter decreases during subsequent processing steps such as chemical etching.

Fig. 1.7



Generic wafer shaping processes.

1.1.2 Orientation Flattening

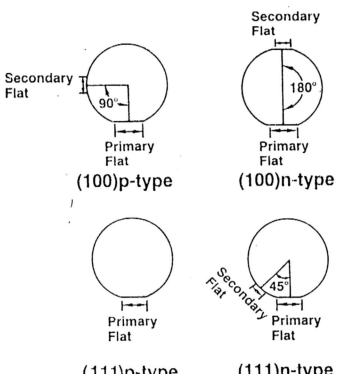
One or more flats that show the crystallographic orientation are ground along the length of the cylindrical ingot. The largest flat called the primary flat, is usually positioned perpendicular to the < 110 > orientation. The primary flat is used to correctly align the wafers during the device fabrication processes with automated wafer handling equipment. Thus, there are some device manufacturer who specified notch instead of primary flat. Since devices fabricated on the wafer must be oriented to specific crystallographic orientations, the primary flat is also used as the reference. The smaller flat or secondary flat, is utilized to identify the wafer plane orientation and the conductive type as shown in Fig. 1.8.

1.1.3 Ingot Etching

The ground crystal ingot is dipped into chemical etchant in order to remove mechanical damage induced by grinding and flattening, since the surface of the ingot will eventually become the edge of a polished wafer. Although the primary purpose of this etching process is to remove the mechanical damage, this operation also has a direct impact on the diameter tolerance. The etchant composition varies but most etchants are based on the well known $HNO_3 \bullet HF$ system. Etchant modifiers such as acetic acid are also used [12]. Chemical etching with this etchant system proceeds with the following two-step reaction :

1. $Si + 4HNO_3 \rightarrow SiO_2 + 4NO_2 + 2H_2O$ and
2. $SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$

Fig. 1.8



Orientation flats for different type wafers.

Since the reactions are exothermic, temperature control is critical for uniform etching. The reaction product NO_x is toxic and safety controls must be used.

1.1.4 Slicing

The slicing step produces silicon slices from the shaped ingot and critically defines the important factors of a wafer: the surface orientation, thickness, taper, bow, warp and so on. The ingot must be rigidly mounted to maintain exact crystallographic orientation obtained with X-ray diffraction, during the slicing process. The most common way to slice large-diameter wafer is inner diameter (ID) slicing which uses stainless steel core blades with diamond particles bonded on the inner edges [13]. Continuous monitoring with a blade deflection sensor is critically important to assure that slices are sawn with a minimum bow, taper and warp.

1.1.5 Edge Rounding

This step can come either before or after lapping. The edges of silicon wafers are rounded by an edge grinder or profiler. Fig. 1.9 illustrates typical shapes of rounded edges. Edge rounding substantially reduces mechanical defects such as edge chips and cracks due to handling with tweezers or loading into furnace boats. The higher mechanical strength of the wafer edge ensures a lower incidence of process-induced plastic deformation (i.e. slip dislocations which are preferentially nucleated at the edge chips and cracks) and increases the wafer yield due to lower frequency of wafer breakages during subsequent processes. Moreover, edge rounding minimizes occurrence of epitaxial crown in the epitaxial deposition process and a pile-up of

photoresist at the periphery of the wafer. The epitaxial crown or photoresist pile-up is schematically illustrated in Fig. 2.0. It is easily understood that this pile-up phenomenon causes serious problems in device patterning especially when contact makes are used.

1.1.6 Lapping

Lapping is performed on both sides of wafers primarily to remove the nonuniform damage left by slicing and to attain a high degree of parallelism and flatness of the wafer. The lapping abrasive slurry is typically a mixture of alumina or silicon carbide and glycerine.

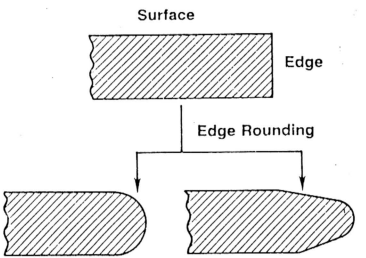
1.1.7 Wafer Etching

The mechanical damage induced during the previous shaping steps is removed entirely by chemical etching. The etching process is mostly accomplished with the chemical systems noted above (under ingot etching). Recently, a caustic etching system has been attractive as an alternative to the acid-etching system [14]. The system employs one of the alkaline hydroxides such as potassium hydroxide with certain stabilizers. The general reaction is

$$Si + 4OH \rightarrow SiO_4 + 2H_2$$

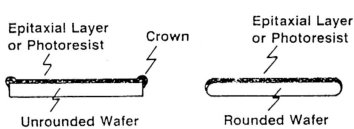
One of the advantages of this system is that the reaction system avoids the production of toxic NO_4. However, the etched surface of silicon tends to be somewhat rougher

Fig. 1.9



Typical shapes of wafer rounding.

Fig. 2.0



Epitaxial crown or photoresist pile-up phenomenon.

than that produced by acid etching since the caustic etching is basically crystal orientation-dependent.

1.1.8 Polishing

The polishing process is to produce a highly reflective and damage-free surface on one side and sometimes on both sides of the silicon wafer depending on the fabricator's requirement. Polishing of silicon is accomplished by a mechanochemical process in which a polishing pad and a polishing slurry of sodium hydroxide and fine silica particles are involved. Removal rate and resulting flatness of the wafer depend on various operating factors such as temperature, pressure, pad material, rotation rate and slurry composition. A slower polishing rate, in general, results in a smoother surface.

A recent decrease in the device geometry requires polished silicon wafers whose surface deviates only a few micrometers from the highest point to the lowest point when the wafer is held on a flat vacuum chuck. The polishing process along with crystal growing, has always been one of the most proprietary areas for the silicon wafer producers.

1.1.9 Cleaning

As mentioned earlier, surface contamination affects the electronic device performance and yields more severely as the device geometry shrinks. Thus, a primary concern in microelectronic circuit fabrication is the level of contamination on the wafers and the removal of such contamination before further processing. Cleaning of wafers is

absolutely required at many steps in device fabrication processes as well as wafer shaping (wafering) processes. The types of contaminants range from organic compounds to metallic impurities that are encountered by handling or processing. These contaminants attach to the wafer surface either chemically or physically. A variety of wafer cleaning techniques have been used to remove various different types of contamination. Contaminations is a yield limiting factors for device fabricators and consequently, this will affect the minority carrier lifetime in a silicon wafers. Therefore, it is critical that contaminations are maintained at its lowest and minority carrier lifetime at its highest level. In the next section, the cleaning procedure after polishing, the final stage before shipping to silicon users is discussed.

Types of Contaminants

Contaminants on silicon surfaces can be classified broadly as molecular, ionic and atomic. Typical molecular contaminants are waxes, resins and oils which are commonly used in the processes after sawing. They may also include organic compounds from human skin and plastic containers used for interim storage of wafers. Such molecular contaminants are usually held to the silicon surface by weak electrostatic forces. Since water-insoluble organic compounds tend to prevent the effective removal of adsorbed contaminants the molecular contaminants must be removed at the first stage in cleaning processes.

Ionic contaminants such as Na^+, Cl^-, F^- and I^-, are present after etching of wafers in HF-containing or caustic etchants. They may deposit on the silicon surface by physical adsorption or by chemical absorption (chemisorption). The removal of

chemisorbed ions is much more difficult than that of physically attached ions and a chemical reaction must be used to remove these contaminants.

The atomic contaminants present on silicon surfaces that are of the most serious concern are transition metals such as gold, iron, copper and nickel. They originate mainly from acid etchants (see Table 1.2). These transition metals as well as ionic

Table 1.2

Concentration of Dissolved Trace Impurities in Semiconductor-Grade Hydrofluoric acid[a]

Element[b]	Concentration (ppma)
Aluminum (Al)	< 0.05
Antimony (Sb)	< 0.02
Arsenic (As)	< 0.05
Barium (Ba)	< 0.1
Beryllium (Be)	< 0.02
Bismuth (Bi)	< 0.1
Boron (B)	< 0.05
Cadmium (Cd)	< 0.02 (typically < 0.01)
Calcium (Ca)	< 0.5 (typically 0.20)
*Chromium (Cr)	< 0.02 (typically < 0.01)
*Cobalt (Co)	< 0.02 (typically < 0.01)
*Copper (Cu)	< 0.02 (typically < 0.01)
Gallium (Ga)	< 0.02
*Gold (Au)	< 0.1 (typically 0.05)
Indium (In)	< 0.02
*Iron (Fe)	< 0.5 (typically 0.23)
Lead (Pb)	< 0.05 (typically 0.03)
Lithium (Li)	< 0.02 (typically < 0.01)
Magnesium (Mg)	< 0.2 (typically 0.06)
*Manganese (Mn)	< 0.05 (typically < 0.01)
*Molybdenum (Mo)	< 0.05
*Nickel (Ni)	< 0.02 (typically < 0.01)
*Platinum (Pt)	< 0.2
Potassium (K)	< 0.1 (typically 0.04)
Silver (Ag)	< 0.02 (typically < 0.01)
Sodium (Na)	< 0.2 (typically 0.08)
Strontium (Sr)	< 0.02 (typically < 0.01)
Thallium (Tl)	< 0.06
*Titanium (Ti)	< 0.1
Tin (Sn)	< 0.1
Vanadium (V)	< 0.05
Zinc (Zn)	< 0.1 (typically 0.02)
Zirconium (Zr)	< 0.1

impurities, seriously degrade device performance. The removal of these transition metals requires reactive agents which dissolve them and form metal complexes to prevent redeposition from the solution.

.3 Chemical Cleaning

Many chemical cleaning processes that aim to eliminate contaminants have been developed. The procedure most widely used in the semiconductor industry, is the so-called RCA method [15], which is a sequence of baths including $H_2O \bullet H_2O_2 \bullet HN_4OH$ solution (solution 1) and $H_2O \bullet H_2O_2 \bullet HCl$ (solution 2). Solution 1, typically 5-1-1 to 7-2-1 parts by volume of $H_2O \bullet H_2O_2 \bullet NH_4OH$, removes organic contaminants by both the solvating action of ammonium hydroxide (NH_4OH) and the powerful oxidizing action of hydrogen peroxide (H_2O_2). The ammonium hydroxide also serves to complex some of the Group I and Group II metals such as copper, gold, nickel, cobalt and cadnium. Solution 2, typically 6-1-1 to 8-2-1 parts by volume of $H_2O \bullet H_2O_2 \bullet HCl$, removes alkali and transition metals and prevents redeposition from the solution by forming soluble metal complexes. The chemical cleaning procedure based on the RCA method but slightly modified may be used by every silicon supplier and device manufacturer in the semiconductor industry.

Since the presence of a natural thin oxide layer on the silicon surface is suspected to hinder surface cleaning. The elimination of the oxide layer prior to further cleaning may further increase the purification efficiency. Brief etching in dilute hydrofluoric acid (HF) solution after Solution 1 cleaning was added to the original RCA procedure. It has been suggested that this brief etching should be performed with a very dilute high-purity HF solution and for a very short period of time to avoid

reinducing the contaminants from the HF solution. It has also been observed that the elimination of DI water rinse between HF and subsequent cleaning solution immersion gives high cleaning efficiencies and will not cause any silicon surface attack as long as only small amounts of HF remain on the silicon surface.

Two very important comments on chemical cleaning of silicon wafers have been made by the developer of the RCA method [16]. First, the wafers must never be dried during the processes because dried residues are difficult to redissolve and may mask the surface during subsequent treatments. Second, ordinary glassware should not be used with solutions 1 and 2 because substantial amounts of sodium, potassium, boron and other impurities are leached out of the glass by the hot solutions. High quality fused quartz ware should be used for wafer-cleaning vessels. Rinse tanks and vessels for HF solution should be constructed of high-grade teflon plastic.

It is unquestionable that the high-purity water is the most important material to assure purity for any cleaning processes. The quality of the water used significantly impacts the purity of the wafers and the yield in manufacturing of complex microelectronic devices [17]. Accordingly, the demands for the water used in the semiconductor industry have become more stringent with the advancing technology as shown in Table 1.3. Significant attention is also being focused on the yield loss problem due to microbes in DI water. Water produced by a sequence of deionization, filtration and ultraviolet irradiation has not been able to avoid the contamination due microbes. A recently developed technique that purifies DI water by oxidation using ozone may provide ultra-high-purity DI water to meet the stringent requirements.

Table 1.3

Trend of Pure Water Specifications for Microelectronic Device Fabrication*

Specification	1980	1983	1984	1985
DRAM bits	16K	64K	256K	1M
Resistivity (MΩ cm at 25°C)	15	17-18	18	18
Particles (μm)	0.2	0.2 0.1	0.1	0.1 0.05
Particles/cm^3	200-300	50 150	20-50	
Total organic carbon (mg/l)	1	0.5 1	0.05-0.2	0.05
Bacteria/cm^3	1	0.5 1	0.02	0.01
SiO_2 (ppb)		20 30	10	10
Dissolved oxygen (mg/l)	8	0.1 0.5	0.1	0.1

4 Wafer Scrubbing and Sonic Cleaning

Wafer cleaning with scrubbing either by special brushes or high-pressure jet fluid can enhance yields particularly when it is applied during wafer final cleaning or device fabrication processing by removing dirt and residual impurities left on the wafer surface by processing and during storage. In ultrasonic cleaning, where the latest technology is megasonic cleaning, wafers are immersed in a solution and are agitated by sonic energy has also a high advantage on wafer cleaning. This is largely used commercially in the current highly quality demanding requirements.

The following section, we will discussed on the theory of minority carrier lifetime before we proceed in the next chapter on the various measurement techniques and the most commonly commercial equipment used to measure diffusion length and minority carrier lifetime of silicon wafers.

5 Minority carrier lifetime theory

Lifetime measurements indicate recombination centers due to;

- contamination,
- oxygen precipitation and
- crystal defects.

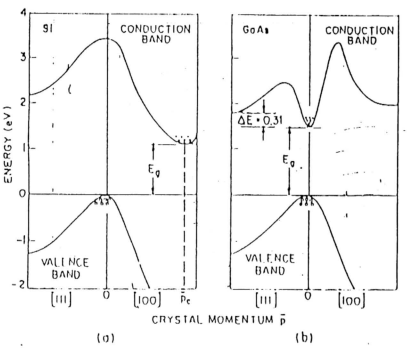
Whenever the thermal-equilibrium condition is disturbed, processes exist to restore the system to equilibrium. In the case of the injection of excess carriers, the

mechanism that restores equilibrium is recombination of the injected minority carriers with the majority carriers. Depending on the nature of the recombination process, the released energy that results from the recombination process can be emitted as a photon or dissipated as heat to the lattice. When a photon is emitted, the process is called radiative recombination; otherwise, it is called nonradiative recombination. Recombination phenomena can be classified as direct and in-direct processes. Direct recombination, also called band-to-band recombination, usually dominates in direct-bandgap semiconductors, such as gallium arsenide while indirect recombination via bandgap recombination centers dominates in indirect bandgap semiconductors, such as silicon. The latter is the topic of discussion.

For indirect-bandgap semiconductors, such as silicon, a direct recombination process is very unlikely, because the electrons at the bottom of the conduction band have nonzero crystal momentum with respect to the holes at the top of the valence band (refer Fig. 2.1). A direct transition that conserves both energy and momentum is not possible without a simultaneous lattice interaction. Therefore the dominant recombination process in such semiconductors is indirect transition via localized energy states in the forbidden energy gap. These states act as stepping stones between the conduction band and the valence band. Because the transition probability depends on the energy differences between the step and conduction and the valence band edges, these intermediate states can substantially enhance the recombination process.

Fig. 2.1

Energy Bands and Carrier Concentration



Energy band structures of Si and GaAs. Circles ( ) indicate holes in the valence bands and dots (•) indicate electrons in the conduction bands.

The lifetime, τ_p, for holes in an n-type semiconductor ; under low-injection condition in an n-type semiconductor so that $n_n >> p_n$, is given by ;

$$\tau_p = 1 / (v_{th} \sigma_p N_t)$$

where,

v_{th} - the thermal velocity of the carriers.

σ_p - the capture cross section i.e. the effectiveness of the center to capture a hole and is a measure of how close the hole has to come to the center to be captured.

N_t - the concentration of the centers in the semiconductor.

We can obtain a similar expression for electrons in a p-type semiconductor. Typical lifetime is about 0.3 μs for τ_p in p-type silicon. The lifetime is independent of the majority carrier concentration. Because there is an abundance of electrons in an n-type semiconductor, as soon as a hole is captured by the center, an electron will immediately be captured by the same center to complete the recombination process. Thus, the rate-limiting step in the recombination process is the capture of the minority carrier. Table 1.4 below compares present silicon characteristic and the stringent requirements of the very-large-scale integration (VLSI) technology.

The lifetime as given above is inversely proportional to N_t, the concentration of recombination centers per unit volume. For device operations that require long recombination lifetimes, the concentration of the recombination centers must be minimized. On the other hand, for high-speed switching operations, short

Table 1.4

Comparison of Silicon Material Characteristics and Requirements for VLSI[10]

Property[1]	Characteristics: Czochralski	Characteristics: Float zone	Requirements for VLSI
Resistivity (phosphorus) *n*-type (ohm-cm)	1–50	1–300 and up	5–50 and up
Resistivity (antimony) *n*-type (ohm-cm)	0.005–10		0.001–0.02
Resistivity (boron) *p*-type (ohm-cm)	0.005–50	1–300	5–50 and up
Resistivity gradient (four-point probe) (%)	5–10	20	1
Minority carrier lifetime (μs)	30–300	50–500	300–1000
Oxygen (ppma)	5–25	Not detected	Uniform and controlled
Carbon (ppma)	1–5	0.1–1	0.1
Dislocation (before processing)(per cm^2)	≤ 500	≤ 500	≤ 1
Diameter (mm)	Up to 200	Up to 100	Up to 150
Slice bow (μm)	≤ 25	≤ 25	≤ 5
Slice taper (μm)	≤ 15	≤ 15	≤ 5
Surface flatness (μm)	≤ 5	≤ 5	1
Heavy-metal impurities (ppba)	≤ 1	≤ 0.01	≤ 0.001

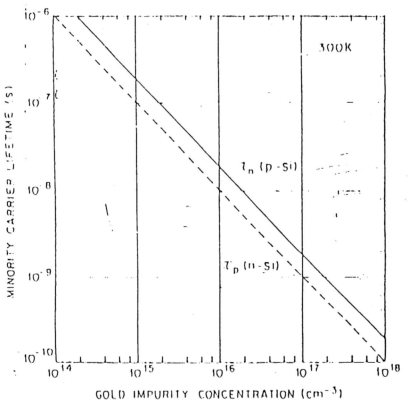
[1] ppma = Parts per million atoms; ppba = parts per billion atoms.

recombination lifetimes are required. In this case, the semiconductor is heavily doped with recombination centers. Many impurities have energy levels close to the middle of the bandgap. These impurities are efficient recombination centers. Typical example is gold in silicon. Fig. 2.2, shows the relationship of recombination lifetime versus gold impurity concentration. The minority carrier lifetime decreases linearly with gold concentration. By increasing the gold concentration from 10^{14} cm^{-3} to 10^{18} cm^{-3}, we can reduce the minority carrier lifetime from 1 μs to 0.1 ns.. In other words, by having contamination (recombination centers) in silicon will varies the minority carriers lifetime. Therefore, it is important that metallic contaminations are not added during the manufacturing processes of silicon wafers in order to improve the minority carriers lifetime to higher value.

Semiconductor crystals have been characterized by numerous kinds of electrical and physicochemical techniques. Meanwhile, specification of silicon wafers is becoming much more sophisticated and stringent as the relationship between microelectronic circuit device yield and specific silicon substrate parameters is being conclusively demonstrated.

The various properties of concern for characterizing silicon wafers are summarized in Table 1.5. Minority carrier lifetime has been one of the parameters to characterize the crystal perfection, since the lifetime depends strongly on crystal purity mainly with respect to metallic impurities - that is, so-called lifetime killers, which act as trap centers [18]. From the device operational point of view, although MOS devices are majority carrier operated, the minority carrier lifetime of the base material as an

Fig. 2.2



Recombination lifetime versus gold impurity concentration in silicon.[3]

Table 1.5

Selected Values and Trends of VSLI/ULSI Silicon Wafers

Material property	Value, trend
Electrical	
Oxide breakdown voltage	$\leq 1\%$ Failure for electric fields $\leq 5 \times 10^6$ V/cm
Flat-band voltage shift	≤ 0.2 V (Specifically defined metal gate test)
Generation lifetime	~300 1000 μsec
Resistivity variation	$\leq 10\%$
Chemical	
Cleanliness	$\leq 0.03/cm^2$ Particles (≤ 0.5 μm) on wafer front surface; $\leq 0.05/cm^2$ (≤ 1 μm) on wafer back surface: no wafer back surface stain
Oxygen concentration	Customer-specified; ± 2 ppma
Oxygen radial gradient	$\leq 3\%$
Carbon concentration	≤ 0.3 ppma
Metals	
Bulk	≤ 0.001 ppba
Surface	$\leq 10^{11}/cm^2$ for specific metals
Structural	
Grown-in dislocation	$0/cm^2$
OSF	$\leq 3/cm^2$ (Specifically defined oxidation test)
Mechanical	
Diameter	≥ 150 mm
Tolerance	≤ 0.2 mm
Thickness	625, 675 μm
Tolerance	≤ 10 μm
Orientation flat tolerance	≤ 1.5 mm
Total thickness variation	≤ 10 μm
Global flatness	≤ 3 μm
Bow	≤ 10 μm
Warp	≤ 10 μm
Local site flatness	≤ 1.0 μm/20 × 20 mm^2 field
Wafer curvature	Convex or concave specified by customer
Edge contour	Chip-free

important parameter controlling leakage currents of the channel, source, and drain. Moreover, a high minority carrier lifetime is desired to reduce the refresh time in RAM circuits and to perform efficiently in charge-coupled (CCDs). However, in some devices such as fast switching devices, the lifetime is intentionally minimized by doping with a metalic impurity such as Au. It also should be noted that high-lifetime is susceptible to discharge of the DRAM stored logic state due to electronic phenomena. For example, minority carrier currents induced by alpha particles result in the loss of information. Consequently, it is necessary to optimize the lifetime according to the device structure. Since it is known that the value of minority carrier lifetime on silicon wafer is an average value, it is critical that we understand the magnitude of this variation. This will have a direct impact on device performance and production yield performance of the device fabricators. Therefore, it is important that minority carrier lifetime is understood and studied on a microscopic level.

As mentioned several times, minority carrier lifetime of silicon wafers will affect the IC performance, thus, there is a substantial interest in the determination of the quality of silicon crystals or wafers, which are used as the starting material for the fabrication of ultra-large-scale integrated (ULSI) circuits, power semiconductors or solar cells as well as other purposes. This is influence by the imperfection of the silicon crystals or wafers. Distribution of lattice vacancies is one of the factors that will influence the quality of the wafers. Vacancies are an important factor for the formation of extrinsic defects such as dislocations, stacking-faults, swirls and other microdefects and for precipitation of oxygen, carbon, nitrogen or metals, which can all deteriorate the performance of semiconductor devices or solar cells fabricated on such low quality

silicon wafers. For instance, Fujimaki [19,20] found a correlation between so-called D-defects [21] and reduce breakdown voltage of metal-oxide-silicon (MOS) capacitors. D-defects are believed to consist of vacancies [22]. The breakdown voltage of thin oxide layers in MOS-FETs (metal-oxide-semiconductor-field-effect-transistors) also can be influenced by crystal defects and also can become too small when metal impurities precipitate in high vacancy concentration regions near the silicon surface. Oxygen precipitates in Czochralski (CZ) silicon also are believed to correlated to the vacancy concentration. Oxygen precipitates, dislocations and stackingfaults all cause high leakage currents and low breakdown voltages of devices and can lead to a decrease in the yield of IC chip production.