# *Chapter 4*

## 4.1 The effects of defects on Electrical Properties

### 4.1.1 Impurities

The contamination with metallic impurities is pervasive at many different silicon wafer processing steps especially during the wafer chemical cleaning processes. The silicon device fabrication processing particularly with furnace operation at high temperature increases the contamination. The primary electrical effect of metallic impurities is the introduction of energy levels close to the center of the bandgap of silicon. Since these levels act as recombination centers, metallic impurities cause a decrease in minority carrier lifetime and an increase in the leakage currents of p-n junctions. When the impurities exceed their solubility limits in silicon, metallic clusters generate and represent a dielectric constant discontinuity and reduce the breakdown strength of the oxide. Metallic impurities also generate other types of defect such as stacking faults or other precipitates and make dislocations and stacking faults electrical active.

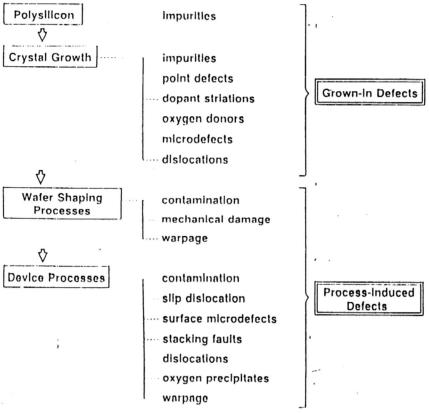
Under most circumstances, oxygen and carbon have no direct effect on the electrical properties of silicon crystals but rather induce secondary defects such as dislocations and stacking faults, which can strongly degrade the electrical performance of silicon devices. They may also act as preferential condensation sites for metallic impurities. Consequently, oxygen and carbon potentially lead to an enhancement of the junction leakage currents and a degradation of minority carrier lifetime.

These process-induced microdefects, excluding OSFs ( oxidation stacking faults ) and slip dislocations have been classified as either surface or interior ( or bulk ) defects as summarized in Fig. 4.3. Contamination, particularly with transition metals, during thermal processing initiates surface microdefects. On the other hand, interior microdefects are exclusively caused by oxygen precipitation which depends on various factors. Oxygen precipitates either can be interior microdefects by themselves or can originate secondary lattice defects such as dislocations and stacking fault by emitting excess silicon self-interstitials. These interior defects play a key role as intrinsic gettering sinks for surface impurities that would otherwise limit the device performance or initiate surface microdefects. These interior defects may also degrade the mechanical strength of silicon wafers when too much oxygen precipitation occurs; this result in serious warpage of silicon wafers. Consequently, it is essential to control oxygen precipitation to an optimum level during the thermal processes in order to maximize the device performance and device fabrication yield.

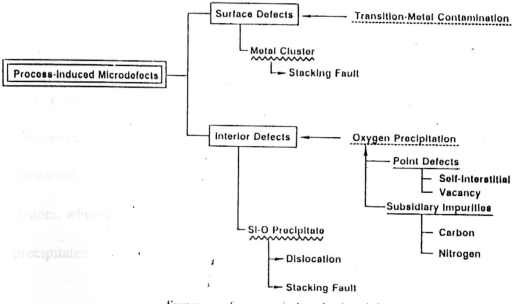
### 4.1.2 Oxygen and Carbon

As mentioned earlier, oxygen and carbon will induce secondary defects such as dislocations and stacking faults which strongly degrade the electrical performance of the silicon devices. Oxygen in silicon can uniquely form donors at up to $2 \times 10^{16}$ per $cm^3$ when the silicon crystal is heated at a temperature between $300\ ^{o}$ and $500\ ^{o}$ C with the highest formation rate at 450 $^{o}$C. This oxygen donor formation may cause variation in the resistivity of the silicon wafers and can even convert p-type silicon into n-type silicon. Fortunately, the oxygen donors can be annihilated by heat

**Fig. 4.3**




Semiconductor silicon manufacturing and device fabrication processes, and defects induced into silicon.




Summary of process-induced microdefects.

treatment in the temperature range between 650 and 800 $^{o}$C. Thus, the resistivity stabilization of silicon crystals is usually achieved by a thermal process called donor annihilation or commonly known in the industry as heat treating, where the wafers are typically maintained at a temperature between 650 and 700 $^{o}$C for about 60 minutes in an inert ambient followed by quenching in clean air. This process effectively removes oxygen donors from the silicon wafers which results in the resistivity being governed only by the dopant concentration. Recent investigation has shown, however, more complicated behavior of oxygen-related carrier concentration which strongly depends on heat treatment temperature [38]. Eventually, another type of oxygen donor called " new donor " [39] can be formed in silicon subjected to heat treatment in the temperature range between 500 and 900$^{o}$C. For convenience, the oxygen donors formed around 450$^{o}$C are occasionally referred to as " old donors ". The new donors can be annihilated by heat treatment at a high temperature > 1000 $^{o}$C [40]. Thus, the standard heat treatment for annihilation of old donors can cause the generation of new donors. In order to avoid new-donor generation, rapid thermal processing ( RTP ) at 650 $^{o}$C for a short time, on the order of seconds, has been suggested as an effective alternative donor-annihilation step. As regards the effect of carbon on oxygen donor formation, it has been reported that carbon strongly inhibits the formation of old donors, whereas it enhances the generation of new donors which are related to oxygen precipitates.

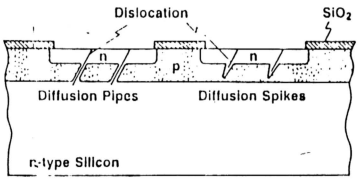
### 4.1.3 Dislocations

The primary effect of dislocations on the electrical properties of silicon electronic devices can be described as an enhancement of dopant diffusion which causes diffusion pipe or diffusion spikes in the p-n junction region as shown in Fig. 4.4. It has also been observed that dislocations directly or indirectly enhance junction leakage current when they cross the p-n junction and degrade the minority carrier lifetime. The effect of metallic impurities on electrical properties is straight forward. Apart from the effect of associated metallic impurities, the effect of dislocations on the electrical properties of silicon would be explained by the bandgap energy variation in the dislocation region. This change in the bandgap can be implied by a part of the lattice in the vicinity of a dislocation being compressed while another part is expanded and the change would have two effects :

1. the electron energy required for impact ionization may be reduced and hence, the ionization rate would be increased and
2. channelling of carriers into the dislocation core would occur.

Thus, the bipolar transistors developed for high-speed operation are particularly susceptible to dislocations because of their thin active regions. Moreover, dislocations act effectively as generation recombination centers and introduce surface states; thus dislocations decrease the minority carrier lifetime.

**Fig. 4.4**




Schematic illustration showing diffusion pipes and diffusion spikes caused by dislocations in *p-n* junction region.

### 4.1.4 Stacking Faults

Every stacking fault is associated with a dislocation loop, which bounds the fault plane. Therefore, the electrical effects of stacking faults are very similar to those of a dislocation. OSFs are defects most commonly observed in silicon device regions. Stacking faults that penetrate p-n junction greatly enhance the recombination centers and consequently enhance the junction leakage currents. Low leakage current is one of the most important conditions for reliable operation of all dynamic MOS devices such as DRAM and CCD. Stacking faults in MOS capacitors result in a deterioration of the refresh behavior of dynamic memories. The density of stacking faults in MOS capacitors has been inversely correlated with refresh time of MOS devices. The excess reverse current is harmful in charge storage type imaging devices such as silicon vidicon and CCD because the current results in bright spot image defects in a video display and lead to dark-current nonuniformity. It has been shown that high-density OSFs generated in MOS structures drastically increase the surface generation velocity and decrease the bulk lifetime. This oxide MOS capacitors that exhibit high leakage and low breakdown strength have been also correlated with the stacking faults located in the silicon substrate near the $SiO_2$/Si interface.

## 4.2 Conclusion

The minority-carrier generation lifetime optimization for DRAMs requires consideration of two apparently contradictory requirements. In one case, a high lifetime is desired to facilitate the retention of charge for an extended period of time, that is, high circuit refresh time. On the other hand, the high-lifetime materials is

especially susceptible to discharge of the DRAM stored logic state due to transient electronic phenomena. For example, alpha - particle - induced minority - carrier currents results in the loss of stored information. Intrinsic gettering in conjunction with the formation of a surface denuded zone can reduce the influence of the transient phenomena and increase circuit performance and yield. This is accomplished by fabricating the circuit and its voltage - dependent space - charge region in a sufficiently deep but essentially defect - free surface zone of high - lifetime material. The denuded zone should be sufficiently thin however, so that the bulk gettering sites are close to the circuit region to ensure effective gettering. It should be noted that the bulk gettering sites can also generate minority carriers during device operation, thereby requiring optimization of the denuded - zone depth for the specific circuit application. This procedure also has beneficial effects on CCD imager performance by collecting minority carriers generated by spurious radiation and on CMOS circuit latch - up control by reducing the recombination lifetime in the substrate. Since ICs typically operate in the temperature range of 75 $^{o}$C, the contribution of the diffusion current from the bulk becomes an important factor due to the exponential increase in $n_i^2$ with increasing temperature [40]. A significantly reduced bulk lifetime due to IG, for example, would increase the diffusion current ; however, increased substrate doping would substantially decrease the diffusion current. The utilization of a lightly doped epitaxial layer on a heavily doped substrate is particularly useful for reducing the diffusion current. This material configuration is capable of achieving both a high generation lifetime in the vicinity of the surface and low bulk diffusion current. The thickness of the epitaxial layer is also of critical importance. A sufficiently high

near-surface generation lifetime ( 300 - 1000 μsec ) at room temperature may be indicative of acceptable material purity at the circuit operating temperature where the diffusion current would be expected to dominate. Although the achievement of " lifetime doping " is still far away, improvements in process and gettering technique have significantly improved minority - carrier lifetime during the past decade.

The wafer parameters are classified as electrical, structural, chemical and mechanical material characteristics. The trends and target values for silicon wafers for VLSI/ULSI technology are summarized in Table 1.5 [41]. It is clearly shown in this table that minority carrier lifetime is one of the critical requirements to ensure the successful fabrication of VLSI/ULSI circuits. Ultimately, the growth of more perfect silicon crystals will be critical to obtain uniform, reproducible wafer characteristics, such as minority carrier lifetime, in order to ensure consistent IC performance [42]. Advanced crystal growth methdologies such as continuous pulling, the use of magnetic fields and automated crystal growth algorithms may present useful improvements. The further understanding and correlation of IC mulfunctions with test-device electronic parameters and ultimately with silicon wafer parameter ( minority carrier lifetime ) is essential to effectively design the silicon wafer characteristics for future circuits. Closer working relationships will be required between the silicon wafer manufacturer and IC manufacturer in order to effectively develope and fabricate advanced IC products. Although it may not be as straightforward, it should be noted that the above objectives strongly depends on the development of advanced diagnostic techniques to effectively assess the device impact of silicon wafer characteristics as well as the individual circuit design and fabrication process technologies. Present state-of-the-art

diagnostics, such as the detection of surface particles to the size of microns, evaluation of the native oxide and the related analysis of impurities such as minority carrier lifetime measurement, may not be sufficient for VLSI/ULSI requirements. The development of improved diagnostic techniques will indeed be a major driving force for establishing VLSI and ultimately, ULSI quality silicon wafers.

From the minority carrier lifetime mapping, we could also observed a big range on the lifetime values within a single wafer. From the old technology whereby, minority carrier lifetime is an average value taken from sample points of a wafer, one had concluded and assume that the minority carrier lifetime values in a single wafer is the same throughout the wafer [43]. However, modern technology with the evolution of state-of-the-art minority carrier lifetime measurement equipment such as ELYMAT, this philosophy had changed. The wafer's minority carrier lifetime mapping had indicated that there could exist a large range of lifetime value within the single wafer. This is a potential yield impacting factor to the device fabricators since certain region of the wafer could not be used for the device purpose. Therefore, it is extremely critical for wafer minority carrier lifetime to be studied on a microscopic level.