CHAPTER ONE : INTRODUCTION

Silicon is a very important technological material. It is one of the materials behind the semiconductor technology. Devices such as diodes and transistors are fabricated on silicon wafer that is produced from silicon single crystal. These wafers used ideally should be perfect single crystals. However real crystal always inevitably contains defects. Some defects are purposely introduced to alter the crystal properties. For example, doping of silicon with boron will result in p-type silicon which its majority charge carriers are holes. When silicon is doped with phosphorus during ingot growing, n-type silicon with electron as its majority charge carrier will be produced.

Besides dopant, other types of defects are normally unfavourable because their presence affect the device performance and some of them are difficult to remove. These included line defects, dislocation and etc. Although these defects are actually crystal imperfections that must be minimized during crystal growth, they do have a very useful property. Their presence can be used to block the diffusion of atoms especially volatile transition metals. The diffusing atoms will be gettered at these defect centres. In silicon wafer, oxidation induced stacking faults (OISF) on the non-device fabricating surface can be used to act as gettering sites for impurities.

1.1 (100) and (111) Silicon Wafers

Silicon is an elemental semiconductor and it crystallizes in diamond-cubic structure that consists of two interpenetrating face-centred cubic (FCC) unit cells. Figure 1.1 illustrates the silicon structure. One of the FCC unit is displaced with respect to the other by a/4<111>, where *a*, is the lattice parameter of the silicon. Each lattice site in silicon is occupied by same type of atom and each atom is tetrahedrally coordinated as in Figure 1.2.

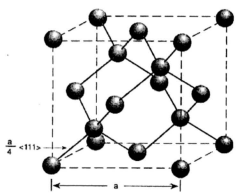

Figure 1.1 : Arrangement of atoms in the diamond-cubic crystal. Each atom has four nearest neighbours, which are arranged at the corners of a tetrahedron.

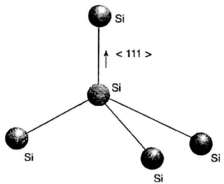

Figure 1.2 : Schematic illustrating the tetrahedral coordination of a silicon atom in silicon crystal.

Silicon atoms in single crystal touch each other along the four <111> bond directions, and the nearest neighbouring distance is $\sqrt{3}\,a/4$. Based on the hard sphere model [2], 34 percent of the silicon lattice is occupied by atoms, where its packing density is about 74 percent. General comparison of (100) and (111) wafer properties is shown in Table 1.1 while Figure 1.3 illustrates the projection of the diamond-cubic structure on a (111) plane.

Table 1.1 : Practical Comparison of <100>, <110> and <111> Silicon Wafers [2].

Factors	**Wafer Orientation**		
	<100>	**<110>**	**<111>**
Grown crystal quality	Good	Poor	Excellent
Growth rate	Excellent	Acceptable	Good
Mechanical Strength	Good	Good	Excellent
Radial dopant distribution	Excellent	Acceptable	Good
Oxidation rate	Good	Excellent	Excellent
OISF growth rate	Acceptable	Acceptable	Good
Surface state density	Excellent	Good	Acceptable

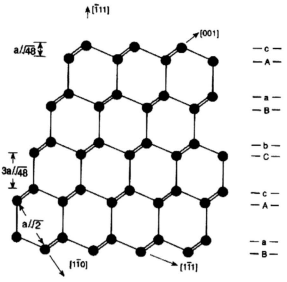

Figure 1.3 : Schematic illustrating the projection of the diamond-cubic structure on a (111) plane [1].

1.2 Stacking Fault (SF) and Oxidation-Induced Stacking Fault (OISF)

Stacking fault (SF) is a two-dimensional defect formed in silicon crystals. It can be formed on {111} planes in two distinct ways [1]: by shear or by agglomeration of point defects. For shear faults formation, stress must exist in the material to move Shockley partials to expand the faulted region. These stresses could develop during the growth of bulk crystal and also during epitaxial layering process. SFs formed of agglomeration, requires non-equilibrium concentrations of point defects, which could evolve during the growth of bulk crystals, oxidation of silicon, diffusion and ion implantation.

Surface of SFs is not electrically active because faulted and non-faulted planes are coherently bonded to each other without creating dangling bonds at the faulted surface. However partials bounding of various faults should be electrically active because of the presence of dangling bonds along the dislocation core. Their electrical activity will vary with the orientation and character of bounding partials.

Macroscopic characterization of SF will provide details on the density and distribution of SF while microscopic evaluation involved investigation of precipitation behaviour of dopant around SF, core structure of SF and crystallography of precipitates.

Figure 1.4 illustrates the formation of intrinsic and extrinsic stacking faults in the diamond-cubic by the agglomeration of point defects on (111) planes. Figure 1.4(a) is the layer arrangement of vacancy disc created on the A-a plane pair while

Figure 1.4(b) and Figure 1.4(c) are the representation of intrinsic fault and extrinsic fault respectively [1].

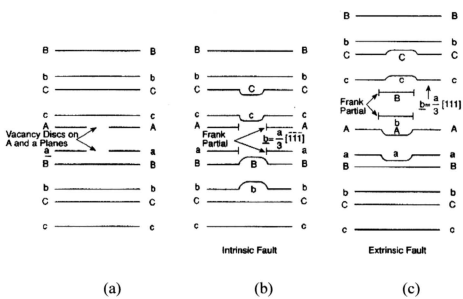

Figure 1.4: Schematic illustrating the formation of intrinsic and extrinsic stacking faults in the diamond-cubic by the agglomeration of point defects on (111) planes [1].

SF is a "platelet" that lies between two adjacent (111) planes. They are formed, by excess silicon atoms coalesced under favourable condition. SF fits between (111) planes causing its surrounding lattice to be strained [31]. After certain strain level is reached, the lattice will rupture, producing a dislocation loop, which bounds the fault. Thermal oxidation of silicon frequently results in the formation of SF. These SFs are commonly known as oxidation-induced stacking faults (OISF) [1, 2].

Many researchers studied OISF using preferential etching technique and optical microscopy. Normally specimens were oxidized at 1100 – 1300°C in steam, wet oxygen and dry oxygen before preferential etching. Researchers found that OISFs

are extrinsic in nature (*Refer Figure 1.4(c)*). The formation of OISFs is accentuated in the presence of surface damage however in the absence of surface damage, faults are observed only in wafer that exhibit the banded or "swirl" type distribution of micro-defects.

Extrinsic OISF is detrimental to silicon device processing [2] because it strongly affects the diffusion of impurities as well as oxidation precipitation in silicon crystal. OISF generated in bulk silicon is called bulk-OISF. They are often generated during prolonged oxidation processes. OISF generated near wafer surface region is known as surface-OISF. They are commonly observed in silicon epitaxial films that grown on silicon substrates and wafers with back surface damage (BSD).

Bulk-OISF and surface-OISF differed in structure and formation mechanism. Epitaxial-SF [2] nucleated dominantly at surface imperfections and SF's subsurface region. Surface-OISF should be differentiated from bulk-OISF because the former was formed by the introduction of process-induced nucleation sites [8], whereas the latter occur at native defect sites that were present in grown ingot.

Although OISF on fabrication side of the wafer is detrimental to silicon device processing, existence of OISF on the back surface of wafer, at required density and size, can become the gettering sites for the wafer. This enables the formation of denuded zone (DZ), for device fabrication on the front side of the wafers. DZ is a predetermined volume from polished surface that is defect and contaminant-free. The depth of denuded zone from polished surface varies from 10-20μm.

OISFs are predominantly generated at certain mechanical damages on the wafer surface [2]. However sodium contaminants, metallic impurities, hydrofluoric acid (HF) attack, swirl defects and oxidation precipitates also able to generate, or be the nucleation sites of OISF. Thermal oxidation of wafers with nucleation sites in dry oxygen (dry O_2) or wet O_2 (or steam), at elevated temperature, will create OISFs that can be delineated by preferential etching process.

Growth of OISF depends on oxidation temperature, oxidation time, oxidation ambient, crystal orientation and impurity concentration in silicon. Growth rates at <100> and <110> directions are about the same but the growth rate at <111> direction is three times slower than <100> and <110> directions. This is caused by higher plane packing density at <111> direction. Disorders caused by HF acids attacks are also more on the (100) oriented surface, results in more OISF on (100) surface compared to (111) surface [2].

1.3 Transition Metals and Gettering

1.3.1 Diffusion Process and Solubility of Transition Metals in Silicon [33, 12]

Transition metal atoms in semiconductors can occupy both interstitial and substitutional lattice sites. However the dominant diffusion mechanism is interstitial diffusion through the open diamond–type lattice. 3d transition metals substitution component can be neglected but this is not applicable to 4d and 5d transition metals.

The activation energies for interstitial diffusion of transition metals in silicon are between 0.5eV to 1eV. Activation energy systematically increases with atomic size in the 3d row from small atoms like Cu, Ni, to larger atom like Ti. The diffusion of the smaller 3d metals, Co, Ni, and Cu, in intrinsic silicon is so rapid that even at low temperature it is not possible to retain them by quenching in the interstitial sites for investigations. In highly phosphorus doped (P-doped) silicon, the diffusion of 3d elements, such as Cu, Fe, Mn and Co, is strongly affected by substitutional species and probably they will paired with the shallow donor. This will affect the mechanism of phosphorus-diffusion gettering.

During diffusion, Cu and Ni diffusing as positively charged species while the other 3d metals diffuse as neutral interstitials. After a sufficiently long diffusion, that is when the concentration of a transition metal is no longer dependent on the diffusion time, the concentration will reach a saturation value. This saturation

concentration is solid-state solubility. It is defined in thermodynamic equilibrium with a silicide as boundary phase below the eutectic temperature, of the respective phase diagram, and with the liquidus as boundary phase above eutectic temperature.

The solubility of 3d metals in intrinsic silicon is determined by interstitial species that are dominant at high temperature in thermal equilibrium. 3d transition metals show a clear trend towards decreasing total solubility for the larger, lighter 3d metals while highly phosphorus-doped silicon shows a solubility enhancement by several orders of magnitude due to multiple acceptor levels introduced by the substitution species.

Even though the equilibrium lattice site of transition metals in silicon is well defined at the diffusion temperature, cooling down the crystal will result in strong super-saturation. This super-saturation can either be frozen in for the case of substitution or slowly diffusing (light) 3d interstitials metals, or it leads to instabilities for fast diffusing interstitial metals. Fast diffusing Co, Ni, Cu, and Pd are found at room temperature in precipitates, as even fastest quenching cannot keep them in interstitial positions. Cr, Fe, Mn, and Co showed instability in their interstitial species through the formation of pairs, with shallow acceptors such as Ga, Al and B.

From the meta-stable behaviour of Fe-Al pairs, and the pairing kinetics of FeB and MnB, it was shown that those pairing reactions could be described by a Coulombic attraction of the positively charged transition metal with the acceptor.

Solubility and diffusivity of transition metals are given by

$$S = S_o \exp\left(\Delta \frac{S}{k} - \frac{\Delta H}{kT}\right)$$

$$D = D_o \exp\left(-\frac{\Delta E}{kT}\right)$$

where S_o, D_o are the pre-exponential factors, ΔS is the entropy, ΔH and ΔE are the enthalpies, k is the Boltzmann constant and T is the temperature in Kelvin.

Formation of transition metal precipitates requires the following conditions [12]:

(i) Increasing solubility of the transition metal with increasing sample temperature in order to reach super-saturation during the cooling period,

(ii) Sufficiently high diffusivity of the transition metal during the cooling period, and

(iii) Presence of nucleation sites either in the form of lattice defects or formed by a homogeneous nucleation process.

The first condition is satisfied by all transition metals. The second condition is satisfied by the fast diffusing metals like Co, Ni and Cu. The presence of lattice defect in the third condition depends on the thermal history of the silicon material. A homogeneous nucleation can be assumed for Co, Ni and Cu. Fe precipitation only happen via heterogeneous nucleation.

1.3.2 Gettering

Transition metals in semiconductors are usually very difficult to control and their presence is detrimental to device processing. They form deep level defects as isolated interstitial or substitutional atoms or in the form of simple complexes, such as metal-acceptor pairs [33]. In order to prevent the existence of transition metals that affects device performance, two strategies are being pursued. The device process steps are either designed to be very clean, from crystal growing to final packaging, so that contamination is reduced to a non-detrimental level, or specific gettering techniques have to be developed which allow removal of electrically active transition metal species reliably.

Volume contamination once introduced to silicon wafers may remain dissolved or precipitated during cooling process. Dissolved transition metals reduce the carrier lifetime and increase the generation-recombination current while precipitated transition metals soften the reverse current-voltage characteristics and increase the generation-recombination current [12].

Gettering [2, 11, 12, 33, 34] refers to a process that reduces the concentration of impurities in part of a wafer by localizing them in predetermined regions of the wafer (away from those to be occupied by devices). Smaller 3d transition metals are generally diffused by interstitial diffusion mechanism. Smaller 3d transition metals with very high diffusivity such as Co, Ni and Cu, they are able to move from front surface of wafer (device fabrication region) to the predetermined

regions, within considerably short gettering time. As for slow diffusing elements like Ti, the gettering process takes about 1 hour at 1000°C.

There are two major types of gettering methods used : intrinsic gettering (IG, also known as internal gettering) and extrinsic gettering (EG). IG is provided by intrinsic or extrinsic defects created after annealing which up to now has been achieved only in Czochralski (CZ) method grown silicon by oxygen precipitation. EG [33] is brought about by intrinsic or extrinsic defects after external treatment, like phosphorus diffusion, ion implantation, surface damage, poly-silicon deposition, etc.

1.3.3 Intrinsic Gettering in Silicon (IG)

IG of impurities [11, 12, 30, 31, 33, 34] (mainly interstitial transition metals) in CZ-silicon has been observed after the following sequence of heat treatments:

(i) Annealing above 1100° for the out diffusion of oxygen

(ii) Annealing below 800°C to nucleate oxygen precipitates

(iii) Annealing above 900°C to accelerate the growth of oxygen precipitates

Annealing step (i) reduces the oxygen concentration in a several 10μm thick layer below the surface towards the solubility at this out diffusion temperature. In the subsequent nucleation step the super-saturation of oxygen in this subsurface layer is no longer sufficient to form stable nuclei. However, nuclei will be formed in the interior of the crystal because homogeneous nucleation requires a higher super-saturation. Nuclei after reaching a critical size remain stable to grow during the third annealing step. The resulting concentration gradient is the driving force for diffusion into the bulk, which is the actual gettering step. Thus the gettering efficiency depends on the difference between the precipitation kinetics of the impurity in denuded zone (DZ) and bulk.

Three main defects found to be stable above 900°C are amorphous oxygen precipitates (SiO_x, $x \approx 2$), SFs, and dislocations. Due to the lower density of silicon in SiO_2 as compared to bulk silicon, the growing oxygen precipitates build up high strain fields. This strain can be relaxed at higher temperatures by punching out dislocations or by emission of silicon self-interstitials. The latter

may precipitate to form bulk-stacking faults. All oxygen-precipitation-induced-defects were decorated by metal impurities after an IG treatment.

1.3.4 Extrinsic Gettering in Silicon (EG)

It has been observed that surface can play an extremely important role in the removal of copper from the lattice. On mechanically polished samples, a characteristic type of precipitation takes place, which tends to concentrate the copper rich phase at the surface. EG usually uses the backside of a wafer to collect impurities. Some of the most commonly used techniques are P diffusion, ion implantation, and mechanical backside damage or poly-silicon deposition.

Defects in the damaged layer like stacking faults and dislocations act as nucleation centers for interstices impurities only after super-saturation [27, 33, 34], i.e. during cooling. As wafer thickness is 10 times larger than a typical denuded zone, effective gettering would take about 100 times longer than what IG required. This means that EG can be achieved within a minute or less for most 3d metals. However this process is expected to be less effective than an optimized IG process.

Thomas [23] studied Cu precipitation at OISF at different copper diffusion temperature. Having very high diffusivity and its marked change in solubility with temperature, Cu is easily precipitated. In order for precipitation to take place nuclei must be formed either homogeneously or heterogeneously. Homogeneous nucleation by aggregation of Cu atoms required high degree of super-saturation (required very high cooling rate). In heterogeneous precipitation, nuclei already present as other imperfections e.g. dislocation or precipitate, therefore a much lower super-saturation ratio is needed.

If Cu is diffused into a mechanically polished silicon wafer at temperature 1000°C or less, precipitation takes place along dislocation lines. Only a small portion of the dislocation act as nuclei and Cu is separated into discrete particles along the dislocation line. As the copper concentration is low, the precipitation is confined to the region of the dislocation and does not assume the crystallographic forms observed in silicon, which has been cooled after Cu diffusion at higher temperatures. The presence of the defects and large numbers of precipitates on the surface caused Cu to be removed from bulk material.

At 1000~1150°C, Cu precipitates lie as discrete particles parallel to {110} planes while Cu-platelets will form on the surface when diffusion temperature is higher than 1150°C. Basically what Thomas [23] observed in his studies was a heterogeneous nucleation for Cu precipitation. Initial precipitation of Cu takes place at dislocations introduced during polishing and which remain near the surface. The amount of Cu dissolved in the silicon appears to be a function of temperature alone, as the total volume of precipitate formed is approximately constant and independent of the number of precipitates formed.

1.4 Motivation and Objectives

OISF nucleation mechanism, OISF growth and factors affecting OISF density were extensively studied using mechanically damaged wafer and defect-free wafers. Sand Blasting is a relatively simple and economical technique used to create mechanical damages on wafer surface for the preparation of external gettering sites.

Currently damaged site density created by sand blasting process on (100) wafer was monitored by OISF density formed on (111) monitor wafer. Sand blasted monitor wafers have to go through a high temperature heat treatment in oxygen to enable OISF formation. OISFs formed were delineated by preferential etching process. OISF formed on (100) wafer tends to overlap, complicating OISF counting process especially when counting was done manually under optical microscope.

Having (111) wafer used to monitor OISF density while most of the wafer processed were (100) wafer, the investigation on the OISF density correlation between these two crystal orientations at different blasting condition and the impact of their differences to extrinsic gettering process become very important.

This project was initiated to study the OISF dimension and OISF density change as a function of different surface removal and blasting pressure, for (111) and (100) sand blasted wafer.

Present work has two main objectives, namely :

(i) To investigate the effect of excessive etching and blasting pressure to OISF density and OISF dimension in (100) and (111) sand blasted wafers.

(ii) To determine the impact of surface removal and blasting pressure to OISF density in (100) and (111) sand blasted wafers

1.5 Outline of This Thesis

This thesis comprises seven chapters. Chapter 1 presents relevant background theory on silicon crystallography and OISF characteristics. Chapter 2 focuses on important findings by researchers studying OISF characteristics and its properties. Chapter 3 describes basic experimental techniques and basic concepts of measurement techniques used in this study. Chapter 4 reports tests results for etching rate comparison between (100) and (111) wafers. Chapter 5 reports experimental results for OISF dimension change as a result of repeated preferential etching and difference blasting pressure. Chapter 6 reports on the comparison of OISF density as a function of surface removal and blasting pressure, between (100) and (111) wafers. Lastly Chapter 7 presents the conclusion of this project.