

ABSTRACT

Testability methods are applied before or concurrently with the system logic design and not as an afterthought when the circuit is completed. This research proves this method by proposing circuit modification or addition of a special test circuitry to allow for a better test process. This dissertation investigates the design for testability (DFT) techniques. In addition, aspects of microprocessor testability features, microprocessor test generation, and the need for built-in self-test (BIST) are presented.

This dissertation discusses the major issues associated with BIST techniques (increased design time, area overhead, and test effectiveness). In particular, the primary objective of this research is to implement a behavioural VHDL description of the AMD2901 processor incorporated with a BIST circuitry into the existing AMD2901 design to produce a testable processor with minimum area overhead. VHDL is used to describe the functional behaviour of the AMD2901 models. The AMD2901 is used because of the simplicity of the individual processors and the regularity of the slice interconnections. This research highlights the use of the linear feedback shift register (LFSR) and multiple input signature register (MISR), as a pattern generator and response analyzer respectively with the aim of reducing the extra amount of circuitry required.

Simulation and synthesis tools in SYNOPSIS are used for simulating and synthesizing the proposed design. The Test Compiler in SYNOPSIS is also used to generate test vectors using the statistical ATPG, and to obtain the associated fault coverage. Finally, a C++ program is written to compare and verify that the LFSR vectors produced give the same fault coverage as the ATPG patterns. The testable AMD2901 is proven to have perfect fault coverage, minimal area overhead, and short testing time.