CHAPTER ONE : INTRODUCTION

1.0 Introduction to Semiconductor Material : Silicon

Silicon is the second most abundant element on earth. It is found mainly in the form of oxides and silicates. With a supply of these raw materials, the problem is to transform oxides and silicates into the high purity and "defect free" silicon substrates required by the semiconductor industries. These silicon substrates can now be produced in mass production using the present technology in silicon crystal growth, wafer preparation processes in clean environment of clean-room system. Hence, the silicon has become most dominant semiconductor material in the semiconductor industries today.

In the semiconductor industries, silicon substrates are mainly used by the manufacturer in devices and integrated circuits fabrication. The devices and integrated circuits are fabricated through many mechanical, chemical, physical and thermal processes. However, the preparation of silicon substrates with mechanically and chemically polished surfaces is the first step in the long and complex fabrication processing. The first and absolute requirement is the extreme purity of the silicon. The required purity of the silicon is 99.999999999 %. Therefore, the purity of the silicon may be affected by small amounts of foreign atoms which could change the electrical properties such as effective minority carrier recombination lifetime or effective lifetime, τ_{eff}.

Effective lifetime is one of the important properties in silicon. It is used by the silicon wafer manufacturers to indicate the quality of the crystals. For example, the effective lifetime for a silicon wafer with resistivity of 9~12 Ωcm is about 10 μsec typically. After surface passivation with oxidation temperature of 1000 °C for 100 minutes, the effective lifetime may increase to more than 250 μsec depending on the quality of the wafer. The effective lifetime can be manipulated during crystal growth and device fabrication to obtain desirable operation characteristic of the devices such as dynamic random access memory (DRAM) and charge coupled devices (CCD)[1,2]. A long effective lifetime will require less refresh time and to perform in more efficient transfer of charges in DRAM and CCD respectively. However, in other devices such as the fast switching devices, the effective lifetime is intentionally minimized by doping with a metallic impurity such as Au[3,4,5].

The study of UV-irradiation effects on the recombination lifetime of silicon wafer has been carried out in S.E.H (M) Sdn. Bhd. which is one of the leading producer of silicon wafers in the world. All the experiments has been done in the class 1000 clean-room.

1.1 Silicon Wafer Production

The following Figure 1.1 shows the wafer production through a sequence of shaping, polishing and cleaning steps after a single crystal ingot has been grown by the Czochralski pulling method[6]. In this method, the ingot is grown from the melted polysilicon in a quartz crucible. After the crystal pulling, the ingot goes through a wafer shaping processes (Figure 1.1(b)~(i))[7] with defined specifications as shown in

Table 1.1. The single crystal ingots mentioned above are imported from Shin-Etsu, Japan whereas the silicon shaping processes are done by S.E.H (M) Sdn. Bhd.

No.	Characteristic	Specification
i	Crystal orientation	⟨100⟩
ii	Diameter	150.0 ± 0.5 mm
iii	Thickness	550 ± 15 μm
iv	Global total thickness variation	≤ 3.5 μm
v	Warpage	≤ 20 μm
vi	Dopant	Boron (*p* -type)
vii	Resistivity	9 to 12 Ωcm
viii	Surface finish	Polished
ix	Backside finish	Etched

Table 1.1 : The physical and electrical characteristics for the silicon wafers used in this work

In the silicon wafer production, the single crystal ingot is first ground to a cylindrical shape. Then one or more flats are ground along the length of the cylindrical ingot to show the crystallographic orientation. After that, the ground single crystal ingot is dipped into chemical etchant in order to remove mechanical damage induced by grinding and flattening. The slicing step produces silicon wafers from the shaped ingot after the previous processes. The following step is to round the edge by an edge grinder. Edge rounding substantially reduces mechanical defects, such as edge chips and cracks. Then, lapping is performed on both sides of wafers, primary to remove the nonuniform damage left by slicing, and to attain a high degree of parallelism and flatness of the wafer. After lapping, the wafers are etched by chemical etchants. The

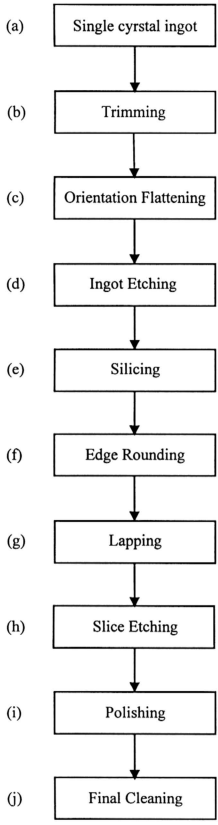

Figure 1.1 : Silicon wafer production processes

etching process is used to remove the mechanical damage induced during the previous shaping steps. The last step in wafer shaping process is wafer polishing. The polishing process is to produce a highly reflective and damage-free surface on one side of the silicon wafers and critically defines the important factors of a wafer as shown in Table 1.1. Finally, the polished silicon wafers are then send for cleaning to remove particles and contaminants from the wafer surface.

1.2 Recombination Lifetimes

In a silicon wafer, the effective lifetime depends on the bulk and surface recombination lifetimes (Chapter 2, eqn. (2.14)). The bulk recombination lifetime is influenced by various types of lattice defects[8] such as vacancy, interstitial and complexes, the impurities introduced during crystal pulling and the wafer shaping process. It introduces localized energy states within the bandgap of the silicon which may act as trapping or recombination centers depending on the relative probability of a trapped carrier being re-emitted to its appropriate band and recombined with a free carrier from the opposite band. A recombination center is effective only if it is capable of existing in two different charge states and equal access to both the conduction and valence bands. Only deep-lying energy states, that is those close to the center of the bandgap, meet both requirements.

For a wafer with finite dimension, the surface energy states and localized energy states at interfacial SiO_x layer[9-25] (region between silicon and other media such as native oxide layer[26,27]) may change the surface recombination lifetime. It

is related to the surface recombination velocity, S_r which is defined as the ratio of the rate of electrons or holes which flow into a unit surface area to the excess carrier density in the bulk just below the surface. The value, $S_r = 0$ implies a perfect surface devoid of trapping states while $S_r >> 1$ corresponds to a perfect sink for excess minority carriers in the silicon. The energy states which may decrease the recombination are formed by abrupt termination of silicon crystal lattice at the interface, imperfections and the contaminants.

The dangling bonds at the silicon wafer surface are highly reactive to various species outside the crystal[28]. Bonding of foreign species on the surface by chemical or physical adsorption may form localized energy states which change the surface recombination velocity. These surface states can be passivated by oxidation, chemical treatment or recently, through UV irradiation[29-32]. The thermally grown oxide layer for passivation is obtained by heating silicon wafer in either the oxygen or water vapor environments. The silicon dioxide (SiO_2) layer is largely impervious to contamination and protects the underlying silicon substrate. In chemical passivation, the hydrofluoric (HF) acid[33-36] or iodine, for example, are used to reduce the dangling bonds on the silicon wafer surface. The stability of the HF or iodine treated surface has been mainly attributed to passivation due to hydrogen and iodine. The present work investigates the UV irradiation effects in some details.

1.3 The Effects of UV Irradiation

Some of the important effects of UV irradiation on the silicon wafers are

(a) The change of effective lifetime

(b) Breaching and regeneration

(c) Internal photoemission

(d) Traps generation

The following will discuss these effects in detail.

(a) The change of effective lifetime after the ultraviolet (UV) irradiation on silicon wafers with a native oxide layer was investigated by Katayama et al[29] using noncontact laser-microwave photo-conductivity (LM-PCD) measurement technique. They have shown that the UV irradiation greatly decreased the surface recombination velocity in wafers already having a native oxide layer. This was deduced from the measured effective minority carrier recombination lifetime (τ_{eff}). The effect disappeared rapidly after the UV irradiation was switched off. A model was also proposed by Katayama[30] to explain the transient recovery of the effective minority carrier lifetime after the UV irradiation. The model proposed that the oxygen molecules in the oxide layer were photoionised which produced an electric field that could bend the energy bands in the silicon. This band bending decreased the surface recombination velocity in both *n*- and *p*-type silicon. These led them to suggest that the effective minority carrier lifetime

recovery process was dominated by the ≡Si-OH bonds which act as a transition step to the electron transfer from the oxide layer to the substrate silicon. Further investigation were done by Zhong et al[31], who showed that the "recovery time" in the effective lifetime could be largely characterized by an exponential term. The explanation was also supported by a theoretical argument by Buczkowski et al[32].

(b) The effect of UV irradiation on silicon wafers was also investigated by Caplan and Poindexter[37,38].They studied UV bleaching and regeneration of Pb ($\bullet Si{\equiv}Si_3$) centers[39-56] using the electron spin resonance (ESR) technique at the Si/SiO_2 interface of a very thin thermal oxide. They proposed a model to explain the bleaching and regeneration of Pb centers after UV irradiation. This model suggested that the 4.9 eV UV photons have ample energy to excite a valence electron to the conduction band of SiO_2. At the conduction band, the electron is attached to the O_2 molecule forming negative ions, O_2^- on the SiO_2 surface. The accumulation of negative charge on the oxide surface bends the energy bands in SiO_2 and Si so much that the Pb centers, which lie above the Fermi level are depopulated and form the $+Si{\equiv}Si_3$, which are invisible to the ESR.

(c) The UV irradiation also produced electrons which move into the E′ sites[57-64] in the oxide layer as reported by Witham and Lenahan[65,66] using the ESR and capacitance-voltage (C-V) measurement techniques. They subjected their MOS devices with a 500 Å thermal oxide layer to UV radiation. The irradiation resulted in the internal photoemission of electrons from the silicon into the oxide. Some of

these electrons were then trapped at the positively charged E′ sites. The positively charged E′ site was formed after a hole trapped inside a deep oxide trap (E′)[67-73]. They showed that the hole trapping process involving E′ centers was entirely consistent with the simple oxygen vacancy model proposed by Feigl et al.[74].

(d) Ling[75] has reported that traps were generated after the MOS transistor was irradiated with 4.9 eV photon and demonstrated the generation of traps at Si/SiO_2 interface of the MOS transistor and proposed the UV-induced breaking of Si-H bonds and the formation of the silicon trivalent ($\bullet Si \equiv Si_3$) defects. The interface traps creation after UV irradiation was also reported by L. Zhong et al.[76] recently. This finding was discussed with the model of the hot-electrons induced hydrogen redistribution in which about 2 eV energy was necessary for the electrons in the oxide conduction band to liberate a trapped hydrogen atom and generate in turn interface traps.

1.4 Motivation and Objectives

The change of the effective lifetime under repeated UV irradiation was first investigated by Shimura et al.[29-32]. They suggested that UV irradiation could be used to passivate the silicon wafer surface other than using thermal oxidation and chemical passivation methods. Thus, UV passivation technique was incorporated into the new designed laser-microwave photo-conductive decay measurement equipment from SEMITECH Co., Japan. This equipment was bought by S.E.H (M) Sdn. Bhd to study the possibility of UV passivation for their silicon wafers. However, the UV

irradiated lifetime results were different compared to those obtained previously. The S.E.H researchers suspected that it may be due to contamination and thermal oxidation of clean wafers could be the main reasons for the discrepancies between their results and those of Shimura et al.[29-32]. Therefore, this project was initiated to investigate the possible effects.

The present work has two main objectives, namely :

(i) To study the effective minority carrier lifetime of metal contaminated and thermally oxidized silicon wafers under ultra-violet (UV) irradiation.

(ii) To propose a model to explain the change of effective minority carrier lifetime under UV irradiation.

1.5 Outline of This Thesis

This thesis comprises five chapters. Chapter 2 presents relevant background theory on the semiconductor surface properties. Chapter 3 describes the sample preparation and measurement techniques. Chapter 4 reports experimental results for contaminated and thermally oxidized wafers after repeated UV irradiation. The lifetime trends from the model are compared with the acquired data. Chapter 5 presents the conclusion of this project and some suggestions for future work.