CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION ON SILICON WASTAGE

A large volume of non-hazardous solid waste is generated in many manufacturing plants. The non-hazardous solid waste produced includes scraps and defective products, material removal, spent manufacturing supplies, trash, used packaging from raw materials and supplies, wastewater treatment sludge and so on. [1] This solid waste must be disposed of safely once it is created. As the amount of non-hazardous solid waste increases, and the space available to put it safely without contaminating the earth decreases, the reliability and affordability in waste disposal is becoming a growing problem faced by the industries. The opportunities to reduce solid waste volume and disposal cost is therefore needed to be seriously considered, which involves the 3Rs, i.e. Reduce, Reuse and Recycle. [2] The approaches taken to reduce material wastage will not only resolve the environmental problems created by the waste, but also will reduce the manufacturing cost and generate maximum profit as well.

In a silicon wafer manufacturing plant, the material wastage which also refers to silicon wastage can be grouped into three major categories, i.e. performance losses, removal and kerf loss. Performance losses refers to the scraps and rejects from the wafer manufacturing processes on surface damages, thickness and flatness fallout, surface contamination, etc. Removal losses refers to the material losses due to removal in the mechanical and chemical shaping process such as lapping, etching and polishing. Kerf loss refers to the material loss in slicing process due to the

thickness of the blade. Although the major proportion of the silicon wastage is contributed by kerf loss and material removal, it is difficult to be avoided or reduced due to the nature of wafering process. Reduction of the performance losses has therefore become the main focus in the industry in order to maximize the yield. A typical table describing the magnitude of these losses is given in Figure 1.1.

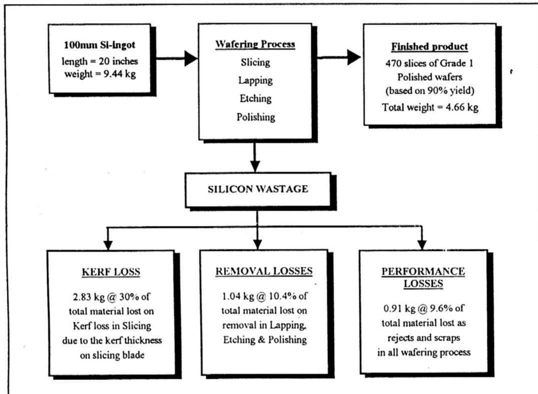

Figure 1.1 An overview on silicon wastage in the wafering processes. (Numerical figures are typical number)

From a manufacturing point of view, performance losses refers to the silicon wastage which is equivalent to yield loss that can be directly converted into dollars and cents. In order to generate maximum profit, the yield losses need to be reduced drastically to reach the ceiling of 100% yield. Assuming a wafer manufacturing plant which produces 5,000,000 of 100mm wafers runs with 90% yield annually. In other words, the plant is losing 10% of the material on performance losses. If the selling price of 100mm wafer is US$15 per wafer, the revenue of the plant could be increased

by US$3.75 million per year with an additional 5% on yield improvement. As profit is depending on selling price and manufacturing cost, it can be increased by reducing the manufacturing cost without changing the selling price. In today's market condition, minimized yield losses has become a requirement for the competitive survival of the manufacturing industry. Companies that did not adopt a focus on competitive price, product quality and customer service will suffer a loss in the market share. [3]

1.2 SILICON WAFER TECHNOLOGY IN MEMC KL

The main steps of converting silicon ingots into grade 1[1] polished wafers in MEMC KL are including Slicing, Edge Profiling, Lapping, Etching, Annealing, Polishing, Cleaning and Inspection. A simplified process flow chart for silicon wafer technology in MEMC KL is shown in Figure 1.2. Crystal Pulling and Epitaxial process is not included in the list as the plant is not equipped with the relevant facilities for these two processes.

The entire manufacturing operations in this plant are divided into three major areas, i.e. Modifications, Polishing, and Clean Room. Modifications processes begins with slicing up to annealing which produces Grade 1 etched wafers. Polishing is the area where etched wafers are polished into mirror finished surface. The polished wafers are finally cleaned and inspected in the Clean Room for all required specifications before shipped to the customer. Each of these processes will be further described in the following sections.

[1] Grade 1 wafers refer to the slices which have been evaluated and accepted based on the quality and specifications requirement by customer or the particular process.

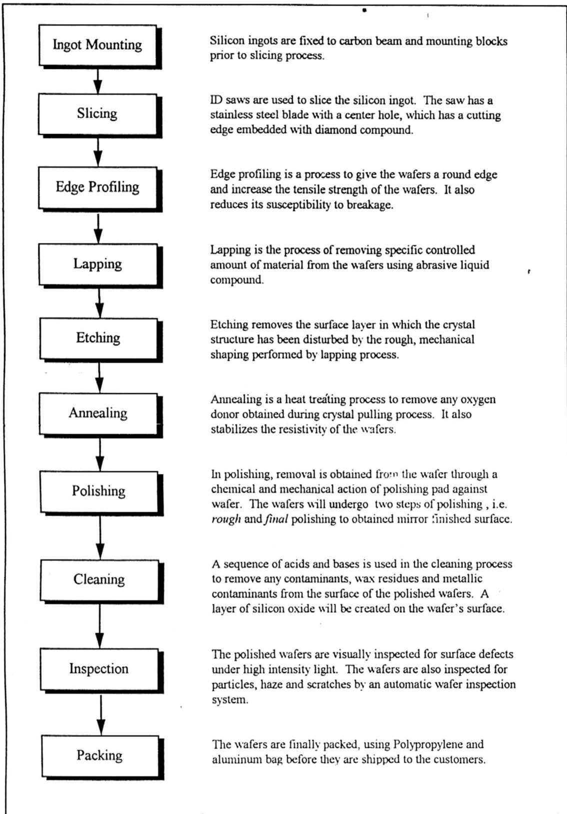

Figure 1.2 Simplified process flow chart of silicon wafer technology in MEMC KL

1.2.1 Slicing

Slicing is the process which slices silicon ingots into wafers by a slicing machine (saw) with a vertical moving wheelhead. The wheelhead is a dish shaped drum mounted with an ID (Inner Diameter) saw blade stretched over it. The cutting edge of the blade is formed with diamond grids which act as the cutting element in slicing operation. [4]

The silicon ingot which has been mounted on a carbon beam with epoxy adhesive is placed into the billet box of the saw. Before the slicing operation begins, the ingot orientation is adjusted according to the cutting plane, based on the X-ray measurement on the first cut (slug) of the ingot. X-ray orientation serves to ensure that cuts are made on the correct crystal orientation. Most (100) oriented ingots are cut parallel to the (100) plane. (111) oriented crystals can either be sliced on orientation, or 3 to 5 degrees off orientation towards (110). The later choice is made when an epitaxial silicon layer will be grown on the wafer in order to improve the growth kinetic of the layer. [5]

Figure 1.3 shows a schematic diagram of the slicing operation. The ingot is extended into the wheelhead through the hole of the blade. The wheelhead which is rotating at several thousand RPM will gradually descends at a rate of 1 to 3 inches per minute and cuts through the ingot and epoxy into the carbon beam, and retracts after the cut is completed. Indexing equipment allows the setting of wafer thickness. The following cut is continued as the ingot is indexed with a distance which is equaled to the specified wafer thickness plus the kerf (thickness of the blade diamond). If the blade does not cut true, either bow or taper can be introduced into the slice as shown in the figure. The wafers are usually removed in packs (5 to 10 slices per pack), each slice is individually separated and placed into the wafer cassettes, waiting for the next process.

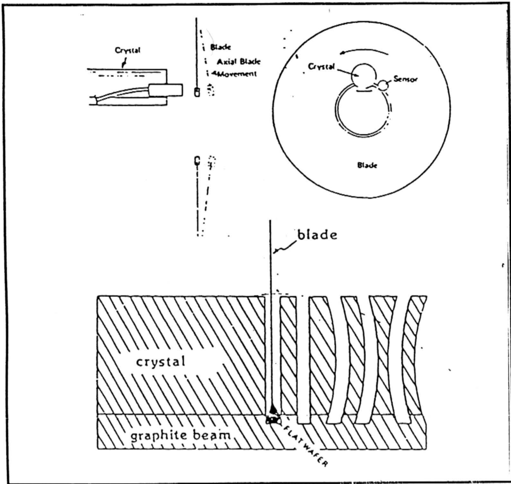

Figure 1.3 Schematic of slicing operation [5]

1.2.2 Edge Profiling

The purpose of Edge Profiling is to increase the physical strength of the wafers and to improve the wafers processability by the rounding of the wafer edge. Edge Profiling is done by an Edge Profiler which profiles the wafer to a tight diameter tolerance. It uses different cams or templates to determine the shape of the finished wafers, based on customer specifications. The entire process is designed to be fully automated, as the operator is only required to load and unload cassettes of wafers. [6]

There are two types of grindwheel used in the Edge Profiler to produce different edge contours, i.e. the SEMI[2] edge contour and the flat edge contour. The multi-grooved grindwheel (R-Wheel) is always used to produce wafers with round edge contour. A wide-grooved grindwheel (T-Wheel) is used to produce the flat edge contour. Coolant is applied to the contact point between the wafer and the grindwheel to lower the temperature generated as the grindwheel is rotating in a very high speed during profiling operation. Figure 1.4 shows the schematic of edge profiling process. After completing the profiling process, the wafers will be cleaned by a Rinser Dryer (rinsed and dried) to remove the silicon sludge and dusts remains on the wafers. The cleaned wafers will be sent to the Lapping process.

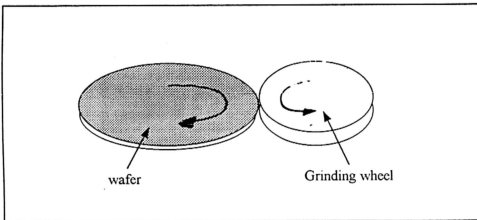

Figure 1.4 Schematic of edge profiling process [7]

1.2.3 Lapping

Lapping is the removal of controlled amounts of material from the silicon wafers to a target thickness, by using a lapping machine (Lapper) together with a lapping compound or slurry. Lapper is a precision machine for producing very flat wafers. The machine consists of two lapping

[2] SEMI is the abbreviation for Semiconductor Equipment and Materials Institute, a trade organization of suppliers to the IC (Integrated Circuit) industry.

plates, i.e. top and bottom plates which rotates in an opposite direction during lapping process. [8] The schematic of lapping process is illustrated in Figure 1.5.

The lapping set up is started by pouring lapping slurry on the entire surface of the bottom plate, and then place the lapping carriers on the plate and position the wafers into the carriers' opening. The top plate is then descent gradually and positioned over the bottom plate, where both plates will start to rotate. Additional slurry is continuously fed between the two plates via the holes in the top plate. When the preset thickness is achieved, the electronic thickness control system will stop the cycle. The top plate is then automatically ascent to its original position, and the lapped wafers are removed from the plate and cleaned in a de-ionized (DI) water bath. Prior to the subsequent processing, two samples from each batch of the wafers will be cleaned, dried and measured for thickness deviation. Based on the deviation, compensation for the plate wear is made on the electronic thickness control system.

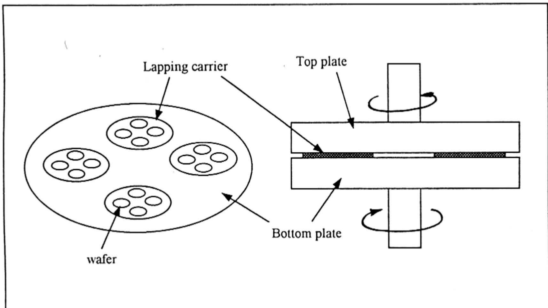

Figure 1.5 Schematic of lapping process

1.2.4 Etching

After Lapping, the cleaned wafers are chemically etched in the Etching Station. The primary purpose of Etching process is to remove the surface layers on the wafers where the crystal lattice has been disturbed by the preceding rough mechanical shaping operations such as Slicing and Lapping. If the damage is not removed, it will cause serious degradation of the bulk crystal structure in the subsequent annealing process.

A mixture of concentrated nitric acid, hydrofluoric acid and acetic acid is used in the Etching process. The nitric acid and hydrofluoric acid enter into the etching reaction directly while the acetic acid is added as a diluent which slows down the reaction rate but improves the etched surface appearance and smoothness. [9]

Etching process also helps in reducing the mechanical distortion of the wafers caused by the difference in damage induced stress on the two surfaces of the wafers. Beside that, the edge smoothness of the wafers will also be improved. The cleanliness, cleanability and the strength of the wafers are very much better after Etching process as the elimination of surface cracks which can harbor debris and serve as stress concentration points.

1.2.5 Annealing

Annealing is a heat treating process for the etched wafers before Polishing. The purpose of annealing is to eliminate the Oxygen donor effect caused by SiOx bonds. The elimination of Oxygen donor enhances structural strength of the wafers and also stabilize the electrical resistivity of the wafers.

The temperature for annealing process is set at approximately 650°C, and the heating time for the wafers is around 20 minutes. Upon the completion of annealing, the wafers are rapidly cooled down to less than 100°C in a short period, so that the resistivity of the wafers can be stabilized. It is very important not to introduce any contamination especially metallics contamination during annealing operation, as it will cause serious degradation in wafer lifetime. To avoid or reduce contamination, the etched wafers are precleaned before they are processed in the Heat Treater. [10]

1.2.6 Polishing

Polishing is the process to produce mirror finished surface on the wafers with very good flatness parameters by fine removal on the wafers. Haze and scratches on the wafers will also be removed in Polishing process. All these parameters on surface finishing are important as they are essential in device fabrications.

Polishing process is carried out in two stages, i.e. rough polishing and fine polishing. Etched wafers fed to Polishing are mounted on polishing blocks with a thin wax layer. The wax layer is controlled to a preset thickness by using a special equipment for wax mounting. Blocks with mounted wafers are then transported to the Polisher via conveyors. [11] The mounted blocks are loaded onto the Rough Polisher for rough polishing, and then followed by fine polishing on the Final Polisher, which will provide a fine removal on the wafers to the target thickness. After fine polishing, the blocks from Final Polishers are rinsed and sent for demounting via the return conveyors. The polishing slurry consists of a solution of colloidal silica maintained at a pH of 11 for rough removal and a pH of 9 for final polish. [12]

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The polished wafers are demounted in a special designed station and then loaded into polypropylene cassettes for dewaxing. Dewaxing is necessary as the residual wax at the wafers have to be removed prior the flatness measurement on ADE Microscan and the final cleaning process as the residual wax will affect measurements as well as cleaning performance.

1.2.7 Cleaning And Inspection

Polished wafers have to be cleaned after dewaxing to remove all foreign materials from the surface of the wafers. The cleaning process, which is also called Polished Slice Cleaning is very delicate as any mechanical contact with the surface will result in scratches. As such, an automated robotic transfer system is used in the Polished Slice Cleaning Station to transfer the cassettes of wafers from bath to bath in the cleaning operation. [13] A sequence of acids and bases is used to remove any contaminants, including wax residues, if any, and metallic contaminants in the polishing medium. The cleaning process is assisted by adding hydrogen peroxide to oxidize these materials, and by heating the liquid baths. The basis for chemical cleaning has been established by Kern. [14]

The final bath in chemical cleaning process is usually chosen so that the wafer surface is hydrophilic, or water-loving. This means that the water wets the surface as the wafer is withdrawn from the bath, and can be removed uniformly. A combination of ammonium hydroxide and hydrogen peroxide is an example of such a bath. On the other hand, a wafer withdrawn from a hydrofluoric acid bath will be hydrophobic, and water will bead on its surface. This beading can lead to spots on the surface after the water dries. The difference between a hydrophilic and hydrophobic surface consists of the difference in the native oxide thickness. Silicon will instantly grow a thin oxide upon emerging from a chemical bath. This can lead to variations in the thickness

of a subsequent thermal oxide layer. This variation is important for thin gate-oxide-layer growth in MOS device fabrication.

The final polished wafers are evaluated for a variety of parameters including physical dimensions, electrical resistivity, flatness, and surface perfection. The polished wafer surface is inspected on a 100% inspection plan, while backside surface is inspected in random basis. The inspection is very important as it serves as a manufacturing feedback tool, concentrating on maintaining highest yields and assuring the best customer quality. After final inspection, the wafers are packaged in Class 100 clean rooms in such a fashion that the cleanliness will be maintained until used by the customer.

1.3 TYPICAL DEFECTS IN WAFER MANUFACTURING PROCESSES

Like many other manufacturing operations, there will be always some scraps or defective wafers in the wafer manufacturing processes. Those defects are usually due to factors like process imperfection, machine malfunction, poor quality supplies, improper handling, human error, etc. The typical defects found on silicon wafers are described in the following sections.

1.3.1 Process-Induced Defects

1.3.1.1 Oxidation-Induced Stacking Faults

Stacking faults are excess silicon atoms that coalesce to form a "platelet" which lies between two adjacent (111) planes. Because the platelet or stacking fault fits between planes, the surrounding lattice is strained. After a certain strain is reached, the lattice will rupture, producing a dislocation loop which bounds the fault. Heat treatment such as oxidation can cause the nucleation and

growth of stacking fault. [15] They are normally electrical inactive, but can serve as diffusion pipes [16] and are generally undesirable near the wafer surface where the active device regions are located. The defects are produced in silicon in quantities which depend on crystal growth conditions, oxygen level, and electrical dopant (boron or phosphorus). [17] Figure 1.6 shows the strong variation in stacking fault density and oxygen level as a function of crystal position in boron doped silicon.

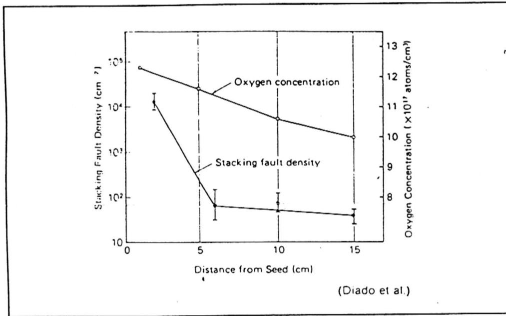

Figure 1.6 : Stacking fault concentration as a function of wafer position in the ingot. Faults are seen after an oxidation procedure. Oxygen level is also shown. [17]

1.3.1.2 Saucer Pits

Certain defects are seen on the silicon wafer surface after oxidation, oxide removal, and defect etching. [18] These are termed saucer pits or shallow pits due to their smooth and featureless appearance. Their appearance is associated with epi stacking faults, if an epitaxial layer is subsequently grown. In addition, most capacitors built on regions of high saucer pit density will show undesirably low minority carrier lifetimes. [19] Recent experiments have determined the

presence of fast diffusing metallic impurities as the source of these defects. [20] Their elimination is accomplished by a variety of "gettering" techniques, including backside abrasion or polysilicon deposition. Besides that, oxygen precipitation in the bulk of the wafer can constitute an "internal gettering" mechanism which also prevents the formation of shallow pit defects.

1.3.2 Slicing Defects

1.3.2.1 Chip (Surface Chip, Exit Chip, Indent Chip)

Surface chip is an area where a flake of material is missing from the surface of a wafer. Exit chip is a rugged edge at the exit end of the wafer. Viewed only on one side of the wafer, often caused by saw blade not exiting properly. Indent chip is a chip that extends through the wafer, often appears to be another flat. [21]

1.3.2.2 Saw Mark (Exit Saw Mark, Rubbing Saw Mark, Tiger Teeth)

Exit saw mark is a pattern of heavy scratch marks on the exit end of the wafer, usually several in series, following the same direction. Rubbing saw mark is a shiny, burnished area that can appear anywhere on the wafer surface. Tiger teeth is a very small v-shape indents or fine lines that extends from the edge of the wafers to the surface of the wafer. [21]

1.3.2.3 Thickness Rejects

Thickness rejects refer to wafers which are sliced too thin or too thick compared to the target thickness. In other words, the thickness of those wafers have thickness fallout of the thickness range required by customer specifications.

1.3.3 Edge Profiling Defects

1.3.3.1 Nick Mark

Nick mark is a slightly flattened arc of edge profiling on the round part of the wafer. This could be caused by the grindwheel approaching the wafer with too much force at the beginning of grinding or by the grindwheel staying in place for too long before leaving the wafer at the end of grinding. [21]

1.3.3.2 Bad Grind (One Sided Grind, Uneven Grind, Not Fully Grind)

One sided grind refers to the wafers that have unequal edge profiles on both sides, one side is grounded more than the other side on the wafer. Uneven grind refers to wafers that have deeper edge grinding on the surface than the other. Not fully grind refers to the ungrounded portion on the edge of the wafer which is not touched by the grind wheel anywhere along 360° of the slice circumference. [21]

1.3.3.3 Dings

Dings are the tiny shiny chips on the grounded edge of the wafers, which could be caused by insufficient grindwheel pressure, excessive chuck speed or improper water adjustment which makes the grindwheel skip around the edge of the wafer. [21]

1.3.4 Lapping Defects

1.3.4.1 Lapping Scratches

Lapping scratches is an abnormality on the surface of lapped wafers as a result of indentation caused by a sharp lapping plate edge or the groove. This could be a long arc type or a short one.

Contamination of harder particles in the lapping slurry or those embedded on the plate could also cause indentation. The scratches are more visible after etching process. [22]

1.3.4.1 Fractures

Fracture is defined as a crack, fissure, crowsfoot, probe damage or cleavage that extends to the surface of the slice. It may or may not extend through the entire thickness of the slice. A fracture will migrate during processing and eventually will break the slice. Fractures are usually caused by improper handling of slices.

1.3.5 Etching Defects

1.3.5.1 Bad Etch

It is a result of chemical reaction over the surface of the wafer in the etching process. It give an appearance of different gloss across the surface. Due to non optimum interaction between the wafer rotation and the acid recirculation. Inspection can be done visually under bright light. [23]

1.3.5.2 Dull Center

It is almost similar to "Bad Etch", however the low gloss area is located toward the center of the wafer. It occurs when the rotation speed is higher than the optimum condition. [23]

1.3.5.3 Roller Mark

It is a mark of partial circle at the edge of the wafer which is located at the roller position. It occurs as a result of the non consistent rotation speed, or the intermittent stoppage of the rotation. The mark is visible under bright light. [23]

1.3.5.4 White Stain

Wafers after lapping process are cold and contain soiled lapping slurry, a suspension agent and DI water. Immediately after unloading from the lapping plate, a relative drying of this soil may occur, which will leave some spots difficult to clear at the ultrasonic cleaning. Upon etching process, the chemical reaction could leave these spots as a white spotted stain. In the event of rough handling, it would appear as a white streak. [23]

1.3.6 Polishing Defects

1.3.6.1 Polishing Scratches (Arced Scratches, Straight Scratches, Irregular Scratches)

Arced Scratches are scratches in uniform and curved shape. It may be deep in the polished surface or shallow. The deep ones are bright white, easily visible and may appear perforated. Shallow scratches is fine, white-blue and seems to flicker in and out of view during rotation. *Straight Scratches* are scratches with fine, smooth, bright white or light blue line longer than one-half inch in length. It may be visible in only one or two positions during rotation. *Irregular Scratches* are the bright white or light blue scratches having various shapes or lengths. It has no pattern, and often made of tiny scratches perpendicular to the main direction of scratch. It is usually visible all the way around and caused by non-uniform impact. It is also called "handling scratches". [24]

1.3.6.2 Dimple

Dimple is a smooth and shallow depression on polished surface of a wafer. It can be seen by using slice as a mirror to focus on fixed fluorescent light source. A dimple distorts the reflection, making it appear to bulge or swell. [24]

1.3.6.3 Streaks

Streaks is defined as white gray or light blue dull film which appears fused to surface. It may form straight trail across slice or smoke-like swirls. [24]

1.3.6.4 Syton Spots

Syton Spots are the small droplets or rings on surface of the wafers. Under fluorescent light, the rings have fine, distinct edges. Under bright light the rings may appear to have etched or dull center. [24]

1.3.7 Light Point Defects (LPD)

1.3.7.1 Particles

Particles are the distinct bright white pinpoints which may be clustered or randomly scattered over the surface of the wafers. Large particles appear above slice surface, glow, and are visible throughout entire rotation. Smaller particles are not as bright and may disappear as the wafer rotates. It is not always visible and too numerous to count. It is detected by the Wafer Inspection System (ESTEK CR80). The particles may be dust, fibers, or lint. [25]

1.3.7.2 Haze

Haze is the white blue or gray cloudiness which dulls the reflective surface. It make the wafers do not look "deep". The intensity of haze may vary across the surface of the wafers, or vary from wafer to wafer. Heavy haze has a "milky" finish. [25]

1.3.7.3 Microscratches

Microscratches is defined as very fine white to pale blue concentric scratches. The scratches may form complete circles or may be incomplete, affecting only part of the wafer. Microscratches is not visible and it can only be detected by Wafer Inspection System (ESTEK CR80). [25]

1.3.8 Flatness Defects

Flatness defects refer to the wafers which fail in any one of the flatness parameters as compared with the customer specifications. There are five major parameters on wafer flatness, i.e. Bow, Warp, Total Thickness Variation (TTV), Total Indicated Readout (TIR) and Site Total Thickness Indicated Readout (STIR). Bow and Warp are the flatness parameters on Slicing process which depend upon the slicing blade deviation. TTV, TIR and STIR are the flatness parameters on lapping, etching and polishing process. These parameters will be improved from the early process to the later process due to finer removal on the wafers. For example, TTV obtained after Polishing is much better than lapped and etched TTV.

1.3.9 Metallic Contamination

Metallic contamination refers to metallic impurities which are deposited on silicon wafer surfaces from various wafering process such as lapping, etching, annealing, polishing and cleaning. According to the French researchers at LETI, the metallic contamination was due to three different mechanism, i.e. physisorption, chemisorption and metal displacement. [26]

The researchers said that physisorption is due to van der Waals interactions that take place when metallic impurities are in solid form in the solution, such as iron III in neutral or alkaline medium. These depositions are identical to particle depositions. On the other hand, chemisorption results from electrons shared between the substrate and impurities. As an example, aluminate deposition in neutral or alkaline medium can be explained by a chemisorption effect. Metal displacement is similar to chemisorption, but instead of electrons shared between the substrate and impurities, an electronic transfer is involved. These three mechanism can be distinguished from one another by the way the impurities bond to the substrates. [27]

1.4 SOME SCHEMATICS OF VARIOUS DEFECTS ON SILICON WAFERS

The schematics and appearance of some defects on silicon wafers mentioned in the previous section are shown in this section. These defects are the most commonly seen in the production floor in MEMC KL, where they are not tolerated in high precision device fabrication.

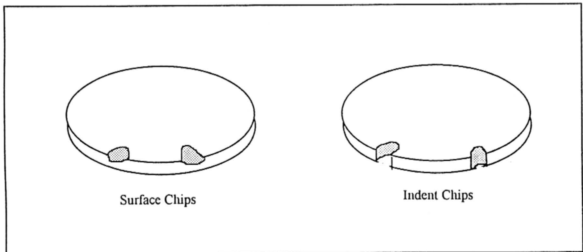

Figure 1.7 : Schematics on typical surface defects on silicon wafers

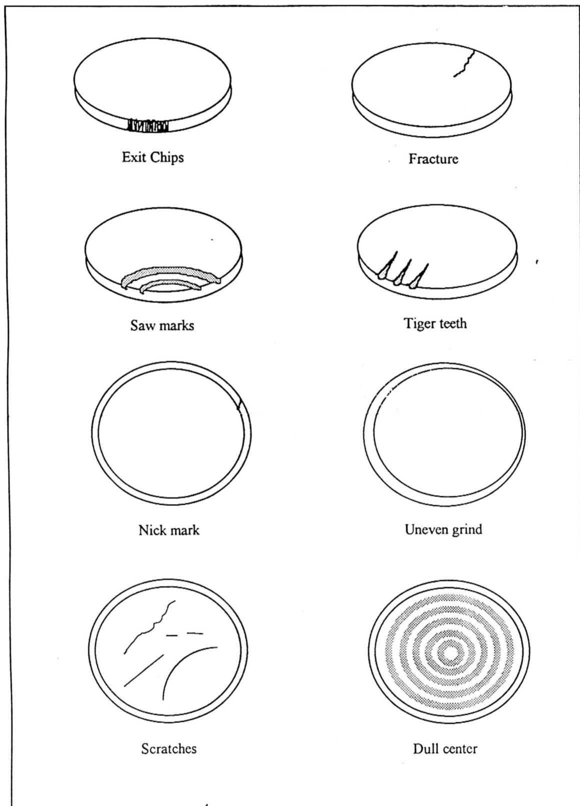

Figure 1.7 : Schematics on typical surface defects on silicon wafers (continued)

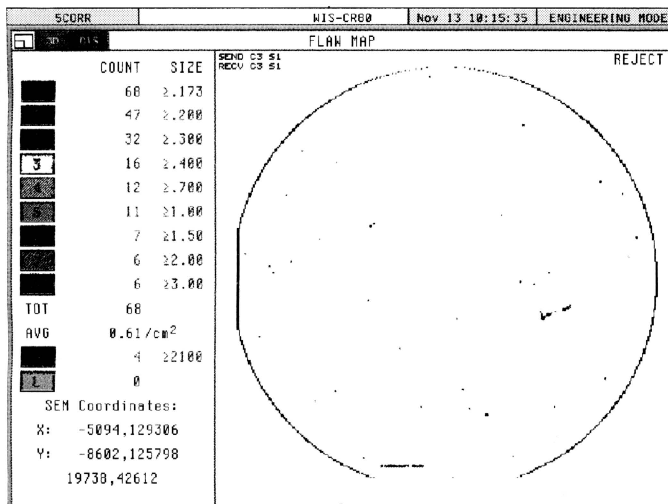

Figure 1.8 : Particle mapping on a reject wafer by ESTEK CR80

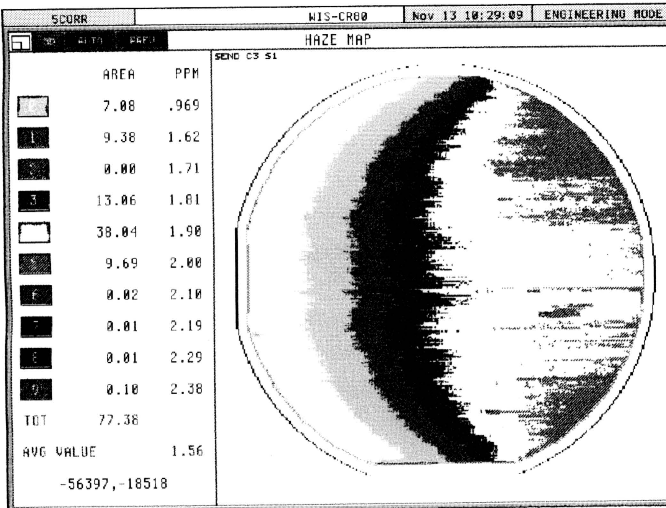

Figure 1.9 : Haze mapping on a reject wafer by ESTEK CR80