# CHAPTER 2

# EXPERIMENTAL TECHNIQUES

## 2.1 INTRODUCTION

There are a large number of techniques available today that have evolved within the industry to meet measurement demands for composition, impurities, structure, physical defects and electrical anomalies. A summary of some characterization techniques is shown in Table 2.1. These techniques play an important role in the growth and development of the semiconductor industry. They not only provide timely failure analysis data for resolution of manufacturing problems, but also continue to stimulate the development of small spot probes, ultra-sensitive impurity detection schemes, and high speed electrical measurements. [28]

In this project, the experimental techniques on defects analysis in wafer manufacturing processes are divided into 4 different sections. The first section starts with the data analysis based on the fourth quarter of 1995 production summary for MEMC KL. Basically this section is a statistical study on the performance of wafer manufacturing processes in MEMC KL, which covers the manufacturing yield performance, the pareto analysis on different types of defects, and the amount of silicon wastage produced at various processes.

The second and third sections are the studies on wafer surface parameters by contactless measurement techniques by Microscan ADE8100 and ESTEK CR80 Wafer Inspection System (WIS) respectively. Microscan uses the principle of Capacitance and Eddy current in measuring

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| Method | Parameter Determined |
|---|---|
| **ELECTRICAL** | |
| Eddy current | Sheet resistance, metal thickness, carrier lifetime |
| Microwave reflection | Minority carrier lifetime |
| Capacitance | Wafer flatness |
| Surface charge analyzer | Interface state density, surface contamination |
| Surface photovoltage | Diffusion length, surface recombination velocity |
| Corona charging | Lifetime, diffusion length, flatband voltage |
| **OPTICAL** | |
| Optical microscopy | Surface topography |
| Ellipsometry | Layer thickness, refractive index, layer growth |
| Photoluminescence | Doping/impurity density, energy levels |
| Transmittance (FTIR) | Impurity density, wafer temperature |
| Internal reflection IR spectroscopy | Chemical nature of film, surfaces and interfaces |
| Reflectance | Layer thickness, line width, particle density |
| Raman spectroscopy | Composition, structure, damage, stress |
| **ELECTRON BEAM** | |
| Scanning electron microscopy | Surface topography |
| Voltage contrast | Voltage, voltage transients |
| Auger electron spectroscopy | Elemental surface composition |
| Electron microprobe | Elemental composition, surface/bulk impurities |
| Low/high energy diffraction | Surface crystallography |
| **ION BEAM** | |
| Rutherfod back scattering | Elemental composition, impurity density/type |
| Heavy ion back scattering spectroscopy | Surface impurity density/type |
| **X-RAY, GAMMA RAY** | |
| X-ray fluorescence | Elemental composition, film thickness |
| X-ray photoelectron spectroscopy | Elemental surface composition, chemical species |
| X-ray topography | Crystal defects, stress |
| Neutron activation analysis | Elemental composition, impurity density/type |
| **MISSCELLANEOUS** | |
| Scanning tunneling microscopy | Surface topography on conductors, defects |
| Atomic force microscopy | Surface topography, linewidth, defects |
| Thermal waves | Damage |
| Acoustic microscopy | Defects, voids |

Table 2.1 Summary of some characterization techniques for semiconductor measurements [29]

wafer flatness, thickness and electrical resistivity, while ESTEK CR80 uses light scattering method to measures wafer surface imperfection such as particles, haze and scratches. The final section of the experimental techniques is the study on visual inspection procedures and techniques to evaluate the defects on the wafers which can be visually detected. The wafers are inspected and evaluated for a variety of parameters on customer requirements at different areas and processes as shown in the material flow chart in Figure 2.1. Details on the measurement techniques on Microscan, ESTEK CR80 and visual inspection will be further described in this chapter.

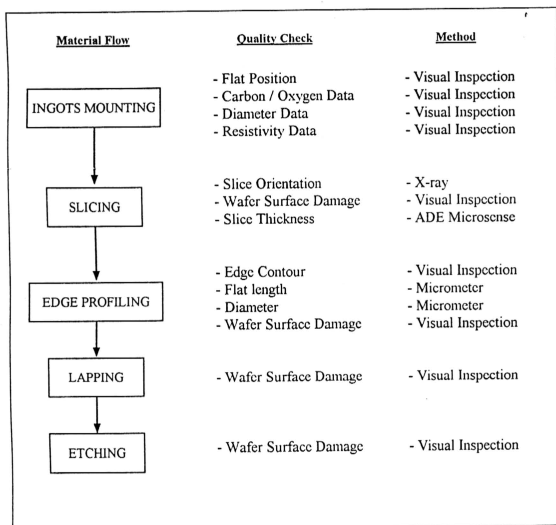


Figure 2.1 Material flow chart of MEMC KL [30]

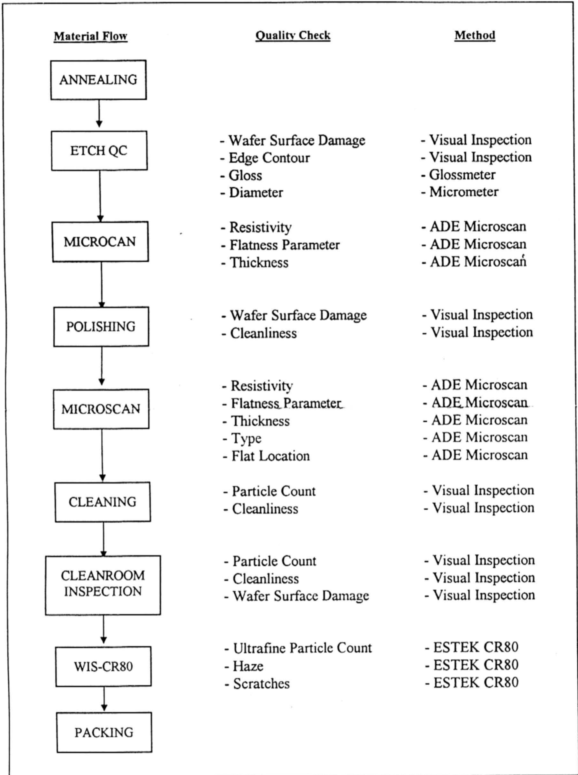


Figure 2.1 Material flow chart of MEMC KL (continued)

## 2.2 MEASUREMENT TECHNIQUES BY MICROSCAN ADE8100

### 2.2.1 Functional Description Of Microscan ADE8100

Microscan ADE8100 wafer measurement system is capable of capturing data on a variety of parameters over the surface of a silicon wafer using ADE's patented noncontact capacitive probe technology. Measurement which may be made describe wafer thickness, flatness, surface deviations over localized areas, semiconductor type, resistivity, bow and warp. The system computer presents measurement data in numerical or graphical form, on the computer screen or on a printer. Data for individual wafer may be plotted in a variety of ways to yield 2D or 3D pictures of the wafer.

The system consists of a system computer, elevators (wafer loading and unloading device), prealigner, and measurement stations as shown in Figure 2.2. The system computer basically controls the movement of the wafers, collects and displays data provided by the measurement stations based on the predefined parameters.

During automatic operation, sender elevators transfer wafers from cassettes to the main transport belt at the start of the measuring process. The prealigner ensures that the wafers are properly positioned for the next station, by centering each wafer on the transport belt and aligning the major fiducial (flat or notch) of each wafer to a pre-determined angular position. The flatness station measures the thickness and flatness of wafers at overlapping points, and the resistivity station determines the bulk resistivity of the wafers. Measurement data are supplied to the system computer for analysis, display, and use in sorting. Receivers transfer the wafers from the transport

belts into cassettes. Each receiver contains wafers of a particular sorting class defined by the operator prior to automatic operation. [31]

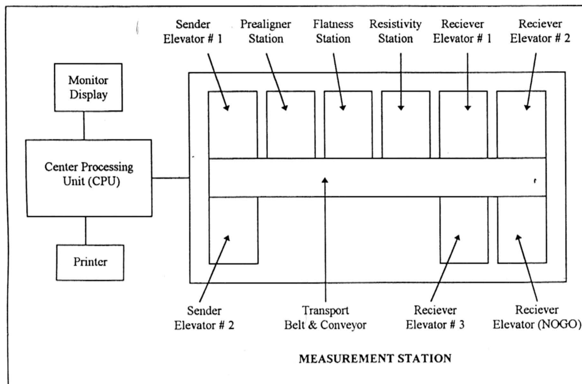


Figure 2.2. Schematic on Microscan ADE8100 wafer measureing system

## 2.2.2 Microscan System Description

### *2.2.2.1 Prealigner Station*

The three principal components of the Prealigner Station are the wafer detecting optoelectronic sensor, the wafer edge sensor, and the station vacuum chuck and its associated drive mechanism. When a wafer is detected in the station by the opto sensor, the positioning procedure may begin. [32] The execution sequence of the Prealigner is shown in Figure 2.3.

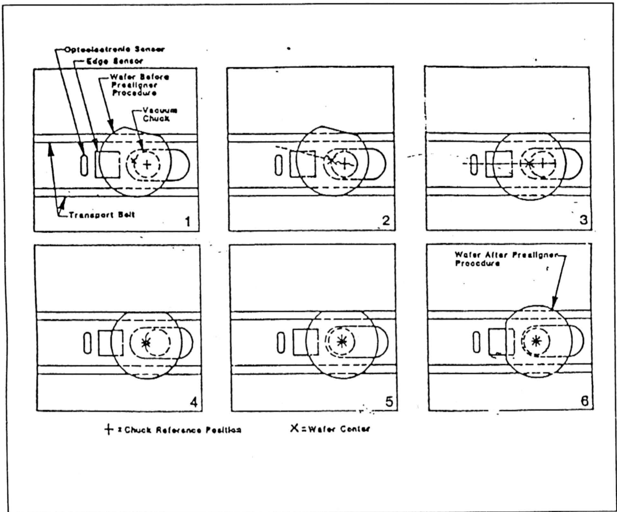


Figure 2.3. Schematic on the execution sequence of the Prealigner

Wafer fiducials are physical markers at certain point along the wafer edge. Fiducials ensure that wafers are properly positioned, and provide information about the crystal structure of the wafers. Wafers generally have one primary fiducial and may have one or more secondary fiducials as well. Primary fiducials may be either flats or notches, while secondary fiducials are assumed to always be flats. Secondary flats are distinguished from primary flats by their shorter length and distance from the wafer edge.

The prealigner puts wafers in a known position before they are advanced by the transport belts to the next station. The Prealigner centers wafers on its vacuum chuck, and positions them rotationally using the primary fiducial as a reference to a fixed angular position. The prealigner also determines the quantity and locations of any secondary flats along the wafer edge. Secondary flat locations are specified by their clockwise angular displacement from the primary fiducial.

When a wafer arrives in the station and is detected by an optoelectronic sensor, a chuck lifts the wafer above the belt. Vacuum suction keeps the wafer in place as it rotates so that the wafer edge passes over the station's sensing area. The edge sensor produces a signal corresponding to the portion of the sensor which the wafer covers. This sensor signal is analyzed, and the amount and direction that the wafer center differs from the chuck position are noted. The computer then rotates the chuck until the wafer's center is between the transport belts. The chuck lowers, moves to the calculated center of the wafer and then picks up the wafer and centers it on the chuck. The chuck holds the wafer again and spins it over the edge sensor to check the centering. The process repeats until the wafer is centered according to the system's specification. The wafer fiducials is ignored in the centering process.

After the wafer is properly centered, the computer rotates it angularly to position the major flat or notch and locate any minor flats. The locations of these secondary flats may be used in sorting wafers. The wafer which is centered and aligned is finally lowered to the transport belt and move to the next station.



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### *2.2.2.2 Flatness Station*

The Flatness station measures wafer thickness and flatness using two non-contact capacitive probes which mounted coaxially above and below the point where the measurement is made. The schematic of Flatness station probe setup is shown in Figure 2.4. Each probe in effect measures the distance between itself and a wafer surface. The signals from these probes and the information received during the station calibration can be used to determine the relative positions of points on a wafer's top and bottom surface. This data is used in calculating values for variety of parameters. The distance between probes is fixed and known in a properly calibrated station. [33]

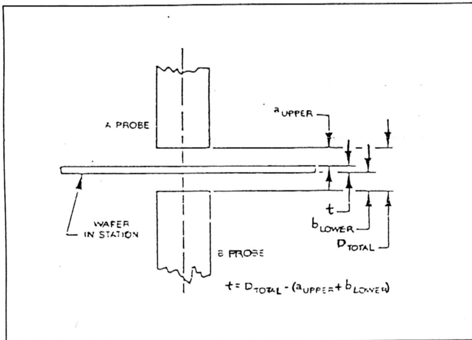


Figure 2.4. Schematic of Flatness station probe setup

When a wafer arrives at the station and is detected by the opto sensor, it is lifted by a vacuum chuck to a point midway between the two probes. The wafer is moved between the probes in a fine scanning pattern, and measurements are taken at hundreds of points on the wafer surface during the period of a few seconds. Measured data is supplied to the system computer for calculation and

display. The number of points examined, the time lapsed and the measurements calculated will depend on the wafer size and the setup selected by the operator. When measurements are completed, the wafer is lowered to the transport belts and advanced to the next station. Figure 2.5 shows the top view of the Flatness station.

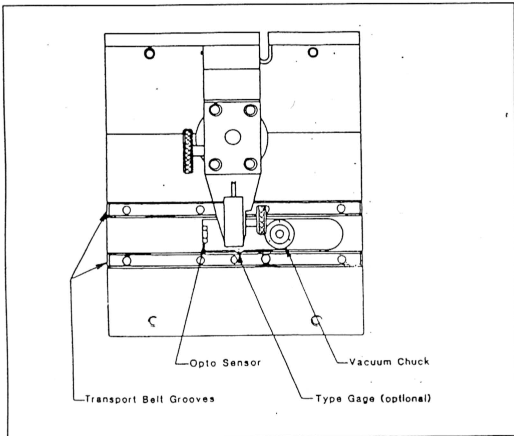


Figure 2.5. Schematic of the top view of the Flatness station

### *2.2.2.3 Resistivity Station*

The Resistivity Station uses the Eddy current principle to measure the bulk resistivity of silicon wafers. [34] The station consists of a transducer mounting assembly with two non contact conductance sensors mounted coaxially above and below the point where measurement is made. Each wafer is placed between the two probes where an oscillating magnetic field induces Eddy

currents in the wafer. The power absorbed is proportional to the material conductance. The wafer's thickness and the conductance measured by the sensors are used to calculate resistivity, by the following equation,

Resistivity = Thickness / Conductance

where resistivity units are in ohm-cm. Resistivity measurements may be made at the wafer's center and to a user selected point on the wafer between the wafer center and the leading edge. Measurement data are supplied to the system computer for calculation and display. There are two types of resistivity gage used for different resistivity ranges, i.e. "High Resistivity" and "Low Resistivity" gage. "High Resistivity" gage measures wafers with resistivity ranges from 0.2 to 199.9 ohm-cm, where as "Low Resistivity" gage measures wafers with resistivity ranges from 0.001 to 0.999 ohm-cm.

### 2.2.3 Thickness/Flatness Station Measurements

Thickness measurements describe the distance between points on the top wafer surface and the points vertically below them on the wafer bottom. Flatness measurements, expressed as "focal plane deviation" (FDP), describe the distance from points on the top wafer surface to a plane fitted to this surface. Focal plane deviation at each point may be either positive (for points above the plane), or negative (for points below the plane). The FDP results are based on a flattened wafer bottom. Measurement results given are for wafers flattened as if by suction, though no suction is actually applied. The schematic of thickness and flatness measurements is shown in Figure 2.6.

The plane fitted to the wafer surface in FPD calculation is defined by one of two methods specified by the operator, i.e. "three point" and "best fit". The "three point" focal plane is defined by three surface points, each 3mm in front the wafer edge. These points, shown in Figure 2.7 are spaced

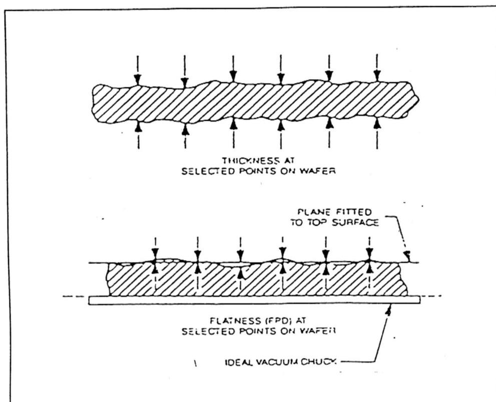


Figure 2.6. Schematic of the thickness and flatness measurements

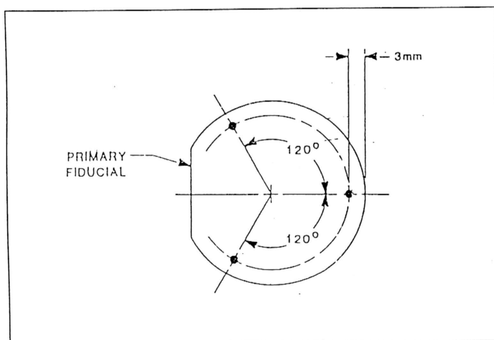


Figure 2.7. Schematic of the "three point" focal plane

120 degrees apart, with one point directly across from the center of the primary fiducial. The "best fit" focal plane is that which yields the lowest sum of the squares of the distances between it and each point on the wafer surface. [35]

Wafers are moved between the flatness station's probes in a fixed pattern while measurements are taken continuously. The portion of the wafer surface examined, known as the Flatness Quality Area (FQA), is specified before measurements are made. The entire specified area is examined, as measurements are made at hundreds of overlapping points. When the FQA is within 4mm of the nominal wafer diameter, the system performs an edge scan to avoid over range conditions.

The wafer surface is divided into two regions for flatness scanning. The wafer is rotated between the probes when measurements of the outer region are being made, and is moved in a back-and-forth pattern when the central region is examined. The size of the central region depends upon the flatness station chuck size. The flatness scanning pattern is illustrated in Figure 2.8.

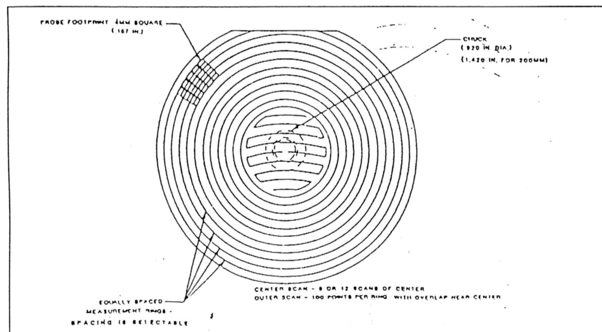


Figure 2.8. Schematic of the flatness scanning pattern

Measurement made over the wafer surface are used to calculate other quantities related to thickness and flatness. Total thickness variation (TTV) represents the difference between the minimum and maximum thickness measured. Total indicator reading (TIR) is the difference between the minimum and maximum focal plane deviations. The percentages of the measured wafer surface within use specified limits for focal plane deviation are calculated as well.

Flatness may also be measured at a local site on the wafer surface, and is expressed as Site Focal Plane Deviation (SFPD) and Site Total Indicator Reading (STIR). Figure 2.9 shows the schematic of site flatness measurement. Local sites are user determined, and may be either square or rectangular. SFPD and STIR measurements indicate the average for all sites on the wafer. Measurement for individual sites may be displayed either in a format providing FPD or TIR values within each site, or providing GO/NOGO status for each site based on user specified limits.

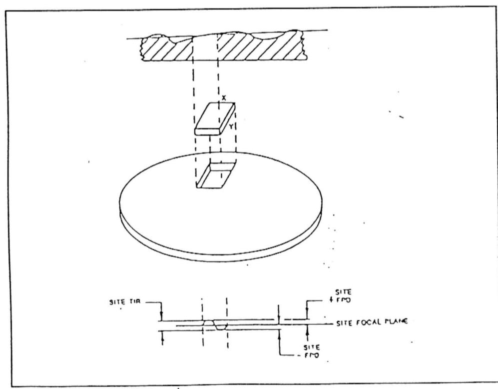


Figure 2.9. Schematic of site flatness measurement

The focal plane used in calculating SFPD and STIR measurements is defined by one of four methods. A single "Frontside Reference Front Focus" focal plane is the same plane used to calculate Global FPD measurements, and may be either "3 point" or "Best Fit" as defined by the operator. The Backside Reference Center Focus plane for each site is that which includes the center of the site and also parallel to the wafer bottom surface. The Frontside Reference Center Focus plane for each site is that which includes the center of the site and also parallel to the Global Frontside plane. The "Site Best Fit" plane for each site is the plane which yields the lowest sum of the squares of the distances between it and each measured point on the site surface. The definition of Site Focal Plane is also shown in Figure 2.10.

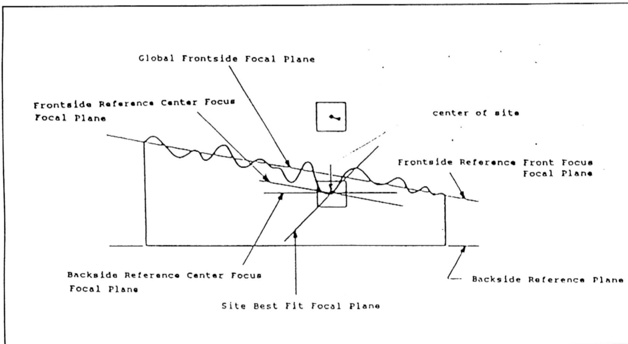


Figure 2.10. Schematic of the site focal plane

Bow and Warp measurements are made in two scans over two fixed regions on the frontside and backside surfaces of the wafer in an unclamped state. The first is the central circular region containing the wafer center and three points on the circle. The wafer is moved back and forth to

measure these points. The second scan is over an outer region extending from the edge of the central region to the edge of the wafer's FQA. The wafer is rotated between the probes to measure the outer region. The edge exclusion of the Bow and Warp scan must be between 3mm and 5mm. The regions of Bow and Warp measurement is shown in Figure 2.11. By measuring points on both the frontside and backside surfaces, the system derives the wafer's median surface, the locus of points equidistant from the frontside and backside surfaces.

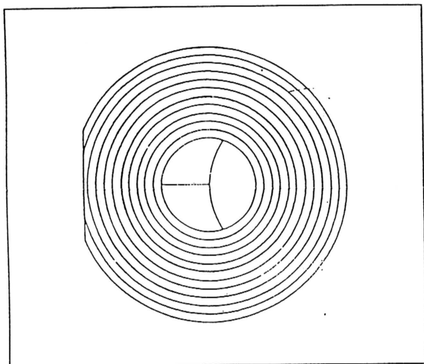

Figure 2.11. Schematic on the regions of Bow and Warp measurement

Bow is a measurement of concave or convex deformation of the median surface at the wafer center, independent of any thickness variation. Bow is calculated by measuring the deviation of the center point of the median surface relative to the median reference plane as shown in Figure 2.12. This reference plane may be calculated based on either 3 point or best fit plane.

Warp is the difference between maximum and minimum deviations of the median surface relative to the backside reference as shown in Figure 2.13. This reference plane may also be calculated based on either 3 point or best fit plane.

Semiconductor type may also be measured in the Flatness station. Two wires rise from below the wafer to make contact with its backside. The wafer type is determined based on the direction of the current which results in the wires.

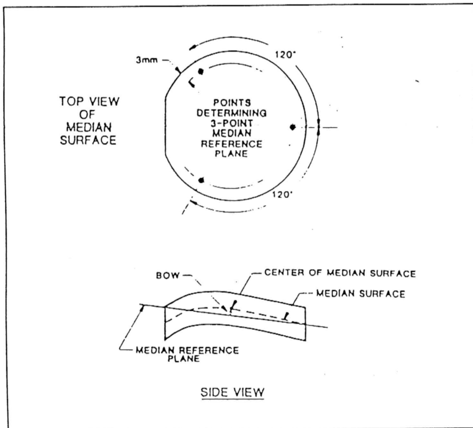


Figure 2.12. Schematic of Bow measurement

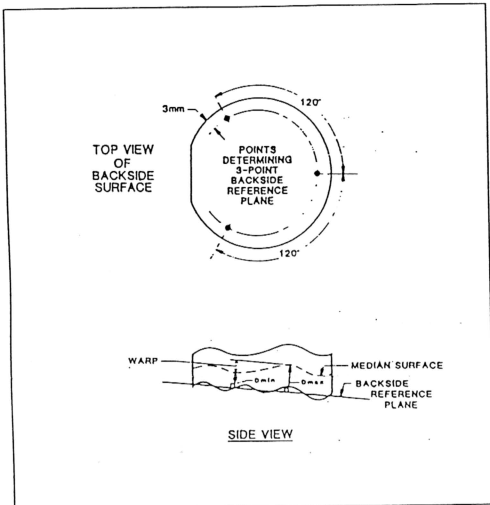


Figure 2.13. Schematic of Warp measurement

## 2.3 MEASUREMENT TECHNIQUES BY ESTEK CR80

### 2.3.1 Functional Description of ESTEK CR80

ESTEK CR80 Wafer Inspection System is a computer-controlled wafer inspection tool. It is used in detecting and measuring the presence, size, and X-Y coordinate location of particles, scratches and haze on non-pattern wafers. The system computer presents measurement data in numerical or graphical form, on the computer screen or on a printer. Data for individual wafers may be plotted in a variety of ways to yield 2D or 3D pictures of the wafer. [36]

The ESTEK CR80 utilizes either a Helium-neon (632.8 nm) or an Argon-ion (488 nm) laser. Differing mechanical methodologies are used to generate a flying spot scan beam with which to inspect the wafer surface. These devices consist of a rotating polygon mirror, a scanning galvanometer and a resonant scanning mirror. The sweeping spot size ranges from 100 microns to as small as 50 microns in diameter. The surface to be inspected is transported perpendicularly through the scan beam, which impinges on the surface at an angle of incidence of 15 degrees. The beam is focused on the wafer surface at location coincident with a foci of the main elliptical mirror collector. This elliptical mirror relays the collected light to the Dark Channel assembly via a second elliptical mirror. One foci of this relay mirror resides at the collection point of the Dark Channel collector assembly. This fiber optic assembly passes the light on into a photomultiplier tube (PMT). A typical setup of CR80 optical system is shown in Figure 2.14.

The light reflected from the wafer surface passes through the exit slit in the primary elliptical collector and into a light trapping assembly. If the system possesses a Light Channel where the reflected signal is gathered and funneled into a second PMT. Currently there are two types of

Light Channel assemblies, i.e. Original Light Channel which uses fiber optics to channel the reflected light into a photomultiplier tube, and Reconvergent Specular Detector which uses mirrors to recreate the laser spot at the aperture of the PMT.

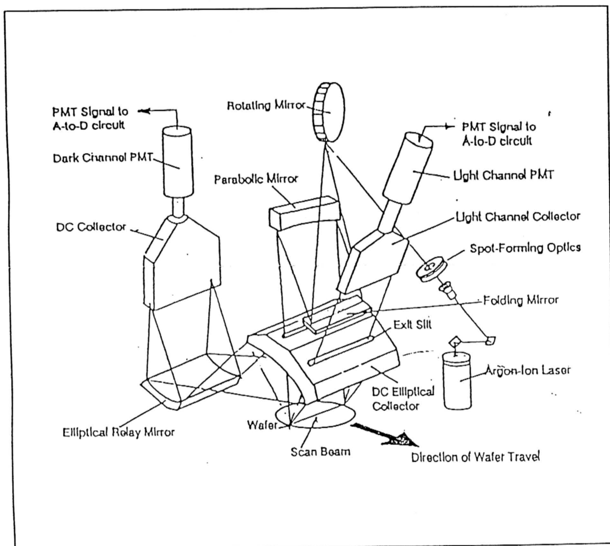


Figure 2.14 : A typical setup of CR80 optical system [37]

The light channel plays an important role in classifying defects. Not all defects scatter light. Some defects like munds, slip, buried particles, and film non-uniformity do not scatter light. In conjunction with the Dark Channel, defect classifications can be made by sorting the various events into bins based on the thresholds or combinations of thresholds which have been exceeded. Figure 2.15 shows the operation block diagram of ESTEK CR80.

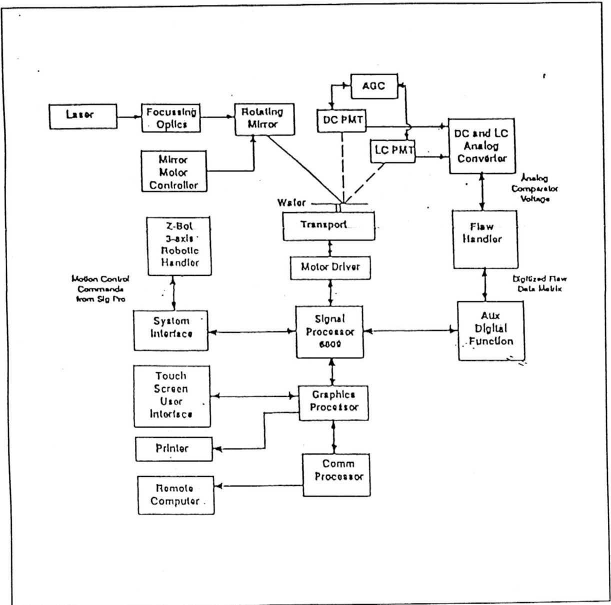


Figure 2.15. Schematic of the operation block diagram of ESTEK CR80.

### 2.3.1.1 Dark Channel Theory

Light collected by the Dark Channel photo multiplier is an analog signal whose amplitude is proportional to the amount of light collected from the surface of the sample. The total intensity collected is the summation of all the individual components of scatter generated from the sample surface. The components in the total signal include scatter from micro roughness (haze), pits, subsurface defects and particles. The output analog signal from the photo multiplier tube (PMT) is digitized by an Analog-to-Digital converter. An 8 bit code called the Analog-to-Digital value, representing the amplitude of the analog signal is generated. [38] Figure 2.16 shows the schematic of Light collection by the Dark Channel PMT.

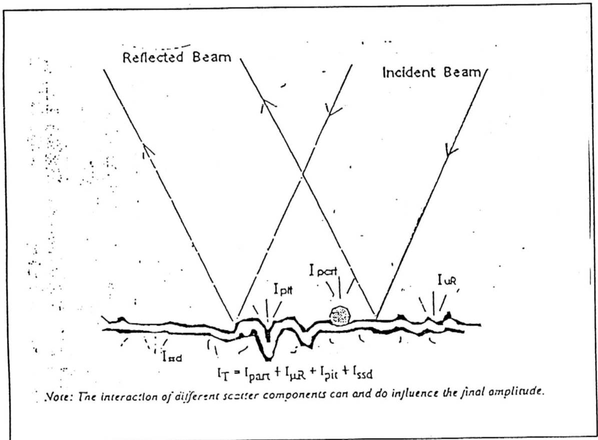


Figure 2.16. Schematic of Light collection by the Dark Channel PMT

*2.3.1.2 Light Channel Theory*

Light Channel detection, also known as Distortion defect detection, utilizes laser light that is directly reflected from the surface of the sample into the Light Channel photo multiplier tube. If the surface of a sample is perfect, on light will be deflected away from the PMT as a constant voltage is maintained. When the laser moves across the sample and encounter a light channel defect, a specular distortion of light will occur and consequently deflect some portion of the light away from the detector. This loss of light is translated into a loss of signal voltage by the PMT and thus a detection is triggered. The analog output from the photo multiplier tube is digitized by an Analog-to-Digital converter. A code is generated which classifies that event as a Light Channel defect. [39] The schematic of the distortion defect detection by the Light Channel PMT is shown in Figure 2.17.

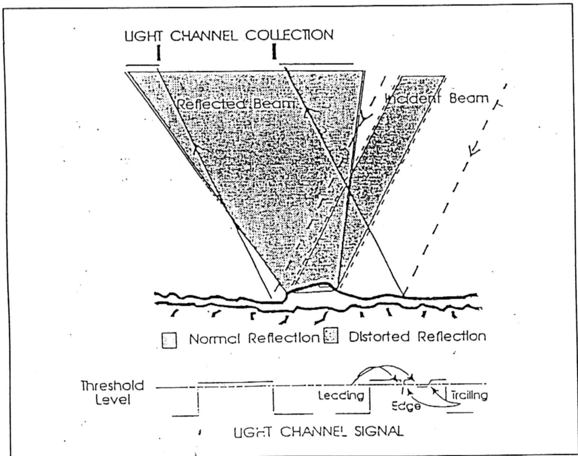


Figure 2.17. Schematic of the distortion defect detection by the Light Channel PMT

### 2.3.2 Measurement Procedures On Particles, Scratches and Haze

#### *2.3.2.1 Particle Measurement*

The sample is moved at a constant speed under the laser beam. Particle events on the sample surface scatter light which is collected by the dark channel filter optic collector and the photo multiplier tube. The output from the photo multiplier tube assembly preamplifier board is sent to the VME card cage where the analog signals are digitized. The digitized signals enter the Array Processor board with the event magnitude and X-Y coordinates. The resulting output is an analytical flaw map with X and Y event positional information and correct event sizing. [40]

The X positional information is related to the spot velocity and the laser spot size on the wafer. Spot velocity refers to the speed with which the rotating polygon mirror moves. The scattering events are collected during this linear scan. The spot velocity is held at a fixed speed resulting in a constant time per unit distance data interval. The ability to know where the laser beam is on the wafer relative to time in the X direction is crucial. Without this knowledge accurate event placement on an event map will be useless. Another important aspect of the X positional information is the laser spot size. The spot size improves event detection of two particle events occurring in close proximity to each other. Figure 2.18 below shows an output of the laser spot size versus the particle resolution.

The Y positional information is related to the optical stage velocity. The smaller the change in Y per unit of distance the more accurate the coordinates can be. Similar to X, the knowledge of laser spot position is crucial to accurate particle locations. The X and Y resolution and position accuracy provide linear parameters for the analytical examination of a flaw map.

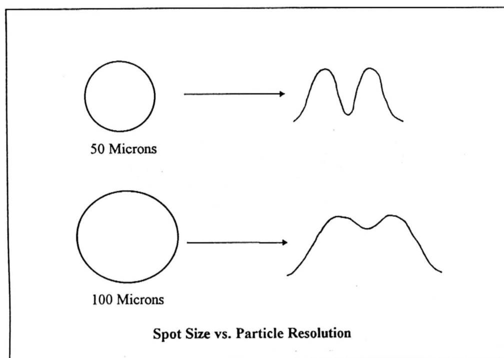


Figure 2.18. Schematic of the laser spot size versus the particle resolution

*2.3.2.2 Scratches Measurement*

There are two computation methods used in detecting scratches as they are difficult to be extracted directly from a processed image due to some interruption from noise and interference. First, the strength of scratch is computed by using the scattered light information to find directional amplitude differences relative to their surrounding area. Secondly, the area of the scratch is calculated and the number of scratches is counted.

The structures of scratch in the flaw image are very similar to a line structures. A line detection algorithm is used to compute the scratch strength. A set of templates is used to detect scratch structures in the image. These templates take advantage of the uniform response of the scratch widths.



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A unique label is assigned to each scratch in order to calculate the properties of the scratch. A connected component labeling algorithm is employed. Consider a binary flaw image 420 x 420 microns, where 0-labeled and 1-labeled pixels are assumed to be the background and foreground of the flaw respectively. [41] Connected component labeling is a process which transforms such a binary flaw map into a symbolic map in which the pixels are labeled according to the maximum connected component to which they belong.

A maximum connected region or component is a set of 1-labeled pixels such that for any two pixels in that set, a sequence of 4 or 8 connected 1-labeled pixels whose first and last pixels correspond to these two pixels can always be found. Two neighboring pixels are 4-connected if they are to the north, south, east, and west of each other. Two neighboring pixels are 8-connected if they are to the north, south, east, west, southwest, southeast, northwest, or northeast of each other. Once the labeling of the flaw images completed, a variety of properties of the scratches can be extracted.

#### *2.3.2.3 Haze Measurement*

Haze is a measurement of diffuse light scatter created both by wafer surface topography and its subsurface properties. In CR80, Haze detection and processing occurs simultaneously with detection and processing particle data.

Haze on a wafer manifests itself in the dark scattering channel as a small positive direct coupled (DC) shift above a quiet reference level. Proper detection of this signal requires a very stable dark channel DC reference be maintained, and all high frequency elements of the signal (flaws) be filtered out.

Input to Haze analog processor is the direct coupled output of the photo multiplier tube. The resulting signal is then sent through a low pass filter and is presented to an analog-to-digital (A/D) converter. A dark channel DC reference level is established immediately prior to the wafer scan, while it is still stationary on the transport, by sampling the dark signal in a quiet area of the scan. The signal is sampled by an A/D circuit. The A/D values obtained is compared to the high scattered target value. Effectively, this eliminates any background illumination variation within the system from effecting the overall Haze measurement of the wafer. [42]

The creation of the Haze map is performed by the map processor. The map processor reads the haze data collected over one scan line. The map processor averages haze data over a number of scan lines to produce one line of haze data. The number of scan lines associated with each line of haze data is taken and applied to a precalculated table resulting in a haze map.

The wafer map is a computer generated representation of the scanned wafer with color coded pixels (bins) to illustrate the Haze levels and its location, as shown in Figure 2.19. A table on the left side of the view shows the bin range magnitude in parts per million(PPM) and the resulting percentage of wafer area covered by haze correlating to the magnitude. Each bin icon range is represented on the map by a distinct color. The haze icons, 0-9, each related to a PPM magnitude range, allow categorization of haze data. In addition, an overall Average Haze level is computed and reported. "Average Haze Allowed" is the average value of haze at which the wafer will be rejected for haze. "Total Haze Allowed" is percent of haze at or above the specified minimum haze value which is allowed before being rejected for haze. Both of this values are controlled via the recipe and wafers will be rejected during classification upon exceeding these values.

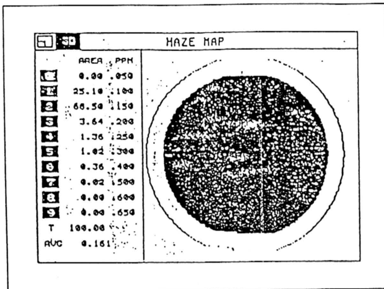


Figure 2.19. A sample haze map

Two analytical views on Haze are available in CR80. The Haze Histogram View graphically deplots the Gaussian distribution of the percentage of total wafer area covered at each haze magnitude in PPM. The Haze Statistics View contains the number of wafers processed, the bin particle size, the total particle counts in the bin, the sample average, and the sample standard deviation. Collection of haze data is automatic and independent of the recipe. Particle counts from each wafer measurement, regardless of recipe, are added continuously until the data is cleared.

## 2.4 VISUAL INSPECTION TECHNIQUES

Visual inspection is a method commonly used to identify defective wafers, in which the defects can be visually detected. Some of these defects are including saw mark, chip, imperfect edge profiling, scratches, stain, dimple, particle, etc. These defects are usually visible under fluorescence light, or

high intensity light. Basically there are two types of visual inspection techniques being practiced in MEMC KL, i.e. in-line visual inspection, and 100% visual inspection at different areas.

In-line visual inspection is carried out within every process, where a few wafers from the batch will be picked and inspected in a random basis. In Slicing for example, 2 of every 25 wafers will be inspected for slicing defects before proceeding to Edge Profiling. This will help in reducing performance losses in any particular process due to deviation on process settings, equipment adjustment, etc. Consequently corrective actions could be undertaken immediately before many defective wafers are produced.

However, some wafers with surface damage such as saw marks which cannot be removed at the preceding process like lapping, etching or polishing are need to be rejected. Besides that, certain defects on the wafers will appear much clearer at the subsequent process and they are also need to be rejected. For example, nick mark on the wafer edge from edge profiling will be much easier to be detected after etching process. Therefore 100% visual inspection is required to evaluate the wafers quality at several areas in Modifications, Polishing and Clean room. This will be further descried in the following sections.

### 2.4.1 Visual Inspection In Modifications Area

After etching process, 100% of the wafers will be evaluated for surface defects which is contributed by any of the process in Modifications, such as chips, saw marks, fractures, imperfect grinding, nick mark, lapping scratches, bad etch, dull center, stain, roller mark, etc. which cannot be captured at the in-line visual inspection. The evaluation is also named as Etched Quality Control (EQC), where the quality of the wafers is assured with customer specifications before

feeding to Polishing area. Wafers are manually handled during the inspection process, therefore extra care is necessary to avoid any defect such as scratch, surface chip, etc. due to improper handling. [43]

The inspection is carried out in a specially designed table equipped with both fluorescent light and Kodak light. Kodak light with intensity ranges from 18,000 to 22,000 foot candle is used as the light source for inspection as most the surface defects are visible under Kodak light. Etched wafers are sent to the inspection table as soon as they are cleaned and dried in the Rinser Dryer. A vacuum pencil is used to handle the wafer during the inspection process. Both sides of the wafers will be inspected with respect to the "Surface Inspection Acceptance Criteria For Grade 1 Wafer" which is established based on customer specifications.

### 2.4.2 Visual Inspection At Polishing Area

At Polishing area, 100% of the wafers will be inspected before and after the polishing process. During the mounting process before polishing, the wafers are counter checked for the surface defects contributed from Modifications process, so that the poor quality wafers from the incoming feed can be minimized. After polishing, the polished wafers which are dewaxed and cleaned are being inspected visually for defects on both sides. The surface inspection with ambient fluorescent light allows for detection of many polishing defects such as scratches, dimple, measles, surface chip and fracture. The inspection under fluorescent light is performed manually, thus the wafers are handled with care as improper handling might damage the wafers. The inspection is carried out for one wafer at a time, by using a vacuum wand to move the wafer so that the fluorescent tubes reflection sweep across the entire surface. Any defect present is easily observed between the reflection and the dark area created by the fluorescent tube and the edge of the lamp housing. [44]

### 2.4.3 Visual Inspection At The Clean Room

In clean room, wafers are inspected at the Multi Angle Inspection Station (MAIS) on several surface defects such as particles, scratches, streaks, stain, etc. before going into the shipping package. MAIS involves several operations performed by operators in an effort to keep product quality parameters in control and high quality product flowing to the customers. [45]

A front surface inspection is carried out when the paddle arm of MAIS transports the wafer into a dark field chamber equipped with multi angle tilt chuck. Kodak light with intensity ranges from 18,000 to 22,000 foot candles is used as the light source for frontside evaluation. For backside inspection, the light source is fiber optic light.

MAIS provides capability for visual inspection on the front and backside of polished wafers which eliminates manual handling. The wafers are automatically fed to the inspection chamber by the robotics paddle arm. The wafers are then visually inspected by the operator. Upon the operator's command, the wafers are transported to the wafer prealigner, flat aligned, and finally transported to the receiving module without and manual handling. By this automation, the possibility of handling scratches introduced onto the wafers can be minimized. The polished surface of the wafers is inspected on a 100% inspection plan, while backside surface is inspected on a 1 wafer per every 25 wafers basis.