CHAPTER 3

RESULTS AND DISCUSSION

3.1 INTRODUCTION

The analysis on silicon wastage of the defective wafers and the removal of material in various wafer manufacturing processes is based on the production data of MEMC KL for the fourth quarter of 1995. The data is collected for three main manufacturing areas in MEMC KL for the standard products 100mm and 125mm diameter wafers, i.e.:

i. ***Modifications*** - which covers the major processes such as slicing, edge profiling, lapping, etching and annealing.

ii. ***Polishing*** - which covers polishing block mounting, rough and final polishing, and demounting.

iii. ***Clean Room*** - which covers the polished slice cleaning (PSC) and inspections (Microscan, ESTEK CR80 and visual inspection).

The data analysis and discussions in this chapter is divided into three major sections. The yield performance of MEMC KL during the fourth quarter of 1995 will be discussed in the first section, where calculations are done based on the material standard specification as shown in Table 1. This section will cover the production summary for 100mm and 125mm materials, the material losses in wafer manufacturing in term of material removal and performance losses. Pareto analysis on the performance losses will also be discussed in this section.

In the next section, the Microscan measurement results and mapping on flatness and thickness parameters such as Total Thickness Variation (TTV), Total Indicated Reading (TIR), Site TIR (STIR), Bow and Warp for some grade 1 and defective wafers will be shown and discussed. The ESTEK CR80 measurement results and mapping on particles, haze and scratches for some grade 1 and defective wafers will be shown and discussed in the last section.

Product Specifications	**Unit**	**Product Type**	
		100mm Material	**125mm Material**
Gram per inch	gram	472	732
Wafer per inch	slice	25.96	23.68
Theoretical weight	gram	18.18	30.53
Off-slicing thickness	mil	25.3	29.2
Slicing Kerf loss	mil	12.6	12.6
Lapping removal	mil	2.5	2.5
Etching removal	mil	1.4	1.4
Polishing removal	mil	0.7	0.7
Finished product thickness (average)	µm	525	625
Actual weight	gram	9.91	17.93

Table 3.1 : Material standard specifications of silicon wafer manufacturing in MEMC KL

3.2 ANALYSIS ON MEMC KL 1995 4TH QUARTER PERFORMANCE

3.2.1 Production Summary

The production summary on 100mm and 125mm materials for MEMC KL during the fourth quarter of 1995 is shown in Table 3.2. A total of 754,734 slices of 100mm wafers and 212,997 slices of 125mm wafers were produced in Slicing during the three months periods. However, there were 43,142 slices and 20,091 slices of 100mm and 125mm wafers being rejected at various processes in Modifications such as slicing, edge profiling, lapping, etching and annealing. The defects were comprising of saw marks, scratches, thickness fallout, chips, breakages, and many others. As a result, the yield in Modifications was 94.28% and 90.57% for 100mm and 125mm materials respectively.

After completing the Modifications processes, a total of 708,953 slices and 191,853 slices of 100mm and 125mm grade 1 etched wafers were fed to Polishing for subsequent processing. Out of this volume, 4,495 slices and 17,007 slices of 100mm wafers were rejected in Polishing and the Clean room respectively. For the 125mm wafers, the total rejects in Polishing and the Clean room were 2,422 slices and 5,720 slices respectively. The rejects in these two areas were made up of scratches, fallout on the flatness parameters (TTV, TIR, STIR), the light point defects (LPD) such as particles and haze contamination, dimple, stain, breakages, etc.

As a whole, a total of 64,644 slices of 100mm wafers and 28,233 slices of 125mm wafers were rejected, out of the total wafers produced, i.e. 754,734 slices of 100mm wafers and 212,997 slices of 125mm wafers. In other words, the plant overall yield in the fourth quarter of 1995 for 100mm and 125mm materials were 91.43% and 86.74% respectively.

Mfg. Area	Production Term	Unit	100mm	125mm
Modifications	Silicon ingots (weight)	Kg	13,707	6,550
	Silicon ingots (length)	Inch	29,040	8,948
	Average thickness at Slicing	mils	25.3	29.2
	Total wafers from Saws	Slices	754,734	212,997
	Rejects in Slicing	Slices	2,639	1,053
	Grade 1 wafers after Slicing	Slices	752,095	211,944
	Rejects in Modifications	Slices	43,142	20,091
	Modifications Yield	Percentage	94.28%	90.57%
Polishing	Feed to Polishing	Slices	708,953	191,853
	Rejects in Polishing	Slices	4,495	2,422
	Polishing Yield	Percentage	99.37%	98.74%
Clean Room	Feed to Clean room	Slices	704,458	189,431
	Rejects in Clean room	Slices	17,007	5,720
	Clean room Yield	Percentage	97.59%	96.98%
Overall	Total Grade 1 Polished Wafer	Slices	687,451	183,711
	Total rejects	Slices	64,644	28,233
	Plant Yield	Percentage	91.43%	86.74%

Table 3.2 : MEMC KL 4th quarter 1995 production summary for 100mm and 125mm materials

In order to study the silicon wastage, the data on 100mm and 125mm materials used during the fourth quarter were extracted from the production data, where they were grouped into four categories, i.e. grade 1 wafers, losses on slicing kerf, removal losses, and performance losses in

term of their total weight in kilograms. The results are shown in Table 3.3, where they were calculated based on the material standard specifications and the production summary as mentioned in the previous paragraphs.

Material Category	Total Weight (Kg)	
	100mm Material	125mm Material
Grade 1 Wafers	6,347	3,109
Kerf loss	4,562	1,956
Material removal	1,623	612
Performance losses	1,175	873

Table 3.3. Material category for 100mm and 125mm materials (by weight)

The results is further illustrated in the material category chart shown in Figure 3.1. It can be seen that there were more than 50% of the total materials issued to the production being wasted as silicon wastage for both 100mm and 125mm materials. For the 100mm materials, 33.3% were wasted for slicing kerf loss, 11.8% for removal losses, and 8.6% for performance losses. On the other hand, 29.9% of the 125mm materials were wasted for slicing kerf loss, 9.3% for removal losses, and 13.3% for performance losses.

3.2.2 Silicon Wastage Analysis for Performance Losses and Removal Losses

3.2.2.1 Performance Losses Analysis

Table 3.4 shows the performance losses for both 100mm and 125mm materials in various manufacturing areas. The losses are presented in term of slices, weight and percentage of rejects.

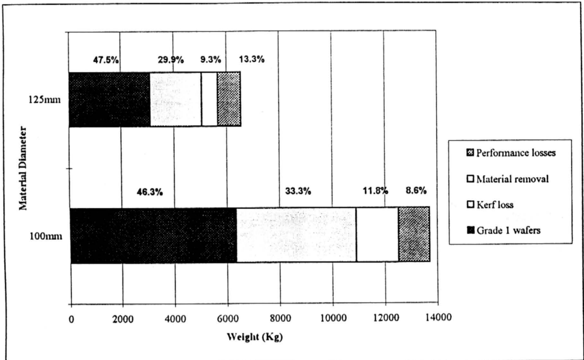

Figure 3.1. Material category chart for 100mm and 125mm materials (by weight)

Product	Mfg. Area	Slices	Weight (kg)	% of Rejects
100mm	Modifications	43,142	784.400	5.72%
	Polishing	4,495	81.727	0.60%
	Clean room	17,007	309.218	2.26%
	Subtotal	64,644	1,175.345	8.57%
125mm	Modification	20,091	621.056	9.48%
	Polishing	2422	74.869	1.14%
	Clean room	5720	176.818	2.70%
	Subtotal	28,233	872.743	13.32%
Overall	**Total**	**92,877**	**2,048.089**	**10.11%**

Table 3.4. Performance losses for 100mm and 125mm in various manufacturing areas

It can be seen that the total rejects on 100mm wafers were 64,644 out of 754,734 slices produced, where Modifications area had the highest percentage of rejects, i.e. 5.72%. This value is also equalled to 66.74% of the total performance losses on 100mm materials. The higher reject rate in Modifications area is because of the wafers had undergone multiple mechanical and chemical shaping processes which had introduced more physical damages on the wafers as compared with the back end processes. The amount of rejects in Polishing was relatively low as compared with Clean room rejects, as Polishing related defects like flatness fallout, microscratches, etc. were not visible and could not be detected in Polishing. These rejects were only be detected at the inspection and measurement stations which are located in the Clean room. Figure 3.2 further illustrates the performance losses on 100mm materials in various manufacturing areas.

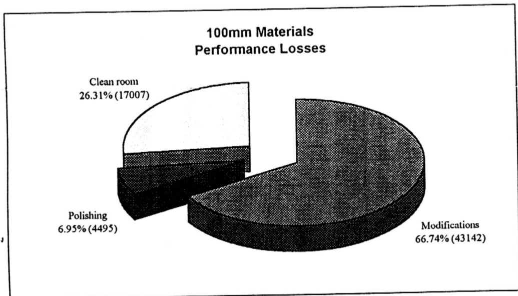

Figure 3.2. Performance losses on 100mm materials in various manufacturing areas

Similarly, the total rejects on 125mm wafers were 28,233 out of 212,997 slices produced, where Modifications area had the highest percentage of rejects, i.e. 9.48%. This value is also equalled to 71.16% of the total performance losses on 125mm materials, where as the percentage of rejects in

Polishing and Clean room are 1.14% and 2.7% respectively. The performance losses on 125mm materials in various manufacturing areas is shown in Figure 3.3. The overall reject rate for 125mm wafers was higher as compared with the reject rate for 100mm wafers, especially in Modifications and Polishing areas. One of the reasons is because of the 125mm wafer has a larger surface area, consequently the wafers will have more exposed area for the mechanical shaping processes and contamination, which results higher rate of rejects on physical damages such as saw marks, scratches, etc.

As a whole, the total rejected wafers on performance losses were 92,877 slices out of 871,162 slices of both 100mm and 125mm wafers which produced during the three months period. The losses were also corresponded with a total weight of 2048.089 kg, which is equalled to 10.11% of the overall production volume for that period.

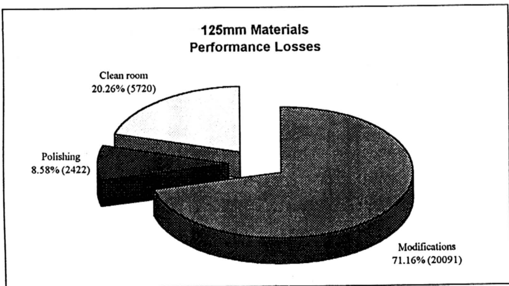

Figure 3.3. Performance losses on 125mm materials in various manufacturing areas

3.2.2.2 Removal Losses Analysis

Besides material losses on the defective wafers, the major proportion of the material wastage is also contributed by the removal of materials in various wafering processes which cannot be avoided due to the process requirement. There are four major processes which involve a significant removal of materials, i.e. Slicing, Lapping, Etching and Polishing. The results of the losses on material removal is presented in Table 3.5.

Process	100mm Material (Kg)	125mm Material (Kg)	TOTAL (Kg)
Slicing	4,561.62	1,955.50	6,517.12
Lapping	888.39	376.43	1264.81
Etching	497.00	138.36	635.36
Polishing	238.05	97.85	335.91
Grand Total	**6,185.06**	**2,568.13**	**8,753.19**

Table 3.5. Removal losses for 100mm and 125mm materials in different processes

The results in Table 3.5 is further illustrated in pie charts for both 100mm and 125mm materials as shown in Figure 3.4 and Figure 3.5 respectively. It can be seen that both charts look similar to each, other as the removal rate at each process are the same for both the materials. The major proportion is made up by the slicing kerf loss which is equalled to 73.75% for 100mm materials and 76.14% for 125mm materials. The remaining proportion for the material removal is followed by the removal at lapping, etching, and finally by polishing in a decreasing manner.

In fact, the proportion on slicing kerf loss is approximately 32% of the total materials used in wafer manufacturing during the fourth quarter of 1995, as shown in Figure 3.1 in Section 3.2.1.

The kerf dimension (12.6 mils) is equalled to almost half of the target thickness for both materials. In other words, almost one third of the material will be wasted in producing one slice of wafer. Kerf loss is however difficult to be reduced, unless the blade with a smaller kerf is used for slicing operation. Similarly, the amount of material removed in other processes is depending upon the removal rate of each process. Lapping removal of 2.4 mils is required to remove the surface damages caused by slicing process and to produce flat wafers. Etching will remove 1.5 mils of the material on each wafer by chemical reactions (with mixed acid), which is also to remove the defects from lapping process. A removal of 0.7 mils in Polishing is the final process to further improve the flatness parameters (TTV, TIR, STIR) on the wafers surface. In other words, more material will be removed from the wafers with the higher removal rate.

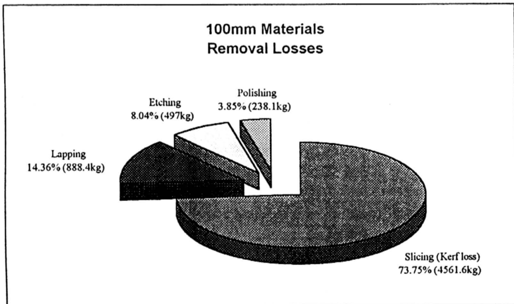

Figure 3.4. Removal losses on 100mm materials in different processes

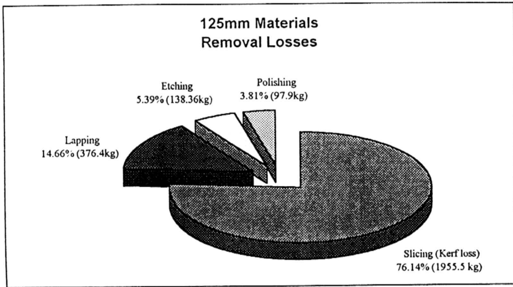

Figure 3.5. Removal losses on 125mm materials in different processes

3.2.3 Pareto Analysis on Performance Losses

3.2.3.1 Performance Losses In Modifications Processes

Table 3.6 shows the types and amount of rejects for the performance losses for both 100mm and 125mm materials in Modifications processes during the 4th quarter production. The pareto chart for these data is shown in Figure 3.6. It can be seen that the three major rejects in Modifications are contributed by scratches (9460 slices), saw marks (8990 slices) and thickness fallout (8295 slices). Scratches is a lapping related defect which is due to the process imperfection, where as the rejects on saw marks and thickness fallout is related to slicing process. The amount of these three rejects is equivalent to approximately 42% of the total rejects in Modifications. The other rejects in the lists are including breakages, off-slicing rejects, chips, hydrogen pits, fracture, edge profiling defects, stain and many others. Most of these defective wafers were rejected at the Etched Quality Control (EQC) inspection station, after completing etching process. Some of the defects were also being rejected in various processes.

Types of Reject	100mm Wafers		125mm Wafers	
	Quantity	Percentage	Quantity	Percentage
Scratches	6438	0.856%	3022	1.426%
Saw marks	6175	0.821%	2815	1.328%
Thickness fallout	5122	0.681%	3173	1.497%
Breakages	3324	0.442%	1596	0.753%
Off slicing rejects	2639	0.351%	1407	0.664%
Chips	2617	0.348%	1337	0.631%
Hydrogen pits	2444	0.325%	1085	0.512%
Fracture	2316	0.308%	1013	0.478%
EP defects	2136	0.284%	997	0.470%
Stain	1963	0.261%	816	0.385%
TTV fallout	1739	0.231%	490	0.231%
Resistivity fallout	1355	0.180%	379	0.179%
Roller mark	925	0.123%	239	0.113%
Warp fallout	790	0.105%	223	0.105%
Dull center	542	0.072%	201	0.095%
Others	2617	0.348%	1297	0.612%
TOTAL	**43142**	**5.736%**	**20091**	**9.479%**

Table 3.6. Breakdown of the performance losses in Modifications processes

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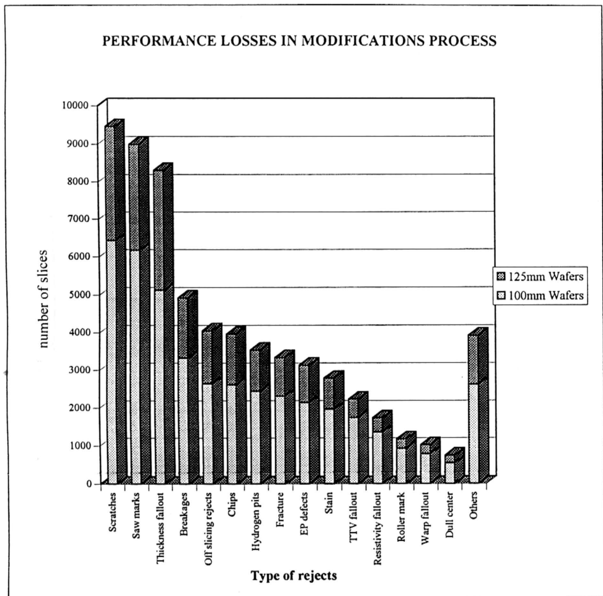

Figure 3.6. Pareto analysis on performance losses in Modifications processes

3.2.3.2 Performance Losses In Polishing And Clean Room Processes

The types and amount of rejects for the performance losses for both 100mm and 125mm materials in Polishing and Clean room processes is presented in Table 3.7. The pareto chart for these data is shown in Figure 3.7. It can be seen that polishing scratches has the highest amount of rejects, where 7,279 out of 900,806 slices of grade 1 etched wafers were rejected due to this defect. The

second and third highest rejects are contributed by flatness parameters fallout on STIR (5982 slices) and TTV (3381 slices). The other rejects in the lists are including the light point defects (LPD such as particles, haze and microscratches), dimples, stain, resistivity fallout, breakages, etc. The flatness defects were rejected in Microscan measurement system, where as the LPD were rejected by ESTEK CR80 wafer inspection system. Most of this these defects were Polishing related, due to process imperfection and the conditions of the environment. Besides that, the quality of the incoming feed from Modifications might also give some effects on the flatness parameters, and the surface damages as well.

Types of Reject	100mm Wafers		125mm Wafers	
	Quantity	Percentage	Quantity	Percentage
Scratches	4998	0.705%	2281	1.189%
STIR fallout	4729	0.667%	1253	0.653%
TTV fallout	2510	0.354%	871	0.454%
LPD	1524	0.215%	647	0.337%
Dimple	1290	0.182%	587	0.306%
Backside stain	950	0.134%	560	0.292%
Resistivity fallout	801	0.113%	334	0.174%
Breakages	744	0.105%	315	0.164%
Streaks	659	0.093%	207	0.108%
TIR fallout	518	0.073%	125	0.065%
Chips	461	0.065%	146	0.076%
Thickness fallout	375	0.053%	111	0.058%
Measles	276	0.039%	90	0.047%
Bad polish	170	0.024%	65	0.034%
Others	1496	0.211%	551	0.287%
TOTAL	21502	3.033%	8142	4.244%

Table 3.7. Breakdown of the performance losses in Polishing and Clean room

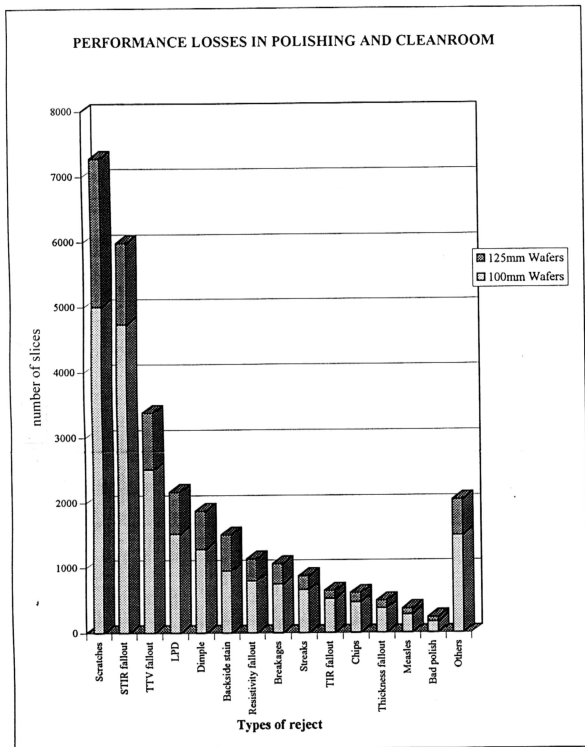

Figure 3.7. Pareto analysis on performance losses in Polishing and Clean room processes

3.3 MEASUREMENT RESULTS FROM MICROSCAN ADE8100

As mentioned in the previous chapter, Microscan ADE8100 is a measuring equipment used to measure wafers thickness and flatness parameters such as bow, warp, TTV, TIR and STIR. Besides that, Microscan also measures the resistivity and type of the wafers. The wafers are being measured by two Microscans, as the one located at Modifications is dedicated for measuring etched wafers, where as the other one in the Clean room is for measuring polished wafers. In this section, the measurement results on a few samples of etched wafers and polished wafers will be presented and discussed, as the printouts on topography (3-Dimension mapping) and site measurements will be included too.

3.3.1 Measurement Results For Etched Wafers

The measurement results of two sample 100mm etched wafers A and B taken from a same lot is presented in Table 3.8. Basically there are 6 parameters need to be measured on the etched wafers, i.e. TTV, TIR, STIR, bow, warp and thickness of the wafers. These measurement are important as to filter the defective wafers, not allowing them to proceeding to the next process as they might affect the polishing process parameters. Besides that, the result can also be a feed back tool for the previous processes for trouble shooting and corrective actions.

Wafer	Class	TTV	TIR	STIR	Bow	Warp	Thickness
Standard	Reference	< 4.0	< 3.50	< 3.50	< 20	< 40	545 ± 15
A	Accept	1.92	1.63	1.17	3.46	22.90	543.53
B	Reject	4.16	4.18	2.37	8.06	8.84	611.37

Table 3.8. Results on thickness and flatness parameters for 100mm etched wafers (all units in μm).

As shown in Table 3.8, the acceptance specification standard is the baseline used for accepting and rejecting wafers for this particular lot. Wafer A was accepted by the lot as all the parameters were within the acceptable limits. However, wafer B was rejected due to some of the parameters were out of the limits, i.e. TTV, TIR and thickness (the light shaded cells). The topography for both wafer A and wafer B are shown in Figure 3.8 and Figure 3.9 respectively, which they were constructed by using "best fit" reference plane for measurement. It can be seen that wafer A has a pretty flat surface, where the thickness of the wafer is evenly distributed over the surface. The topography for wafer B shows that there is a significant "bump" at the center of the wafer, which was caused by etching process imperfection. This defect is called dull center, which results bad flatness on the wafer.

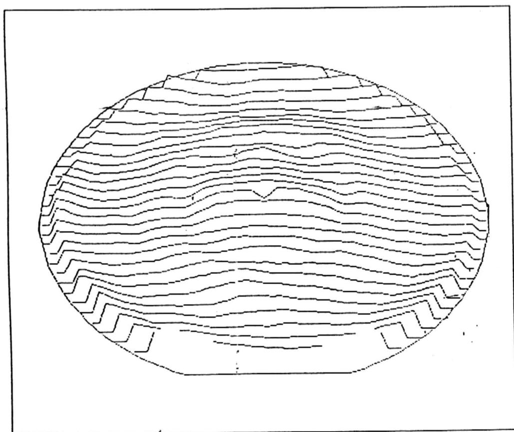

Figure 3.8. Schematic of flatness mapping for etched wafer A (grade 1)

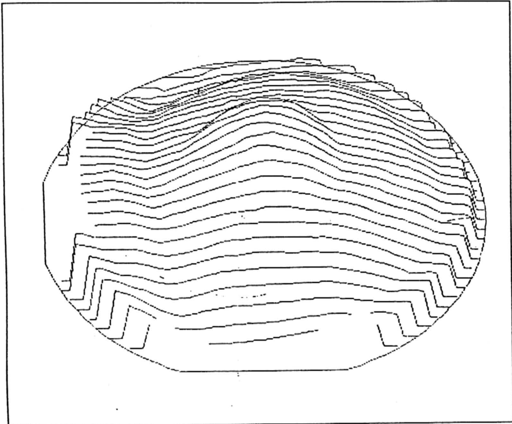

Figure 3.9. Schematic of flatness mapping for etched wafer B (reject)

3.3.2 Measurement Results For Polished Wafers

Two sample 100mm polished wafers C and D taken from a same lot were measured by Microscan located in the Clean room. The measurement results is presented in Table 3.9. The parameters measured on the polished wafers are including TTV, TIR, STIR, thickness, type and the resistivity of the wafers. The acceptance specification limits for polished wafers measurement are much tighter as these wafers will be the final products that meeting the customer needs.

As shown in Table 3.9, the acceptance specification standard is the baseline used for accepting and rejecting wafers for this particular lot. Wafer C was accepted by the lot as all the parameters were within the acceptable limits. Wafer D was however rejected due to the STIR reading was greater

Wafer	Class	TTV	TIR	STIR	Thickness	Type	Resistivity
Standard	Reference	< 2.0	< 1.5	< 1.5	525 ± 10	P	0 - 200.
C	Accept	0.87	0.28	0.35	525.38	P	15.83
D	Reject	2.53	1.83	1.89	531.93	P	13.83

Table 3.9. Measurement results on thickness and flatness parameters for 100mm polished wafers (all unit in μm, except resistivity in ohm-cm)

than the standard. Consequently the global TIR reading was affected by the site reading too. Besides that, wafer D was also rejected for TTV as the result was greater than the specification.

Two topographies were made for each of these wafers (C and D), which were constructed by using "best fit" reference plane for measurement. Figure 3.10 and Figure 3.12 are the 3-dimension mapping on flatness, where as Figure 3.11 and 3.13 are the numerical mapping for STIR (Site measurement). There are a total of 16 site measurements, where each site is made up of a 20mm by 20mm square box.

It can be seen in Figure 3.10 that wafer C has a very fine finishing on the flatness, and the wafer thickness is consistent over the entire surface. The measurement on site as shown in Figure 3.11 also, shows a relatively low flatness result as compared to the standard. As a result, wafer C was accepted for further processing.

On the other hand, the topography for wafer D in Figure 3.12 shows a taper shape wafer with a hole close to the right edge, which is a dimple defect occurred in the polishing process. It can be seen in Figure 3.13 that the TIR at that particular site is especially high compared with the others. As the result is greater than the standard, wafer D is therefore rejected from the lot.

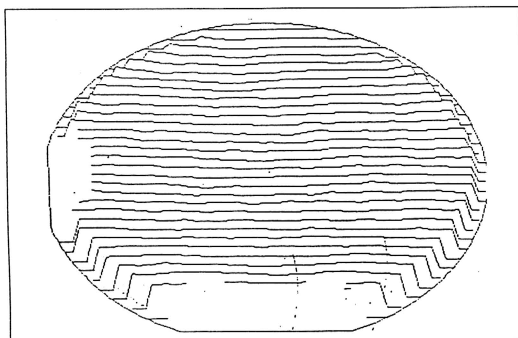

Figure 3.10. Schematic of flatness mapping for grade 1 polished wafer C

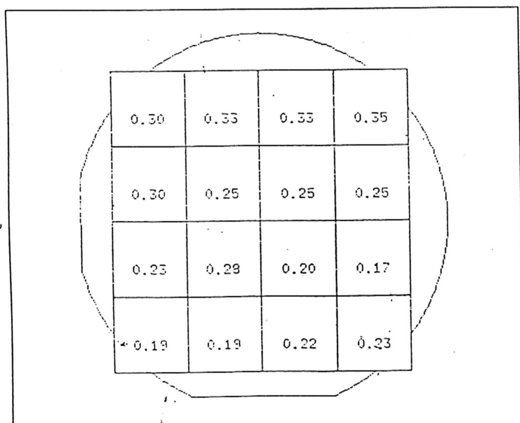

Figure 3.11. Numerical mapping on STIR for grade 1 polished wafer C

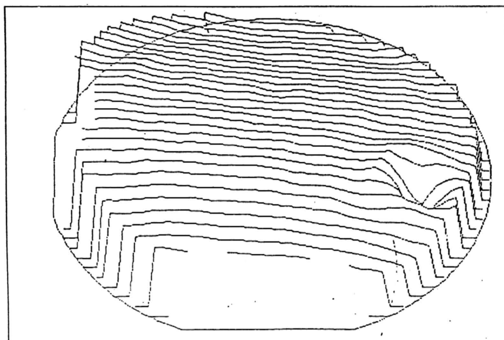

Figure 3.12. Schematic of flatness mapping for rejected polished wafer D.

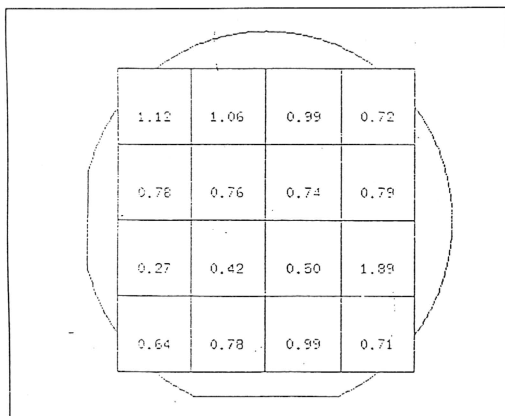

Figure 3.13. Numerical mapping on STIR for rejected polished wafer D

3.4 MEASUREMENT RESULTS FROM ESTEK CR80

After the wafers are being inspected by Microscan ADE8100 for thickness and flatness parameters, the wafers will be chemically cleaned. The wafers will be inspected by ESTEK CR80 for surface contamination such as particle, haze and scratches, before they are packed and shipped to the customers. In this section, 3 sample polished wafers have been measured by ESTEK CR80 and the printouts for each wafer are presented in the later part. These wafers were measured based on the acceptance limits for particle and haze as shown in Table 3.10 and 3.11 respectively. It can be seen that for particle measurement, there are 9 different flaws (acceptance limit for each particle size), ranging from 0.173μm to 3μm, where the flaw for larger particle size will has less allowable amount of particles. Flaw "S" in the last row represents the allowable limit for scratches.

Flaw	Size (μm)	Allowed (Qty)
0	≥ 0.173	350
1	≥ 0.200	15
2	≥ 0.300	5
3	≥ 0.400	5
4	≥ 0.700	5
5	≥ 1.000	5
6	≥ 1.500	5
7	≥ 2.000	5
8	≥ 3.000	5
S	≥ 2100	0

Table 3.10. Acceptance limits for Particle measurement

Haze	PPM	Allowed (%)
0	0.969	100
1	1.62	100
2	1.71	100
3	1.81	100
4	1.90	100
5	2.00	100
6	2.10	100
7	2.19	100
8	2.29	100
9	2.38	100

Table 3.11. Acceptance limits for haze measurement

On the other hand, there are 10 different allowable haze limits as shows in Table 3.11. The average haze allowed is not greater than 2.50 ppm, where the area contaminated by haze should be added up to 100% or less.

Figure 3.14 shows the CR80 printout for a grade 1 polished wafer. The printout consists of a flaw map (particle map), a haze map, and 2 histograms for both flaw and particle mapping results. On the flaw map, it can be seen that there are only two particle counts on the wafer, where one is less than 0.173μm and the other one is in between 0.173 and 0.2μm. On the haze map, 71.48% of the total area on the wafer is covered by level 5 haze, where as level 4 and 3 cover 23.08% and 3.44% of the surface area respectively, with an average haze of 1.95 ppm. This particular wafer was therefore accepted as a grade 1 finished product as compared with the acceptance limits.

The CR80 printout for a rejected polished wafer is shown in Figure 3.15. It can be seen in the flaw map that the wafer was badly contaminated by particles of all different sizes, especially high for the smaller particle sizes. This reflects the cleaning process might be inefficient at that particular time. From the results shown in the haze map, the haze level of this wafer was still acceptable as the average haze was 1.56 ppm, which level 4 haze dominant the wafer surface area. Even though the haze level was acceptable, the wafer was rejected due to particles contamination as this is not tolerated in wafer fabrications process.

At the same time, a series of mapping on another grade 1 polished wafer are presented, where the printouts are inclusive of both 2-dimension and 3-dimension mapping on particles and haze measurement. The 2D maps are shown in Figure 3.16 and 3.17, where as the 3D maps for particles and haze are shown in Figure 3.18 and 3.19 respectively. With the 3D mapping, the failure analysis process on surface contamination could be enhance and more efficient.

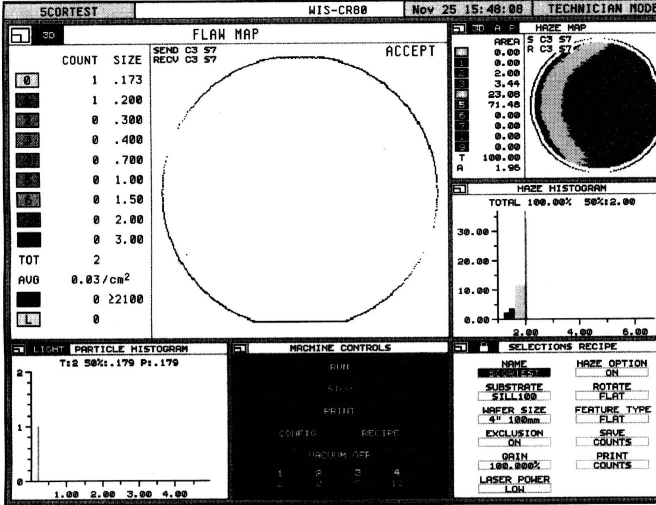

Figure 3.14. ESTEK CR80 printout on particle and haze for a sample grade 1 polished wafer

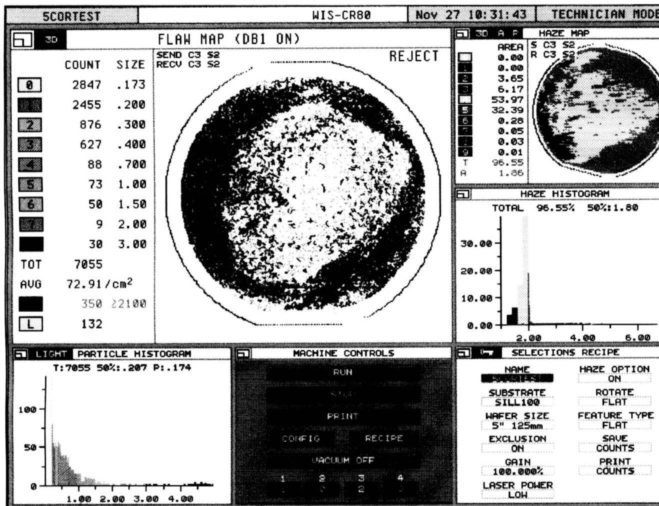

Figure 3.15. ESTEK CR80 printout on particle and haze for a sample rejected polished wafer

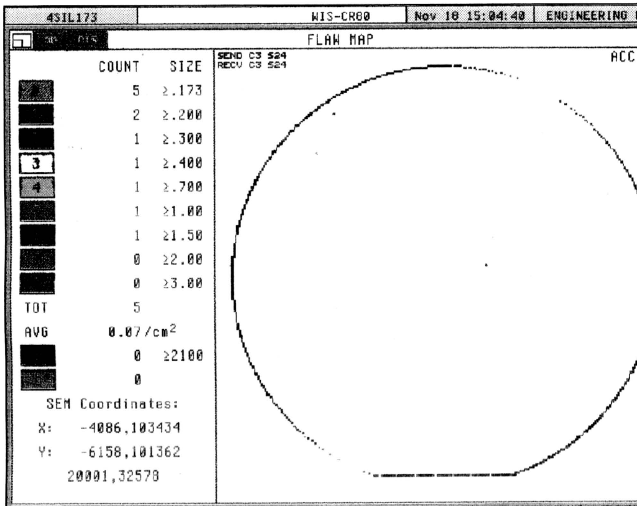

Figure 3.16. 2-D flaw map for a sample grade 1 polished wafer

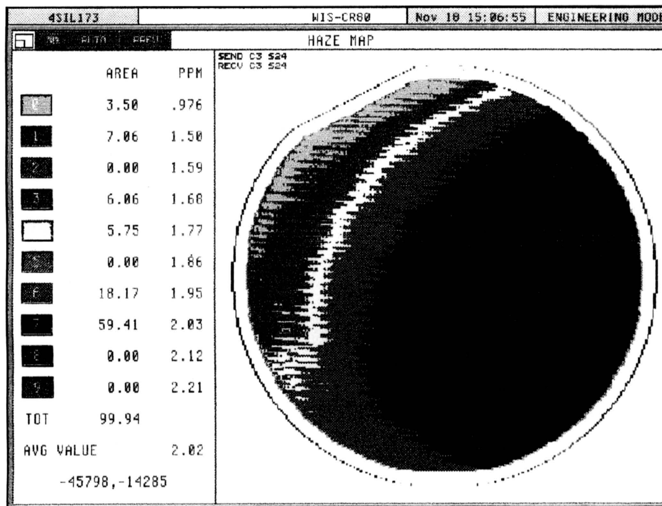

Figure 3.17. 2-D haze map for a sample grade 1 polished wafer

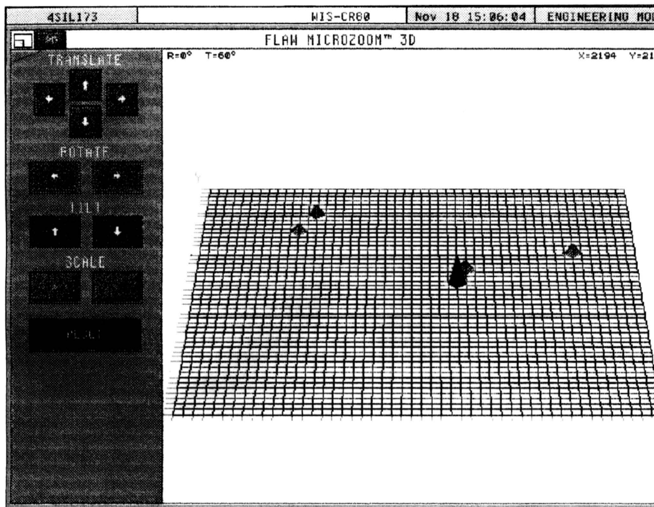

Figure 3.18. 3-D flaw map for a sample grade 1 polished wafer

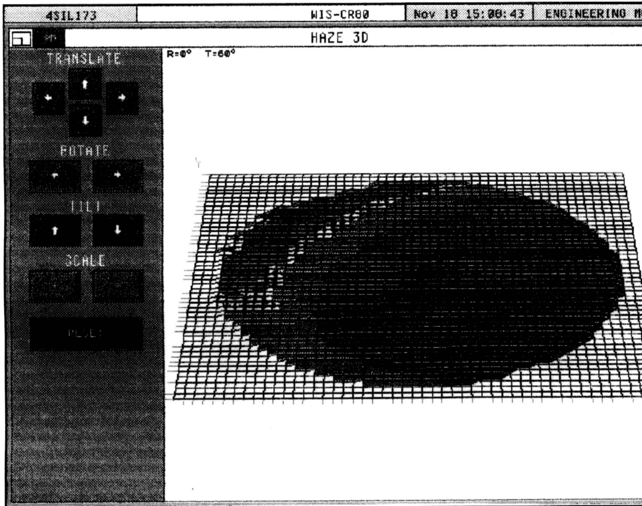

Figure 3.19. 3-D haze mapfor a sample grade 1 polished wafer