ANALYSING RANDOM ACCESS MEMORY CHIP YIELD PERFORMANCE

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ABSTRACT

Despite advances in integrated circuits (IC) equipment and fabrication techniques, there still exist random fluctuations or statistical disturbances in any IC manufacturing facility, which can adversely affect the production yield. Actually devices and circuits are being designed with increasingly tighter parameter and performance margins. As a result, chip performance becomes even more sensitive to the statistical variations, and this may result in low production yield.

One of the significant detractors of cost in a manufacturing line is yield loss due to contamination and the time required to increase the yield to profitable levels. Yield loss in a manufacturing line is determined by the various attributes of fabrication, product, testing and failure analysis. This research attempts to determine whether there are any significant differences in the average yield by tester, by day and by test insert at each different level of temperature i.e. TOS, TLO and THI test insert. This paper also attempts to examine the yield across the various tests and investigated the major defect type that contributed to yield loss.

Table of Contents

CHAPTER 6
CONCLUSION

List of Figures

List of Tables

ACRONYMS

ASIC	Application Specific Integrated
ATE	Automatic Test Equipment
BGA	Ball Grid Array
CIM	Computer Integrated Manufacturing
CMOS	Complementary Metal Oxide Semiconductor
DRAM	Dynamic Random Access Memory
DRET	Data Retention Test
DSP	Digital Signal Processor
DUT	Device under Test
ECL	Emitter-couple
EPROM	Electronic Programmable Memory
FSRAM	Fast Static Random Access Memory
GaAs	Gallium Arsenide
GHKH	Cycle Time
HDTV	High Definition TV
I_{DD}	Active Power Supply Current
I_{OH}	Output Logic High
I_{OL}	Output Logic Low
ICs	Integrated Circuits
I/O	Input Output
JTAG	Joint Test Action Group
LWSH	Long Write Static Hold
MOS	Metal Oxide Semiconductor
NMOS	n-channel Metal Oxide Semiconductor
PC	Process Control
PMOS	p-channel Metal Oxide Semiconductor
QA	Quality Assurance
ROM	Read-only Memory
RAM	Random Access Memory
SRAM	Static Random Access Memory
THI	High Temperature Test
TLO	Low Temperature Test
TOS	Open Short Test
Vdd	Core Power Supply Voltage
V_{IH}	DC Input Logic High
V_{IL}	DC Input Logic Low
V_{OH}	Light Load Output Logic High
V_{OL}	Light Load Output Logic Low
VREG	Voltage Register