CHAPTER 2

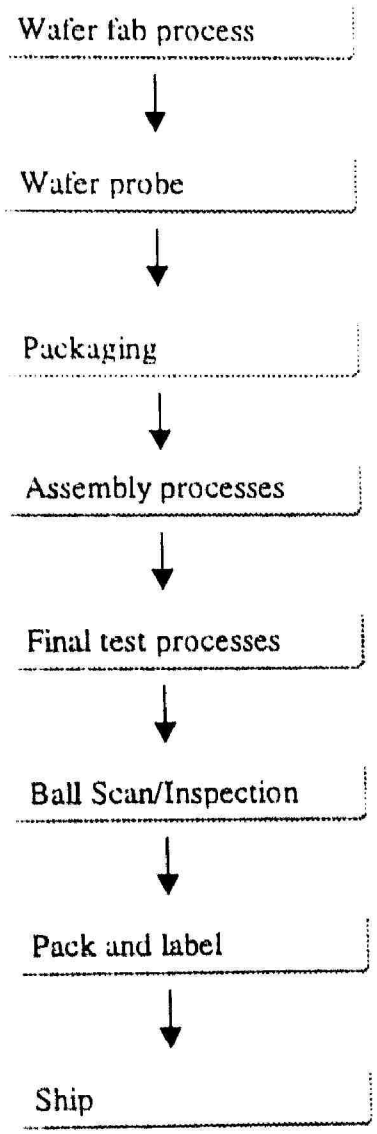
GENERAL MANUFACTURING

PROCESS FLOW

2.1 Introduction

In this chapter, we describe the entire integrated circuits (ICs) processes from wafer process to final test and packaging. These processes will enable us to understand the nature of ICs manufacturing, the need to identify defects and the procedure for identifying defects. The latter is important because any delay in detecting possible yield problems and in identifying the source of the problem can result in significant revenue loss.

Figure 2.1 shows a typical general process flow from wafer fabrication to pack and label and ship. These eight stages are wafer fab process, wafer probe, packaging, assembly process, final test process, ball scan/inspection, pack and label and ship. Section 2.2 below discusses wafer fabrication, which consists of wafer fab process, wafer probe and packaging. This is follow in section 2.3 by a discussion of the assembly processes. A detail discussion on final test processes is presented in section 2.4. Finally, in section 2.5 presented a brief discussion of final stages, which consists of ball scan/inspection, pack and label and ship.

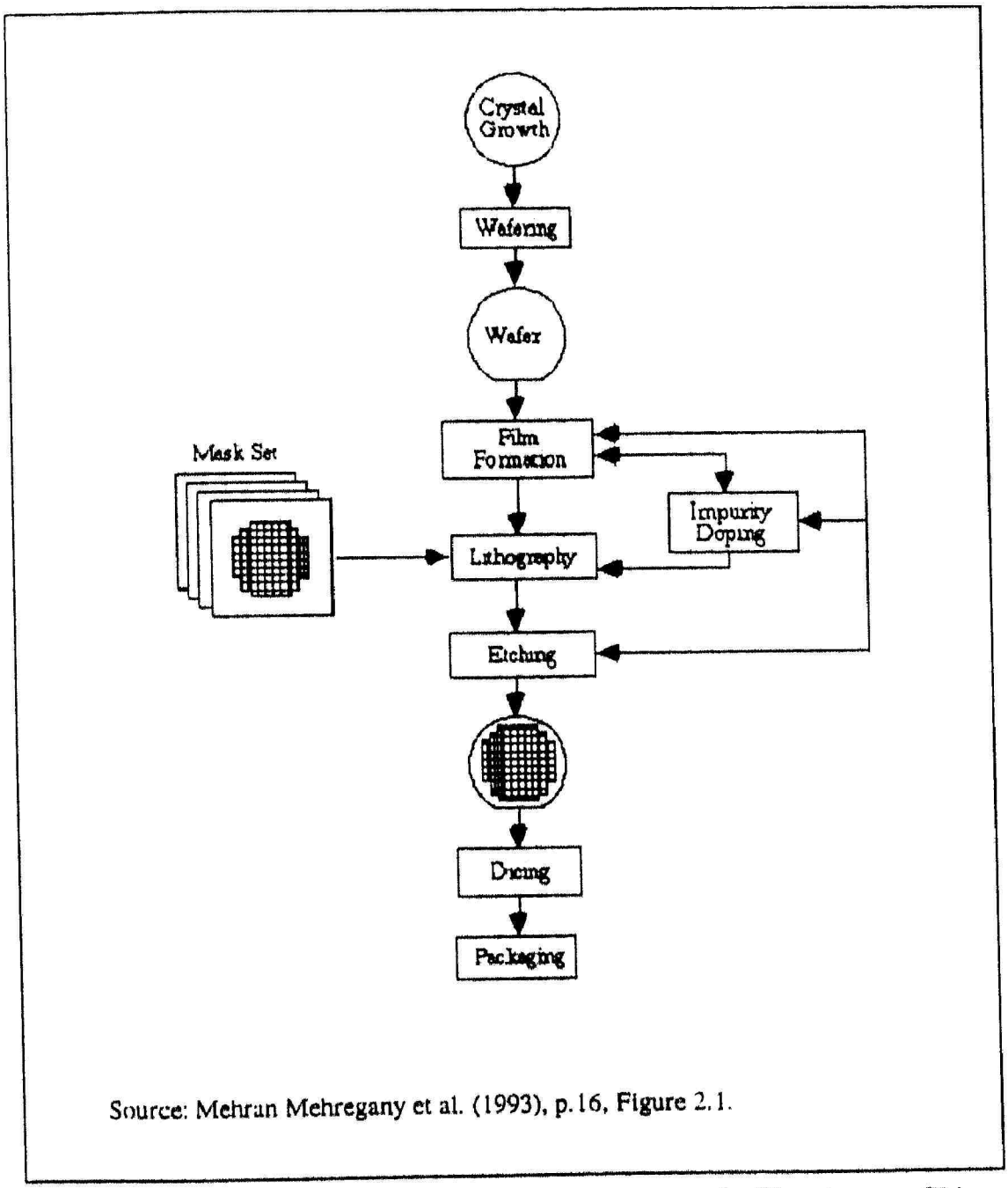


Source: Teh et al. (1998), p.2, Figure 1.

Figure2.1 Typical General Process Flow of Semiconductor Device Manufacturing

2.2 Wafer Fabrication

This section provides an overview of basic processes used to fabricate silicon wafers (Beadle W. et al 1985, Wolfe et al 1986, Thompson L.F. et al 1984). The steps of main process used in wafer fabrication are illustrated in Figure 2.2. Tests on the wafers are usually conducted before packaging.

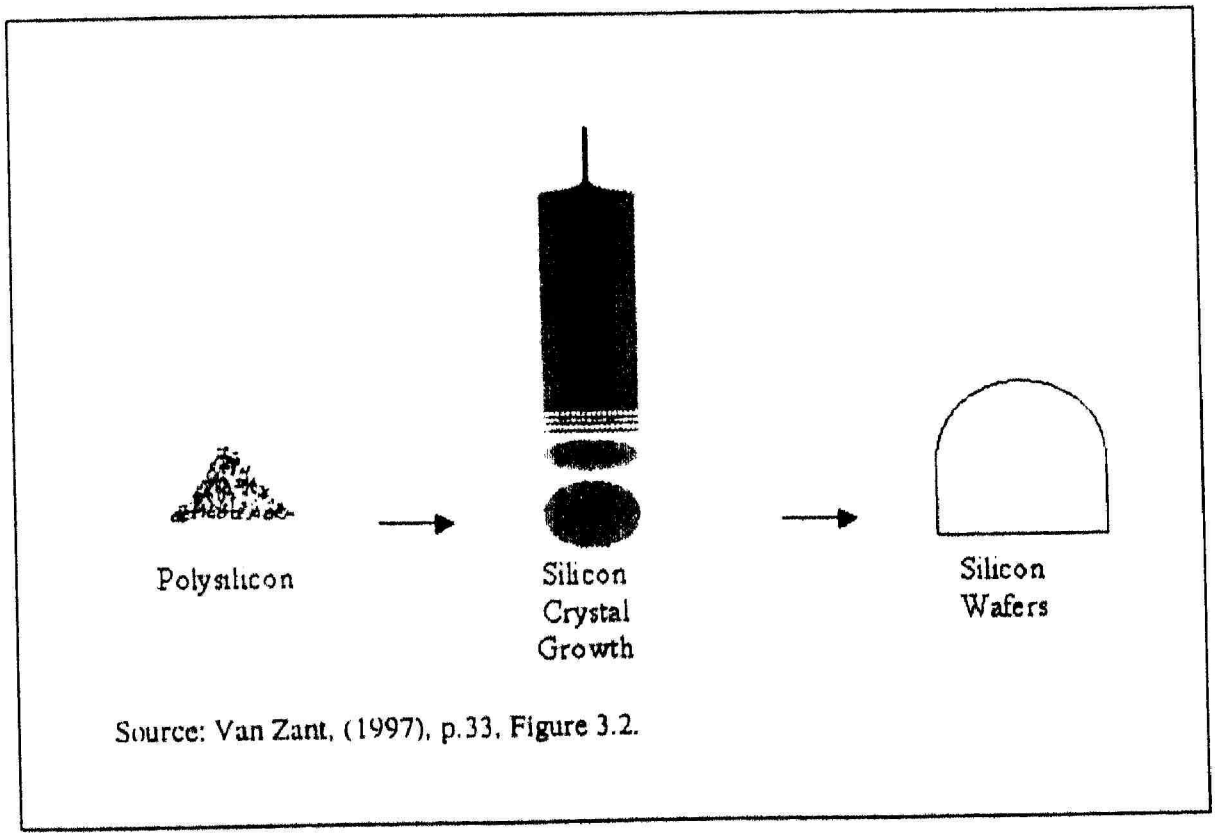


Source: Mehran Mehregany et al. (1993), p.16, Figure 2.1.

Figure 2.2 Major Processing Steps in Integrated Circuit or Chips Fabrication.

2.2.1 Wafer Fab Process

Semiconductor crystal growth, wafers slicing and polishing produce the wafers on which the devices are fabricated. Crystal growth is a specialized technology, which involves precise environment control to maintain high purity of the grown ingot (see Figure 2.3). A small piece of solid silicon (seed) is placed on the molten liquid, and as the seed is slowly pulled from the melt, the liquid cools to form a single crystal ingot. The crystal ingot is then ground to a uniform diameter and a diamond saw blade cuts the ingot into thin wafers and chemically polished to a mirror-like luster. Wafers are thin slices of silicon crystal substrate on which hundreds of copies of integrated circuits are formed on a single wafer.



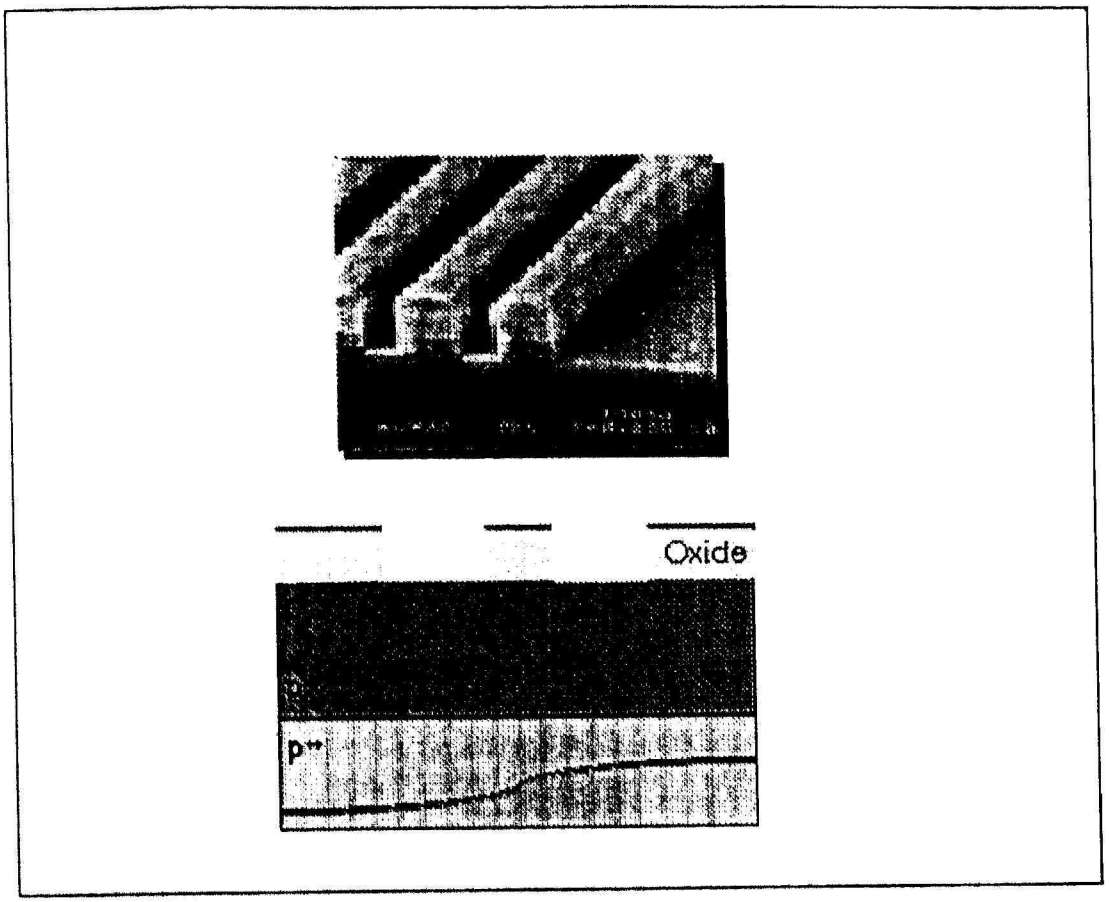
Source: Van Zant, (1997), p.33, Figure 3.2.

Figure 2.3 Crystal Growth and Wafer Preparation

Film formation processes are used for a variety of materials including: (1) epitaxial layers, (2) silicon dioxide films, (3) dielectric films, such as silicon nitride, (4) polysilicon films, and (5) metallization films. These films are used not only to build the active components, but also the interconnections and passive components in the circuit. Along with film formation, the wafers and the different deposited films often undergo an impurity doping step to modify the electrical properties of the layer, which may be thermal diffusion or ion implantation.

Then a lithographic process is used to imprint the circuit patterns, layer by layer, on the wafer. Lithography processes are used to transfer the pattern from the mask to the film surface, which is then selectively etched away to remove unwanted film or substrate regions to complete the pattern transfer. The radiation used may be optical, X-ray, electron beam (e-beam), or ion beam. Each technique involves a specialized technology. The major steps in lithography are (1) fabrication of masks (or pattern generation): and (2) transfer of the pattern to the wafer.

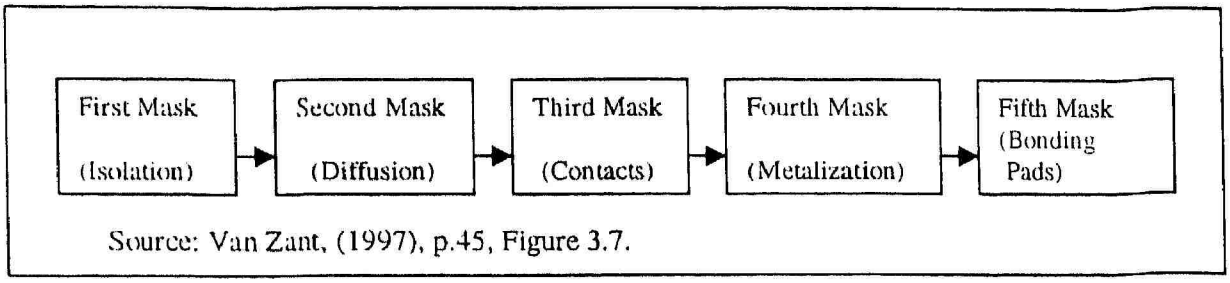
The oxide firm layer is then removed by another etching process (see Figure 2.4), revealing the original wafer surface. Impurities (doparts) is gaseous form are introduced into the wafer through a process known as diffusion. These dopart elements alter the electrical properties of the doped areas. The entire etching-diffusion process is repeated several times, the exact number depending on the complexity of the circuits being fabricated. After dissolving each layer of oxide film, a layer of silicon is deposited on the wafer surface before the entire process is



Source: Carl Johnson, (1997), p.7, Figure 1.7.

Figure 2.4 Etch and Strip

repeated. Once the final oxide layer has been etched to expose circuit contact areas, a layer of metal is applied in a process known as metal deposition, then the wafer is coated with photoresist and exposed to light. The wafer is heated by two banks of lamps, one bank of lamps above the wafer surface and the other below the surface. The temperature of the wafer is monitored by a single pyrometer that records the temperature at the wafer's center. Finally, the metal is selectively etched away so as to complete the circuit. This cycle is repeated for each mask in the set (see Figure 2.5).



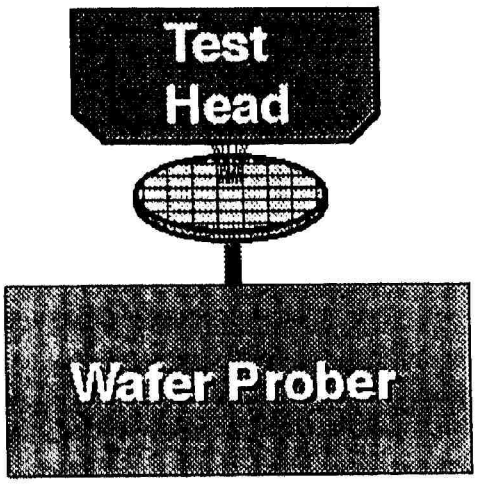
Source: Van Zant, (1997), p.45, Figure 3.7.

Figure 2.5 Mask Set

Once the processing is completed, the wafers are probed for yield, and diced into chips. These chips are encapsulated or packaged in various ways as final devices.

2.2.2 Wafer Probe

After wafer fabrication, the devices (or chips) on the wafer are complete but untested. Wafer sort (electrical testing/probe test) is performed on every chip to identify those that meet customer specifications. In order to improve wafer sort yield, dies that fail to function are put through a diagnostic test routine. This diagnostic program characterizes the failure so that specific process problem may be isolated and monitored. The information obtained by diagnostic testing can be valuable to the process engineer who is attempting to improve yields.



Source: Carl Johnson, (1997), p.18, Figure 1.18.

Figure 2.6 Wafer Probe

Dies are electrically probed in wafer form using automated test equipment and test programs written to check the electrical parameters of the device (see Figure 2.6). Electrical probe is usually done at room temperature although there may be some critical devices that require probing at high temperature. Dies that fail are inked or wafer-mapped so that they will not be assembled. Those that pass will be assembled and then every unit will be tested at final test using a similar or extended final test program from the probe program. In most cases, the test system used at probe and final test is the same so as to improve probe to final test correlation of test readings and reduce test program development time.

2.2.3 Packaging

At packaging stage, the wafer will be place into wafer carrier, the first level of protection for the wafers. It consists of a carrier body, a top cover and a bottom cover, protect the wafers from contamination and damage. There are different sizes of wafer for each wafer carrier, i.e. 200 and 300mm standard wafers, and 200 and 300mm thin wafers (see Figure 2.7, 2.8 and 2.9 respectively). Wafers will then to be shipped to respective warehouse.

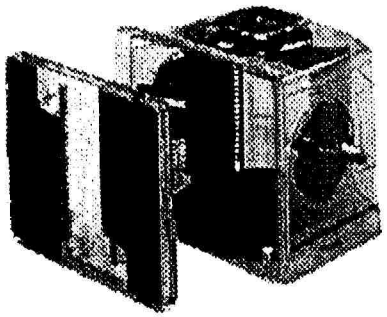


Figure 2.7 300mm Wafer Carrier (A Photo Captured at Die Cage)

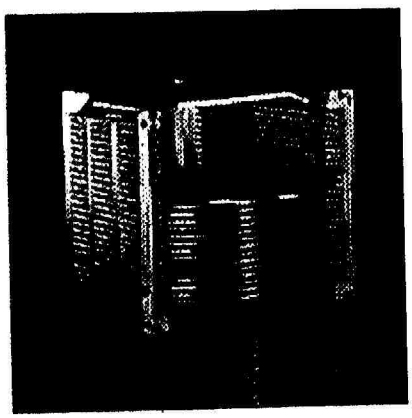


Figure 2.8 200mmWafer Carrier (A Photo Captured at Die Cage)

Figure 2.9 Packaging (A Photo Captured at Wafer Fab)

2.3 Assembly Processes

The following sections illustrate detailed assembly processes from die-preparation, wafer saw, UV irradiation, die bond, wire bond, UVO clean, mold, solder ball attach until laser mark process.

2.3.1 Die-Preparation

Wafers are collected from the die warehouse based on a daily schedule prepared by business planners and sent to the assembly floor. An operator releases piece parts for production according to part number, lot number and quantity when required per the schedule list. Wafers are then sent for wafer saw.

2.3.2 Wafer Saw

Unsawn wafers are placed onto tacky wafer mounting tape and stretched across wafer film frame. Sticky tape is mounted on wafer frames/rings. Wafers are mounted on tape, baked, then sawn and cleaned. A diamond saw typically slices the wafer into single chips. The wafer is sawn with a straight cut finish. After saw or clean, the inked chips are discarded, and the remaining chips are visually inspected under a microscope.

2.3.3 UV Irradiation

This process reduces the adhesive strength of the UV mounting tape by irradiation of ultraviolet rays to ease die pick-up at the die process (see Figure 2.10).

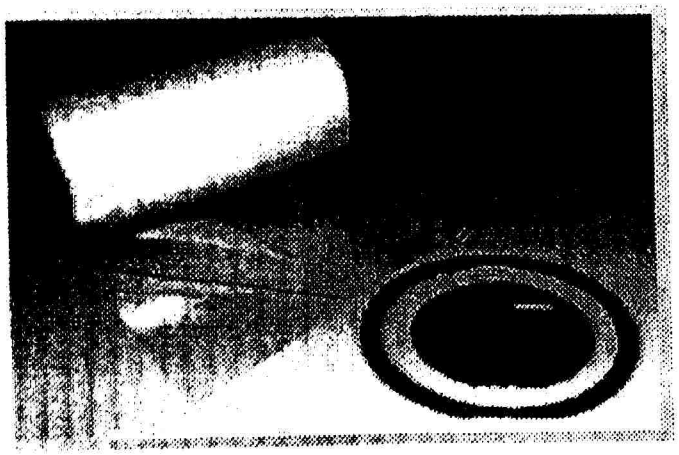
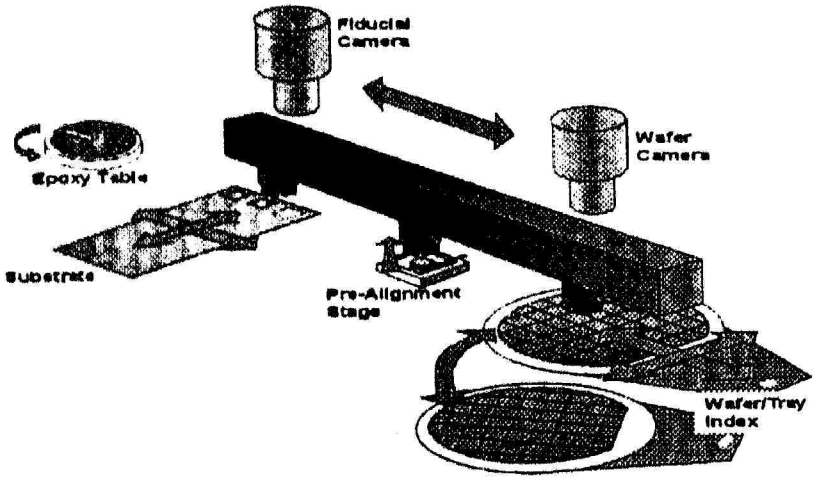


Figure 2.10 UV Mounting Tape (A Picture Captured at Assembly Floor)

2.3.4 Die Bond

This process is to perform eutectic solder and epoxy die bonding by using Foton or ESEC die bonder or Alphasem machine (see Figure 2.11). Pick-up head transfers die from wafer to pre-alignment stage. Pre-alignment stage mechanically centers die before the bonding. While bonding head picks up die at pre-alignment stage, stamping head transfers epoxy from epoxy table to the substrate prior to die attach.

The die on the flags of the lead frames must be cured to harden and strengthen the bonds. This is purely a manual in which the operator transfers a lot of magazines into an oven. The temperature and duration of cure depend on the particular products.



Source: Carl Johnson, (1997), p.20, Figure 1.20.

Figure 2.11 Die Bond Process

2.3.5 Wire Bond

A wire-bonding machine then attaches wires, a fraction of the width of a human hair, to the leads of the package (see Figure 2.12 and 2.13 respectively). Wire bonding is a process of interconnecting the chips, substrates and output pins. Typically, high purity 001" diameter gold wire is used and a ball bond is formed at one end and a stitch bond at the other. The first bonds are ball bonds on pads while the second bonds are stitch bonds on leads or post using any the three wire types. For all wire, both bonds are stitch bonds. After complete wire bonding, the lot will be sending for QA gate. QA will perform the gate inspection as per specification and sampling plan.

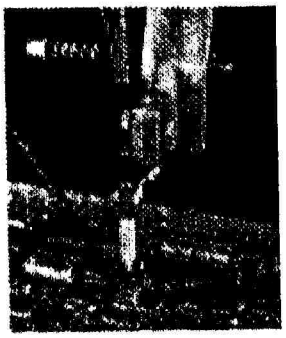


Figure 2.12 Wire Bond Machine (A Picture Captured at Assembly Floor)

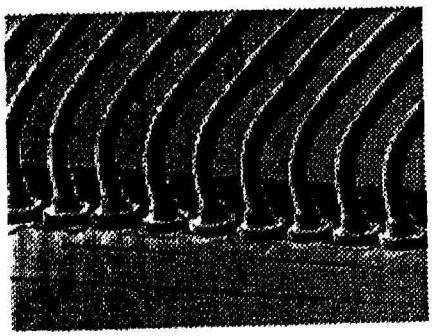


Figure 2.13 Wire Bond (A Picture Captured at Assembly Floor by Using Microscope)

2.3.6 UVO Clean

UV-Ozone cleaning is a cleaning process for devices, done after the wire bond process. This process improves die and solders mask adhesion to the mold and package integrity.

2.3.7 Mold

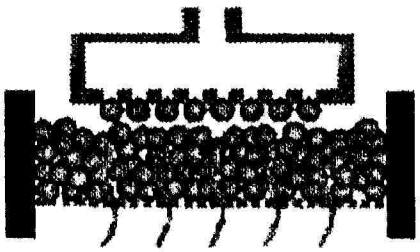
A random sample of molded strips is scanned by X-ray to ensure that the molded units are in good condition, i.e. the wire bonds are in place and sweep is within tolerable range and molds are free from bubble formations (de laminations).

The cleaning material will be place over the bottom mold surface (see Figure 2.14). Then the material will transfer to cure for 120 seconds to 300 seconds. All excess compounds are removed from the mold by scrapping with brass scraper, air gun, vacuum or brush. After mold is cleaned, material will sent for 4 hours cure.

Figure 2.14 Molding Process (A Picture Captured at Assembly Floor)

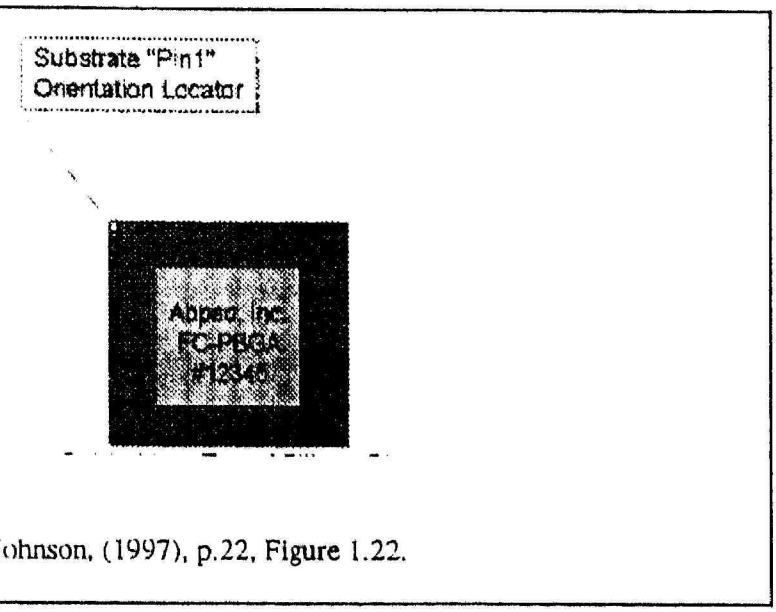
2.3.8 Solder Ball Attach and Laser Mark

Solder ball will be attach on the package and go through the furnace (see Figure 2.15). Then, the marking operation uses a laser system that transfers an ink pattern to the heatspreader. In case of heat spreader marking, an additional "Pin 1" orientation in form of 1 mm ink dot can be printed on the top (see Figure 2.16). After the solder ball attach or bump and laser mark using accel centrifugal cleaning system without CFC's for all BGA (ball grid array) packages, the units will sent for Flux cleaning. Upon completion above process, units will be pack and sent to test area.



Source: Carl Johnson, (1997), p.21, Figure 1.21.

Figure 2.15 Ball Attach



Source: Carl Johnson, (1997), p.22, Figure 1.22.

Figure 2.16 Mark

2.3.9 Final Outgoing Inspection

Before sending the completed units for testing, every unit will be visually inspected, cleaned and repaired if necessary. Operators also check all other specifications before sealing the trays in boxes, ready for the next process sequence.

2.4 Final Test Processes

At final test, various test flows are used that may include room temperature, low temperature and high temperature testing and also burn-in. The number of test insertions adopted is dependent on the device maturity, application and customer requirements. In addition to the test insertions, quality assurance

sampling is carried out to provide assurance that the devices are tested correctly. Detail of each process is described below.

2.4.1 Burn-in

After material have completed assembled, the units will sent for burn-in as per specification after test under room temperature (TOS). Burn-in is the application of thermal and electrical stresses for the purpose of inducing the failure of marginal (microelectronic) devices, those with inherent defects or defects resulting from manufacturing aberrations which cause time and stress dependent failures.

Devices are loaded into high temperature sockets, which make temporary electrical contact with the device leads, and are mounted on high temperature circuit boards with circuitry to provide the proper voltages and stimuli to the devices. The devices are isolated from one another with passive components, which limit the current each device can draw, and filter noise from voltage busses. The boards containing the devices (called Burn-in boards) are then loaded into a convection oven which elevates the temperature of the devices and provides an electrical interconnect to the power supplies and signal generators. The devices remain in the oven for an amount of time determined to induce failure in the marginal devices. As for product A, burn-in condition is temperature 100^{0}C for 40 hours with burn –in voltage PS1=5.0V and PS2 = 5.0V power supply. Burn-in will be performed on MAX oven.

igure 2.17 **Burn-in Process (A Picture Captured at Burn-in Area)**

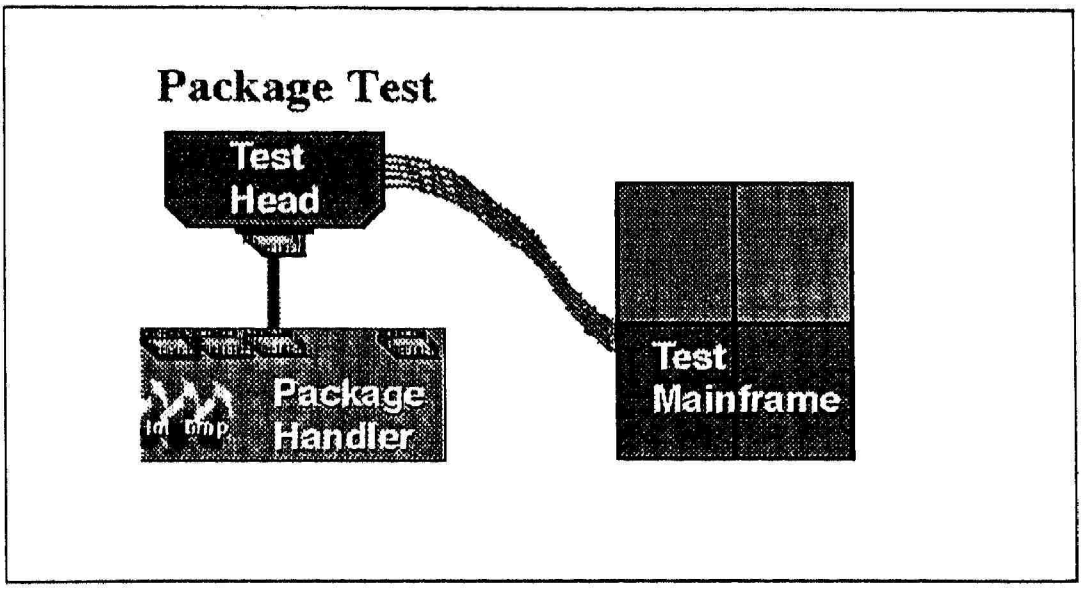
.4.2 TOS (room temperature), TLO (low temperature) and THI (high temperature)

This is the operation where all the product will undergo extensive testing t different worse case temp condition as well test condition. Normally :mperature is set at 80C for high temperature test and -5C for low temperature nd room temperature. THI and TLO inserts are referred as high and low :mperature tests respectively. Tests are usually done at tighter electrical limits ıan what is stated in customer data sheets. These differences are called guard ands. This is used to ensure that the units may not marginally pass certain test. Veek or poor products which unable to meet mentioned test conditions will be ejected.

Both high and low temperature tests have a number of tests in itself. These include tests for voltage levels, open short, margin, current and etc. ests.

Operator will load the test program at correct tester and enter data required by tester such as lot number, wafer lot, assembly back side code, operator badge number and shift. Temperature will be set at handler according to what is specified in the shop order. Operator will ensure proper bin as required by the shop order.

Testing consists of mounting chips (either wafer or packaged devices) onto automatic test equipment (ATE), applying stimuli to the input pins, and comparing responses at the output pins against expected responses.



Source: Carl Johnson, (1997), p.28, Figure 1.28.

Figure 2.18 Electrical Testing

As illustrated by Figure 2.18, the devices are connected to the tester through sockets; the socket unit is known as the test head. The devices are inserted into the test head manually or by an automatic unit known as a handler.

This handler may be mechanical or robotic, depending on the speed and complexity of the operation.

A typical test process is shown in Figure 2.19 where DUT refers to "device under test". It can be either a wafer or a package device. The tester is a computer that controls the whole test process and analyses the test results. The interface between the tester and the DUT can be either a probe card or a DUT board, depending on whether a wafer or a package device is being tested. The test program defines the input output (I/O) terminals, input stimulus, and input test vectors. The mapping file contains the inter connecting information of the DUT under a certain test specification. A standard output file provides standard output information under the given test vectors.

During testing, the tester first loads the test program file and the mapping file, and then controls the probe card or DUT board to connect the DUT to a certain topology according to the connection information contained in the mapping files. Next, the test-input vectors are applied at the input of the DUT and the tester collects the corresponding responses at the output as samples. Finally, the tester compares the output with the standard output file for fault reporting.

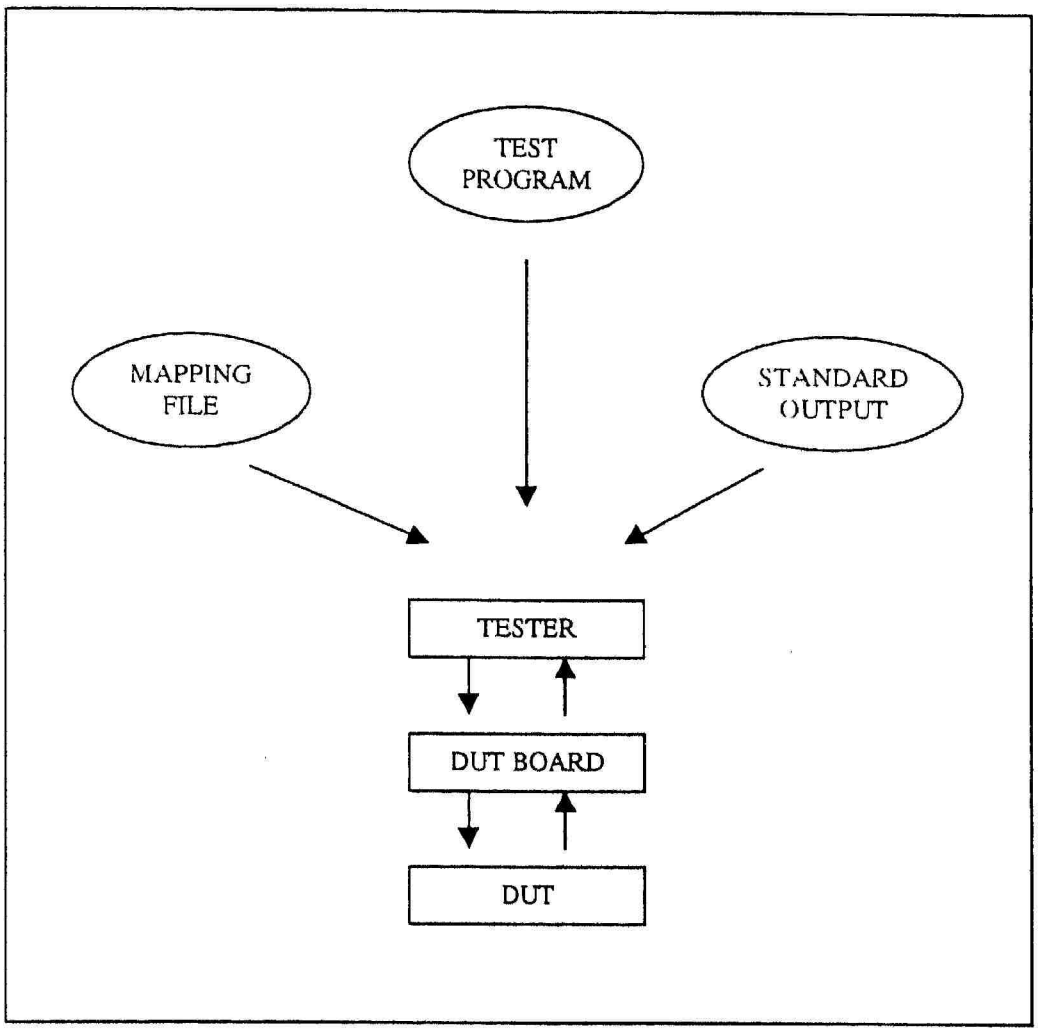


Figure 2.19 Typical Test Process

At TLO, units will be sort out into 8 bins, i.e. bin1 is good units, bin 2, 3 and 4 units are not used, bin 5,6,7 and 8 are reject units. At THI, units will be sort out by speed, i.e. bin1 is not used, bin 2 is 4 nanosecond, bin 3 is 4.4 nanosecond and bin 4 is 5 nanosecond. As for bin 5, 6, 7 and 8 are the rejected units and eventually will be scrapped.

2.4.3 Combination and Mark

There are two types of combination done at final test i.e. bin combination and lot combination. Bin combination combines different bins in a lot while lot combination combines several bins from different lots. Although several devices of different speeds are produced after speed sort, they may not necessary be marked and sold at their respective speeds. Depending on the demand for a particular speed, some device is to be downgraded from higher speed to a lower speed. Since each speed is represented by a bin number, this is called bin combination. However, the lowers speed bins are not allowed to be combined to a higher speed bin.

At combination area, the computerized combination software is developed and designed so that it is able to generate: -

- Correct device marking
- Correct Tractability Code
- Correct Combination Lot Number
- Elimination of Wrong Binning
- Fast Access to database for Traceability of Lots From Customer Return

At this process, operator will scan the bar code raw stock number, enter target device together with the speed, key in source number, moo number, woo number, assembly site (all as per shop order), scanning assembly lot number, and key in backside code. Then, operator will select the correct bin with its quantity.

Finally, operator will need to choose package requirement (dry pack or tape and reel) before print out combination and mark shop order. Upon completed combination through system, units will sent for marking.

All the device will be mark according to combined speed. In addition to speed identification, other information is also found in the marking in the devices. This includes date, device name lot sequence and others, all in code form. The actual marking is done by using a marker machine. Before a unit can mark, it has to be flamed. This is to make the surface the unit suitable for marking. If a unit is not flamed, the marking will not stick properly on the device package. A unit is flamed with a flame, which blows a jet of hydrogen flame onto the unit for a very short period of time. If the unit is flamed too long its surface will damaged. After a unit is marked, the ink needs to be cured with ultra-violet light to make if permanent. The ink can be cleaned off with acetone (a kind of alcohol) before curing.

At marking, operator will put in 3 units in the marking verification tray and make sure the unit's orientation is correct and marking position on the units is at the center on both units.

The automated parts handler moves two parts at a time from an input tube, through the laser enclosure and to the output tubes (see Figure 2.20). The tubes are automatically loaded and unloaded. Operator can access the tubes with stopping the machine processing.

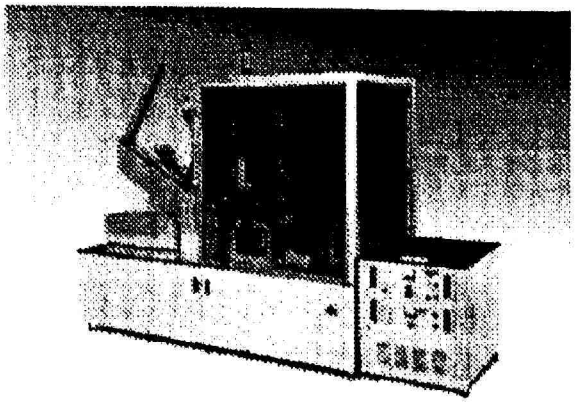
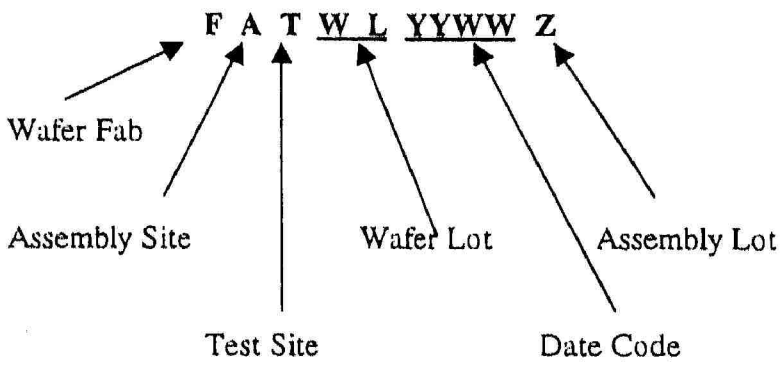


Figure 2.20 Mark Machine (A Picture Captured at Marking area)

Standard Marking For Integrated Circuits

This is applies to all Semiconductor Products Sector and outside Contract House locations. All Standard Products must be correctly identified and marked as follows (Company's Specification, 1999): -



2.4.4 Quality Control Inline

There are two types of Quality Control (QC) in-line plan. For material qualified for skip QC in-line plan (Plan A), lot number 1 to 9 will be skipped and lot number 10 is to be gated at high temperature. This sequence is repeated for lots until lot number 50 which is to be gated at low temperature. This repeated

for every 50 lots. As for normal QC in-line plan (Plan B), lot number 1 to 8 is to be gated at high temperature, lot number 9 to 12 is to be gated at low temperature. And lot number 13 to 20 is to be gated at high temperature. The sequence is repeated every 20 lots.

The operator shall load the current QC program and the test temperature per the lot sequence in the appropriate plan. If the QC sample pass, operator will print a new summary and proceed the lot. If the QC sample fails, the lot will be put on hold for engineer verification, analysis and disposition.

2.5 Final stages

Units that have passed the Quality Control (QC) inline will to final stages for further processes such as ball scan/inspection, packing and ship.

2.5.1 Ball scan/Inspection

A vision system is used together with a map to detect mechanical and physical defects of the leads such as bent coplanarity and etc.

2.5.2 Packing

After the wafer lot pass all the test inserts and also quality assurance (QA) gating, it will be packed. There is two form of finished device packaging available for customers. i.e." tape and reel " or " dry pack ". Tape and reel is a packing process where units and put into capsules which is joined as a long chain. This chain is then rolled onto a paper reel. Each reel normally contains one thousand or 500 units, depend on the package. Dry pack is an easier

process where units, which are in tray form, will be directly pack in dry static shielded bags. Units will then transport to warehouse and ready for ship.

2.6 Summary

A detailed description of the manufacturing process of integrated circuits or chips from wafer process to final test and packing has been presented. It shows that during IC manufacturing, lots are processed at different stages and are involved in a lot of process operations, and for each several machines can be used. It is pertinent to note that this study evaluates yield performance at the final test stage for different test processes and test equipment.