CHAPTER 5

CONCLUSION

Conclusion

A p-channel MOSFET with gate length of 1000 μm was successfully fabricated as the test device for the Charge Pumping Technique. The source and drain were diffused from PBF layer, which was coated on to the silicon by spin coating technique. The gate oxide was grown by dry oxidation and aluminum layer was thermally evaporated on the gate oxide to form the gate electrode. Capacitance-Voltage (C-V), Current-Voltage (I-V) and Charge Pumping (CP) measurements were done on the sample. For the C-V measurement, the oxide impurity was estimated to be in the order of 10^{11} cm^{-2} and improved to the order of 10^{10} cm^{-2} after the sample was annealed. As for the CP measurements, the interface traps density were estimated to be in the order of 10^{12} cm^{-2} before annealing and improved to the order of 10^{11} cm^{-2} after the sample went through heat treatment at source and drain reverse bias, V_R = 0.0V. However, these three measurement methods do show a common observation that contaminants exist at the Si-SiO_2 interface. These contaminants caused the difference in the results of the C-V, I-V and CP measurement before the sample was annealed. After annealing, these contaminants seem to be distributed and discharged across the channel, therefore the results are closer to the theoretical or expected results. Comparatively between the C-V measurement and the CP measurements on the analysis on the interface traps density, both also showed agreeable results on the interface impurity although both measurements settings are different from each other. For CP technique, the interface traps density can be measured across the channel by varying the source and drain reverse bias voltage.

Furthermore, if the device's operation speeds is higher than the respond time of the surface states, the CP pulse width can be narrower by increasing or decreasing the pulse duty cycle depending on which type of pulses were used. However, the accuracy and suitability of the CP measurement could not be confirmed with a commercial MOSFET as the source and back contact of the device was shorted together. This prevents the measurement of the CP current through the back contact to the device.

Further work needs to be done on the CP system, as the instruments used for this study were limited to certain range and setting. The measurements should be automated to minimum human error and should be done in an enclosed probe station to shield away from environmental effect on the measurement. From the results, fabricated device was contaminated. The fabrication steps especially in the cleaning of the device should be revised to further improve the process. A commercially fabricated device should be obtained as reference to check the accuracy of the CP system. However, this commercially fabricated device should have four terminals; gate, source, drain and back contact. Apart from that, further analysis and measurement should be carried out on the C-V method in order to extract the interface traps density at the interface of the device in order to compare with the CP measurement. This can be achieve with low frequency C-V measurement.