Development of Object Oriented Components for ATM Network Simulation with Emphasis on Switch Architecture

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GAN MENG KIAT

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ABSTRACT

Asynchronous Transfer Mode (ATM) is considered to be the foundation on which B-ISDN is to be built. It is the new generation of communication protocol that being deployed throughout the telecommunication industry. An important component of this communication networks is the ATM switch whose basic functions are to direct cells from input port to output port and to buffer cell destined to the same output port from different input port. Understanding an ATM switch before building it, is a challenging task as one must consider the design of switching architecture and cell buffering at the same time.

As the switching architecture is important, this project focuses on the development of an object-oriented simulator for simulation and prototyping of ATM switching architecture. It also focuses on the identification of functional requirements of the switch fabric at ATM layer, i.e. develops an improved architecture which considers QoS at the switch fabric, and ensures the correctness and fairness of routing within the switch fabric for ATM applications. As such, the implemented switching architecture is Banyan switching architecture. The design of switching element used in Banyan Switch includes a 2x2 crossbar switch and first-in-first-out buffers at each input controller.

Finally, object-oriented approach is proven to be the most suitable approach for the development of network simulator. Multithreading has been applied to closely simulate the real ATM switch. The results of this project clearly stated that this simulator is platform independent and can be placed into the World Wide Web easily.

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ABBREVIATIONS

AAL	ATM Adaptation Layer
ATM	Asynchronous Transfer Mode
CAC	Connection Admission Control
CDV	Cell Delay Variation
CER	Cell Error Ratio
CLR	Cell Loss Rate
CMR	Cell Misinsertion Rate
Delsi	Delphi Simulation
EFCI	Explicit Forward Congestion Indication
FIFO	First-in-first-out
GUI	Graphical User Interface
HEC	Header Error Control
IC	Input Controller
IDE	Integrated Development Environment
Max CTD	Maximum Cell Transfer Delay
MBS	Maximum Burst Size
MCR	Minimum Cell Rate
MIN	Multistage Interconnection Network
NetSim	Network Simulator
NIST	National Institute of Standards and Technology
NPC	Network Parameter Control
OAM	Operations and Maintenance
OC	Output Controller
OMNeT++	Objective Modular Network Testbed in C++
OOP	Object-Oriented Programming
OPNET	Optimised Network Engineering Tools
PARSEC	Parallel Simulation Environment for Complex System

PCR	Peak Cell Rate
PLASA	Piecewise Linear Aggregate Simulation Architecture
QoS	Quality of Service
SCR	Sustainable Cell Rate
SECBR	Severely Errored Cell Block Ration
SF	Switch Fabric
TCP/IP	Transmission Control Protocol over Internet Protocol
TCT	Total Cells Tranffered
UPC	Usage Parameter Control
VCI	Virtual channel identifier
VISTA	Configurable Visualization and Simulation Tool for ATM switches
VPI	Virtual Path Identifier