CHAPTER 1: INTRODUCTION

The main theme of this thesis is the high-speed Asynchronous Transfer Mode (ATM) network. The ATM network transmits data in small packets in fixed size of 53 bytes. Transfer rate at ATM switch can go up to as high as 2 Gbps. As a result of the very high data rates, a fast switching ATM switch is required to handle thousands up to millions of cells each second.

This thesis attempts to present a survey, and describe the design and development of a high-speed Asynchronous Transfer Mode (ATM) switching simulator using an object-oriented approach. The key area of research emphasises on the switching architecture design used in transferring ATM cells from one ATM switch to another.

1.1 Introduction to Asynchronous Transfer Mode

Asynchronous Transfer Mode (ATM) also known as cell relay, is a technology that was developed as part of the work on broadband ISDN in the 1970s and 1980s. It is a high-performance, cell-oriented switching and multiplexing technology that utilises fixed-length packets to carry different types of traffic. Technically, it can be viewed as an evolution of packet switching. Like packet switching for data (e.g., TCP/IP), ATM integrates the multiplexing and switching functions. It is well suited for bursty traffic in contrast to circuit switching and allows communications between devices that operate at different speeds. Unlike packet switching, ATM is designed for high-performance multimedia networking.

ATM technology has been implemented in a very broad range of networking devices like PC, workstation, and server network interface cards, switched-Ethernet and token-ring workgroup hubs, workgroup and campus ATM switches, ATM enterprise network switches, ATM multiplexes, ATM–edge switches, and ATM–backbone switches.

ATM is capable to be offered as an end-user service by service providers (as a basis for tariffed services) or as a networking infrastructure for these and other services. The most basic service building block is the ATM virtual circuit, which is an end-to-end connection that has defined end points and routes but does not have bandwidth dedicated to it. Bandwidth is allocated on demand by the network as users have traffic to transmit. ATM also defines various classes of service to meet a broad range of application needs [1].

1.1.1 Quality of Service

ATM Quality of Service (QoS) quality of service is part of the connection traffic contract, and it is measured by a set of performance-related parameters. The level of quality that an ATM connection requires depends on the types of traffic. QoS support is one of the key advantages of ATM compared to other transport methods. With proper QoS set up for the ATM connection, the connection can be effectively transport time-sensitive formation as well as a simple data transfer. The ATM forum defines the following QoS parameters.

Maximum Cell Transfer Delay (Max CTD)

The delay is the sum or accumulation of all delays for system. Cell Transfer Delay is contributed to by cell-propagation time, cell–switching time, and cell-transmission time.

Peak-to-peak Cell Delay Variation (CDV)

CDV is mostly related to the software aspects, such as cell scheduling, cell processing, and cell-buffering time.

Cell Loss Rate (CLR)

CLR is the result of the lost cells divided by the total number of transmitted cells. The CLR is negotiated during call-setup time. Each node in the network accepts or rejects

calls based on its own CLR data. This data may include a range of cell loss ratios numbers for connections or connection groups.

Cell Error Ratio (CER)

CER is the result of errored cells divided by the total of cells transmitted successfully and the errored cells

Severely Errored Cell Block Ration (SECBR)

SECBR is the result of errored cell blocks divided by the total number of cell blocks transmitted.

Cell Misinsertion Rate (CMR)

CMR is the result of the total misinserted cells divided by the time interval. It is measured as a rate parameter, because there are no base values as in the parameters discussed [2].

1.1.2 ATM Service Classes

ATM network is designed to transfer many different types of traffic simultaneously. The way the data flow is handled within the network depends on the characteristics of the traffic flow and the requirements of the application. For example, real-time video traffic must be delivered within minimum variation in delay.

The ATM Forum has defined four ATM Layer service classes, each with scalable (QoS) levels:

Class A

Class A is defined as Constant Bit Rate (CBR). It is used by applications that require a fixed data rate that is continuously available during the connection lifetime and a relatively tight upper bound on transfer delay. Class A traffic is low-bandwidth traffic,

i.e. highly sensitive to delay and intolerant to cell loss. Examples of CBR applications include video conferencing, interactive audio, distance learning, and video-on-demand.

Class B

Class B traffic is real-time Variable Bit Rate (rt-VBR). This category is intended for time-sensitive applications where end-to-end delay is critical. The principal difference between applications appropriate for rt-VBR and CBR is that rt-VBR applications transmit at a rate that varies with time. Equivalently, an rt-VBR can be characterised as somewhat bursty.

Class C

Class C is non-real time (nrt-VBR) traffic, where delay is not so critical. For some non-real-time applications, it is possible to characterise the expected traffic flow so that the network can provide substantially improved QoS in the areas of loss and delay. Such application (like video playback, training tapes and video mail messages) can use the nrt-VBR service. With this service, the end system will specify a peak cell rate, a sustainable or average cell rate, and a measure of how bursty or clumped the cells may be. With this information, the network can allocate resources to provide relatively low delay and minimal cell loss.

Class D

Class D traffic is split into two classes: Available Bit Rate (ABR) and Unspecified Bit Rate (UBR). These classes are for bursty LAN traffic and data that is more tolerant of delays and cell loss. UBR is a "best effort" service that does not specify bit rate or traffic parameters and has no quality of service guarantees. Originally devised as a way to make use of excess bandwidth, UBR is subject to increased cell loss and the discard of whole packets. ABR, like UBR, is also a best effort service, but differs in that it is a managed service, based on minimum cell rate (MCR) and with a low cell loss. No

delay variation guarantee is currently envisioned for either UBR or ABR service classes [3][4].

Figure 1.1 describes how a network allocates resources during a steady-state period of time and table 1.1 shows the service classification for ATM.

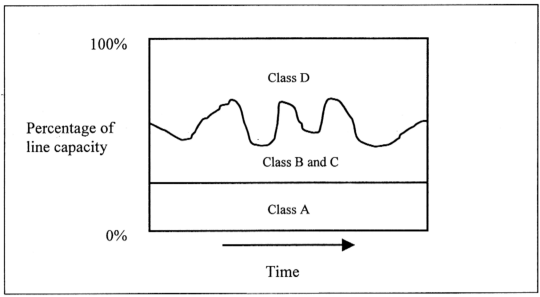

Figure 1.1: ATM Bit Rate Services

Table 1.1: ATM Service Classification

	Class A	**Class B**	**Class C**	**Class D**
Timing relation between source and destination	Required		Not required	
Bit rate	Constant	Variable		
Connection mode	Connection oriented			Connectionless
AAL protocol	AAL 1	AAL 2	AAL ¾	
			AAL 5	

1.2 Introduction to ATM Switching

The primary function for ATM switching is to accept calls from different sources and to transport them to the right destination. Various switching architectures were developed in the past for different application based modes like Synchronous Transfer Mode (STM) and packet switching. However, these switching architectures are not directly applicable for broadband ATM. There are three major factors that impact on the implementation of the ATM switching architecture

- The switch has to operate at a high-speed rate (from 150 Mbit/sec up to 600 Mbit/sec).
- The statistical behaviour of the ATM stream passing though the ATM switching system.
- The switching elements have pre-defined routing tables to minimise the complexity of single switch routing because ATM is connection oriented.

1.2.1 ATM Switching Function

ATM network defines the virtual path through different switches for the established connection. The Virtual Channel Identifier (VCI) is local to each switch port (The VCI is translated into a new value as the cell travels across an ATM switch). The switch needs to build the new ATM header containing the new VCI and possibly new Virtual Path Identifier (VPI), after that calculate the Header Error Checksum (HEC) value.

The main responsibility of ATM switching is to transport cell from an incoming logical ATM channel (inlet) to an outgoing logical ATM channel (outlet). Logical ATM channel is characterised by two identifies

- The physical inlet/outlet which is characterised by a physical port number.
- The logical channel on the physical port which is identified by the VCI and/or the VPI.

Two functions have to be implemented in the ATM switching system. The first function is the space switching function. This function allows the connection between every input and every output. Internal routing is an important aspect of space switching. The internal structure of the switch must allow connections between every input to every output.

The second function is time switching. Since ATM is working in an asynchronous mode, cells which had arrived in various time slots from the different inputs, can be delivered to different outputs in different time slots. A contention problem arises if more than two logical channels are connected to the same output at the same time slow. However, this problem is solved by the queuing function in ATM switch system [5].

1.2.2 ATM Switching Structure

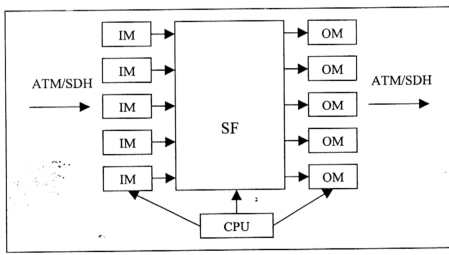

Figure 1.2: A Generic ATM Switching Structure

ATM switching consists of the following main modules, Input Module, Switch Fabric, and Output Module. The Input Module is responsible for recovering the STM cells from the incoming bit-stream. Input Module also translates VPI/VCI values and

determines the output port. The Output Module performs the inverse of the Input Module functions, mainly translation of ATM cells to the outgoing bit-stream. The switch fabric handles cell buffering, concentration and multiplexing, multicasting, broadcasting, cell discarding, and the actual cell transfer [6].

1.3 Introduction to Network Simulation

Computer Network Simulation is a valuable tool when attempting to form ideas on the correct solution for data communications needs. Complex network architectures and topologies are commonplace. With the advent of ATM high-speed networking solutions, network simulations allow designers make decisions without the need to invest in this new technology. Designers can test their new designs and carry out performance related studies using a simulation and therefore freed from the burden of the "trial and error" implementations. Huge saving can be made both in terms of investment and the cost in terms of unnecessary restructuring for experimentation.

Simulation is the basis for making decision. Decisions are formulated based on the information resulting from the simulation. The objective of simulation is to form a correct decision. A number of factors influence the probability of making a correct decision. These are summarised here as:

The level of understanding of the Problem

The problem should be well defined and manageable. A clear understanding of the problem is essential before a simulation model can be developed.

Correct Model

A software model may often be syntactically correct (i.e. compiles in software environment) but might not accurately simulate the problem area being addressed (i.e. the semantics). Any result generated from an inaccurate model will simply lead to

incorrect decisions being formulated given the problem area. It is also essential that the model is correctly designed to reflect the original objectives of the simulation.

Interpretation of Results

The simulation model simply produces output data. This data must be manipulated and interpreted by the developer. The correct interpretation of this data is dependent on the usefulness of the output data and also the user's understanding of statistical methods (e.g. variance, distribution functions) [7].

1.3.1 Advantages and Disadvantages of Simulation

The advantages of simulation are described as below:

- Economical and quick to assemble.
- Given sufficient computing resources, can do large-scale tests.
- Tests are controlled, reproducible.

However, certain problems exist with simulation too:

- Need to redo code for simulation environment.
- Simulation implementation may differ considerably from real one.
- Synthetic environment may also poorly represent real one [8].

1.3.2 Type of Simulation

There are two forms of network simulation: Analytical Modelling and Discrete Event Simulation.

Analytical Modelling is a mathematical technique that characterises a network as a set of equations. The over simplistic view of the network and the inability to simulate the dynamic nature of a computer network are the main disadvantages of this technique.

Discrete Event Simulation is a computer model of some physical system, where the state of the system is assumed to change only at discrete points in simulated time. It is the study of a complex system by computing the times that would be associated with real events in a real-life situation. This could be the average end to end delay of packets. Discrete Event Simulation has many advantages; it requires far greater processing time. Also, quite a considerable investment of time is needed to accurately simulate most models [9].

1.4 Project Objectives

The first objective of this project is to study and understand the ATM switching simulation techniques. Through the study of these techniques can improve the existing switching architectures. Numerous switching techniques have been proposed, this thesis begins with a study on the current switching techniques and their effectiveness.

The second objective which is of primary importance is the development of the ATM switching simulator itself. The simulator is developed using an object-oriented approach to take advantage of the features such as modularity, extensibility, reusability and others. Moreover, applying multithreading into a simulator design can be used to closely model the real ATM switch.

The final objective is the creation of a portable, cross-platform and web-enabled simulator.

1.5 Goals

The primary goal of this project is to create a component-based ATM switching simulator. These switching-components should be able to be integrated to form a complete ATM network topology. The ATM switching simulator shall have the following capabilities:

- Allow the multiplexing of different ATM applications over a single ATM port.

- Allow ATM cells to be routed properly to the output port.
- When two ATM cells are addressed to same output port, this simulator shall ensure fairness of switching.
- Control the transfer rate of ATM application within an ATM switch.

1.6 Report Organisation

In Chapter 2, a survey on various simulators is covered. This chapter also contains programming techniques, languages and tools that will be used in assisting the development of the system. In addition, a survey of different switching techniques used in ATM networks, different buffering and queuing schemes also had been conducted.

The details of switching functions, ATM switch architecture, and ATM traffic parameters used in the simulation model is highlighted in Chapter 3. At the end of this chapter, the considerations taken into account in designing the high performance ATM switch is also presented.

The following chapter concentrates in the design of simulation tool. In Chapter 4, an overall architecture will be shown, followed by component design, algorithm design, and others.

Chapter 5 consists of two parts, which is implementation and testing. Implementation focuses on declaration of objects and testing describes component testing, module testing, and system testing.

Finally, a conclusion for this project is provided in Chapter 6. Discussions about the strengths of the simulator, its limitations and the possibilities for future enhancements are highlighted here.

1.7 Summary

Two major roles of the ATM switch (i.e. Virtual Channel Identifier translation and switching) are presented in this chapter. The ATM switching structure, (Figure 1.2) shows the flow of the ATM signal from the input module, passing through the switching fabric and finally reaching the output module. Subsequently, the report describes on the simulation aspects and factors which influences the correct decisions of the ATM simulator. The advantages and disadvantages of the simulation and the two types of simulation: analytical modelling and discrete event simulation were also covered. At the end, a discussion on the project objectives, goals and report organisation are covered.