CHAPTER 3: SIMULATION OVERVIEW

This chapter begins with a detailed illustration about ATM switch functions and switching architectures. The Switch Function is broken down into user plane, control plane and the management plane. The ATM switch architecture gives an overview of the whole ATM structure and also provides detailed explanation on the cell switch fabric where switching is actually performed. At the end, a description of the ATM traffic parameters and the simulation model are discussed.

3.1 Switch Functions

In ATM switch, switching functions can be examined in the context of the three planes of the ATM model, i.e. user plane, control plane, and management plane.

3.1.1 User Plane

In user plane, the main function for ATM switch is to relay user data cells from input ports to the appropriate output ports. Only 5 bytes cell header will be processed by the switch and the 48 bytes payload is carried transparently. Virtual Path Identifier/Virtual Channel Identifier (VPI/VCI) is used to route the cells to the appropriate output ports. User plane function can be divided into three functional blocks: Input module, output module and the cell switch fabric

3.1.2 Control Plane

The main function in control plane is to establish and control the Virtual Path and Virtual Channel connections. Information in control cells payload is not transparent to the network. The switch identifies signalling cell, and even generates some itself. The Connection Admission Control (CAC) performs major signalling functions. Signalling information may/may not pass through the cell switch fabric, or may be exchanged through a signalling network such as SS7.

3.1.3 Management Plane

Major operations of management plane are fault management functions, configuration management functions, performance management functions, security management functions accounting management, and traffic management. These functions can be represented as being performed by the functional block Switch Management. The Switch Management is responsible for supporting the ATM layer Operations and Maintenance (OAM) procedures. OAM cells may be recognised and processed by the ATM switch [23].

3.2 ATM Switch Architecture

ATM switching architecture includes a few elements. There are input modules, output modules cell switch fabric, connection admission control, and switch management. This switching model is shown in Figure 3.1.

3.2.1 Input Module

ATM input module determines the incoming signal and extracts the ATM cell stream. This involves signal conversion and recovery, processing cell overhead, and cell delineation and rate decoupling. The following functions should be performed for input module.

- Header error checking using Header Error Control (HEC) field.
- Validation and translation of VPI/VCI.
- Determination of the destination output port.
- Passing signalling cell to Congestion Admission Control (CAC)
- Passing Operations and maintenance (OAM) cell to switch Management.
- Usage parameter control/network parameter control (UPC/NPC) for each VPC/VCC.
- Adding internal tag containing internal routing and performance monitoring information for use within the switch only.

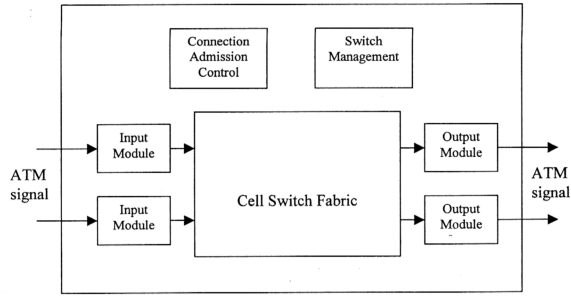

Figure 3.1: ATM Switching Model

3.2.2 Output Module

The function of output module is preparing AM cell streams for physical transmission. It is basically doing the reverse processes of the input module like:

- Removing and processing internal tag.
- Possible translation of VPI/VCI.
- Possible mixing of cells from Switch Management and CAC with outgoing cell streams.
- Cell rate decoupling.
- Mapping cells to appropriate payloads and generate the overhead.
- Conversion of digital bitstream to optical signal.
- Generating Header Error Control (HEC) field.

3.2.3 Cell Switch Fabric

The cell switch fabric consists of input controller (IC), switching element, and the output controller (OC). The input and output controller handle the communication

between switching element, also input and output modules. The switching element routes the cells from an input port to an appropriate output according to the routing information in cell header. A routing table provides an association between the incoming and outgoing links for each connection is maintained in the switching node [6][23].

The functions of cell switch fabric can be categorised as:

- Cell buffering.
- Cell routing.
- Traffic concentration and multiplexing.
- Multicasting and Broadcasting.
- Redundancy for fault tolerance.
- Cell scheduling base on delay priorities
- Congestion monitoring and activation of Explicit Forward congestion Indication (EFCI).

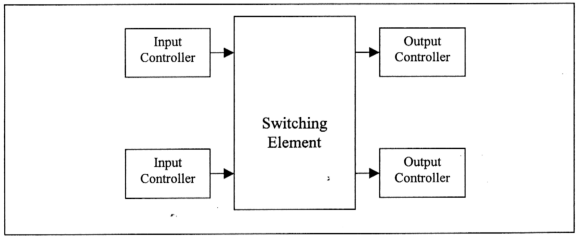

Figure 3.2: Cell Switch Fabric [6]

Cell Buffering

In ATM switch, arriving cell may be aligned in time by means of singe-cell buffers. Cell buffering may be necessary since the cells may be addressed to the same output

simultaneously. The switch may buffer cells in input controller, cell switch fabric, output controller, or use a combination of all. Output buffering is desirable from a performance point of view, the hardware requirements on this method are much larger than input buffering [6][23].

Cell Routing

Cell routing mechanism transfers the cells from the input port to the output port. The input module attaches a routing tag to each cell, and the switch fabric routes the arriving cells from its input port to the appropriate output port. It may be necessary to discards. Cell transfer can be achieved with one large switching element or with several smaller interconnected switches [6][23].

Concentration and Multiplexing

Traffic needs to be concentrated at the inputs of the switching fabric to better utilise the incoming link connected to the switch. The concentrator aggregates the lower variable bit rate traffic into higher bit rate for the switching matrix to perform the switch at standard interface speed. The concentration is highly correlated with the traffic characteristics, so it needs to be dynamically configured. The concentrator can also aid in dynamic traffic distribution to multiple routing and buffering planes, and duplication of traffic for fault tolerance. At the outputs of the routing and buffering fabric, traffic can be expanded and redundant traffic can be combined [23].

Multicasting and Broadcasting

Multicasting is the term used when a cell is transmitted to several outputs, while broadcasting refer to the transmission of a cell to all outputs. Both can either be performed directly in the switching elements or by inserting a copy network in front of the switch fabric. A copy network makes several copies to the multicasted/broadcasted cell and assures that the copies are routed to the appropriate outputs [6].

3.2.4 Connection Admission Control (CAC)

Connection Admission Control responsible for major signalling functions including establishes, modifies, and terminates virtual path/ virtual channel connections. The functions can be illustrated as below.

- High level signalling.
- Signalling ATM Adaptation layer (AAL) functions to interpret or generate signalling cells.
- Interface with a signalling network.
- Renegotiations with users to change established VPCs/VCCs.
- Allocation of switch resources for VPCs/VCCs, including route selection.
- Admission/rejection decisions for requested VPCs/VCCs.
- Generation of UPC/NPC parameters.

CAC can be either placed centralised or distributed to the blocks of input modules. In the former case, a single processing unit would receive signalling cells from the input modules, interpret them, and perform admission decisions and resource allocation decisions for all connections in the switch. In the later case, all the CAC located at each input modules has a smaller number of input ports. This approach divides the job among the various CACs and performs them in parallel, thus solves the connection processing bottleneck problem. However, it is more difficult to implement compare to centralised CACs.

3.2.5 Switch Management

Functions of Switch management are

- Handle the physical layer OAM, ATM layer OAM
- Configuration management of switching elements
- Security control for the switch database
- Usage measurements of the switch resources, traffic management,
- Administration of a management information base,

- Customer-network management, interface with operations systems
- Support of network management.

Like CAC, switch management might be centralised or distributed among input modules. Again, a distributed switch management solves the performance bottleneck problem but a lot of co-ordination will be required. Each distributed input module switch management unit can monitor the incoming user data cell streams to performance accounting and performance measurement. Output module switch management units can also monitor outgoing cell streams [23].

3.3 ATM Traffic Parameters

When an ATM source sends ATM cell traffic to its corresponding ATM destination over the network, the traffic characteristics are described or specified by source traffic parameters. These traffic parameters are the values that can indicate the nature of the source-traffic characteristics and they includes Peak Cell Rate (PCR), *Sustainable Cell Rate* (SCR), *Maximum Burst Size* (MBS), *Minimum Cell rate* (MCR), and others.

3.3.1 Peak Cell Rate (PCR)

PCR defines an upper bound on the traffic that can be submitted by a source on an ATM connection. PCR is equal to the inverse of the minimum cell inter-arrival time T.

$$PCR = 1/T$$

3.3.2 Sustainable Cell Rate (SCR)

SCR is the average maximum rate which measurement based on a longer time scale than used for PCR. SCR is needed to specify a VBR source. It enables network to allocate resources efficiently among a number of VBR sources without dedicating the amount of resources required to support a constant PCR rate. The SCR is only useful if SCR < PCR.

3.3.3 Maximum Burst Size (MBS)

MBS is the maximum number of cells that can be sent continuously at the peak cell rate. If cells are presented to the network in clumps equal to the MBS, then the idle gap between clumps must be sufficient so that the overall rate does not exceed the SCR.

3.3.4 Minimum Cell Rate (MCR)

MCR defines the minimum commitment requested of the network. It is used with the ABR service. The quantity (PCR – MCR) represents an elastic component of data flow for which the network provides only the assurance that this capacity will be shared fairly among the ABR flows.

3.4 Switch Architecture: Impact on Traffic Handling

The performance an application requires from ATM network can be defined in terms of the following parameters.

- Throughput – bits per second delivered to the application.
- Latency – total of the transmission delay, propagation delay, and queuing delay through each network element or switch.
- Jitter – variation of delay, or the variation in the intercell arrival of consecutive cell. Some application are very sensitive to jitter such as voice.
- Cell loss – cell loss already described in section 1.1.1. TCP data services can recover from packet loss and use it for gaining information on the congestive state of the network. Nevertheless, packet retransmission caused by cell loss can seriously affect application throughput [34].

The design of the ATM switch used to create ATM network will have a major impact on the network's ability to support simultaneously the different ATM service class.

Throughput/Cell Lost

For a switch to ensure that it maximises throughput and minimises the cell loss, a non-blocking design should be used. A switch must not loose any cells in the traffic switched to each output. If the traffic is less than or equal to physical capacity of the port, a non-blocking switch should exhibit no loss when handling full rate input load if the traffic pattern is congested.

It is also important that the traffic on a congested port does not interfere with traffic on a non-congested port. Input buffered switches can suffer what is known as head-of-line blocking.

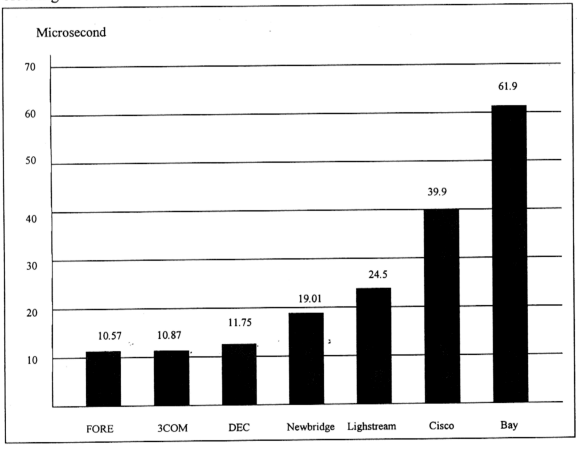

Figure 3.3: Latency per Port [34]

Latency/Jitter

Many applications require that latency added by the switch be minimised. Low latency also delivers low jitter for those applications sensitive to jitter. Figure 3.3 illustrates the latency through a switch is significantly influenced by the switches internal design.

3.5 Switching Model

This subsection gives an idea regarding the whole simulation environment for this project. ATM Network Topology describes how ATM switch is connected in the ATM network environment. Besides, it also gives a description on the basic simulator model: Banyan Switching.

On top of that, this model describes the Buffering in ATM switch and the decision for selecting the cell to transmit when there are two cells addressed to same output outlet. The ways of implementing multithreading in ATM network environment will also be discussed.

3.5.1 ATM Network Topology

This simulator focuses on the development of 4 ports or 8 ports ATM switching which simulate the Banyan switching architecture. Each port may be connected to a link where the link will be further connected to either another ATM switch or an end system. An end system might have several applications. Each application is uniquely identify by the value of VPI/VCI. Hence, a link might have only one ATM application or several ATM applications might be multiplexed together through that link.

3.5.2 Banyan 4x4 and Banyan 8x8 Switching

For Banyan NxN switch architecture, the number of stages can be determined by

$$s = \log_2 N$$

and the number of switching elements (c) within a stage is

$$c = N/2$$

Finally, the total number of switching elements (t) for a Banyan NxN switch is

$$t = sc$$

This simulation model simulates both Banyan 4x4 and Banyan 8x8 switches. For Banyan 4x4 switch, it consists of 2 stages, and each stage consists of 4 input buffers. The incoming ATM cells will be first placed into the input buffers for switching element in stage 1, these cells will be switched to the intermediate buffers between switching elements in stage 1 and stage2. At the output of the last stage, there are 4 output buffers where all the switched cells will be placed in here before transmitted through the link component. For Banyan 8x8 switch, it consists of 3 stages and each stage consists of 8 input buffers. Again, all the incoming cells will be placed in those buffers before internal switching is performed within an individual switching element. Finally, all the switched ATM cells will be placed in the output buffers before transmitted to the link components.

3.5.3 Buffering

As mentioned in the sub-section above that a switching element consists of two input buffers and two output buffers. Input buffer and output buffer for switching element at stage n+1 is the output buffer of switching element at stage n and input buffer for switching element at stage n+2. Cells inserted into buffer will be placed in First Come First Serve (or first in first out, FIFO) basis and the cell selected from each buffer is the head-of-line cell of that buffer.

The buffer described is a fix size buffer. All the buffers within an ATM switch have same size. Discarding of cell only happen at input buffers and output buffers to the Switch (not switching elements) which is connected to the outside links. This situation

occurs when input buffer to switch is full while the incoming link still sending in the cell or the outgoing link is too slow when the output buffer is full.

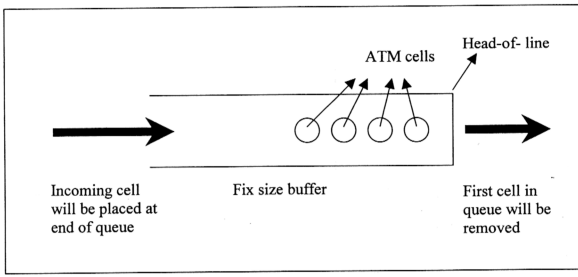

Figure 3.4: First Come Fist Serve Buffer

3.5.4 Switching

A routing table will be created once the network topology is set. All the information for ATM applications, which will be switched through that ATM switch, will be stored in this table. When performing switching for an ATM cell, the output port for that cell will be determined by that routing table. For switching within a switching element, the output buffer will be checked first. If the buffer is full, the operation will be stopped.

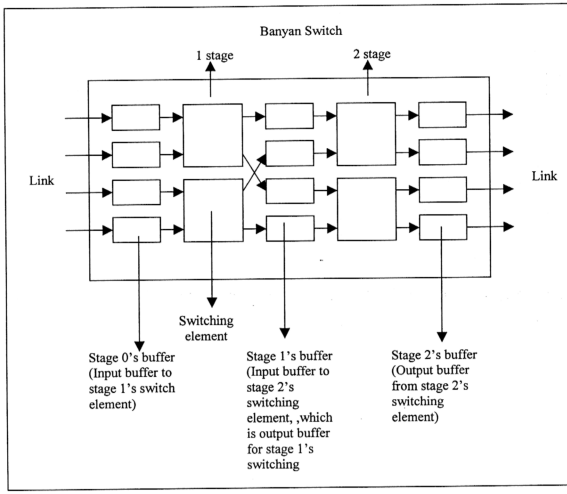

Figure 3.5: Example of Simulator for Banyan 4x4

3.5.5 Cell Selection Decision for Switching

ABR traffic defines MCR and PCR to control the cell transfer rate so that it would not falls below MCR value and also would not exceed PCR value. ATM switch operates in high-speed when compare to the link's transmission rate, as a result the switch is capable to fulfil the MCR value. However, two questions arise. Firstly, if there is an internal conflict when two ATM applications from two different inlets are addressed to same outlet, one of the ATM cells will be blocked. If no proper control over decision for selecting cell for transmitting, there is a chance for that cell to be blocked forever and causing the transfer rate for that ATM application flow below MCR value. In this situation, a simple round-robin method for switching decision might not be enough or

fairness to these ATM applications. Secondly, if there is no proper control over switching decision, there is another chance for the ATM application's transfer rate to grow beyond PCR value. It seems like more efficiency when cell transfer rate exceed PCR value, but this might causes the congestion in output buffer or produces another congestion in the input buffer for the connected ATM switch.

As a result from above, an ATM cell for ABR traffic is not necessary to be switched even when there is no internal conflict or the destination buffer is not full. Before switching a cell through a switching element, the PCR, MCR and the total cells transferred (TCT) within current second will be considered. Both PCR and MCR values will be converted from *bits/second* to *cells/second* to ease the calculation, i.e.

$$PCR_{in\ cells/second} = round\ (PCR_{in\ bits/second} / (53 \times 8))$$

$$MCR_{in\ cells/second} = round\ (MCR_{in\ bits/second} / (53 \times 8))$$

If two ABR cells in two different inlets are addressed to the same outlet in the following TCT values:

- When both TCT values are under MCR, then the cell with lower TCT/MCR value is selected for transmitting and other is blocked.
- When only one of the TCT values are below MCR, then that cell will be selected for transmitting.
- When both TCT value are in between MCR and PCR, then the cell with lower TCT/PCR value is selected for transmitting
- When the TCT value of either one is exceeds PCR, that cell will not be selected for transmitting. In this case, neither one cell might be selected for transmitting when both TCT values exceed PCR.

Every time when the cell is transmitted, the TCT value is increased by one. Table 3.1 gives a summary for cell selection decision.

Table 3.1: Criteria for Selecting ATM cell for transmission

Upper inlet cell (u)	Lower inlet cell (i)	Decision
$TCT_u < MCR_u$	$TCT_i < MCR_i$	Select cell with lower TCT/MCR value
$TCT_u >= MCR_u$	$TCT_i < MCR_i$	Select i
$TCT_u < MCR_u$	$TCT_i >= MCR_i$	Select u
$MCR_u <= TCT_u < PCT_u$	$MCR_i <= TCT_i < PCT_i$	Select cell with lower TCT/PCR value
$TCT_u >= PCR_u$	$MCR_i <= TCT_i < PCT_i$	Select i
$MCR_u <= TCT_u < PCT_u$	$TCT_i >= PCR_i$	Select u
$TCT_u >= PCR_u$	$TCT_i >= PCR_i$	Neither one is selected

Initially, the TCT value will be zero, every time when a cell is transmitted through the switching element, the TCT value is increased by one. After one second, TCT value will be reset to zero again. Assuming that the ATM switch is fast enough compare to external physical link, this approach confirms with fairness and guarantees that the ABR cell will be switched with the transfer rate greater or equal to MCR and lower or equal to PCR.

3.5.6 Multithreading

One of the interested part for this model is multithreading. Every component in the network is a single thread and all of them can run simultaneously. The speed of operation for each component is controlled under the general clock. For example, there might be two switches existing in the network environment and both of them might have different speeds.

3.6 Summary

The ATM switch functions can be viewed from three separate ATM planes. Each of the planes has different roles. On the other hand, the ATM switch architecture consists of several parts, which includes congestion admission control, switch management,

input module, cell switch fabric and the output module. ATM cells flow from the incoming link to the input module, passing through the cell switch fabric and the output module, and then finally into the outgoing link. For the proposed simulation model, the project has focused primarily on the switching within the ATM switch itself. As a result, congestion admission control and switch management are not within the scope of this project. However, ATM traffic parameters are of concern, because they play an important role in ensuring QoS. Lastly, the chapter concludes by presenting an overview of stimulator model to be designed.