References

Chapter 2

[1] D. O. Hebb, *The organization of behavior: A neuropsychological theory*, Wiley edition, New York, 1949.

[2] B. G. Cragg,, H. N. V. *Temperley, Electroenceph. Clin. Neurophysiol.*, **6**, 85, 1954.

[3] W. A. Little, "The existence of persistent States in the Brain," *Math. Biosci.*, **19**, 101, 1974.

[4] J. J. Hopfield, "Neural Networks and Physical Systems with Emergent Collective Computational Abilities," *Proc. Natl. Acad. Sci.* USA **79**, 2554, 1982.

[5] J. J. Hopfied, "Artificial Neural Networks," *IEEE Circuits and Devices Magazine*, 8755-3996 September 1988.

[6] H. Gutfreund, D. J. Amit, H. Sompolinsky, *Ann. Phys.*, N. Y. 173, **30**, 1987.

[7] E. Gardner, *J. Phys.* A21, 257, 1988.

[8] E. R. Kandel, *Sci. Am.*, 241, **60**, 1979.

[10] J. J. Hopfield, "Artificial Neural Networks," *IEEE Circuits and devices magazine*, pp. 3-9, September 1988.

[11] J. J. Hopfield and D. W. Tank, *Biol. Cybern.*, **52**, 141, 1985.

[12] D. J. Amit, H. Gutfreund, and H. Sompolinsky, *Ann. Phys.*, N. Y. 173, **30**, 1987.

[13] D. L. Stein, Spin glass and Biology, Directions in Condensed Matter Physics, **vol. 6**, Chap. 1, H. Gutfreund, *The Physics of neural networks*, World Scientific, 1992.

[14] S. Kirkpatrick and D. Sherrington, *Phys. Rev.*, B **17**, 4384, 1978.

[15] T. Geszti, *Physical Models of Neural Networks*, World Scientific, 1990.

[16] D. C. Mattis, *Phys. Lett.*, **56A**, 421, 1976.

[17] S. Kirkpatrick and D. Sherrington, *Phys. Rev.*, **B17**, 983, 1978.

[18] R. Meir and E. Domany, *Phys. Rev.* **A37**, 2660, 1988.

[19] E. Gardner, "The space of interactions in neural network models," *J. Phys. A: Math. Gen.* **21**, pp. 257-270, 1988.

[20] G. Mahler, V. A. Weberruß, *Quantum Networks, Dynamics of Open Nanostructures*, Springer-Verlag, 1995.

[21] W. S. McCulloch, W. Pitts, "A logical Calculus of the Ideas Immanent in Nervous Activity," *Bull. of Math. Biophys*, 115, 1943.

[22] E. R. Caianiello, "Outline of a theory of Thought Processes and thinking machine," *J. Theo. Biol.*, **1**, 204, 1961.

[23] F. Rosenblatt, *Principles of Neurodynamics, Spartan*, New York, 1962.

[24] H. D. Block, "The perceptron: A model for Brain functioning," *Rev. Mod. Phys.* **34**, 123, 1962.

[25] M. Minsky, S. Papert: Perceptron, *An introduction to Computational Geometry*, MIT Press, Cambridge, 1969.

[26] P. Werbos, Beyond Regression: *New tools for prediction and Analysis in the behavioral science*, Ph.D. thesis, Harvard University, 1974.

[27] W. A. Little, G. L. Show, "Analytic Study of the memory Capacity of a neural Network," *Math. Biosci.*, **39**, 281, 1978.

[28] D. B. Parker, "Learning-Logic: *Casting the cortex of the Human Brain in Silicon*," MIT Tech. Rep. TR47, 1985.

[29] D. E. Rumelhart, G. E. Hinton, R. J. Williams, "Learning Representations by Back-Propagation errors," *Nature* 323-533, 1986.
[30] Okajima, K., Tanaka, S., Fujiwara, S., "A heteroassociative memory network with feedback connection," *Proceedings of the IEEE First International Conference on Neural Networks*, M. Caudill and C. Butler, eds, **vol. II**, pp. 711-718, San Diego, 1987.
[31] Hassoun M. H., "Adaptive dynamic heteroassociative neural memories for pattern classification," *Proc. of the SPIE, Optical Pattern Recongnition*, 1053, 75-83, 1989.
[32] Hassoun M. H., Dynamic heteroassociative neural memories, *Neural Networks*, 2(4), 275-287, 1989.
[33] Leung, C. S., and Cheung, K. F., "Householder encoding for discrete bidirectional associative memory," *Proc. of the IJCNN*, **vol. 1**, pp. 237-241, IEEE, New York, 1991.
[34] Kosko, B., "Adaptive bidirectional associative memories," *Applied Optics*, **26**, 4947-4960, 1987.
[35] Kosko, B., "Bidirectional Associative Memories," *IEEE Trans. On Sys.*, Man and Cybernetics, SMC-**18**, 49-60, 1988.
[36] Hassoun M. H., *Fundamentals of Artificial Neural Networks*, The MIT Press, Cambridge, Massachusetts, London, England, 1995.
[37] Wang, C., *A robust System for Automated Decomposition of the Electromyogram Utilising a Neural Network Architecture*, Ph.D. dissertation, Department of Electrical and Computer Engineering, Wayne State University, Detroit, Mich. USA. 1991.
[38] Simpson, P. K., "Higher-ordered and interconnected bidirectional associative memory," *IEEE Trans. On Systems, Man and Cybernetics*, **20(3)**, 637-653, 1990.
[39] Wang, Y. F., Cruz, J. B., Jr., Mulligan, J. H., Jr., Two coding Strategies for bidirectional associative memory, *IEEE Trans. On Neural Networks*, **1(1)**, 81-92, 1990.

Chapter 3

[1] J. M. J. Murre, "Transputters and Neural Networks: An analysis of implementation constraints and performance," *IEEE Trans. on Neural Networks*, **4(2)**, 284-292, March 1993.
[2] J. Wawrzynek et al., "The design of a Neuro-Microprocessor," *IEEE Trans. On Neural Networks* **4(3)**, 394-399, May 1993.
[3] T. Nordstrom and B. Svensson, "Using and Designing massively parallel computers for Artificial Neural Networks," *Optics Letters*, **16(8)**, 611-63, 1991.
[4] K. A. Grasjki, Neurocomputing using the MasPar MP-1, In K. W. Przytula and V. K. Prasanna, eds., *Parallel Digital Implementation of Neural Networks*, Prentice Hall, Englewoods Cliffs, NJ, pp. 51-76, 1992.
[5] *DARPA Neural network Study*, pp.34 (figure 2.14-15), pp.330 (figure 28.5), AFCEA International Press, Nov. 1988.
[6] H.P. Graph, "A Reconfigurable CMOS Neural Network," *Digest of Technical Papers of the int. Solid State Circuits Conf.*, **vol.33**, pp144, San Francisco, Feb. 1990.
[7] J. B. Theeten et al., "The L-Neuro-Chip: A Digital VLSI With On-Chip Learning Mechanism," *Proc. Int. Neural Network Conf.*, pp. 593-596, Kluwer Academic Publishers, July 1990.
[8] D. Hammerstrom, E. Means, "System Design for A Second Generation Neurocomputer," *Proc. IJCNN*-90, **vol. II**, pp. 80-83, LEA Publishers, Jan. 1990.
[9] M. Yasunaga et al., Design, "Fabrication And Evaluation Of A 5-Inch Wafer Scale Neural Network LSI Composed of 57644 Digital Neurons," *Proc. Of the IJCNN*-90, **vol. II**, pp. 527-535, San Diego, June 1990.

[10] A. Chiang et al., "A programmable CCD Signal Processor," *Digest of technical papers of the int. Solid State Circuits Conf.*, **vol.33**, pp. 146,San Francisco, Feb. 1990.
[11] M. Holler et al., "An Electrically Trainable Artificial Neural Network (ETANN) with 10240 Floating Gate Synapses," *Proceedings of the IJCNN*-89, pp. 11-191, Washington DC, June 1989.
[12] H. P. Graph at al., "VLSI Implementation of Neural Network Memory with Several Hundreds of Neurons," *AIP Cof. Proc. Neural Networks for Computing*, Snowbird, Utah, 1986.
[13] C. A. Mead et al., "VLSI-Architectures for implementation of Neural Networks," California Institute of Technology, Pasadena, USA, *AIP Conf. Proc. Neural Networks for Computing*, Snowbird, Utah, 1986.
[14] A. P. Thakoor et al., "Electronic Neural Network with optically modulated Variable Strength. Resistive a-Si:H Interconnects for Analogue Computation," *MRS Spring Meeting*, paper E 7.5 , Reno, Nevada, 1988.
[15] M. Misra, V. K. Prasanna, "Implementation of Neural Networks on Massive Memory Organisations," *IEEE Trans. On Circuits and Systems-II, Analogue and Digital Signal Processing*, **39(7)**, pp.476-480, July 1992.
[16] J. L. Meador et al., "Programmable Impulse Neural Circuits," *IEEE Trans. On Neural Networks*, **2(1)**, pp.101-109, January 1991.
[17] A. F. Murray, A. V. W. Smith, "Asynchronous Arithmetic for VLSI Neural Systems," *Electronics Letters*, **23(12)**, pp. 642-643, June 1987.
[18] A. F. Murray, A. V. W. Smith, "A novel Computational and Signalling Method for VLSI Neural Networks using Pulse Stream Arithmetic," *IEEE Journal of Solid State Circuits and Systems*, **23 (3)**, pp. 688-697, 1988.
[19] T. D. Chieuh, R. M. Goodman, "VLSI Implementation of a High-Capacity Neural Network Associative Memory, Advances in Neural Information Processing Systems", **2**, D. S. Touretzky, ed. Morgan Kaufmann, San Mateo, CA, pp. 793-800.
[20] A. F. Murray et al., "Pulsed Silicon Neural Networks," from *of VLSI Design Neural Networks*, Edited by U. Ramacher & U. Ruckert Kluwer Academic Publishers, pp 103-123, 1991.
[21] K. A. Boahen et al., "A Heteroassociative Memory Using Current-Mode MOS Analogue VLSI Circuits," *IEEE Trans. On Circuits and Systems*, **36(5)**, pp.747-755, May 1989.
[22] M. Verleysen, P. Jespers, *Precision of Computations in Analogue Neural Networks*, chapt. 4.
[23] J. J. Hopfield, "Artificial Neural Networks", *IEEE circuits and devices magazine*, pp.3-9, September 1988.
[24] S. Y. Kung, "*Digital Neural Networks*, Prentice Hall Inc, Englewood Cliffs, NJ07632, 1993.
[25] H. T. Kung and C. E. Leiserson, *Systolic arrays (for VLSI). In Sparse Matrix Symposium*, pp. 256-282, SIAM, 1978.
[26] H. T. Kung, *Why systolic architectures, IEEE computer*, **15(1)**, Jan 1982.
[27] M. Marchesi, G. Orlandi, F. Piazza, A. Uncini, *International Neural Networks Conference*, Paris, France, 1990.
[28] S. Eun et al., Systolic Array algorithm for the Hopfield Neural Network Guaranteeing convergence, *Electronic letters*, pp. 609-610. **29(7)**, April 1993.
[29] C. Lehmann et al., "A generic systolic array building block for neural networks with on chip learning, *IEEE Trans. On neural networks*, **4(3)**, pp.400-407, May 1993.

[30] S. Jones et al., "*Toroidal Neural Network: Architecture and processor Granularity Issues,* from, *VLSI Design of Neural Networks*, Edited by U. Ramacher and U. Ruckert, Kluwer Academic Publishers, pp.229-253. 1991.
[31] B. Raggad, B. Jin, "*A reconfigurable Architecture for a VLSI implementation of artificial neural Networks, A VLSI design of a basic neural unit*".
[32] Y. c. Lim and B. Liu, "Design of cascade from FIR filters with discrete valued coefficients, *IEEE Trans. Acoust. Sp. Sig. Proc*, **vol. 36**, pp. 1735-1739, 1988.
[33] B. A. White, M. I. Elmasry, "The digi-neocognitron: a digital neocognitron neural network model for VLSI", *IEEE Trans. Neural Networks*, **vol. 3**, pp. 73-85, 1992.
[34] M. Marchesi, G. Orlandi, Fast Neural Networks Without Multipliers, *IEEE transactions on neural Networks*, **vol. 4**, No. 1, January 1993.
[35] M. Marchesi, G. Orlandi, F. Piazza, and A. Uncini, Multi-layer perceptrons with discrete weights, in *Proc. IEEE IJCNN*, **vol. II**, pp. 623-630, San Diego, CA. 1990.
[36] Kuniharu Uchimura, Osamu Saito, Yoshihito Amemiya, "A High-Speed Digital Neural Network Chip with Low-Power Chain-Reaction Architecture," *IEEE Journal of Solid State Circuits*, **vol. 27**, No. 12, December 1992.
[37] Mohamad H. Hassoun, *Fundamentals of Artificial Neural Networks*, The MIT Press, Cambridge, Massachusetts, London, England, 1995.
[38] Vladimir Bochev, "Distributed Arithmetic Implementation of Artificial Neural Networks", *IEEE Transaction on Signal Processing*, **vol. 41**, No 5, May 1993.
[39] T. Watanaba, K. Katsutaka, M. Aoki, A single 1.5-V "Digital Chip for a 10^6 Synapse Natural Network, *IEEE transaction on Neural Networks,* **vol. 4**, No. 3, May 1993.

Chapter 4

[1] Kandel, E. R. *Cellular Basis of behaviour*, San Francisco: W. H. Freeman, 1976.
[2] Ebbinghause, *Human Memory*, H. A. Ruger and C. E. Bussenius, trans. New York: Teachers College, 1913. Reprint. New York: Dover, 1964, Originally published in 1885.
[3] P. B. Post, "A lifelike model for association relevance", *Proc. Int. Joint Computer Conf. Artificial Intelligence*, May 1969.
[4] M. Hagiwara, "Knowledge Processing System using Multidirectional Associative Memory", *ICNN*, **vol 3**, Page 1304, 1995.
[5] J. R. Anderson, G. H. Bower, *Human Associative Memory*, John Wiley & Sons, 1973.
[6] D. O. Hebb, *The organisation of the behaviour*, McGill university, J. Wiley & sons, Inc. 1949, 8th edition, Oct 1966.
[7] C. N. Cofer, *The structure of Human Memory*, W. H. Freeman and company, The Pennsylvania state university, 1975.
[8] R. Galambos, *Glia, Neurons, and information storage*, from F. O. Schmitt, *Macromolecular specificity and biological memory*, The M.I.T Press, Cambridge, Massachusetts, 1962.
[9] R. Galambos, "A glia-neural theory of brain function," *Proc. Natl. Acad. SC. U. S.*, **47**, 129-136, 1961.
[10] Saffih Faycal, W. A. T. Wan Abdullah, Z. A. Ibrahim, A. Iftekhar, "Parallel Learning-Processing for Artificial Neural Networks Implementation," *Scientific International*, **10 (3)**, 1998, Presented in UPM, Kuala Lumpur, Malaysia, at ISO 98, 7-9 May, 1998.
[11] Wang, Y. F., Cruz, J. B., Jr., and Mulligan, J. H., Jr., "Two coding Strategies for bidirectional associative memory," *IEEE Trans. On Neural Networks*, **1(1)**, 81-92, 1990.

[12] G. Mathai, B. R. Upadhyaya, "Performance analysis and application of the bidirectional associative memory to industrial spectral signatures," *Proceedings of International Joint Conference on Neural Networks*, **vol. 1**, pp. 33-37, 1989.
[13] Bai-Ling Zhang, Bing-Zheng Xu, Chung-Ping Kwong, "Performance analysis of the bidirectional Associative Memory and an Improved Model from the Matched-Filtering Viewpoint," *IEEE Transactions on Neural Networks*, **vol. 4**, No. 5, September 1993.
[14] R. J. Marks II, L. E. Atlas, J. J. Choi, S. Oh, K. F. Cheung, and D. C. Park: "Performance analysis of associative memories with non-linearities in the correlation domain," *Applied Optics*, **vol. 27**, No. 14 /15 July 1988.

Chapter 6

[1] J. BHASKER, *A VHDL Primer*, Prentice Hall PTR, Englewood Cliffs, New Jersey 07632, 1995.
[2] J. R. *Armstrong, Chip-Level modelling with VHDL*, Prentice-Hall International, Inc, 1989.

Chapter 7

[1] Saffih Faycal, W. A. T. Wan Abdullah, Z. A. Ibrahim, "New Systolic Architecture for the PLP Artificial Neural Network Implementation Strategy," to be published.
[2] Kung. H. T, Why systolic architectures, *IEEE Computer*, 37-46, Jan 1982.
[3] Mario De Blasi, *Computer Architecture*, Translated by Charles Foot, Addison-Wesley Publish Company, 1990.
[4] Saffih Faycal, W. A. T. Wan Abdullah, Z. A. Ibrahim, "Encoding Comparing Technique for Interfacing Neural Networks Associative Memory," to be published.
[5] J. F. Fontanary, R. Koberle, "Neural Networks with transparent memory," *J. Phys.* A: Math. Gen., **21**, L259-L262, 1988.
[6] L. Personnaz et al., "Specification and Implementation of a Digital Hopfield-Type Associative Memory with on Chip Learning," *IEEE Trans on Neural Networks*, **3(4)**, pp 529-539, July 1992.
[7] Man Young Rhee, *Error Correcting Coding Theory*, McGraw-Hill 1989.
[8] M. H. Hassoun, *Fundamental of Artificial Neural Networks*, The MIT Press, Chapter 7, 1995.

Chapter 8

[1] T. Kurkawa, H. Yamashita, Bus connected network hardware system, *Electronics Letters*, **vol. 30**, No. 12, June 1994.

Chapter 9

[1] P. D. Tougaw, C. S. Lent and W. Porod, "Bistable Saturation in coupled quantum-dot cells," *J. Appl. Phys.* 74 (5), pp. 3558-2566, September 1993.
[2] H. Körner, G. Mahler, "Optically driven quantum networks: Applications in molecular electronics," *Phys. Rev.* B, 48 (4), pp. 2335-2346, July 1993.