# Digital Implementation of Artificial Neural Networks

By

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**Submitted to the Physics Department,
Faculty of Science for the Degree of:**

**Master of Science in Physics**

University of Malaya,

***1998***



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*In the Name of Allah the Most beneficent, the Most Merciful*

*For my Lord, Fur mein Gott, Pour Mon Dieu*

*Kepada Allah yang nikmatnya meliputi saya,*

*Saya semadikan tesis ini.*

*I would never forget you, whom I am ever missing, who taught me the love of science and its shining, you my beloved father, my first sign of life who tough me when alive the perseverance and patience. To your spirit and memory all my Doa and righteous deeds.*

*To my beloved mother who I will never be able to satisfy her deserved love and care.*

*To all of my family, my Brothers and Sisters.*

*To my beloved Land, Algeria, Land of Greatest Martyrs Chouhada may Allah bless them.*

*To Malaysia, the saved and welcome Land where I opened my eyes on science and technology.*

*To the Physics Department staff, from Prof. M. Rasat ex-head of Physics Department to Tuan Hj. Harun, Encik Ramly and Cik Habibah.*

*To all of you, I dedicate my thesis*

# Acknowledgement

The present thesis could not see the light of existence without the help of the creator of this wonderful universe to whom I will never be able to satisfy all his deserve of the thankfulness.

*"...O my Lord! so order me that I may be grateful for Thy favours, which thou hast bestowed on me and on my parents, and that I may work the righteousness that will please Thee: And admit me, by Thy Grace, to the ranks of Thy righteous Servants...".*[1]

Verse 19, AN-NAML

I would like to thank my supervisors Dr. W. A. T. Wan Abdullah, Dr Z. A. Ibrahim and Dr A. Iftekhar for their encouragement during the enrolment of my research and guidance of my project towards its best fulfilment. It is worthy mentioning the collaboration of the system administrator of the Faculty of Computer Science and Information Technology Puan M. Mohaidah and Professor Hj. Y. Mashkuri the head of the faculty, for their providence and assistance of VHDL Synopsis tools.

I am also grateful, to the IRPA for the financial support it provided through grant number 04-02-03-345 during the whole of my research

[1] Verse 19 of AN-NAML of the Holly Quran, translated by Yusuf Ali. See http://www.islam-quran.org/frame.htm.

# Abstract

This thesis is concerned with the philosophy and the strategies related to the digital implementations of artificial neural networks ANN. An open and deep insight of the biological origin of ANN as well as its tidy relation with physics through statistical mechanics and the Hopfield revolutionary concept of *computational energy* (See Ref [4] of Chapter 2) is given. The Very Large-Scale Integration VLSI implementation of ANN (mainly digital) with its diverse methodologies, strategies and goals are also discussed. The notion of parallelism that was the corner stone of the third chapter in the processing (or the hardware) point-of-view and is enhanced in the fourth chapter to introduce the parallel learning-processing PLP notion. The Printed Circuit Board PCB technique is applied for the implementation of PLP-based neuron Bidirectional Associative Memory BAM using the cad tool of *EEDIII* that simulates it and shows the technique limited capabilities. The powerful Very Hardware Description Language VHDL is introduced and used to implement more suitable versions of the previous circuit and other, to be downloaded on a Field Programmable Gate Arrays FPGA chips. The PLP neuron-based BAM implementation is enhanced further by the introduction of the encoding-comparing technique as a user interface with the network as well as the expandability technique based on the suggested systolic-like architecture. Finally, the bus-based architecture technique is presented for the implementation of the Hopfield ANN.

# Ikhtisar

Tesis ini adalah berkenaan dengan falsafah dan strategi yang berkaitan dengan implementasi rangkaian neuron rekaan RNR. Suatu kajian yang terbuka dan mendalam diberikan bagi sistem RNR berasaskan biologi serta kaitan rapinya dengan fizik melalui mekanik statistik dan revolusi konsep Hopfield bagi teraja komputeran (tengok Ref [4] dalam Bab 2).

Implementasi VLSI bagi RNR (berdigit) dengan percapahan motodologinya, strategi dan sasarannya juga di bentangkan. Kaedah keselarian yang merupakan 'petanda' di bab ke-4 dan sudut pemprosesan (atau secara *hardware*) dan ditingkatkan di bab-bab seterusnya bagi memperkenalkan kaedah pemprosesan pembelajaran selari PPS. Teknik papan litar tercetak PCB di gunakan bagi implementasi PPS pada ingatan. Sekutuan Dwiarah ISD dengan mengguna perisian EEDIII bagi membuat simulasi yang telah menunjukkan had kegunnannya. Kaedah VHDL iaitu Bahasa Huraian *hardware* di perkenalkan dan digunakan bagi implementasi versi yang bersesuaian bagi litar yang di sebut itu dan di *downloaded* pada chip implementasi *Field Programmable Gate Arrays* FPGA. Kaedah PPS ditingkatkan seterusnya dengan memperkenalkan teknik bandingan pengkodan sebagai perantaramukaan penguna dengan rangkaian dan juga teknik perkembangan berdasar atas senibina seperti *systolic* yang disaran. Teknik senibina berdasarkan bas di tunjukkan bagi implementasi RNR Hopfield mempergunakan bahasa pemprograman *hardware* yang disaran dengan kuat bagi implementasi litar kompleks berdigit seperti RNR berdigit.