Chapter 1

Introduction,

Objectives and Planing

1-1 Overview and Alternative

The objective of the thesis is the implementation of digital neural networks using two completely different methods, the classical Printed Circuit Board PCB technique and the hardware description technique using VHDL language. The use of the above techniques was not the main motivation of present work, although a comparison between them is presented, but rather it is the implementation of the *functional parallelism* notion in digital neural networks. We think that current implementations of artificial neural networks need other dimension to extend their *stagnant* limit before being spread world wide as intelligent devices. These stagnant aspects of the current implementations are reflected by the *low dynamicity degree* of the implemented devices. Indeed, the current artificial neural networks implementations consist of neuro-devices operating in two distinguished phases; the learning phase and the processing phase. Despite the alternative use of the same electronic unites to reduce the implementation expense, the dynamicity of the network still remains stagnant limiting therefore, the implementation flexibility to overcome the computational dynamics. If the implementation flexibility is enhanced neural network device will be able to realise a real-time intelligent-processing of a dynamical computational task and therefore to be self-adapted with dynamical systems. In this way, new strategy called Parallel Learning-Processing PLP mapping the above mentioned functional parallelism is proposed. In the PLP strategy, the neuron phase functionalities namely learning and processing of the Hebbian-based neural networks are paralleled. In order to strengthen the PLP and exploiting its similarity with the systolic arrays dynamics, a new architecture realising the expandability of a neural networks namely Bidirectional Associative Memory BAM based the PLP strategy is

proposed. Beside this architectural enhancement, an interfacing technique called Encoding-Comparing Technique ECT is suggested (and simulated) in order to create an interface between the network and its user. Finally, a network imitating the Ising model is realised. The network is based on the bus communication between a given number of neurons and an arbiter circuit, which will update only one neuron for each configuration. We think that such devices could be very important to simulate not only the Ising model but also to emulate the biological neural networks in which the symmetry of the synaptic strength is no more verified. As perspective implementations, we suggest the physical networks such as the *nanostructure* devices to be a future realisation for the implementation of artificial neural networks. This is a result of the *intelligent* laws governing the physical interactions mainly concerning the physical quantum systems such as the quantum dots. This implementation is, however, possible because of the above statement arguments, which are truly strong at least for theoretical modelling of artificial neural networks such as the Hopfield model (see ref. [1] of Chapter 2).

1-2 Planning & Presentation

The first chapter is an introduction to the foundations and historical origin of both biological and artificial neural networks beside their developments with quick insight on the Bidirectional Associative Memory BAM. In the next chapter, we present the importance of physics for the understanding of the artificial neural network dynamics mainly the Hopfield model through the statistical mechanics analysis. The third chapter is a description of the Very Large Scale Integration VLSI techniques for the implementation of ANN.

After these introductory chapters, the fourth chapter analyses the concept of Parallel Learning Processing PLP neuron with different arguments. In chapter five and six, the implementation of the PLP based BAM, using the PCB and VHDL description techniques, is presented. The seventh chapter is dedicated for the operational and architectural enhancement techniques of the BAM namely the Systolic-like architecture and the Encoding Comparing Technique ECT. The Last implementation of a bus-based architecture of the Hopfield neural network is proposed in chapter eight. Finally, general conclusion of the above implementations is formulated and new perspective and open problems are proposed.