RUJUKAN

[1] Cnet Hongkong Glossary, *Floating Point Unit*, http://hongkong1.cnet.com/Briefs/Glossary/Terms/fpu.html Cnet Hong Kong, Nov 1999.

[2] Intel Corporation, *High Performance Floating Point Unit*, http://homepage.eusica.fr/~frances/intel/procs/pentium/pptech/floatpt.html Intel Corporation, 1995

[3] Chuck Purdy, *Floating Point Unit*, http://www.whatis.com/fpu.htm whatis.com, Oct 1999

[4] G. Goto et. al, *A 4.1ns compact 54×54-bit Multilier Utilizing Sign-Select Booth Encoder*. IEEE J. Solid State Circuit, vol. 32, pp 1676-1682, Nov 1997.

[5] R. Woods and S. Masud. *Chip design for high-performance DSP*. Electronic & Communication Engineering Journal, pp 191-200, August 1998.

[6] M. Nagamatsu, S. Tanaka, J. Mori, K. Hirano and T. Noguchi, *A 15ns 32×32 bit CMOS Multiplier with Improved Parallel Structure*. IEEE J. Solid State Circuit vol. 25, pp 494-497, Apr. 1990.

[7] J. Mori et al, *A 10ns 54×54-bit Parallel Structured Full Array Multiplier With 0.5μm CMOS Tevhnology*. IEEE J. Solid State Circuit, pp 600-606, Apr 1991.

[8] G. Goto et al, *A 54×54-bit Parallel Structured Full Array Multiplier*. IEEE J. Solid State Circuit, vol 27, pp 1229-1236, Sept. 1992.

[9] N. Ohkubo et al, *A 4.4ns CMOS 54×54-bit multiplier using pass-transistor multiplexer*, IEEE J. Solid State Circuit, pp 251-257, vol. 30, Mar. 1995.

[10] M. Hanawa et al, *A 4.3ns 0.3μm CMOS 54×54-bit multiplier using precharged pass-transistor logic,* ISSCC Dig. Tech. Papers, pp 364-365, Feb. 1996.

[11] Y. Hagihara et al, *A 2.7ns 0.25μm CMOS 54×54-bit multiplier,* ISSCC Dig. Tech. Papers, pp 296-297 & 449, Feb. 1998.

[12] M. Santoro and M. Horowitz, SPIM: *A Pipelined 64×64bit Iterative Multiplier.* IEEE J. Solid State Circuit vol. 24, pp 487-493, Apr. 1989.

[13] Israel Koren, *Computer Arithmetic Algorithms.* Prentice Hall, 1993.

[14] Amos R. Omondi, *Computer Arithmetic System : Algorithms, Architectures And Implementation.* Prentice Hall, 1994.

[15] Wayne Wolf. *Modern VLSI Design: Systems on Silicon.* 2nd Edition, Prentice Hall, 1998.

[16] C. S. Wallace, *A suggestions for fast multipliers.* IEEE Trans. Electron Computers. vol. EC-13, pp 14-17, Feb. 1964.

[17] Hema Dhanesha et. al, *Array-of-array architecture for parallel floating point multiplication.* Advanced Research in VLSI, pp 150-157, March 1995.

[18] J. F. Cavanagh, *Digital Computer Arithmetic: Design and Implementation.* New York: Mc. Graw Hill, 1984.

[19] A. Wu, C.K. Ng and K.C Tang , *Modified Booth Pipelined Multiplication.* Electonic Letter. vol. 34, pp 1179-1180, June. 1998.

[20] Shen-Fu Hsiao, Ming-Roun Jiang and Jia-Sien Yeh, *Design of high-speed low-power 3-2 counter and 4-2 compressor for fast multipliers.* Electronic Letter. vol. 34, pp 341-343, Feb. 1998.

[21]   Stuart F. Oberman and Michael J. Flynn, *Design Issues in Division and Other Floating Point Operations*: IEEE Transsactions On Computers vol. 46, pp 154-161, Feb. 1997.

[22]   Nobuhiro Ide et al, *A 320-MFLOBS CMOS Floating Point Unit For Superscalar Processors*. IEEE J. Solid State Circuit, pp 352-360, Mar 1993.

[23]   Daniel D. Gajski. *Principles of Digital Design*. Prentice Hall, 1997.

[24]   Daniel C. Biederman and Esther T. Ososanya, *Design of a neural network-based digital multiplier*, IEEE ASSP, pp 320-326, 1997.

[25]   Lin, Ta-Cheng. *Digital system synthesis with complex functional units*. PHD Dissertation, pp 1-12, Electrical and Computer Engineering, Virginia Tech. University, 1998.

[26]   *Welcome To VHDL-AMS.COM*, http://www.vhdl-ams.com/   VHDL-AMS.COM, 1999.

[27]   John F. Wakerly. *Digital Design. Principles and Practices*. pp882-890 & pp895-902, 3rd Edition, Prentice Hall, 2000.

[28]   *VHDL Compiler Reference Manual*. pp(1-2)-(1-12), Version 1997.08, Synopsys, August 1997.

[29]   K.C. Chang. *Digital Design and Modeling with VHDL and Synthesis*. Chapter 1, IEEE publication 1998.

[30]   Peter J. Ashenden, *The Designer's Guide in VHDL*. Chapter 1, pp341 & pp608-609. Morgan Kaufmans, 1996.

[31]   Douglas L. Perry, *VHDL*. Chapter 1, 2nd Edi. New York: McGraw Hill.

[32]   *Guidelines and Practices for Successful Logic Synthesis*, pp(3-1)-(3-22) Version 1997.08 Synopsys, August 1997.

[33]   *Synopsys DesignWare DataBook* pp(3-1)-(3-54), Version 3.1a, Mac 1994.

[34]   K. Hwang, *Computer Arithmetic: Principles, Architecture and Design.* pp167-168, New York: Wiley, 1979.

[35]   *XC4000XL/XLA Series FPGAs,* http://www.xilinx.com/products/xc4000XLA.html XILINX.COM 1999.

[36]   Synopsys *VSS Family Tutorial.* Pp4-2, Version 3.1a, March 1994.

[37]   Pedro Soria Rodriguez, *Applet flo2bin,*
         http://ece.wpi.edu:8080/infoeng/java/FLOAT_BIN_CONV/flo2bin.html Feb. 1998

[38]   *Synopsys FPGA Express*, Chapter 3, Getting Started. Dec. 1997

[39]   *Design Compiler Tutorial*, Chapter 5, 6&7, Version 1997.08 Synopsys. August 1997.

[40]   *Design Analyzer Reference Manual*, Chapter 2, Version 1997.08 Synopsys, August 1997.

[41]   *Quick Start Guide for Xilinx Alliance*, Chapter 3, Series 1.5. 1998

[42]   *FPGA Compiler User Guide*, pp(7-17)-(7-18), Version 1997.08 Synopsys, August 1997.

[43]   Barry Fagin and Cyril Renard. *Field Programmable Gate Array and Floating Point Aritmetic.* IEEE Trans. On VLSI Systems. pp365-367 Vol 2, No.3 Sept 1994.

[44]   Jasvinder Pal Singh et. al, *A multiplier generator for Xilinx FPGA's.* 9th International Conference on VLSI Design, pp 322-323, Jan 1996.

[45]   Rao R. Tummala and Vijay K. Madisetti. *System on Chip or System on Package. IEEE Design & Test Computer.* pp48-54, April-June 1999.